Contents

1. Summary

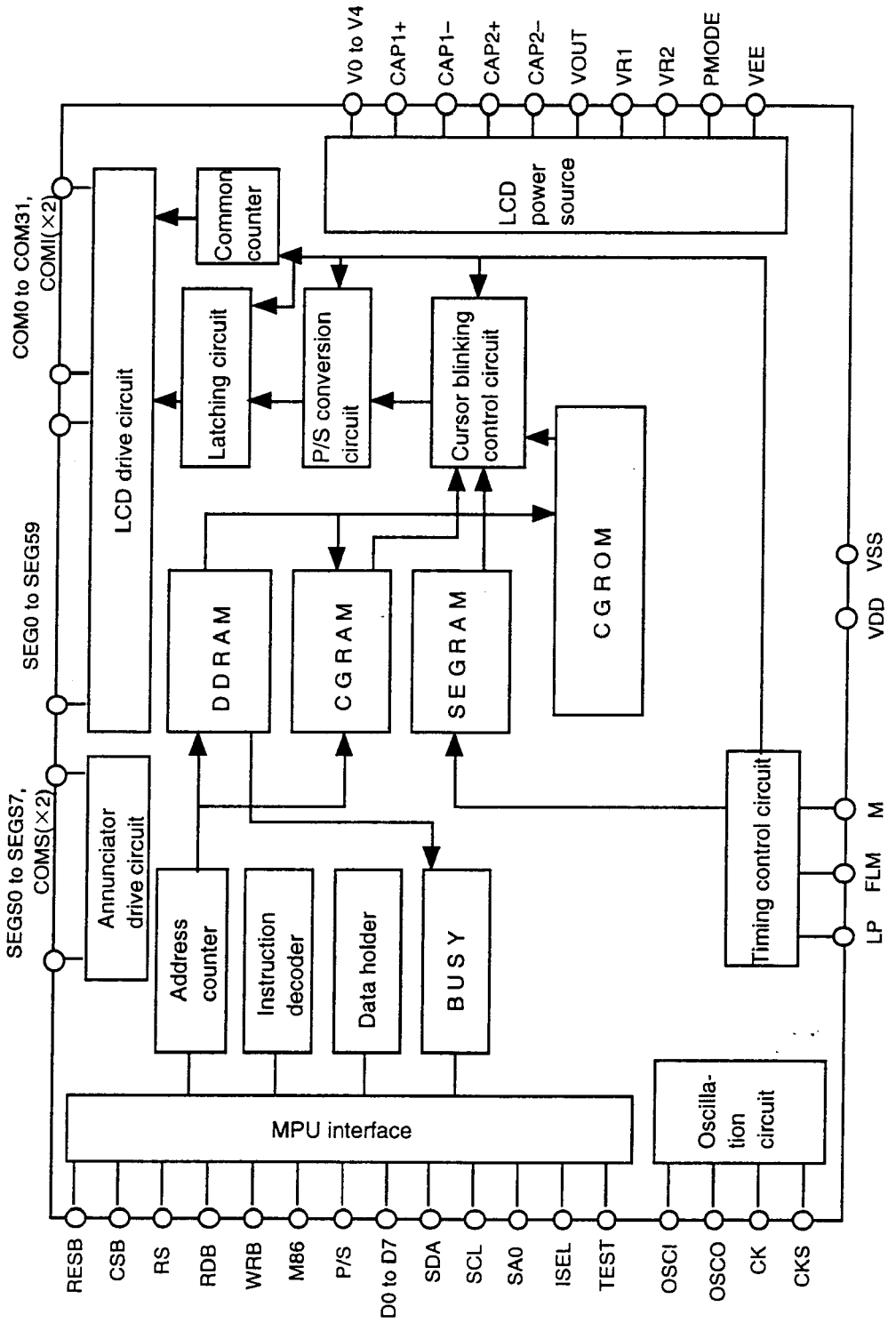
The LH1592 is a dot matrix LCD driver with a built-in character ROM, which can be directly connected to a microcomputer via a bus.
Eight-bit or serial data sent by a microcomputer is used to generate LCD drive signals for displaying characters.
Incorporating the character ROM which has font characters configured in the format of 5 x 8 dots and the character RAM which allows the user to define characters, the LH1592 provides a higher freedom of display.
Since the LH1592 has 60 output pins for a segment driver circuit and output pins for a common driver circuit in a single chip, a display system for 12 characters x 4 lines can be implemented easily.
Because of its lower power consumption and wider operating voltage range, the LH1592 makes itself most suited for an LCD unit on battery-operated portable information-oriented equipment.

2. Features

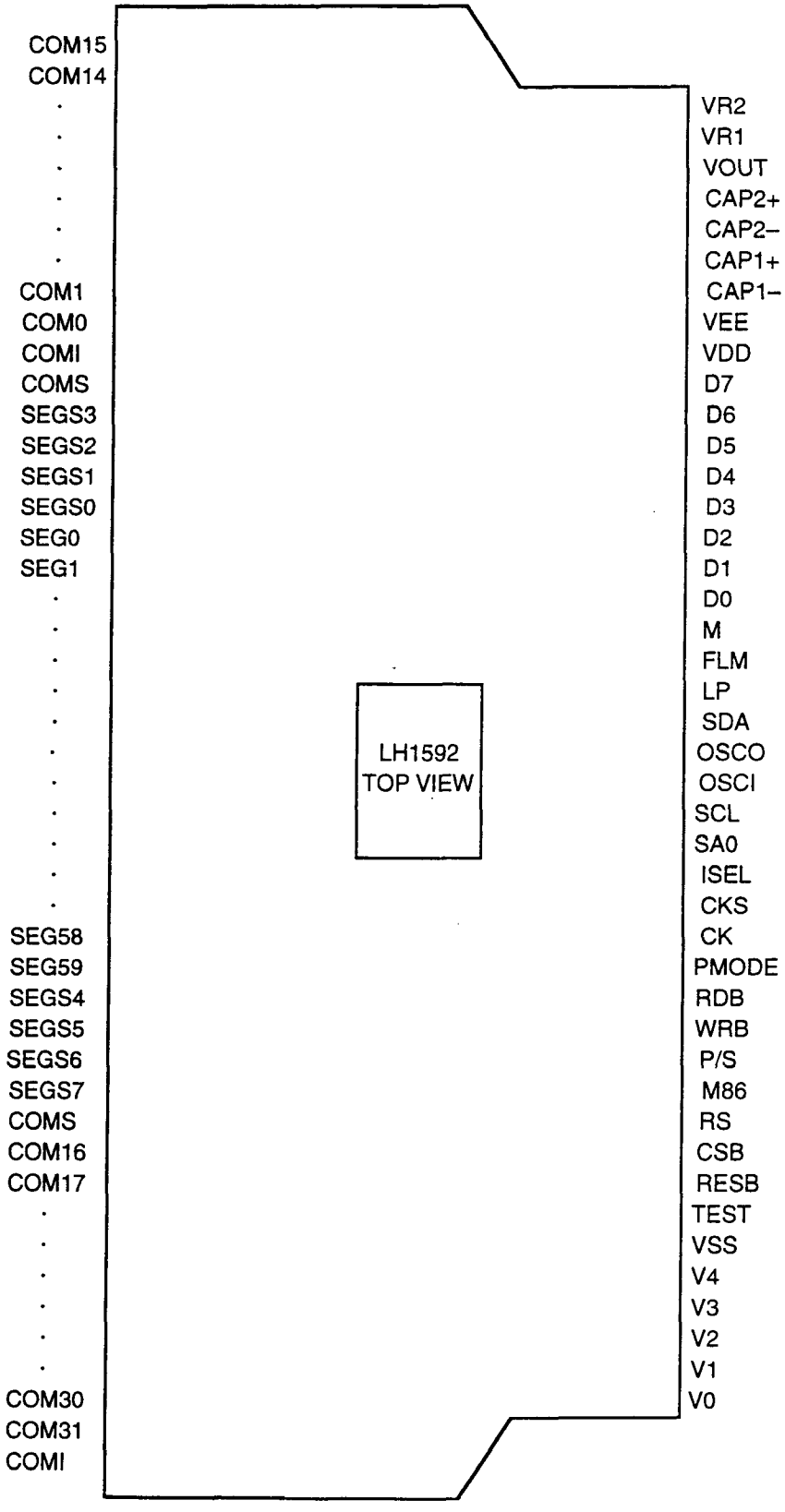
- Built-in CGROM: 240 characters (5×8×240 = 9600 bits)
- Built-in CGRAM: 8 characters (5×8×8 = 320 bits)
- Built-in SEGRAM: 60 segments (12×7 = 84 bits)
- Built-in display data RAM: 48 characters (48×8 = 384 bits)
- Format of font character: 5×8 dots including 1 dot which also serves for display a cursor
- General-purpose 8-bit MPU interface:
  Allows direct connection with the 80 or 68-family MPU over a bus
- Allows serial interfacing (* I^2CBUS format)
- Display duty ratio: 1/24, 1/25, 1/32, 1/33
- Command features
  - Display of 3 or 4 lines by 12 characters
  - Display ON/OFF
  - Normal/reverse display control
  - Busy flag read-out
  - Cursor display
  - Blinking (per character or per line)
  - Display double fonts lengthwise
  - Setting up shift direction of common outputs
  - Power saving mode
- Built-in LCD drive power circuit
  - Built-in Booster circuit: Enables two or three times higher voltage
  - Built-in voltage conversion circuit: Generates LCD drive voltage (V0, V1, V2, V3, or V4) based on stepped-up voltage.
  - Bias ratio of built-in power source: 1/6
  - Built-in electronic control: Controllable in 16 steps
- Power source: Supply voltage for logic system: +2.4 V to +5.5 V
  LCD drive voltage: +4.0 V to +11.0 V
- Operating temperature: –30 to +85 ℃
- Packaging: TCP-147-pin
- CMOS silicon gate process (p-type silicon circuit substrate)
- Not designed or rated as radiation hardened

* I^2CBUS is a PHILIPS's registered trademark

3. Block Diagram



4. Pin Configuration



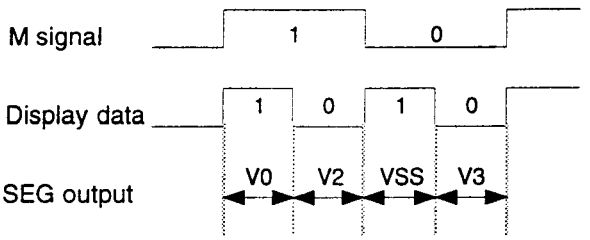
Note: This layout does not restrict the outer dimensions of the TCP.

5. Description of Pins

5.1 System bus pins

Symbol	I/O	Pin Description
RESB	I	Used to reset the LH1592. The LH1592 is reset when "0" is entered.
D0 to D7	I/O	Used as an 8-bit bi-directional data bus, which is connected to data bus in 8-bit MPU
CSB	I	Used to enter chip select signal. Normally, address bus signal is decoded and then entered.
RS	I	Used to identify data sent by MPU at D0 to D7.
RDB (E)	I	• When connected to 80-family MPU: Used to connect RDB signal for 80-family MPU. When this signal becomes "L", data bus in the LH1592 enters the output mode. • When connected to 68-family MPU: Used to connect enable clock E signal for 68-family MPU. When this signal becomes "H", LH1592 is made active.
WRB (R/W)	I	• When connected to 80-family MPU: Used to connect WRB signal for 80-family MPU. When this signal becomes "L", LH1592 is made active and any signal over data bus is captured at leading edge of WRB signal. • When connected to 68-family MPU: Used to connect read/write control signal for 68-family MPU. R/W="H" : READ R/W="L" : WRITE
M86	I	Used to select MPU interface type. Fixed at either M86 = "H" for 68-family interface or M86 = "L" for 80-family interface.
SDA	I/O	I/O for the I2CBUS data line when serial interface is selected. Must be connected to a positive supply via pull-up resistor.
SCL	I	Input for the I2CBUS clock signal when serial interface is selected. Must be connected to a positive supply via pull-up resistor.
P/S	I	Used to switch between parallel and serial interface. P/S = "H" for parallel interface. Fixes SDA and SCL at "H" or "L". P/S = "L" for serial interface. Fixes D7 to D0 at HI-Z; RDB and WRB at "H"
SA0	I	Used for LSB bit of slave address for I2CBUS(7 bits width). Mustbe fixed at "H" or "L".
ISEL	I	Used to identify I2CBUS. When use I2CBUS,need to fix "H". If ISEL is set "L", LH1592 operation is not warranty
TEST	I	Used for testing purpose. Must be fixed at "L".

5.2 LCD drive pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Pin Description</th></tr>
<tr><td>LP</td><td>O</td><td>Used as latch signal output pin for display data. Outputs LCD drive signal when LP signal fall.</td></tr>
<tr><td>FLM</td><td>O</td><td>Used as LCD sync signal (first line marker) output pin.</td></tr>
<tr><td>M</td><td>O</td><td>Used as alternation signal output pin for LCD drive output.</td></tr>
<tr><td>COM0
to COM31</td><td>O</td><td>Used as common driver output pin for LCD drive (for character display).
Among V0, V1, V4, and VSS levels, one level is selected depending on the combination of scanned data and M signal.
<table>
<tr><th>Data</th><th>M</th><th>Output level</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>COMI</td><td>O</td><td>Used as common output pin for marker display.
Becomes common output pin when duty + 1 (PLUS) command is executed.
Having two output pins for COMI , they output same level. it is able to select output pin for COMI when wiring pattern.
<table>
<tr><th></th><th>Duty+1 ON</th><th>Duty+1 OFF</th></tr>
<tr><td>COMI state</td><td>COM32(when displaying 4lines),
COM24(when displaying 3lines)</td><td>V0 or V4</td></tr>
</table></td></tr>
<tr><td>SEG0
to SEG59</td><td>O</td><td>Used as segment driver output pin for LCD drive.
Among V0, V2, V3, and VSS levels, one level is selected depending on the combination of M signal and display data.

</td></tr>
<tr><td>COMS</td><td>O</td><td>Used as common driver output pin for static LCD drive (for annunciator display).
Having two output pins for COMS, they output same level. it is able to select output pin for COMS when wiring pattern.
When DA = "0", outputs VSS level.</td></tr>
<tr><td>SEGS0
to SEGS7</td><td>O</td><td>Used as segment driver output pin for static LCD drive (for annunciator display).
Among VDD and VSS levels, one level is selected depending on the combination of COMS signal and display data.
When DA = "0", outputs VSS level.</td></tr>
</table>

5.3 Pins for oscillation circuit

Symbol	I/O	Pin Description
OSCI	I	Used as oscillation circuit input pin (Feedback resistor must be inserted between this pin and OSCO).
OSCO	O	Used as oscillation circuit output pin. The CK pin must be fixed at VSS if oscillation circuit is used as source oscillation clock.
CK	I	Used as external clock input pin. The OSCI pin must be fixed at VSS if this pin is used for original oscillation input.
CKS	I	Used as external clock select pin. CKS = "H": External clock is input at the CK pin. CKS = "L": Oscillation circuit using the OSCI and OSCO pins is used.

5.4 Power supply pins

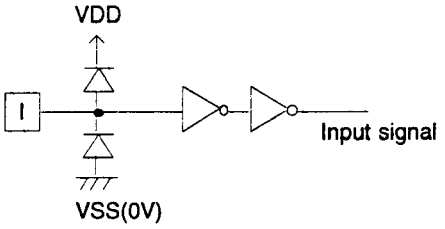
Symbol	I/O	Pin Description
VDD	Power source	Used as logic system power pin, which must be connected to +2.4 to +5.5 V.
VSS	Power source	Used as ground pin, which must be connected to 0 V.
V0 V1 V2 V3 V4	Power source	Used as bias power pin for LCD drive voltage. • When using an external power supply,convert impedance by using resistance-division of LCD drive power supply or operation amplifier before adding voltage to the pins. • When using the external power supply,maintain the following power supply conditions. VSS<V4<V3<V2<V1<V0 • When the power supply circuit is ON, LCD drive voltage of V0 to V4 are generated by the built in booster and voltage converter. • When using the built-in power supply,be sure to connect each capacitor between V0 to V4 and VSS.

5.5 LCD power circuit pins

symbol	I/O	Pin Description
CAP1+	O	Used to connect positive side of capacitor for built-in booster circuit. A capacitor must be connected between this pin and the CAP1- pin.
CAP1-	O	Used to connect negative side of capacitor for built-in booster circuit. A capacitor must be connect between this pin and the CAP1+ pin.
CAP2+	O	Used to connect positive side of capacitor for built-in booster circuit. A capacitor must be connect between this pin and the CAP2– pin.
CAP2-	O	Used to connect negative side of capacitor for built-in booster circuit. A capacitor must be connect between this pin and the CAP2+ pin.
VEE	I	Used to apply voltage for generating booster voltage. Normally this pin must be set at the same level as at the VDD pin.
VOUT	O	Used as output pin when built-in booster circuit is used . A capacitor must be connected between this pin and the VSS pin. If only voltage conversion circuit is used, voltage must be input so that the condition of VOUT > V0 is satisfied.
VR1	I	Used as input pin for voltage conversion circuit. Voltage must be input between the VOUT and VSS pins by dividing voltage by resistors, and must be input so that the condition of VR1≧VR2>4.0 V is satisfied.
VR2	I	Used as input pin for voltage conversion circuit. Voltage must be input between the VOUT and VSS pins by dividing voltage by resistors, and must be input so that the condition of VR1≧VR2>4.0 V is satisfied.
PMODE	I	Used as LCD power control pin. The operation condition of power circuit must be selected using the combination of the PMODE pin and the power circuit ON/OFF command (PON).

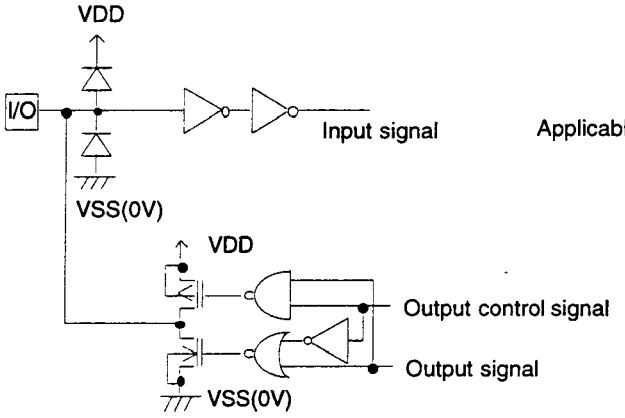
5.6 Input/output circuit types

(a) Input circuit 1



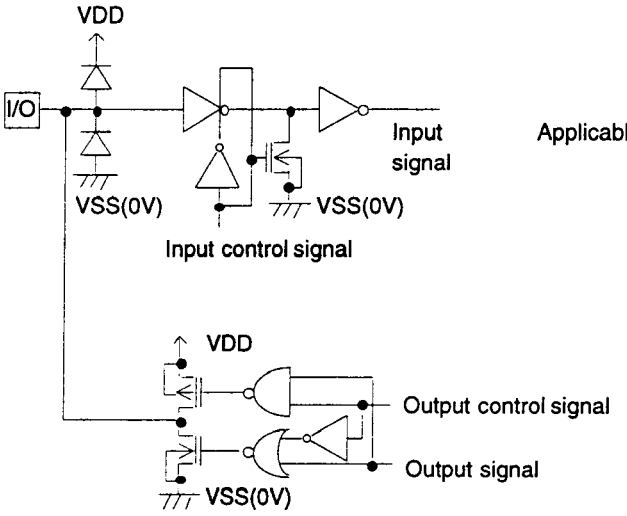
Applicable pins: CSB, RS, RDB, WRB, M86, P/S, SCL, SA0, ISEL, OSCI, CK, CKS, PMODE, RESB, TEST

(b-1) Input/output circuit 1



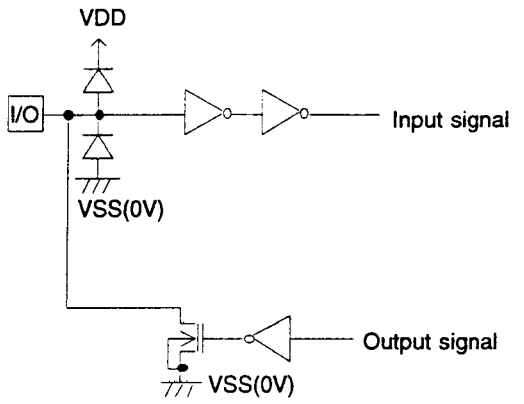
Applicable pins: OSCO

(b-2) Input/output circuit 2



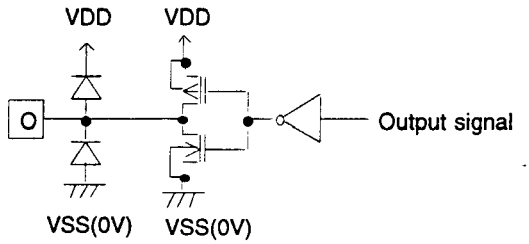
Applicable pins: D0 to D7

(b-3) Input/output circuit 3



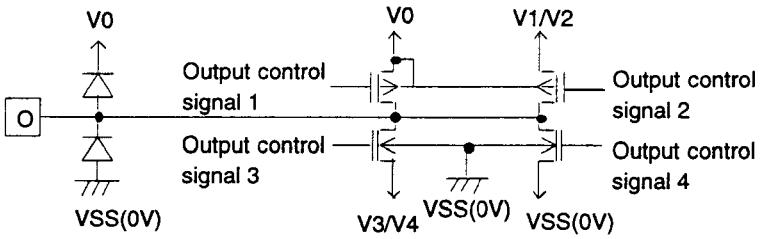
Applicable pins: SDA

(c) Output circuit



Applicable pins: LP, FLM, M
SEGS0 to SEGS7,
COMS

(d) LCD drive output circuit



Applicable pins: SEG0 to SEG59,
COM0 to COM31,
COMI

6. Description of Functions

6.1 Interface type selection

The LH1592 performs data transfer via the 8-bit data bus or the serial data input (the SDA or SCL pin). The parallel or serial interface is selected by setting the polarity of the P/S pin to "H" or "L".

P/S	I/F type	CSB	RS	RDB	WRB	M86	SDA	SCL	Data bus
H	Parallel	CSB	RS	RDB	WRB	M86	—	—	D0 to D7
L	Serial	—	—	—	—	—	SDA	SCL	—

6.2 Parallel input

The LH1592 allows parallel data transfer by directly connecting the data bus to an 8-bit MPU if the parallel interface is selected with the P/S pin.
For this 8-bit MPU, the 80-family or 68-family MPU type interface can be selected with the M86 pin.

M86	MPU type	CSB	RS	RDB	WRB	D0 to D7
H	68-family MPU	CSB	RS	E	R/W	D0 to D7
L	80-family MPU	CSB	RS	RDB	WRB	D0 to D7

6.3 Data identification

The LH1592 identifies data types over the 8-bit data bus by combinations of RS, RDB, and WRB signals.

	68-family	80-family		Function
RS	R/W	RDB	WRB	
0	1	0	1	Reads out busy flags
0	0	1	0	Writes commands
1	1	0	1	Reads out RAM data
1	0	1	0	Writes RAM data

6.4 Serial interface

The serial interface for the LH1592 is I2CBUS format.
I²CBUS is for bidirectional,two-line communication between different ICs or other modules.
LH1592 always operated for Slave device, Sending data start and stop is controlled by Start/Stop bit which are sent by Master device.
* I²CBUS is a PHILIPS's registered trademark

6.5 Busy flag

When the busy flag is "1", this indicates that the LH1592 is internally operating. In this state, the LH1592 does not accept the next instruction. As shown in the instructions table, the busy flag is output to the data bus D7 when RS is "0" or R/W is "1" (for the 68-family interface), and when RS is "0" or RDB is "0" (for the 80-family interface). The busy flag is generated only when the display clear command or the ACL command is executed. It must be checked that the busy flag is "0" before the next instruction can be executed.

6.6 Address counter (AC)

The address counter (AC) is used to address the DDRAM, CGRAM, or SEGRAM. When the addressing instruction is written into the AC, the address information is transferred to the AC. Simultaneously, the instruction also determines which RAM is to be selected among the DDRAM, CGRAM, and SEGRAM. After data is written into (read out into) the DDRAM, CGRAM, or SEGRAM, the AC is automatically counted up or down by one. As shown in the instructions table, the AC outputs data to the data buses D6 to D0 when RS is "0" or R/W is "1" (for the 68-family interface).

6.7 Display data RAM (DDRAM)

The DDRAM stores display data presented with 8-bit character codes. Its capacity is 48 characters in the format of 8 bits.

6.8 Character generator ROM (CGROM)

The CGROM generates 240 different character patterns in the format of 5×8 dots from 8-bit character codes.

6.9 Character generator RAM (CGRAM)

The CGRAM allows you to freely overwrite characters with your program. Eight different types of characters can be written by the format of 5×8 dots.

6.10 Segment RAM (SEGRAM)

The SEGRAM allows you to freely control icons and marks with your program. When the COMI outputs the select signal, the data stored in the SEGRAM is read out to display 60 segments.

6.11 Timing generator circuit

The timing generator circuit generates the timing signals to operate the internal circuits including the DDRAM, CGROM, CGRAM, and SEGRAM as well as those for segment and common driver outputs. Read-out of the display data to the LCD drive circuit is completely independent of MPU. Therefore,MPU that has no relationship the read-out operation of the display data can access.

6.12 Cursor blinking control circuit

This circuit generates the cursor, the blinking cursor, or the reverse-display cursor. The cursor or the blinking cursor appears in the digit that corresponds to the address in the DDRAM which was specified in the address counter.

6.13 Oscillation circuit

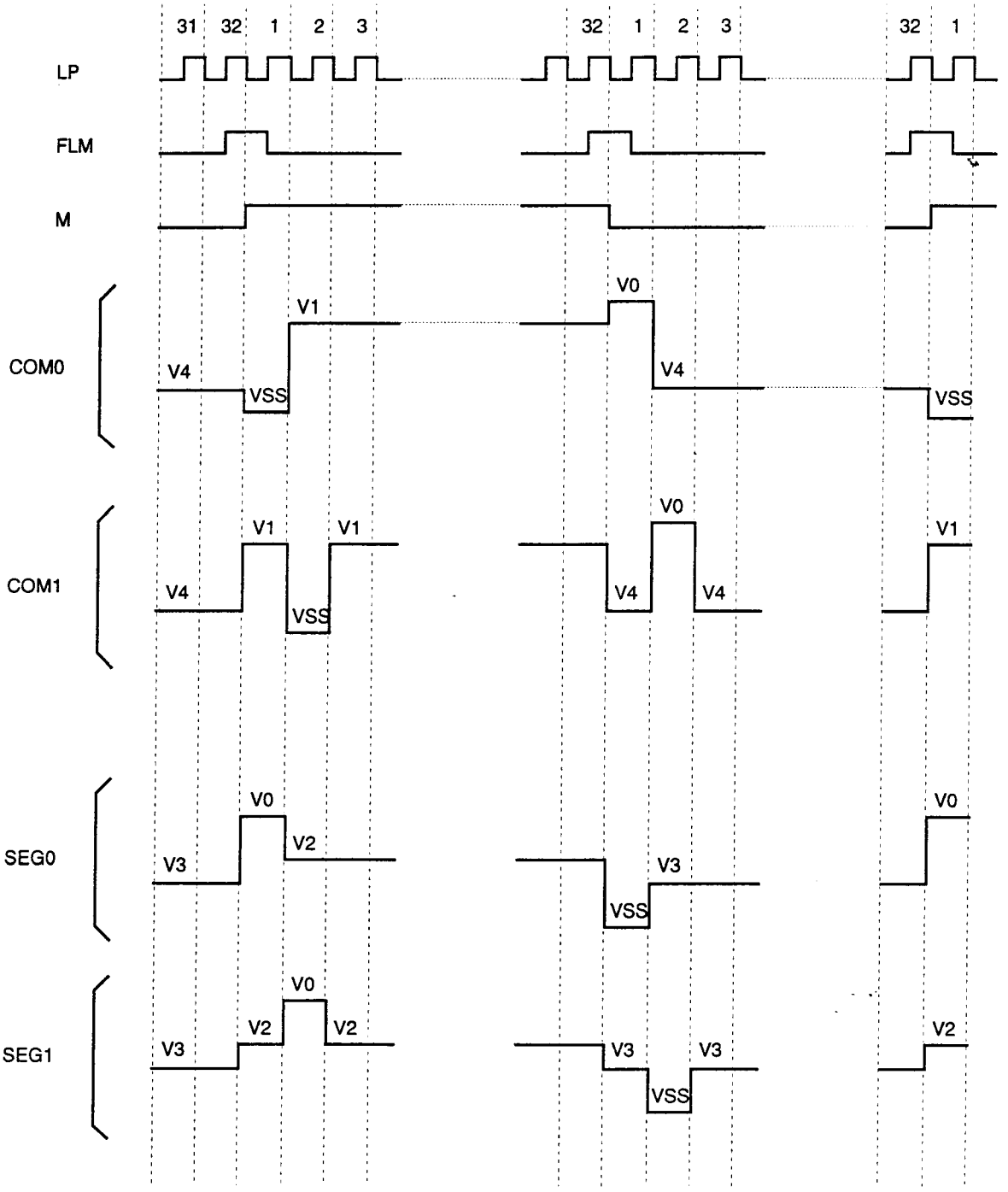
This is the CR oscillation circuit which controls the oscillation frequency with feedback resistor Rf. This circuit is used as the source of display timing signals and the boost clock for the Booster circuit.
If external clock is used,maintain OSCI pin at VSS and OSCO pin open(NC), and feed the clock to CK pin. The duty cycle of the external clock must be 50%.
The CKS pin is used to switch between the oscillation circuit and the external clock input.

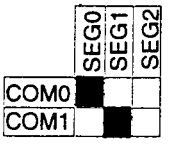
CKS	Oscillation circuit	External clock
"L"	Enabled	Disabled
"H"	Disabled	Enabled

6.14 LCD driver circuit

This is the drive circuit which generates 4-value levels for LCD drive. It consists of 33 common drivers and 60 segment drivers.
Character data is transferred by 60 bits from the CGROM or the CGRAM to the segment driver circuit. The combination of the transferred display data and the M signal is used to output LCD drive voltage.
Among the common outputs, one output (COMI) is used to marker display. The common driver circuit has a shift register and sequentially outputs common scan select signals.

6.15 LCD driver output timing





6.16 Annunciator circuit

This is the drive circuit which generates 2-value levels for static LCD drive. This circuit provides displaying annunciators for Icons or Marks. It consists of common drivers (COMS×2) and 8 segment drivers(SEGS0 to SEGS7). Among VDD amd VSS levels, one level is selected for static LCD drive. When this circuit is not displaying announciator, it outputs VSS level.

6.17 Power supply circuit

The power supply circuit generates the voltage required for LCD drive. It consists of a booster circuit, an electronic volume, and a voltage conversion circuit. High voltage boosted by the booster circuit is input to the voltage conversion circuit so that the necessary voltages for LCD drive (V0, V1, V2, V3, and V4) are generated.
If the number of pixels on your LCD panel is large, i.e., the display capacity is large, the built-in power circuit should not be used for driving that LCD panel. If used, this could greatly deteriorate the display quality. In this case, an external power source should be used.
The power circuit is controlled with the power circuit ON/OFF command (PON). When the built-in power circuit is off, the booster circuit and the voltage conversion circuit are also off.
If an external power source is used, LCD drive voltages V0, V1, V2, V3, and V4 must be externally supplied with the built-in power circuit off; the CAP1+, CAP1–, CAP2+, CAP2–, VOUT, VEE, VR1, and VR2 pins must be opened; and the PMODE pin must be connected to the VSS pin.
The functions of the power circuit can be selected depending on the status of the PMODE pin. Some functions of the external power source and the built-in power source can be combined to use together.

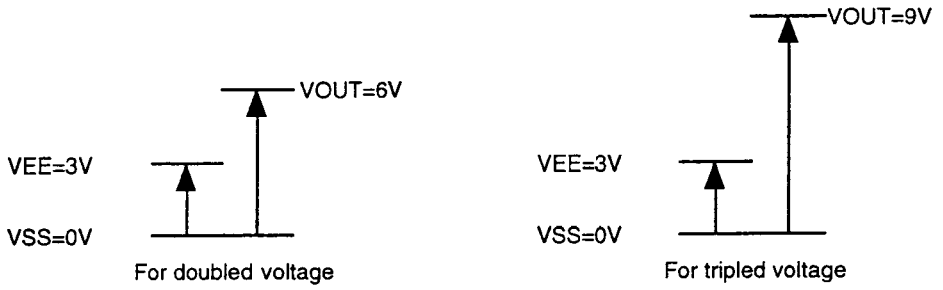
PON	PMODE	Booster circuit	Voltage conversion circuit	External voltage input	Remarks
0	0	Disabled	Disabled	V0, V1, V2, V3, and V4 are supplied.	*1
0	1	Disabled	Disabled	V0, V1, V2, V3, and V4 are supplied.	*1
1	0	Enabled	Enabled	—	
1	1	Disabled	Enabled	VOUT, VR1, and V2 are supplied.	*2

*1: The power circuit does not operate. Therefore, open the CAP1+, CAP1–, CAP2+, CAP2–, VOUT, VEE, VR1, and VR2 pins; and externally supply LCD drive voltages.

*2: The Booster circuit does not operate. Therefore, open the CAP1+, CAP1–, CAP2+, CAP2–, and VEE pins; supply power for the voltage conversion circuit at the VOUT pin; and supply reference voltage for LCD drive at the VR1 and VR2 pins.

6.18 Booster circuit

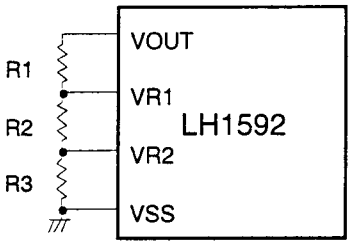
The capacitor C1 is connected between the CAP1+ and CAP1–, between the CAP2+ and CAP2–, and between the VOUT and VSS so that the electric potential between the VEE and VSS is tripled and then output at the VOUT pin. For the doubled electric potential, the capacitor between the CAP2+ and CAP2– is removed from the above connections and the CAP1+ and CAP2+ are short-circuited. Then the doubled voltage can be obtained at the VOUT pin.
The booster circuit uses the clock signal from the oscillation circuit or the CK pin as the booster signal. This requires that the oscillation circuit is operating or that the clock signal is input at the CK pin.
You must take care that the output level at the VOUT pin does not exceed the recommended maximum operating voltage (11.0 V) when the voltage is doubled or tripled. If this value is exceeded, the operation of the LH1592 is not warranty.



For doubled voltage For tripled voltage

6.19 Voltage control circuit

The boosted voltage at the VOUT pin is connected to the VR1 and VR2 pins and then the LCD drive voltages (V0, V1, V2, V3, and V4) are generated via the voltage conversion circuit. The input level at the VR1 and VR2 must meet the electric potential condition of VR1 > VR2. The built-in electric volume divides the electric potential between the VR1 and VR2 into 16 segments. Since the VR1 and VR2 pins have high input impedance, the input voltage levels at the VR1 and VR2 are determined by the resistance ratio of R1, R2, and R3. The current flowing between the VOUT and VSS pins is determined by the combined resistance of R1, R2, and R3.
Therefore, R1, R2, and R3 must be selected in accordance with the above current as well as the input voltage levels at the VR1 and VR2.
The boosted voltage at the VOUT pin originates from the voltage supplied at the VEE pin. Thus, the DC path current generated with R1, R2, and R3 connected between the VOUT and VSS pins is consumed as consumption current at the VEE pin. The electric current value three times larger than the DC path current generated between the VOUT and VSS pins when the voltage is tripled is added as consumption current at the VEE pin (two times larger current is added for doubled voltage). You must take sufficient care that the input levels at the VR1 and VR2 pins do not fluctuate with external noise.



Example of voltage control circuit

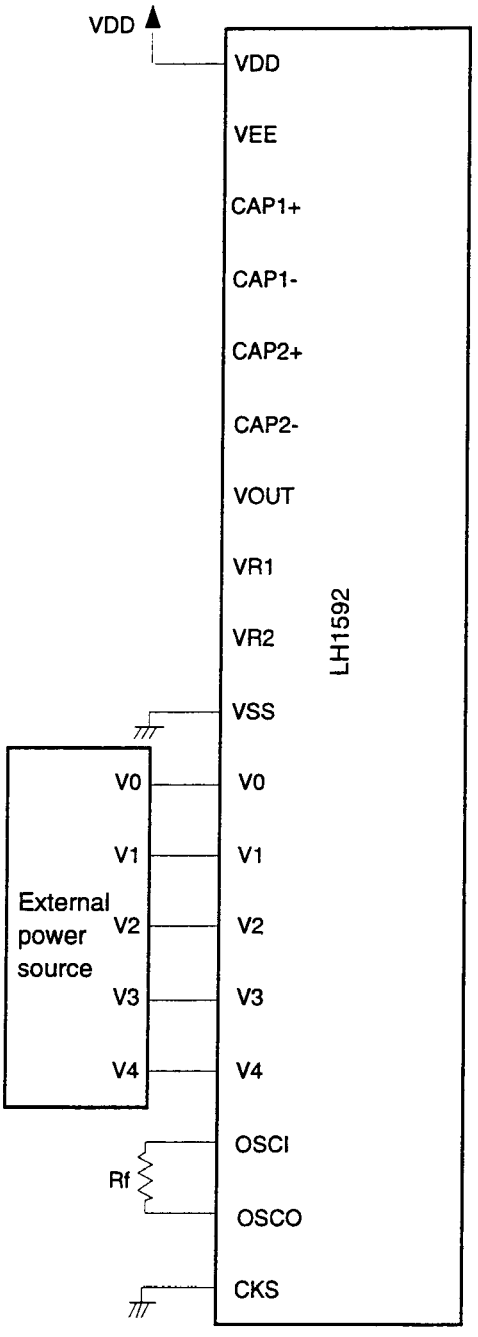
6.20 Electronic volume

The voltage conversion circuit incorporates an electronic volume, which allows the LCD drive voltage level V0 to be controlled with a command and also allows the tone of LCD display to be controlled.
If 4-bit data is stored in the register of the electronic volume, one level can be selected among 16 voltage values for the LCD drive voltage V0.
The voltage control range of the electronic control is determined by the input voltage levels at the VR1 and VR2. This means that the voltage range of (VR1 - VR2) is the controllable voltage range of the electronic volume. The electric potential relation between the VR1 and VR2 pins must be VR1>VR2. The input voltage levels at the VR1 and VR2 pins must be selected in accordance with the voltage levels to be obtained with the electronic volume.

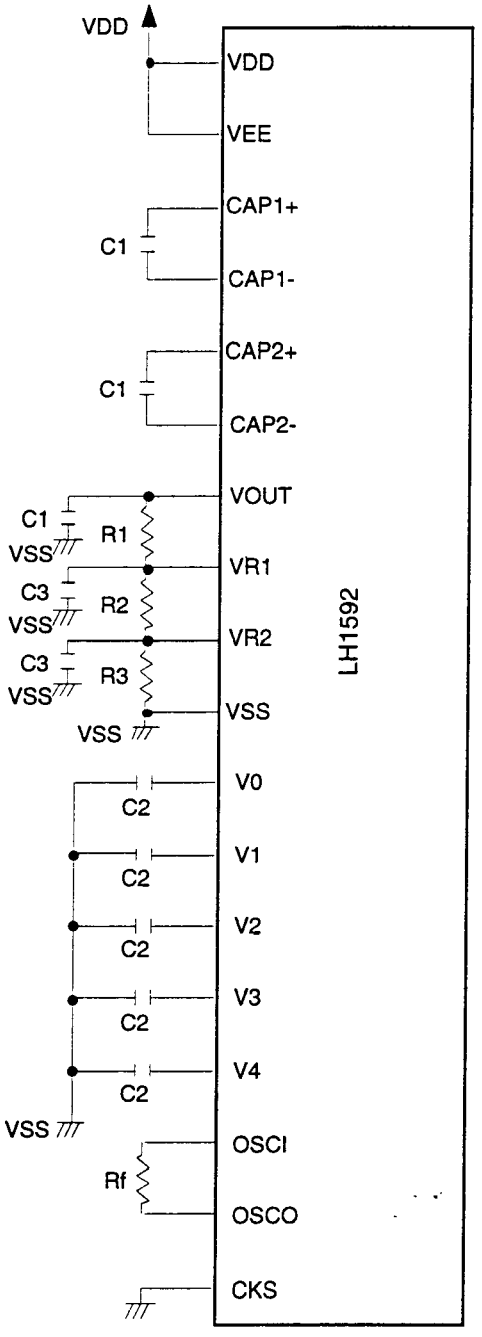
6.21 LCD drive voltage generation circuit

The voltage conversion circuit incorporates a voltage generation circuit, which divides the electric potential at the V0 pin with resistors to generate the electric potentials V0, V1, V2, V3, and V4 which are required for LCD drive. The LCD drive voltage bias for the LH1592 is fixed at 1/6.
If the built-in power source is used, the capacitor C2 for voltage stabilization must be connected to the LCD power pin. The constant of the capacitor C2 should be selected by using the LCD panel to display data.
In order to stabilize the input voltages at the VR1 and VR2, the capacitor C3 must be connected for the actual system by selecting its value as appropriate.

6.22 Example of power circuit connection



When built-in power circuit is not used



When built-in power circuit is used

* Recommended values

C1	1.0 to 5.0 µF
C2	1.0 to 2.0 µF
Rf	910 kΩ
R1+R2+R3	2.0 to 4.0 MΩ

6.23 Resetting function

The LH1592 can be initialized by setting the RESB pin to the "L" level. Normally, the RESB pin is connected to the reset pin on the MPU so that the LH1592 can be initialized together with the MPU. When the LH1592 is turned on, the resetting must be performed.

Item	Pin Description
Function set	RE = 0: Writes to expanded register disabled. BE = 0: SEGRAM blink off DUB = 0: Normal display mode. (Displaying double fonts lengthwise OFF) DL0, DL1 = (0, 0)
Entry mode set	I/D = 1: Increments by one S = 0: No shift occurs.
Display mode set	SHIFT = 0: Scan the shift direction from COM0 to COM31. NL = 0: Display 4 lines.
Display control 1	D = 0: Display OFF C = 0: Cursor OFF B = 0: Blink OFF
Display control 2	PLUS = 0: 1/32 duty REV = 0: Normal display ALON = 0: Normal display
Power control	HALT = 0:.Power saving OFF PON = 0: Power circuit OFF ACL = 0: ACL operation OFF
Register in electronic volume	(1, 1, 1, 1)
Annunciator control / Display blinking control per line	DA = 0: Display annunciator OFF LREV = 0: Display blinking per line OFF I0 to I7 = (0, 0, 0, 0, 0, 0, 0, 0)
RAM data	DDRAM: Not determined CGRAM: Not determined SEGRAM: Not determined

7. Description of command (functions)

Since the instructions for the LH1592 are executed within execution cycle time, the MPU can be operated at a high speed without waiting time. The busy state check is only necessary when the Display clear command or the ACL command is executed.

7.1 List of command functions

Instruction	Instruction code										Description
	RE	RS	D7	D6	D5	D4	D3	D2	D1	D0	
Display clear	0/1	0	0	0	0	0	0	0	0	1	Specifies address 0 from DDRAM in AC after clearing all display.
Cursor home	0/1	0	0	0	0	0	0	0	1	*	Allocates address 0 for DDRAM in AC and resets shifted display.
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Specifies cursor moving direction and whether or not to shift display.
Display mode set	1								SHIFT	NL	Sets display 4lines or 3lines (NL). Sets shift direction of common outputs (SHIFT).
Display control 1	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF all display (D); turns ON/OFF cursor (C); or specifies blinking character indicated by cursor (B).
Display control 2	1							PLUS	REV	ALON	Specifies duty + 1 (PLUS); Displays data in reverse Display (REV); or Turns ON all display (ALON).
Cursor / Display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing data in DDRAM.
Power control	1						*	HALT	PON	ACL	Specifies power saving (HALT); Turn ON power circuit (PON); or specifies resetting (ACL).
Function set	0/1	0	0	0	1	BE	DUB	RE	DL1	DL0	Enables writes to expanded register (RE). Enables blinking for SEGRAM (BE). Enables display double font lengthwise (DUB). Sets display line for DUB (DL1, DL0).
CGRAM address set	0	0	0	1	ACG						CGRAM address set
SEGRAM address set	1				*	*	ASEG				SEGRAM address set
DDRAM address set	0	0	1	0	ADD						DDRAM address set
Electronic volume set	1				*	*	DVOL				Electronic volume set
Annunciator control / Display blinking control per line	0	0	1	1	I5	I4	I3	I2	I1	I0	Sets data for annunciator (I0 to I7). Enables display annunciator (DA). Enables display blinking per line (LREV). Sets display line for LREV (LIN1, LIN0).
	1				LREV	LIN1	LIN0	DA	I7	I6	
Busy flag / Address read	0/1	0	BF	*	AC						Reads out busy flag and data from AC.
RAM data write	0/1	1	WRITE DATA								RAM data write
RAM data read	0/1	1	READ DATA								RAM data read

Note: * mark shows "Don't care".

7.2 Description of instructions

(1) Display clear

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	0	0	0	0	1

Space code "20H" (for 48 characters) is written to all addresses in the DDRAM. The address counter specifies DDRAM address 0.
If the display is shifted, it is reset in place. This means that the display is cleared and the cursor or blinking cursor, if displayed, returns to the left end in the first line.
Set the I/D of the increment mode to "Increment". "S" will not change.
If you start clearing the display, the busy flag is generated. Therefore, to execute an instruction after clearing the display, monitor the busy flag and then execute the next instruction after checking that the flag has been released; or allow an waiting period for 50 times the source clock frequency .

(2) Cursor home

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	0	0	0	1	*

Specify DDRAM address 0 in the address counter. If the display is shifted, it is reset in place. The data in the DDRAM remains unchanged. The cursor or the blinking cursor, if displayed, returns to the left end in the first line.

(3) Entry mode set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	I/D	S

When the extended register enable bit (RE) is "0", the following I/D, and S bits are accessed:

I/D: When any character code is written into or read out from the DDRAM, the DDRAM address is shifted by +1 (I/D = 1) or −1 (I/D = 0). In case of +1, the cursor or the blinking cursor moves to the right. This is also applicable when any data is written into or read out from the CGRAM or SEGRAM.

S: If S = 1, the entire display is shifted to either the left or right when any character code is written into the DDRAM. If I/D = 1, the entire display is shifted to the left; or if I/D = 0, the entire display is shifted to the right. Therefore, if I/D = 1, the cursor looks stationary with only the display shifted. When any character code is read out from the DDRAM, the display is not shifted. If S = 0, the display remains unshifted.
When any data is written into or read out from the CGRAM or SEGRAM, the display also remains unshifted.
When duty+1 command is ON (PLUS=1), if S=1 and any code is written into DDRAM, the line that COMI scans is also shifted,so that this command is allowed only duty+1 command is OFF (PLUS=0) state.

(4) Display mode set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1	SHIFT	NL

When the extended register enable bit (RE) is "1", the following I/D, and S bits are accessed:

SHIFT: This command selects the direction of common scanning outputs.
SHIFT = "0": Scans the shift direction from COM0 to COM31.
SHIFT = "1": Scans the shift direction from COM31 to COM0.

NL: This command selects the displaying lines.
NL = "0": Displays 4 lines. Display duty ratio is 1/32.
NL = "1": Displays 3 lines. Display duty ratio is 1/24.

(5) Display control 1

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	C	B

When the extended register enable bit (RE) is "0", the following D, C, and B bits are accessed:

D: Turns ON the display if D = 1; or turns OFF the display if D = 0. Since the data in the DDRAM is retained, the display can be resumed by specifying D = 1.

C: Displays the cursor if C = 1; or hides the cursor if C = 0. Even if the cursor is hidden, I/D and other features remain unchanged when the display data is written. The cursor is shown using 5 dots in the 8th line.

B: Blinks the character in the cursor position if B = 1. This blinking turns ON/OFF all dots displayed in reverse. The blinking frequency is 450 ms when fosc = 55 KHz and displays 4lines. This value varies in proportion to the inverse number of fosc.

(6) Display control 2

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	PLUS	REV	ALON

When the extended register enable bit (RE) is "1", the PLUS, REV, and ALON bits are accessed. Once the specified values are stored in this register, they are retained even if the RE bit is set to "0".

PLUS: Specifies "Duty + 1". Toggles the display duty. The COMI pin functions as the COM25 (when displaying 3 lines) or COM32 (when displaying 4 lines) for marker. When the COMI is scanned, the data in the SEGRAM is output as display data from the segment driver.
PLUS = "0": Sets the display duty to 1/24 (when displaying 3 lines) or 1/32 (when displaying 4 lines).
PLUS = "1": Sets the display duty to 1/25 (when displaying 3 lines) or 1/33 (when displaying 4 lines).

REV: Toggles between normal and reverse video for display.
REV = "0": Normal video
REV = "1": Reverse video

ALON: Toggles between normal and full lit-up display regardless the data type in the DD RAM. The setting of this bit takes priority over that of REV.
ALON = "0": Normal display
ALON = "1": Full lit-up display

(7) Cursor / Display shift

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	S/C	R/L	*	*

When the extended register enable bit (RE) is "0", the following S/C and R/L bits may be set. The cursor position or the display is shifted to the left or right without writing the display data or reading it out. This may be used to modify or search the display. The cursor movement from the 1st to 2nd line occurs after the 12th digit in the 1st line. Note that all the lines are shifted simultaneously.
When duty+1 command is ON (PLUS=1), if S=1 and any code is written into DDRAM, the line that COMI scans is also shifted,so that this command is allowed only duty+1 command is OFF (PLUS=0) state.

S/C	R/L	Action
0	0	Shifts cursor to left (counts down the AC by one).
0	1	Shifts cursor to right (counts up the AC by one).
1	0	Shifts entire display to left. Cursor moves as display is shifted.
1	1	Shifts entire display to right. Cursor moves as display is shifted.

If only the display shift is made, the address counter (AC) remains unchanged.

(7) Power control

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	*	HALT	PON	ACL

HALT: Turns ON/OFF the power saving mode. When the LH1592 enters the power saving mode, the consumed current can be decreased to nearly the standby current value.
HALT = "0": Normal mode.
HALT = "1": Power saving mode.
The internal state in the power saving mode is described below
- The oscillation and power circuits are stopped.
- The LCD drive is disabled. The output from the segment and common drivers are made at the VSS level.
- The clock input at the CK pin is inhibited.

PON: Turns ON/OFF the internal power circuit.
PON = "0": Turns OFF the power circuit.
PON = "1": Turns ON the power circuit.
The booster circuit and the voltage conversion circuit become active when the power circuit is turned on. The operating section in the circuits varies depending on the setting of the PMODE pin. For further details, see the description of functions.

ACL: The internal circuit can be initialized.
ACL = "0": normal mode.
ACL = "1": ACL operation is ON.
If you turn ON ACL command,the busy flag is generated. Therefore,to execute an instruction after ACL operation, monitor the busy flag and then execute the next instruction after checking that the flag has been released; or allow an waiting period for 2 times the source clock frequency.

(9) Function set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	1	BE	DUB	RE	DL1	DL0

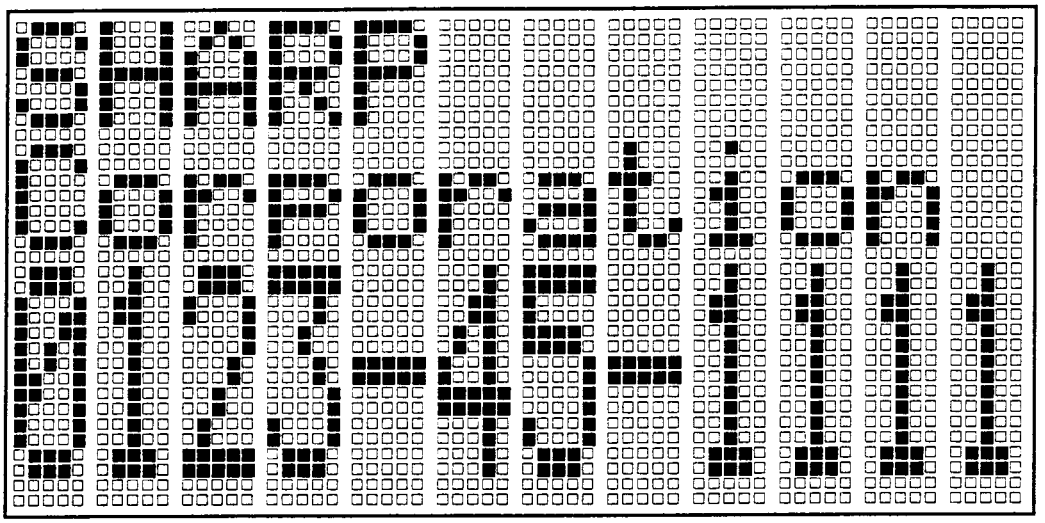
RE: This bit is the enable bit for extended register. If RE = "1", the extended function setting can be accessed. when setting instruction, it is necessary to follow the state of RE bit. (refer to instruction code.)
RE bit is consisting of resister , once the specified value is stored in this register, it is retained the value.

BE: When BE = "1", the information which was stored in the SEGRAM using its upper 2 bits may be used to allow for blinking the display data from the SEGRAM.

DUB: This bit is toggled the display double fonts lengthwise.
DUB = "0": Display normal mode.
DUB = "1": Display double fonts lengthwise.
DL1/DL0: Specifies displaying double fonts lengthwise line when setting DUB = "1".

DL1	DL0	Display double fonts lengthwise line
0	0	Specifies 1st line
0	1	Specifies 2nd line
1	0	Specifies 3rd line*
1	1	Specifies 1st and 2nd lines*

*Note : Not using these setting, when displaying 3 lines mode. (NL=1)



Example of Display (DUB = "1", DL1 = "1", DL0 = "0")

(10) CGRAM address set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	A	A	A	A	A	A

If the extended register enable bit (RE) is "0", CGRAM addresses may be specified .
In the above example, the address shown in binary number for "AAAAAA" is allocated in the address counter. Subsequently data is written or read from the MPU by referencing the CG RAM.

(11) SEGRAM address set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	*	A	A	A	A

If the extended register enable bit (RE) is "1", SEGRAM addresses may be specified .
The SEGRAM address shown in binary number for "AAAA" is allocated in the address counter. Subsequently data is written or read from the MPU in reference to the SEGRAM.

(12) DDRAM address set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	A	A	A	A	A	A

If the extended register enable bit (RE) is "0", DDRAM addresses may be specified .
The DDRAM address shown in binary number for "AAAAAA" is allocated in the address counter. Subsequently data is written or read from the MPU in reference to the DDRAM.

(13) Electronic volume register set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	*	*	MSB	....	....	LSB

The LCD drive voltage V0 output from the built-in power circuit can be controlled and the display tone on the LCD can be also controlled.
The LCD drive voltage V0 takes one out of 16 voltage values by setting 4 bit data register.

MSB	....	....	LSB	V0
0	0	0	0	Smaller
	:			:
	:			:
1	1	1	1	Larger

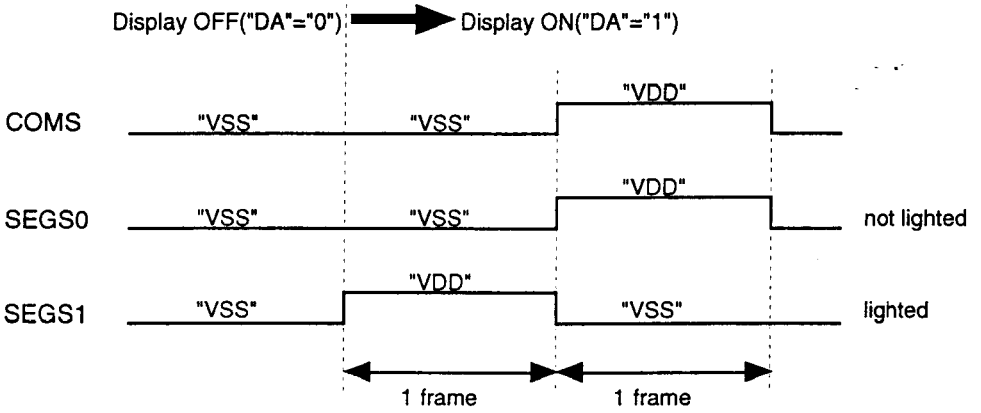
If the electronic control is not used, specify (1, 1, 1, 1) in the 4-bit data register. After the LH1592 is reset, the 4-bit data register is automatically set to (1, 1, 1, 1).

(14) Annunciator control / Display blinking control per line

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	I5	I4	I3	I2	I1	I0
1				LREV	LIN1	LIN0	DA	I7	I6

I0 to I7: These bits are setting data for annunciator. Io to I7 correspond to SEGS0 to SEGS7 for static LCD drive outputs.

DA : When DA = "1", outputs pin for static LCD drive (for annunciator display). Among VDD and VSS levels, one level is selected depending on the combination of COMS signal and display data (I0 to I7). When DA = "0", outputs VSS level.



Example of outputs for annunciator (DA = "1", I0 = "0", I1 = "1")

LREV: This bit is toggled the display blinking per line.

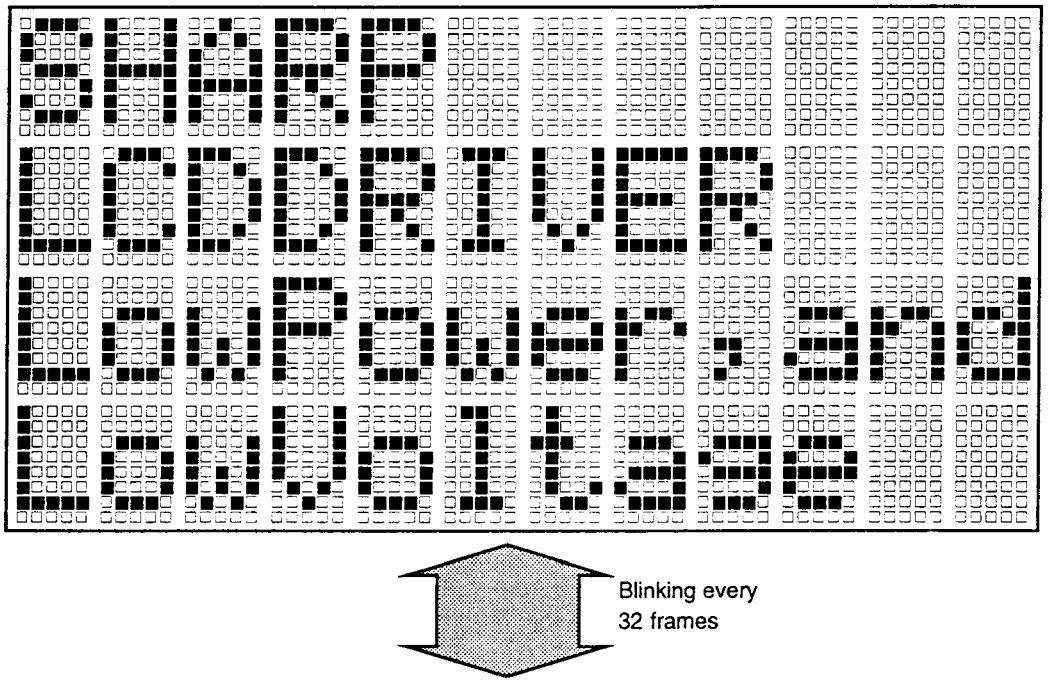
LREV = "0": Display normal mode.

LREV = "1": Display blinking per line.

LIN1/LIN0: Specifies displaying blinking line when setting LREV = "1".

LIN1	LIN0	Display blinking line
0	0	Specifies 1st line
0	1	Specifies 2nd line
1	0	Specifies 3rd line
1	1	Specifies 4th line*

*Note : Not using these setting, when displaying 3 lines mode. (NL=1)



Example of Display (LREV = "1", LIN1 = "0", LIN0 = "0")

(15) Busy flag/address read

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	BF	*	A	A	A	A	A	A

"BF = 1" indicates that the LH1592 is internally operating and the next instruction is not accepted until "BF = 0".
The busy flag is only generated when the display clear or the ACL command is executed. Therefore, any other instruction can be executed without monitoring the busy flag.
Simultaneously, the address counter value presented in binary number for "AAAAAA" is read out. The address counter is used by the DDRAM, CGRAM, and SEGRAM. The data read out from the RAMs is determined by specifying a command before this.

(16) Wrire data to RAM

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0/1	1	D	D	D	D	D	D	D	D

Writes binary 8-bit data D0 to D7 to the CGRAM or DDRAM or SEGRAM.
Whether the CGRAM or DDRAM or SEGAM is to be written into is determined by the previous specification of CGRAM or DDRAM or SEGRAM adress setting. After writing, the adress automatically increments or decrements by 1, in accordance with the entry mode.

(17) Read data to RAM

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0/1	1	D	D	D	D	D	D	D	D

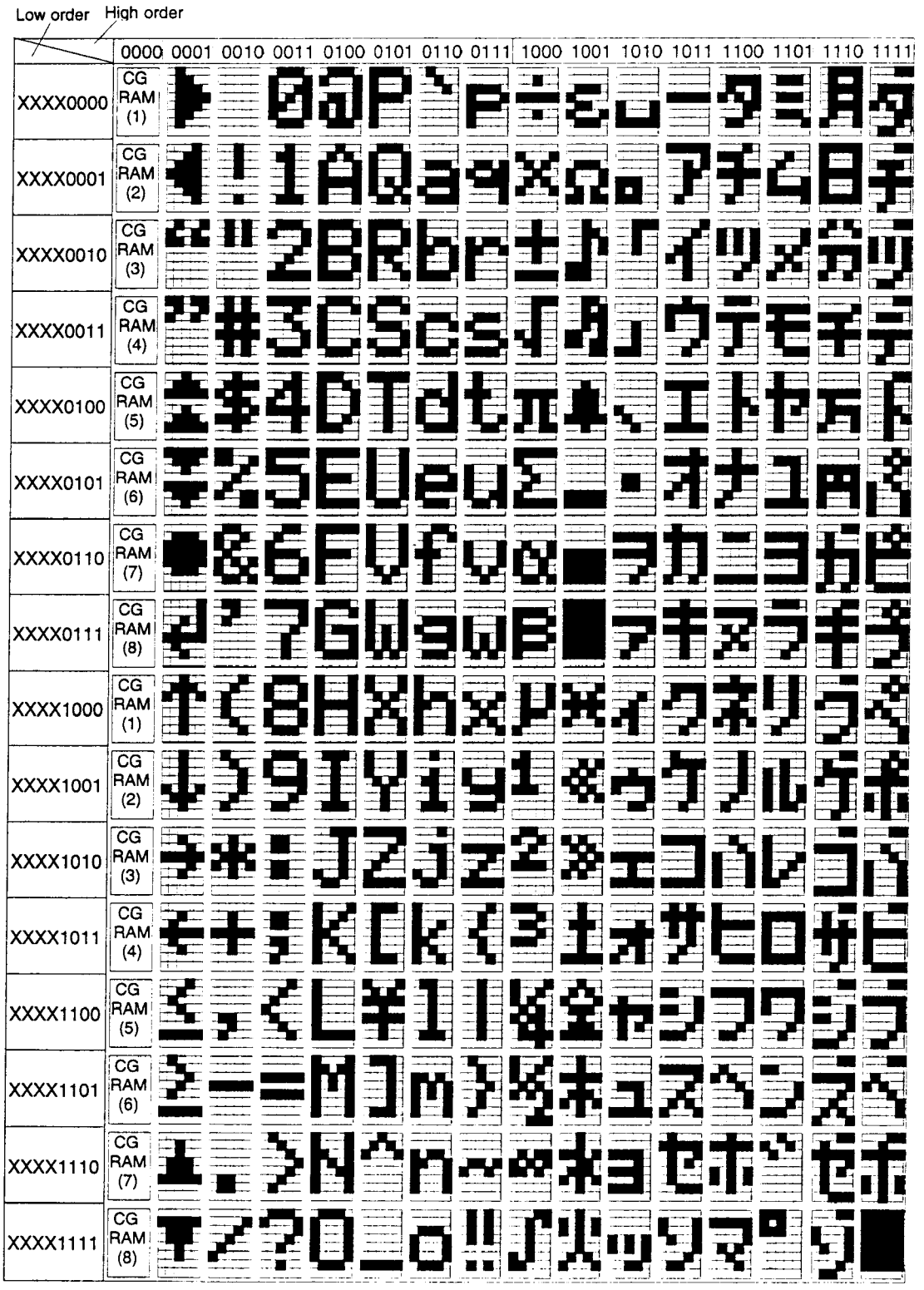
Reads binary 8-bit data D0 to D7 from the CGRAM or DDRAM or SEGRAM.
The most recent Set Adress command determines whether the CGRAM or DDRAM or SEGAM is to be read. After writing, the adress automatically increments or decrements by 1, in accordance with the entry mode.

(18) Example of instructions vs. display

No.	Instruction RS D7 D6 D5 D4 D3 D2 D1 D0	Display	Action
1	Power ON		No display appears.
2	Function set 0 0 0 1 * * 0 0 *		"0" is written to RE bit.
3	Display clear 0 0 0 0 0 0 0 0 1		Display is cleared.
4	Display ON/OFF control 0 0 0 0 0 1 1 1 0	_	Turns ON display and cursor. If Display clear,display is filled with blank spaces.
5	Entry mode set 0 0 0 0 0 0 1 1 0	_	Counts up address by one and moves cursor to right when data is written to RAM.
6	DDRAM data write 1 0 1 0 1 0 0 1 1	S_	Writes "S".
7	: :		
8	DDRAM data write 1 0 1 0 1 0 0 0 0	SHARP_	Writes "P".
9	DDRAM address set 0 1 * * 0 1 1 0 0	SHARP _	Set DDRAM address so that cursor is positioned at top of 2nd line.
10	DDRAM data write 1 0 1 0 0 1 1 0 0	SHARP L_	Writes "L".
11	: :		
12	DDRAM data write 1 0 1 0 1 0 0 1 0	SHARP LCDDRIVER_	Writes "R".
13	: :		
14	Cursor home 0 0 0 0 0 0 0 1 *	SHARP LCDDRIVER	Resets both display and cursor in place (address 0).

8. Configuration of CG ROM

Character codes vs. character patterns



9. Configuration of CGRAM

CGRAM addresses vs. character codes (DDRAM) and character patterns (CGRAM).

Character code								CGRAM address						CGRAM data							
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	0	1
											0	0	1				1	0	0	0	1
											0	1	0				1	0	0	0	1
											0	1	1				0	1	0	1	0
											1	0	0				0	0	1	0	0
											1	0	1				0	0	1	0	0
											1	1	0				0	0	1	0	0
											1	1	1				0	0	0	0	0
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	*	1	0	0	0	1
											0	0	1				1	0	0	0	1
											0	1	0				1	0	0	0	1
											0	1	1				1	1	1	1	1
											1	0	0				1	0	0	0	1
											1	0	1				1	0	0	0	1
											1	1	0				1	0	0	0	1
											1	1	1				0	0	0	0	0

* mark shows "Don't care".

Upper section: Character pattern 1 (Y display)
Lower section: Character pattern 2 (H display)

Notes:

1. Character code bits D2 to D0 correspond to CGRAM addresses A5 to A3 (3 bits: 8 types)
2. CGRAM addresses A2 to A0 correspond to line positions of the character pattern (3 bits: 8 lines)
3. The columns of the character pattern are laid out with bit 0 allocated to the right end. Therefore, the pattern of bits 4 to 0 is displayed.
4. If the upper 4 bits (7 to 4) of the character code are zeros, the CGRAM is selected. Since bit D3 are "Don't care", "00H" and "08H" are the same CGRAM address.
5. If the CGRAM data is "1" data is displayed ; if "0", data isn't displayed.

10. Configuration of SEGRAM

SEGRAM Addresses vs. Display Patterns

SEGRAM address	SEGRAM data
A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0	B1 B0 * S0 S1 S2 S3 S4
0 0 0 1	B1 B0 * S5 S6 S7 S8 S9
0 0 1 0	B1 B0 * S10 S11 S12 S13 S14
0 0 1 1	B1 B0 * S15 S16 S17 S18 S19
0 1 0 0	B1 B0 * S20 S21 S22 S23 S24
0 1 0 1	B1 B0 * S25 S26 S27 S28 S29
0 1 1 0	B1 B0 * S30 S31 S32 S33 S34
0 1 1 1	B1 B0 * S35 S36 S37 S38 S39
1 0 0 0	B1 B0 * S40 S41 S42 S43 S44
1 0 0 1	B1 B0 * S45 S46 S47 S48 S49
1 0 1 0	B1 B0 * S50 S51 S52 S53 S54
1 0 1 1	B1 B0 * S55 S56 S57 S58 S59
1 1 0 0	* * * * * * * *
1 1 0 1	* * * * * * * *
1 1 1 0	* * * * * * * *
1 1 1 1	* * * * * * * *

* *mark shows "Don't care".*

Blink control (D7 and D6) — Pattern displayed (D4 to D0)

Notes:

1. Data stored in the SEGRAM is output for one-line display when COMI is selected.
2. Pins S0 to S59 are segment driver pins. Pin S0 is shown at the left end on the screen.
3. After output at pin S59, that at pin S0 is repeated.
4. For SEGRAM data, the lower 5 bits are used for display data.
5. If BE bit in the function set register is set to "1", the upper 1 bit (D7) in SEGRAM is used to control the blinking of the lower 5-bit pattern. When D7 is set to "1", the lower 5-bit display blinks. If bit D6 is "1", only the pattern of bit D4 can be blinked.
6. If SEGRAM data is "1", data is displayed; or if "0", data isn't displayed.

11. Configuration of DDRAM

Display positions vs. display data RAM (DDRAM) addresses

digit	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th
COM0 to 7	0 0	0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	0 A	0 B
COM8 to 15	0 C	0 D	0 E	0 F	1 0	1 1	1 2	1 3	1 4	1 5	1 6	1 7
COM16 to 23	1 8	1 9	1 A	1 B	1 C	1 D	1 E	1 F	2 0	2 1	2 2	2 3
COM24 to 31	2 4	2 5	2 6	2 7	2 8	2 9	2 A	2 B	2 C	2 D	2 E	2 F

The above addressing is used because 12 digits are displayed. The DDRAM stores data for 48 characters.
If the display data is shifted, the DDRAM addresses are changed as follows:

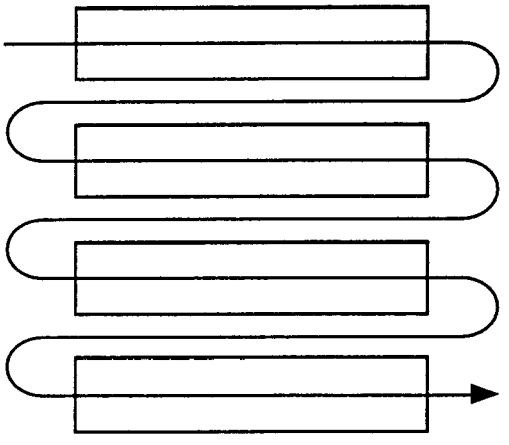
Shift to right

digit	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th
COM0 to 7	2 F	0 0	0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	0 A
COM8 to 15	0 B	0 C	0 D	0 E	0 F	1 0	1 1	1 2	1 3	1 4	1 5	1 6
COM16 to 23	1 7	1 8	1 9	1 A	1 B	1 C	1 D	1 E	1 F	2 0	2 1	2 2
COM24 to 31	2 3	2 4	2 5	2 6	2 7	2 8	2 9	2 A	2 B	2 C	2 D	2 E

Shift to left

digit	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th
COM0 to 7	0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	0 A	0 B	0 C
COM8 to 15	0 D	0 E	0 F	1 0	1 1	1 2	1 3	1 4	1 5	1 6	1 7	1 8
COM16 to 23	1 9	1 A	1 B	1 C	1 D	1 E	1 F	2 0	2 1	2 2	2 3	2 4
COM24 to 31	2 5	2 6	2 7	2 8	2 9	2 A	2 B	2 C	2 D	2 E	2 F	0 0

Note: The memory in the DDRAM is configured as follows:



Display area (12 characters × 4 line)

As shown above, the 2nd data appears following the end of the data in the 1st line. Notice that the addresses are consecutive.

12. Description of Serial interface

LH1592 built-in I²CBUS format interface.
The I²CBUS is for bidirectional,two-line communication between different ICs or modules.

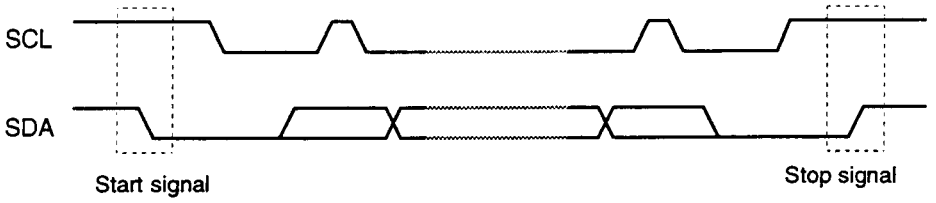
12-1. I²CBUS protocol

I²CBUS protocol consists of data receiver and data transmitter.
The device which control protocol is Master,the device which is controlled is Slave.
Master controls data translation and provides clock signal.
The LH1592 is used as Slave receiver or Slave transmitter.

(1)Data transfer
The chenge of SDA-state is allowed during SCL is low level. If SDA change during SCL is High, this action is recognized as Start bit or Stop bit.

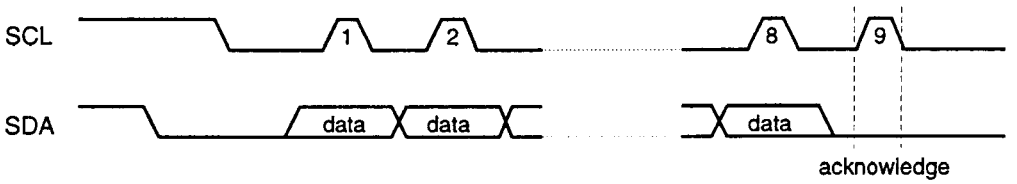
(2)Start signal
When the bus is not busy,SDA transfer High to Low during SCL is High. This state is defined as the start condition.

(3)Stop signal
When the bus is not busy,SDA transfer Low to High during SCL is High. This state is defined as the stop condition.



Start/Stop timing

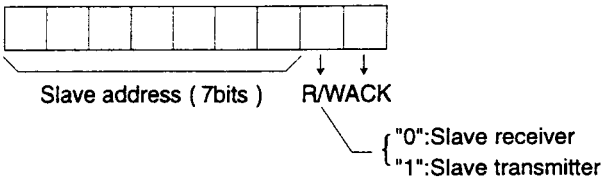
(4)Acknowledge
Acknowledge bit is used to confirm data translation.
A transmitter (Master or Slave) release bus line after receive 8 bit data.During next clock(9th clock) receiver,put Low Level on the bus to indicate data receive completely.



Acknowledge timing

(5)Device Address code

After sending start bit,Master device must transfer 8bit device address code at first.Address code consists of 7bits slave address and 1 bit R/W. When read operation,R/W bit is "1".When write operation,R/W bit is "0".



Send data at first cycle

(6)Device addressing

Bus master must generate start-condition to start data translation between 2 devices.
After generate start condition,Master puts 8 bit word on SDA bus line.
LH1592 is fixed higher order bits (corresponding to DB7 to DB2) for identify device,it is fixed"011101".
Next 1 bit is used to select LCD driver among some devices connecting to same bus.
LH1592 can connect to same bus up to 2 chips. SA0 is used for LSB bit for identify device.
8th bit (R/W bit) define operation mode.

R/W="0" : Write operation
R/W="1" : Read operation

0	1	1	1	0	1	SA0	R/W

LH1592 Slave address

(7)Second transferred data

After received start condition,,first cycles of 1 byte ,when Slave receive mode,LH1592 is specified control-byte waiting mode. Control-byte consists of 3 bits.
These bits are used to specify function mode for operating instruction.

Co :This bit define translation mode.
"0": last control byte, only data bytes to follow
"1": next two bytes are a data byte and another are control byte
RS: RS is correspond to "RS"signal in instruction table. This bit specified translation data.
R/W:This bit specified Read/Write mode.
"0": Readable mode
"1": Write enable mode.

Co	RS	R/W	*	*	*	*	*

Send Data at second cycle

12-2. Description of PIN connected with the I²CBUS

· SCL

Serial clock input pin
SCL is used for clock of all data I/O

· SDA

SDA is bidirectional pin,which is used to data I/O.
SDA is open drain pin,so please connect to VDD via pull-up resistor.

· SA0

SA0 is used for LSB bit of slave address (7 bits width). must be fixed at "H" or "L" externally.

· ISEL

ISEL select to use I²CBUS or not.
When ISEL is "H", I²CBUS is enable.
If ISEL is LOW , I²CBUS-operation of LH1592 is not warranty.

12-3. Example of I2CBUS operation

STEP	I2C BYTE	DISPLAY	OPERATION
1	I2C START		Initialized. Nothing display
2	Writing Slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1		During the acknowledge cycle SDA will be pull-downed by LH1592
3	Send a control byte Co RS R/W ACK 0 0 0 0 0 0 0 0 1		control bits RS and Co and R/W are specified
4	Function set D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 0 1 0 0 0 0 0 1		Set RE bit "0"
5	Display Clear D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 0 0 0 0 0 0 1 1		Display Clear
6	Display ON/OFF control D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 0 0 0 1 1 1 0 1	–	Display and cursor are ON All Display are clear by operating Display clear
7	Entry mode set D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 0 0 0 0 1 1 0 1	–	Entry mode set When RAM writing,address is up by 1 and cursor is shifted right
8	CGROM address set D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 1 0 0 0 0 0 0 1	–	Set address to write into CGRAM
9	Start condition	–	Set RS bit "1" and generated start condition for writing
10	Send Slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	–	
11	Send Control byte Co RS R/W ACK 0 1 0 0 0 0 0 0 1	–	
12	CGRAM data write D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 0 0 CG4 CG3 CG2 CG1 CG0 1	–	Write CGRAM data
13	: : :		
14	Start condition	–	Generated start condition again for setting RS "0"
15	Send Slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	–	
16	Send control byte Co RS R/W ACK 0 0 0 0 0 0 0 0 1	–	

STEP	I2CBYTE	DISPLAY	OPERATION
17	SET DDRAM address D7 D6 D5 D4 D3 D2 D1 D0 ACK 1 0 0 0 0 0 0 0 1	_	Setting address for DDRAM writing
18	Start condition	_	Set RS "1" and generated start condition again for DDRAM writing
19	Send Slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	_	
20	Send control byte Co RS R/W ACK 0 1 0 0 0 0 0 0 1	_	
21	Write DDRAM data D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 1 0 1 0 0 1 1 1	S_	Write "S"
22	:		
23	Send DDRAM data D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 1 0 1 0 0 1 1 1	SHARP_	Write "H"
24	Start condition	SHARP_	Set RS "1" and generated start condition again for DDRAM writing
25	Send Slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	SHARP_	
26	Send control byte Co RS R/W 0 0 0 0 0 0 0 0 1	SHARP_	
27	Set DDRAM address D7 D6 D5 D4 D3 D2 D1 D0 ACK 1 0 0 0 1 1 0 0 1	SHARP _	Set DDRAM address for cursor set ahead of 2nd line
28	Start condition	SHARP _	Set RS "1" and generated start condition again for DDRAM writing
29	Send Slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	SHARP _	
30	Send control byte Co RS R/W 0 1 0 0 0 0 0 0 1	SHARP _	
31	Write DDRAM data D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 1 0 0 1 1 0 0 1	SHARP L_	Write "L"
32	:		

STEP	I2C BYTE	DISPLAY	OPERATION
33	Write DDRAM data D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 1 0 1 0 0 1 0 1	SHARP LCDDRIVER_	Write"R"
34	Start condition	SHARP LCDDRIVER_	Set RS "1" and generated start condition again for DDRAM writing
35	Send Slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	SHARP LCDDRIVER_	
36	Send control byte Co RS R/W 1 0 0 0 0 0 0 0 1	SHARP LCDDRIVER_	Set control bit Co "1"
37	Set DDRAM address D7 D6 D5 D4 D3 D2 D1 D0 ACK 1 0 0 0 0 0 0 0 1	SHARP LCDDRIVER_	Set address for read-out DDRAM data
38	Send control byte Co RS R/W 0 1 1 0 0 0 0 0 1	SHARP LCDDRIVER_	Set control bit RS "1" and R/W "1"
39	Start condition	SHARP LCDDRIVER_	Set RS "1" and generated start condition again for DDRAM writing
40	Send Slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 1 1	SHARP LCDDRIVER_	Set R/W "1" for read-out DDRAM data
41	Read out data D7 D6 D5 D4 D3 D2 D1 D0 ACK MSB••LSB 0	SHARP LCDDRIVER_	Read-out DDRAM data from MSB to LSB Master doing acknowledge
42	: : :		
43	Read out data D7 D6 D5 D4 D3 D2 D1 D0 ACK MSB••LSB 1	SHARP LCDDRIVER_	As master don't acknowledge ,data will not be output in next cycle
44	Stop condition	SHARP LCDDRIVER_	Generated Stop condition and finish

13 Absolute Maximum Ratings

Item	Symbol	Condition	Applicable pin	Rated value	Unit
Supply voltage (1)	VDD	Relative to Vss (0 V): Ta = + 25 °C	VDD	–0.3 to + 7.0	V
Supply voltage (2)	VEE		VEE	–0.3 to + 7.0	V
Supply voltage (3)	VOUT		VOUT	–0.3 to + 13.0	V
Supply voltage (3)	VR		VR	–0.3 to + 13.0	V
Supply voltage (3)	V0		V0	–0.3 to + 13.0	V
Supply voltage (4)	V1,V2,V3,V4		V1,V2,V3,V4	–0.3 to V0 + 0.3	V
Input voltage	VI		*1	–0.3 to VDD + 0.3	V
Storage temperature	Tstg			–45 to + 125	°C

*1: D0 to D7, CSB, RS, M86, RDB, WRB, CK, CKS, OSCI, SDA, SCL, P/S, RESB, PMODE, SA0, ISEL, and TEST pins

14 Recommended Operating Conditions

Item	Symbol	Applicable pin	MIN	TYP	MAX	Unit	Remarks
Supply voltage	VDD	VDD	2.4		5.5	V	*1
Recommended operating voltage	V0	V0	4		11	V	*2
	VOUT	VOUT	4		11	V	
Operating temperature	Topr		–30		85	°C	

*1: This is the voltage applied to the VSS pin.

*2: The voltage relation shall meet the condition of VSS<V4<V3<V2<V1<V0.

15. Electrical Characteristics

15.1 DC characteristics

Unless otherwise specified, VSS = 0 V, VDD = +2.4 to +5.5 V, and Ta = –30 to +85 °C.

Item	Symbol	Applicable condition		MIN	TYP	MAX	Unit	Applicable
High-level input voltage (1)	VIH			0.8VDD		VDD	V	*1
Low-level input voltage (1)	VIL			0		0.2VDD	V	*1
High-level output voltage (1)	VOH	IOH = -0.4 mA		VDD–0.4			V	*2
Low-level output voltage (1)	VOL	IOL = 0.4 mA				0.4	V	*2
Input leak current	ILI	VI=VSS or VDD		–10		10	µA	*3
Output leak current	ILO	VI=VSS or VDD		–10		10	µA	*4
Resistance when LCD driver output is turned ON	RON1	| △Von | = 0.5 V	V0=8 V		4	8	kΩ	*5
Resistance when static LCD driver output is turned ON	RON2	| △Von | = 0.5 V				8	kΩ	*6
Standby current	ISTB	CK = 0V	VDD=3V			5	µA	*7
		CSB=VDD	VDD=5V			10		
Oscillation frequency	fosc	Rf = 910 kΩ±2 %	VDD=3V	30	55	80	kHz	*8
Booster input voltage	VEE			2.7		5.5	V	*9
Booster output voltage	VOUT	When voltage is tripled(VEE= 3 V)		8.6			V	*10
		When voltage is doubled(VEE = 3 V)		5.7				
Current consumption(1)	IDD1	V0=6V, VDD=3 V(triple voltage)			45	80	µA	*11
Current consumption(2)	IDD2	V0=5V, VDD=3 V(double voltage)			30	45	µA	*12
Reset "L" pulse width	tRW			10			µs	*13

Applicable pins

*1: D0 to D7, CSB, RS, M86, RDB, WRB, CK, CKS, OSCI, SDA, SCL, P/S, SA0, ISEL, RESB, PMODE, and TEST pins

*2: D0 to D7, LP, FLM, and M pins.

*3: CSB, RS, M86, RDB, WRB, CK, CKS, OSCI, SDA, SCL, P/S, SA0, ISEL, RESB, PMODE, and TEST pins.

*4: Applicable when D0 to D7 are at high impedance.

*5: SEG0 to SEG59, COM0 to COM15, and COMI pins.
Resistance value when 0.5 V is applied between each output pin and each power source (V0, V1, V2, V3, V4, or VSS).
Applicable when power is supplied at the power bias ratio of 1/7 in the external power supply mode.

*6: SEGS0 to SEGS7, and COMS pins.

*7: Current at the VDD pin when the source oscillation frequency clock is stopped; the chip is not selected (CSB = VDD); and no load is used.

*8: Oscillation frequency when feedback resistor Rf of 910 kΩ is connected between OSCI and OSCO.

*9: If the step-up circuit is used, the primary power VEE must be used within the above range. If the drive voltage for the LCD panel you are mounting can boost using the voltage level at the VDD pin, connect to the normal VDD power supply.

*10: VOUT pin
Applicable when the built-in oscillation circuit (Rf = 910 kΩ) and power circuit (PMODE = "L") are used.
Measuring conditions: C1 = C2 = 1 μF; VOUT pin is connected only C1 and the LCD driver pin is not loaded.

*11: Applicable if no access is made by the MPU when the built-in oscillation circuit (Rf = 910 kΩ) and power circuit (PMODE = "L") are used. The electronic control is not used(The code is "1 1 1 1"). The step-up circuit is used for tripling voltage. The display is off and the LCD driver pin is not loaded.
Measuring conditions: VDD = VEE; VR1=VR2; C1 = C2 = 1 μF; R1 + R2 + R3 = 4MΩ; the current flowing through voltage control resistors (R1, R2, and R3) is included.

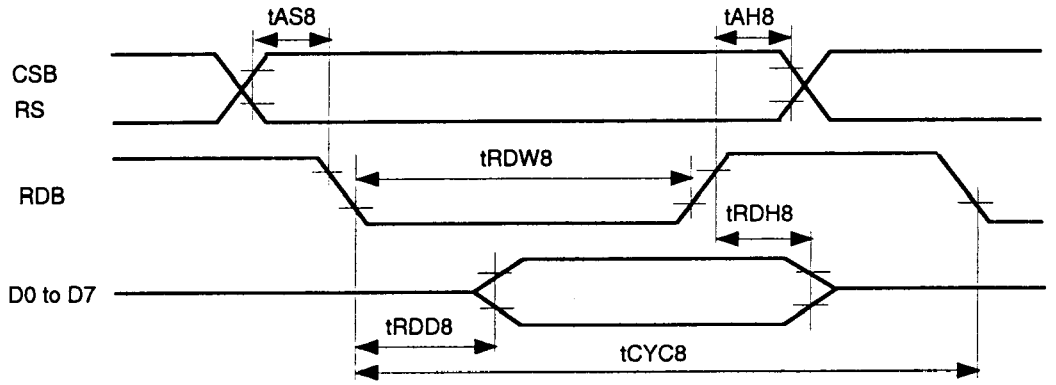
*12: Applicable if no access is made by the MPU when the built-in oscillation circuit (Rf = 910 kΩ) and power circuit (PMODE = "L") are used. The electronic control is not used(The code is "1 1 1 1"). The step-up circuit is used for double voltage. The display is off and the LCD driver pin is not loaded.
Measuring conditions: VDD = VEE; VR1=VR2; C1 = C2 = 1 μF; R1 + R2 + R3 = 4 MΩ; the current flowing through voltage control resistors (R1, R2, and R3) is included.

*13: RESB pin

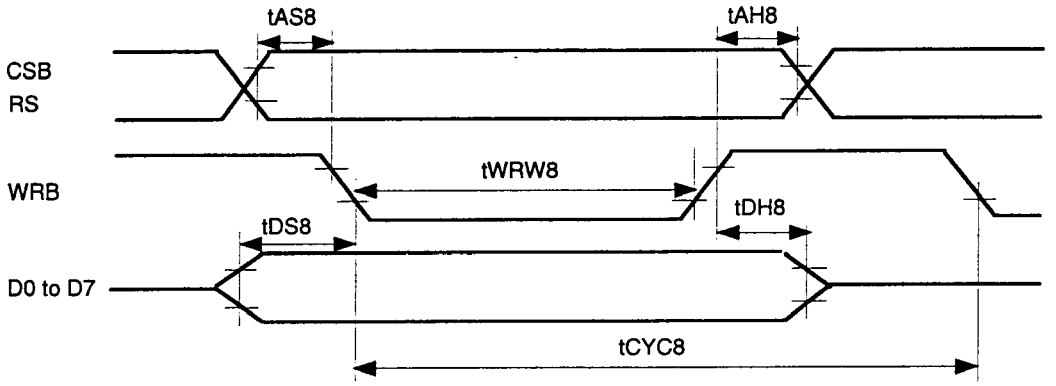
15.2 AC characteristics

(1) System bus read/write timing (80-family MPU)

(Read timing)



(Write timing)



(80-family MPU timing characteristics)

(VDD=4.5 to 5.5 V, Ta=–30 to +85 °C)

Item	Symbol	Measuring condition	MIN	MAX	Unit	Applicable pin
Address hold time	tAH8		20		ns	CSB
Address setup time	tAS8		20		ns	RS
System cycle time	tCYC8		400		ns	WRB
Read pulse width	tRDW8		300		ns	RDB
Write pulse width	tWRW8		100		ns	
Data setup time	tDS8		20		ns	D0 to D7
Data hold time	tDH8		20		ns	
Read data output delay time	tRDD8	CL=15pF		200	ns	D0 to D7
Read data hold time	tRDH8		10		ns	
Input signal rise and fall time	tr,tf			15	ns	All of above pins

(VDD=2.7 to 4.5 V, Ta=–30 to +85 °C)

Item	Symbol	Measuring condition	MIN	MAX	Unit	Applicable pin
Address hold time	tAH8		40		ns	CSB
Address setup time	tAS8		40		ns	RS
System cycle time	tCYC8		500		ns	WRB
Read pulse width	tRDW8		400		ns	RDB
Write pulse width	tWRW8		150		ns	
Data setup time	tDS8		40		ns	D0 to D7
Data hold time	tDH8		40		ns	
Read data output delay time	tRDD8	CL=15pF		350	ns	D0 to D7
Read data hold time	tRDH8		10		ns	
Input signal rise and fall time	tr,tf			15	ns	All of above pins

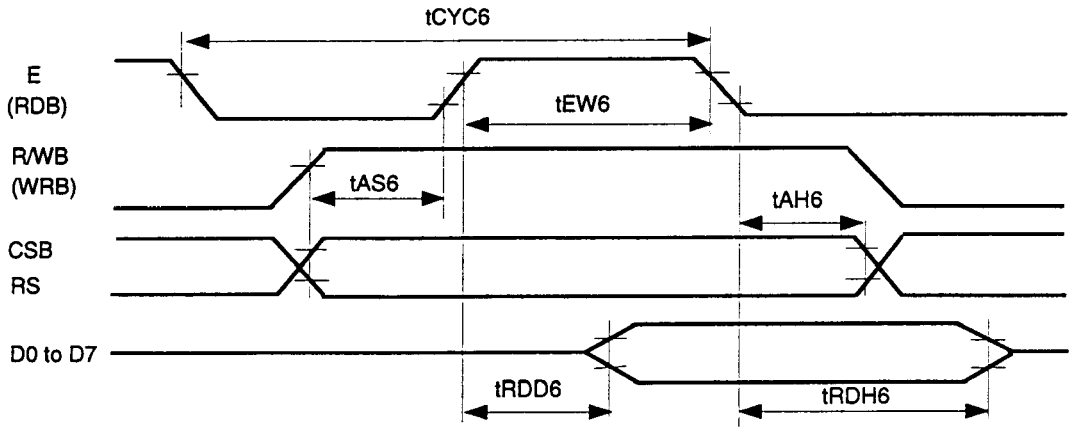
(VDD=2.4 to 2.7 V, Ta=–30 to +85 °C)

Item	Symbol	Measuring condition	MIN	MAX	Unit	Applicable pin
Address hold time	tAH8		80		ns	CSB
Address setup time	tAS8		80		ns	RS
System cycle time	tCYC8		1000		ns	WRB
Read pulse width	tRDW8		500		ns	RDB
Write pulse width	tWRW8		200		ns	
Data setup time	tDS8		80		ns	D0 to D7
Data hold time	tDH8		80		ns	
Read data output delay time	tRDD8	CL=15pF		400	ns	D0 to D7
Read data hold time	tRDH8		10		ns	
Input signal rise and fall time	tr,tf			30	ns	All of above pins

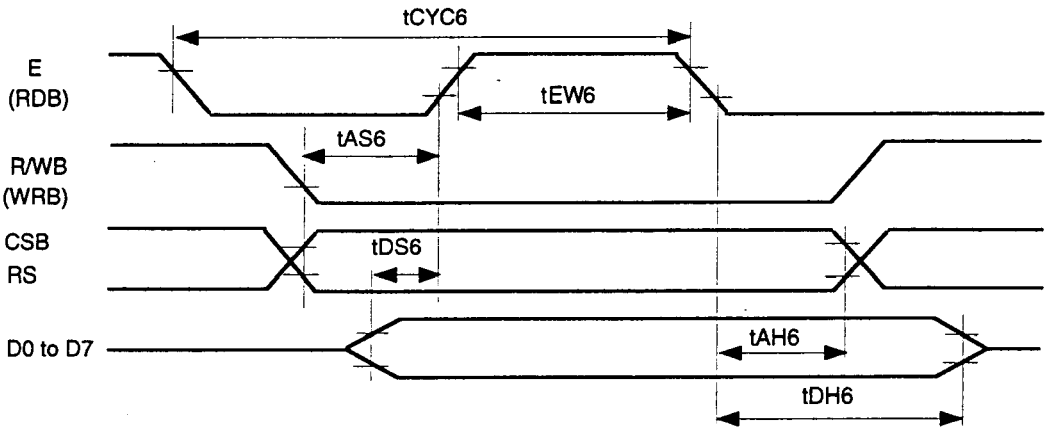
Note: All the timings must be specified relative to 20 % and 80 % of VDD voltage.

(2) System bus read/write timing (68-family MPU)

(Read timing)



(Write timing)



(68-family MPU timing characteristics)

(VDD=4.5 to 5.5 V, Ta=–30 to +85 °C)

Item	Symbol	Measuring condition	MIN	MAX	Unit	Applicable pin
Address hold time	tAH6		20		ns	CSB
Address setup time	tAS6		20		ns	RS
System cycle time	tCYC6		400		ns	RDB
Enable pulse width (READ)	tEW6		300		ns	
Enable pulse width (WRITE)			100		ns	
Data setup time	tDS6		20		ns	D0 to D7
Data hold time	tDH6		20		ns	
Read data output delay time	tRDD6	CL=15 pF		200	ns	D0 to D7
Read data hold time	tRDH6		10		ns	
Input signal rise and fall time	tr, tf			15	ns	All of above pins

(VDD=2.7 to 4.5 V, Ta=–30 to +85 °C)

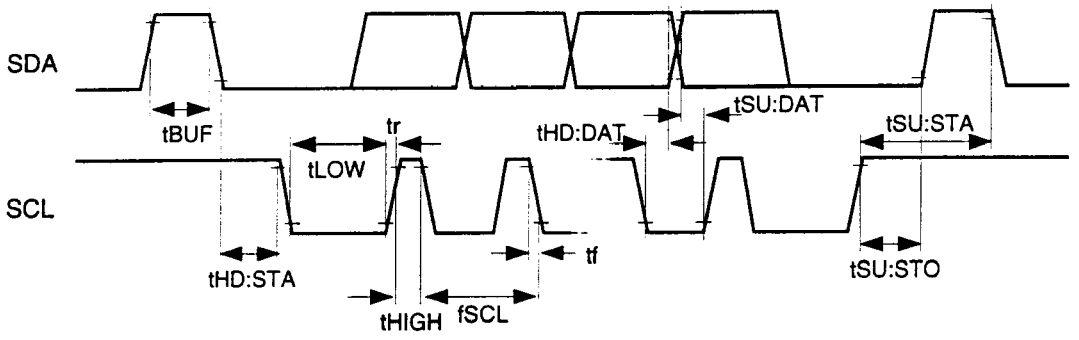
Item	Symbol	Measuring condition	MIN	MAX	Unit	Applicable pin
Address hold time	tAH6		40		ns	CSB
Address setup time	tAS6		40		ns	RS
System cycle time	tCYC6		500		ns	RDB
Enable pulse width (READ)	tEW6		400		ns	
Enable pulse width (WRITE)			150		ns	
Data setup time	tDS8		40		ns	D0 to D7
Data hold time	tDH8		40		ns	
Read data output delay time	tRDD8	CL=15 pF		350	ns	D0 to D7
Read data hold time	tRDH8		10		ns	
Input signal rise and fall time	tr, tf			15	ns	All of above pins

(VDD=2.4 to 2.7 V, Ta=–30 to +85 °C)

Item	Symbol	Measuring condition	MIN	MAX	Unit	Applicable pin
Address hold time	tAH6		80		ns	CSB
Address setup time	tAS6		80		ns	RS
System cycle time	tCYC6		1000		ns	RDB
Enable pulse width (READ)	tEW6		500		ns	
Enable pulse width (WRITE)			200		ns	
Data setup time	tDS8		80		ns	D0 to D7
Data hold time	tDH8		80		ns	
Read data output delay time	tRDD8	CL=15 pF		400	ns	D0 to D7
Read data hold time	tRDH8		10		ns	
Input signal rise and fall time	tr, tf			30	ns	All of above pins

Note: All the timings must be specified relative to 20 % and 80 % of VDD voltage.

(3) Serial interface timing (I²CBUS)



(Serial interface timing characteristics)

(VDD=2.4 to 5.5 V, Ta=–30 to +85 °C)

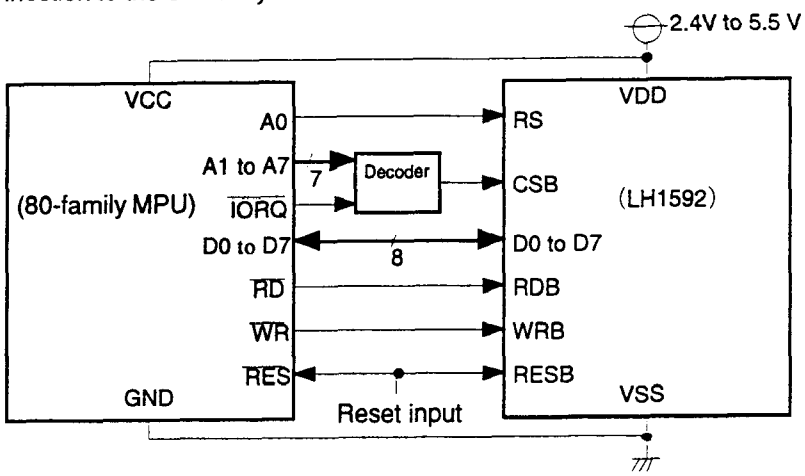
Item	Symbol	MIN	TYP	MAX	Unit	applicable pin
SCL clock frequency	fSCL			100	kHz	SCL
Start condition hold time	tHD:STA	4.7			µs	
SCL LOW time	tLOW	4.7			µs	
SCL HIGH time	tHIGH	4			µs	
bus free time	tBUF	4.7			µs	SDA
data set-up time	tSU:DAT	250			ns	
data hold time	tHD:DAT	0			ns	
set-up time for START condition	tSU:STA	4.7			µs	SCL,SDA
set-up time for STOP condition	tSU:STO	4			µs	
SCL and SDA rise time	tr			1	µs	
SCL and SDA fall time	tf			0.3	µs	

Note: All the timings must be specified relative to 20 % and 80 % of VDD voltage.

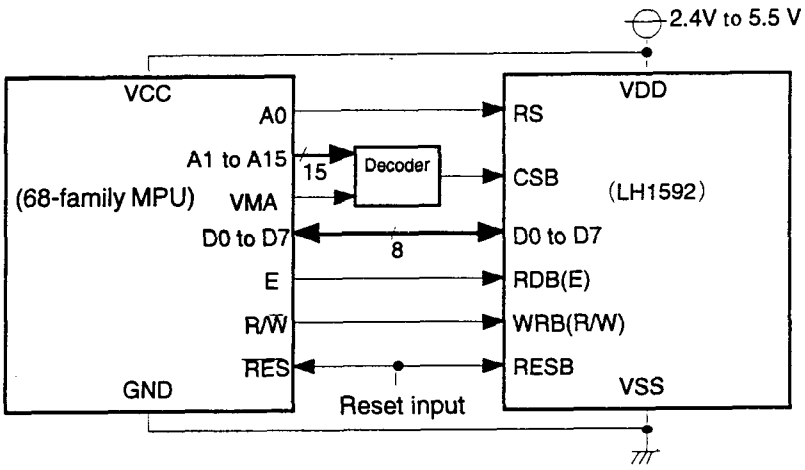
16. Typical Application (for reference)

16.1 Connection to the MPU

(a) Connection to the 80-family MPU



(b) Connection to the 68-family MPU



17. Typical Example of Characteristics

Item	Condition	MIN	TYP	MAX	Unit
Basic gate propagation delay time	Ta=+25 °C, VSS=0 V, VDD=5.0 V		10		ns