



SANYO Semiconductors

**DATA SHEET****LV23100T-A**

Bi-CMOS IC

— For Portable Audio System

**1-chip Tuner IC****Incorporating PLL****Overview**

The LV23100T-A is a one-chip tuner IC incorporating PLL for portable audio system.

**Functions**

- FM tuner
- MPX stereo decoder
- PLL frequency synthesizer

**Specifications**

**Maximum Ratings** at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max	V <sub>CC</sub>	4.0	V
	V <sub>DD</sub> max	V <sub>DD</sub>	4.0	V
Maximum input voltage	V <sub>IN1</sub> max	CE, CI, CL	6.0	V
	V <sub>IN2</sub> max	XIN	V <sub>DD</sub> +0.3	V
Allowable power dissipation	Pd max	Ta≤70°C	180	mW
Maximum output voltage	V <sub>O1</sub> max	DO	6.0	V
	V <sub>O2</sub> max	XOUT, PD	V <sub>DD</sub> +0.3	V
	V <sub>O3</sub> max	BO1, BO2, AOUT	12.0	V
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Note : This product should be handled with care because the resistance against electrostatic discharge damage is low.

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**SANYO Semiconductor Co., Ltd.**

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**Operating Condition** at  $T_a = 25\text{ }^\circ\text{C}$ 

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	$V_{CC}$		3.0	V
	$V_{DD}$		3.0	V
Operating supply voltage range	$V_{CC\text{ op}}$		2.2 to 3.6	V
	$V_{DD\text{ op}}$		2.2 to 3.6	V

**PLL block Allowable Operating Range** at  $T_a = -20\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ 

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$		2.2		3.6	V
Input high level voltage	$V_{IH}$	CE, CL, DI	$0.7V_{DD}$		6.0	V
Input low level voltage	$V_{IL}$	CE, CL, DI	0		$0.3V_{DD}$	-
Output voltage	$V_{O1}$	DO	0		6.0	V
	$V_{O2}$	BO1, BO2, AOUT	0		10	V
Operating frequency	$f_{IN1}$	XIN ; $V_{IN1}$		75		kHz
	$f_{IN2}$	FMIN ; $V_{IN2}$	10		160	MHz

Note : Due attention must be paid on leak because the XIN pin has an extremely high input impedance.

**Operating Characteristics** at  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = V_{DD} = 3.0\text{V}$ , See the specified circuit.

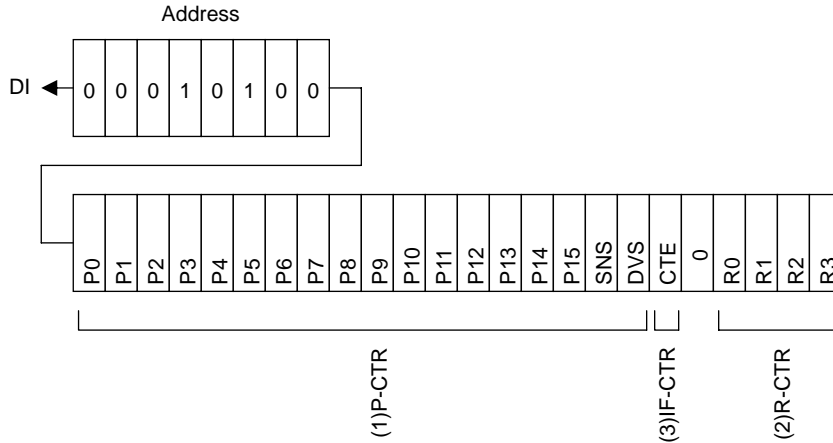
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Current dissipation]						
FM tuner block	$I_{CCFM}$	No input in FM mode	9	12.5	16	mA
PLL block	$I_{DDFM}$	fr = 98MHz, No input at tuner	1	2	4	mA
[FM-FE characteristics] : $f_c = 98\text{MHz}$ , $f_m = 1\text{kHz}$ , $\text{dev} = 22.5\text{kHz}$						
3dB sensitivity	-3dBLS	$V_{IN} = 60\text{dB}\mu\text{V}$ EMF reference, -3dB input		10		$\text{dB}\mu\text{V}$ EMF
Actual sensitivity	QS	S/N = Input at S/N = 30dB		13		$\text{dB}\mu\text{V}$ EMF
[FM-IF monaural characteristics] : $f_c = 10.7\text{MHz}$ , $f_m = 1\text{kHz}$ , $\text{dev} = 75\text{kHz}$						
Demodulation output	$V_O$	$V_{IN} = 100\text{dB}\mu\text{V}$	140	180	210	mVrms
3dB sensitivity	LS	$V_{IN} = 100\text{dB}\mu\text{V}$ reference, -3dB input	26	31	36	$\text{dB}\mu\text{V}$
Signal-to-noise ratio	S/N	$V_{IN} = 100\text{dB}\mu\text{V}$	63	70		dB
IF count sensitivity	IF-C1	0%mod, SDC = 1	42	50	56	$\text{dB}\mu\text{V}$
Mute attenuation	MUTE	$V_{IN} = 100\text{dB}\mu\text{V}$ , L output	55	60		dB
[FM-IF stereo characteristics] : $f_c = 10.7\text{MHz}$ , $f_m = 1\text{kHz}$ , $\text{dev} = 75\text{kHz}$ (L+R = 90%, Pilot = 10%)						
Separation	SEP	$V_{IN} = 100\text{dB}\mu\text{V}$ , L output/R output	25	40		dB
Total harmonic distortion	THD	$V_{IN} = 100\text{dB}\mu\text{V}$ , MAIN-MOD		0.5	1.5	%

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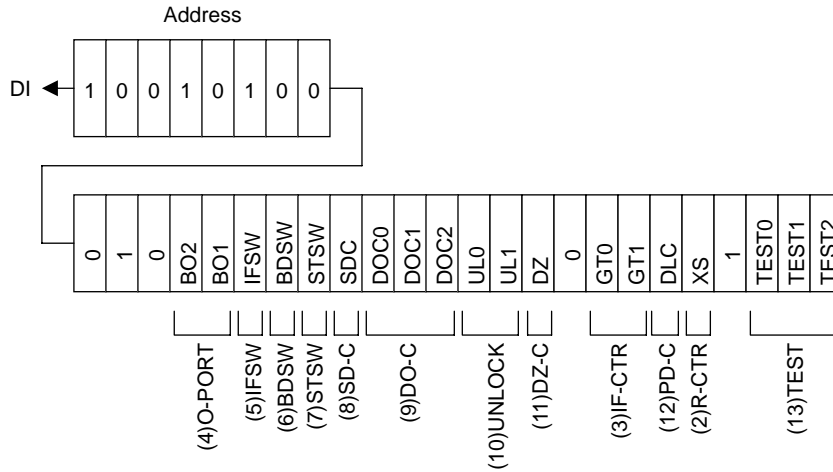


**Composition of DI control data (serial data input)**

(1) IN mode



(2) IN2 mode



**Description of DI control Data**

No.	Control block data	Description	Related data																												
(1)	DO pin Control data  DOC0 DOC1 DOC2	<ul style="list-style-type: none"> <li>Data to set the dividing number of programmable divider Binary value with P15 assumed to be MSB. LSB varies according to DVS and SNS. (* : don't care)</li> </ul> <table border="1"> <thead> <tr> <th>DVS</th> <th>SNS</th> <th>LSB</th> <th>set dividing number (N)</th> <th>actual dividing number</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>*</td> <td>P0</td> <td>272 to 65535</td> <td>Twice the set value</td> </tr> <tr> <td>0</td> <td>1</td> <td>P0</td> <td>272 to 65535</td> <td>Set value</td> </tr> <tr> <td>0</td> <td>0</td> <td>P4</td> <td>4 to 4095</td> <td>Set value</td> </tr> </tbody> </table> <ul style="list-style-type: none"> <li>* P0 to P3 invalid when LSB : P4</li> <li>To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range. (* : don't care)</li> </ul> <table border="1"> <thead> <tr> <th>DVS</th> <th>SNS</th> <th>Input</th> <th>Operation frequency range</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>*</td> <td>FMIN</td> <td>10 to 160MHz</td> </tr> </tbody> </table>	DVS	SNS	LSB	set dividing number (N)	actual dividing number	1	*	P0	272 to 65535	Twice the set value	0	1	P0	272 to 65535	Set value	0	0	P4	4 to 4095	Set value	DVS	SNS	Input	Operation frequency range	1	*	FMIN	10 to 160MHz	
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No.	Control block data	Description	Related data																																																																																					
(2)	Reference divider data  R0 to R3 XS	<ul style="list-style-type: none"> <li>Reference frequency (fref) selection data</li> </ul> <table border="1"> <thead> <tr> <th>R3</th> <th>R2</th> <th>R1</th> <th>R0</th> <th>Reference frequency</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25kHz</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25kHz</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25kHz</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25kHz</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5kHz</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25kHz</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125kHz</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125kHz</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5kHz</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5kHz</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5kHz</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1kHz</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3kHz</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15kHz</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT+X'tal OSC STOP</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr> </tbody> </table> <ul style="list-style-type: none"> <li>* PLL INHIBIT</li> <li>The programmable divider and IF counter stop, with FMIN, AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance.</li> <li>XS must be zero.</li> </ul>	R3	R2	R1	R0	Reference frequency	0	0	0	0	25kHz	0	0	0	1	25kHz	0	0	1	0	25kHz	0	0	1	1	25kHz	0	1	0	0	12.5kHz	0	1	0	1	6.25kHz	0	1	1	0	3.125kHz	0	1	1	1	3.125kHz	1	0	0	0	5kHz	1	0	0	1	5kHz	1	0	1	0	5kHz	1	0	1	1	1kHz	1	1	0	0	3kHz	1	1	0	1	15kHz	1	1	1	0	PLL INHIBIT+X'tal OSC STOP	1	1	1	1	PLL INHIBIT	
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(3)	IF counter control data  CTE GT0, GT1	<ul style="list-style-type: none"> <li>IF counter counting start data CTE = 1 : Counting start = 0 : Counting start</li> <li>Determines the counting time of universal counter</li> </ul> <table border="1"> <thead> <tr> <th>GT1</th> <th>GT0</th> <th>Counting time</th> <th>Wait time</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>4ms</td><td>3 to 4ms</td></tr> <tr><td>0</td><td>1</td><td>8ms</td><td>3 to 4ms</td></tr> <tr><td>1</td><td>0</td><td>16ms</td><td>3 to 4ms</td></tr> <tr><td>1</td><td>1</td><td>32ms</td><td>3 to 4ms</td></tr> </tbody> </table>	GT1	GT0	Counting time	Wait time	0	0	4ms	3 to 4ms	0	1	8ms	3 to 4ms	1	0	16ms	3 to 4ms	1	1	32ms	3 to 4ms																																																																		
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(4)	Output port data  $\overline{BO1}$ , $\overline{BO2}$	<ul style="list-style-type: none"> <li>Data to determine output of output ports <math>\overline{BO1}</math> and <math>\overline{BO2}</math> "Data" = 0 : OPEN 1 : Low</li> </ul>																																																																																						
(5)	MUTE control data  IFSW	<ul style="list-style-type: none"> <li>Data to determine the output of output port IFSW, controlling the MUTE function. "Data" = 0 : at receiving 1 : MUTE</li> </ul>																																																																																						
(6)	FM/AM BAND selection control data BDSW	<ul style="list-style-type: none"> <li>Data to determine the output of output port BDSW, controlling selection of BAND. "Data" = 0 : AM 1 : FM</li> </ul>																																																																																						
(7)	Forced monaural control data  STSW	<ul style="list-style-type: none"> <li>Data to determine the output of output port STSW, controlling the forced stereo functions. "Data" = 0 : MONO 1 : STEREO</li> </ul>																																																																																						
(8)	SD sensitivity control data  SDC	<ul style="list-style-type: none"> <li>Data to determine the output of output port SDC, controlling the FM-SD sensitivity (at IF input).</li> </ul> <table border="1"> <thead> <tr> <th>SDC</th> <th>FM-SD sensitivity</th> </tr> </thead> <tbody> <tr><td>0*</td><td>38dB<math>\mu</math>V</td></tr> <tr><td>1</td><td>48dB<math>\mu</math>V</td></tr> </tbody> </table>	SDC	FM-SD sensitivity	0*	38dB $\mu$ V	1	48dB $\mu$ V																																																																																
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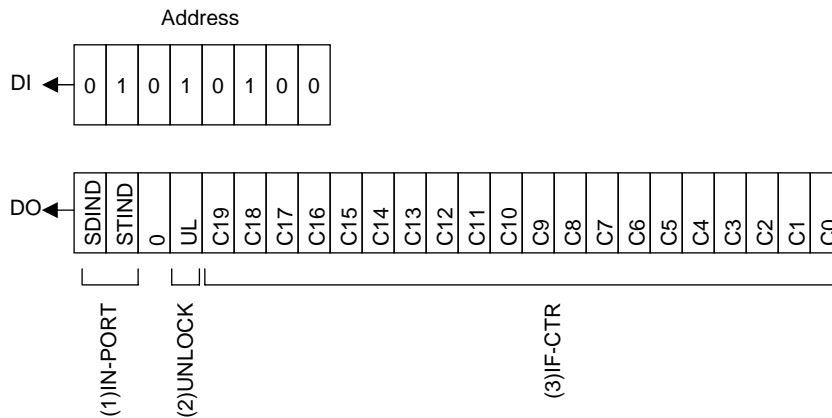
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No.	Control block data	Description	Related data																																				
(9)	DO pin control data  DOC0 DOC1 DOC2	<ul style="list-style-type: none"> <li>Data to determine the output of the DO pin.</li> </ul> <table border="1"> <thead> <tr> <th>DOC2</th> <th>DOC1</th> <th>DOC0</th> <th>DO pin condition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Open</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Low when unlock is detected.</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>end-UC (See the item with asterisk below)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Open</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Open</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Low when stereo</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Low when SDON</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Open</td> </tr> </tbody> </table> <ul style="list-style-type: none"> <li>The open condition is selected at power ON/reset.</li> <li>* IF counter counting end check</li> </ul> <p>① Counting start      ② Counting end      ③ CE : Hi</p> <p>① With end-UC set and IF counter starting (CTE = 0→1), DO pin opens automatically.          ② At end of counting of the IF counter, DO pin goes LOW and check on counting end can be made.          ③ DO pin opens when serial data is entered/output (CE pin : Hi)          Note : DO pin is always in the open condition during data input (IN1 and IN2 modes, during CE : Hi period), regardless of DO pin control data (DOC0 to 2). In the DO pin condition during data output (OUT mode, CE-Hi period), the content of internal DO serial data is output in synchronization with CL, regardless of DO pin control data (DOC).</p>	DOC2	DOC1	DOC0	DO pin condition	0	0	0	Open	0	0	1	Low when unlock is detected.	0	1	0	end-UC (See the item with asterisk below)	0	1	1	Open	1	0	0	Open	1	0	1	Low when stereo	1	1	0	Low when SDON	1	1	1	Open	UL0, UL1 CTE
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(10)	Unlock detection data  UL0, UL1	<ul style="list-style-type: none"> <li>Phase error (<math>\phi E</math>) detection width selection data to judge if PLL is locked.</li> <li>Phase error exceeding the detection width is judged that PLL is locked (* : don't care)</li> </ul> <table border="1"> <thead> <tr> <th>UL1</th> <th>UL0</th> <th><math>\phi E</math> Detection width</th> <th>Detection output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Stop</td> <td>Open</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Direct output of <math>\phi E</math></td> </tr> <tr> <td>1</td> <td>*</td> <td><math>\pm 6.67 \mu s</math></td> <td><math>\phi E</math> extended by 1 to 2 ms</td> </tr> </tbody> </table> <p>* DO pin is LOW. Serial data output : UL = 0.</p>	UL1	UL0	$\phi E$ Detection width	Detection output	0	0	Stop	Open	0	1	0	Direct output of $\phi E$	1	*	$\pm 6.67 \mu s$	$\phi E$ extended by 1 to 2 ms	DOC0 DOC1 DOC2																				
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(11)	Phase comparator control data  DZ	<ul style="list-style-type: none"> <li>Data to control the dead zone of phase comparator</li> </ul> <table border="1"> <thead> <tr> <th>DZ</th> <th>Charge pump output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DZA</td> </tr> <tr> <td>1</td> <td>DZB</td> </tr> </tbody> </table> <p>Dead zone width : DZA&lt;DZB</p>	DZ	Charge pump output	0	DZA	1	DZB																															
DZ	Charge pump output																																						
0	DZA																																						
1	DZB																																						
(12)	Charge pump control data  DLC	<ul style="list-style-type: none"> <li>Data to enforce control of charge pump output</li> </ul> <table border="1"> <thead> <tr> <th>DLC</th> <th>Charge pump output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal</td> </tr> <tr> <td>1</td> <td>Forced to LOW</td> </tr> </tbody> </table> <p>In case of dead lock because of VCO oscillation stop when the VCO control voltage (Vtune) is 0V, it is possible to clear dead lock by setting the charge pump output to LOW and V tune to V<sub>CC</sub>. (Dead lock clear circuit)</p>	DLC	Charge pump output	0	Normal	1	Forced to LOW																															
DLC	Charge pump output																																						
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(13)	LSI test data  TEST0 to 2	<ul style="list-style-type: none"> <li>LSI test data</li> </ul> <p>TEST0 }          TEST1 } All to be set to "0"          TEST2 }</p> <p>All set to zero at power ON/reset</p>																																					

## DO control data (serial data output) composition

## (1) OUT mode

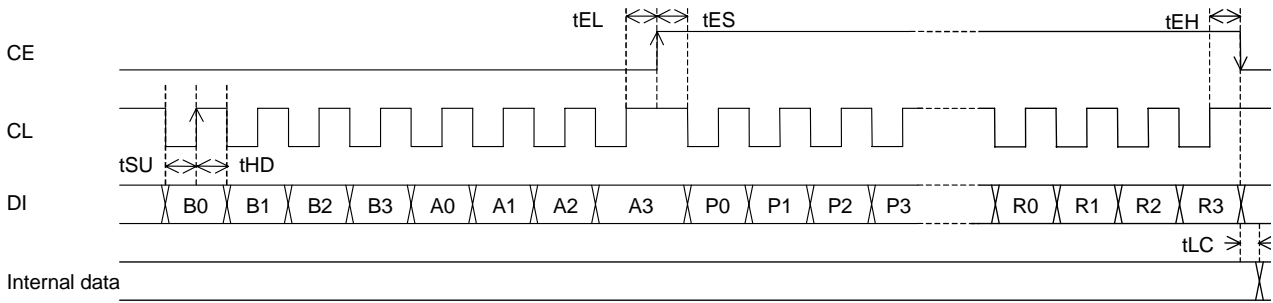


## Description of DO output data

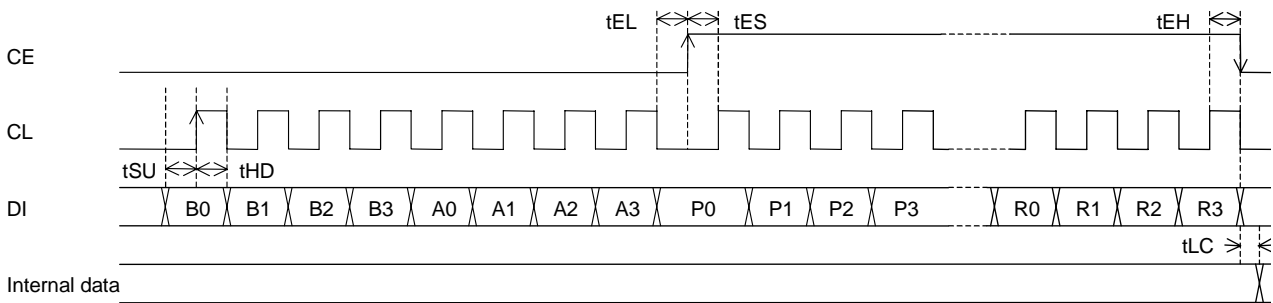
No.	Control block data	Description	Related data
(1)	SD and Stereo indicators control data  STIND, SDIND	<ul style="list-style-type: none"> <li>Data latching SD and stereo indicator conditions. Latching made in the data output (OUT) mode. SDIND←SD indicator condition    0 : SD ON, 1 : SD OFF STIND←Stereo indicator condition    0 : ST ON, 1 : ST OFF</li> </ul>	
(2)	PLL unlock data  UL	<ul style="list-style-type: none"> <li>Data latching the content of unlock detection circuit UL←0 : At unlock 1 : At lock or detection stop mode</li> </ul>	UL0 UL1
(3)	IF counter, binary counter  C19 to C0	<ul style="list-style-type: none"> <li>Data latching the content of IF counter (20-bit binary counter) C19←MSB of binary counter C0 ←MSB of binary counter</li> </ul>	CTE GT0 GT1

**Serial data input (IN1/IN2)  $t_{SU}$ ,  $t_{HD}$ ,  $t_{EL}$ ,  $t_{ES}$ ,  $t_{EH} \geq 0.75\mu s$   $t_{LC} < 0.75\mu s$**

CL : Normally Hi

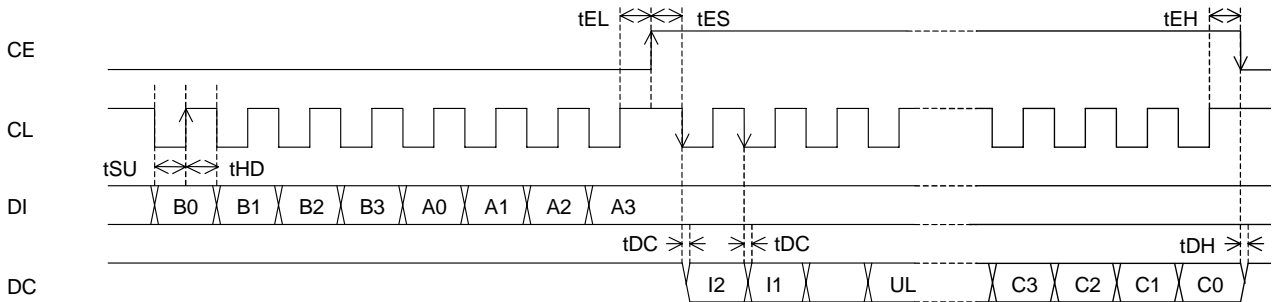


CL : Normally Low

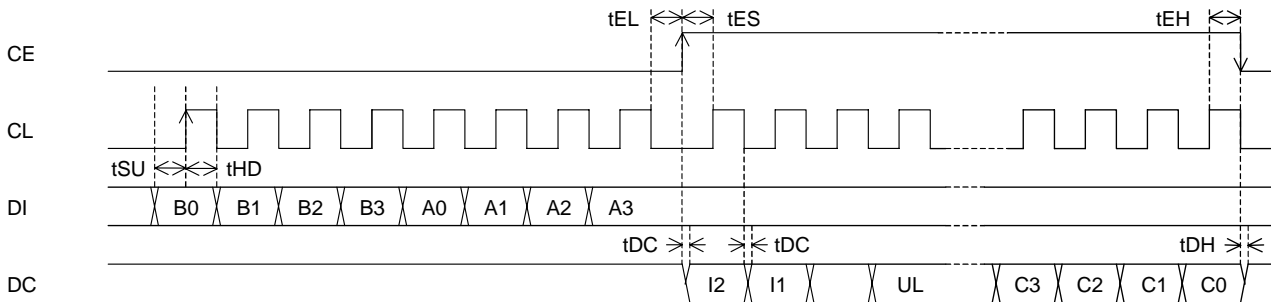


**Serial data output (OUT)  $t_{SU}$ ,  $t_{HD}$ ,  $t_{EL}$ ,  $t_{ES}$ ,  $t_{EH} \geq 0.75\mu s$   $t_{DC}$ ,  $t_{DH} < 0.35\mu s$**

CL : Normally Hi

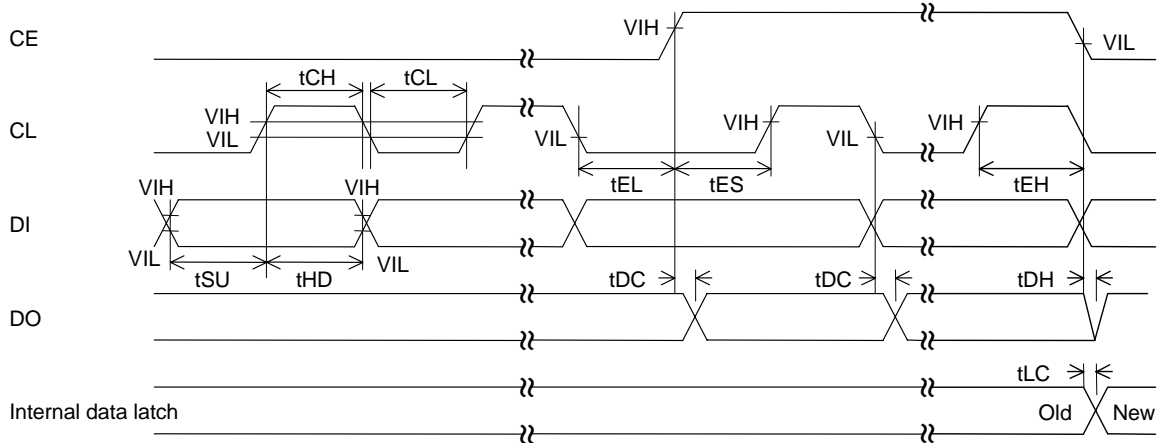


CL : Normally Hi

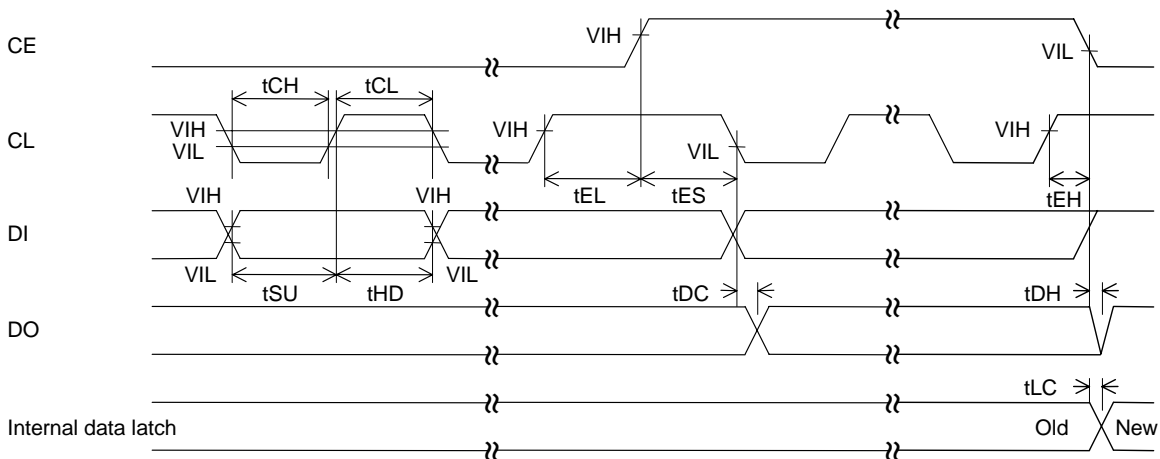


(Note) DO pin is an Nch open drain pin, so that the data varying time ( $t_{DC}$  and  $t_{DH}$ ) differs depending on the pull-up resistance and substrate capacity.

**Serial data timing**



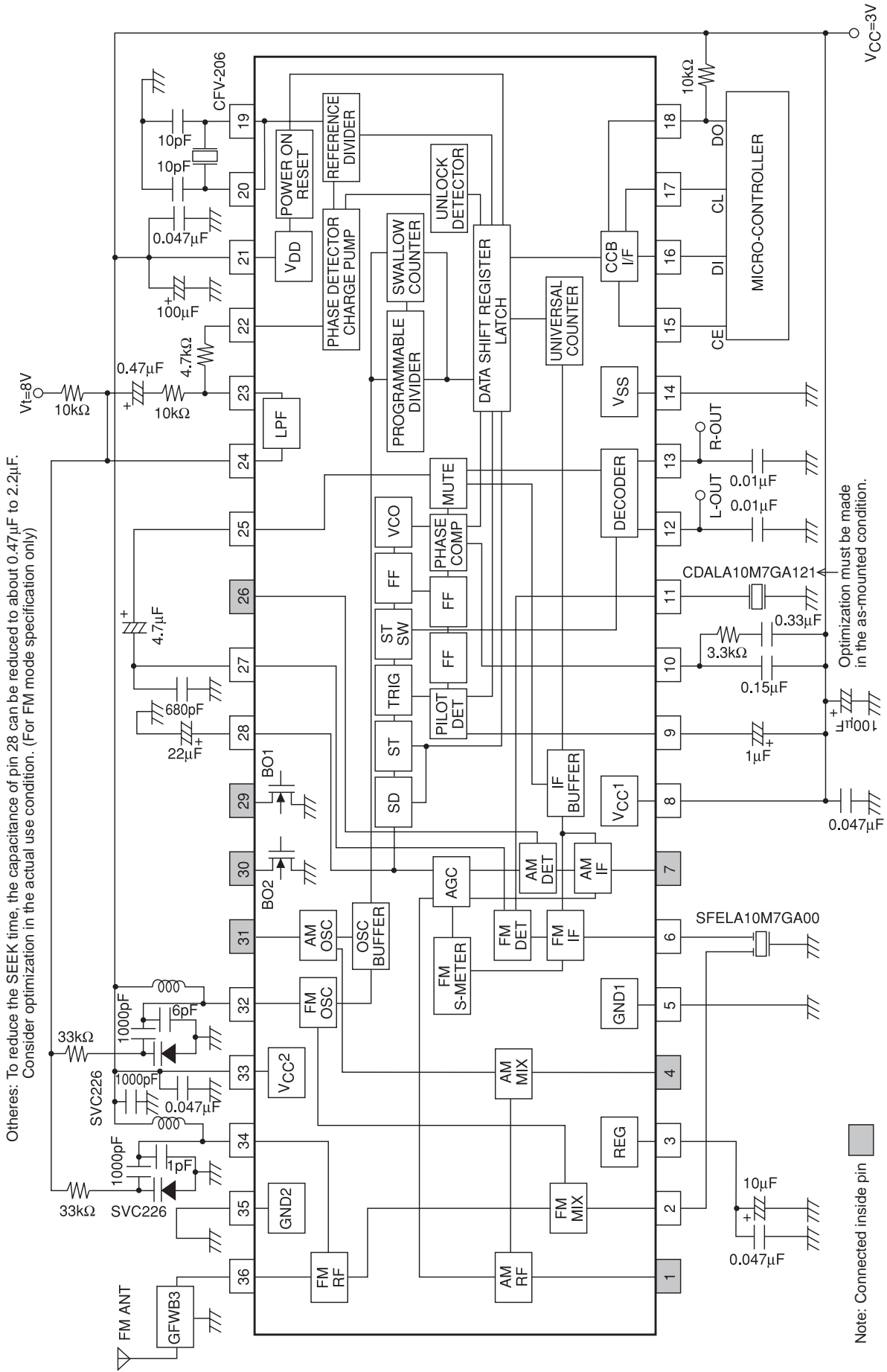
<< When CL stops at the "L" level >>



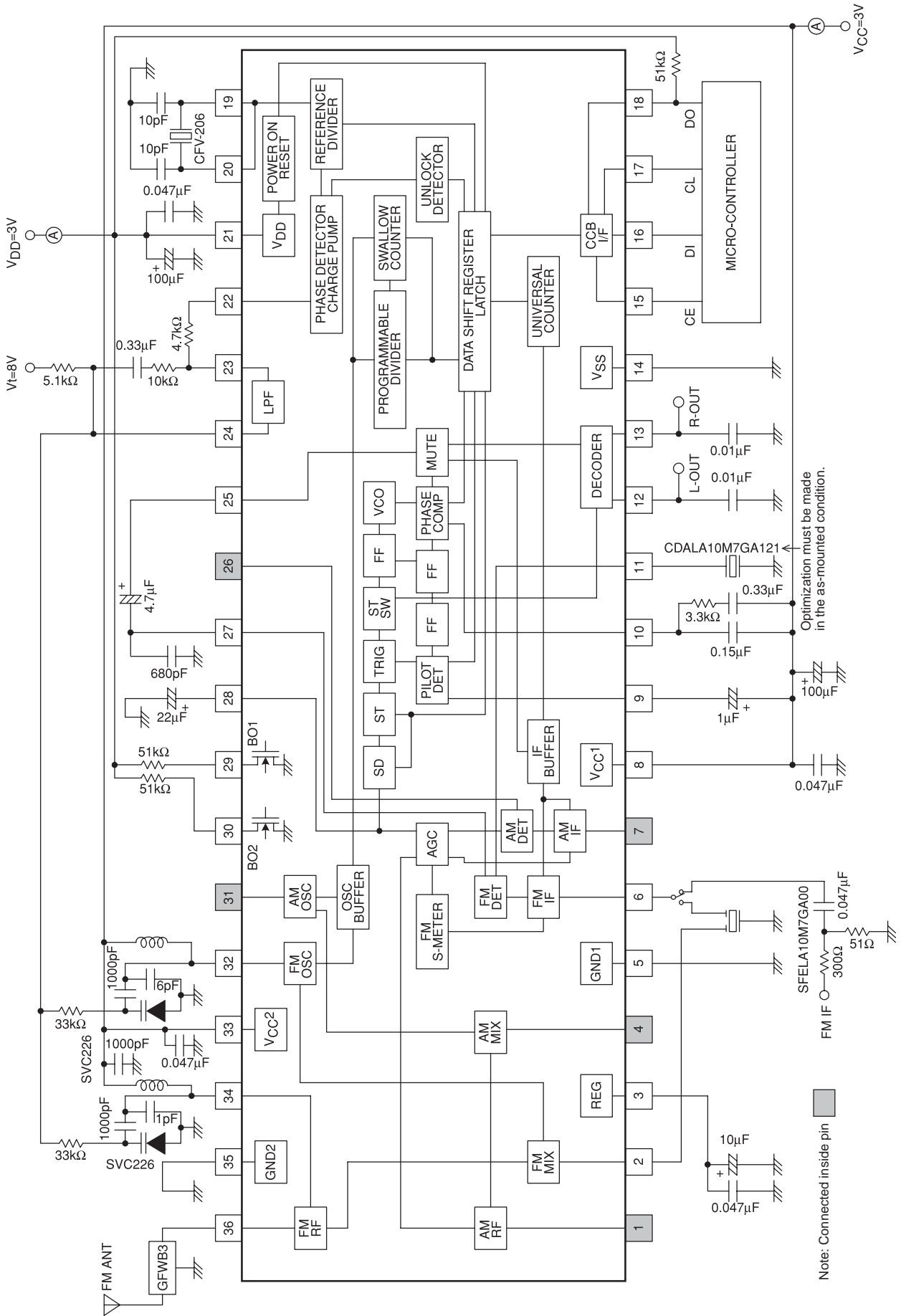
<< When CL stops at the "H" level >>

Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	$t_{SU}$	DI, CL		0.75			$\mu\text{s}$
Data hold time	$t_{HD}$	DI, CL		0.75			$\mu\text{s}$
Clock "L" level time	$t_{CL}$	CL		0.75			$\mu\text{s}$
Clock "H" level time	$t_{CH}$	CL		0.75			$\mu\text{s}$
CE wait time	$t_{EL}$	CE, CL		0.75			$\mu\text{s}$
CE setup time	$t_{ES}$	CE, CL		0.75			$\mu\text{s}$
CE hold time	$t_{EH}$	CE, CL		0.75			$\mu\text{s}$
Data latch change time	$t_{LC}$					0.75	$\mu\text{s}$
Data output time	$t_{DC}$	DO, CL	Differs depending on the pull-up resistance and substrate capacity			0.35	$\mu\text{s}$
	$t_{DH}$	DO, CE					

**Block Diagram and Sample Application Circuit**



**Test Circuit**



Note: Connected inside pin

Optimization must be made in the as-mounted condition.

**Coil specifications** (Example: Carry out optimization in the as-mounted condition.)

• FM-BPF : GFWB3 (Soshin) 76MHz to 108MHz
• FM-RF : SA-149 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 4.5T
• FM-OSC : SA-151 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 3.5T
• FM-IF Filter : SFELA10M7GA00 (Murata)
• FM-Discriminator : CDALA10M7GA121 (Murata)
• Crystal oscillator : CFV-206 (Citizen)

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