

N-CHANNEL ENHANCEMENT-MODE DMOS POWER FETs

FEATURES

- High Gate Oxide Breakdown, $\pm 40V$ min.
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays
- Motor Controls
- Power Supplies

ORDERING INFORMATION

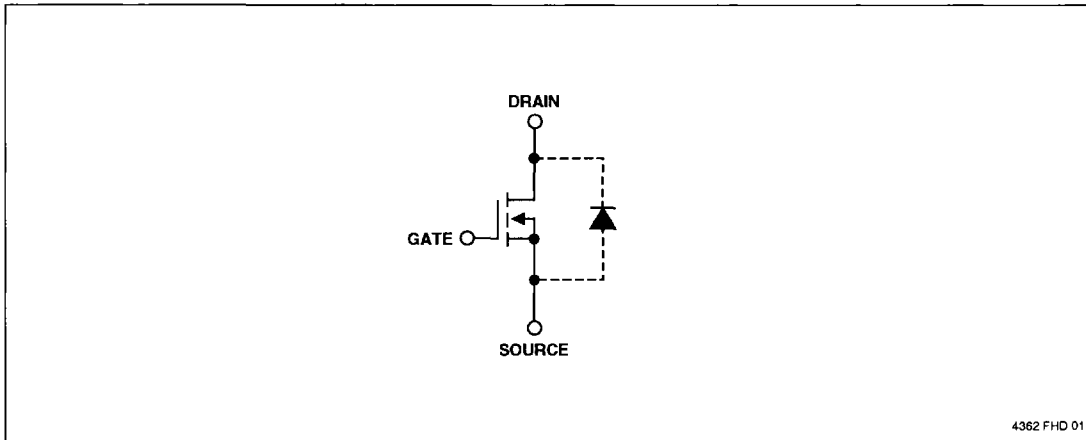
Part No.	Package	Description
VN0610LL	TO-92 Plastic Package	60V, 5 Ω
VN2222LL	TO-92 Plastic Package	60V, 7.5 Ω

ABSOLUTE MAXIMUM RATINGS

Drain-Source Voltage	+60V
Drain-Gate Voltage ($V_{GS} = 0$)	+60V
Gate-Source Voltage	$\pm 40V$
Continuous Drain Current	
VN0610LL	
$T_A = +25^\circ C$	0.18A
$T_C = +25^\circ C$	0.32A
VN2222LL	
$T_A = +25^\circ C$	0.15A
$T_C = +25^\circ C$	0.26A
Peak Pulsed Drain Current	1.0A
Continuous Device Dissipation	
$T_A = +25^\circ C$	0.3W
$T_C = +25^\circ C$	1.0W
Linear Derating Factor	
$T_A = +25^\circ C$	2.4mW/ $^\circ C$
$T_C = +25^\circ C$	8.0mW/ $^\circ C$
Operating Junction	
Temperature Range	-55 to +150 $^\circ C$
Storage Temperature Range	-55 to +150 $^\circ C$
Lead Temperature (1/16" from mounting surface for 30 sec)	+260 $^\circ C$

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



4362 FHD 01

N-CHANNEL ENHANCEMENT-MODE DMOS POWER FETs

VN0610LL
VN2222LL

ELECTRICAL CHARACTERISTICS: ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	VN0610LL			VN2222LL			Units
			Min	Typ	Max	Min	Typ	Max	
Static									
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 100\mu\text{A}, V_{GS} = 0$	60	100	—	60	100	—	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	$I_D = 1.0\text{mA}, V_{DS} = V_{GS}$	0.8	1.9	2.5	0.6	1.9	2.5	V
I_{GBS}	Gate-Body Source Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0$	—	± 1.0	± 100	—	± 1.0	± 100	nA
I_{DSS}	Drain-Source OFF Leakage Current	$V_{DS} = 48\text{V}, V_{GS} = 0$	—	0.1	10	—	0.1	10	μA
		$V_{DS} = 48\text{V}, V_{GS} = 0$ $T_A = 125^\circ\text{C}$	—	5.0	500	—	5.0	500	μA
$I_{D(on)}$	ON Drain Current	$V_{DS} = 10\text{V}, V_{GS} = 10\text{V}^{(1)}$	1.0	2.2	—	1.0	2.2	—	A
$V_{DS(on)}$	Drain-Source ON Voltage	$V_{GS} = 5\text{V}, I_D = 0.2\text{A}^{(1)}$	—	0.9	1.5	—	0.9	1.5	V
		$V_{GS} = 10\text{V}, I_D = 0.5\text{A}^{(1)}$	—	1.5	2.5	—	1.5	3.75	
$r_{DS(on)}$	Drain-Source ON Resistance	$V_{GS} = 5\text{V}, I_D = 0.2\text{A}^{(1)}$	—	4.5	7.5	—	4.5	7.5	Ω
		$V_{GS} = 10\text{V}, I_D = 0.5\text{A}^{(1)}$	—	3.0	5.0	—	3.0	7.5	
		$V_{GS} = 10\text{V}, I_D = 0.5\text{A}^{(1)}$ $T_A = +125^\circ\text{C}$	—	4.7	9.0	—	4.7	13.5	
Dynamic									
g_{fs}	Common-Source Forward Transcond	$V_{DS} = 10\text{V}, I_D = 0.5\text{A}$ $f = 1\text{kHz}^{(1)}$	100	400	—	100	400	—	mmhos
C_{iss}	Common-Source Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$	—	80	100	—	80	100	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$	—	1.3	5.0	—	1.3	5.0	pF
C_{oss}	Common-Source Output Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$	—	10.5	25	—	10.5	25	pF
t_{on}	Turn-On Time	$V_{DD} = 15\text{V}, V_{G(on)} = 10\text{V}$ $R_G = 25\Omega, R_L = 25\Omega$	—	5.0	10	—	5.0	10	nSec
t_{off}	Turn-Off Time	$V_{DD} = 15\text{V}, V_{G(on)} = 10\text{V}$ $R_G = 25\Omega, R_L = 25\Omega$	—	6.0	10	—	6.0	10	nSec

NOTE: 1. Pulse Test 80 μ Sec, 1% Duty Cycle