24 Mbit/sec Data Synchronizer, (1,7) ENDEC, Frequency Synthesizer, and Write Precompensation with Register Controls

Preliminary Information

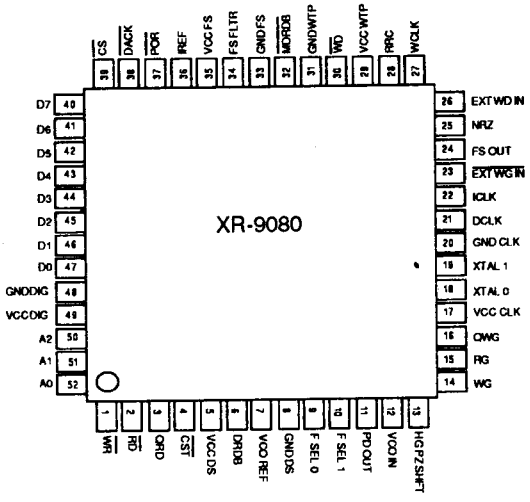
GENERAL DESCRIPTION

The XR-9080 combines the functions necessary for Data R/W in a zoned recording system at multiple data rates. It features high-speed, single +5V supply, low power fully integrated Data Synchronizer, 1,7 RLL ENDEC,PLL Clock Recovery, and a complete M divide by N ratio Frequency Synthesizer. In combination with a disk controller IC, a pulse detector IC, a Read/Write Preamp, and a microcontroller, the electronics of a disk drive system utilizing the 1,7 RLL recording format is realized. All functions can be controlled by the drive control microcontroller via a byte-wide demultiplexed parallel interface. The XR-9080 is implemented in a high performance BiCMOS process, giving low power dissipation through CMOS logic and providing accurate timing with the bipolar integrated PLL.

FEATURES:

Low Noise, Low Jitter Data Separator
Zero Phase VCO Restart to both Data and Crystal
Programmable Lock Detect Field Length
(4 - 31 bits)
Programmable PLL Loop Filter Adjustment:
2 pins for Zones under Register control
1 pin for High Gain adjust during
Lock Detect
Four Levels of Charge Pump Current,
Register Selectable
High Gain Mode during Lock Detect,
Register Selectable
Microprocessor Controlled VCO Center Frequency
and 1/3 Cell Delay Centering
High Speed 1,7 RLL ENDEC
Tunable Write Precompensation
Ratio controlled Frequency Synthesizer
Intended for Any Zoned Recording Application
Advanced BiCMOS technology
Programmable Readback Window Margin Capability
Typical Power Dissipation: 350 mW at 20 Mbits/sec

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-9080CQ	52 Pin QFP	0 °C to 70 °C

APPLICATIONS

SCSI Bus Hard Disk Drives
IDE Interface (AT) Hard Disk Drives
ESDI Bus Hard Disk Drives

ABSOLUTE MAXIMUM RATINGS

VCC DS, VCC CLK, VCC WTP, VCC FS, VCC DIG	+7VDC
Digital Inputs	-0.3V to VCC DIG + 0.3V
Junction Temperature	150 °C
Storage Temperature	-65 °C to 150 °C

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ELECTRICAL CHARACTERISTICS

Test Conditions:

TA = 25 °C

4.75 VDC ≤ VCC DS = VCC CLK = VCC WTP = VCC FS = VCC DIG ≤ 5.25 VDC.

7.5 MHz ≤ 1 / TORC* ≤ 24 MHz, 22.5 MHz ≤ 1/TVCO ≤ 72 MHz

Digital Load Capacitance limited to 15 pF.

*TORC = Time of One Recording Cell

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
ICC	Supply Current		40	60	mA	
PD	Power Dissipation		200		mW	1/TORC =15MHz
DIGITAL SIGNALS						
VIL	Input "Low" Voltage			0.8	V	
VIH	Input "High" Voltage	2.0			V	
IIL	Input "Low" Current	-0.4			mA	VIL = 0.4 V
IIH	Input "High" Current			10	µA	VIH = 2.4 V
VOL	Output "Low" Voltage			0.4	V	IOL = 4 mA
VOH	Output "High" Voltage	2.8	4.8		V	IOH = -0.4 mA
READ MODE						
	Maximum Data Rate		24.0		Mb/s	
TRD	Read Data Pulse Width	15	TORC - 20		ns	
TFRD	Read Data Fall Time		15		ns	2.0V to 0.8V
TRRC	Read Clock Rise Time		8		ns	0.8V to 2.0V
TFRC	Read Clock Fall Time		5		ns	2.0V to 0.8V
TPNRZ	NRZ Set Up/ Hold Time	.31 TORC			ns	
	1/3 Bit Cell Delay	.8TD		1.2TD	ns	TD = .5 TVCO
WRITE MODE						
TWD	Write Data Pulse Width	.94 TVCO		1.06TVCO	ns	
TFWD	Write Data Fall Time			8	ns	
TRWC	Write Data Clock Rise Time			10	ns	0.8V to 2.0V
TFWC	Write Data Clock Fall Time			8	ns	2.0V to 0.8V
TSNRZ	WDNRZ Pin Set Up Time	5			ns	
THNRZ	WDNRZ Pin Hold Time	5			ns	
WRITE PRECOMPENSATION						
TPC	Precompensation Time Shift Magnitude Accuracy					TPC0 = .02TVCO WPC0, WPC1 in register 7
	$\overline{WPC0}$ = 1 $\overline{WPC1}$ = 1					No Shift, This setting
	$\overline{WPC0}$ = 0 $\overline{WPC1}$ = 1	0.8* TPC0 -0.2		1.2* TPC0 +0.2	ns	
	$\overline{WPC0}$ = 1 $\overline{WPC1}$ = 1	1.6* TPC0		2.4* TPC0	ns	
	$\overline{WPC0}$ = 0 $\overline{WPC1}$ = 0	2.4* TPC0		3.6* TPC0	ns	

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DATA SEPARATOR						
KVCO	VCO Control Voltage Gain	0.14 ω_0		0.26 ω_0	rad/ sec V	$\omega_0 = 2\pi/TO$ 1V ≤ VCO IN ≤VCC - 0.6V
KD	Phase Detector Gain	0.83 KD		1.17 KD	A/rad	$KD = \frac{(VCC - VBE)*N}{2\pi(RREF + 1K)}$ N = 1, 1.5, 2, 2.5, per Register 5 bits 1, 0
	KD * KVCO Product Accuracy	-28		+28	%	
	VCO Restarted Phase Error	-10		+10	ns	To RRC
	Decode Window Centering Accuracy		±2		ns	
	Decode Window	(2/3 * TORC) - 2			ns	
FREQUENCY SYNTHESIZER						
KVCO	VCO Control Voltage Gain	0.14 ω_0		0.26 ω_0	rad/ sec V	$\omega_0 = 2\pi/TO$ 1V ≤ VCO IN ≤VCC - 0.6V
KD	Phase Detector Gain	0.83 KD		1.17 KD	A/rad	$KD = \frac{(VCC - VBE)*N}{2\pi(RREF + 1K)}$ VCC = 5.0V PLL REF = RD
	KD * KVCO Product Accuracy	-28		+28	%	
SWITCHING CHARACTERISTICS (see fig. 1 and 2 for waveforms)						
tcsswr	Chip select set up before Write Reg-assertion	10			ns	
tcshwr	Chip select Hold time after Write Reg-deassertion	10			ns	
tdaswr	Data and Address Set up before Write Reg-assertion	10			ns	
tdahwr	Data and Address Hold time after Write Reg-assertion	10			ns	
tpwwr	Pulse width of Write Reg-	50			ns	
tpdawr	Propogation delay from Write Reg- to Acknowledge-assertions			10	ns	
tcssrd	Chip select Set up before Read Reg-assertion	10			ns	
tcshrd	Chip select Hold time after Read Reg-assertion	10			ns	
tasrd	Address Set up time before Read Reg-assertion	10			ns	
tahrd	Address Hold time after Read Reg-deassertion	10			ns	
tpwrd	Pulse width Read Reg-	50			ns	
tpdard	Propogation delay from Read Reg- to acknowledge assertions			10	ns	
tpdvrd	Propogation delay from Read Reg- assertion to Data valid			10	ns	
tdhrd	Data hold time after Read Reg-deassertion	0			ns	

SYSTEM INFORMATION

The XR-9080 is a 24 MBit/sec 1,7 RLL Data Synchronizer, ENDEC, and Frequency Synthesizer implemented in a BiCMOS process. This allows for independent optimization of the linear VCOs and charge pumps in high performance bipolar technology, while using fine geometry and low power CMOS for the ENDEC logic functions, the control DACs, and the microcontroller interface. The resultant device is faster, more compact, and lower power dissipation than any bipolar implementation of the same functions. The XR-9080 data rate is adjusted via register controlled, internal DACs. The register control of the 9080 is covered in the section called "Registers". All necessary internal timings will track the settings of the DACs and allow zoned recording applications.

PIN DESCRIPTION

Power Pins

Pin #	Symbol	Description
5	VCC DS	+5V for Data Separator, Analog 17 VCC CLK+5V for Clock Output Drivers, Digital
29	VCC WTP	+5V for Write Precompensation Circuit, Analog
35	VCC FS	+5V for Frequency Synthesizer, Analog
49	VCC DIG	+5V for ENDEC and Microcontroller Interface, Digital
8	GND DS	Ground for Data Separator, Analog
20	GND CLK	Ground for Clock Output Drivers, Digital
31	GND WTP	Ground for Write Precompensation Circuit, Analog
33	GND FS	Ground for Frequency Synthesizer Section, Analog
48	GND DIG	Ground for ENDEC and Microcontroller Interface, Digital

Control Pins

52	A0	Least significant Register selection address bit
51	A1	Address bit 1
50	A2	Most significant Register selection address bit
47	D0	Least significant Register Data bit read or written
46	D1	Register Data bit read or written
45	D2	Register Data bit read or written
44	D3	Register Data bit read or written
43	D4	Register Data bit read or written
42	D5	Register Data bit read or written
41	D6	Register Data bit read or written
40	D7	Most significant Register Data bit read or written
39	$\overline{CS}$	9080 Chip Select, input, asserts low. Allows writing to or reading from addressed register.
1	$\overline{WR}$	Write Register control, input, asserts low. Latches are state controlled, not edge triggered, therefore address and data inputs should be held valid for full time period that $\overline{WR}$ input is asserted.
2	$\overline{RD}$	Read register control, input, asserts low. Controls the direction switching of the data bus, turning it into outputs. This occurs only when register 3 or 7 is addressed and $\overline{RD}$ is asserted.
38	$\overline{DACK}$	Data Acknowledge,output asserts low. Pulses low after the $\overline{WR}$ or $\overline{RD}$ inputs asserts low and $\overline{CS}$ active. This output is OCL and requires an external pullup.Used for Microcontroller handshake.
37	$\overline{POR}$	Power On Reset, input, asserts low. This input initializes the state of various flip-flops. After initialization, the device register can be properly loaded.

Read Mode Pins

Pin #	Name	Description
3	QRD	Qualified Read Data, input, asserts high. Digital data stream input, 1,7 RLL format.
4	$\overline{CST}$	Coast, input, asserts low. Provides capability to disable the phase detector in the Data Separator. This allows the user to set up applications where the QRD input can have sections of servo and the clock/PLL can "coast over" them without being affected.
6	$\overline{DRD}$	Delayed Read Data, output, asserts low. Provides the delayed version of the QRD signal (after the 1/3 cell delay circuit). DRD runs at ECL levels.
32	$\overline{MDRD}$	Margin Delayed Read Data, output, asserts low. Provides a delayed version of the QRD signal that has also gone through the margin delay circuit. Magnitude of delay available at this output is under control of register 6, bits 5 through 0.The positive edge is the real bit, and is an ECL output which requires a 1 K pull down resistor to ground.
7	VCOREF	VCO Reference Clock. Test point output for Readback Clock
9	F SEL 0	Filter Select Control 0, open collector output to change the PLL loop filter characteristics. Set by register 7 bit 6.
10	F SEL1	Filter Select Control 1, open collector output. Set by register 7 bit 5.
11	PD OUT	Phase Detector Output. Analog output of current pulses of the Data PLL phase detector and charge pump. Normally connected to the loop filter.
12	VCO IN	Voltage Controlled Oscillator Input. Controlling input for the VCO operating point. Also normally connected to the loop filter .
13	HG PZ SHFT	High Gain Phase Shift. Open collector output provides dynamic grounding to change the filter configuration. This occurs while switched into High Gain, during Lock Detect mode.
15	RG	Read Gate, input. Provides overall control of the read operation. When asserted starts the lock detect counter, and switches to the high gain acquisition state of the PLL.
25	NRZ	Non Return to Zero Data. This bi-directional pin is an input in the write mode for the NRZ write data. In all other modes it is an output for the data decoder. The decoder is only active in the readback operation.
28	RRC	Readback Reference Clock. The RRC output is (in all modes except after lock detection) the frequency synthesizer clock divided by three. During a read operation, this output is switched to the PLL clock divided by three.

Write Mode Pins

14	WG	Write Gate, input. Allows control of write operations indirectly by controlling the presence of QWG.
16	QWG	Qualified Write Gate, output. Is asserted immediately after WG goes active,and causes 3T pattern to be output from the $\overline{WD}$ pin. After 6 RRC clock cycles, the $\overline{WD}$ output is switched to the NRZ data encoded to 1,7 RLL.When WG is deasserted, QWG stays asserted 6 clock cycles to allow the1,7 ENDEC to completely encode the NRZ input during the write cycle and output to the $\overline{WD}$ pin.

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Pin #	Name	Description
30	$\overline{WD}$	$\overline{Write\ Data}$, output, asserts low. It is a serial data stream of pulses for 1,7 RLL write pattern. This output is intended for a toggling flip-flop in the write circuits of a R/W preamplifier IC. The pulses are encoded from the NRZ input.
27	WCLK	Digital input which clocks the write data input at the NRZ pin. Note that input clocking of the encoder is from the frequency synthesizer output. Therefore WCLK and the NRZ input must be phase /frequency locked to the frequency synthesizer (FS OUT) in order to allow data input flip-flop's timing to be valid.The data latches on the positive edge.
23	$\overline{EXT\ WG\ IN}$	$\overline{External\ Write\ Gate}$, input, asserts low. Register selectable test mode which allows bypassing the WG input.
26	EXT WD IN	External Write Data In. Register selectable test mode which bypasses the NRZ ENDEC for $\overline{WD}$ output.

Frequency Synthesizer

19	XTAL 1	Crystal Input 1. This input is the active node which is either connected to a passive crystal reference or driven actively by direct drive at CMOS levels. TTL input levels should be capacitively coupled.
18	XTAL 2	Crystal Input 2. This is the non-active node. When driving XTAL 1 with a CMOS level clock, this pin should be left floating.
21	DCLK	Digital Clock. TTL level output of the crystal oscillator which can be switched off under internal register control.
22	ICLK	Internal Clock. TTL level output of the crystal oscillator, continuously running.
24	FS OUT	Frequency Synthesizer Output. The output buffer of the Frequency Synthesizer may be turned off under register control.
34	FS FLTR	Frequency Synthesizer Filter. This pin is common to both the frequency synthesizer charge pump output and the VCO control voltage input.Analog Inputs
36	IREF	Reference Current Input. Establishes all modes and delays operating point currents. Requires resistor to VCC DS synthesizer clock divided by three. During a read operation, and after lock detection, this output is switched to the PLL clock which is derived from the RLL data stream.

CIRCUIT OPERATION

The three basic operational modes of the XR-9080 are Idle, Read and Write. Idle mode is selected by deasserting BOTH pins RG and WG. Read is selected by asserting RG and Write is selected by asserting WG. Asserting BOTH pins RG and WG is an illegal state, and the last asserted will be ignored.The common operation to both Read and Write modes is the selection of the data rate, and the use of the XTAL inputs to generate internal clocks. A series resonant crystal should be installed between the pins XTAL 1 and XTAL 2. Optionally, two capacitors to ground can be connected to these inputs when using a crystal. Alternately, a CMOS level clock can be used to drive the XTAL 1 input, and the XTAL 2 input should then be left floating. Also a TTL level clock can be capacitively coupled to XTAL 1 input, and the XTAL 2 input be left floating. The output of the crystal oscillator is fed to the frequency synthesizer which develops the frequency used for both writing data and readback data recovery.

The Frequency Synthesizer output frequency is set by the formula:

$$Fout = \frac{2\,(NUM)\,Fin}{(DEN)}$$

Where:

Fout = Frequency available at FSOUT.
Fin = Frequency applied at XTAL1,2 inputs.
NUM = NUMerator placed in B5-B0 of R0.
DEN = DENominator placed in B6-B0 of R1.

READ MODE

For a read operation, the user asserts RG, when the head is over the 3T Preamble. The PLL immediately begins the Preamble count. This starts the following sequence of operations:

1. Preamble is recognized upon the presence of 3 data bits.

2. Recognition of preamble switches phase detector input from reference clock to delayed readback data (DRD).

3. PLL acquisition, with zero phase restart, begins with the first readback pulse seen after switching of the phase detector input. Lock Detect Counter (register 4) is started. If enabled by register 7, High Gain mode is entered and HIGH GAIN PZ SHIFT becomes a ground, and the Charge Pump currents are quadrupled.

4. The number of pulses specified in register 4 are counted, then decoder functions are started, RRC switches to the readback clock, and decoded data is output from the pin NRZ.

8. Decoded data and readback clock are continually output until RG deasserts.

WRITE MODE

For a write operation, the user should assert WG. This becomes the first step in a sequence of operations:

1. WG input is asserted and NRZ input should begin. WD output outputs 3T pattern immediately.

2. Six cycles of RRC are counted.

3. QWG asserts and encoded RLL output at WD begins.

4. Encoded RLL output continues until deassertion of WG.

5. QWG remains asserted for 6 RRC clocks after the deassertion of WG. $\overline{WD}$ continues encoding until QWG deasserts. This insures that the last data bit is flushed from the encoder in a Write.

This part has a secondary Write mode which is used in a similar manner. First, set the ENAWR (Enable Write) bit placed in register 3. After that, assert $\overline{EXT\ WG\ IN}$ (External Write Gate In) and input data Pulses, (Active low) on the input EXT WD IN. These will bypass the encoder and go directly to the $\overline{WD}$ output and to the preamplifier to be recorded.

SPECIAL FEATURES

$\overline{COAST}$ feature:

When it is asserted, the currents that would flow for a phase error are not output to the loop filter from the PD OUT pin. In effect, the voltage on the loop filter is held constant by this lack of current flow until $\overline{COAST}$-is deasserted. Since Read Gate (RG) is asserted, NRZ decoding continues and is output, and Read Reference Clock is still the PLL VCO divided by 3. There is no "high-gain" mode (High current output from the phase detector,and filter modification signals true) for the device available at $\overline{COAST}$- deassertion. In addition, the zero phase restart logic is not armed by $\overline{COAST}$-. Phase lock is NOT guaranteed after deassertion, no matter the time duration of the $\overline{COAST}$- assertion.

In terms of timing, it should only be asserted after the user data field has been entered, i.e. RG should be asserted and several bytes of data decoding have occurred.

Above Voltage monitor bit (Register 3, B0):

This feature allows the drive microprocessor to set the VCO to the center of its capture range, and to

remove any offset error from the delay one-shots in the Data Separator. By changing the setting of the VCO DAC via register 2, the drive microprocessor can maximize the loop lock range, and minimize margin timing error at power up. The comparator driving this bit allows for setting the VCO DAC (Register 2) to place the Data Separator VFO to its mid-point of operation. It is intended for use as a power-up time calibration, but can be done at any time power is applied to the XR-9080. The microprocessor which loads the register values monitors this bit in the following algorithm:

1. Set the Numerator and Denominator values for the first data rate in Register 0 and 1, respectively.

2. Write the nominal value chosen to the VCO DAC, Register 2.

3. Read the Above Voltage bit: If it is HIGH, decrease the value in Register 2 by 1. If it is LOW, increase the value in Register 2 by 1.

4. Read the bit again; if it has reversed polarity store the value written to Register 2 as the Calibrated VCO DAC Register 2 value for future use when in that zone. If it has not, repeat step 3.

5. Repeat the same procedure (steps 1 to 4) for all zones and store the Calibrated Register 2 values for future use.

REGISTERS

REGISTER ADDRESS (A2-A1-A0)	REGISTER FUNCTION	REGISTER ACCESS
R0 (000)	Frequency Synthesizer: Enable Phase Detector Numerator	Write
R1 (001)	Frequency Synthesizer: Enable Phase Detector Denominator	Write
R2 (010)	Frequency Synthesizer VCO Operating Range DAC	Write
R3 (011)	Assorted Control Bits: Frequency Synthesizer Output Enable Low Power Mode Control Enable External Write Data Mode VCO Correction vs. Reference Voltages	Read & Write
R4 (100)	Lock Detect Field Length	Write
R5 (101)	Charge Pump Current	Write
R6 (110)	Window Margin Controls: DAC for Window Margin Delay Select/Eliminate Window Margin Data	Write
R7 (111)	Assorted Control Bits: Filter Switch Selection Enable High Gain PLL Acquisition Write Precompensation Magnitude D Clock Output Enable	Read & Write

R0, R1, & R2 FREQUENCY SYNTHESIZER & PLL CONTROL REGISTERS

R0 & R1 are totally devoted to control of the frequency synthesizer. R2 controls the operating point of the VCOs in both the frequency synthesizer and the PLL.R3,R7 each contain 1 bit which can affect the output of the frequency synthesizer or one of it's clocks.The frequency synthesizer output is primarily a function of three registers and the reference frequency from the crystal oscillator. Output of the frequency synthesizer is available at the FS OUT pin. This output may be switched on/off under control of R3, B3.ENPD, asserted high, enables the phase detector in the frequency synthesizer.The state of this one bit is controlled by B7 of either R0 or R1. Last register loaded controls the state of the bit.Nominal operating point of the VCO in the synthesizer and the VCO in the PLL are under control of a single DAC, with digital control placed under R2, B7-B0. Setting of VCDAC = 11111111 will achieve max operating frequency capability. Setting to 0 will give the minimum. Monitoring of the AV (Above Voltage) control bit, R3, B0, will aid in the setting of the VCO's to a nominal operating point.

REG#	MSB							LSB
R0:	B7	B6	B5	B4	B3	B2	B1	B0
	+ENPD	DC	NUM5	NUM4	NUM3	NUM2	NUM1	NUM0

REG#	MSB							LSB
R1:	B7	B6	B5	B4	B3	B2	B1	B0
	+ENPD	DEN6	DEN5	DEN4	DEN3	DEN2	DEN1	DEN0

REG#	MSB							LSB
R2:	B7	B6	B5	B4	B3	B2	B1	B0
	VC	VC	VC	VC	VC	VC	VC	VC
	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

(DC = Don't Care, Bit has no internal use.)

R3 CONTROL BITS

EFSOUT - Enable Frequency Synthesizer Output. Bit placed high here enables the output buffer for the frequency synthesizer, bringing FSOUT active. EXDWR - EXternal Data WRite. Before the device can accept the External Write Gate In control and write pulses from the External Write Data in pins, this bit must be set high. To do a normal write, this pin should be reset.

LP - Low Power. Setting this bit high switches the chip into low power mode, shutting down as much circuitry as possible to minimize power consumption. Cycling of POR control after bringing power up on the device will leave this bit set in low power mode. Consequently, the power-up cycling of the device will require: a) turning on of power supplies, b) cycling low of POR briefly to initialize registers, flip-flops, and latches, c) loading of the LP bit with a low state to put the IC into a fully functional mode, d) loading of all registers with proper data necessary for desired operating parameters.

AV - Above Voltage. Readback of a high logic state here indicates that the PLL correction voltage is above that of the reference voltage. Reference voltage equals 2.7 volts, middle of the VCO operating range. Readback of the AV bit while adjusting VCDAC, R2, will allow the user to adjust for a nominal operating point.

REG#	MSB							LSB
R3:	B7	B6	B5	B4	B3	B2	B1	B0
	DC	DC	DC	DC	+EFSOUT	+ENAWR	+LP	+AV

R4 - DEFINITION OF PLL LOCKUP FIELD LENGTH

LDL4 - LDL0: The value placed in this 5 bit register/counter determines the number of data pulses counted before the LOCK DETECT signal is asserted. The number placed here will be counted to, in the form of pulses present at the DRD pin. After this count the mode of the PLL will change from High Gain to Track. This drops the loop into low gain mode, and switches the RRC output from the frequency synthesizer divided by to PLL VCO divided by 3.

REG#	MSB							LSB
R4:	B7	B6	B5	B4	B3	B2	B1	B0
	DC	DC	DC	LDL4	LDL3	LDL2	LDL1	LDL0

R5 - DATA SEPARATOR CHARGE PUMP GAIN

Two bit control of the charge pump provides a gain range of 4:1under register control. Currents available at the charge pump output are:

QP1	QP0	PUMP CURRENT
0	0	I_0
0	1	$1.5 * I_0$
1	0	$2.0 * I_0$
1	1	$2.5 * I_0$

$$I_0 = \frac{1.25 * (VCC - Vbe)}{(RREF + 1\ K)}$$

REG#	MSB							LSB
R5:	B7	B6	B5	B4	B3	B2	B1	B0
	DC	DC	DC	DC	DC	DC	QP1	QP0

R6 - MARGIN DELAY; MAGNITUDE CONTROL AND SELECTION

This register sets the optional margin delay of the Data Separator. It is a separate data path from the normal 1/3 cell delay used in decoding, and is enabled by a write to this register B6. The time relationship is for a capacitor being charged by a current, so the delay is INVERSELY proportional to the setting (+/-) of this DAC.The delay is approximately:

Tdelay =TBD

MDENA: Margin Delay Enable. Controls multiplexing selection of data stream into data detection and synchronization (DD&S) module. When set high, data stream follows path through margin delay circuit into DD&S. Low setting of MDENA takes data stream through 1/3 Cell Delay module.

MD5 - MD0: Margin Delay Control DAC. Controls magnitude of the margin delay time period. Setting all bits high will give maximum delay time period.

REG#	MSB							LSB
R6:	B7	B6	B5	B4	B3	B2	B1	B0
	DC	MDENA	MD5	MD4	MD3	MD2	MD1	MD0

Write Precompensation Pattern

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-2	n-1	n	n+1	n+2	BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.
EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

R7 - ASSORTED CONTROL BITS

FS1, FS0: Filter Select 1, Filter Select 0. High assertion states on these control bits bring the corresponding FSEL0 and FSEL1 filter control lines down into a low impedance (< 100 Ohms), ground output state.

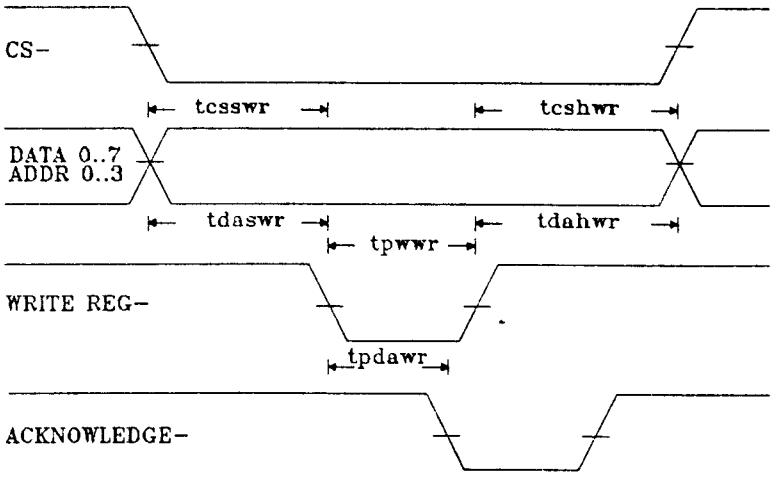
HG: High Gain. High assertion on this control bit allows for a high gain lockup mode during clock acquisition to the data stream. The High Gain is 4 times the normal loop gain, and is changed by quadrupling the Charge Pump current programmed in register 5. The High Gain mode extends between the assertion of READ GATE plus 3 data pulses and LOCK DETECT timeout of the number of bits set in register 4.

WPC1, WPC0: Write Precompensation Magnitude. Controls magnitude of the phase shifts introduced during the write precompensation process. Please note that the assertion is complementary/low for these inputs, i.e. 00gives maximum time shift:

WPC1	WPC0	PRECOMP SHIFT
0	0	3
0	1	2
1	0	1
1	1	0

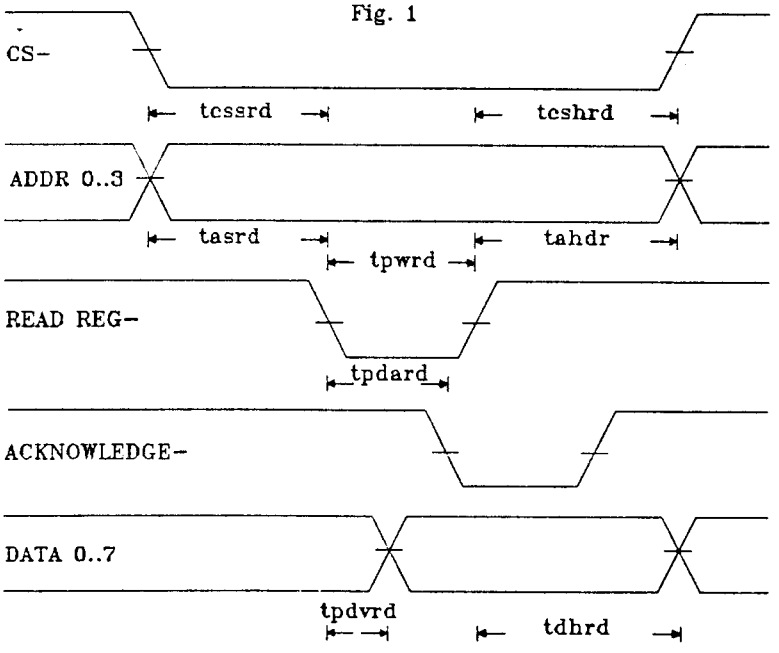
*(3 = Max time shift, 0 = No time precomp.)The actual time shift is Precomp Shift * .02*TVCO*

ENADC: Enable D Clock Output. High assertion state enables the output buffer for the DCLK signal.



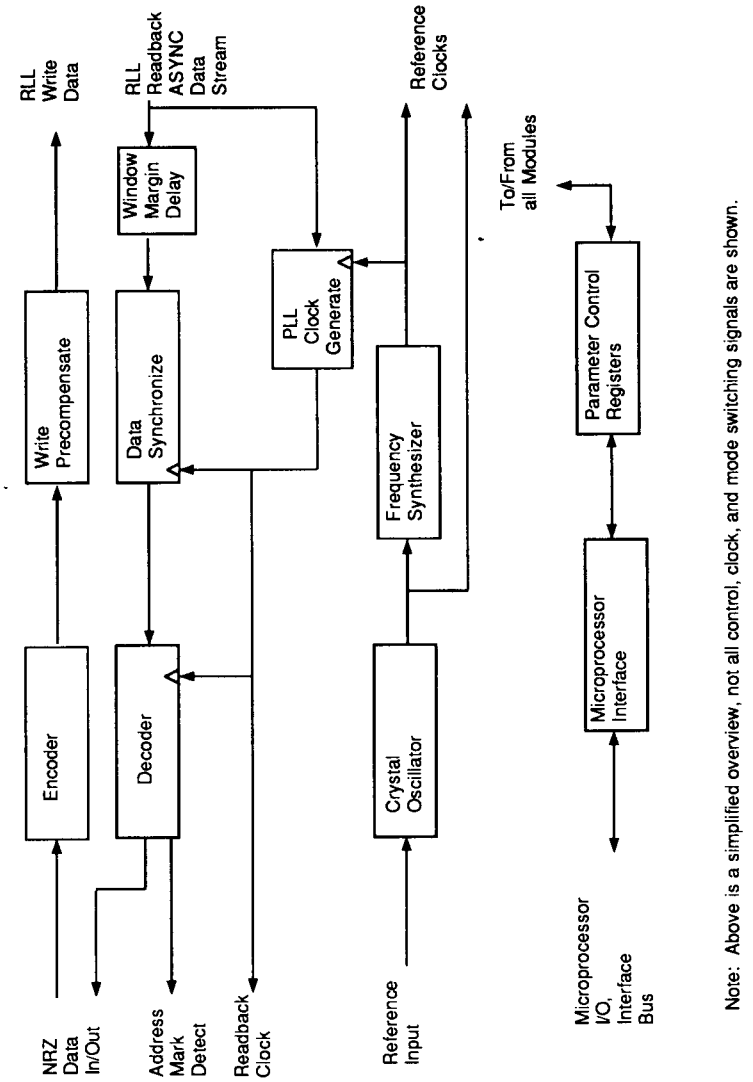
XR-9080 WRITE REGISTER TIMING

Fig. 1



XR-9080 READ REGISTER TIMING

Fig. 2



Note: Above is a simplified overview, not all control, clock, and mode switching signals are shown.

Figure 3. Simplified Functional Overview

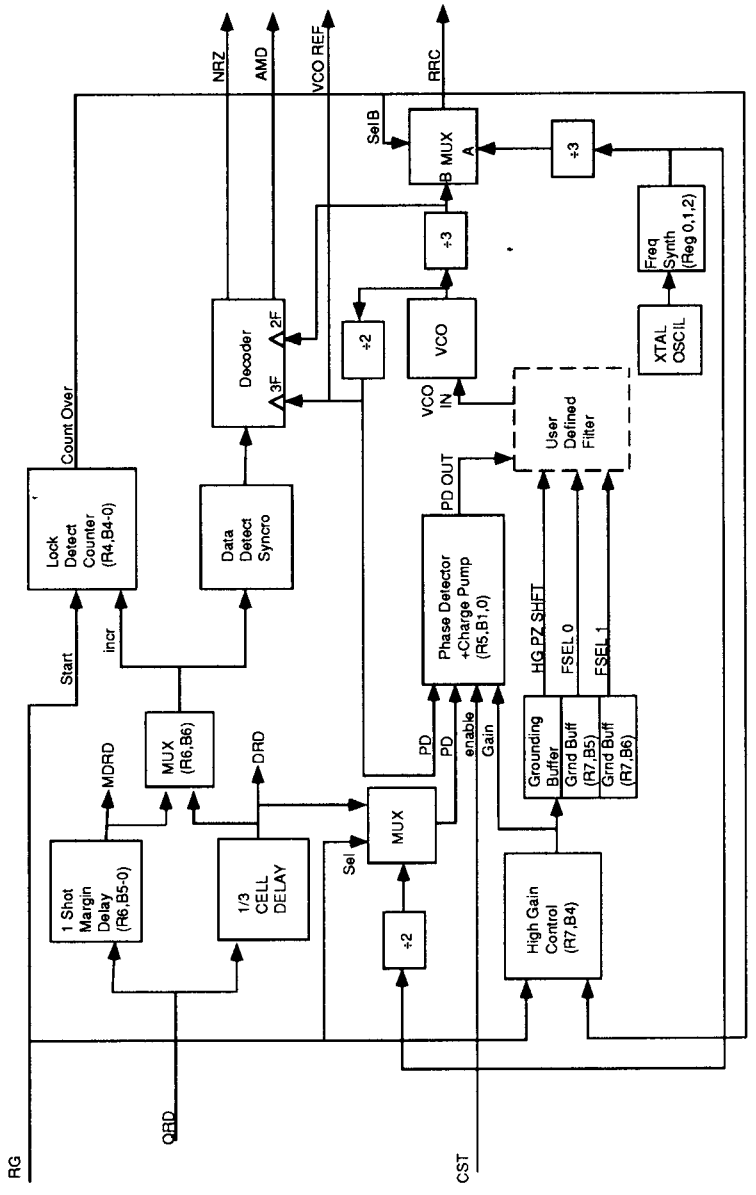
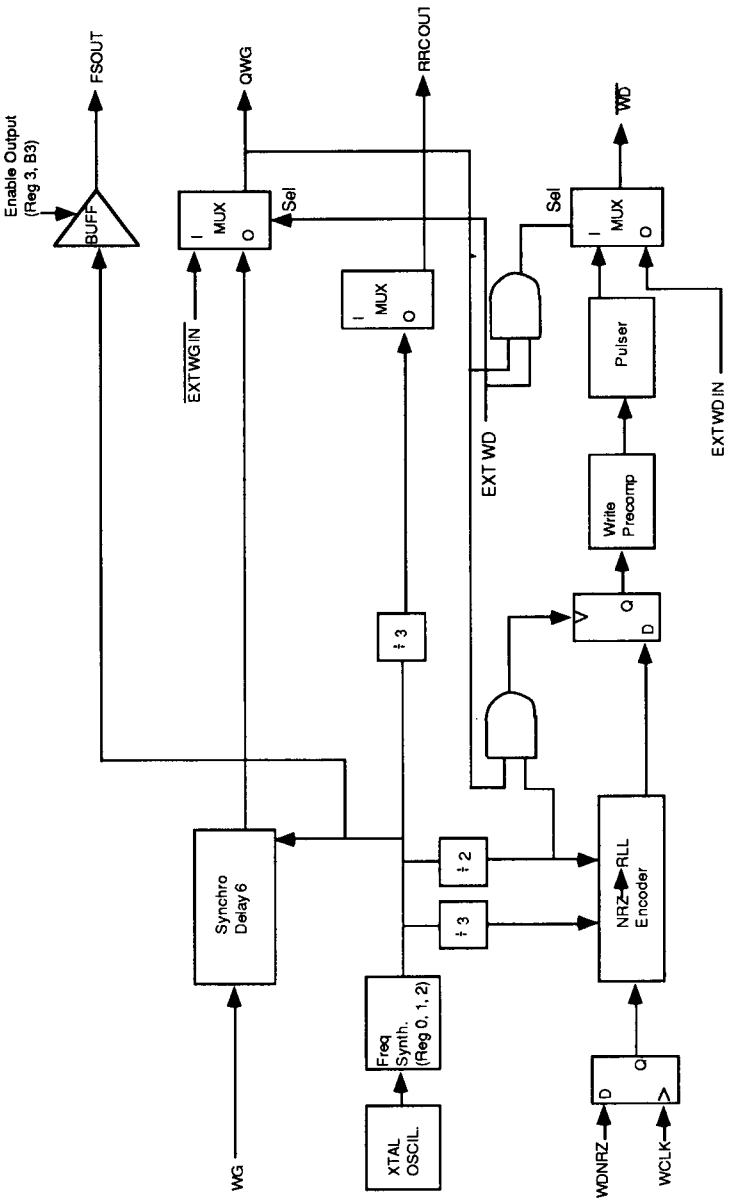
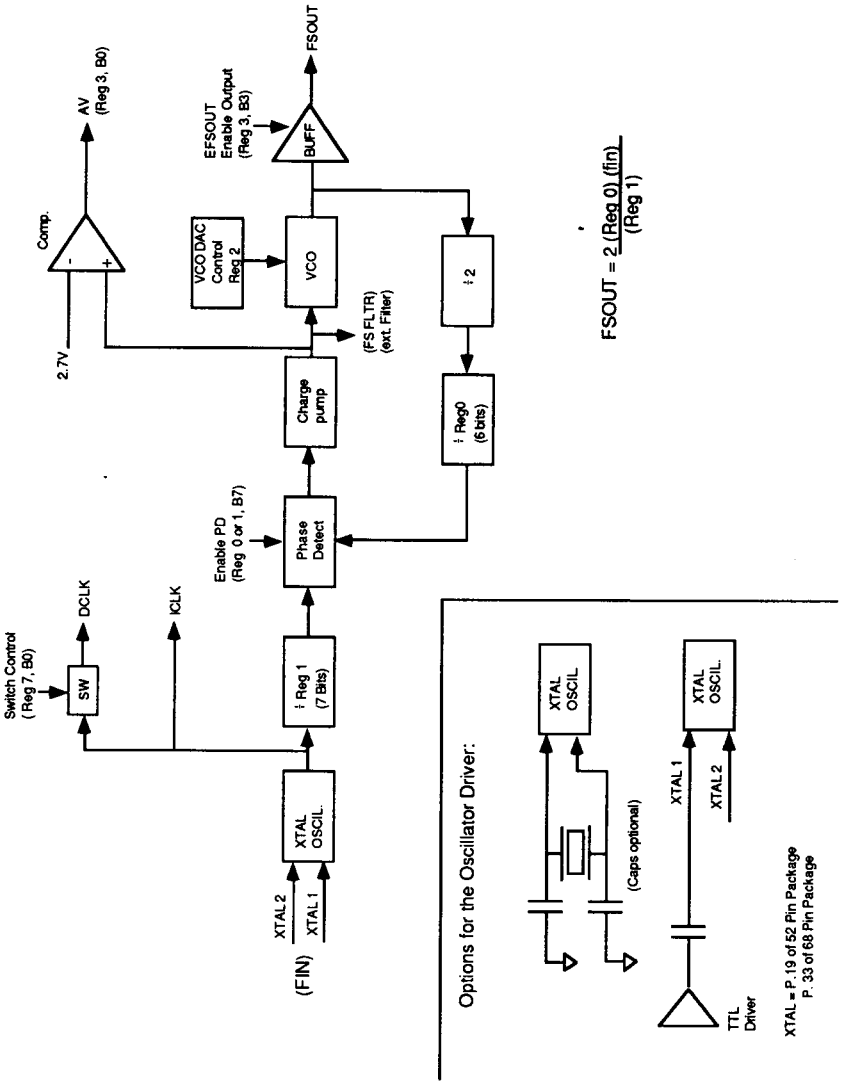


Figure 4. Read Process - 9080



Note: WCLK and the XTAL oscillator must be phase locked for proper Encoder functioning. Generally done by using frequency synthesizer as the WCLK source.

Figure 5. Write Process - 9080



$$FSOUT = \frac{2\,(Reg\ 0)\,(fin)}{(Reg\ 1)}$$

Figure 6. Frequency Synthesizer - 9080

4

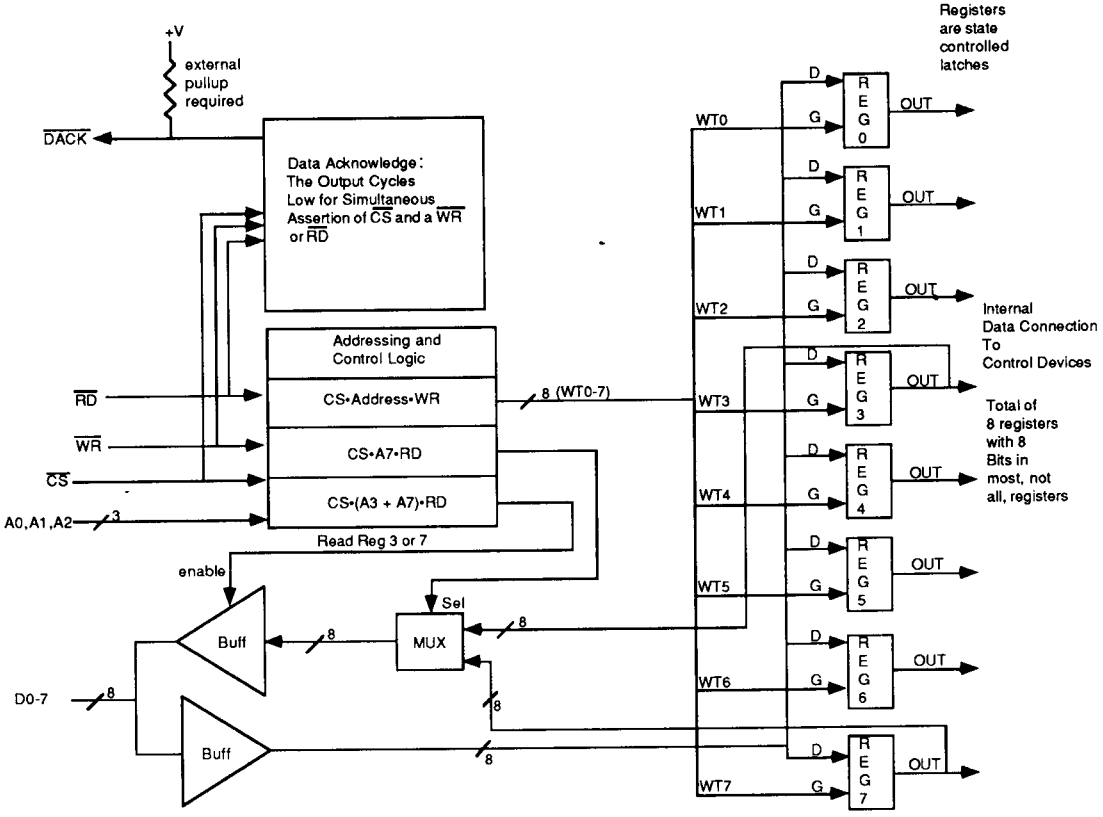


Figure 7. Microprocessor Interface