P/ACTIVE® CLOCK TERMINATION AND FILTER

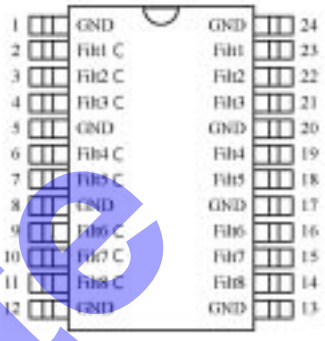
Features

- 8 Channels in Miniature QSOP Package
- Frequency Response to greater than 3 GHz
- Low In-Band Insertion Loss Maintains Signal Integrity
- Low Distortion, Low Cross Talk
- ESD Protected

Applications

- High speed microprocessor clock termination

Pin Assignments



Product Description

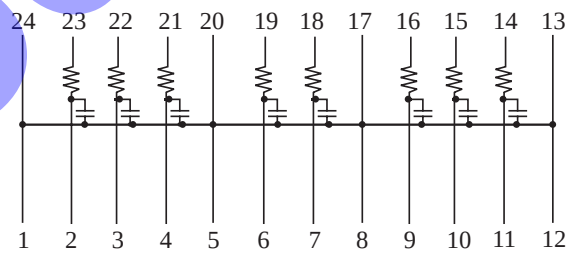
High speed microprocessor systems require well controlled, precise, fast edge-rate clock signals. Clock lines behave as transmission lines for fast-edge signals and therefore the lines may exhibit transients caused by reflections and switching noise. The PACTF clock filter reduces reflections and slows down edges to help reduce EMI/RFI radiation.

California Micro Devices' P/Active Tapped Filter is an integrated thin film resistor-capacitor network designed to filter clock lines and suppress EMI/RFI noise in personal computers and peripherals, workstations, Local Area Network (LAN), Asynchronous Transfer Mode (ATM), and Wide Area Network (WAN). The filter includes ESD protection circuitry which prevents device destruction when subjected to ESD discharges less than 2KV. The ESD protection circuitry permits the filter to operate on bipolar signals of up to ±6V. California Micro Devices' PAC TF is housed in a surface mount package suitable for bottom side mounting to the board. This integrated network solution minimizes space and routing problems and improves reliability and yields.

STANDARD SPECIFICATIONS	
Absolute Tolerance (R)	±10%
Absolute Tolerance (C)	±20%
Operating Temperature Range	0°C to 70°C
Power Rating/Resistor	100mW
Leakage Current	1 µA @ 25°C max.
Crosstalk (see Text Circuit)	< 5% (typical)
ESD Clamp Positive Clamp Negative Clamp	 > 6 Volts < -6 Volts
ESD Protection*	2KV min.
Storage Temperature	-60°C to 150°C
Package Power Rating	1.00W, max.

* ESD Protection level guaranteed by design.

SCHEMATIC CONFIGURATION

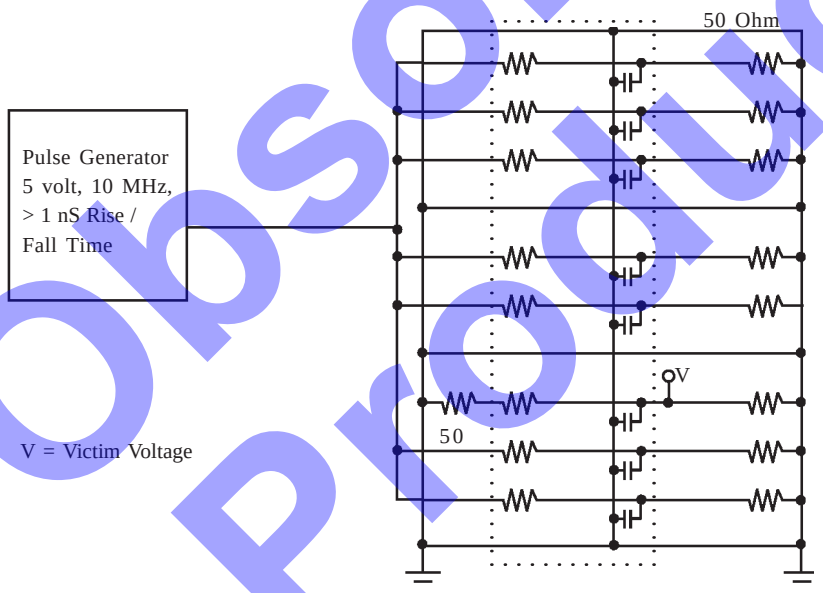


STANDARD VALUES			
R(Ω)	C(pf)	RC Code	fc @ 3db‡
22	10	220/100T	723 MHz
22	15	220/150T	482 MHz
33	10	330/100T	482 MHz
33	15	330/150T	322 MHz

‡ with 0 source impedance

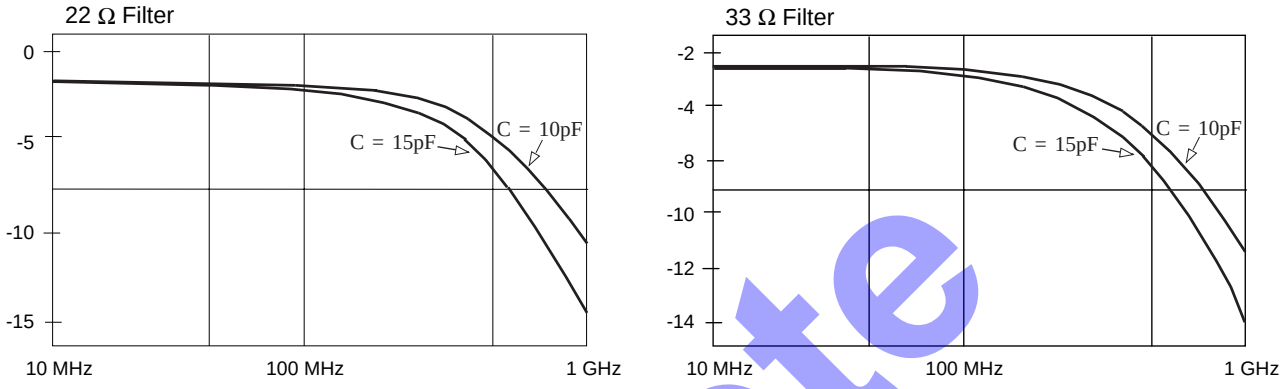
STANDARD PART ORDERING INFORMATION					
	Package		Ordering Part Number		
RC Code	Pins	Style*	Tubes	Tape & Reel	Part Marking
220/100T	24	QSOP	PAC220/100TFQ/T	PAC220/100TFQ/R	PAC220/100TFQ
220/150T	24	QSOP	PAC220/150TFQ/T	PAC220/150TFQ/R	PAC220/150TFQ
330/100T	24	QSOP	PAC330/100TFQ/T	PAC330/100TFQ/R	PAC330/100TFQ
330/150T	24	QSOP	PAC330/150TFQ/T	PAC330/150TFQ/R	PAC330/150TFQ

Filter Cross Talk Test Circuit (T_A=25°C)



Filter Insertion Loss (S12, dB), Typical (T_A = 25°C) Representative Sample

ATTENUATION CURVES



S parameters are measured using a Hewlett Packard HP8753C Network Analyzer with a HP85047A S-parameter Test Set.

Application Information

The PACTF-2 is designed to minimize the EMI/RFI noise from the clock signals on PC motherboards. In order to get the best results, the PACTF should be located as close as possible to the clock generator chips, such as Cypress CY2030 (used for peripherals) and CY2275 (used for CPU, AGP, PCI, and SDRAM).