

Single Rail CODEC

Description

7543 (μ -law) and 7544 (A-law) are CMOS devices containing A companding CODEC And PCM voice filters on a single chip.

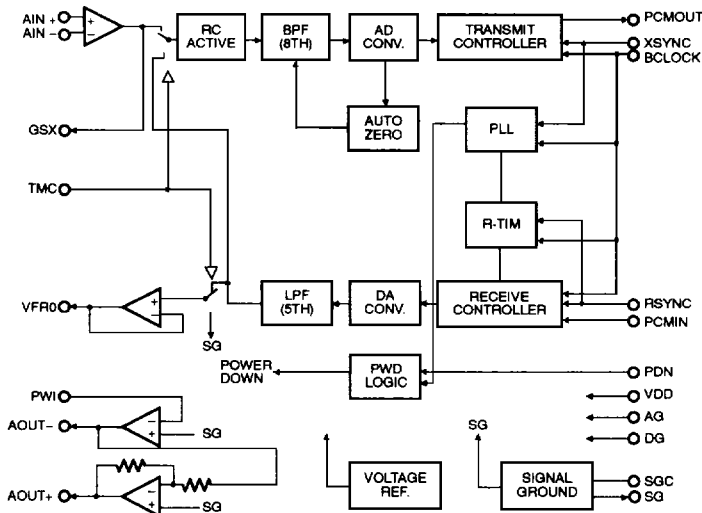
The most featured point is to operate with + 5 V single power supply, which provides cost effective design for ISDN digital telephones, digital portable equipments, digital PABXs, and etc.

Features

- Single Power Supply : + 5 V \pm 5 %
- Low Power Dissipation Operating Mode :
Typ 20 mW, Max 31.5 mW
- Power Save Mode P:
Typ 4.5 mW, Max 8 mW
- Power Down Mode :
Typ 1.5 mW, Max 3 mW
- Companding Law
7543 : μ -law
7544 : A-law
- Complies with CCITT Recommendation G.714
- Transmit/Receive Synchronous Mode Only
- Serial Data Rate : 64/96/128/192/256/384/
512/768/1024/1536/1544/2048 kbps
- Transmit/Receive Gain Adjustable
- Analog Loop Back Test Mode
- On-chip Precision Voltage Reference
- Analog Output : Push-pull Drive, 600 Ω
- Package
20 Pin Skinny DIP :
24 Pin SOIC :

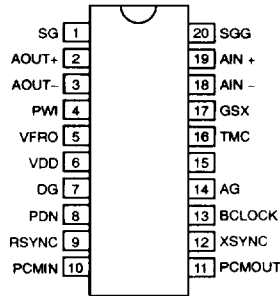
Interface

Block Diagram

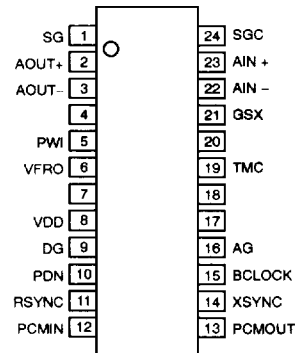


7543/7544

Pin Assignment



**DIL 20 pin
Top view**



**SOIC 24 pin
Top view**

Pin Description

AIN+, AIN-, GSX

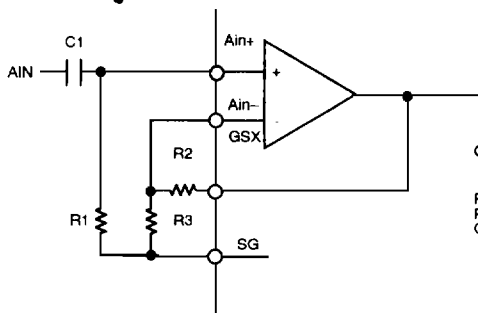
These three pins are used for the transmit gain adjustment.

AIN+ is a non-inverting input of the transmit amplifier.

AIN- is an inverting input of the transmit amplifier.

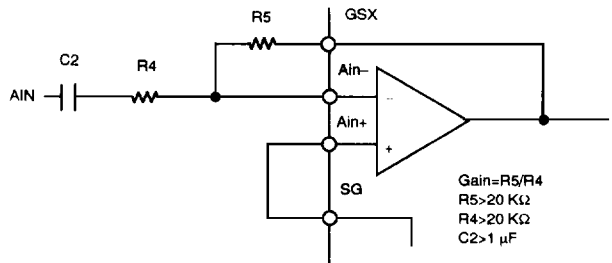
GSX is transmit amplifier output pin.

Gain adjustment should be referred to the following figure.



$$\text{Gain} = 1 + \frac{R2}{R3} \leq 10$$

$$\begin{aligned} R2 + R3 &> 50 \text{ K} \\ R1 &> 50 \text{ K} \\ C1 &> 0.47 \mu\text{F} \end{aligned}$$



$$\begin{aligned} \text{Gain} &= R5/R4 \\ R5 &> 20 \text{ K}\Omega \\ R4 &> 20 \text{ K}\Omega \\ C2 &> 1 \mu\text{F} \end{aligned}$$

AG

AG is the analog ground pin (0 V).

AG is separated from DG on the chip, but should be connected to DG on a printed board.

VFRO

VFRO is the receive filter output pin.

The maximum voltage swing is 2.4 V_{p-p} and the signal ground level is at around the potential of SG (on-chip signal ground VDD/2). Minimum load resistance is 20 kΩ

PWI, AOUT+, AOUT-

PWI is connected to the internal inverting input of the receive power amplifier.

AOUT- is the inverted output of the receive power amplifier.

AOUT+ is the inverted output of the another receive power amplifier.

Receive signal level can be adjusted by using PWI, AOUT- and VFRO refer to Block diagram.

VDD

VDD is the + 5 V power supply pin.

PCMIN

PCM signal input pin.

This signal is serial data and converted to the analog signal under control of RSYNC and BCLOCK.

The recommended PCM data is 64/96/128/192/256/288/384/512/768/1024/1536/1544/2048 kbps.

PCM serial data is shifted out at the falling edge of BCLOCK.

When total 8 bits data are shifted, all 8 bits data are latched to the internal control register.

MSD (the first bit) is indicated at the rising edge of RSING.

BCLOCK

BCLOCK is the shift clock input pin.

The clock frequency is same to the data transmission speed and is recommended to be 64/96/128/192/256/288/384/512/768/1024/1536/1544/2048 kHz.

When BCLOCK is continuously at digital "0" or "1" level both transmit and receive sections become the power save mode.

RSYNC

Receive synchronizing signal input pin.

This signal should be synchronous to BCLOCK and is used for taking in the required 8 bits data from the input serial PCM data stream.

At the same time this signal makes the whole receive operation timing to be synchronous.

XSYNC

Transmit synchronizing signal input pin. This signal should be synchronous to BCLOCK and is used for taking out the required 8 bits serial PCM data from PCMOUT. At the same time, this signal makes the whole transmit operation timing to be synchronous when XSYNC is continuously at digital "0" or "1" level, both transmit and receive sections become power save mode automatically.

Both RSYNC and XSYNC should be within 8 kHz ± 50 ppm.

DG

DG is the digital ground (0 V) pin.

DG is separated from AG on the chip, but should be connected to AG on a printed board.

TMC

This is a control input pin for operating mode selection, such as normal operating mode and analog loop back mode.

The operating mode are as follows.

TMC Input	Mode
< 0.8V	normal mode
> 2.2V	analog-loop back

PDN

Power down control signal input pin.

By putting PDN on digital "0" state, the whole transmit and receive sections enter to the power down mode.

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PCMOUT

PCM signal output pin.

This pin is open drain output.

PCM signal is output from this pin. PCM signal is output being synchronized to the rising edge of BCLOCK with MSD first.

This pin shows the high output impedance except the 8 bit PCM data duration, including the case of the power down mode and power save mode. The companding law and coding pattern conform to CCITT recommendation. In case of 7544 (A-law), the even bits are reversed except MSD.

SG

On-chip signal ground output pin.

The potential is about a half of the supply voltage (VDD/2) and its forcing/sinking capability is 300 μ A.

SGC

The bypass capacitor for the signal ground should be put between SGC and AG 0.1 μ F low inductance capacitor, such as multilayer ceramic component is recommended.

PCMIN/PCMOUT		
	7543	7544
	MSD ↓	MSD ↓
+ Full scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
+ 0	1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1
- 0	0 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1
- Fulls scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Condition	Rating	Unit
V _{DD}	Supply voltage	-	0 ~ 7	V
V _{AIN}	Analog input voltage	-	-0.3 ~ V _{DD} + 0.3	V
V _{DIN}	Digital input voltage	-	-0.3 ~ V _{DD} + 0.3	V
T _{OP}	Operating temperature	-	-30 ~ +85	°C
T _{sig}	Storage temperature	-	-55 ~ +150	°C

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{DD}	Supply voltage		+ 4.75	+ 5.0	+ 5.25	V
V _{AIN}	Analog input voltage	connect AIN - and GSX	-	-	2.4	V _{PP}
V _{IH}	Digital input high voltage	XSYNC, RSYNC, BCLOCK, PCMIN, PDN, TMC	+ 2.2	-	V _{DD}	V
V _{IL}	Digital input low voltage		0		+ 0.8	V
F _C	Bit clock frequency	BCLOCK	64, 128, 256, 288, 512, 1024, 2048, 96, 192, 384, 768, 1536, 1544			kHz
F _C	Sync pulse frequency	XSYNC, RSYNC	-	8.0	-	kHz
D _C	Clock duty cycle	BCLOCK	40	50	60	%
T _{IR}	Digital	Rise time XSYNC, RSYNC, BCLOCK, PCMIN, PDN, TMC	-	-	50	ns
T _{IF}	Input		Fall time	-	-	50
T _{XS}	Transmit sync timing	BCLOCK → XSYNC Ref Fig1	100	-	-	ns
T _{SX}		XSYNC → BCLOCK Ref Fig1	100	-	-	ns
T _{RS}	Receive sync timing	BCLOCK → RSYNC Ref Fig1	100	-	-	ns
T _{SR}		RSYNC → BCLOCK Ref Fig1	100	-	-	ns
T _{WS}	Sync pulse width	XSYNC, RSYNC Ref Fig1	1BCLK	-	100	µs
T _{DS}	PCMIN set-up time	Ref Fig1	100			ns
T _{DH}	PCMIN hold time	Ref Fig1	100			ns
R _{DL}	Digital output load	Pull up resistor	0.5	-	-	kΩ
C _{DL}			-	-	100	pF
V _{off}	Analog input allowable	Transmit gain : 0 dB	-100	-	+100	mV
	DC offset	Transmit gain : 20 dB	-10	-	+10	mV
	Allowable jitter	XSYNC, RSYNC	-	-	1000	ns

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DC Characteristics ($V_{DD} = +5\text{ V} \pm 5\%$, $T_A : -30 \sim 85^\circ\text{C}$)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD1}	Supply current	Operating mode	-	4.0	6.0	mA
I_{DD2}		Power down mode PDN = 1 XSYNC or BCLOCK off	-	0.9	1.5	mA
I_{DD3}		Power save mode PDN = 0	-	0.3	0.5	mA
V_{IH}	Input high voltage		2.2	-	V_{DD}	V
V_{IL}	Input low voltage		0.0	-	0.8	V
I_{IH}	Input leakage current	$V_I = V_{DD}$	-	-	2.0	μA
I_{IL}		$V_I = 0\text{V}$	-	-	0.5	μA
V_{OL}	Output low voltage	Pull-up : 0.5 K Ω	0.0	0.2	0.4	V
I_O	Output leakage current	PCMOUT	-	-	10	μA
C_{IN}	Input capacitance	All pins	-	5	-	pF

AC Characteristics ($V_{DD} = +5\text{ V} \pm 5\%$, $T_A : -30 \sim 85^\circ\text{C}$)

Symbol	Parameter	Freq (Hz)	Level (dBm0)	Condition	Min	Typ	Max	Unit
Loss T1	Transmit frequency response	60	0		20	26	-	dB
Loss T2		300			-0.20	0.07	0.20	
Loss T3		1 020			reference			
Loss T4		2 020			-0.15	-0.04	0.20	
Loss T5		3 000			-0.15	0.06	0.20	
Loss T6		3 400			0	0.40	0.80	
Loss R1	Receive frequency response	300	0		-0.15	-0.03	0.20	dB
Loss R2		1 020			reference			
Loss R3		2 020			-0.15	-0.02	0.20	
Loss R4		3 000			-0.15	0.15	0.20	
Loss R5		3 400			0.0	0.56	0.80	
SD T1	Transmit signal to distortion ratio	1 020	3	*1 (7543/7544)	35	43	-	dB
SD T2			0		35	41	-	
SD T3			-30		35	38	-	
SD T4			-40		29	31.5/31	-	
SD T5			-45		24	27.0/26	-	
SD R1	Receive signal to distortion ratio	1 020	3	*1 (7543/7544)	36	43	-	dB
SD R2			0		36	41	-	
SD R3			-30		36	40	-	
SD R4			-40		30	33.5/32	-	
SD R5			-45		25	30/27	-	

Note : *1 P-message filter.

Transmit Analog Interface ($V_{DD} = +5\text{ V} \pm 5\%$, $T_A : -30 \sim 85^\circ\text{C}$)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{INX}	Input resistance	AIN+, AIN-	10	-	-	M Ω
R_{LGX}	Output load resistance	GSX to SG	20	-	-	k Ω
C_{LGX}	Output load capacitance		-	-	100	pF
V_{OGX}	Output voltage		-1.2	-	1.2	V
V_{OSGX}	Offset voltage		Gain=1	-20	-	20

Receive Analog Interface ($V_{DD} = +5\text{ V} \pm 5\%$, $T_A : -30\text{ to }85^\circ\text{C}$)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{INPW}	Input resistance	PWI	10	-	-	M Ω
R_{LVF}	Output load resistance	VFRO to SG	20	-	-	k Ω
R_{LAO}		AOUT+, AOUT- to SG	600	-	-	Ω
C_{LVF}	Output load capacitance	VFRO	-	-	100	pF
C_{LAO}		AOUT+, AOUT-	-	-	50	pF
V_{OVF}	Output voltage	VFRO, RL=20K Ω to SG	-1.2	-	1.2	V
V_{OAO}		AOUT+, AOUT-, RL=0.6K Ω to SG	-1.3	-	1.3	V
V_{OSVF}	Offset voltage	VFRO to SG	-100	-	100	mV
V_{OSAO}		AOUT+, AOUT- Gain=1 to SG	-100	-	100	mV

AC Characteristics ($V_{DD} = +5\text{ V} \pm 5\%$, $T_A : -30\text{ to }85\text{ }^\circ\text{C}$)

Symbol	Parameter	Freq (Hz)	Level (dBm0)	Condition	Min	Typ	Max	Unit
GT T1	Transmit gain tracking	1 020	3		-0.2	0.01	0.2	dB
GT T2			-10		reference			
GT T3			-40		-0.2	0.0	0.2	
GT T4			-50		-0.4	-0.03	0.4	
GT T5			-55		-1.2	0.15	1.2	
GT R1	Receive gain tracking	1 020	3		-0.2	-0.06	0.2	dB
GT R2			-10		reference			
GT R3			-40		-0.2	-0.02	0.2	
GT R4			-50		-0.4	-0.02	-0.4	
GT R5			-55		-0.8	-0.27	-0.8	
Nidel T	Idle channel noise	-	-	A1N SG *2	-	-74.5/ -72.5	-70/-69	dBm0
Nidel R		-	-	*2 *3	-	-78	-75	p
AV T	Absolute level	1 020	0	VDD=5.0 V T=25 °C *4	0.580	0.6007	0.622	Vrms
AV R					0.580	06007	0.622	
AV Tt	Absolute level variation with temp. and supply	1 020	0	VDD=5 V ± 5% T=-30 ~ 85 °C *4	-0.2	-	0.2	dB
AV Rt					-0.2	-	0.2	
Td	Absolute delay	1 020	0	A to A BCLOCK=64kHz	-	-	0.60	ms
Tgd T1	Transmit group delay	500		*5	-	0.19	0.75	ms
Tgd T2		600			-	0.11	0.35	
Tgd T3		100	0		-	0.02	0.125	
Tgd T4		2 600			-	0.05	0.125	
Tgd T5		2 800			-	0.07	0.75	

Notes : *2 P-message filter

*3 PCM input data : code "0"

*4 AVR defined at VFRO

*5 The minimum value of the group delay distortion should be referred as 0 ms

AC Characteristics ($V_{DD} = +5V \pm 5\%$, $T_A : -30 \sim 85^\circ C$)

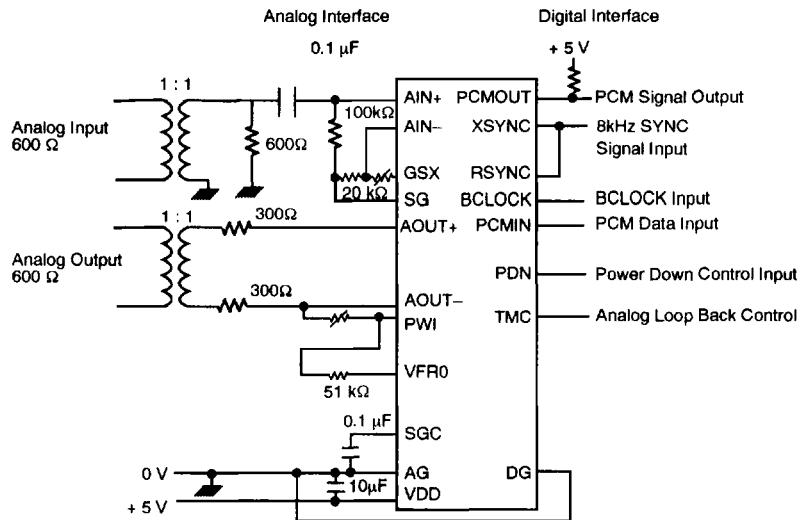
Symbol	Parameter	Freq (Hz)	Level (dBm0)	Condition	Min	Typ	Max	Unit
Tgd R1	Receive group delay	500	0	*6	-	0.00	0.75	ms
Tgd R2		600			-	0.00	0.35	
Tgd R3		1 000			-	0.00	0.125	
Tgd R4		2 600			-	0.09	0.125	
Tgd R5		2 800			-	0.12	0.75	
CR T	Crosstalk attenuation	1 020	0	TRANS → RECV	75	85	-	dB
CR R				RECV → TRANS	70	77	-	
DIS	Discrimination	4.6K ~ 72K	0	0 ~ 4000Hz	30	32	-	dB
S	Out-of-band spurious	300 ~ 3 400	0	4.6K ~ 100kHz	-	-37.5	-35	dBm0
IMD	Intermodulation distortion	$f_a=470$ $f_a=320$	-4	2 f_a - f_b	-	-52	-35	dBm0
	D to D mode gain	1 020	0	TMC=1 PCNIN to PCMOUT	-1.0		1.0	dB
PSR T	PSRR	0 ~ 50K	30 mVpp	Inband	-	30	-	dB
PSR R								
Tsd	Digital output delay time	CL=100pF + 1LSTTL			50		200	ns
Txd1					50		200	
Txd2					50		200	
Txd3					50		200	

Notes : *6 The minimum value of the group delay should be referred as 0ms.

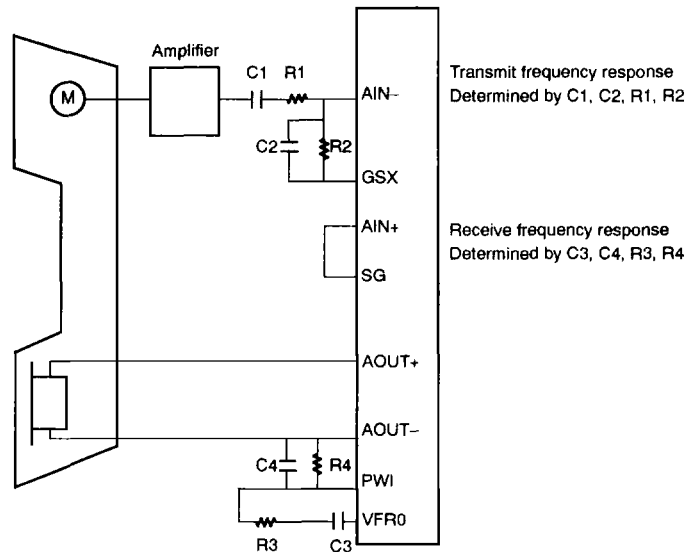


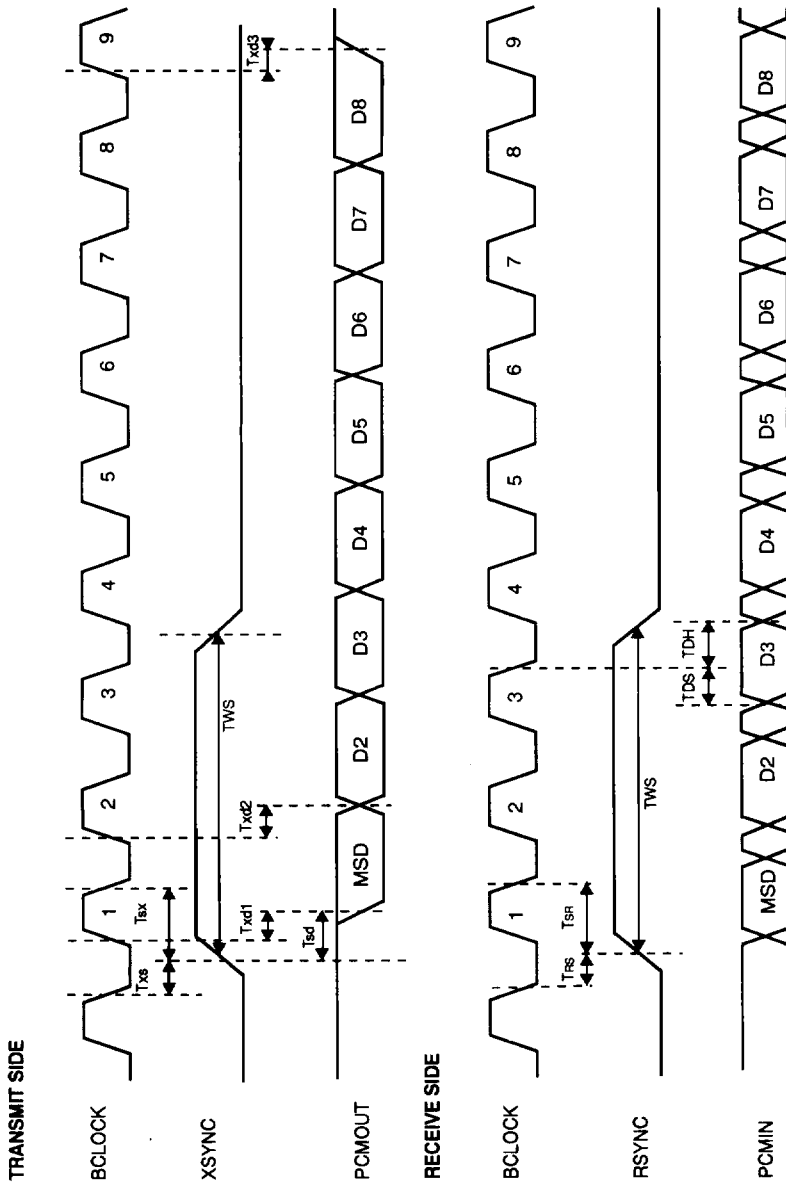
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Application



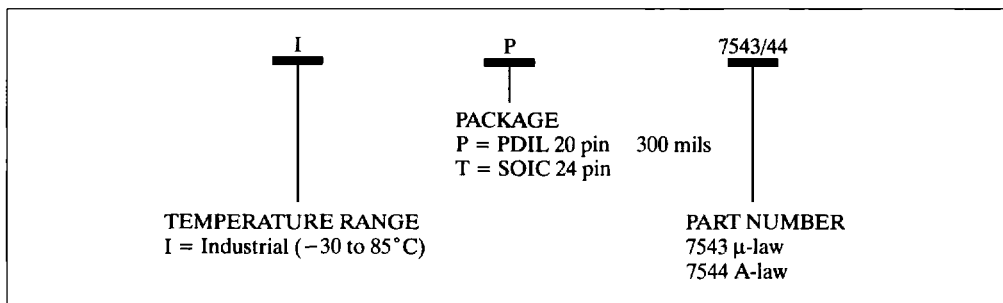
Frequency Response Adjustment





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