Signetics

54F164
Shift Register

8-Bit Serial-In Parallel-Out Shift Register

Product Specification

Military Logic Products

FEATURES

- **Gated serial data inputs**
- **Typical shift frequency of 90 MHz**
- **Asynchronous master reset**
- **Fully buffered Clock and Data inputs**
- **Fully synchronous data transfers**

DESCRIPTION

The 54F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (Dsa · Dsb); either input can be used as an active High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two data inputs (Dsa · Dsb) that existed one set-up time before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

ORDERING INFORMATION

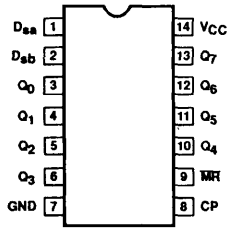
DESCRIPTION	ORDER CODE
Ceramic DIP	54F164/BCA
Ceramic Flat Pack	54F164/BDA
Ceramic LLCC	54F164/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{sa}, D_{sb}	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active Low)	1.0/1.0	20μA/0.6mA
Q_0 - Q_7	Outputs	50/33	1.0mA/20mA

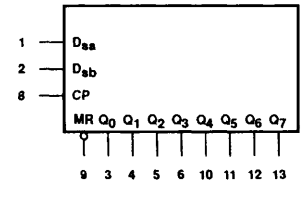
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

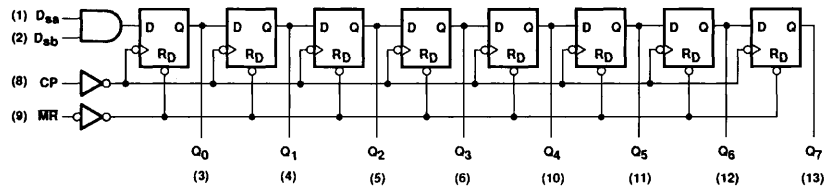
LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1	—	Q_7
Reset	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_6
	H	↑	l	h	L	q_0	—	q_6
	H	↑	h	l	L	q_0	—	q_6
	H	↑	h	h	H	q_0	—	q_6

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High Clock transition
q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High Clock transition
X = Don't care
↑ = Low-to-High Clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V		5	100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-60	-80	-150	mA
I_{CC}	Supply current (total)	V_{CC} = Max		33	50	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	80	90		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.5 5.0	6.0 7.5	8.0 11.0	4.5 5.0	10 13	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.5	10.5	13	5.5	14	ns

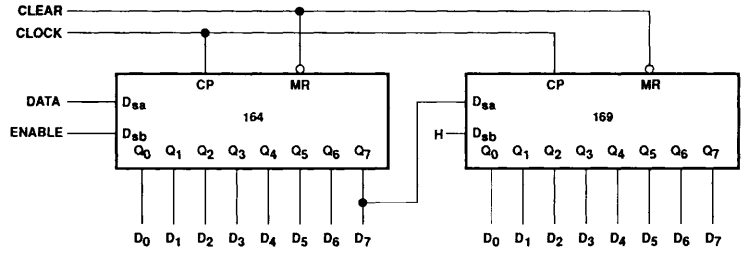
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time High or Low A or B to CP	Waveform 3	7.0 7.0			7.0 7.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low A or B to CP		1.0 1.0			1.0 1.0		ns ns
t_w(H) t_w(L)	CP pulse width, High or Low	Waveform 1	4.0 7.0			4.0 7.0		ns ns
t_w(L)	$\overline{MR}$ pulse width Low	Waveform 2	7.0			7.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			9.0		ns

NOTES:

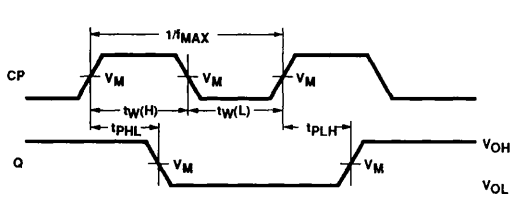
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type per the functional table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.
5. Parameter guaranteed, but not tested.

APPLICATION DIAGRAM

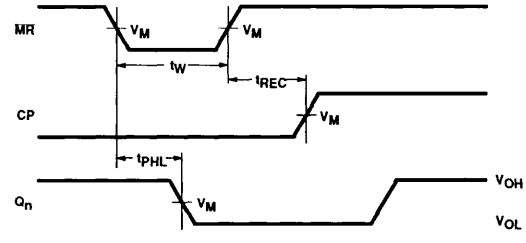


NOTE:
The 54F164 can be cascaded to form synchronous shift registers of longer length.
Here, two devices are combined to form a 16-bit shift register.

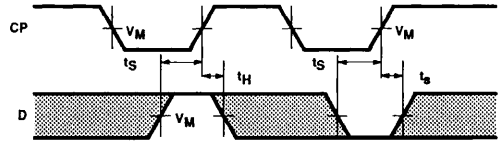
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



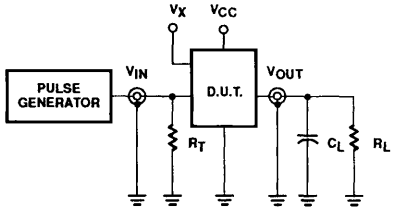
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



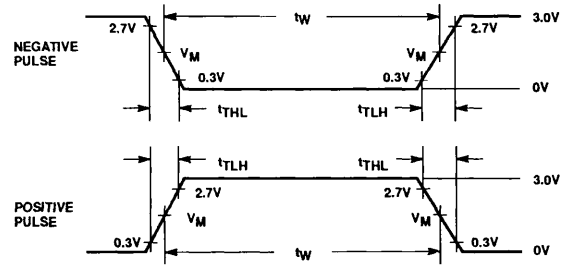
Waveform 3. Data Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns