# SN54ABTH18652A, SN54ABTH182652A, SN74ABTH18652A, SN74ABTH182652A
# SCAN TEST DEVICES WITH
# 18-BIT BUS TRANSCEIVERS AND REGISTERS

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs of 'ABTH182652A Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation

- One Boundary-Scan Cell Per I/O Architecture Improves Scan Efficiency
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel-Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54ABTH18652A, SN54ABTH182652A . . . HV PACKAGE
(TOP VIEW)
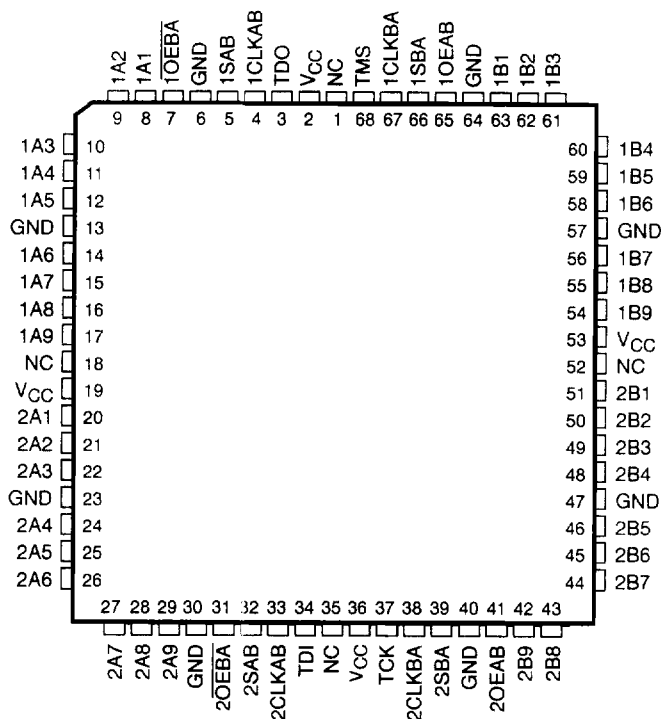


NC – No internal connection

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**SN74ABTH18652A, SN74ABTH182652A . . . PM PACKAGE**
**(TOP VIEW)**
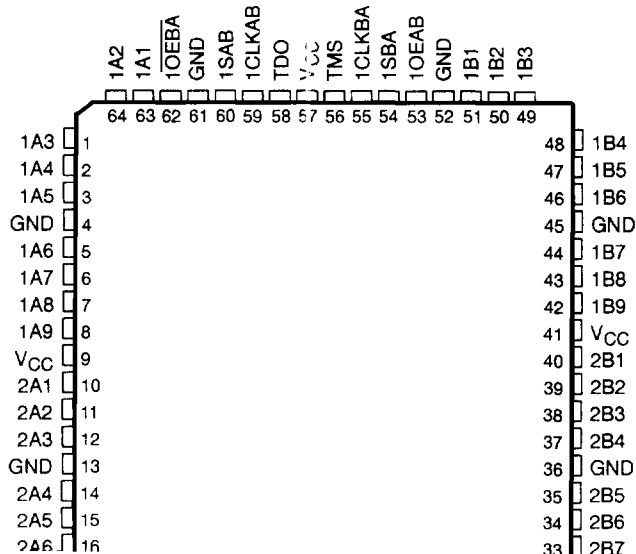


Top pins (left to right, 64–49): 1A2, 1A1, $\overline{1OEBA}$, GND, 1SAB, 1CLKAB, TDO, V$_{CC}$, TMS, 1CLKBA, 1SBA, 1OEAB, GND, 1B1, 1B2, 1B3

Left side (pins 1–16):
| Pin | Signal |
|---|---|
| 1 | 1A3 |
| 2 | 1A4 |
| 3 | 1A5 |
| 4 | GND |
| 5 | 1A6 |
| 6 | 1A7 |
| 7 | 1A8 |
| 8 | 1A9 |
| 9 | V$_{CC}$ |
| 10 | 2A1 |
| 11 | 2A2 |
| 12 | 2A3 |
| 13 | GND |
| 14 | 2A4 |
| 15 | 2A5 |
| 16 | 2A6 |

Right side (pins 48–33):
| Pin | Signal |
|---|---|
| 48 | 1B4 |
| 47 | 1B5 |
| 46 | 1B6 |
| 45 | GND |
| 44 | 1B7 |
| 43 | 1B8 |
| 42 | 1B9 |
| 41 | V$_{CC}$ |
| 40 | 2B1 |
| 39 | 2B2 |
| 38 | 2B3 |
| 37 | 2B4 |
| 36 | GND |
| 35 | 2B5 |
| 34 | 2B6 |
| 33 | 2B7 |

PRO

## description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

Improved scan efficiency is accomplished through the adoption of a one boundary-scan cell (BSC) per I/O pin architecture. This architecture is implemented in such a way as to capture test data of most interest. A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The B-port outputs of 'ABTH182652A, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54ABTH18652A and SN54ABTH182652A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH18652A and SN74ABTH182652A are characterized for operation from –40°C to 85°C.

### FUNCTION TABLE
(normal mode, each 9-bit section)

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| OEAB | OEBA | CLKAB | CLKBA | SAB | SBA | A1 THRU A9 | B1 THRU B9 | |
| L | H | L | L | X | X | Input disabled | Input disabled | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | L | X | X | Input | Unspecified† | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | L | ↑ | X | X | Unspecified† | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | X | X | H | Output | Input | Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | X | X | H | X | Input | Output | Stored A data to B bus |
| H | L | X | X | H | H | Output | Output | Stored A data to B bus and stored B data to A bus |

† The data output functions can be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
  Select control = H: clocks must be staggered in order to load both registers.

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| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|------|------|-------|-------|-----|-----|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|------|------|-------|-------|-----|-----|
| H | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|------|------|-------|-------|-----|-----|
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**

| OEAB | $\overline{OEBA}$ | CLKAB | CLKBA | SAB | SBA |
|------|------|-------|-------|-----|-----|
| H | L | X | X | H | H |

**TRANSFER STORED DATA**
**TO A AND/OR B**
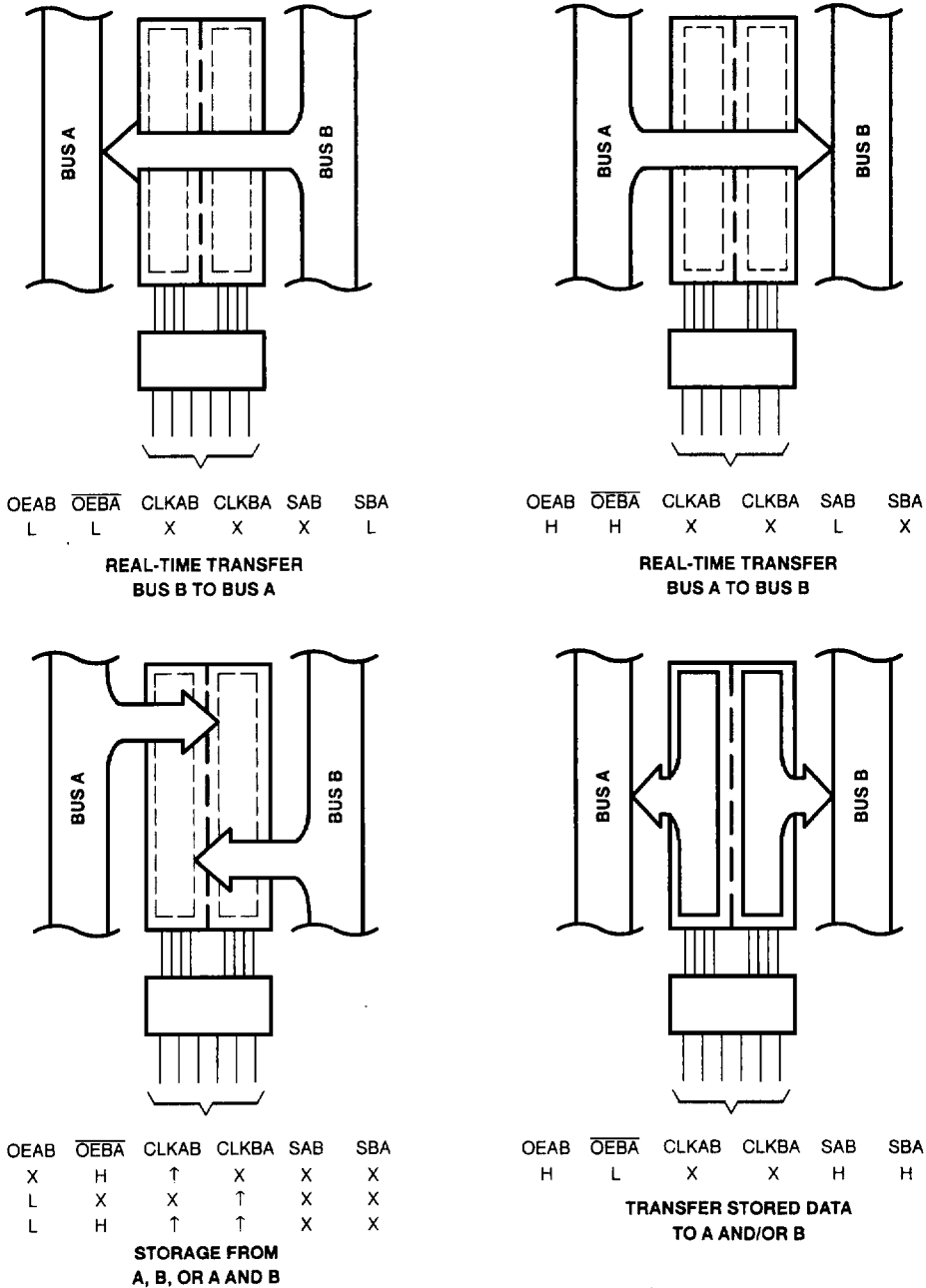
**Figure 1. Bus-Management Functions**

## functional block diagram
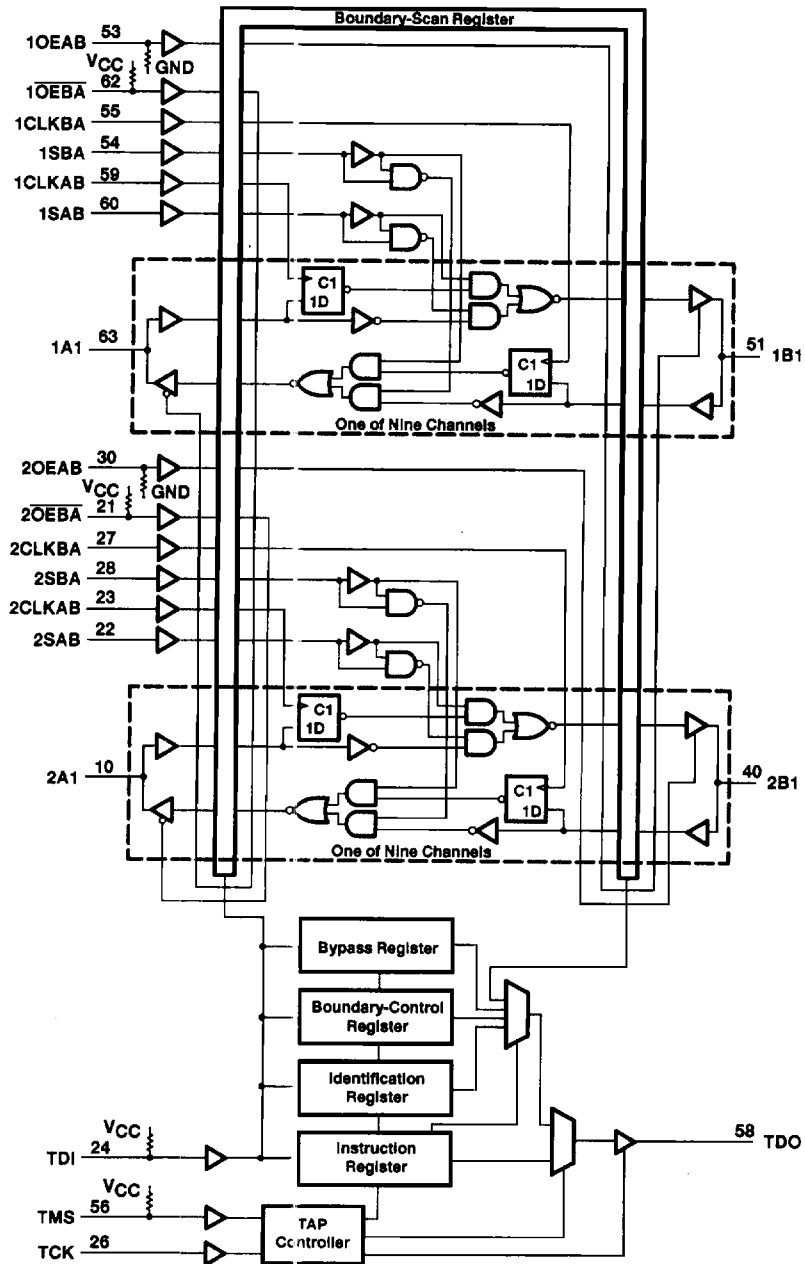


Pin numbers shown are for the PM package.

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## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| GND | Ground |
| 1OEAB, 2OEAB | Normal-function active-high output enables. See function table for normal-mode logic. An internal pulldown at each terminal forces the terminal to a high level if left unconnected. |
| 1OEBA, 2OEBA | Normal-function active-low output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| 1SAB, 1SBA, 2SAB, 2SBA | Normal-function select controls. See function table for normal-mode logic. |
| TCK | Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| V$_{CC}$ | Supply voltage |

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## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 2 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and four test-data registers: a 48-bit boundary-scan register, a 3-bit boundary-control register, a 1-bit bypass register, and a 32-bit device-identification register.
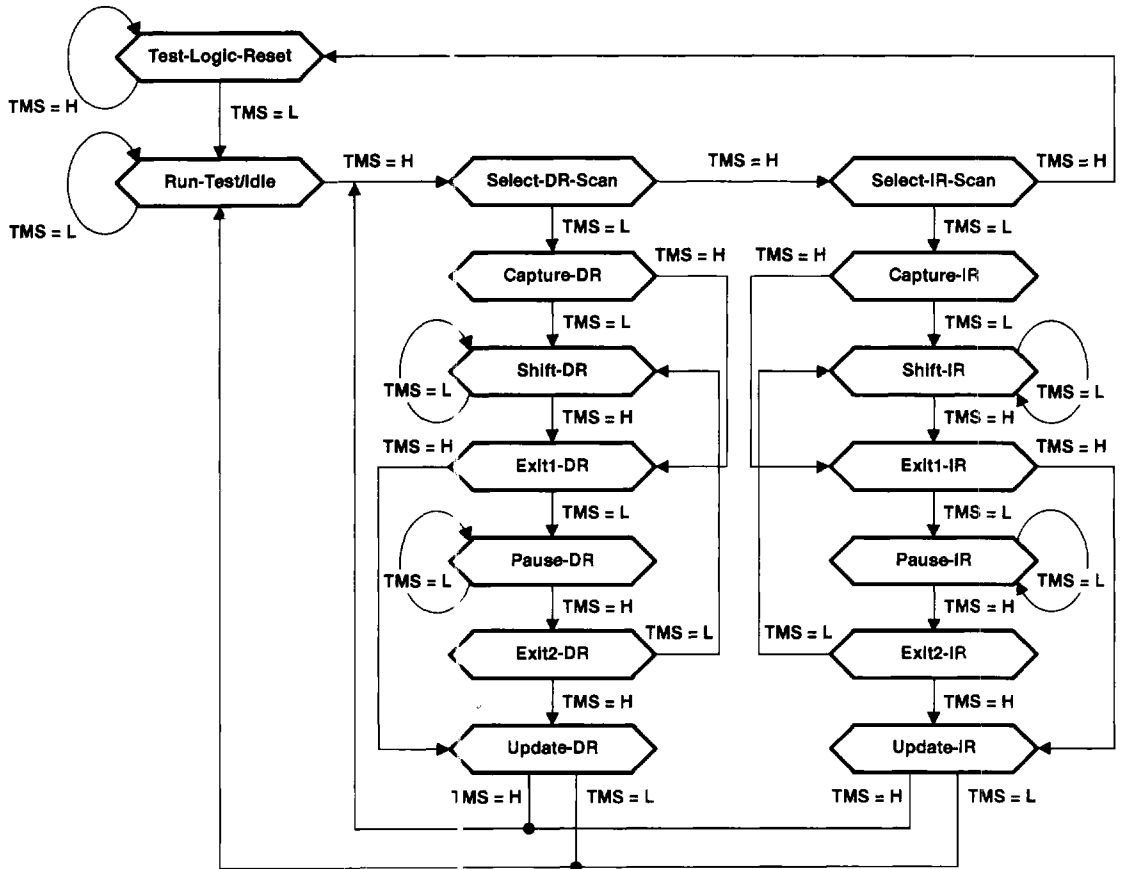


Figure 2. TAP-Controller State Diagram

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## state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated in Figure 2 and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABTH18652A and 'ABTH182652A, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–46 in the boundary-scan register are reset to logic 0 while bits 45–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other bits in the boundary-scan register should be considered indeterminate. The boundary-control register is reset to the binary value 010, which selects the PSA test operation.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

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### Shift-DR (continued)

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

### Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK following entry to the Update-DR state.

### Capture-IR

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state. For the 'ABTH18652A and 'ABTH182652A, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

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## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

## instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABTH18652A and 'ABTH182652A. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is illustrated in Figure 3.
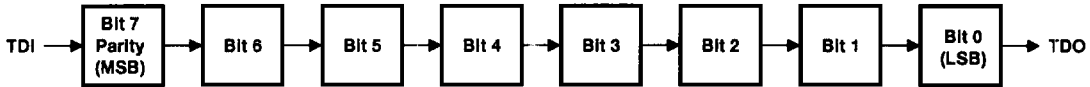


**Figure 3. Instruction Register Order of Scan**

## data register description

### boundary-scan-register

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–46 are reset to logic 0, while BSCs 45–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

### Table 1. Boundary-Scan-Register Configuration

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | 2OEAB | 35 | 2A9-I/O | 17 | 2B9-I/O |
| 46 | 1OEAB | 34 | 2A8-I/O | 16 | 2B8-I/O |
| 45 | 2$\overline{\text{OEBA}}$ | 33 | 2A7-I/O | 15 | 2B7-I/O |
| 44 | 1$\overline{\text{OEBA}}$ | 32 | 2A6-I/O | 14 | 2B6-I/O |
| 43 | 2CLKAB | 31 | 2A5-I/O | 13 | 2B5-I/O |
| 42 | 1CLKAB | 30 | 2A4-I/O | 12 | 2B4-I/O |
| 41 | 2CLKBA | 29 | 2A3-I/O | 11 | 2B3-I/O |
| 40 | 1CLKBA | 28 | 2A2-I/O | 10 | 2B2-I/O |
| 39 | 2SAB | 27 | 2A1-I/O | 9 | 2B1-I/O |
| 38 | 1SAB | 26 | 1A9-I/O | 8 | 1B9-I/O |
| 37 | 2SBA | 25 | 1A8-I/O | 7 | 1B8-I/O |
| 36 | 1SBA | 24 | 1A7-I/O | 6 | 1B7-I/O |
| — | — | 23 | 1A6-I/O | 5 | 1B6-I/O |
| — | — | 22 | 1A5-I/O | 4 | 1B5-I/O |
| — | — | 21 | 1A4-I/O | 3 | 1B4-I/O |
| — | — | 20 | 1A3-I/O | 2 | 1B3-I/O |
| — | — | 19 | 1A2-I/O | 1 | 1B2-I/O |
| — | — | 18 | 1A1-I/O | 0 | 1B1-I/O |

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### boundary-control register

The boundary-control register (BCR) is three bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 010, which selects the PSA test operation. The BCR order of scan is illustrated in Figure 4.
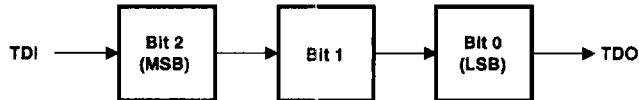


**Figure 4. Boundary-Control Register Order of Scan**

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is illustrated in Figure 5.
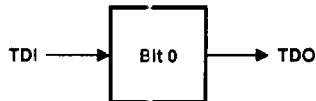


**Figure 5. Bypass Register Order of Scan**

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### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the 'ABTH18652A , the binary value 00000000000001010100000000101111 (0002A02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74ABTH18652A.

For the 'ABTH182652A , the binary value 00000000000001011100000000101111 (0002E02F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN54/74ABTH182652A.

The IDR order of scan is from TDI through bits 31 –0 to TDO. Table 2 shows the IDR bits and their significance.

#### Table 2. Device-Identification-Register Configuration

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10[†] |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09[†] |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08[†] |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07[†] |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06[†] |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05[†] |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04[†] |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03[†] |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02[†] |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01[†] |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00[†] |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1[†] |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

[†] Note that for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

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## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

### Table 3. Instruction-Register Opcodes

| BINARY CODE[†]<br>BIT 7 → BIT 0<br>MSB → LSB | SCOPE OPCODE | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000011 | BYPASS[‡] | Bypass scan | Bypass | Normal |
| 10000100 | BYPASS[‡] | Bypass scan | Bypass | Normal |
| 00000101 | BYPASS[‡] | Bypass scan | Bypass | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 10001000 | BYPASS[‡] | Bypass scan | Bypass | Normal |
| 00001001 | RUNT | Boundary run test | Bypass | Test |
| 00001010 | READBN | Boundary read | Boundary scan | Normal |
| 10001011 | READBT | Boundary read | Boundary scan | Test |
| 00001100 | CELLTST | Boundary self test | Boundary scan | Normal |
| 10001101 | TOPHIP | Boundary toggle outputs | Bypass | Test |
| 10001110 | SCANCN | Boundary-control register scan | Boundary control | Normal |
| 00001111 | SCANCT | Boundary-control register scan | Boundary control | Test |
| All others | BYPASS | Bypass scan | Bypass | Normal |

[†] Bit 7 is used to maintain even parity in the 8-bit instruction.
[‡] The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the 'ABTH18652A or 'ABTH182652A.

### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–44 of the BSR). When a given output enable is active (logic 0 for $\overline{OEBA}$, logic 1 for OEAB), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Standard 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

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### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

### control boundary to high impedance

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

### control boundary to I/0

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

### boundary-run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

### boundary read

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

### boundary self test

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

### boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK in Run-Test/Idle. Data in the input-mode BSCs remains constant. Data appearing at the device input or I/O pins is not captured in the input-mode BSCs. The device operates in the test mode.

### boundary-control-register scan

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

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## boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

### Table 4. Boundary-Control-Register Opcodes

| BINARY CODE BIT 2 → BIT 0 MSB → LSB | DESCRIPTION |
|---|---|
| X00 | Sample inputs/toggle outputs (TOPSIP) |
| X01 | Pseudo-random pattern generation/36-bit mode (PRPG) |
| X10 | Parallel-signature analysis/36-bit mode (PSA) |
| 011 | Simultaneous PSA and PRPG/18-bit mode (PSA/PRPG) |
| 111 | Simultaneous PSA and binary count up/18-bit mode (PSA/COUNT) |

While the control input BSCs (bits 47–36) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 47–44 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are valid only when both bytes of the device are operating in one direction of data flow (that is, 1OEAB = 1$\overline{\text{OEBA}}$ and 2OEAB = 2$\overline{\text{OEBA}}$) and in the same direction of data flow (that is, 1OEAB = 2OEAB and 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$). Otherwise, the bypass instruction is operated.

## sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input-mode I/O pins is captured in the shift-register elements of the associated BSCs on each rising edge of TCK. Data in the shift-register elements of the selected output-mode BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK.

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### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output-mode I/O pins on each falling edge of TCK. Figures 6 and 7 illustrate the 36-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.
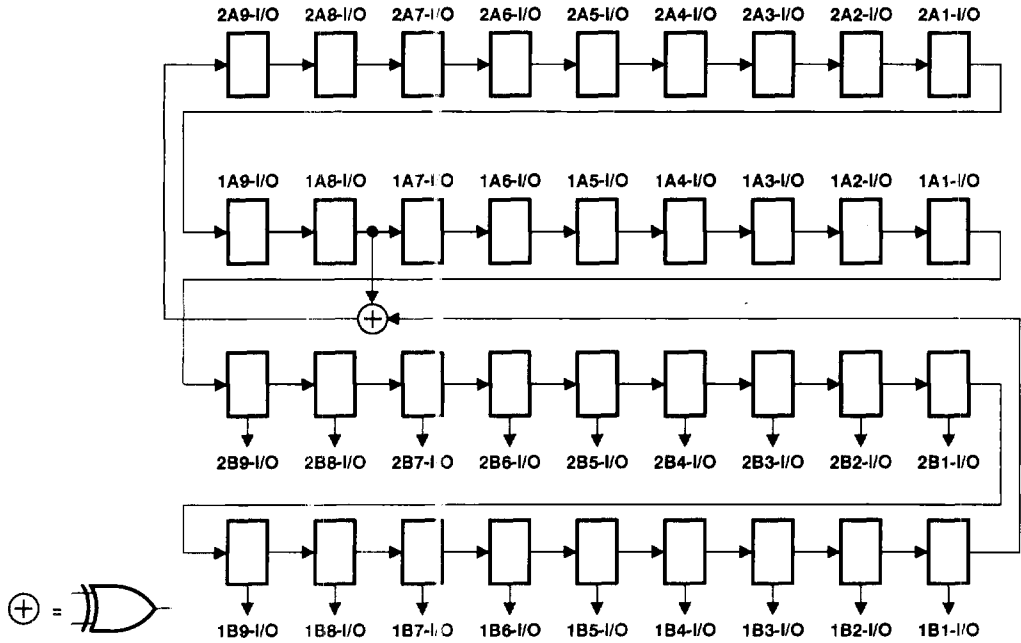


Figure 6. 36-Bit PRPG Configuration (1OEAB = 2OEAB = 1, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 1)

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Figure 7. 36-Bit PRPG Configuration (1OEAB = 2OEAB = 0, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 0)

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### parallel-signature analysis (PSA)

Data appearing at the selected device input-mode I/O pins is compressed into a 36-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. Data in the shadow latches of the selected output-mode BSCs remains constant and is applied to the associated device I/O pins. Figures 8 and 9 illustrate the 36-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.
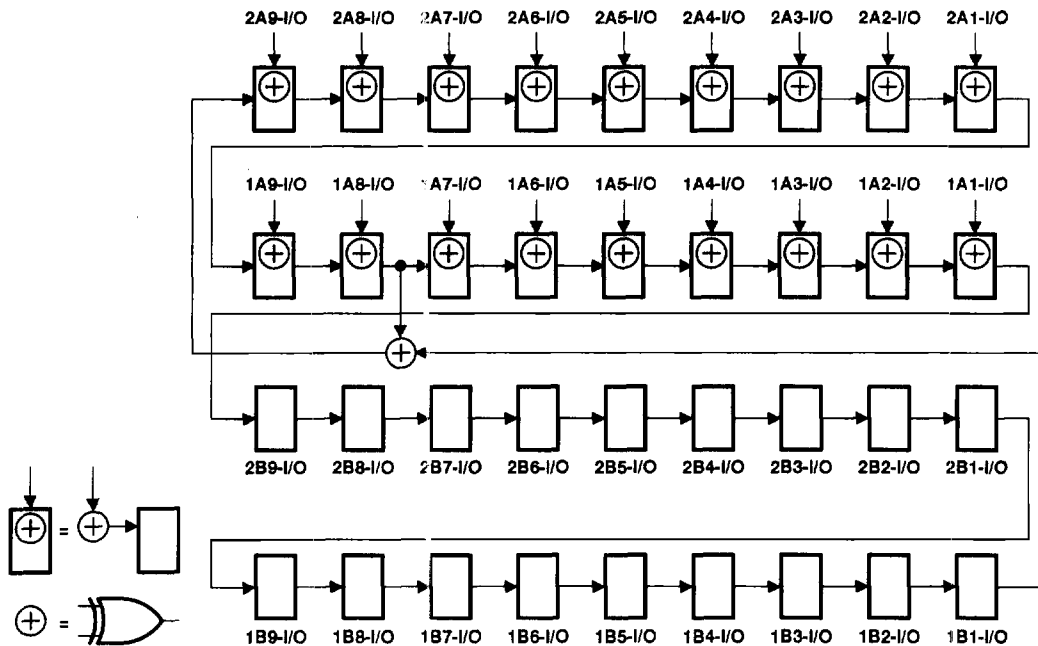


Figure 8. 36-Bit PSA Configuration (1OEAB = 2OEAB = 1, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 1)

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# SN54ABTH18652A, SN54ABTH182652A, SN74ABTH18652A, SN74ABTH182652A
# SCAN TEST DEVICES WITH
# 18-BIT BUS TRANSCEIVERS AND REGISTERS

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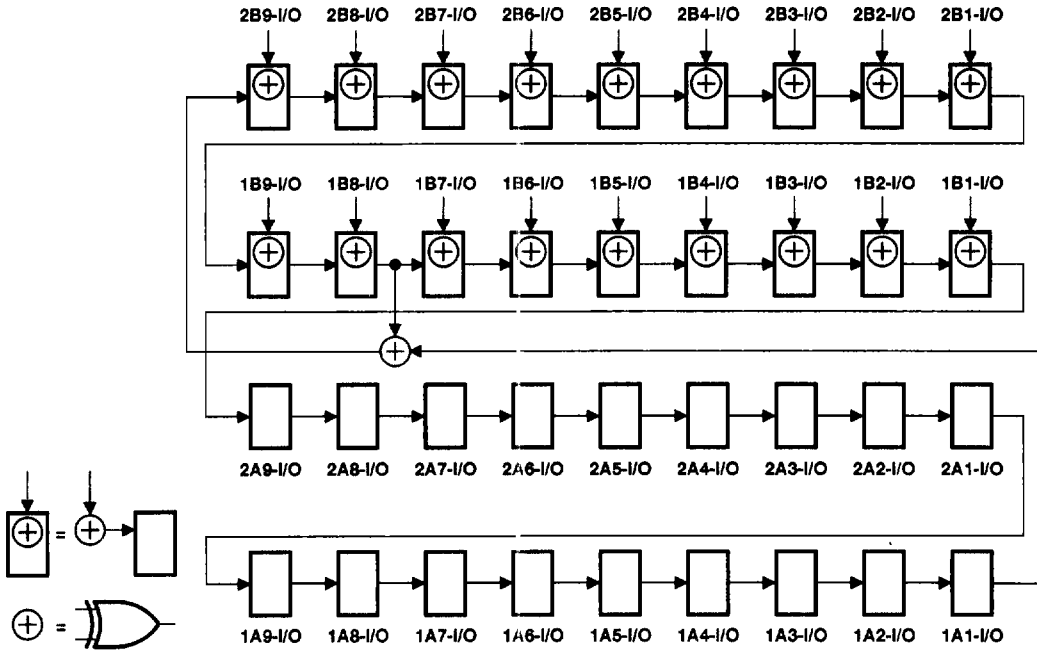
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Figure 9. 36-Bit PSA Configuration (1OEAB = 2OEAB = 0, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 0)

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### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit pseudo-random pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 10 and 11 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.
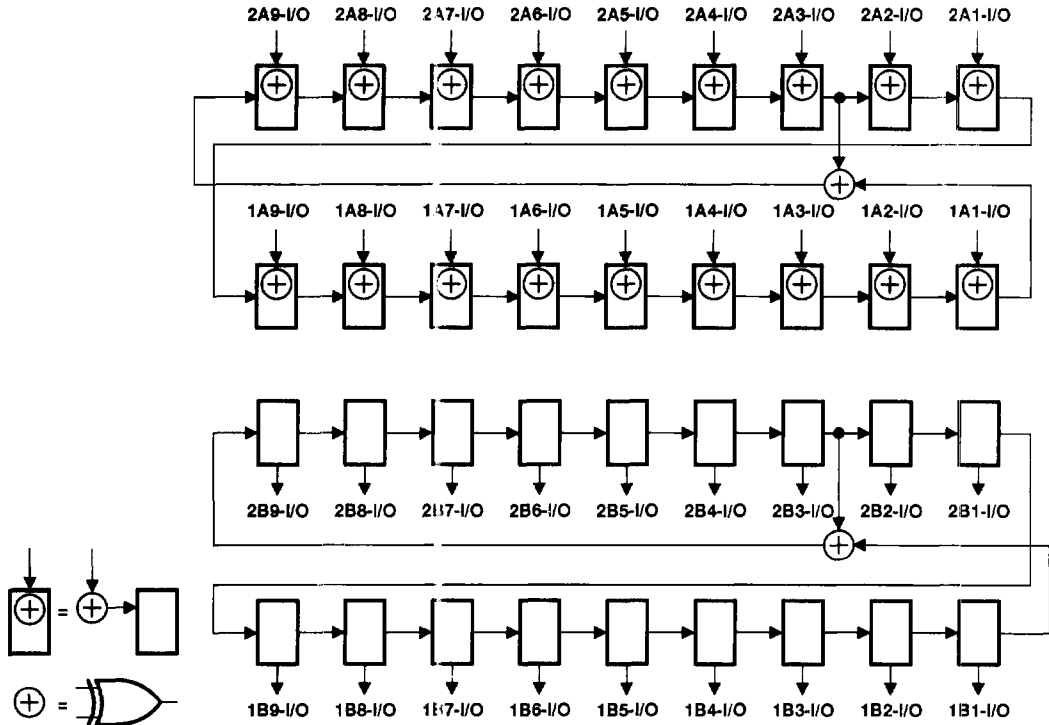


Figure 10. 18-Bit PSA/PRPG Configuration (1OEAB = 2OEAB = 1, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 1)

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Figure 11. 18-Bit PSA/PRPG Configuration (1OEAB = 2OEAB = 0, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 0)

### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input-mode I/O pins is compressed into an 18-bit parallel signature in the shift-register elements of the selected input-mode BSCs on each rising edge of TCK. At the same time, an 18-bit binary count-up pattern is generated in the shift-register elements of the selected output-mode BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device I/O pins on each falling edge of TCK. Figures 12 and 13 illustrate the 18-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.
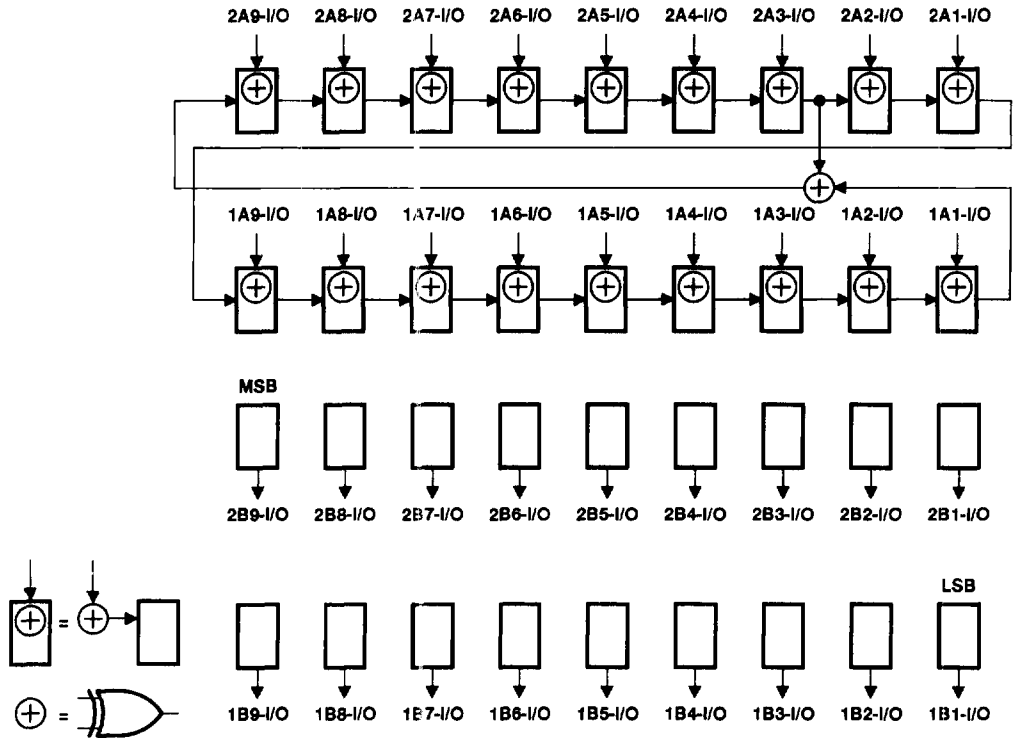


Figure 12. 18-Bit PSA/COUNT Configuration (1OEAB = 2OEAB = 1, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 1)

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Figure 13. 18-Bit PSA/COUNT Configuration (1OEAB = 2OEAB = 0, 1$\overline{\text{OEBA}}$ = 2$\overline{\text{OEBA}}$ = 0)

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## timing description

All test operations of the 'ABTH18652A and 'ABTH182652A are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in Figure 2) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 14. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

**Table 5. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation complete. |

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# SN54ABTH18652A, SN54ABTH182652A, SN74ABTH18652A, SN74ABTH182652A
# SCAN TEST DEVICES WITH
# 18-BIT BUS TRANSCEIVERS AND REGISTERS
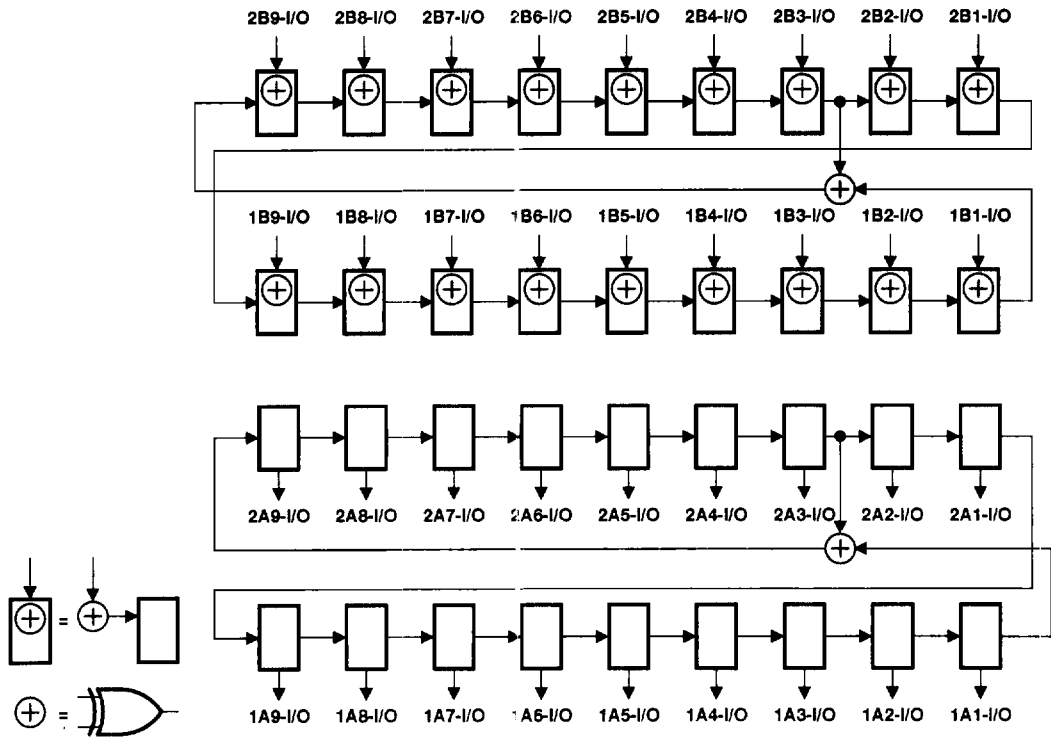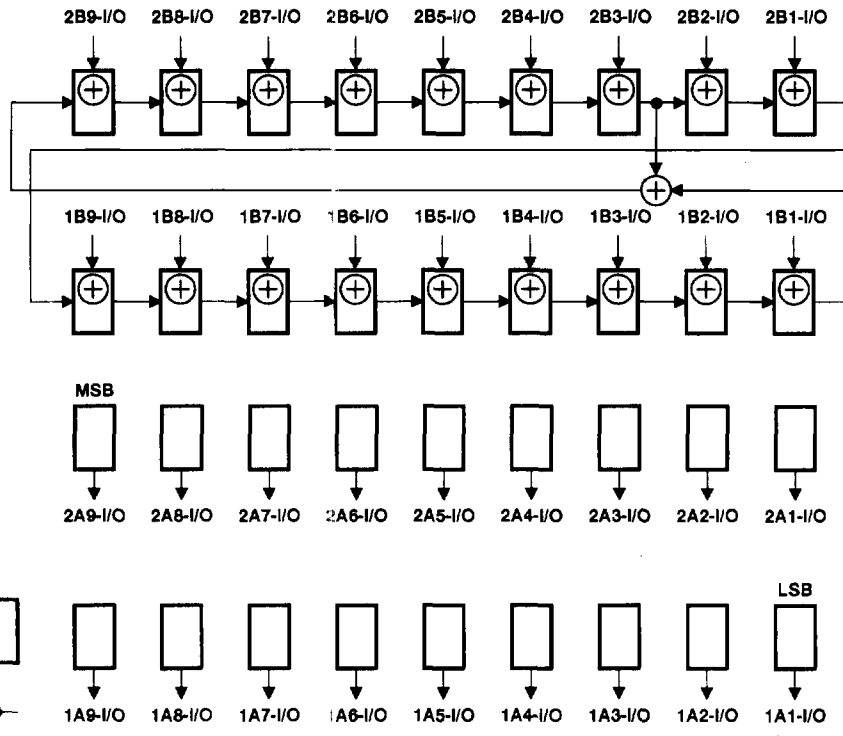
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3-State (TDO) or Don't Care (TDI)
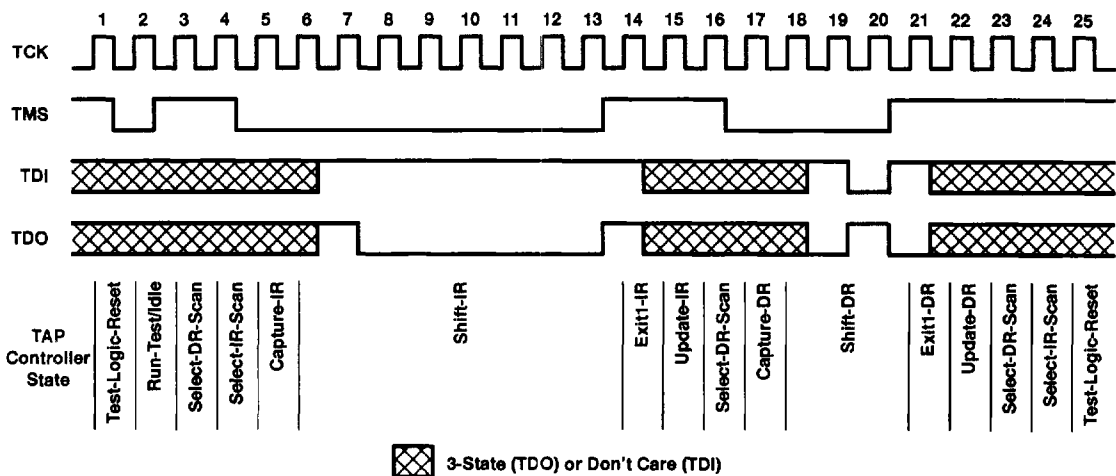
**Figure 14. Timing Example**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ........................................ −0.5 V to 7 V
Input voltage range, $V_I$: except I/O ports (see Note 1) .............................. −0.5 V to 7 V
               I/O ports (see Note 1) .................................... −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, $V_O$ ............. −0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABTH18652A ............................... 96 mA
                                     SN54ABTH182652A (A port or TDO) .................. 96 mA
                                     SN54ABTH182652A (B port) ........................ 30 mA
                                     SN74ABTH18652A ............................. 128 mA
                                     SN74ABTH182652A (A port or TDO) ................ 128 mA
                                     SN74ABTH182652A (B port) ........................ 30 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) ...................................................... −18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) .................................................... −50 mA
Maximum package power dissipation at $T_A = 55°C$ (in still air) (see Note 2) .................... 885 mW
Storage temperature range ...................................................... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
       2. For the SN74ABTH18652A and SN74ABTH182652A (PM package), the power derating factor for ambient temperatures greater than 55°C is −10.5 mW/°C.

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## recommended operating conditions

| | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | −24 | | −32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | −55 | 125 | −40 | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

| PARAMETER | | TEST CONDITIONS | | $T_A = 25°C$ | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC} = 4.5$ V, | $I_I = -18$ mA | | | −1.2 | | −1.2 | | −1.2 | V |
| $V_{OH}$ | | $V_{CC} = 4.5$ V, | $I_{OH} = -3$ mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC} = 5$ V, | $I_{OH} = -3$ mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC} = 4.5$ V, | $I_{OH} = -24$ mA | 2 | | | 2 | | | | |
| | | $V_{CC} = 4.5$ V, | $I_{OH} = -32$ mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC} = 4.5$ V | $I_{OL} = 48$ mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL} = 64$ mA | | | 0.55* | | | | 0.55 | |
| $I_I$ | CLK, S, TCK | $V_{CC} = 0$ to 5.5 V, $V_I = V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | μA |
| | A or B ports | $V_{CC} = 5.5$ V, $V_I = V_{CC}$ or GND | | | | ±20 | | ±20 | | ±20 | |
| $I_{IH}$ | OEAB | | | | | 150 | | 150 | | 150 | μA |
| | $\overline{OEBA}$, TDI, TMS | $V_{CC} = 5.5$ V, $V_I = V_{CC}$ | | | | 10 | | 10 | | 10 | |
| $I_{IL}$ | OEAB | | | | | −10 | | −10 | | −10 | μA |
| | $\overline{OEBA}$, TDI, TMS | $V_{CC} = 5.5$ V, $V_I = $ GND | | | | −150 | | −150 | | −150 | |
| $I_{I(hold)}$ | A or B ports | $V_{CC} = 4.5$ V | $V_I = 0.8$ V | 75 | 220 | 500 | | | 75 | 500 | μA |
| | | | $V_I = 2$ V | −75 | −180 | −500 | | | −75 | −500 | |
| $I_{OZH}$‡ | | $V_{CC} = 2.1$ V to 5.5 V, $V_O = 2.7$ V, OE = 0.8 V, $\overline{OE} = 2$ V | | | | 10 | | 10 | | 10 | μA |
| $I_{OZL}$‡ | | $V_{CC} = 2.1$ V to 5.5 V, $V_O = 0.5$ V, OE = 0.8 V, $\overline{OE} = 2$ V | | | | −10 | | −10 | | −10 | μA |
| $I_{OZPU}$ | | $V_{CC} = 0$ to 2.1 V, $V_O = 2.7$ V or 0.5 V, OE = 2 V, $\overline{OE} = 0.8$ V | | | | ±50 | | | | ±50 | μA |

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.
NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued) (see Note 3)**

| PARAMETER | | TEST CONDITIONS | $T_A = 25°C$ | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $I_{OZPD}$ | | $V_{CC}$ = 2.1 V to 0, $V_O$ = 2.7 V or 0.5 V, OE = 2 V, $\overline{OE}$ = 0.8 V | | | ±50 | | | | ±50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, $V_I$ or $V_O \le 4.5$ V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, $V_O$ = 5.5 V | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, $V_O$ = 2.5 V | –50 | –110 | –200 | –50 | –200 | –50 | –200 | mA |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | 1.6 | 2.2 | | 2.2 | | 2.2 | mA |
| | Outputs low | | A or B ports | | 19 | 24 | | 24 | | 24 | |
| | Outputs disabled | | | 0.9 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | 5 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O$ = 2.5 V or 0.5 V | | 8 | | | | | | pF |

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 15)**

| | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | 4 | | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | 4.5 | | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | 0.5 | | ns |

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 15)**

| | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | 8 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, OEAB, $\overline{OEBA}$, or S before TCK↑ | | | 6 | | ns |
| | | TDI before TCK↑ | | | 4.5 | | |
| | | TMS before TCK↑ | | | 3 | | |
| $t_h$ | Hold time | A, B, CLK, OEAB, $\overline{OEBA}$, or S after TCK↑ | | | 1.5 | | ns |
| | | TDI after TCK↑ | | | 1 | | |
| | | TMS after TCK↑ | | | 1.5 | | |
| $t_d$ | Delay time | Power up to TCK↑ | | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | 1 | | µs |

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5$ V, $T_A = 25°C$ | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | | | | | | 2 | 5.4 | ns |
| $t_{PHL}$ | | | | | | | | 2 | 6.6 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | | | | | | 2.5 | 8 | ns |
| $t_{PHL}$ | | | | | | | | 2.5 | 7.4 | |
| $t_{PLH}$ | SAB or SBA | B or A | | | | | | 2 | 7.5 | ns |
| $t_{PHL}$ | | | | | | | | 2 | 8 | |
| $t_{PZH}$ | OEAB or $\overline{OEBA}$ | B or A | | | | | | 2 | 8.6 | ns |
| $t_{PZL}$ | | | | | | | | 2.5 | 9.3 | |
| $t_{PHZ}$ | OEAB or $\overline{OEBA}$ | B or A | | | | | | 3 | 10.5 | ns |
| $t_{PLZ}$ | | | | | | | | 1.5 | 8.5 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5$ V, $T_A = 25°C$ | | | SN54ABTH18652A | | SN74ABTH18652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | | | | | | 2.5 | 12.4 | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | | 2 | 5.6 | ns |
| $t_{PHL}$ | | | | | | | | 2 | 5.6 | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | | 4 | 13.4 | ns |
| $t_{PZL}$ | | | | | | | | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | | 2 | 6.6 | ns |
| $t_{PZL}$ | | | | | | | | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | | 4 | 15 | ns |
| $t_{PLZ}$ | | | | | | | | 3 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | | 3 | 7.2 | ns |
| $t_{PLZ}$ | | | | | | | | 2.5 | 6.3 | |

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

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### recommended operating conditions

| | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | A port TDO | | −24 | | −32 | mA |
| | | B port | | −12 | | −12 | |
| $I_{OL}$ | Low-level output current | A port TDO | | 48 | | 64 | mA |
| | | B port | | 12 | | 12 | |
| $\Delta t / \Delta v$ | Input transition rise or fall rate | | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)**

| PARAMETER | | TEST CONDITIONS | | $T_A = 25°C$ | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC} = 4.5$ V, $I_I = -18$ mA | | | | -1.2 | | -1.2 | | -1.2 | V |
| $V_{OH}$ | A port, TDO | $V_{CC} = 4.5$ V, $I_{OH} = -3$ mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC} = 5$ V, $I_{OH} = -3$ mA | | 3 | | | 3 | | 3 | | |
| | | $V_{CC} = 4.5$ V | $I_{OH} = -24$ mA | 2 | | | 2 | | | | |
| | | | $I_{OH} = -32$ mA | 2* | | | | | 2 | | |
| | B port | $V_{CC} = 4.5$ V, $I_{OH} = -1$ mA | | 3.35 | | | 3.3 | | 3.35 | | |
| | | $V_{CC} = 5$ V, $I_{OH} = -1$ mA | | 3.85 | | | 3.8 | | 3.85 | | |
| | | $V_{CC} = 4.5$ V | $I_{OH} = -3$ mA | 3.1 | | | 3 | | 3.1 | | |
| | | | $I_{OH} = -12$ mA | 2.6* | | | | | 2.6 | | |
| $V_{OL}$ | A port, TDO | $V_{CC} = 4.5$ V | $I_{OL} = 48$ mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL} = 64$ mA | | | 0.55* | | | | 0.55 | |
| | B port | $V_{CC} = 4.5$ V | $I_{OL} = 8$ mA | | | 0.8 | | 0.8 | | 0.65 | |
| | | | $I_{OL} = 12$ mA | | | 0.8* | | | | 0.8 | |
| $I_I$ | CLK, S, TCK | $V_{CC} = 0$ to 5.5 V, $V_I = V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | $V_{CC} = 5.5$ V, $V_I = V_{CC}$ or GND | | | | ±20 | | ±20 | | ±20 | |
| $I_{IH}$ | OEAB | $V_{CC} = 5.5$ V, $V_I = V_{CC}$ | | | | 150 | | 150 | | 150 | µA |
| | $\overline{OEBA}$, TDI, TMS | | | | | 10 | | 10 | | 10 | |
| $I_{IL}$ | OEAB | $V_{CC} = 5.5$ V, $V_I = $ GND | | | | -10 | | -10 | | -10 | µA |
| | $\overline{OEBA}$, TDI, TMS | | | | | -150 | | -150 | | -150 | |
| $I_{I(hold)}$ | A or B ports | $V_{CC} = 4.5$ V | $V_I = 0.8$ V | 75 | 220 | 500 | | | 75 | 500 | µA |
| | | | $V_I = 2$ V | -75 | -180 | -500 | | | -75 | -500 | |
| $I_{OZH}$‡ | | $V_{CC} = 2.1$ V to 5.5 V, $V_O = 2.7$ V, OE = 0.8 V, $\overline{OE} = 2$ V | | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$‡ | | $V_{CC} = 2.1$ V to 5.5 V, $V_O = 0.5$ V, OE = 0.8 V, $\overline{OE} = 2$ V | | | | -10 | | -10 | | -10 | µA |
| $I_{OZPU}$ | | $V_{CC} = 0$ to 2.1 V, $V_O = 2.7$ V or 0.5 V, OE = 2 V, $\overline{OE} = 0.8$ V | | | | ±50 | | | | ±50 | µA |
| $I_{OZPD}$ | | $V_{CC} = 2.1$ V to 0, $V_O = 2.7$ V or 0.5 V, OE = 2 V, $\overline{OE} = 0.8$ V | | | | ±50 | | | | ±50 | µA |
| $I_{off}$ | | $V_{CC} = 0$, $V_I$ or $V_O ≤ 4.5$ V | | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC} = 5.5$ V, $V_O = 5.5$ V | | | | 50 | | 50 | | 50 | µA |
| $I_{OS}$§ | A port, TDO | $V_{CC} = 5.5$ V, $V_O = 2.5$ V | | -50 | -110 | -200 | -50 | -200 | -50 | -200 | mA |
| | B port | $V_{CC} = 5.5$ V, $V_O = 2.5$ V | | -25 | -55 | -100 | -25 | -100 | -25 | -100 | |

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

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**PRODUCT PREVIEW**

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued) (see Note 3)

| PARAMETER | | TEST CONDITIONS | | $T_A = 25°C$ | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $I_{CC}$ | Outputs high | $V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND | A or B ports | | 1.6 | 2.2 | | 2.2 | | 2.2 | mA |
| | Outputs low | | | | 21 | 27 | | 27 | | 27 | |
| | Outputs disabled | | | | 0.9 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$‡ | | $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I = 2.5$ V or 0.5 V | | | 5 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O = 2.5$ V or 0.5 V | | | 10 | | | | | | pF |
| $C_o$ | TDO | $V_O = 2.5$ V or 0.5 V | | | 8 | | | | | | pF |

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 15)

| | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | | | 4 | ns |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | | | 4.5 | ns |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | | | 0.5 | ns |

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 15)

| | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | 0 | 50 | 0 | 50 | MHz |
| $t_w$ | Pulse duration | TCK high or low | | | | 8 | ns |
| $t_{su}$ | Setup time | A, B, CLK, OEAB, $\overline{OEBA}$, or B before TCK↑ | | | | 6 | ns |
| | | TDI before TCK↑ | | | | 4.5 | |
| | | TMS before TCK↑ | | | | 3 | |
| $t_h$ | Hold time | A, B, CLK, OEAB, $\overline{OEBA}$, or B after TCK↑ | | | | 1.5 | ns |
| | | TDI after TCK↑ | | | | 1 | |
| | | TMS after TCK↑ | | | | 1.5 | |
| $t_d$ | Delay time | Power up to TCK↑ | | | | 50 | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | | | | 1 | µs |

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | 130 | | 100 | | 100 | | MHz |
| $t_{PLH}$ | A or B | B or A | | | | | | 2 | 6.4 | ns |
| $t_{PHL}$ | | | | | | | | 2 | 7.6 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | | | | | | 2.5 | 9 | ns |
| $t_{PHL}$ | | | | | | | | 2.5 | 8.4 | |
| $t_{PLH}$ | SAB or SBA | B or A | | | | | | 2 | 8.5 | ns |
| $t_{PHL}$ | | | | | | | | 2 | 9 | |
| $t_{PZH}$ | OEAB or $\overline{OEBA}$ | B or A | | | | | | 2 | 9.6 | ns |
| $t_{PZL}$ | | | | | | | | 2.5 | 10.3 | |
| $t_{PHZ}$ | OEAB or $\overline{OEBA}$ | B or A | | | | | | 3 | 10.5 | ns |
| $t_{PLZ}$ | | | | | | | | 1.5 | 8.5 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 15)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABTH182652A | | SN74ABTH182652A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | 90 | | 50 | | 50 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | | | | | | 2.5 | 13.1 | ns |
| $t_{PHL}$ | | | | | | | | 2.5 | 13.4 | |
| $t_{PLH}$ | TCK↓ | TDO | | | | | | 2 | 5.6 | ns |
| $t_{PHL}$ | | | | | | | | 2 | 5.6 | |
| $t_{PZH}$ | TCK↓ | A or B | | | | | | 4 | 14.4 | ns |
| $t_{PZL}$ | | | | | | | | 4 | 13.6 | |
| $t_{PZH}$ | TCK↓ | TDO | | | | | | 2 | 6.6 | ns |
| $t_{PZL}$ | | | | | | | | 2 | 6.9 | |
| $t_{PHZ}$ | TCK↓ | A or B | | | | | | 4 | 15 | ns |
| $t_{PLZ}$ | | | | | | | | 3 | 15 | |
| $t_{PHZ}$ | TCK↓ | TDO | | | | | | 3 | 7.2 | ns |
| $t_{PLZ}$ | | | | | | | | 2.5 | 6.3 | |

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.
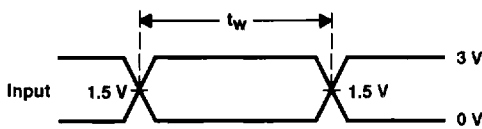
**PRODUCT PREVIEW**

![Texas Instruments logo] **TEXAS INSTRUMENTS**
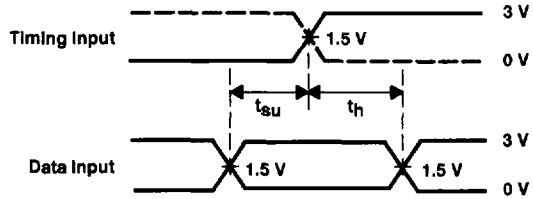
PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION
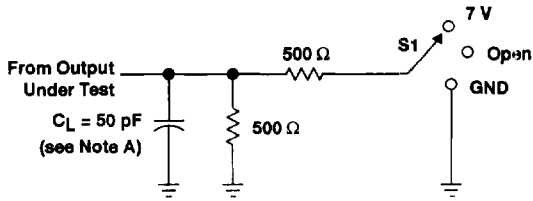


**LOAD CIRCUIT FOR OUTPUTS**

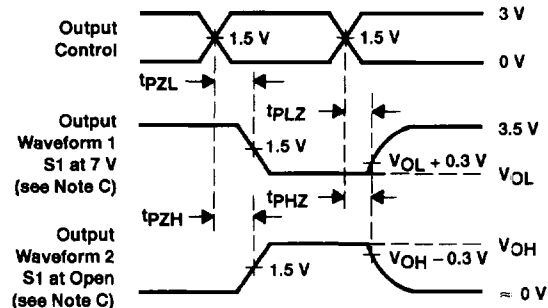| TEST | S1 |
|---|---|
| tPLH/tPHL | Open |
| tPLZ/tPZL | 7 V |
| tPHZ/tPZH | Open |



**VOLTAGE WAVEFORMS**
**PULSE DURATION**

**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**
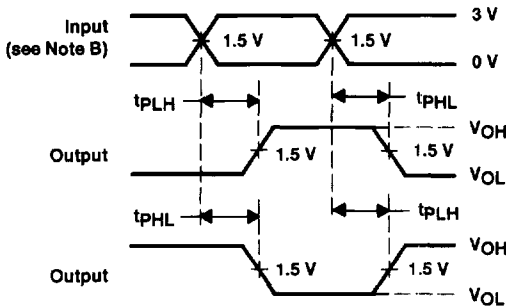
**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 15. Load Circuit and Voltage Waveforms**