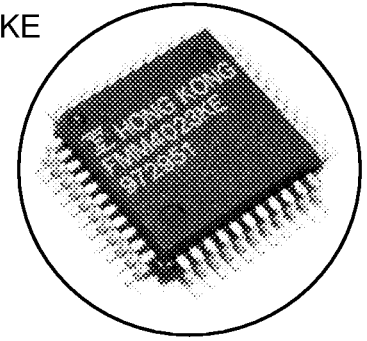


FMM4023KE

1.0625Gbps Port Bypass Circuit

KE



DESCRIPTION

The FMM4023 is a quad port bypass circuit designed with 0.5 μ m GaAs MESFET technology for 1.0625Gbps Fibre Channel applications. Small Computer Systems Interface (SCSI) is the common interface medium for large computer systems and peripherals today. Advances in multimedia have significantly increased the demand for high speed data transmission interfaces. Fibre Channel products are the next generation of serial interface which are capable of Gbps data transmission rates.

FEATURES

- 4 Loop Resiliency Circuits for 1.0625Gbps Fibre Channel
- Low Power Consumption: 0.3W
- Single Power Supply Voltage: +3.3V
- LVTTTL and PECL Interface
- Thermally Enhanced, QFP44 Mold Package with Heat Sink

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta = 25°C)

The maximum ratings are the limit values that must never be exceeded even for an instant. The device will not be damaged as long as the device is used within the maximum ratings specified.

Parameter	Symbol	Values	Unit
Supply Voltage	V _{DD}	-0.5 ~ +4.0	V
Output Current	PECL I _{OUP}	-50 ~ +50	mA
	LVTTTL I _{OUTT}	-25 ~ +25	mA
Input Voltage	PECL V _{INP}	-0.5 ~ V _{DD} +0.5	V
	LVTTTL V _{INT}	-0.5 ~ 5.5	V
Maximum Input ESD (MIL-STD-883C)	V _{ESD}	1500	V
Storage Temperature	T _{STG}	-65 ~ +150	°C
Case Temperature	T _C	-55 ~ +120	°C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions are the recommended values for assuring normal logic operation. When the device is used within the specified operating conditions, the electrical characteristics(DC and AC characteristics) described below are assured.

Parameter	Symbol	Values	Unit
Supply Voltage	V _{DD}	+3.3 ~ \pm 5%	V
AC Coupled Differential PECL Output Load	R _L	50	Ω
Ambient Temperature	T _A	0 ~ +70	°C
Junction Temperature	T _J	0 ~ +100	°C

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ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS for PECL ($V_{DD}=3.3V$, $T_A=25^\circ C$)

Parameter	Symbol	Test Conditions	Limit		Unit
			Min.	Max.	
Single Ended Output Voltage Swing	V_{OUTL}	50Ω to $V_{DD} - 2.0V$	600	1300	mV
Differential Input Voltage Swing	V_{IND}	–	200	2600	mV

DC CHARACTERISTICS FOR LVTTTL ($V_{DD}=3.3V$, $T_A=25^\circ C$)

Parameter	Symbol	Test Conditions	Value		Unit
			Min.	Max.	
Output HIGH Voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	V_{DD}	V
Output LOW Voltage	V_{OL}	$I_{OL}=+1.0mA$	0	0.6	V
Input HIGH Voltage	V_{IH}	–	2.0	5.5	V
Input LOW Voltage	V_{IL}	–	0	0.8	V
Input HIGH Current	I_{IH}	$V_{IN}=V_{DD} - 0.5V$	-	50	μA
Input LOW Current	I_{IL}	$V_{IN}=0.5V$	-500	-	μA

SUPPLY CURRENT

Parameter	Symbol	Test Conditions	Limit		Unit
			Min.	Max.	
Supply Current	I_{DD}	$V_{DD} = 3.3V$, $T_A = 25^\circ C$ 50Ω to $V_{DD} - 2.0V$	–	130	mA

AC CHARACTERISTICS ($V_{DD}=3.3V$, $T_A=25^\circ C$)

Parameter	Symbol	Test Conditions	Value		Unit
			Min.	Max.	
Serial Baud Rate	B_r		-	1300	Mbps
PECL Output Rise and Fall Time	T_{tr}, T_{tf}	20% to 80% 50Ω single ended load	-	300	pS
Random Jitter	JRC	IN to OUT(SELn=Low)	-	10	pS
Deterministic Jitter	JDC	IN to OUT(SELn=Low)	-	100	pS

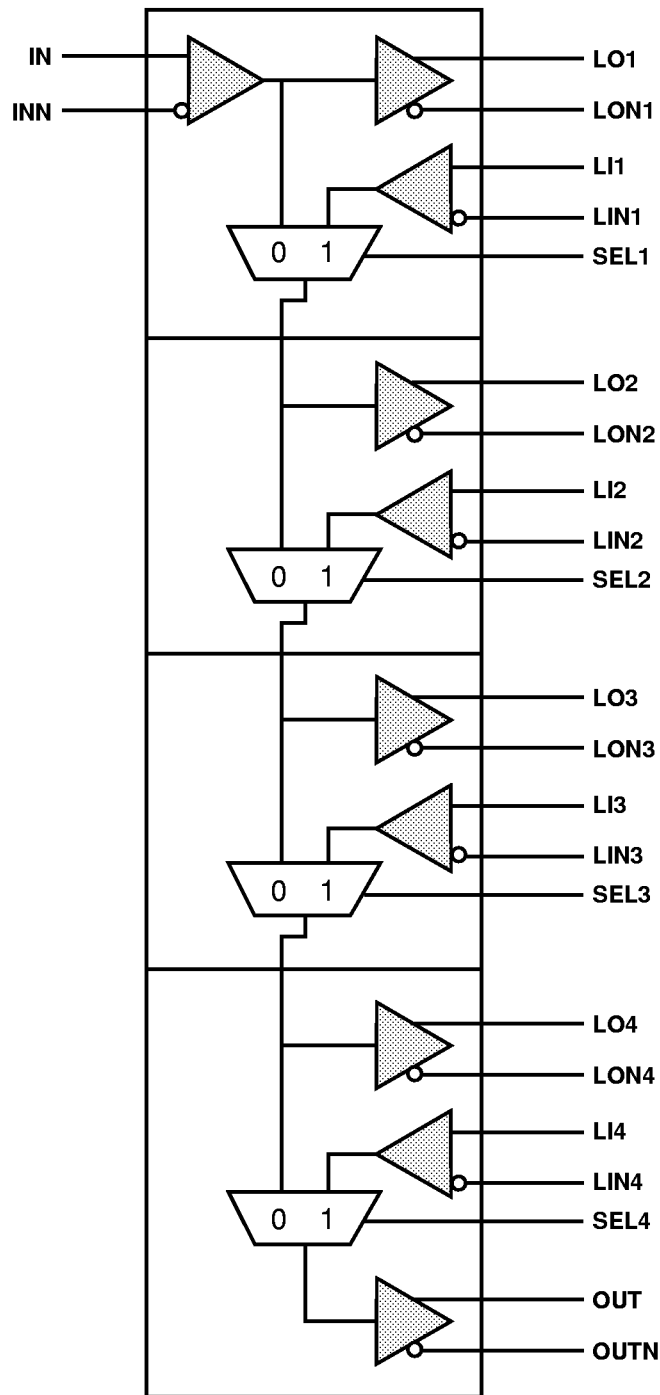


Figure 1: Functional Block Diagram of FMM4023KE

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Function of Port Bypass

The FMM4023 has four port bypass circuits cascaded into a single device. Port bypass is used to provide loop resiliency or electronic bypass in Fibre Channel Arbitrated Loop (FC-AL) configurations. The basic function of the loop resiliency circuits is a 2:1 multiplexer. There are two inputs to each bypass circuit, the loop signal (IN) and the local drive input signal (LI-n). The select signal (SELn) controls which input signal is selected. If SEL is high, the disk drive is connected to the loop. If SEL is Low, data is bypassed to the next port. If a disk drive is not present or not functioning properly, the multiplexer functions as a switch to re-route the loop signal. Table 1 shows the data flow of each multiplexer in a truth table format.

Table 1: Truth Table

SELECTOR INPUT				DATA OUTPUT				
SEL1	SEL2	SEL3	SEL4	LO1	LO2	LO3	LO4	OUT
L	L	L	L	IN	IN	IN	IN	IN
H	H	H	H	IN	LI1	LI2	LI3	LI4
H	L	L	L	IN	LI1	LI1	LI1	LI1
L	H	L	L	IN	IN	LI2	LI2	LI2
L	L	H	L	IN	IN	IN	LI3	LI3
L	L	L	H	IN	IN	IN	IN	LI4

Package Information

The FMM4023 uses a small outline, 10-mm size, thermally enhanced HQFP package. This package has a copper heat spreader for die attach to reduce the thermal resistance from chip junction to package surface.

Figure 2: Package Pin Assignment

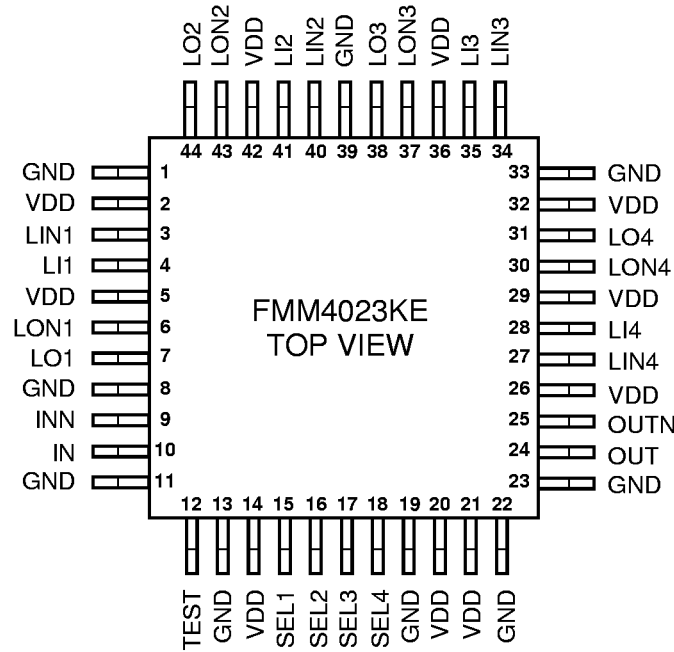


Table 2: Pin Description

Pin Name	Pin No.	I/O	Description
IN	10	I-PECL	Differential Inputs Serial inputs from downstream loop.
INN	9		
LI1	4	I-PECL	Differential Inputs Serial inputs from local transmitters.
LIN1	3		
LI2	41		
LIN2	40		
LI3	35		
LIN3	34		
LI4	28		
LIN4	27		
SEL1	15	I-TTL	Mode Control Inputs These signals are used as selector switches of each 2:1 multiplexer.
SEL2	16		
SEL3	17		
SEL4	18		
TEST	12	I-TTL	Factory Test Pin This signal used for factory test only. For normal operation, connect to logic "0" or leave open. This signal pin is internally pulled down.
OUT	24	O-PECL	Differential Outputs Serial outputs for local receivers.
OUTN	25		
LO1	7	O-PECL	Differential Outputs Serial outputs for local receivers.
LON1	6		
LO2	44		
LON2	43		
LO3	38		
LON3	37		
LO4	31		
LON4	30		

I-TTL: LVTTTL INPUT, I-PECL: PECL INPUT, O-PECL: PECL OUTPUT

Table 3: Pin Description of Power Supply Voltage

Pin Name	Pin No.	Description
GND	1, 8, 11, 13, 19, 22, 23, 33, 39	Power Supply: 0V
VDD	2, 5, 14, 20, 21, 26, 29, 32, 36, 42	Power Supply: +3.3V

Table 4: Propagation Delay

Parameter	Symbol	Values		Unit
		Min.	Max.	
Propagation Delay (Up to Up)	TPDU	-	7.0	nS
Propagation Delay (Down to Down)	TPDD	-	7.0	nS

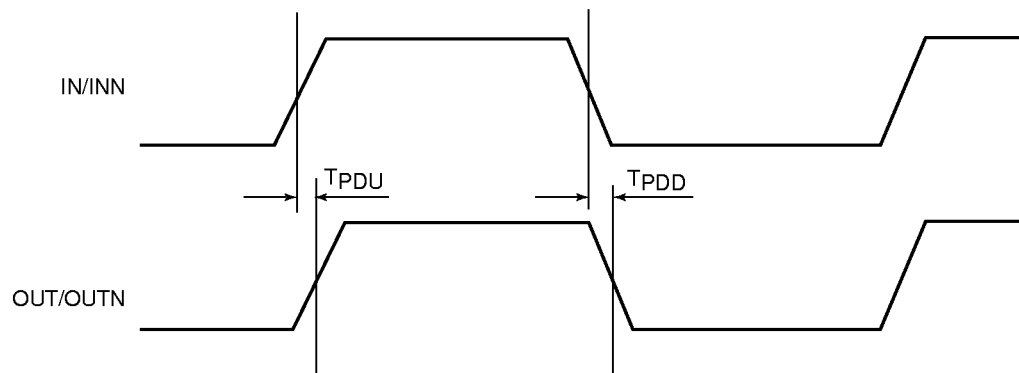


Figure 3: Propagation Delay

High Speed Signal Termination

The FMM4023 has two high speed output pins. These pins must be terminated to pseudo ECL termination levels ($V_{DD}-2.0V$). Figure 4 shows the typical termination circuit.

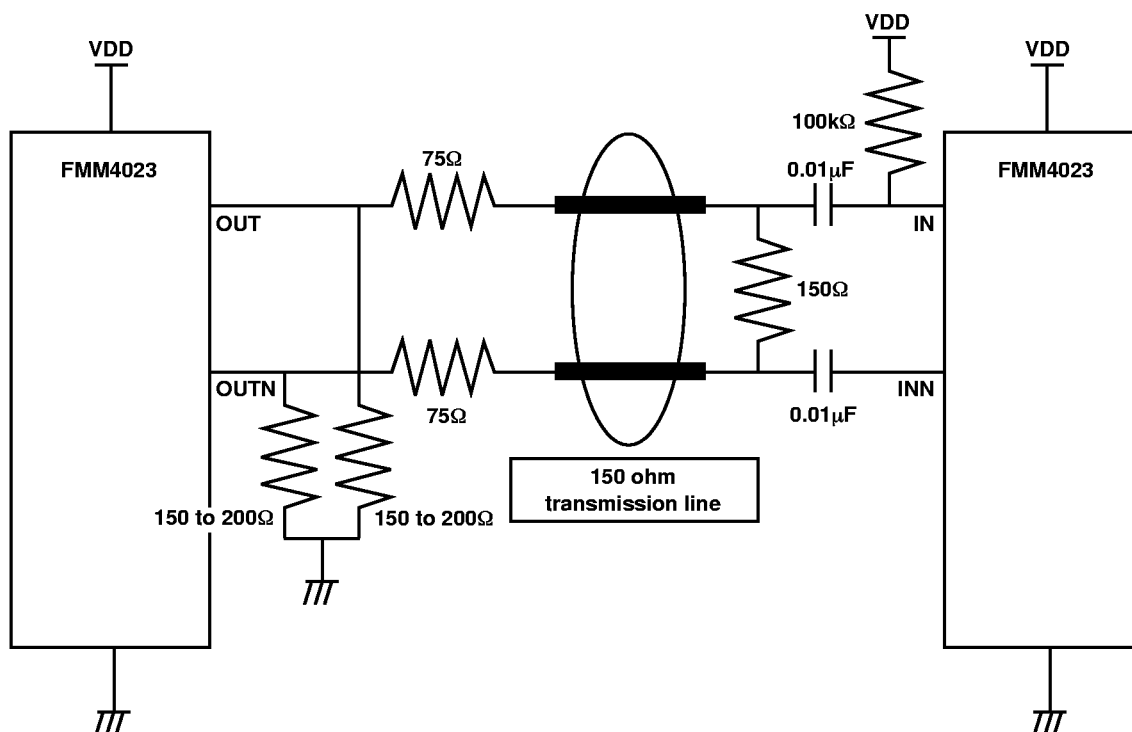


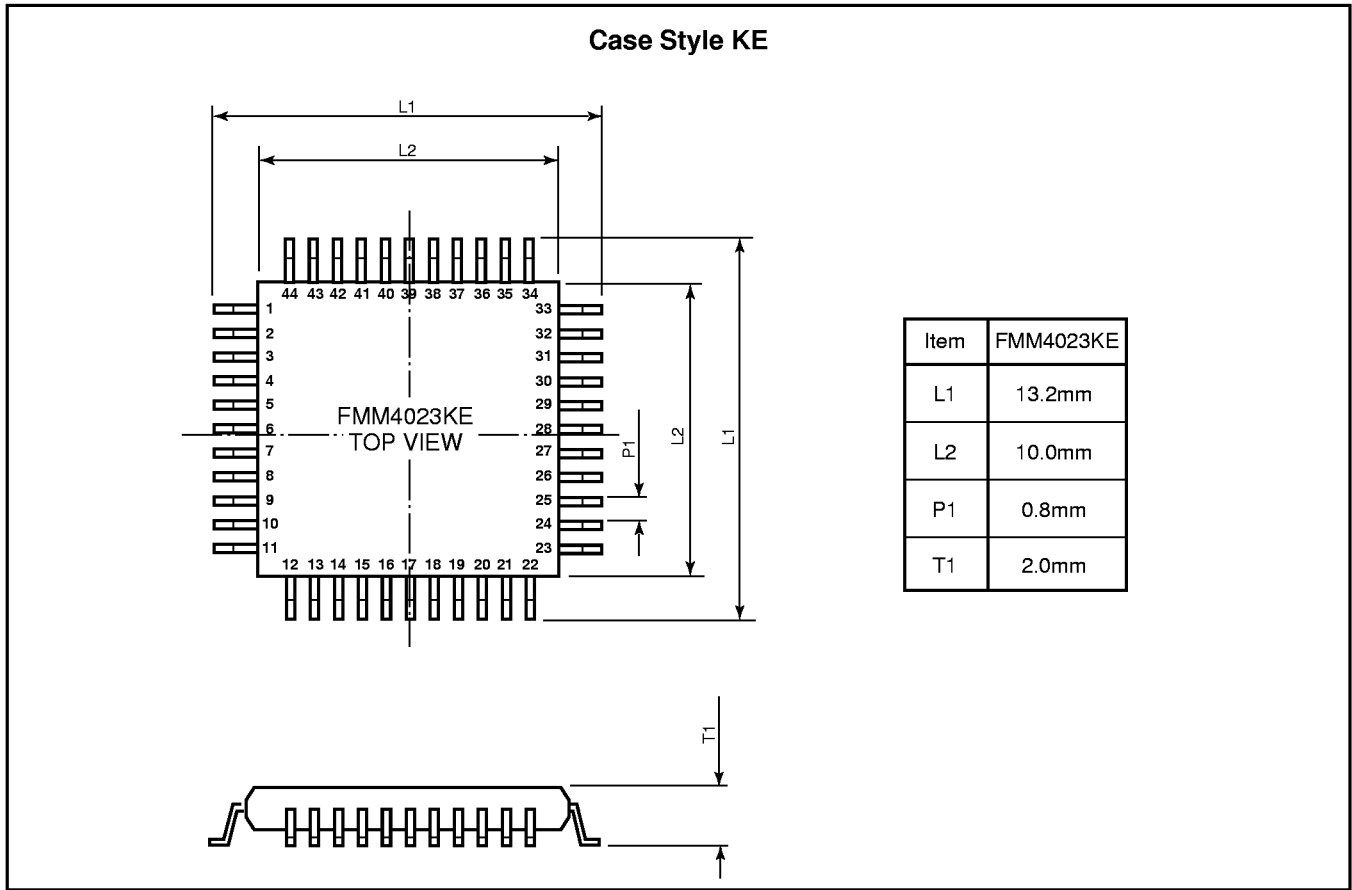
Figure 4: Termination Circuit for PECL Output

Power Supply Circuit

To reduce power supply noise, bypass capacitor should be used as close as possible to each power supply pin. All bypass capacitors are 0.1 μF ceramic chip capacitors.

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