LG Semicon Co.,Ltd.

GM72V66841CT -7/8/10

2,097,152 WORD x 8 BIT x 4 BANK
SYNCHRONOUS DYNAMIC RAM

Description

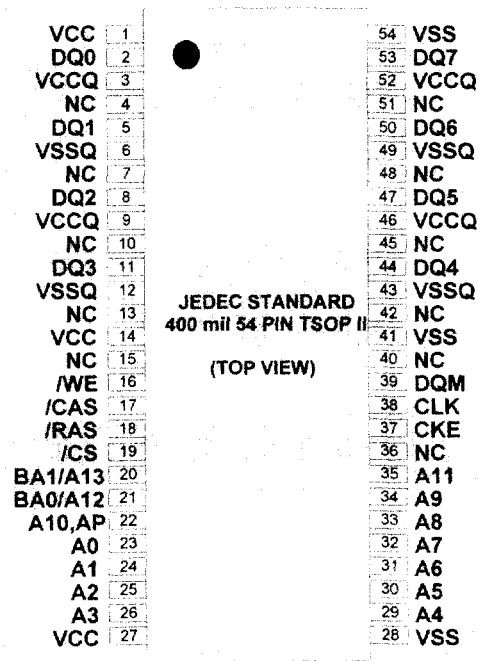
The GM72V66841CT is a synchronous dynamic random access memory comprised of 67,108,864 memory cells and logics including input and output circuits operating synchronously by refering to the positive edge of the externally provided clock.

The GM72V66841CT provides four banks of 2,097,152 word by 8 bit to realize high bandwidth with the clock frequency up to 125 Mhz.

Features

- 3.3V single power supply
- LVTTL interface
- Max clock frequncy for $\overline{CAS}$ latency of 3
  100/125 MHz
- 4,096 refresh cycle per 64 ms
- Two kind of refresh operation
  Auto refresh/ Self refresh
- Programmable burst access capability ;
  - Sequence:Sequential / Interleave
  - Length :1/2/4/8/FP
- Programmable $\overline{CAS}$ latency : 2/3
- 4 Banks can operate independently or simultaneously
- Burst read/burst write or burst read/single write operation capability
- Input and output masking by DQM input
- One clock of back to back read or write command interval
- Synchronous power down and clock suspend capablity with one clock latency for both entry and exit
- JEDEC Standard 54Pin 400mil TSOP II Package

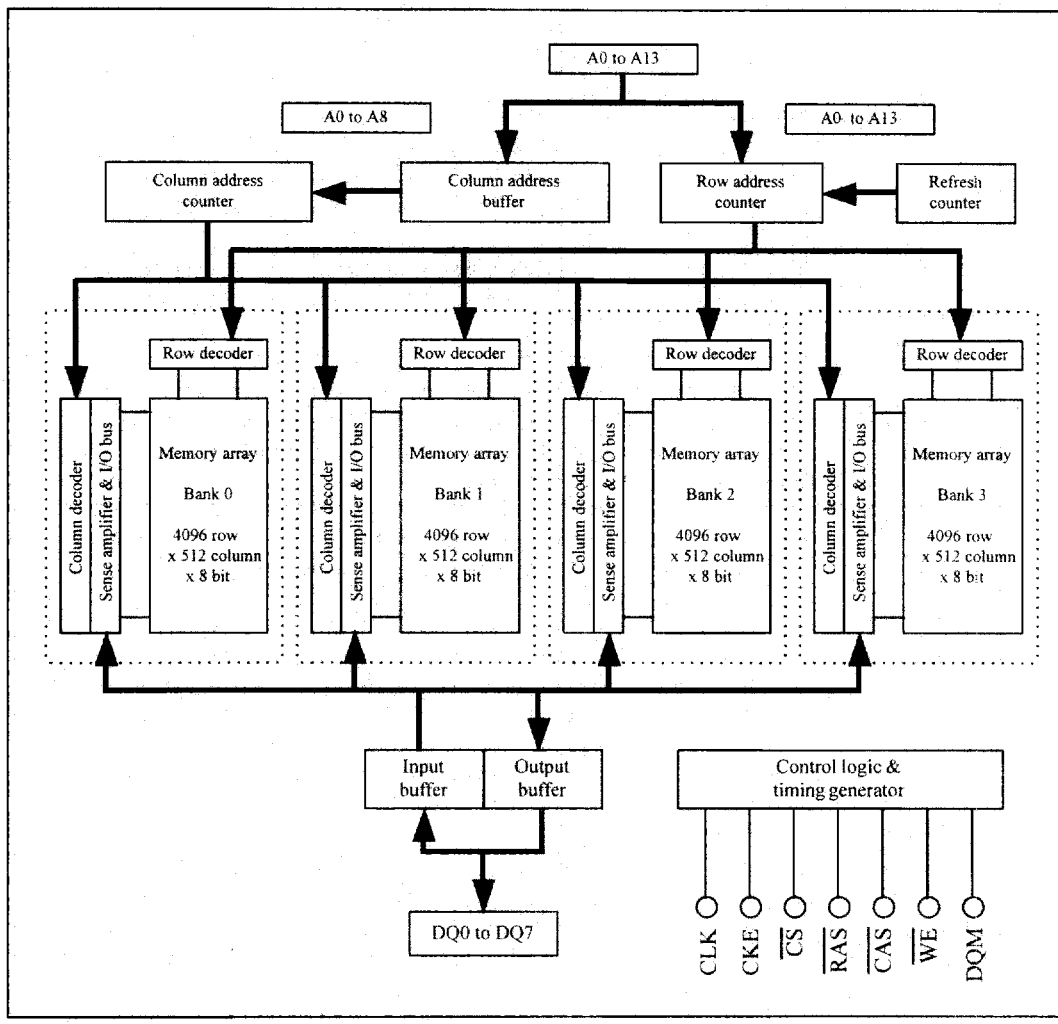
Pin Configuration



Pin Name

CLK	CLocK
CKE	ClocK Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A9,A11	Address input
A10 / AP	Address input or Auto Precharge
BA0/A12	Bank select
~BA1/A13	
DQ0~DQ7	Data input / Data output
DQM	Data input / output Mask
VCCQ	Vcc for DQ
VSSQ	Vss for DQ
VCC	Power for internal circuit
VSS	Groud for internal circuit
NC	No Connection

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. Column address(AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) is determined by A0 to A7, A8 or A9 (A7; GM72V661641CT, A8;GM72V66841CT, A9; GM72V66441CT) level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A12/A13 (BS) is precharged.
A12/A13 (input pin)	A12/A13 are bank select signal (BS). The memory array of the GM72V661641CT, the GM72V66841CT, and the GM72V66441CT is divided into bank 0, bank 1, bank2 and bank 3. GM72V661641CT contain 4096-row x 256-column x 16-bits. GM72V66841CT contain 4096-row x 512-column x 8-bits. GM72V66441CT contain 4096-row x 1024-column x 4-bits. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.
DQM, DQMU/DQML (input pins)	DQM, DQMU/DQML controls input/output buffers. • Read operation: If DQM, DQMU/DQML is High, The output buffer becomes High-Z. If the DQM, DQMU/DQML is Low, the output buffer becomes Low-Z. • Write operation: If DQM, DQMU/DQML is High, the previous data is held (the new data is not written). If DQM, DQMU/DQML is Low, the data is written.

Pin Description(Continued)

Pin Name	DESCRIPTION
DQ0 ~ DQ7 (I/O pins)	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A12~A13	A10	A0~A11
		n-1	n							
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank active	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	V	V	V

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}, V: Valid address input

• **Ignore command [DESL]:** When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignores command input at the clock. However, the internal status is held.

• **No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

• **Burst stop in full page [BST] :** This command stops a full-page burst operation (burst length = full-page(256 ; GM72V661641CT, 512 ; GM72V66841CT, 1024 ; GM72V66441CT)), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

• **Column address strobe and read command [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY7 ; GM72V661641CT , AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13). After the read operation, the output buffer becomes High-Z.

• **Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

• **Column address strobe and write command [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13).

• **Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

• **Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A12/A13(BS) and determines the row address (AX0 to AX11). If A12 is Low and if A13 is Low, bank 0 is activated. If A12 is High and A13 is Low, bank 1 is activated. If A12 is Low and A13 is High, bank 2 is activated. If A12 is High and A13 is High, bank 3 is activated.

• **Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A12/A13. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.

• **Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

• **Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

• **Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE		DQM
		n-1	n	
Write enable/output enable	ENB	H	X	L
Write inhibit/output disable	MASK	H	X	H

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
Write : I_{DID} is needed.
Read : I_{DOD} is needed.

The GM72V66841CT can mask input/output data by means of DQM.
During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the GM72V66841CT operating instructions.

CKE Truth Table

Current State	Function	CKE n -1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry	H	L	H	X	X	X	X
Any	Clock suspend	L	L	X	X	X	X	X
Clock Suspend	Clock suspend mode exit	L	H	X	X	X	X	X
Idle	Auto-refresh (REF) command	H	H	L	L	L	H	X
Idle	Self-refresh (SELF) entry	H	L	L	L	L	H	X
Idle	Power down entry	H	L	L	H	H	H	X
		H	L	H	X	X	X	X
Self refresh	Self refresh (SELFX) exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Power down	Power down Exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

• **Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

• **ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

• **READ suspend and READ A suspend:** The data being output is held (and continues to be output).

• **WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

• **Clock suspend:** During clock suspend mode, keep the CKE to Low.

• **Clock suspend mode exit :** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

• **IDLE:** In this state, all banks are not selected, and completed precharge operation.

• **Auto-refresh command[REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4,096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

• **Self-refresh entry[SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

• **Self-refresh exit[SELFX]:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

• **Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

• **Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active *1 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

* Notes : 1. H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
The other combinations are inhibit.
2. An interval of t_{RWL} is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, this operation is illegal.
4. BA:Bank Address, RA:Row Address, CA:Column Address

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the Idle state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-0.5 to Vcc+0.5 ($\leq$ 4.6 (max))	V	1
Supply voltage relative to Vss	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2 , 3
Input low voltage	V_{IL}	-0.3	0.8	V	1, 4

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = Vcc + 0.5V for pulse width $\leq$ 5ns at Vcc.(DQ pins).

3. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

4. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ±0.3 V, Vss, V_{SSQ}= 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current	(CL= 2)	I_{CC1}	-	60	-	65	-	50	mA	Burst length= 1 t_{RC} = min	1, 2, 3
	(CL= 3)	I_{CC1}	-	80	-	85	-	70	mA		
Standby current in power down		I_{CC2P}	-	3	-	3	-	3	mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)		I_{CC2PS}	-	2	-	2	-	2	mA	CKE=V_{IL}, t_{CK}= ∞	6
Standby current in non power down ($\overline{CAS}$ latency=2)		I_{CC2N}	-	20	-	20	-	20	mA	CKE,CS = V_{IH}, t_{CK} = 12ns	4
Standby current in non power down (input signal stable)		I_{CC2NS}	-	9	-	9	-	9	mA	CKE = V_{IH}, t_{CK} = ∞	8
Active standby current in power down		I_{CC3P}	-	6	-	6	-	6	mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		I_{CC3PS}	-	5	-	5	-	5	mA	CKE = V_{IL}, t_{CK} = ∞	2,6
Active standby current in non power down		I_{CC3N}	-	30	-	30	-	30	mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		I_{CC3NS}	-	20	-	20	-	20	mA	CKE = V_{IH}, t_{CK} = ∞	2,8
Burst operating current	(CL= 2)	I_{CC4}	-	70	-	95	-	70	mA	t_{CK} = min BL = 4	1,2,3
	(CL= 3)	I_{CC4}	-	120	-	155	-	120	mA		
Refresh current	(CL= 2)	I_{CC5}	-	80	-	85	-	60	mA	t_{RC} = min	3
	(CL= 3)	I_{CC5}	-	130	-	140	-	110	mA		
Self refresh current		I_{CC6}	-	2	-	2	-	2	mA	$V_{IH} \geq V_{CC}$ - 0.2 $V_{IL} \leq 0.2V$	7

Parameter	Symbol	-7		-8		-10		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \leq Vin \leq Vcc$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \leq Vout \leq Vcc$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance ($Ta = 25℃$, V_{CC}, $V_{CCQ} = 3.3\ V \pm 0.3\ V$)

Parameter	Symbol	Typ.	Max.	Unit	Notes
Input capacitance (CLK)	C_{I1}	-	4	pF	1, 3, 4
Input capacitance (Signals)	C_{I2}	-	5	pF	1, 3, 4
Output capacitance (DQ)	C_O	-	6.5	pF	1, 2, 3, 4

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM, DQMU/DQML = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.
4. Measured with 1.4 V bias at the pin under measurement.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	15	-	12	-	15	-	ns	1
	(CL=3)	t_{CK}	10	-	8	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	7	-	8	-	9	ns	1, 2
	(CL=3)	t_{AC}	-	6	-	6	-	8		
Data-out hold time		t_{OH}	2.5	-	2.5	-	2.5	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedence (CL = 2,3)		t_{HZ}	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t_{DS}	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	72	-	90	-	ns	1
Active to Precharge command period		t_{RAS}	50	120000	48	120000	60	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	24	-	30	-	ns	1
Precharge to active command period		t_{RP}	20	-	24	-	30	-	ns	1

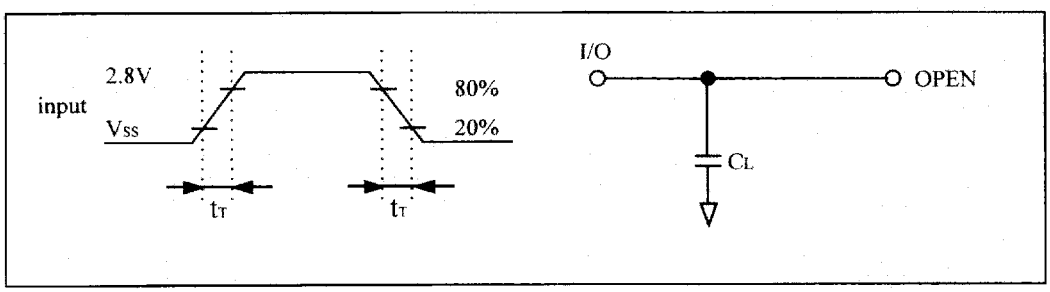
AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	-7		-8		-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7		-8		-10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Active command to column command (same bank)		l_{RCD}	3	2	3	2	3	2	1
Active command to active command (same bank)		l_{RC}	7	6	9	6	9	6	= [l_{RAS} + l_{RP}], 1
Active command to precharge command (same bank)		l_{RAS}	5	4	6	4	6	4	1
Precharge command to active command (same bank)		l_{RP}	2	2	3	2	3	2	1
Write recovery or data-in to precharge command (same bank)		l_{RWL}	1	1	1	1	1	1	1
Active command to active command (different bank)		l_{RRD}	2	2	2	2	2	2	1
Self refresh exit time		l_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		l_{APW}	5	3	5	3	5	3	= [l_{RWL} + l_{RP}], 1
Self refresh exit to command input		l_{SEC}	9	6	9	6	9	6	= [l_{RC}]
Precharge command to high impedence	(CL=2)	l_{HZP}	-	2	-	2	-	2	
	(CL=3)	l_{HZP}	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)		l_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=2)	l_{EP}	-	-1	-	-1	-	-1	
	(CL=3)	l_{EP}	-2	-2	-2	-2	-2	-2	
Column command to column command		l_{CCD}	1	1	1	1	1	1	
Write command to data in latency		l_{WCD}	0	0	0	0	0	0	
DQM to data in		l_{DID}	0	0	0	0	0	0	
DQM to data out		l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable		l_{CLE}	1	1	1	1	1	1	
Register set to active command		l_{RSA}	1	1	1	1	1	1	
$\overline{CS}$ to command disable		l_{CDD}	0	0	0	0	0	0	
Power down exit to command input		l_{PEC}	1	1	1	1	1	1	

Relationship Between Frequency and Minimum Latency

Parameter		Symbol	- 7		- 8		- 10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	-	1	-	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	
Burst stop to output high impedence	(CL=2)	l_{BSH}	-	2	-	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	

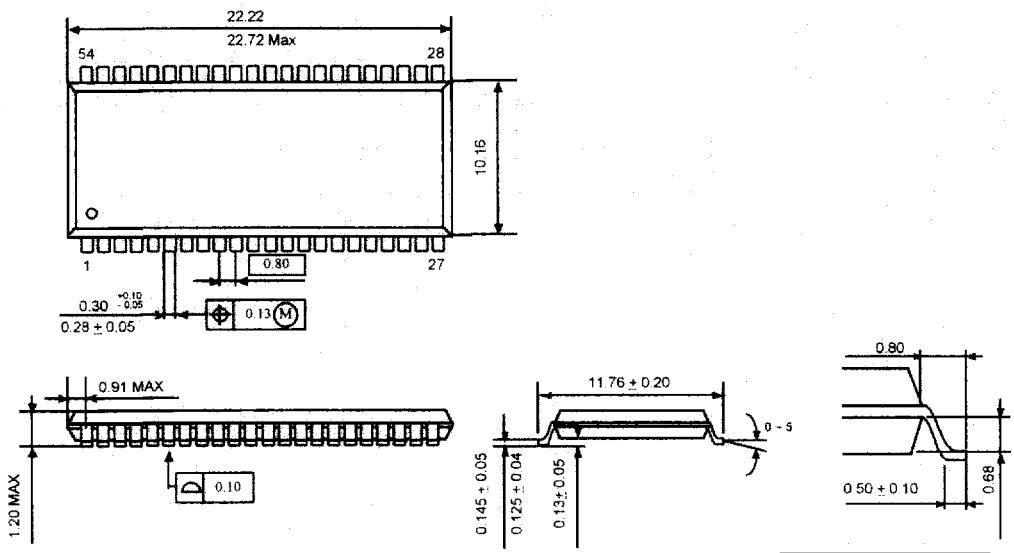
Notes : 1. l_{RCD} to l_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimensions

GM72V66841CT Series (TTP-54D)

Preliminary

Unit: (mm)



Hitachi Code	TTP-54D
JEDEC Code	-
EIAJ Code	-
Weight(reference value)	0.53g

Dimension including the plating thickness
Base material dimension