CL-GD1052/GD1053

Advance Data Book

FEATURES

- **TV encoder**
  - — VGA controller and MPEG digital encoder inputs
  - — NTSC and PAL output
- **S-Video and composite video output**
  - — S-Video luminance and chrominance
  - — Composite video
- **Macrovision® copy protection (CL-GD1053)**
  - — Macrovision® Revision 7
  - — Programmable parameters
  - — Enables DVD movie and DSS satellite content to be played through graphics device
- **Two-wire serial host interface**
  - — Read/write access to all register resources
  - — Up to 1 Mbit/sec.
- **Dynamic adaptive flicker-filter processing**
  - — Five tap filter
  - — Text mode improves legibility
  - — Graphics mode for minimum flicker
  - — Movie mode for smooth picture
  - — Four filter levels:
    - Two 5-tap filters
    - One 3-tap filter
    - One combination tap filter
- **Internal color bar generator**
  - — 100% amplitude, 100% saturation EIA colors (NTSC)
- **WSS support for NTSC and PAL**

(cont.)

Digital NTSC/PAL Encoder with Flicker-Filter Preprocessor

CL-GD1052: without Macrovision®
CL-GD1053: with Macrovision® Rev. 7

OVERVIEW

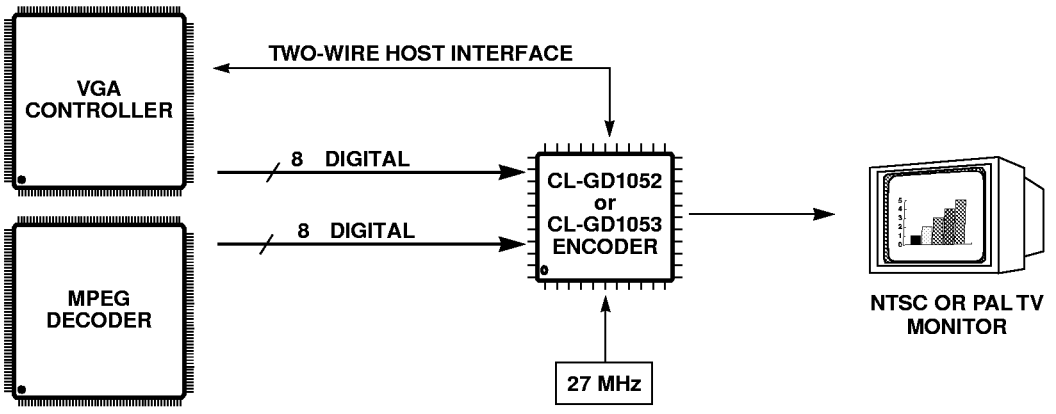
The CL-GD1052/GD1053 is a digital television encoder that accepts video from a VGA controller, MPEG decoder, or DSS satellite and produces NTSC or PAL video. The CL-GD1052/GD1053 can simultaneously produce composite video and S-Video (separate luminance and chrominance).

The CL-GD1053 supports Macrovision copy protection Revision 7. This industry-standard anti-copy method allows DVD- and DSS-based video to display on a TV while simultaneously defeating attempts to make a usable video tape copy.

The CL-GD1052/GD1053 incorporates a two-wire serial host interface that provides read/write access to all programmable registers. This interface operates internally at 27 MHz, allowing a relatively high data transfer rate.

(cont.)

System Block Diagram



FEATURES (cont.)

- **Localization software support**
- **Video window**
  - — Allows video within video
  - — Programmable position and size
- **Scaling**
  - — Horizontal upscaling and downscaling
  - — Vertical downscaling
  - — Input formats from 320 × 400 to 800 × 600
  - — Scales to NTSC or PAL
- **Closed caption insertion (NTSC)**
  - — Line 21 and/or 284
- **Power down by software or PDN pin**
- **Interrupt request output**
  - — Closed caption line 21
  - — Closed caption line 284
  - — Every video field
- **Cost-effective 44-pin PLCC package**

OVERVIEW (cont.)

The CL-GD1052/GD1053 incorporates an intelligent adaptive flicker-filter processor. This processor dynamically selects one of four filters based on the local two-dimensional picture content. This allows more flicker filtering in picture areas where it is useful, while minimizing the loss in resolution in areas where filtering is not necessary. Also included is a text mode that improves legibility, and a movie mode that provides a more pleasing blended picture on the TV screen.

A programmable video window allows two video streams to be displayed simultaneously. The size and position of the window can be programmed into internal registers in the CL-GD1052/GD1053.

The CL-GD1052/GD1053 accepts a number of input formats (from 320 × 400 up to 800 × 600) and scales them to interlaced NTSC or PAL.

Software Support

- **BIOS support**
  - — Autodetection of TV or monitor
  - — VGA Compatibility modes to 800 × 600
  - — PC97 compliant (entertainment PC97)
- **OS support**
  - — Windows® 95, Windows 97
  - — NT 4.0, 5.0
- **TV-Out tab on display properties**
  - — Centering
  - — NTSC/PAL
  - — Test pattern
  - — Filter selection
  - — TV-display adjustments (luminance)

TV Standards

Standard	Device Support	BIOS[a] Support
NTSC-J (Japan)	✔	✔
NTSC-M	✔	✔
PAL-B, G	✔	–
PAL-H	✔	–
PAL-I	✔	–
PAL-N (Argentina)	✔	–
PAL-N (non-Argentina)	✔	–
PAL-D	✔	–
PAL-M	✔	–
NTSC-N	No	No
SECAM	No	No

[a] Initial product offering.

Typical VGA Display Formats

Input Format	Active Pixels	DOT_CLKX2	Scaled Output Size	Vertical Scaling	Horizontal Scaling
Interlaced NTSC	720 × 480/2	27.000	720 × 480/2	5/5	1.00000
Interlaced PAL	720 × 576/2	27.000	720 × 576/2	5/5	1.00000
Non-interlaced NTSC	320 × 400	24.924	580 × 400/2	5/5	1.81250
	360 × 400	27.692	580 × 400/2	5/5	1.61111
	400 × 600	41.236	640 × 428/2	5/7	1.60000
	512 × 768	64.800	640 × 426/2	5/9	1.25000
	640 × 350	44.308	508 × 350/2	5/5	0.79375
	640 × 400	44.308	580 × 400/2	5/5	0.90625
	640 × 480	44.308	692 × 480/2	5/5	1.08125
	640 × 480	54.982	580 × 400/2	5/6	0.90625
	720 × 400	49.090	580 × 400/2	5/5	0.80556
	800 × 600	77.538	640 × 482/2	5/7	0.80000
Non-interlaced PAL	320 × 400	24.750	502 × 400/2	5/5	1.56875
	360 × 400	27.500	502 × 400/2	5/5	1.39444
	400 × 600	35.100	588 × 500/2	5/6	1.47000
	512 × 768	57.600	580 × 480/2	5/8	1.13281
	640 × 350	44.000	440 × 350/2	5/5	0.68750
	640 × 400	44.000	502 × 400/2	5/5	0.78438
	640 × 480	44.000	580 × 480/2	5/5	0.90625
	720 × 400	49.000	502 × 400/2	5/5	0.69722
	800 × 600	66.000	588 × 500/2	5/6	0.73500

REVISION HISTORY

Major changes between the previous data book (dated June 1997) and this version are listed below.

Section	Revision
Overview	NTSC-J for Japan added.
3.2	Digital video pins: VID1IO has text added.
9.1	Global registers Address 01h[2]: power on value changed from '0' to '1' Address 03[3]: power on value changed from '0' to '1'
9.3	VGA Synchronization registers Address 0Dh: power on value changed from '1000 0000' to '0000 0000' Address 0Fh: power on value changed from '0111 1000 = 480 decimal' to '0'
9.5	Serial Address Interface register Address 15h[7:0]: The bit is reserved
9.10	Status registers Address 42h: power on values changed to: '0011 0100 (CL-GD1052) and 0011 0101 (CL-GD1053)'
9.12	Typical values Register 1Ah, Byte 3: Interlaced PAL and Non-interlaced PAL changed to '0100 0100'
Bit Index	New
index	New

Table of Contents

1. CONVENTIONS

Abbreviations

Symbol	Units of measure
°C	degree Celsius
Hz	hertz (cycles per second)
Kbyte	kilobyte (1,024 bytes)
kHz	kilohertz (1,000 Hertz)
kΩ	kilohm
Mbyte	megabyte (1,048,576 bytes)
MHz	megahertz (1,000 kilohertz)
µA	microampere
µH	microhenry
µF	microfarad
µs	microsecond (1,000 nanoseconds)
µW	microwatts
mA	milliampere
ms	millisecond (1,000 microseconds)
ns	nanosecond
pF	picofarad
pV	picovolt
V	volt

The use of 'tbd' indicates values that are 'to be determined'; 'n/a' designates 'not available'; and 'n/c' indicates a pin that is a 'no connect'.

Acronyms

Acronym	Definition
AC	alternating current
BIOS	basic input/output system
bpp	bits-per-pixel
CCIR	Consultative Committee for International Radio
CMOS	complementary metal-oxide semiconductor
CRT	cathode ray tube
DAC	digital-to-analog converter
DSS	direct satellite service
DVD	digital versatile disk
EIA	Electronic Industries Association
FIFO	first in/first out
HSYNC/VSYNC	horizontal/vertical synchronization
MPEG	Moving Pictures Experts Group
NTSC	National Television System Committee
PAL	phase alternation (or alternating) line
PCI	peripheral component interconnect
PLL	phase-locked loop
PLCC	plastic leaded chip carrier
RGB	red, green, and blue
R/W	read/write
SECAM	Systeme Electronique Couleur Avec Memoire (Sequential Color with Memory)
VGA	video graphics array

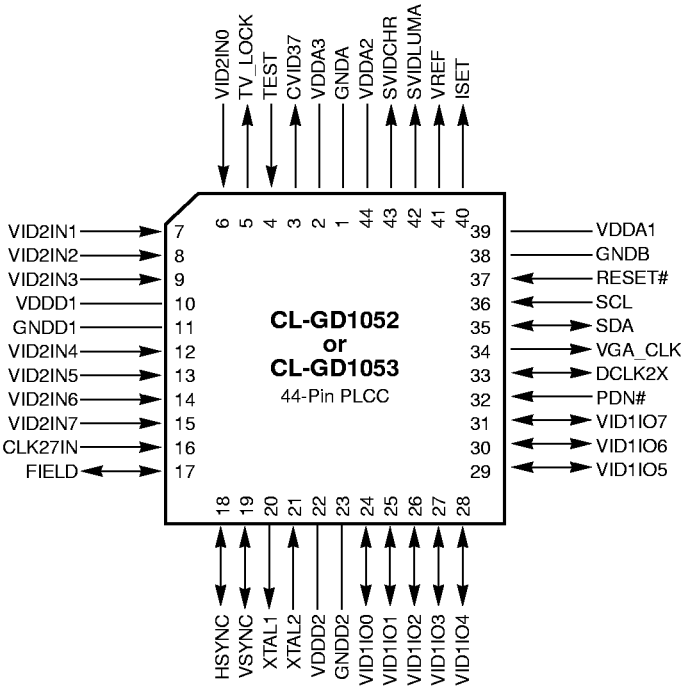
Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase and appended with a lowercase ‘h’ (for example, ‘14h’, ‘3A7h’, and ‘C000h’ are hexadecimal numbers). Binary numbers are appended with a lowercase ‘b’. Numbers not indicated by a ‘b’ or an ‘h’ are decimal.

2. PIN INFORMATION

The CL-GD1052/GD1053 is available in a 44-pin PLCC package.

2.1 Pin Diagram — 44-Pin PLCC



2.2 Pin Summary

2.2.1 Pin Type Definitions

The following tables list each CL-GD1052/GD1053 pin by name, functional pin type, and number. Functional pin types are abbreviated as follows:

Type	Abbreviation
Analog	A
Input	I
Output	O
Power	PWR

Type	Abbreviation
Ground	GND
Input/output	I/O
Open collector	OC
Tristate output	TS

2.3 Microprocessor Interface and Two-Wire Serial Interface Pins

Name	Pin (PLCC)	Type	I_{OH} (mA)	I_{OL} (mA)
SCL	36	I	–	–
SDA	35	I/O	–	6
PDN#	32	I	–	–
RESET#	37	I	–	–
TEST	4	I	–	–
TV_LOCK	5	O	–4	4

2.4 Digital Video Pins

Name	Pin (PLCC)	Type	I_{OH} (mA)	I_{OL} (mA)
VID1IO0	24	I/O	–4	4
VID1IO1	25	I/O	–4	4
VID1IO2	26	I/O	–4	4
VID1IO3	27	I/O	–4	4
VID1IO4	28	I/O	–4	4
VID1IO5	29	I/O	–4	4
VID1IO6	30	I/O	–4	4
VID1IO7	31	I/O	–4	4
VID2IN0	6	I	–	–
VID2IN1	7	I	–	–
VID2IN2	8	I	–	–

2.4 Digital Video Pins *(cont.)*

Name	Pin (PLCC)	Type	I_{OH} (mA)	I_{OL} (mA)
VID2IN3	9	I	–	–
VID2IN4	12	I	–	–
VID2IN5	13	I	–	–
VID2IN6	14	I	–	–
VID2IN7	15	I	–	–

2.5 Clock and Timing Pins

Name	Pin (PLCC)	Type	I_{OH} (mA)	I_{OL} (mA)
CLK27IN	16	I	–	–
FIELD	17	I/O	–4	4
HSYNC	18	I/O	–4	4
VSYNC	19	I/O	–4	4
XTAL1	20	O	–	–
XTAL2	21	I	–	–
DCLK2X	33	I/O	–4	4
VGA_CLK	34	O	–4	4

2.6 DAC Pins

Name	Pin (PLCC)	Type	I_{OH} (mA)	I_{OL} (mA)
ISET	40	A	–	–
VREF	41	A	–	–
SVIDLUMA	42	Analog Out		
SVIDCHR	43			
CVID37	3			

2.7 Power and Ground Pins

Name	Pin (PLCC)	Type
VDDD1	10	PWR
VDDD2	22	PWR
VDDA1	39	PWR
VDDA2	44	PWR
VDDA3	2	PWR
GNDD1	11	GND
GNDD2	23	GND
GNDA	1	GND
GNDB	38	GND

3. DETAILED PIN DESCRIPTIONS

The following tables provide a detailed description of each CL-GD1052/GD1053 pin by name and functional type.

3.1 Microprocessor Interface and Two-Wire Serial Interface Pins

Name	Type	Description
SCL	I	**Serial Interface Clock:** This is the two-wire serial interface clock. This is always an input on the CL-GD1052/GD1053. Data is clocked into and out of the SDA pin on the positive edge of this input.
SDA	I/O	**Serial Interface Data:** This is the two-wire serial interface data pin. This is an input when a two-wire serial interface write is occurring; this is an open-drain output when a two-wire serial interface read is occurring.
PDN#	I	**Power Down #:** When this input is driven low, the CL-GD1052/GD1053 is placed in a low-power state. All internal clocks are disabled and all three DACs are powered down. The nominal device power dissipation in Power Down mode is 100 µW. All input pins must be held at valid levels or can transition between valid levels with normal edge rates.
RESET#	I	**Reset #:** This active-low input forces the CL-GD1052/GD1053 into an initialized state. Register bits with defined reset states are forced to those reset states. RESET# should be active when power is applied to the device.
TEST	I	**Test:** This active-high input places the CL-GD1052/GD1053 into Factory Test mode. This is intended for factory test purposes only. This pin can be tied directly to ground in an application design.
TV_LOCK	O	**TV_LOCK:** This pin provides timing information to the VGA controller. The relationship of this signal with respect to HSYNC and VSYNC is programmable.

3.2 Digital Video Pins

Name	Type	Description
VID1IO [7:0]	I/O	**Video 1 I/O [7:0]:** This bus is an input when the IN_SEL field is either '00b' or '10b' and is an output when the IN_SEL field is '11b'. This bus has a data format of ITU-656, which only accepts YCbCr digital input format.
VID2IN [7:0]	I	**Video 2 In [7:0]:** This bus in an input when the IN_SEL field is '01b', '10b', or '11b'.

3.3 Clock and Timing Pins

Name	Type	Description
CLK27IN	I	**27-MHz Clock in:** This pin is a reference clock input. TV timing is generated from this reference.
FIELD	I/O	**Field:** This pin indicates the current field (odd/even) when the CL-GD1052/GD1053 is in Master Timing mode. This pin is unused when the CL-GD1052/GD1053 is in Slave Timing mode.
HSYNC	I/O	**HSYNC/Composite Blank:** This pin is composite blank or horizontal sync out when the CL-GD1052/GD1053 is in Master Timing mode. This pin is horizontal sync in when the CL-GD1052/GD1053 is in Slave Timing mode.
VSYNC	I/O	**VSYNC:** This pin is vertical sync out when the CL-GD1052/GD1053 is in Master Timing mode. This pin is vertical sync in when the CL-GD1052/GD1053 is in Slave Timing mode.
XTAL1	O	**XTAL1:** This pin is used with the XTAL2 pin to control an on-chip oscillator. This oscillator is typically used to generate 14.31818 MHz for VGA reference or subcarrier reference clock.
XTAL2	I	**XTAL2:** This pin is used with the XTAL1 pin to control an on-chip oscillator. If an external reference is supplied for this function, inject it on this pin.
DCLK2X	I/O	**Dot Clock 2x:** This clock is nominally two times the VGA pixel clock. This pin is typically an input, but becomes an output if IN_SEL is programmed to '11'.
VGA_CLK	O	**VGA_CLK:** When this pin is configured as a clock output, it can source the frequency from the on-chip oscillator, the CLK27IN, or one-half the frequency on CLK27IN. **INT:** When this pin is configured as an interrupt output, this active-high output indicates that the event associated with an enabled interrupt has occurred. The pin remains high until the corresponding clear interrupt bit is set.

3.4 DAC Pins

Name	Type	Description
ISET	A	**DAC Current Set:** This pin sets the full-scale DAC outputs. This pin connects to a resistor (typically 9.5 kΩ) returned to analog ground.
VREF	A	**External Voltage Reference In:** This pin can be used to inject an external voltage reference. Normally it is not connected.
SVIDLUMA	A	**S-Video Luminance Output:** This is the analog output for S-Video luminance. This DAC should be terminated in 37.5 Ω. A 75-Ω resistor to analog ground provides half the termination (the other half is in the monitor). Place this resistor close to the CL-GD1052/GD1053. An LC filter (consisting of a 330-pF input capacitor, a 2.2-µH inductor, and 220-pF output capacitor) connects this DAC to the respective connector pin. The capacitors are returned to analog ground.
SVIDCHR	A	**S-Video Chrominance Output:** This is the analog output for S-Video chrominance. Terminate this DAC in 37.5 Ω. A 75-Ω resistor to analog ground provides half the termination (the other half is in the monitor). Place this resistor close to the CL-GD1052/GD1053. An LC filter (consisting of a 330-pF input capacitor, a 2.2-µH inductor, and 220-pF output capacitor) connects this DAC to the respective connector pin. The capacitors are returned to analog ground.
CVID37	A	**Composite Video 37.5-Ω Output:** This is the analog output for composite video. Terminate this DAC in 37.5 Ω. A 75-Ω resistor to analog ground provides half the termination (the other half is in the monitor). Place this resistor close to the CL-GD1052/GD1053. An LC filter (consisting of a 330-pF input capacitor, a 2.2-µH inductor, and 220-pF output capacitor) connects this DAC to the respective connector pin. The capacitors are returned to analog ground.

3.5 Power and Ground Pins

Name	Type	Description
VDDD [2:1]	PWR	**Digital Power:** These two pins supply power to the digital I/O and digital logic. These pins must be connected to the digital power plane island and each should be bypassed with a 0.1-µF capacitor placed as close to the pin as possible. Each capacitor is returned to digital ground.
VDDA1	PWR	**Bandgap Reference Power:** This pin supplies power to the bandgap reference generator. This pin must be connected to the analog power plane island and bypassed with a 0.1-µF capacitor placed as close to the pin as possible. This capacitor is returned to analog ground.
VDDA [2:3]	PWR	**DAC Power:** These two pins supply power to the DACs. These pins must be connected to the analog power plane island and should be bypassed with a 0.1-µF capacitor placed close to the pins. These two pins can share one bypass capacitor. This capacitor is returned to analog ground.
GNDD [2:1]	GND	**Digital Ground:** These pins supply ground reference to the digital I/O and digital logic. These pins must be connected to digital ground.
GNDA	GND	**Analog Ground:** This pin supplies ground reference to the DAC. This pin must be connected to analog ground.
GNDB	GND	**Bandgap Reference Ground:** This pin supplies ground reference to the bandgap reference circuits. This pin must be connected to analog ground.

4. PRODUCT DESCRIPTION

4.1 Features

The CL-GD1052/GD1053 accepts digital video and produces analog NTSC or PAL television outputs. The input video is compliant with CCIR656. There are three analog outputs: S-Video luminance, S-Video chrominance, and composite video. All three outputs are designed for a 37.5-Ω load.

The CL-GD1052/GD1053 accepts video data from a VGA controller or MPEG decoder. As the CL-GD1052/GD1053 does not support a retiming frame buffer, the input video must be timed appropriately. The input video data can be in formats from 320 × 200 up to 800 × 600. The video is scaled for NTSC or PAL and output as S-Video or composite video. An adaptive flicker-filter processor selects a filter appropriate for the local two-dimensional picture content.

The operating parameters of the CL-GD1052/GD1053 are programmed by a two-wire serial interface bus. Examples of programmable parameters are the TV-output format and closed-caption data.

The CL-GD1052/GD1053 requires a 27-MHz frequency reference and a 2× VGA pixel clock. Optionally, a 14.318-MHz oscillator can be applied to support VGA BIOS parameters. Color burst timing is generated on-chip from the 27-MHz reference.

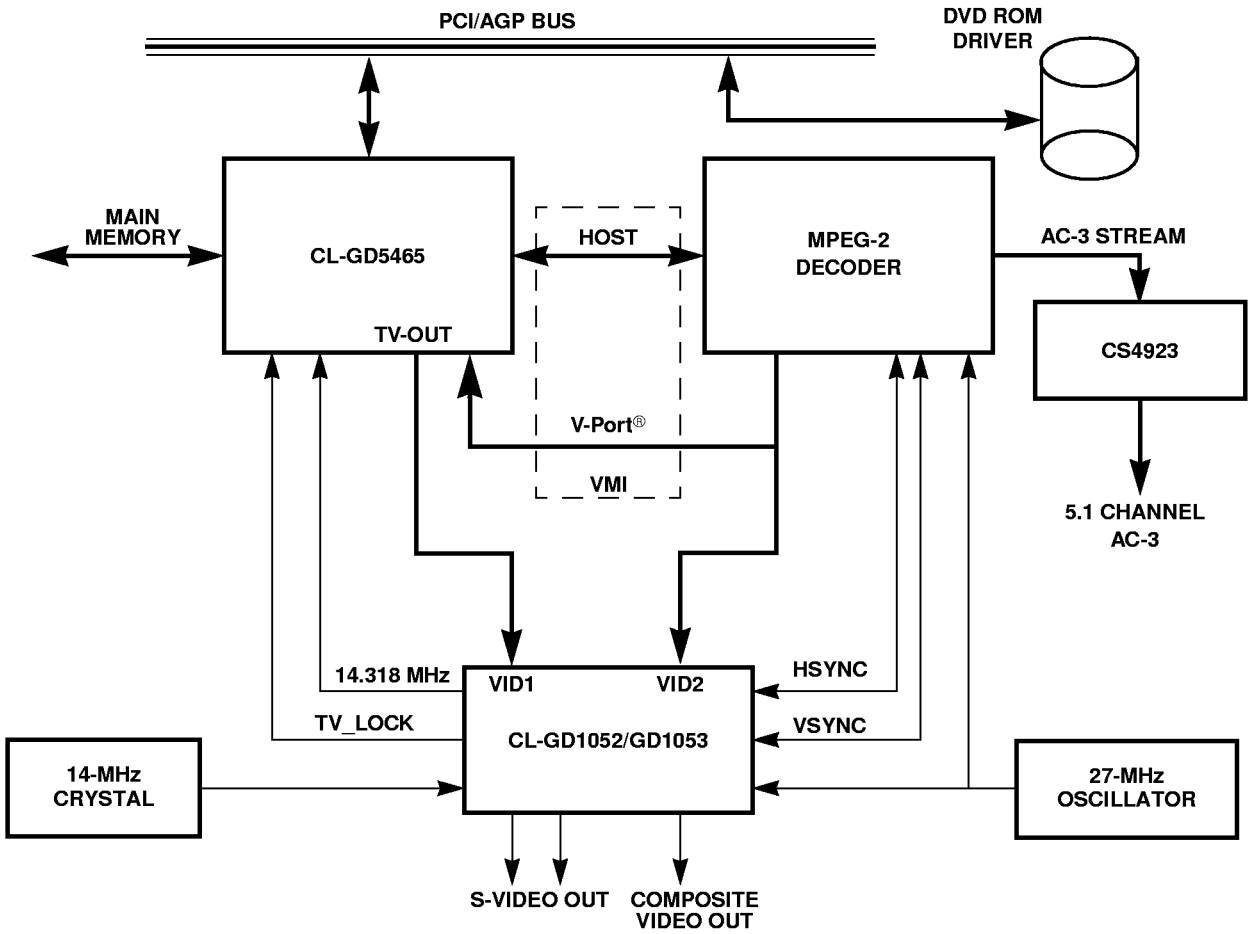


Figure 4-1. System Overview

4.1.1 Master and Slave Operation

The CL-GD1052/GD1053 can be configured for either Master or Slave Timing mode. In Master Timing mode, the CL-GD1052/GD1053 generates the horizontal and vertical synchronization signals and expects incoming video is available when required. In addition to HSYNC and VSYNC, the CL-GD1052/GD1053 also generates FIELD. In Slave Timing mode and only when the CCIR601 input is applied, the CL-GD1052/GD1053 accepts HSYNC and VSYNC as inputs.

4.1.2 Macrovision® Copy Protection

The CL-GD1053 implements Macrovision copy protection Revision 7. A video signal with copy protection enabled is viewable on TV, but cannot be used to make a video tape. A license from Macrovision is required to use this scheme. Cirrus Logic cannot accept sample requests or orders for the CL-GD1053 without evidence of a license. In addition, the detailed programming information for the Macrovision logic is available separately.

Macrovision specifies that the following 'Product Notice' appear in printed collateral with products using this device.

"This device is protected by U.S. patent numbers 4,631,603, 4,577,216, and 4,819,098, and other intellectual property rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision. Reverse engineering or disassembly is prohibited."

4.1.3 Closed-Caption

The CL-GD1052/GD1053 enables closed-caption for NTSC only (both Master and Slave Timing modes). Closed-caption data is inserted into lines 21 and 284 of the composite video signal. The host specifies two data bytes for each scanline.

4.1.4 Power Down Mode

The CL-GD1052/GD1053 can be powered down by programming a single bit in a register or by driving a pin. In Power Down mode, the CL-GD1052/GD1053 dissipates no more than 100 µW. Register contents are maintained when the device is powered down, so that normal operation can be restored quickly and easily.

4.1.5 Color Bar Generator

The CL-GD1052/GD1053 has a built-in color bar generator. The test pattern generated is 75% amplitude and 100% saturation EIA colors for NTSC.

4.1.6 CCIR656 Compliance

When the CL-GD1052/GD1053 is configured for Slave Timing mode, the input video is compliant with CCIR656, including synchronization control words. The CL-GD1052/GD1053 does not check or use the P bits in the control word. CCIR601 timing is also supported.

4.1.7 Interrupts

The CL-GD1052/GD1053 can generate interrupt requests for closed-caption lines (lines 21 and 284) and at the beginning of each video field. Each interrupt condition has an individual Enable bit and an individual Clear bit for maximum programming flexibility. This feature is operational if the VGA clock is not used.

4.1.8 Video Window

The CL-GD1052/GD1053 has two video input ports and can be programmed to display video from either port. In addition, the video streams on the two ports can be mixed so that one stream appears within a window in the other stream (VID2 on top of VID1). The size and position of the window are programmable.

4.2 Functional Description

This section describes the functionality and is not intended to describe actual implementation.

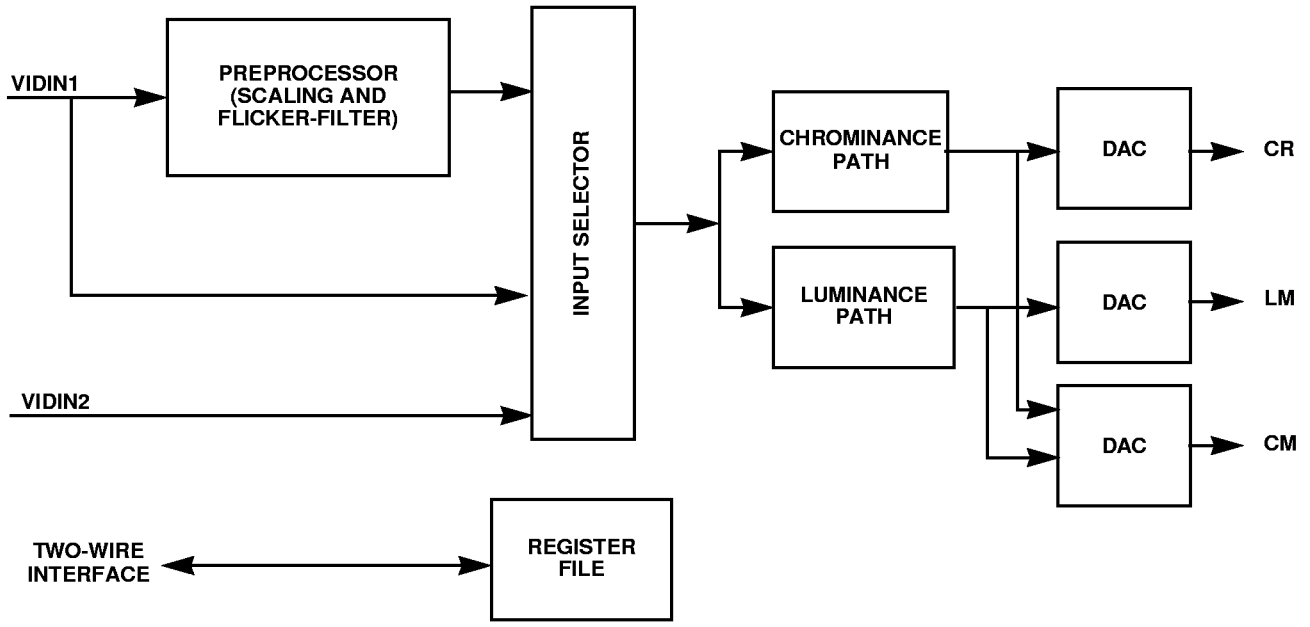


Figure 4-2. Functional Block Diagram

4.2.1 Preprocessor

The preprocessor converts non-interlaced video to interlaced, NTSC, or PAL. This occurs in two stages: the scaler and the flicker filter. If interlaced NTSC or PAL video is supplied, the preprocessor is bypassed.

The scaler transforms the video from VGA resolution (for example 640 × 480) to NTSC or PAL. The luminance data is treated separately from chrominance data.

4.2.2 Adaptive Flicker Filter

The adaptive flicker filter automatically selects one of four filters, depending on the local two-dimensional picture content. Some picture content (for example, thin horizontal lines) can take advantage of a lower cut-off frequency filter. Text, however, does not gain much from heavy filtering; it retains the high-frequency components for better resolution.

4.2.3 Input Selection

Depending on how the CL-GD1052/GD1053 is programmed, the input selector selects either interlaced video from VIDIN1, interlaced video from VIDIN2, or scaled video from the preprocessor. If a video window is programmed, the selector can select from both video streams within a single scanline.

If necessary, the video data is converted from YCbCr to YUV, then split into separate chrominance and luminance paths.

4.2.4 Chrominance Path

In the chrominance path, the video data enters a low-pass filter and then an interpolation unit that converts it to YUV 4:4:4. The chroma modulator multiplies U and V times the sine and cosine, respectively, of the subcarrier clock and adds the products together. The hue phase is adjustable in steps of approximately 0.35 degrees.

The color burst is inserted appropriately for NTSC or PAL. In PAL, the burst alternates at each line, so the phase changes from line to line. The chrominance data enters through an output interpolation filter and then a chrominance DAC. In parallel, it is summed with the luminance data and sent to the composite DAC.

4.2.5 Luminance Path

The luminance data enters through a programmable delay that matches the group delay through the chrominance path. The delays of the luminance and chrominance paths become the same. The sync signal is inserted and the luminance data enters the output interpolation filter. The luminance data enters the luminance DAC and is also combined with the chrominance data for the composite DAC.

4.2.6 DACs

All three DACs are designed to 75-Ω doubly-terminated loads (37.5-Ω impedance). The CL-GD1052/GD1053 includes a current reference based on an internal bandgap reference. Each DAC has a programmable enable and a programmable power-down control.

NOTE: If one or more DAC output is not required, it is highly recommended to power down those DACs to reduce power consumption.

4.2.7 Two-Wire Serial Interface

The CL-GD1052/GD1053 provides a two-wire serial interface for accessing the internal control and status registers. This interface is always a slave and does not operate in master mode.

4.2.8 Register File

The CL-GD1052/GD1053 includes approximately 70 bytes of control and status information, accessible by the two-wire serial interface. The registers are described in detail in Chapter 9.

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Ambient temperature under bias . . . . . 0°C to 70°C
Storage temperature . . . . . –65°C to 150°C
Voltage on any digital signal pin . . . . . GND – 0.5 V to V_{DD} + 0.5 V
Voltage on 5-V tolerant digital signal pin . . . . . GND – 0.5 V to 5.5 V
Power supply voltage . . . . . 5.0 V
Injection current (latch-up testing) . . . . . 100 mA

CAUTION: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

5.2 DC Specifications

(V_{DD} = 3.3 V ± 0.15 V, T_A = 0°C to 70°C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
V_{DD} (+3.3 V)	Power supply voltage	3.15	3.45	V	Normal operation	
V_{IL}	Input low voltage	–0.5	0.3 V_{DD}	V	(non 5-V tolerant)	
V_{IH}	Input high voltage	0.7 V_{DD}	1.05 V_{DD}	V	(non 5-V tolerant)	
V_{IH5T}	Input high voltage	0.7 V_{DD}	5.5 V	V	(5-V tolerant)	1
V_{OL}	Output low voltage	–	0.1 V_{DD}	V	I_{OL} = 3.2 mA	2
V_{OH}	Output high voltage	0.7 V_{DD}	–	V	I_{OH} = –200 µA	3
I_{DD} (+3.3 V)	Supply current	–	320	mA	V_{DD} nominal	
I_{OZ}	Input leakage	–10	10	µA	$0 < V_{IN} < V_{CC}$	
C_{IN}	Input capacitance	–	10	pF		4
C_{OUT}	Output capacitance	–	10	pF		4

NOTES:

1) VID[7:0] and CLK27IN are 5-V tolerant, all other digital pins are 3.3-V tolerant.
2) I_{OL} is specified for a standard buffer.
3) I_{OH} is specified for a standard buffer.
4) This is not 100% tested, but is periodically sampled.

5.3 DAC Characteristics

(V_{CC} = 3.3 V ± 0.15 V, T_A = 0°C to 70°C, unless otherwise specified)

Parameter	MIN	TYP	MAX	Units	Note
Resolution	9	9	9	Bits	
Full-scale output voltage	1.23	1.30	1.37	V	[a]
Full-scale output current	31.2	34.7	38.1	mA	[a]
DAC output delay	–	4	12	ns	
DAC rise/fall time	–	2.5	5.0	ns	
DAC output skew	–	0.2	1.0	ns	
Differential non-linearity	–	0.5	0.75	LSB	
Integral non-linearity	–	0.75	1.0	LSB	

[a] Load is 37.5 Ω

5.4 AC Characteristics

5.4.1 List of Timings

5.4.2 I/O Timing

Symbol	Parameter	MIN	MAX	Units
t_1	DOTCLKX2 period	tbd[a]	–	ns
t_1	CLK27IN period	37.04	37.04	ns
t_2	High period (either clock input)	40	60	% t_1
t_3	CLK27IN to HSYNC, VSYNC, FIELD delay (Master Timing mode)	tbd	30	ns
t_3	CLK27IN to VIDIN1 valid delay (IN_SEL = 11)	tbd	30	ns
t_4	Data to DCLKX2 setup	tbd	–	ns
t_5	Data to DCLKX2 hold	tbd	–	ns
t_4	Data to CLK27IN setup	6	–	ns
t_5	Data to CLK27IN hold	0	–	ns

[a] 'tbd' indicates to be determined.

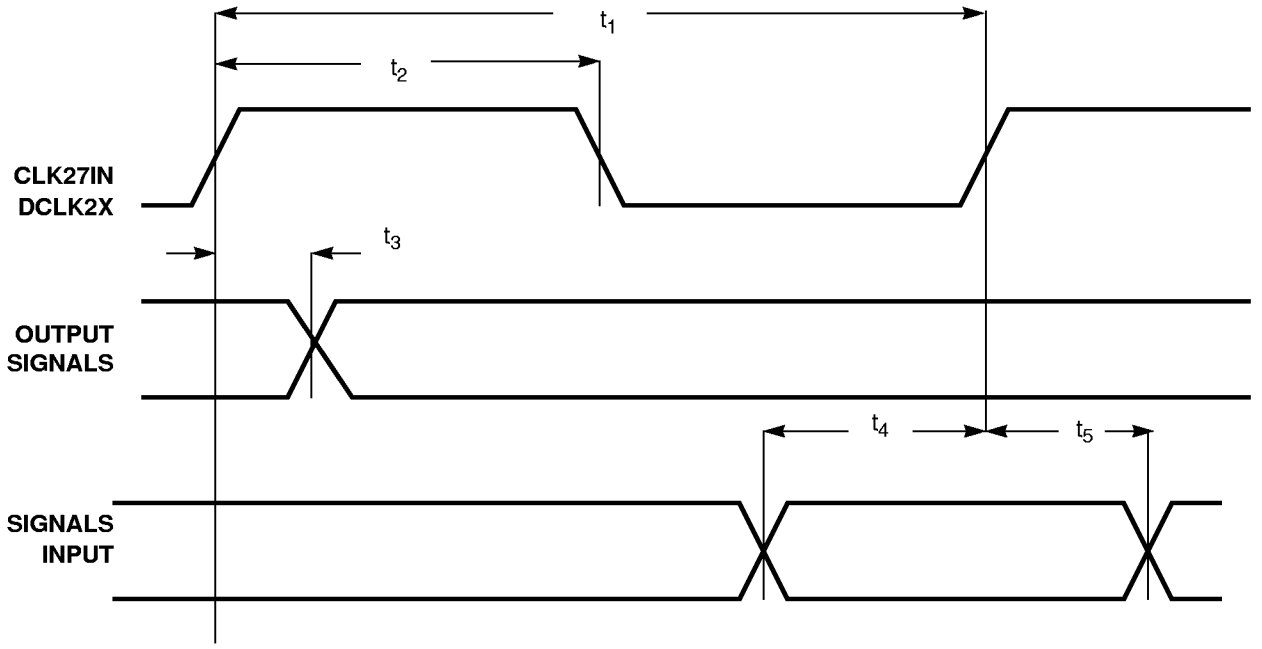


Figure 5-1. I/O Timing

5.4.3 Serial Interface Timing: Clock

Symbol	Parameter	MIN	MAX	Units
t_{SCL}	SCL clock period	100	1000	kHz
t_R[a]	Rise time for both SDA and SCL	20 + 0.1 Cb[b]	300	ns
t_F[a]	Fall time for both SDA and SCL	20 + 0.1 Cb	300	ns
t_{LOW}	Low period of the SCL clock	1.3	–	µs
t_{HIGH}	High period of the SCL clock	0.6	–	µs

[a] This is not 100% tested, but is periodically sampled.
[b] Cb is bus capacitance in pF.

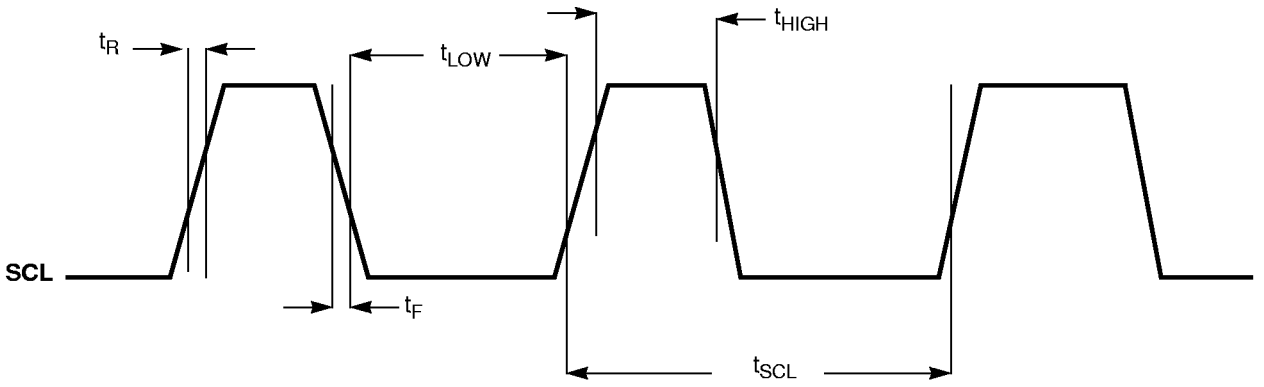
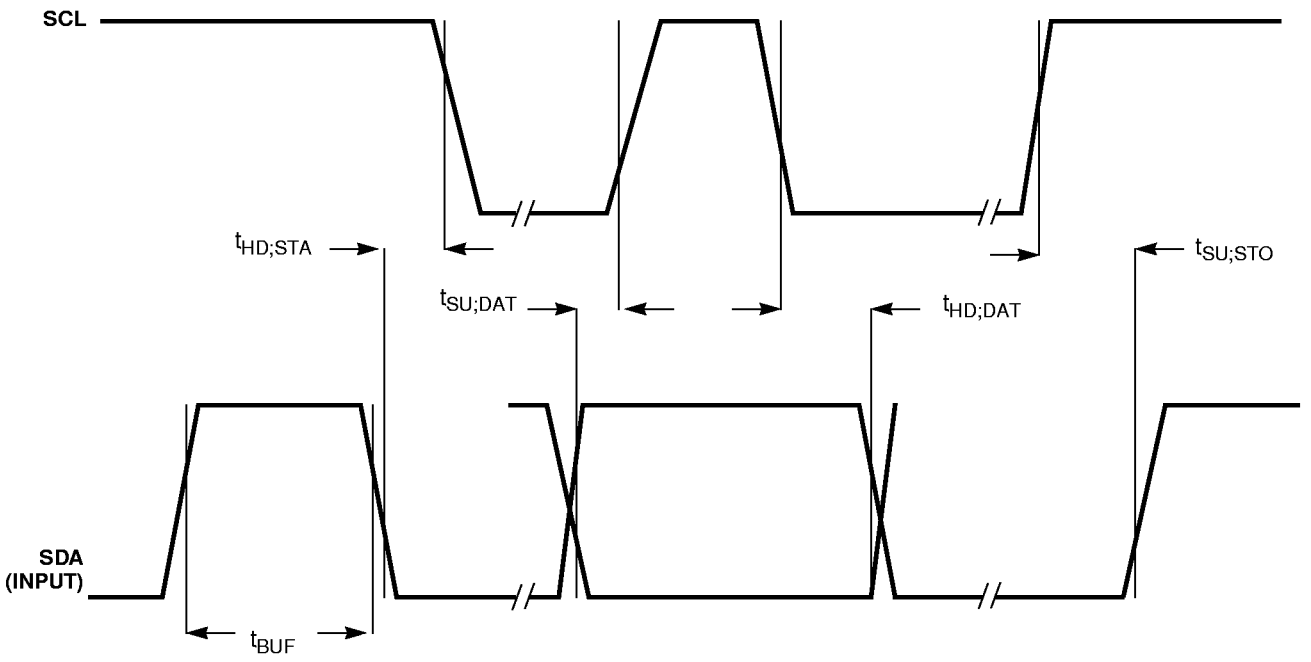


Figure 5-2. Serial Interface Timing: Clock

5.4.4 Serial Interface Timing: Receiver

Symbol	Parameter	MIN	MAX	Units
t_{BUF}	Bus free time between a STOP and START condition	1.3	–	µs
$t_{HD;STA}$	Hold time (repeated) START condition	1.3	0.6	µs
$t_{SU;STO}$	Set-up time for a STOP condition	0.6	–	µs
$t_{SU;DAT}$	Data set-up time	100	–	ns
$t_{HD;DAT}$	Data hold time	0	0.9	ns



NOTE: STOP condition: SDA rises with SCL high
START condition: SDA falls with SCL high.

Figure 5-3. Serial Interface Timing: Receiver

5.4.5 Serial Interface Timing: Transmitter

Symbol	Parameter	MIN	MAX	Units
$t_{PH;DAT}$	Propagation delay; SCL to SDA	0	3.4	µs

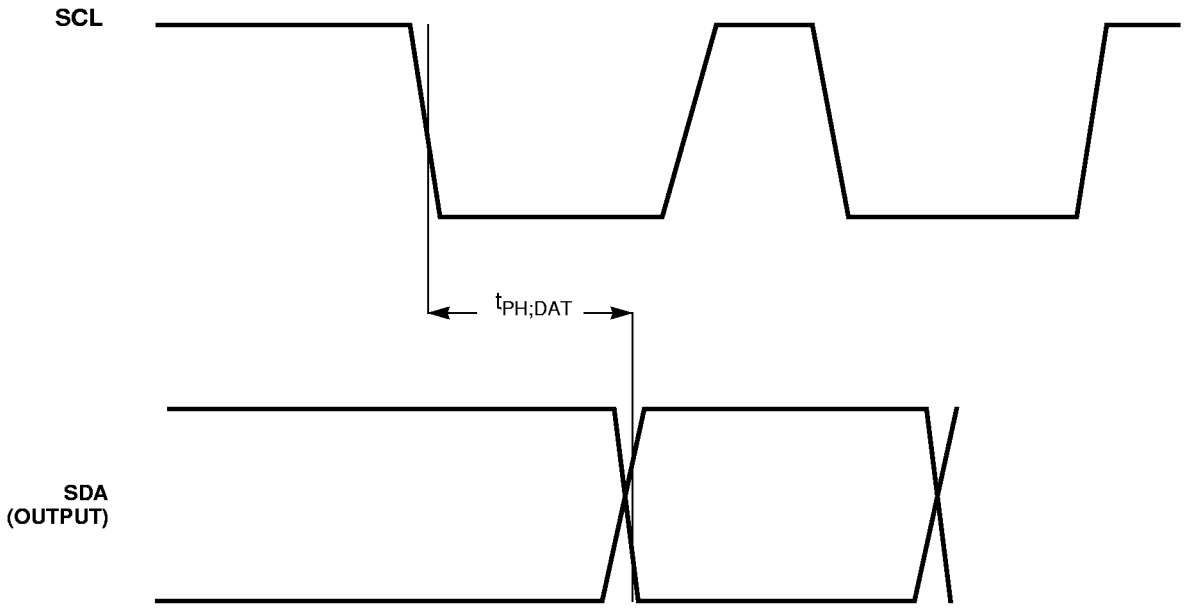


Figure 5-4. Serial Interface Timing: Transmitter

6. BOARD DESIGN NOTES

This section discusses board design and provides layout recommendations.

6.1 Component Placement

Placement of the CL-GD1052/GD1053 is not critical, although it should be close to the video connectors and close to the VGA controller. This dimension is not critical since the bus is only eight bits wide and operates at a relatively low frequency.

6.2 Power and Ground

Problems with video board design can usually be traced to improper power and ground distribution.

NOTE: Customers designing boards should pay close attention to the following recommendations.

6.2.1 Power Conditioning and Distribution

When the CL-GD1052/GD1053 is placed on a board with a CL-GD546X, there is already an inner layer dedicated to power distribution. Generally, part of the power plane is dedicated to 5.0 V and part to 3.3 V. The CL-GD1052/GD1053 is powered by 3.3 V, and the 3.3-V area should encompass it. There should be two islands cut in the power plane to completely isolate digital power and analog power for the CL-GD1052/GD1053 from the rest of the plane. Power is brought into each isolated area through ferrite beads. Each power pin is bypassed with a 0.1-µF capacitor placed as close to the pin as possible.

These isolated areas are shown in Figure 6-1. It should be noted that this diagram is an artistic rendition and may not reflect the actual cuts in any real design.

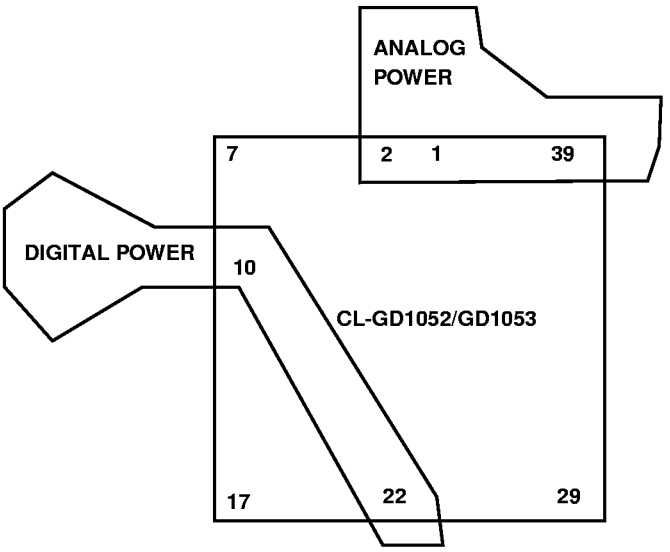


Figure 6-1. Power Isolation

6.2.2 Ground Isolation

The ground plane should have a cut that isolates the analog ground from the digital ground. The cut should come under the device between pins 3 and 4, and exit between pins 38 and 37. This places all the pins that should return to (or are referenced to) analog ground on one side, and all the digital pins on the other side.

The analog ground must extend to the video connectors. The grounds on the video connectors must connect to the analog ground. The filters on the video signals must return to the analog ground. The analog ground must connect to the digital ground at a single point. Use a ferrite bead at this junction; however, it can be replaced with a short circuit.

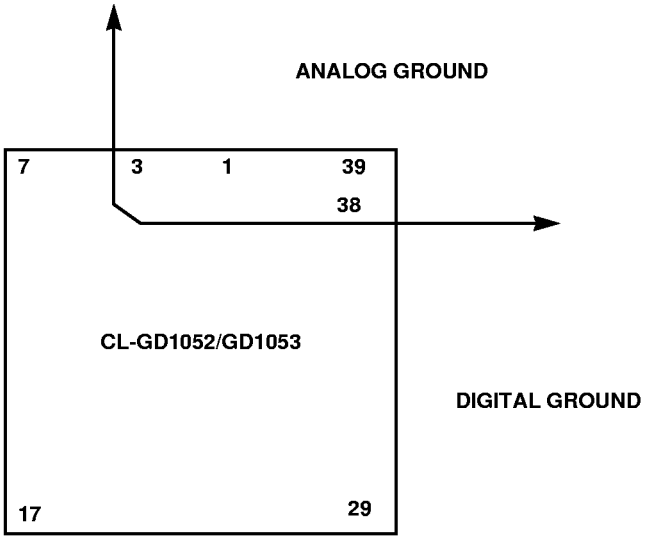


Figure 6-2. Ground Plane Cuts

6.2.3 Design Review Service

There is a certain amount of art (as opposed to science) involved in the placement of the power and ground plane cuts. Some experimentation may be required to obtain satisfactory results. The Cirrus Logic applications team is competent and eager to review customer schematics and board designs before they are committed to manufacturing.

6.3 Reference Design

There is a reference design that uses the CL-GD5465 (Laguna 3D AGP) and the CL-GD1052/GD1053 on a single PCI adapter card. Cirrus Logic can provide a complete design kit, including schematic diagrams, Gerber files, and a bill of materials.

6.4 CL-GD5465 Connections

Table 6-1 defines the connections required between the CL-GD5465 and the CL-GD1052/GD1053.

Table 6-1. CL-GD5465 Connections

CL-GD5465	CL-GD1052/GD1053	Description	Direction
Pull-down resistor on RD[3]	–	TV-Out attached	–
Optional pull-down resistor on RD[3]	–	Install for PAL	–
EV [7:0]	VIDI [7:0]	Encoded data to CL-GD1052	CL-GD1052/GD1053 input
EVCLK	DCLK2X	Encoder video clock	CL-GD1052/GD1053 input
EVSYNC	TV_LOCK	Encoder	CL-GD1052/GD1053 output
XTAL0	VGA_CLK	Reference	CL-GD1052/GD1053 output
SDA2	SDA	Serial interface data	Bidirectional
SCL2	SCL	Serial interface clock	CL-GD1052/GD1053 input

7. VIDEO FORMATS

This section provides details on the specific video formats supported by the device.

7.1 Typical VGA Input Formats

Input Scan Format	Format Mode	Input Format (Active Pixels)	DOTCLKX2	Total Pixels for VGA	VGA PLL	Scaled Output
Interlaced NTSC	0	720 × 480/2	27.000	858 × 480/2	–	720 × 480/2
Interlaced PAL	1	720 × 576/2	27.000	864 × 576/2	–	720 × 576/2
Non-interlaced NTSC	2	320 × 400	24.924	396 × 525	12/13	580 × 400/2
	3	360 × 400	27.692	440 × 525	40/39	580 × 400/2
	4	400 × 600	41.236	468 × 735	84/55	640 × 428/2
	5	512 × 768	64.800	572 × 945	12/5	640 × 426/2
	6	640 × 350	44.308	704 × 525	64/39	508 × 350/2
	7	640 × 400	44.308	704 × 525	64/39	580 × 400/2
	8	640 × 480	44.308	704 × 525	64/39	692 × 480/2
	9	640 × 480	54.982	728 × 630	112/55	580 × 400/2
	10	720 × 400	49.090	780 × 525	20/11	580 × 400/2
	11	800 × 600	77.538	880 × 735	112/39	640 × 428/2
Non-interlaced PAL	12	320 × 400	24.750	396 × 625	11/12	502 × 400/2
	13	360 × 400	27.500	440 × 625	55/54	502 × 400/2
	14	400 × 600	35.100	468 × 750	13/10	588 × 500/2
	15	512 × 768	57.600	576 × 1000	32/15	580 × 480/2
	16	640 × 350	44.000	704 × 625	44/27	440 × 350/2
	17	640 × 400	44.000	704 × 625	44/27	502 × 400/2
	18	640 × 480	44.000	704 × 625	44/27	580 × 480/2
	19	720 × 400	49.000	784 × 625	49/27	502 × 400/2
	20	800 × 600	66.000	880 × 750	22/9	588 × 500/2

7.2 Typical Frame Formats

Format	DOTCLKX2 (MHz)	Format Mode	SAV (Start Video)	Active Video	EAV (End Video)	Blanking	Total [a]	Blanking Lines
NTSC Interlaced	27.000	0	4	1440	4	268	1716	22 odd, 23 even
PAL Interlaced	27.000	1	4	1440	4	280	1728	24 odd, 25 even
NTSC 320 × 400	24.924	2	4	640	4	144	792	125
NTSC 360 × 400	27.692	3	4	720	4	152	880	125
NTSC 400 × 600	41.236	4	4	800	4	128	936	135
NTSC 512 × 768	64.800	5	4	1024	4	112	1144	177
NTSC 640 × 350	44.308	6	4	1280	4	120	1408	175
NTSC 640 × 400	44.308	7	4	1280	4	120	1408	125
NTSC 640 × 480	44.308	8	4	1280	4	120	1408	45
NTSC 640 × 480	54.982	9	4	1280	4	168	1456	150
NTSC 720 × 400	49.090	10	4	1440	4	112	1560	125
NTSC 800 × 600	77.538	11	4	1600	4	152	1760	135
PAL 320 × 400	24.750	12	4	640	4	144	792	225
PAL 360 × 400	27.500	13	4	720	4	152	880	225
PAL 400 × 600	35.100	14	4	800	4	128	936	150
PAL 512 × 768	57.600	15	4	1024	4	120	1152	232
PAL 640 × 350	44.000	16	4	1280	4	120	1408	275
PAL 640 × 400	44.000	17	4	1280	4	120	1408	225
PAL 640 × 480	44.000	18	4	1280	4	120	1408	145
PAL 720 × 400	49.000	19	4	1440	4	120	1568	225
PAL 800 × 600	66.000	20	4	1600	4	152	1760	150

[a] Total = SAV + Active Video + EAV + Blanking

7.3 TV Standards

Standard	Device Supports	BIOS Supports	TV_FORMAT Code	Note
NTSC-M	Yes	Yes	000	CCIR601 timing
NTSC	Yes	–	001	RS170A timing
NTSC-J	Yes	–	001	–
PAL-B, G	Yes	–	010	–
PAL-H	Yes	–	010	–
PAL-I	Yes	–	010	–
PAL-N (Argentina)	Yes	–	100	–
PAL-N (non Argentina)	Yes	–	101	–
PAL-D	Yes	–	010	–
PAL-M	Yes	–	011	–
NTSC-N	No	No	n/a	–
SECAM	No	No	n/a	–

7.4 CCIR656 Input Format

Input data is transmitted in the CCIR656 order. Input data is clocked on the positive edge of the respective clock.

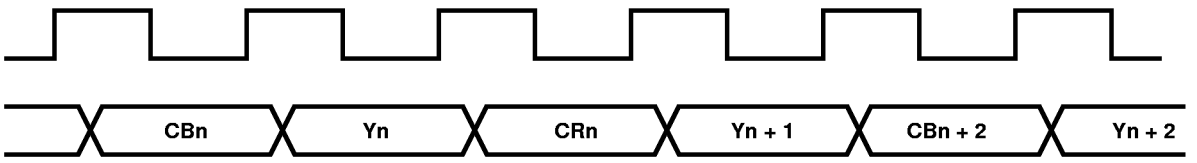


Figure 7-1. CCIR656 Input Format

8. TWO-WIRE SERIAL INTERFACE

The CL-GD1052/GD1053 register file is accessed by two-wire serial interface. This two-wire serial connection is similar to that defined by Philips Semiconductor®. For more information on the I²C bus, visit the Philips Semiconductor web site at:

http://www-us2.semiconductors.philips.com/i2c/

The CL-GD1052/GD1053 is always a slave and is expected to operate significantly faster than 400 kbit/sec. Refer to Chapter 5 for limit determination.

8.1 Two-Wire Serial Interface Transactions

The CL-GD1052/GD1053 is designed to execute two transactions. No other transactions should be programmed.

8.1.1 Write Register Byte

The write register byte transaction writes one byte of the register file. The packet consists of three bytes. The first byte is the device address with the direction bit set to '0' to indicate a write. The second byte is the register address (from 0 to 255). The third byte is the data to be written to the defined register. The first bit within each byte is the most-significant bit.

The device address is forced to '00h' at reset. The address can be reprogrammed at any time by writing a new value to register '15h'. Subsequent accesses use this address until the device is reset.

8.1.2 Read Register Byte

This transaction reads one byte of the register file. The master transmits two bytes and the CL-GD1052/GD1053 responds with one byte. The first byte is the device address with the direction bit set to '1' to indicate a read. The second byte is the register address (from 0 to 255). The CL-GD1052/GD1053 then responds with a single byte of data from the specified register.

8.2 Two-Wire Serial Interface Bus Design

In a design based on the CL-GD5465, the two-wire serial interface bus uses the second two-wire serial interface of the CL-GD5465. This bus should be routed directly between the two devices. The placement of the pull-up resistors is not critical, although it is important that the resistors do not form stubs.

9. REGISTER SUMMARY

The CL-GD1052/GD1053 has a number of registers that control the device and return status to the host. These registers are accessible through the two-wire serial interface. The following sections describe each register to the bit level. The registers are grouped into several categories and listed in hex address order. Programming values for typical modes is provided in Section 9.13 on page 64.

Table 9-1. Register Quick Reference

Address	Register Name	Page
00h	Global Register 0	37
01h	Global Register 1	37
02h	Global Register 2	38
03h	Global Register 3	39
04h	Global Register 4	40
05h	Global Register 5	41
06h	Background Color	41
07h	VGA Horizontal Total LSB	42
08h	TV_LOCK Horizontal Delay	42
09h	TV_LOCK Vertical Delay	43
0Ah	VGA Horizontal Total MSB	44
0Bh	Horizontal Downscaler Output Width	45
0Ch	Horizontal Downscaling Factor	45
0Dh	Horizontal Upscaling Factor	46
0Eh	Horizontal Origin	47
0Fh	Vertical Origin	47
10h	Horizontal Size	47
11h	Vertical Size	48
12h	Filter Miscellaneous	49
13h	Chrominance Amplitude Coefficient	50
14h	Luminance Amplitude Coefficient	50
15h	Serial Interface Address	51
16h	Color Burst Amplitude	52
17h	Color Carrier Synthesis Byte 0	52

Table 9-1. Register Quick Reference *(cont.)*

Address	Register Name	Page
18h	Color Carrier Synthesis Byte 1	52
19h	Color Carrier Synthesis Byte 2	53
1Ah	Color Carrier Synthesis Byte 3	53
1Bh	Hue Phase Shift Byte 0	53
1Ch	Hue Phase Shift Byte 1	54
1Dh	Closed Caption Control	54
1Eh	Closed Caption Data Line 21 Byte 1	55
1Fh	Closed Caption Data Line 21 Byte 2	55
20h	Closed Caption Data Line 284 Byte 1	55
21h	Closed Caption Data Line 284 Byte 2	56
22h	Window Horizontal Start	57
23h	Window Vertical Start	57
24h	Window Horizontal Size	57
25h	Window Vertical Size	58
3Ch–3Eh	Miscellaneous Window 3–1	58
40h	Interrupt Enable	60
41h	Interrupt Clear	60
42h	Device ID	61
43h	Status	61
44h	Revision Code	62
45h	RAM Test Control	62
46h	Test Control Byte 0	62
47h	Test Control Byte 1	63

9.1 Global Registers

9.1.1 Global Control Register 0

Register Description: **Global Control Register 0**							*Intel Hex Address:* **00h**
Access: **Read/Write**							
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
TV_FORMAT			Reserved	CC1R656_ON	PROG	IN_MODE	CBCR_UV

Bit	Power-On Value	Description
7:5	000	**Select TV Display Format** 000: NTSC-M (CCIR601) 001: NTSC-M (RS-170A), NTSC-J 010: PAL-B, G, H, I, D 011: PAL-M 100: PAL-N (Argentina) 101: PAL-N (non Argentina) 110: Reserved 111: Reserved
4		**Reserved**
3	0	**Input is CCIR656** 0: Off 1: On
2	0	**Progressive Scanning Enable** 0: Interlaced 1: Progressive
1	0	**Input Select** 0: Solid Background 1: Normal
0	1	**Enable YCbCR-to-YUV Conversion** 0: Disable (YUV input) 1: Enable (YCbCR input)

9.1.2 Global Control Register 1

Register Description: **Global Control Register One** *Intel Hex Address:* **01h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
CB_H_SEL	LUM_DEL	CH_BW	LPF_ON	RELOPOL	PEDESTAL	CBAR	CBCRSEL

Bit	Power-On Value	Description
7	0	**CB/HSYNC Output** 0: HSYNC 1: Composite blank
6	0	**Luminance-to-Chrominance Delay** 0: No delay 1: One13.5-MHz cycle
5	0	**Chrominance Low-Pass Filter Bandwidth** 0: 650 kHz 1: 1.3 MHz
4	0	**Enable Chrominance Low-Pass Filter** 0: Disable 1: Enable
3	0	**Polarity of Field Zero** 0: Odd field = 0 1: Odd field =1
2	1	**Pedestal Offset** 0: 0 1: 7.5 IRE
1	0	**Enable Internal Color Bar Generator** 0: Disable 1: Enable
0	0	**CbCr Select** 0: Chrominance not delayed 1: Chrominance delayed one clock cycle

9.1.3 Global Control Register 2

Register Description: **Global Control Register Two** *Intel Hex Address:* **02h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
VGA_CLK		CLIP_OFF	S_PDN	Y_BW	SYNC_DLY	XTAL	BU_DIS

Bit	Power-On Value	Description
7:6	00	**VGA_CLK Frequency Select** 00: 14.31818 MHz (XTAL1/XTAL2) 01: 27 MHz (CLK27IN) 10: 13.5 MHz (CLK27IN divided by two) 11: Reserved
5	0	**Disable Clipping** 0: Luminance and chrominance clipping on 1: Luminance and chrominance clipping off
4	0	**Software Power Down** 0: Software power up 1: Software power down
3	0	**Luminance Bandwidth** 0: 4.2 MHz 1: 6.0 MHz
2	0	**Delay HSYNC/CB and VSYNC** 0: No delay 1: One 27-MHz clock cycle
1	0	**Crystal Oscillator Subcarrier Adjust Enable** 0: Disable 1: Enable
0	0	**Disable Chrominance Burst** 0: Enable 1: DIsable

9.1.4 Global Control Register 3

Register Description: **Global Control Register Three** *Intel Hex Address:* **03h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
PREPROC_BP	VID_SEL		MASTER	SLAVE_SEL	TV_LOCK_OEN	DAC_DET_EN	

Bit	Power-On Value	Description
7	0	**Bypass Preprocessor Module** 0: No bypass 1: Bypass
6:5	00	**Selects Input Port (IN_MODE = 1)** 00: VIDIN1 only 01: VIDIN2 only 10: VIDIN1 and VIDIN2 multiplexed 11: VIDIN2 input, VIDIN1 output
4	0	**Master Mode** 0: Slave mode 1: Master mode
3	1	**Input Port (Slave modes) (IN_MODE = 1)** 0: VIDIN_1 port only 1: VIDIN_2 port only
2	0	**Enable TV_LOCK Output** 0: Tristate 1: Enable
1:0	00	**DAC Autodetect for TV Connection** 00: No autodetect 01: Autodetect composite DAC only 10: Autodetect S-Video DACs only 11: Autodetect all DACs

9.1.5 Global Control Register 4

Register Description: **Global Control Register Four** *Intel Hex Address:* **04h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved		COMDAC37_PD	SVIDLUM_PD	SVIDCHR_PD	ENC_37	ENS_L	ENS_C

Bit	Power-On Value	Description
7:6		**Reserved**
5	0	**Power-Down Composite DAC** 0: Power up 1: Power down
4	0	**Power-Down Luminance DAC** 0: Power up 1: Power down
3	0	**Power-Down Chrominance DAC** 0: Power up 1: Power down
2	1	**Enable Composite DAC** 0: Tristate 1: Enable
1	1	**Enable Luminance DAC** 0: Tristate 1: Enable
0	1	**Enable Chrominance DAC** 0: Tristate 1: Enable

9.1.6 Global Control Register 5

Register Description: **Global Control Register Five** *Intel Hex Address:* **05h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved			MASTER	Reserved		CH_XS	CH_DM

Bit	Power-On Value	Description
7:5	0	**Reserved**
4	0	**Master Mode** 0: Normal operation 1: FIELD, HSYNC, VSYNC pins tristate in Master mode
3:2	0	**Reserved**
1	0	**Replicate Chrominance in Horizontal Downscaler** 0: Replicate chrominance 1: Filter chrominance
0	0	**Replicate Chrominance in Video Demultiplexor** 0: Replicate chrominance 1: Filter chrominance

9.2 Front End Register

9.2.1 Background Color Register

Register Description: **Background Color Register** *Intel Hex Address:* **06h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
BG							

Bit	Power-On Value	Description
7:0	0000 0011 (Blue)	**Background color** (7:5 = Red, 4:2 = Green, 1:0 = Blue)

9.3 VGA Synchronization Registers

9.3.1 VGA Horizontal LSB

Register Description: **VGA Horizontal Total LSB** *Intel Hex Address:* **07h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
TV_HTOTAL_L							

NOTE: TV_HTOTAL_L and TV_HTOTAL_M specify the total number of VGA pixel clocks divided by 4 (mod4(pixel_clocks)). This value is used with TV_ADJ_V by the TV_LOCK generator for counting VGA line times. TV-Out solutions are limited to those where the total pixel clocks per line are a multiple of four.

Bit	Power-On Value	Description
7:0	0000 0000	**Total VGA pixels per input line**: 8 LSBs

9.3.2 TV_LOCK Horizontal Delay LSB

Register Description: **TV_LOCK Horizontal Delay LSB** *Intel Hex Address:* **07h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
TV_ADJ_H_L							

NOTE: TV_ADJ_H specifies the horizontal start position of the TV_LOCK signal with respect to TV_HSYNC. It is measured in VGA pixel clocks. The actual register value divided by 4 defines the delay, with a resolution of four pixel clocks.

Bit	Power-On Value	Description
7:0	0000 0000	**Horizontal Delay of TV_LOCK**: 8 LSBs

9.3.3 TV_LOCK Vertical Delay

Register Description: **TV_LOCK Vertical Delay** *Intel Hex Address:* **09h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
TV_ADJ_V							

NOTE: TV_ADJ_V specifies the vertical start position of the TV_LOCK signal with respect to TV_VSYNC. It is measured in VGA line times. The register value is the actual value, with a resolution of one VGA line.

Bit	Power-On Value	Description
7:0	0000 0000	**Vertical Delay of TV_LOCK**

9.3.4 VGA Horizontal Total MSB

Register Description: **VGA Horizontal Total MSB** *Access:* **Read/Write**					*Intel Hex Address:* **0Ah**		
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
PP_OUT_DLY[1:0]		FLD_INVRT	TST_PP_OUT	TST_IN_SEL	TV_LOCK_EN	TV_HTOTAL_M	TV_ADJ_H_M

Bit	Power-On Value	Description
7:6	00	**Preprocessor Output Delay of YCrCb** 00: No delay 01: One 27-MHz clock cycle 10: Two 27-MHz clock cycles 11: Three 27-MHz clock cycles
5	0	**Invert Field Bit** (Preprocessor only) Swap even and odd fields 0: Do not invert 1: Invert
4	0	**Send Preprocessor Output to VIDIN1** (Test only) 0: Normal operation 1: Preprocessor output to VIDIN1
3	0	**Select Video Input to Preprocessor** (Test only) 0: VIDIN1 is input port 1: VIDIN2 is input port
2	0	**Enable TV_LOCK** 0: TV_LOCK disabled (always high) 1: TV_LOCK enabled
1	0	**Horizontal Total MSB:** VGA pixels per input line: 1 MSB
0	0	**Horizontal Delay of TV_LOCK:** 1 MSB

9.3.5 Horizontal Downscaler Output Width

Register Description: **Horizontal Downscaler Output Width** *Intel Hex Address:* **0Bh**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
H_SIZE_D							

NOTE: H_SIZE_D contains the output width of the horizontal downscaler (mod4(pixel counter)). H_SIZE_D is the output width divided by 4 of the horizontal downscaling filter. This is the actual number of active pixels per line that pass through the preprocessor, and are written to the rate buffer FIFO one VGA line at a time. If 7.5 = 111, a test mode is selected.

Bit	Power-On Value	Description
7:0	1010 0000 = 640 decimal	**Output Width** (mod 4(pixel counter)) of horizontal downscaler.

9.3.6 Horizontal Downscaling Factor

Register Description: **Horizontal Downscaling Factor** *Intel Hex Address:* **0Ch**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
H_STEP_D							

NOTE: H_STEP_D defines the horizontal downscaling factor as derived with Equation 9-1. It is the fractional part of the step value (input/output) of the input horizontal scaler. The step range is 1.00000000 through 1.11111111 with the integer '1' implied. The value '0000 0000' specifies no scaling.

$$HSTEPD = \left(\left(\frac{\text{input width}}{\text{output width}}\right) \bullet 256\right) - 256 \qquad \textbf{Equation 9-1}$$

Bit	Power-On Value	Description
7:0	0000 0000 = 1	**Horizontal Downscaling Factor**

9.3.7 Horizontal Upscaling Factor

Register Description: **Horizontal Upscaling Factor** *Intel Hex Address:* **0Dh**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
H_STEP_U							

NOTE: H_STEP_U defines the horizontal upscaling factor after rate conversion as derived with Equation 9-2. It is the lower part of the step value (input/output) of the output horizontal scaler. The step range is 00.0000001 through 10.0000000. The value '0000 0000' specifies a scale factor of 2.0 (the MSB is implied). The value '0000 0001' specifies a scale factor of 1.0 (no scaling).

$$HSTEPU = \left(\left(\frac{\text{input width}}{\text{output width}}\right) \bullet 512\right) - 256$$

Equation 9-2

Bit	Power-On Value	Description
7:0	0000 0001	**Horizontal Upscaling Factor** 0000 0000: 2.00 scaling factor

9.3.8 Horizontal Origin

Register Description: **Horizontal Origin** *Intel Hex Address:* **0Eh**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
X_ORIG							

Bit	Power-On Value	Description
7:0	0000 1010 = (pixel 20)	**Horizontal Origin** of scaled and filtered picture within 720 active pixel window (2 pixel step size)

9.3.9 Vertical Origin

Register Description: **Vertical Origin** *Intel Hex Address:* **0Fh**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Y_ORIG							

Bit	Power-On Value	Description
7:0	0	**Vertical Origin** of scaled and filtered picture within 240 (288 for PAL) active line window. This is measured by counting lines in the even fields.

9.3.10 Horizontal Size

Register Description: **Horizontal Size** *Intel Hex Address:* **10h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
X_SIZE							

Bit	Power-On Value	Description
7:0	1010 0000 = 640 pixels	**Number of output pixels** from the preprocessor within 720 active pixel window (4 pixel step size). If [7:5] are '111', this filter is bypassed (test purposes only).

9.3.11 Vertical Size

Register Description: **Vertical Size**							*Intel Hex Address:* **11h**
Access: **Read/Write**							
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Y_SIZE							

Bit	Power-On Value	Description
7:0	0111 1000 = 480 lines	**Number of output lines** after vertical scaling within the 480 (288 for PAL) active line window (4 lines resolution)

9.4 Filter Registers

9.4.1 Filter Miscellaneous

Register Description: **Filter Miscellaneous** *Intel Hex Address:* **12h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Y_STEP			FLICK_FILT			H_ALIAS	

Bit	Power-On Value	Description
7:5	000	**Vertical Scaling Factor** 000: 5/5 001: 5/6 010: 5/7 011: 5/8 100: 5/9 101: Reserved 110: Reserved 111: Bypass (test purposes only)
4:2	000	**Select Flicker Filter Algorithm** 000: autodetect among F1, F2, F3, F4) 001: Filter 1 010: Filter 2 011: Filter 3 100: Filter 4 101: Autodetect among F1, F3, F4 only 110: Autodetect among F1, F2, F4 only 111: Autodetect with gray levels (evaluation only)
1:0	00	**Horizontal Anti-aliasing Control** 00: No anti-aliasing (bypass) 01: Anti-aliasing filter bandwidth is 5.0 MHz 10: Anti-aliasing filter bandwidth is 5.5 MHz 11: Bypass filter – test purposes only

9.4.2 Chrominance Amplitude Coefficient

Register Description: **Chrominance Amplitude Coefficient** *Intel Hex Address:* **13h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
CH_AMP							

Bit	Power-On Value	Description
7:0	1000 0000	**Chrominance Amplitude Coefficient**

9.4.3 Luminance Amplitude Coefficient

Register Description: **Luminance Amplitude Coefficient** *Intel Hex Address:* **14h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Y_AMP							

Bit	Power-On Value	Description
7:0	1000 0000	**Luminance Amplitude Coefficient**

9.5 Serial Address Interface Register

9.5.1 Serial Interface Device Address

Register Description: **Serial Interface Device Address** *Access:* **Read/Write**							*Intel Hex Address:* **15h**
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved	SERIAL_ADDR						

Bit	Power-On Value	Description
7		**Reserved**
6:0	0000 0000	**Serial Interface Device Address**

9.6 Subcarrier Registers

9.6.1 Color Burst Amplitude Coefficient

Register Description: **Color Burst Amplitude Coefficient** *Intel Hex Address:* **16h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
BU_AMP							

Bit	Power-On Value	Description
7:0	0001 1100	**Color Burst Amplitude**

9.6.2 Color Carrier Synthesis Byte 0

Register Description: **Color Carrier Synthesis Byte 0** *Intel Hex Address:* **17h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
CC_0							

Bit	Power-On Value	Description
7:0	0011 1110	**Color Carrier Synthesis** [7:0]

9.6.3 Color Carrier Synthesis Byte 1

Register Description: **Color Carrier Synthesis Byte 1** *Intel Hex Address:* **18h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
CC_1							

Bit	Power-On Value	Description
7:0	1111 1000	**Color Carrier Synthesis** [15:8]

9.6.4 Color Carrier Synthesis Byte 2

Register Description: **Color Carrier Synthesis Byte 2** *Intel Hex Address:* **19h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
CC_2							

Bit	Power-On Value	Description
7:0	1100 1000	**Color Carrier Synthesis** [23:16]

9.6.5 Color Carrier Synthesis Byte 3

Register Description: **Color Carrier Synthesis Byte 3** *Intel Hex Address:* **1Ah**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
CC_3							

Bit	Power-On Value	Description
7:0	0100 0011	**Color Carrier Synthesis** [31:24]

9.6.6 Hue Phase Shift Byte 0

Register Description: **Hue Phase Shift Byte 0** *Intel Hex Address:* **1Bh**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
HUE_LSB							

Bit	Power-On Value	Description
7:0	0000 0000	**Hue Phase Shift** [7:0]

9.6.7 Hue Phase Shift Byte 1

Register Description: **Hue Phase Shift Byte 1** *Intel Hex Address:* **1Ch**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
SCH_HDJ						HUE_MSB	

Bit	Power-On Value	Description
7:2	0000 00	**Subcarrier-to-Horizontal Sync Phase Adjust**
1:0	00	**Hue Phase Shift** [9:8]

9.7 Closed-Caption Registers

9.7.1 Closed-Caption Control

Register Description: **Closed-Caption Control** *Intel Hex Address:* **1Dh**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved						CCEN1	CCEN0

Bit	Power-On Value	Description
7:2		**Reserved**
1	0	**Enable Closed-Caption for Line 284** 0: Disable 1: Enable
0	0	**Enable Closed-Caption for Line 21** 0: Disable 1: Enable

9.7.2 Closed-Caption Data Line 21: First Byte

Register Description: **Closed-Caption Data Line 21: First Byte** *Intel Hex Address:* **1Eh**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
CC_21_1							

Bit	Power-On Value	Description
7:0	0000 0000	**First Byte of Closed-Caption Data** for line 21

9.7.3 Closed-Caption Data Line 21: Second Byte

Register Description: **Closed-Caption Data Line 21: Second Byte** *Intel Hex Address:* **1Fh**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
CC_21_2							

Bit	Power-On Value	Description
7:0	0000 0000	**Second byte of closed-caption data** for line 21

9.7.4 Closed-Caption Data Line 284: First Byte

Register Description: **Closed-Caption Data Line 284: First Byte** *Intel Hex Address:* **20h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
CC_284_1							

Bit	Power-On Value	Description
7:0	0000 0000	**First byte of closed-caption data** for line 284

9.7.5 Closed-Caption Data Line 284: Second Byte

Register Description: **Closed-Caption Data Line 284: Second Byte**							*Intel Hex Address:* **21h**
Access: **Read/Write**							
Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
CC_284_2							

Bit	Power-On Value	Description
7:0	0000 0000	**Second byte of closed-caption data** for line 284

9.8 Window Registers

9.8.1 Window Horizontal Start

Register Description: **Window Horizontal Start** *Intel Hex Address:* **22h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
WIN_X_ORIG							

Bit	Power-On Value	Description
7:0	0000 0000	**Horizontal coordinate** for window start (4 pixel step)

9.8.2 Window Vertical Start

Register Description: **Window Vertical Start** *Intel Hex Address:* **23h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
WIN_Y_ORIG							

Bit	Power-On Value	Description
7:0	0000 0000	**Vertical coordinate** for window start (4 scanline step)

9.8.3 Window Horizontal Size

Register Description: **Window Horizontal Size** *Intel Hex Address:* **24h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
WIN_X							

Bit	Power-On Value	Description
7:0	0000 0000	**Horizontal size** of window (4 pixel step)

9.8.4 Window Vertical Size

Register Description: **Window Vertical Size** *Intel Hex Address:* **24h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
WIN_Y							

Bit	Power-On Value	Description
7:0	0000 0000	**Vertical size** of window (4 scanline step)

9.8.5 Miscellaneous Window Registers 3–1

Register Description: **Misc. Window 3–1** *Intel Hex Address:* **3Ch–3Eh**
Access: **Read/Write**

Bit 23	*Bit 22*	*Bit 21:0*
WSS_EN	WSS_PAL_F2	WSS[21:0]

Bit	Power-On Value	Description
23	0	**WSS_EN:** When this bit is set, the WSS process is enabled.
22	0	**WSS_PAL_F2:** This bit encodes WSS also in field 2, line 23 in PAL, NTSC: X.

Bit	Power-On Value	Description *(cont.)*
21:0	00h	**WSS_21:** PAL: group 4, bit 13, NTSC: X **WSS_20:** PAL: group 4, bit 12, NTSC: X **WSS_19:** PAL: group 4, bit 11, NTSC: bit 20 **WSS_18:** PAL: group 3, bit 10, NTSC: bit 19 **WSS_17:** PAL: group 3, bit 9, NTSC: bit 18 **WSS_16:** PAL: group 3, bit 8, NTSC: bit 17 **WSS_15:** PAL: group 2, bit 7, NTSC: bit 16 **WSS_14:** PAL: group 2, bit 6, NTSC: bit 15 **WSS_13:** PAL: group 2, bit 5, NTSC: bit 14 **WSS_12:** PAL: group 2, bit 4, NTSC: bit 13 **WSS_11:** PAL: group 1, bit 3, NTSC: bit 12 **WSS_10:** PAL: group 1, bit 2, NTSC: bit 11 **WSS_9:** PAL: group 1, bit 1, NTSC: bit 10 **WSS_8:** PAL: group 1, bit 0, NTSC: bit 9 **WSS_7:** PAL: X, NTSC: bit 8 **WSS_6:** PAL: X, NTSC: bit 7 **WSS_5:** PAL: X, NTSC: bit 6 **WSS_4:** PAL: X, NTSC: bit 5 **WSS_3:** PAL: X, NTSC: bit 4 **WSS_2:** PAL: X, NTSC: bit 3 **WSS_1:** PAL: X, NTSC: bit 2 **WSS_0:** PAL: X, NTSC: bit 1

9.9 Interrupt Registers

9.9.1 Interrupt Enable

Register Description: **Interrupt Enable** *Intel Hex Address:* **40h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved				INT_EN	INT_21_EN	INT_284_EN	INT_V_EN

Bit	Power-On Value	Description
7:4		**Reserved**
3	0	**Interrupt Enable** 0: Pin 34 is a clock output 1: Pin 34 is an interrupt request output
2	0	**Enable interrupt** for line 21
1	0	**Enable interrupt** for line 284
0	0	**Enable interrupt** for video field

9.9.2 Interrupt Clear

Register Description: **Interrupt Clear** *Intel Hex Address:* **41h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved					CLR_INT_21	CLR_INT_284	CLR_INT_V

Bit	Power-On Value	Description
7:3	0	**Reserved**
2	0	**Clear interrupt** for line 21
1	0	**Clear interrupt** for line 284
0	0	**Clear interrupt** for video field

9.10 Status Registers

9.10.1 Device ID

Register Description: **Device ID** *Intel Hex Address:* **42h**
Access: **Read**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
DEVICE_ID							

Bit	Power-On Value	Description
7:0	0011 0100 (CL-GD1052) 0011 0101 (CL-GD1053)	**Device Identification**

9.10.2 Status

Register Description: **Status** *Intel Hex Address:* **43h**
Access: **Read**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
SENSE_C	SENSE_S	INT_21	INT_284	INT_V	FLD		

Bit	Power-On Value	Description
7		**Monitor Connected (Composite Video)** 0: Connected 1: Not connected
6		**Monitor Connected (S-Video)** 0: Connected 1: Not connected
5		**Interrupt Flag:** line 21 complete
4		**Interrupt Flag:** line 284 complete
3		**Interrupt Flag:** video field change
2:0		**Field Status** (001 = Field 1, 000 = Field 8)

9.10.3 Revision Code

Register Description: **Revision Code** *Intel Hex Address:* **44h**
Access: **Read**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							

Bit	Power-On Value	Description
7:0		**Reserved**

9.11 Test Registers

9.11.1 RAM Test Control

Register Description: **RAM Test Control** *Intel Hex Address:* **45h**
Access: **Read/Write**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							

Bit	Power-On Value	Description
7:0	0	**Reserved**

9.11.2 Test Control Byte 0

Register Description: **Test Control Byte 0** *Intel Hex Address:* **46h**
Access: **Read/Write**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							

Bit	Power-On Value	Description
7:0	0	**Reserved**

9.11.3 Test Control Byte 1

Register Description: **Test Control Byte 1** *Intel Hex Address:* **47h**
Access: **Read/Write**

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Reserved							

Bit	Power-On Value	Description
7:0	0	**Reserved**

9.12 CL-GD5465 Programming

The PV1_CONFIG register should be programmed as shown in Table 9-2.

Table 9-2. PV1_CONFIG Register Programming

Field Name	Bit Position	Value (Binary)	Note
PVport2XIntfClk	10	1	–
PVClockMode	9	0	Default
PVDir	8	0	Default
PVIntf[3:0]	7:4	0011	–
PVTstate	3	0	–

9.13 Typical Values

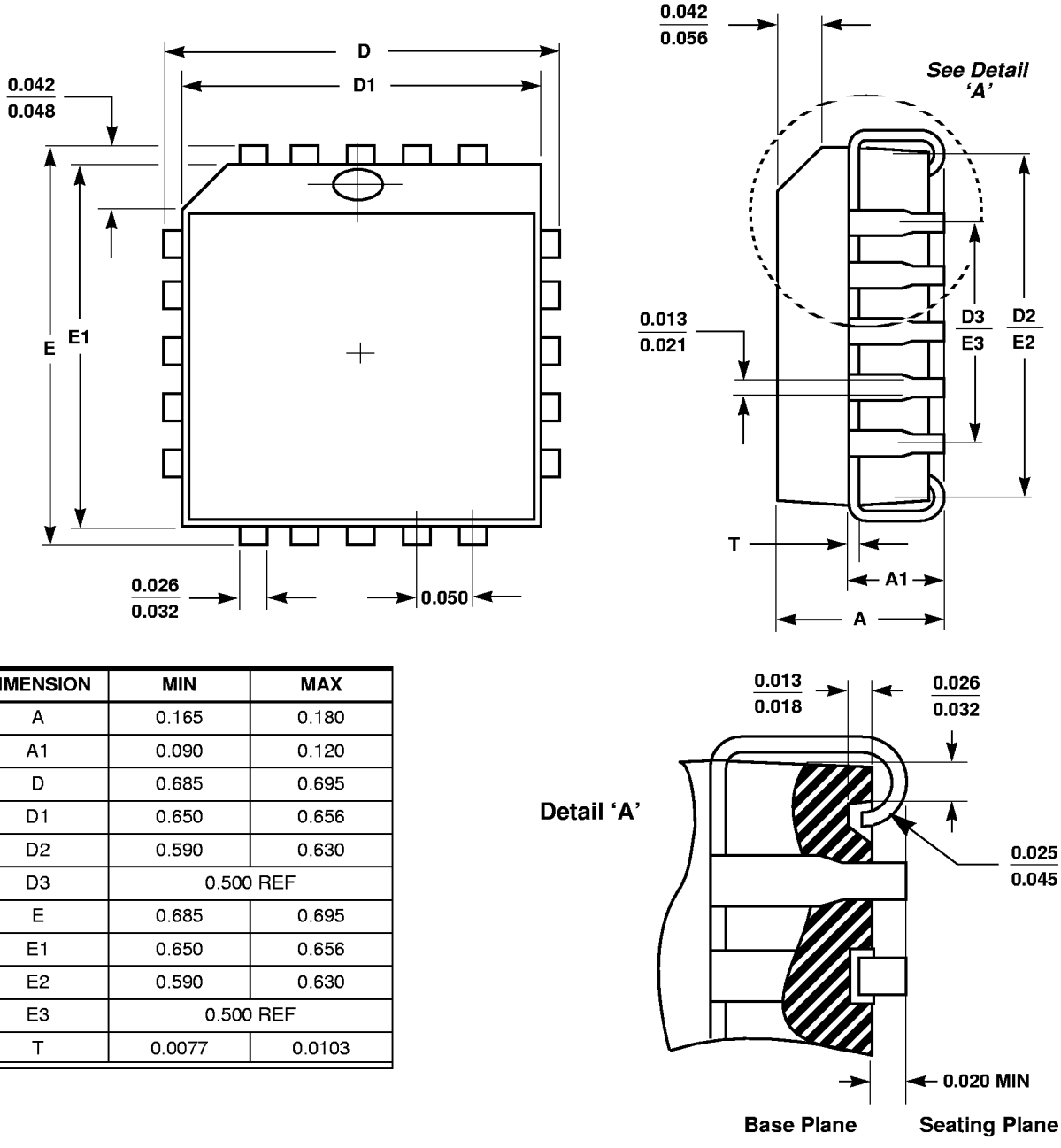
Table 9-3. Typical Programming Values (Binary)

Register Name	Interlaced NTSC-M	Interlaced PAL	Non-Interlaced NTSC	Non-Interlaced PAL
00h: Global Control 0	001X 1011	010X 1011	001X 1011	010X 1011
01h: Global Control 1	0000 0100[a]	0010 0000	0000 0100	0010 0000
02h: Global Control 2	XX00 0000	XX00 1000	XX00 0000	XX00 1000
03h: Global Control 3	1000 0100	1000 0100	0000 0100	0000 0100
04h: Global Control 4	XX11 1000	XX11 1000	XX11 1000	XX11 1000
05h: Global Control 5	XXXX XXXX	XXXX XXXX	XXXX XXXX	XXXX XXXX
06h: Background Color	0000 0011	0000 0011	0000 0011	0000 0011
07h: VGA Horizontal Total				
08h: TV_LOCK Horizontal Delay				
09h: TV_LOCK Vertical Delay				
0Ah: VGA Horizontal MSBs	0000 0100	0000 0100	0000 0100	0000 0100
0Bh: Horizontal Downscaler Width				
0Ch: Horizontal Downscaler Factor				
0Dh: Horizontal Upscale Factor				
0Eh: Horizontal Origin	0000 1010	0000 1010	0000 1010	0000 1010
0Fh: Vertical Origin	0000 0000	0000 0000	0000 0000	0000 0000
10h: Horizontal Size	1010 0000	1010 0000	1010 0000	1010 0000
11h: Vertical Size	0111 1000	0111 1000	0111 1000	0111 1000
12h: Vertical Scale Factor				
13h: Chrominance Amplitude Coefficient	1000 0000	1000 0000	1000 0000	1000 0000
14h: Luminance Amplitude Coefficient	1000 0000	1000 0000	1000 0000	1000 0000
16h: Color Burst Amplitude	0001 1100	0001 0101	0001 1100	0001 0101
17h: Color Carrier Byte 0	0011 1110	1001 0110	0011 1110	1001 0110
18h: Color Carrier Byte 1	1111 1000	0001 0101	1111 1000	0001 0101
19h: Color Carrier Byte 2	1110 0000	0001 0011	1110 0000	0001 0011
1Ah: Color Carrier Byte 3	0100 0011	0101 0100	0100 0011	0101 0100
1Bh: Hue Phase Shift Byte 0	0000 0000	0000 0000	0000 0000	0000 0000
1Ch: Hue Phase Shift Byte 1	0000 0000	0000 0000	0000 0000	0000 0000

[a] NTSC-J settings = 0000 0000.

10. PACKAGE SPECIFICATIONS

10.1 44-Pin PLCC (Plastic-Leaded Chip Carrier) Package Data

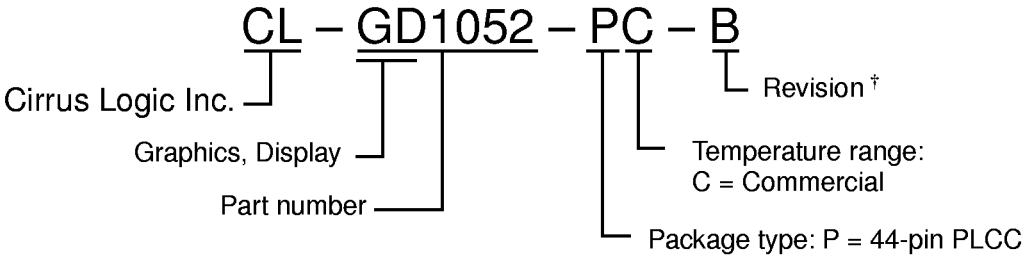


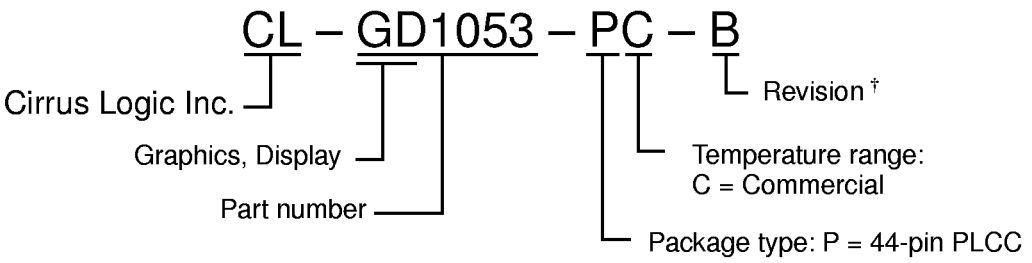
DIMENSION	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
D3	0.500 REF	
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
E3	0.500 REF	
T	0.0077	0.0103

NOTES:

1) Dimensions are in inches, and the controlling dimension is also in inches.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

11. ORDERING INFORMATION





† Contact Cirrus Logic for up-to-date information on revisions.

Appendix A

BIBLIOGRAPHY

The following documents are referenced in this data book or contain additional relevant information.

- *I²C-bus Specification (including fast-mode)*, Philips Semiconductor®, Desktop Video Products, 1993
- CCIR Recommendation 601-2, International Telecommunication Union, 1990
- *CL-GD5465 Technical Reference Manual*, Cirrus Logic Inc., May 1997 (order no. 385465-002)
- *Programmer's Guide to the EGA and VGA Cards*, Ferraro, Richard F., Third Edition (ISBN 0-201-62490-7)
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