National Semiconductor

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MM54240
Asynchronous Receiver/Transmitter Remote Controller

General Description

The MM54240 is a monolithic MOS integrated circuit utilizing N-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. The circuit is designed for processor-type remote control applications. The data transmission consists of a pulse width modulated serial data stream of 18 bits. This stream consists of 7 address bits, 1 command bit, 8 data bits, 1 parity bit and 1 dummy bit in that order.

The MM54240 can be operated in two modes; namely "master" and "slave". The master interfaces to a processor bus, and is capable of polling and controlling 128 slave circuits. The slave circuits are interfaced to remote data sources and/or data destinations.

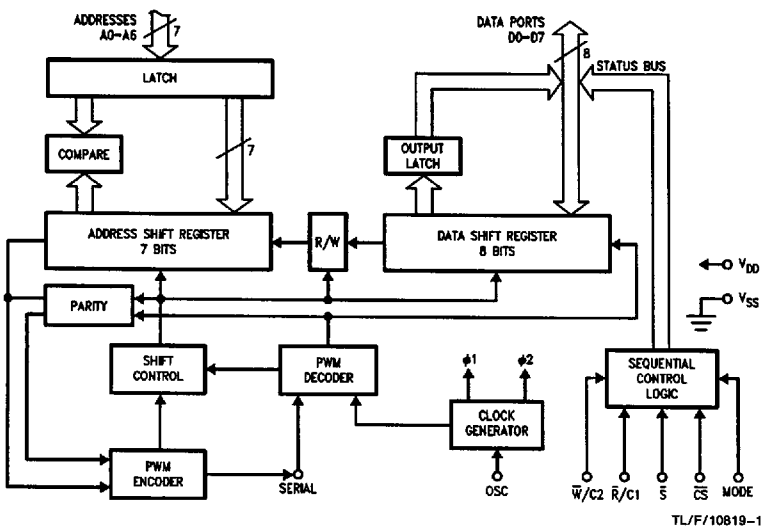
Applications

The MM54240 finds application in transmitting data to and receiving data from remote A-D/D-A, remote microprocessor units, remote digital transducer or remote data peripheral devices.

Features

- Supply voltage range—4.75V to 11.5V single supply
- Low quiescent current—5.0 mA maximum
- On-chip oscillator based on inexpensive R-C components
- Pulse width modulation techniques minimize error and maximize frequency tolerance
- Mode input for either master or slave operations
- Chip select ($\overline{CS}$) input in the master mode
- Selectable output port options in the slave mode
- Transmit/receive control output ($\overline{CS}$) in the slave mode

Functional Block Diagram



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Pin	Configuration
1	V_{SS}
2	D7 (MSB)
3	D6
4	D5
5	D4
6	D3
7	D2
8	D1
9	D0 (LSB)
10	Serial
11	Mode
12	$\overline{CS}$
13	V_{DD}
14	$\overline{R}$/C1
15	$\overline{W}$/C2
16	$\overline{S}$
17	OSC
18	A6 (MSB)
19	A5
20	A4
21	A3
22	A2
23	A1
24	A0 (LSB)

Order Number MM54240N
See NS Package Number N24C

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RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings

(exceeding these ratings could result in permanent damage to the device)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

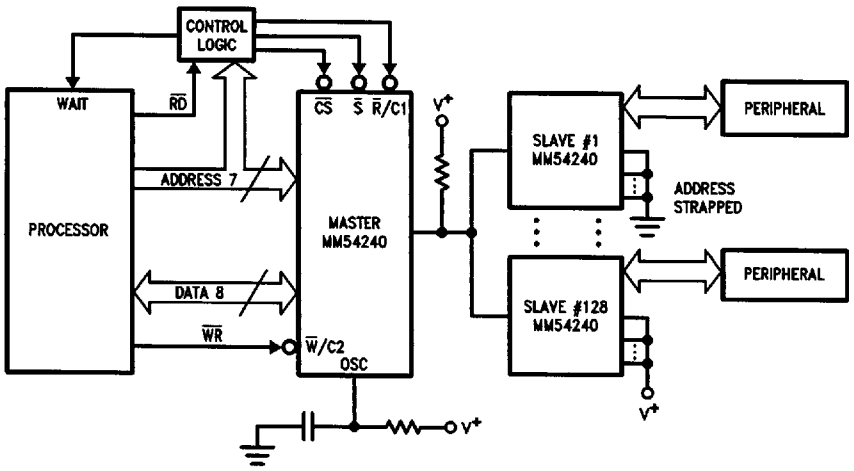
Voltage on Any Pin with Respect to V_{SS}	−0.5V to +12.0V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A within operating range, V_{SS} = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.75		11.5	V
I_{DD}	Supply Current, Quiescent	V_{DD} = 4.75V to 11.5V			5.0	mA
	Input Voltage					
V_{IL}	Logic "0"	V_{DD} = 4.75V to 11.5V	0		0.8	V
V_{IH}	Logic "1"	V_{DD} = 4.75V to 5.25V	2.4		V_{DD}	V
V_{IH}	Logic "1"	V_{DD} = 5.25V to 11.5V	V_{DD} − 2.85		V_{DD}	V
	Output Current (D0–D7)					
I_{OL}	V_{OL} = 0.4V	V_{DD} = 4.75V to 11.5V	2.0			mA
I_{OH}	V_{OH} = 2.4V	V_{DD} = 4.75V to 5.25V	200			μA
I_{OH}	V_{OH} = 0.5 V_{DD}	V_{DD} = 5.25V to 11.5V	200			μA
I_{OH}	V_{OH} = 0.6 V_{DD} (Weak V_{OH})	V_{DD} = 4.75V to 11.5V	0.5		30	μA
I_{OS}	Short Circuit Output Current	V_{DD} = 4.75V to 5.25V		5		mA
	Output ($\overline{CS}$ Slave)					
I_{OL}	V_{OL} = 0.5V	V_{DD} = 4.75V to 11.5V	0.4			mA
	Frequency RC Input					
F	For a Fixed $(RC)_1$ (Note 1)	V_{DD} = 4.75V to 7.0V	200	400	600	kHz
F	For a Fixed $(RC)_2$ (Note 1)	V_{DD} = 7.0V to 11.5V	200	400	600	kHz
	Output Current (Serial)					
I_{OL}	V_{OL} = 0.4V	V_{DD} = 4.75V to 11.5V	2.0			mA
I_{LEAK}	Open-Drain Leakage	V_{DD} = 4.75V to 11.5V			10	μA
	Internal Input Pull-Up Resistors, $\overline{CS}$, Mode					
I_{IL}	V_{IN} = V_{SS}	V_{DD} = 4.75V to 11.5V	15		100	μA

Note 1: $(RC)_1$ or $(RC)_2$: suggested R 1 kΩ–10 kΩ, suggested C 50 pFd–500 pFd.

Typical Application



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Circuit Description

The MM54240 consists of four major logic blocks: Sequential Control, Shift Register, PWM Encoder and PWM Decoder.

Data Ports (D0–D7): The data ports are bidirectional and have three output levels (high, low and weak pull-up). The weak pull-up mode is only available when the MM54240 is a slave device. For the master circuit, the outputs are configured with standard high and low states coincident with properly enabled $\overline{CS}$ and $\overline{R}$. This permits direct interface or buffered interface with the standard bus structure of a processor system. The first three data ports (D0, D1, D2) also serve as status pins coincident with enabled $\overline{CS}$ and $\overline{S}$.* For the slave circuit, specialized input and output options are available by selecting the C1 and C2 inputs. The data port can still be read even if it is configured as an output port.

Address Ports (A0–A6): The address ports are for the input of address information into the MM54240. For the master circuit, the input must be valid during the $\overline{R}$ and $\overline{W}$ command strobes. For the slave circuit, a unique hard-wired code must be on the address ports. This code is the address of the slave circuit for addressing purposes. No internal pull-ups are provided.

Mode: This input is low for slave and high (or open) for master selections. An internal pull-up resistor is provided.

Chip Select ($\overline{CS}$): This pin has an internal pull-up resistor to V_{DD}. In the master mode, $\overline{CS}$ is an input and has to be pulled low before the $\overline{R}$, $\overline{W}$, or $\overline{S}$ strobes can be acknowledged. When $\overline{CS}$ is a logic high, the data port pins are high impedance. In the slave mode, $\overline{CS}$ is an output. It is a logic "0" when the circuit is expecting to receive a transmission. $\overline{CS}$ is intended only for controlling a transceiver buffer device. During the receive mode, $\overline{CS}$ will produce a high-going pulse when the dummy bit is received, but prior to the internal address compare. Thus, all slaves (addressed or not addressed) will produce this pulse when receiving a transmission. The slave that is addressed will keep $\overline{CS}$ high until it completes the transmission to the master.

Read/Control 1 ($\overline{R}$/C1): In the master mode, while $\overline{CS}$ is active low, this input can be used to initiate either of the following three operations depending upon the present status of the circuit.

1. To initiate a read command
2. To enable output ports if transmission received is valid
3. To terminate read command if transmission received is incorrect (if master is in state 4 awaiting data from slave, a dummy read will set master to initialize)

In the slave mode, this input, together with $\overline{W}$/C2, selects the specialized output port configuration.

Write/Control 2 ($\overline{W}$/C2): In the master mode, while $\overline{CS}$ is active low, this input can be used to initiate a write command. In the slave mode, this input, together with $\overline{R}$/C1, selects the specialized output port configuration.

Status ($\overline{S}$): In the master mode, while $\overline{CS}$ is active low, this input enables circuit status information to be output at the first three data ports. The other five data ports will be at logic "0". In the slave mode, this input sets all the output (D0–D7) latches to the logic "1" state. In the slave mode, status cannot be interrogated.

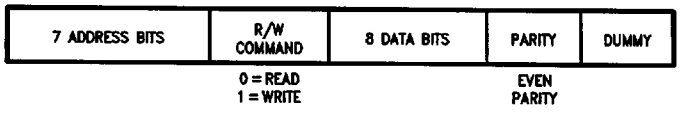
OSC: This input is for connection to a resistor-capacitor circuit for the on-chip oscillator. Frequency tolerance is specified for two voltage ranges. In a master-slave system, if no one circuit has a frequency more than a factor of 2 different from any other circuit, then, valid transmission is guaranteed. Nominal setting is 400 kHz.

Serial: Input and output pin for serial transmission. Output has open-drain configuration.

* The other data ports will output logic "0".

Data Format

1. Serially transmitted data



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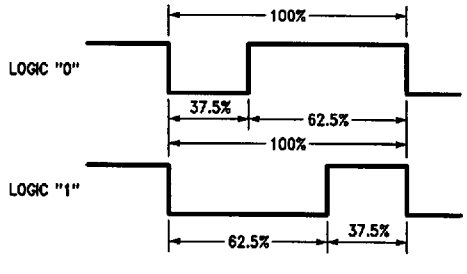
2. Pulse width modulation coding



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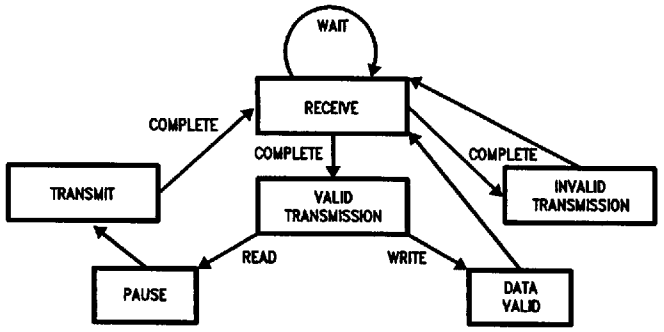
A bit is equivalent to 96 clocks of the R-C oscillator frequency i.e.; when R-C frequency = 400 kHz, 1 bit = 240 μs, 1 word = 4.32 ms.

Circuit Description (Continued)

Slave Circuit Logic Flow Diagram



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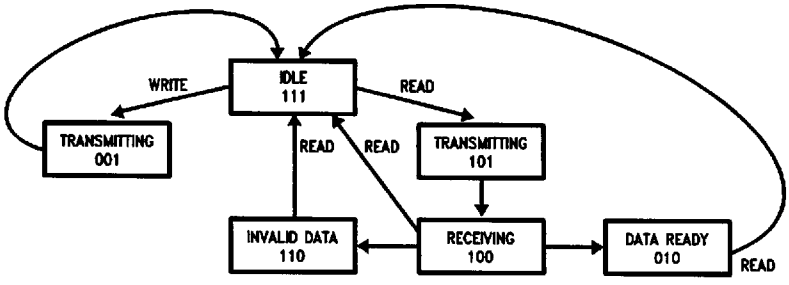
Specialized Output Options for Slave Circuits

C1	C2	Description
1	1	All 8 Pins are High Impedance Input Ports
0	1	All 8 Pins are Standard Low Impedance Output Ports
0	0	D1–D4 are Standard Low Impedance Output Ports D5–D8 are High Impedance Input Ports
1	0	Logic "0" Outputs are Low Impedance Output Ports Logic "1" Outputs are Weak Pull-Ups to V_{DD}

* In this option, the slave data ports can be connected in a wired-OR configuration with open-collector or open-drain outputs on the peripheral.

Master Circuit Logic Flow Diagram



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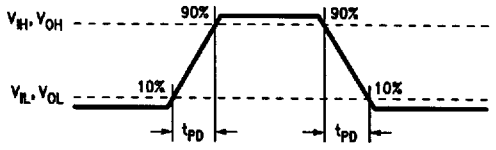
Master Configuration State Chart

Status Register			Description
D2	D1	D0	
0	0	0	Not Used
0	0	1	In Process of Transmitting to Slave during Write Slave Mode
0	1	0	Valid Data Received from Slave
0	1	1	Not Used
1	0	0	Awaiting Data from Slave during Read Slave Mode
1	0	1	In Process of Transmitting to Slave during Read Slave Mode
1	1	0	Invalid Data Received from Slave*
1	1	1	Initialization/Idle Condition

* This state is entered if address or parity do not match.

Timing Diagram Description



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Symbol	Parameter	Min	Max	Units
t_{DS}	Data and Address Set-Up Time	—	2	t_{OSC}
t_{DH}	Data and Address Hold Time	5	—	t_{OSC}
t_{PV}	Serial Port Valid	—	5	t_{OSC}
t_{PF}	Serial Port Float	—	1733	t_{OSC}
t_{DV}	Output Data Valid	—	1.0	μs
t_{DF}	Output Data Float	0		ns
t_1	Overlap Requirement	none		—
t_2	Delay Between Master-Slave Transmission	0.2	1.4	ms
t_3	CS • Function	3	—	t_{OSC}
t_{PD}	Rise and Fall Time	—	100	ns

Oscillator Calculations

Conditions:

$V = 5V \pm 5\%$

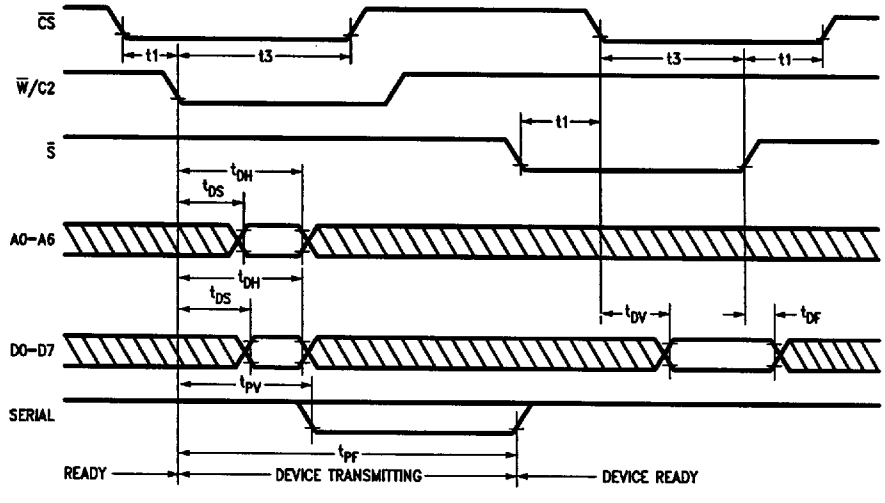
$F \approx 400\ kHz$

$-40°C \leq T \leq 85°C$

$$F = \frac{K}{RC}$$

where $0.8 \leq K \leq 1.4$

Master Write Operation



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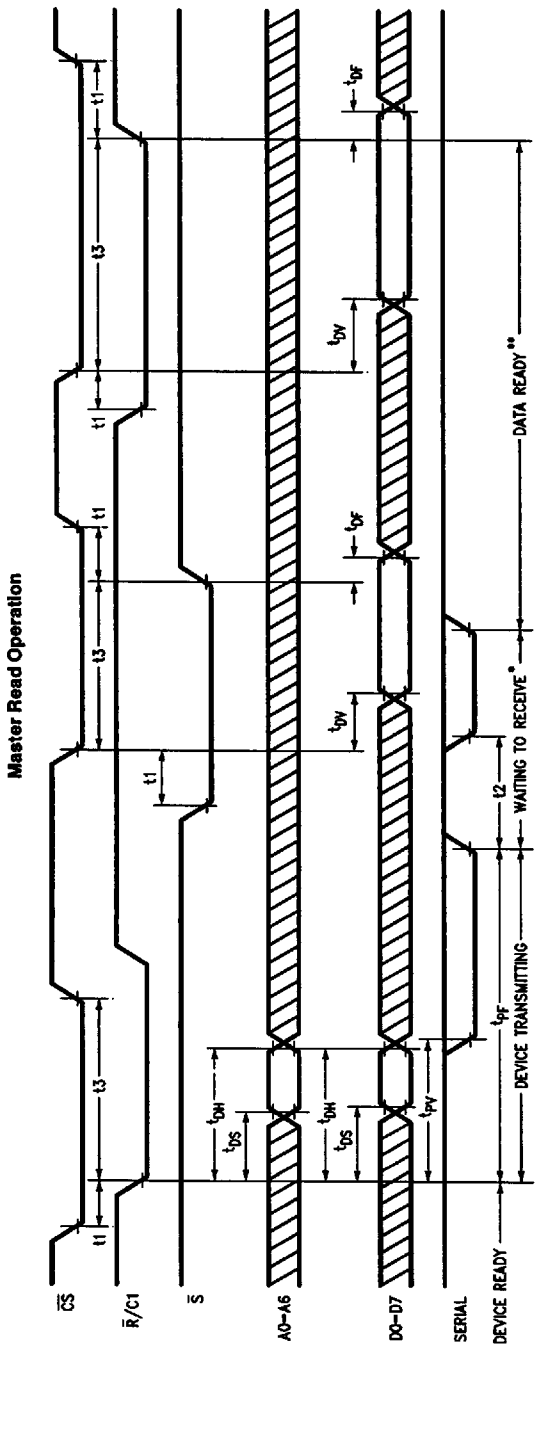
Timing Diagram Description (Continued)



t_1—There is no overlap requirement for CHIP SELECT

t_2—Delay between master-slave transmission 0.2 ms to 1.4 ms

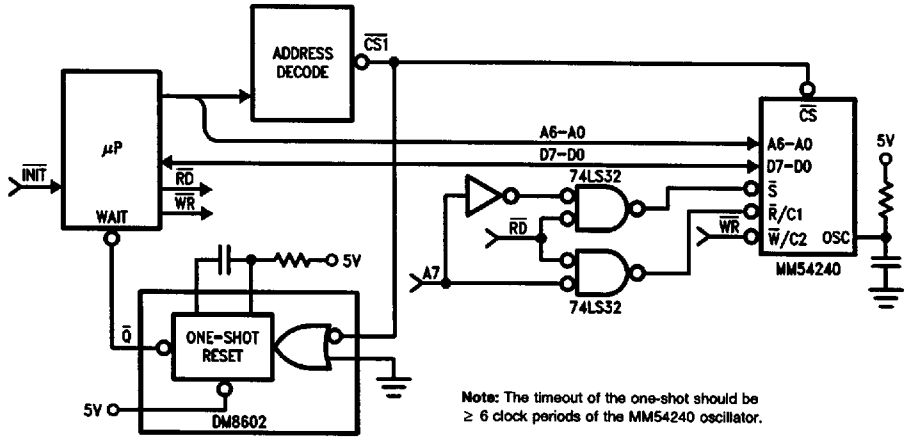
t_3—Minimum duration is 3 cycles of oscillator clock

* During "waiting to receive" state, $\overline{CS}$ coupled with R/C1 will force device into the device ready state.

** If address or parity do not match, the data invalid state is entered. $\overline{CS}$ coupled with R/C1 will force device into the device ready state.

Typical Applications

Microprocessor Interface to Master



Note: The timeout of the one-shot should be ≥ 6 clock periods of the MM54240 oscillator.

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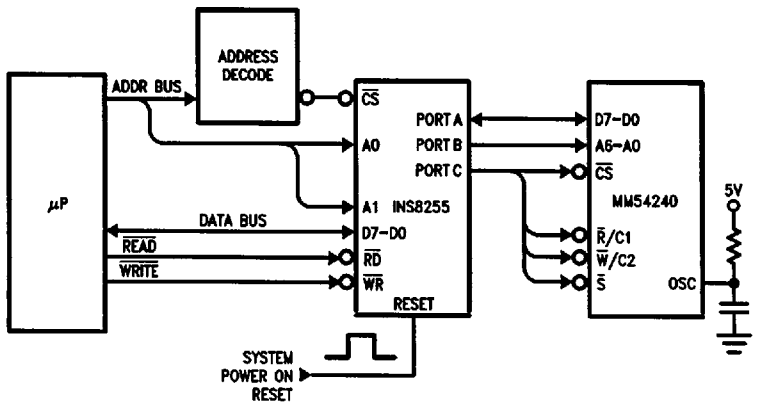
Microprocessor Interface to Master



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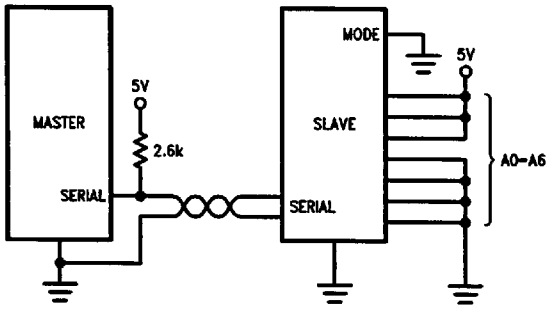
Note: The INS8255 is specified by the microprocessor to operate in mode 0. Port A is configured as input or output. Ports B and C are configured as output only. Load ports A and B prior to loading port C.

Typical Applications (Continued)

Master to Slave (Short Distance)



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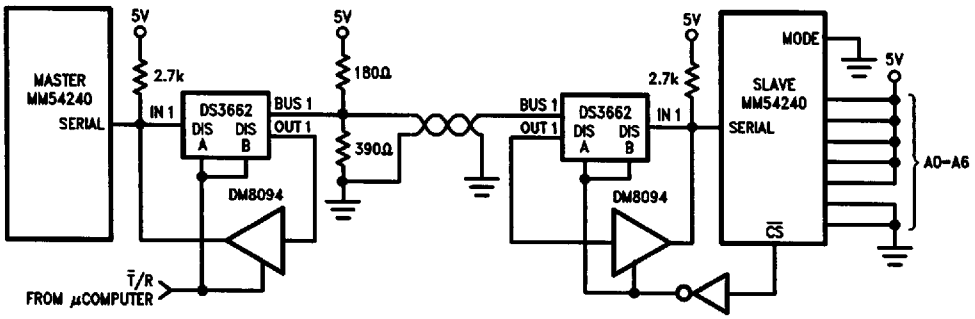
Master to Slave (Long Haul)



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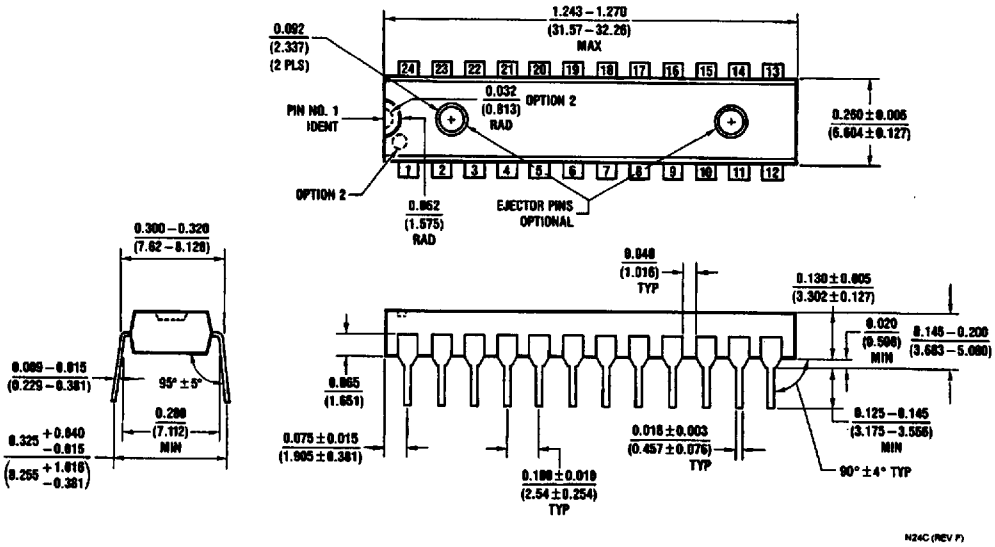
Physical Dimensions inches (millimeters)



24-Lead (SD) Molded Dual-In-Line Package (N)
Order Number MM54240N
NS Package Number N24C

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