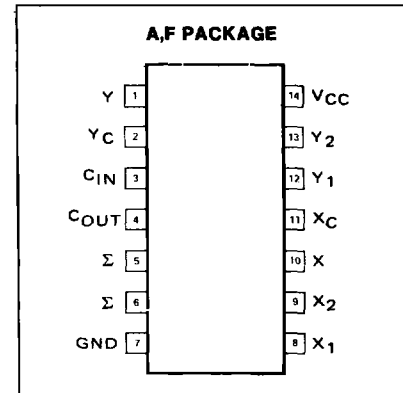
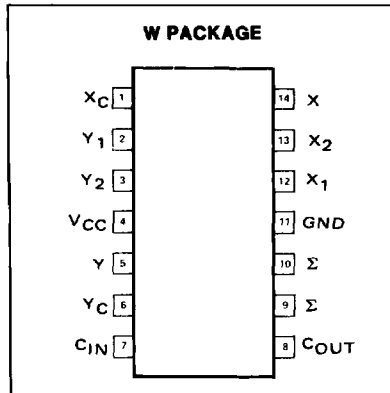


DESCRIPTION

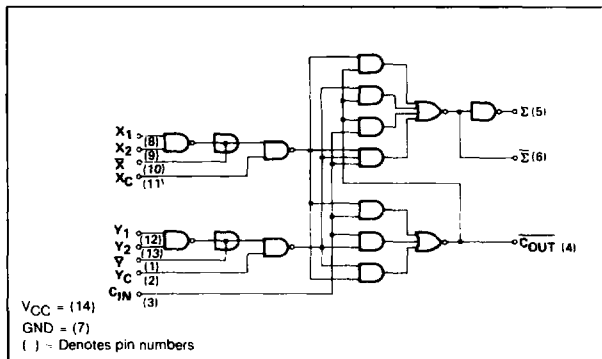
The 8268 is a single-bit full adder with gated true and complementary inputs, complementary sum (Σ and $\bar{\Sigma}$) outputs and an inverted carry output. By taking advantage of the unique true or inverted inputs and true or inverted outputs, parallel addition speed is greatly enhanced (by eliminating unnecessary inversions).

The device is designed for medium speed parallel and serial adder systems.

PIN CONFIGURATION



LOGIC DIAGRAM



TRUTH TABLE

CIN	Y	X	COUT	Σ	$\bar{\Sigma}$
0	0	0	1	0	1
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	1	0

NOTES:

- $X = \bar{X} \cdot X_c$, $Y = \bar{Y} \cdot Y_c$, where $\bar{X} = \bar{X}_1 \cdot Y_2$, $\bar{Y} = \bar{Y}_1 \cdot X_2$
- When \bar{X} or \bar{Y} are used as inputs, X_1 and X_2 or Y_1 or Y_2 respectively must be tied to GND.
- When X_1 and X_2 or Y_1 and Y_2 are used as inputs, \bar{X} or \bar{Y} respectively must be left open or used to perform the WIRED-AND function.

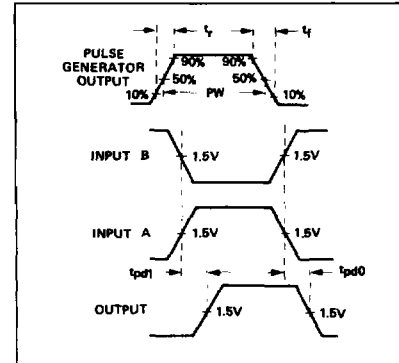
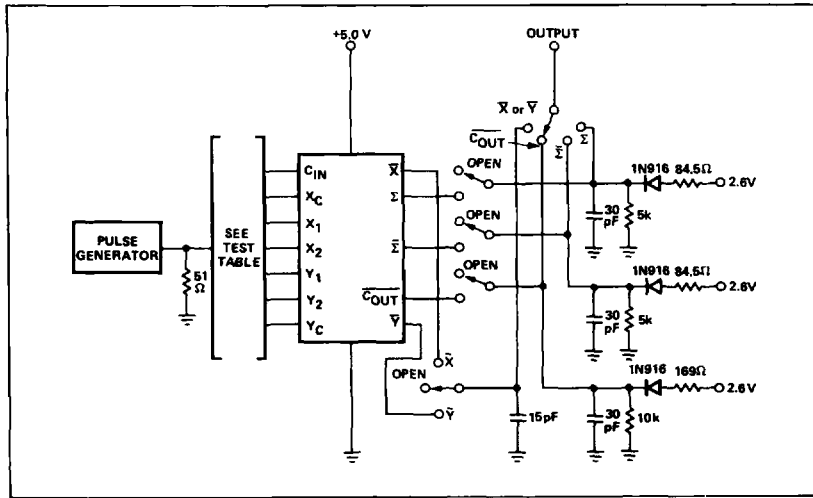
SWITCHING CHARACTERISTICS $T_A = 25^\circ C$, $V_{CC} = 5V$

PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS	LIMITS		UNIT
				TYP	MAX	
Propagation delay time						
tPLH	Low-to-high	CIN		8	13	ns
tPHL	High-to-low			8	13	
tPLH	Low-to-high	Yc		20	25	ns
tPHL	High-to-low			20	25	
tPLH	Low-to-high	Xc		35	45	ns
tPHL	High-to-low			35	45	
tPLH	Low-to-high	Yc		25	35	ns
tPHL	High-to-low			25	35	
tPLH	Low-to-high ¹	X1, X2		30	40	ns
tPHL	High-to-low ¹			15	20	
tPLH	Low-to-high ¹	Y1, Y2		30	40	ns
tPHL	High-to-low ¹			15	20	

NOTES:

- This test is a measure of the required worst-case data set-up time.

AC TEST FIGURE AND WAVEFORMS



NOTES:

1. Perform test in accordance with test table.
2. Each output is tested separately
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics
 $V_{gen} = 2.6V$, $t_r = t_f \leq 15ns$, $PW = 0.5ns$, $PRR = 1MHz$.
5. Inputs and outputs not otherwise specified are open
6. Capacitance shown include probe and μg capacitance
7. All resistances are in ohms.

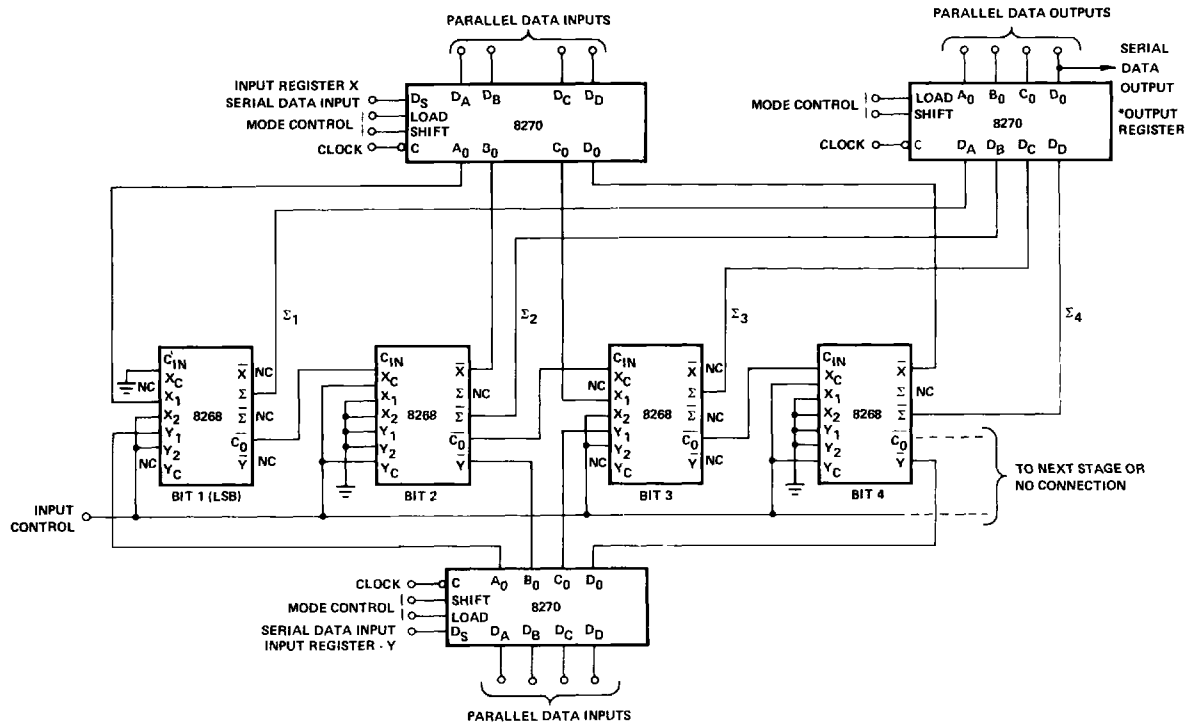
TEST TABLE (See Note 5)

TEST NO.	OUTPUTS UNDER TEST	APPLY INPUT A TO	APPLY INPUT B TO	APPLY +2.6V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	\bar{C}_{out}	None	C_{in}	None	Y_1	\bar{C}_{out}
2	\bar{C}_{out}	None	C_{in}	None	Y_1	\bar{C}_{out}
3	\bar{C}_{out}	Y_c	None	C_{in}	X_1, Y_1	\bar{C}_{out}
4	\bar{C}_{out}	Y_c	None	C_{in}	X_1, Y_1	\bar{C}_{out}
5	Σ	X_c	None	C_{in}	X_1, Y_1	Σ
6	Σ	X_c	None	C_{in}	X_1, Y_1	Σ
7	$\bar{\Sigma}$	Y_c	None	C_{in}	Y_1	$\bar{\Sigma}$
8	$\bar{\Sigma}$	Y_c	None	C_{in}	Y_1	$\bar{\Sigma}$
9	\bar{X}	None	X_1	X_2	None	\bar{X} (CL = 15 pF)
10	\bar{X}	None	X_1	X_2	None	\bar{X} (CL = 15 pF)
11	\bar{Y}	None	Y_1	Y_2	None	\bar{Y} (CL = 15 pF)
12	\bar{Y}	None	Y_1	Y_2	None	\bar{Y} (CL = 15 pF)

10101

TYPICAL APPLICATIONS

N-BIT PARALLEL ADDER



NOTES:

- To expand storage register for serial/parallel operation, connect D₀ to D_S of next stage and common the mode control lines and the clock line of the first stage to their respective second stage equivalents
- To expand output register for parallel outputs common clock, shift and load lines with their respective counterparts. For serial data output, also connect D₀ of first register to D_S of next register.

4-BIT SERIAL ADD/SUBTRACTOR

