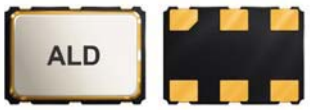
PECL/LVDS/CMOS OUTPUT SMD CRYSTAL CLOCK OSCILLATOR

ALD SERIES

RoHS Compliant



5.0 x 7.0 x 1.8mm

FEATURES:

- Based on a proprietary digital multiplier
- Tri-State Output
- Low Phase Noise and Jitter
- 2.5V to 3.3V +/- 5% operation
- Ceramic SMD, low profile package
- 156.25MHz, 187.5MHz, and 212.5MHz applications

APPLICATIONS:

- SONET, xDSL
- SDH, CPE
- STB

STANDARD SPECIFICATIONS:

PARAMETERS	
ABRACON P/N:	ALD Series
Frequency range:	750 kHz to 800 MHz
Operating temperature:	0° C to + 70° C (see options)
Storage temperature:	- 55° C to + 125° C
Overall frequency stability:	± 50 ppm max. (see options)
Supply voltage (Vdd):	3.3V ±10% (see options)
Jitter (12KHz - 20MHz) =	RMS phase jitter 3ps typ., <5ps max. period jitter < 35 ps peak to peak typical.
Low Phase Noise:	-109 dBc/Hz @ 1kHz Offset from 622.08MHz -110 dBc/Hz @ 10kHz Offset from 622.08MHz -109 dBc/Hz @ 100KHz Offset from 622.08MHz -112 dBc/Hz @ 1kHz Offset from 155.52MHz -125 dBc/Hz @ 10kHz Offset from 155.52MHz -123 dBc/Hz @ 100KHz Offset from 155.52MHz
Tristate Function:	"1" (V_{IH} ≥ 0.7*Vdd) or open: Oscillation "0" (V_{IL} < 0.3*Vdd): No Oscillation / Hi Z

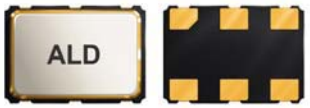
PECL:	Supply current (I_{DD}):**25mA max (for Fo<24MHz),65mA max (for 24MHz<Fo<96MHz) 100mA max (96MHz<Fo<700MHz)** Output Logic High: **V_{dd}-1.025V min, V_{dd}-0.880V max.** Output Logic Low: **V_{dd}-1.810V min. V_{dd}-1.620V max.** Symmetry (Duty Cycle): **45% min, 50% typ, 55% max,** Rise time: **0.85ns** Fall time: **0.85ns**
LVDS	Supply current (I_{DD}):25**mA max (for Fo<24MHz),45mA max (for 24MHz<Fo<96MHz),100mA max (96MHz<Fo<700MHz)** Output Clock Duty Cycle @ 1.25V: **45% min, 50% typical, 55% max** Output Differential Voltage (V_{OD}): **247mV min, 355mV typical, 454mV max** VDD Magnitude Change (ΔV_{OD}): **-50mV min, 50mV max** Output High Voltage : **V_{OH} = 1.4V typical, 1.6V max.** Output Low Voltage: **V_{OL} = 0.9V min, 1.1V typical** Offset Voltage [R_L = 100Ω]: **V_{OS} = 1.125V min, 1.2V typical, 1.375V max** Offset Magnitude Change [R_L = 100Ω]: **ΔV_{OS} = 0mV min, 3mV typical, 25mV max** Power-off Leakage (I_{OXD}) [Vout=VDD or GND, VDD=0V] = **±1µA typical, ±10µA max.** Differential Clock Rise Time (t_r) [R_L=100Ω, CL=10pF]: **0.2nS min, 0.7nS typical, 1.0nS,max** Differential Clock Fall Time (t_f) [R_L=100Ω, CL=10pF]: **0.2nS min, 0.7nS typical, 1.0nS max**
CMOS:	Supply current (I_{DD}):15**mA max (for Fo<24MHz),30mA max (for 24MHz<Fo<96MHz),40mA max (96MHz<Fo<700MHz)** Output Clock Rise/ Fall Time [10%~90% VDD with 10pF load]: **1.2ns typ, 1.6ns max.** Output Clock Duty Cycle [Measured @ 50% VDD]: **45% min, 50% typical, 55% max**

30332 Esperanza, Rancho Santa Margarita, California 92688
tel 949-546-8000 | fax 949-546-8001 | www.abracon.com

PECL/LVDS/CMOS OUTPUT SMD CRYSTAL CLOCK OSCILLATOR

ALD SERIES

RoHS Compliant



5.0 x 7.0 x 1.8mm

OPTIONS AND PART IDENTIFICATION

(Left blank if standard)

ALD□-Frequency-□-□-□-□-□

Supply Voltage	
Blank*	3.3V
2	2.5V

* 3.3V: Standard

Freq. Stability	
Blank*	±50ppm
R	±25ppm
K	±30ppm
H	±35ppm

Packaging	
T	Tape and Reel (1000pcs)

Operating Temperture Options	
Blank*	0°C to +70°C
D	-10°C to +60°C
E	-20°C to +70°C
F	-30°C to +70°C
N	-30°C to +85°C
L	-40°C to +85°C

*Standard Specification

Output	
P	PECL
P1	PECL1
V	LVDS
C	CMOS

Tristate Option	
A	Pin 1= NC Pin 2= tristate

TRI-STATE PIN OUT DESCRIPTION:

OUTPUT TYPE OPTION		PIN 1 logic level*	Output State
P	PECL	0 (Default)	Enabled
		1	Tri-state
P1	PECL1	1 (Default)	Enabled
		0	Tri-state
V	LVDS	0	Tri-state
		1(Default)	Enabled
C	CMOS	0	Tri-state
		1(Default)	Enabled

*Connect to VDD for logic level "1", connect to ground for logic level "0".

30332 Esperanza, Rancho Santa Margarita, California 92688
tel 949-546-8000 | fax 949-546-8001 | www.abracon.com

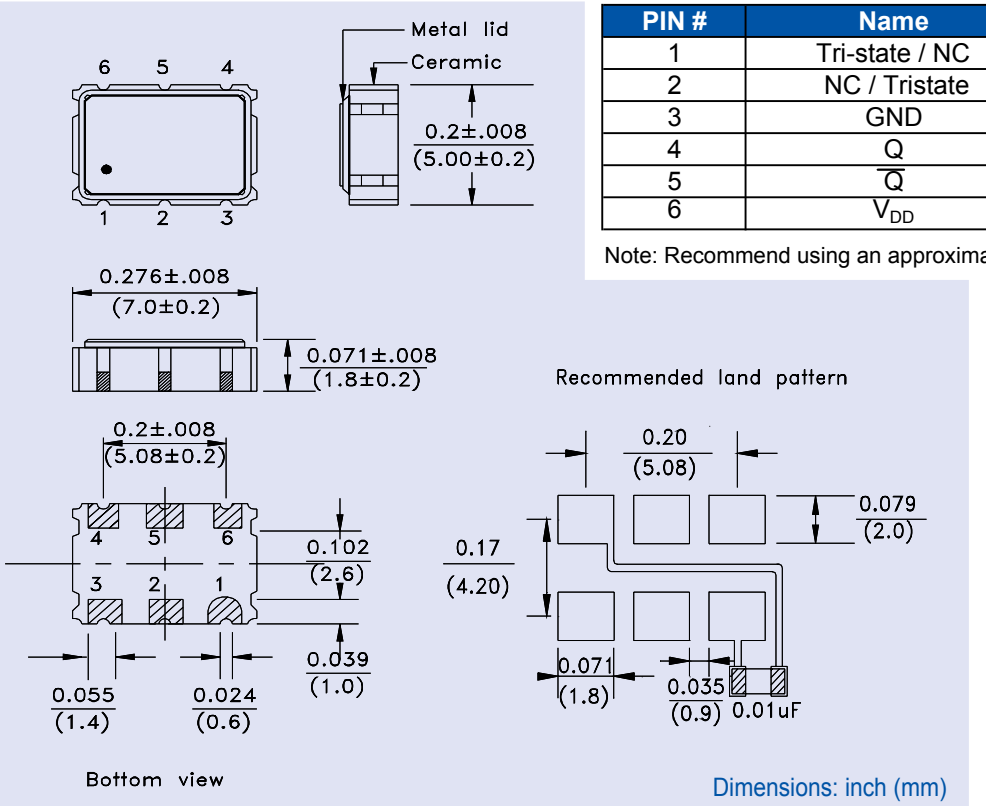
PECL/LVDS/CMOS OUTPUT SMD CRYSTAL CLOCK OSCILLATOR

ALD SERIES

RoHS Compliant

5.0 x 7.0 x 1.8mm

OUTLINE DIMENSIONS:

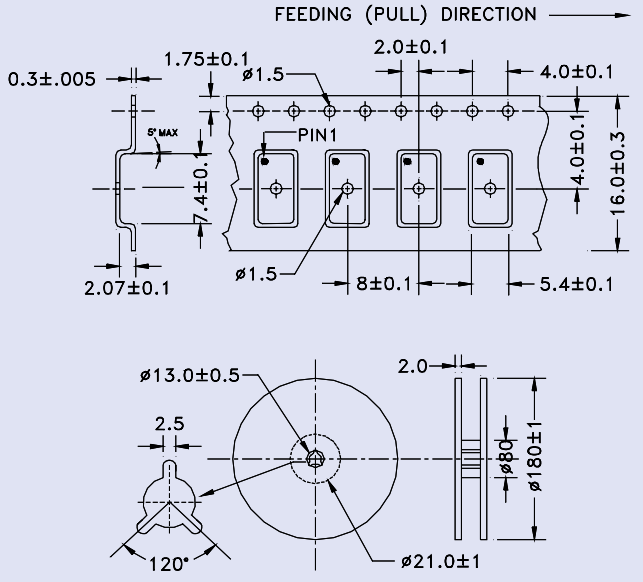


Dimensions: inch (mm)

PIN #	Name	DESRIPTION
1	Tri-state / NC	Tristate or No Connect
2	NC / Tristate	No Connect / Tristate
3	GND	Ground
4	Q	PECL, LVDS, or CMOS Output.
5	$\overline{Q}$	Complimentary PECL,LVDS, or NC.
6	V_{DD}	VDD Connection.

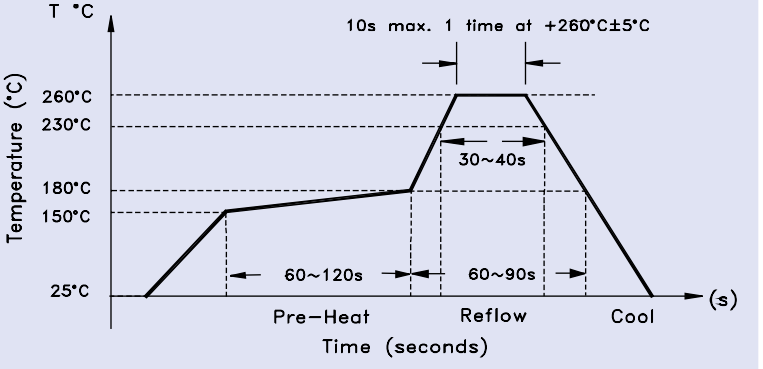
Note: Recommend using an approximately 0.01uF bypass capacitor between PIN 3 and 6.

TAPE AND REEL: T= tape and reel (1,000pcs/reel)



Dimension : mm

REFLOW PROFILE:



NOTE: Abracon manufactured products are intended for general commercial and industrial use. For applications requiring high reliability and/or presenting extreme operating environment, written consent & authorization from Abracon is required.

30332 Esperanza, Rancho Santa Margarita, California 92688
tel 949-546-8000 | fax 949-546-8001 | www.abracon.com