MCTC

CT2500

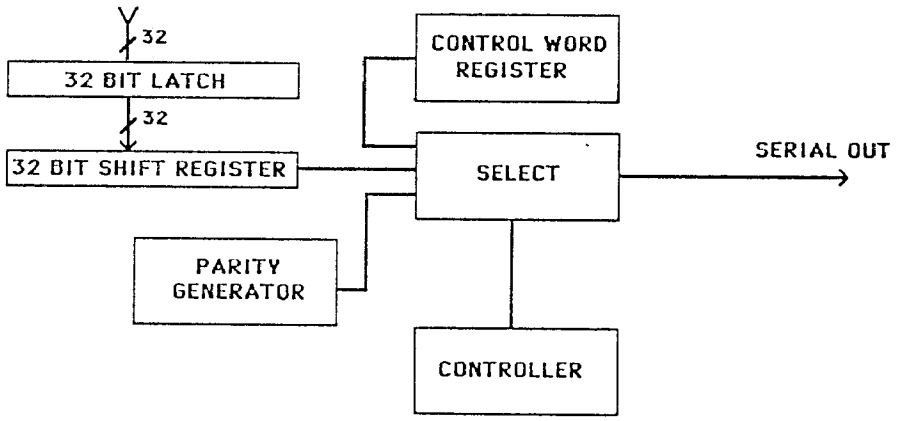
MIL-STD-1397 TYPE D&E
LOW LEVEL SERIAL INTERFACE
PROTOCOL CHIP

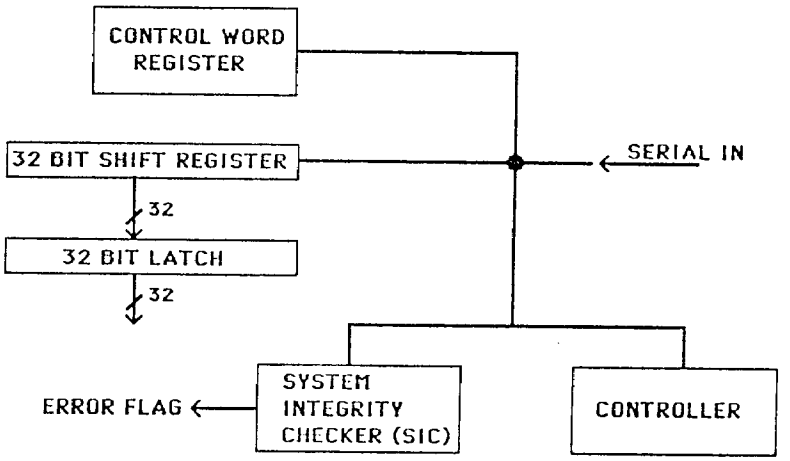
GENERAL DESCRIPTION

The CT2500 provides a complete interface between the MIL-STD-1397 transceiver chip set (CT1698) and most microprocessor based systems. The unit is monolithic and fabricated in CMOS technology, thereby having very low power requirements. The unit handles all protocols of Type D&E interfaces including Burst Mode Data and Forced EF functions.

FEATURES

* Preforms Source and sink functions
* Implements Type D&E protocols
* Burst Mode Capability
* Built in System Integrity Features
* Double Buffered Communications
* Low Power CMOS





I/O CONTROL

The CT2500 is very flexible in it's I/O architecture. The unit can handle 16 bit and 32 bit data and command word loading. In addition, data words can be preloaded into a FIFO and the unit will load data words from the FIFO directly without subsystem intervention. Similarly, data can be received and automatically loaded into a FIFO. This frees up the subsystem until the data transfer is complete. These options are desirable especially when operating under burst mode transmission. Control frames are sent by strobing LDCNTRL and data is sent by strobing STRZ.

DATA TRANSFERS

The CT2500 is built to send and receive Type D and E Control frames. It can transmit and receive 32-bit command and data word. All 32-bit communications are double buffered for maximun flexibility. This allows the subsystem to respond with less critical timing constraints. Burst mode data transmission can be initiated by setting the "Burst Mode" pin high. Automatic FIFO operation is enabled by setting "FIFO IN" pin high. The serial data out is automatically formatted for the CT1698 to send out along the cable.

SOURCE AND SINK MODES

Both Source and Sink Mode operations are available in the CT2500. Selection of modes is accomplished through the Source/ Sink pin. In the Source Mode, the unit will transmit control frames, 32 bit command and data words including burst mode data. It will receive control frames only in Sink mode, the unit will transmit control frames only and receive control frames, 32 bit command and data words, and burst mode data.

SYSTEM INTEGRITY FEATURES

The CT2500 has built in system integrity features. The unit can generate and send parity with all 32 bit transmissions. For reception of 32 bit words, the unit can check for parity , frame, and overrun errors.

1. DESCRIPTION

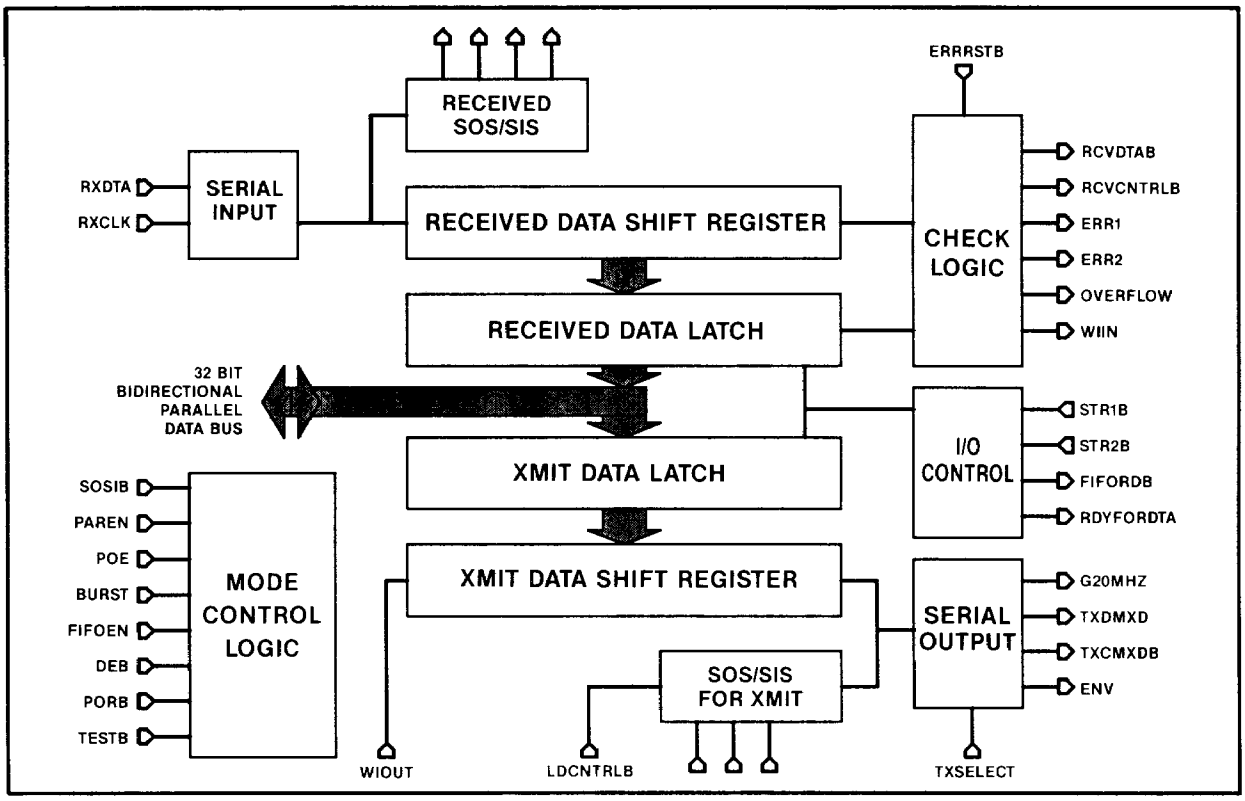
The CT2500 is an interface chip between MIL-STD-1397 low level serial data bus and a 32 or 16 bit parallel data bus and can be used in either a Source or Sink mode. It accepts decoded serial data along with a reconstucted clock from an external Manchester decoder. It delivers NRZ serial data and associated shift clock as well as Manchester encoded bipolar data.

The 32 bit input and output data registers are double buffered with provisions for Burst mode operation as well as direct connection with a FIFO.

The control frame format is selectable between type D and type E protocols.

There is detection circuitry for parity and bit count errors of command and data words

2. BLOCK DIAGRAM



CT2500

3. D.C. ELECTRICAL CHARACTERISTICS (-55 DEG. C TO +125 DEG. C)

SYMBOL	PARAMETER	LIMIT (VDD = 5 V +/- 10%)
Idd	Quiescent current	100 uA max
Iin	Input leakage	10 uA max
Ioz	Tri-state leakage	10 uA max
Vih	Input high level	2.0 V min
Vil	Input low level	0.8 V max
Voh	Output high level	2.4 V min @ Ioh = -4 mA
Vol	Output low level	0.4 V max @ Iol = 4 mA

4. I/O PIN FUNCTION LISTING

NAME	I/O	DESCRIPTION
SOSIB	I	"1" = Source emulation. This mode requires the chip to be able to send 4 bit control frames, 32 bit command and data words, and burst mode data. It must be able to recieve 4 bit control frames. "0" = Sink emulation. This mode requires the chip to be able send 4 bit control frames only. It must be able to recieve 4 bit control frames and 32 bit command or data words, including burst mode.
D0-D31	I/O	32-bit bi-directional data bus for loading or unloading parallel data. Source mode: Input to 32 bit latch. Sink mode: Output (tri-state) from 32 bit latch.
D/EB	I	"1" = All control frames are 3 bits long for D-type interface. "0" = All control frames are 4 bits long for E-type interface.
PAREN	I	"1" = Parity checking/generation enabled. (int. pullup)
POE	I	"1" = Odd parity. (int. pullup) "0" = Even parity.
CLK	I	20 MHZ clock. 50% duty cycle.
BURST	I	"1" Data transmission is under Burst mode. Source mode: All data transmitted will be continuous with no SYNC or WI bits after the initial word. This line must remain stable for the entire duration of the loading and transmission of the data. (Burst mode is only for 32 bit data words; 32 bit command words are only transmitted on a word by word basis.)

NAME	I/O	DESCRIPTION
		Sink mode: All data recieved will be in one block following the SYNC and WI bits with no gaps. Data recieved will be in multiples of 32 bits (including parity when enabled). When a gap is detected, transmission is considered ended. Line must be stable during burst mode reception.
STR1B and STR2B	I	Control strobes for reading and writing the 32-bit data latch. Source mode: STR1B loads the lower 16 bits into the data latch for transmission. STR2B loads the upper 16 bits into the data latch for transmission. Upon completion of STR2B, the entire 32 bits are loaded into the shift register and shifted out. This means means the lower 16 bits must be loaded at or prior to the upper 16 bits. For a normal 32 bit load, STR1B and STR2B are tied together. Sink mode: STR1B reads the lower 16 bits of the recieved data register. STR2B reads the upper 16 bits of the recieved data register. The entire 32 bit latch must be read before reception of the next data word or else the data will be over written. When this occurs, the overflow error flag (OVRFLOW) will go high. The data latch is considered read upon completion of STR2B.
CMDIN	O	Source mode: "1" = Sink device indicates it's ready for command word. Sink mode: "1" = Source device indicates it has a command word.
DTAIN	O	Source mode: "1" = Sink device indicates it's ready for data. Sink mode: "1" = Source device indicates it has data. NOTE: CMDIN and DTAIN are bits from a recieved control frame and are valid after RCVCNTRLB is pulsed low.

NAME	I/O	DESCRIPTION
RCVCNTRLB	O	This signal is pulsed low to indicate a reception of a control frame. This applies to both Sink and Source modes.
RCVDATA	O	This signal is pulsed low to indicate a reception of a 32 bit data or command word. This applies to Sink mode. Error flags are valid after this line is pulsed low.
ERR1 ERR2	O O	ERR2,ERR1 = (0,0) No error. (0,1) Bit error in received data/command or control frame. (1,0) Parity error in received data/command word. (1,1) Sync error in received data/command or control frame
OVRFLOW	O	"1" = Overflow in data register, data not read in time.
RSTERRB	I	This line is pulsed low to reset error flags.
PORB	I	This resets error flags and internal counters.
WIOUT	I	Word Identifier bit Out for the 32 bit word loaded for transmit. "0" = Data Word, "1" = Command/Interrupt Word Source mode: WIOUT is used to identify what type of data is being loaded into the register This line must be valid during STR2B.
WIIN	O	Word Identifier bit Out for the 32 bit word received "0" = Data Word, "1" = Command/Interrupt Word Sink mode: WIIN is used to identify what type of data was received in the register. This line is valid after RCVDTAB is pulsed low. The line is latched at the first RCVDTAB for an entire burst reception.
CMDOUT	I	Source mode: "1" = Have a command word to transmit. Sink mode : "1" = Ready to receive command word.
DTAOUT	I	Source mode: "1" = Have data to send. Sink mode : "1" = Ready to receive data. NOTE: CMDOUT and DTAOUT are bits in the control word sent out back and forth across the line.

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NAME	I/O	DESCRIPTION
LDCONTROLB	I	This loads the status of CMDOUT and DTAOUT into the control frame to be transmitted out. Transmission of this frame will commence when loading is completed. This applies to both Source and Sink modes.
FIFOEN	I	Source mode: A 1 will generate FIFORDB's which will load 32 bits of data into the data latch for transmission as long as it is empty (RDYFORDTA=1). For non-burst (single word) transmission, FIFOEN must be removed before RDYFORDTA comes back. A positive pulse of 100 ns duration satisfies this requirement. Sink mode : The parallel data bus, D0-D31, is active during the RCVDTAB signal and will hold for approx 25 ns after its rising edge. With a FIFO directly connected to the data bus, RCVDTAB can be used to load all data and command words into the FIFO. Gating RCVDTAB with WI selects only data words for loading into the FIFO.
FIFORDB	O	Source mode: Output control signal from the chip to read data from the FIFO and load it into the data latch. Sink mode: Not used. Must remain unconnected.
RDYFORDTA	O	"1" = Data input latch is empty and ready for data to be loaded in. This applies to Source mode only.
ENV	O	"1" = There is a transmission occuring on serial bus.
TXDMXD	O	Serial Data out / Manchester encoded Data out.
TXCMXDB	O	Serial Clock out / Manchester encoded Databar out.
GATED20MHZ	O	Gated 20MHZ signal used to generate Manchester data with TXD and TXCLK when TXSELECT = "0".

NAME	I/O	DESCRIPTION
TXSELECT	I	"0" = Configures TXDMXD and TXCMXDB for serial data and clock. (int. pulldown) "1" = Manchester Data and Databar appear on TXDMXD and TxcMXDB.
RXDATA	I	Serial received Data in.
RXCLOCK	I	Serial received Clock in.
TESTB	I	"0" = Internal wrap-around test. TXDATA and TXCLOCK are internally connected to RXDATA and RXCLOCK, bypassing the external channel. The chip must be in Source mode and only 32 bit data loads and reads are allowed. In this test mode, STR2B will be used to load a full 32 bit word for transmission. When this word is wrapped back, RCVDTAB will pulse low indicating a reception of a data or command word. STR1B will allow the contents of the received data latch to be read out. The sending and receiving of control frames can also be tested. They do not require any redefinition of pin functions in test mode.
BIT4	O	Fourth bit of received E type control frame.
BITOUT	I	Fourth bit of transmitted E type control frame. (int. pullup)
SYNCIN	O	Output of the sync bit position of the received data latch
CFRMSYNC	O	Output of the sync bit position of the received control frame latch.
PRTYIN	O	Output of the parity bit position of the received data latch.
POWER	S	
GROUND	S	

5. TIMING DIAGRAMS

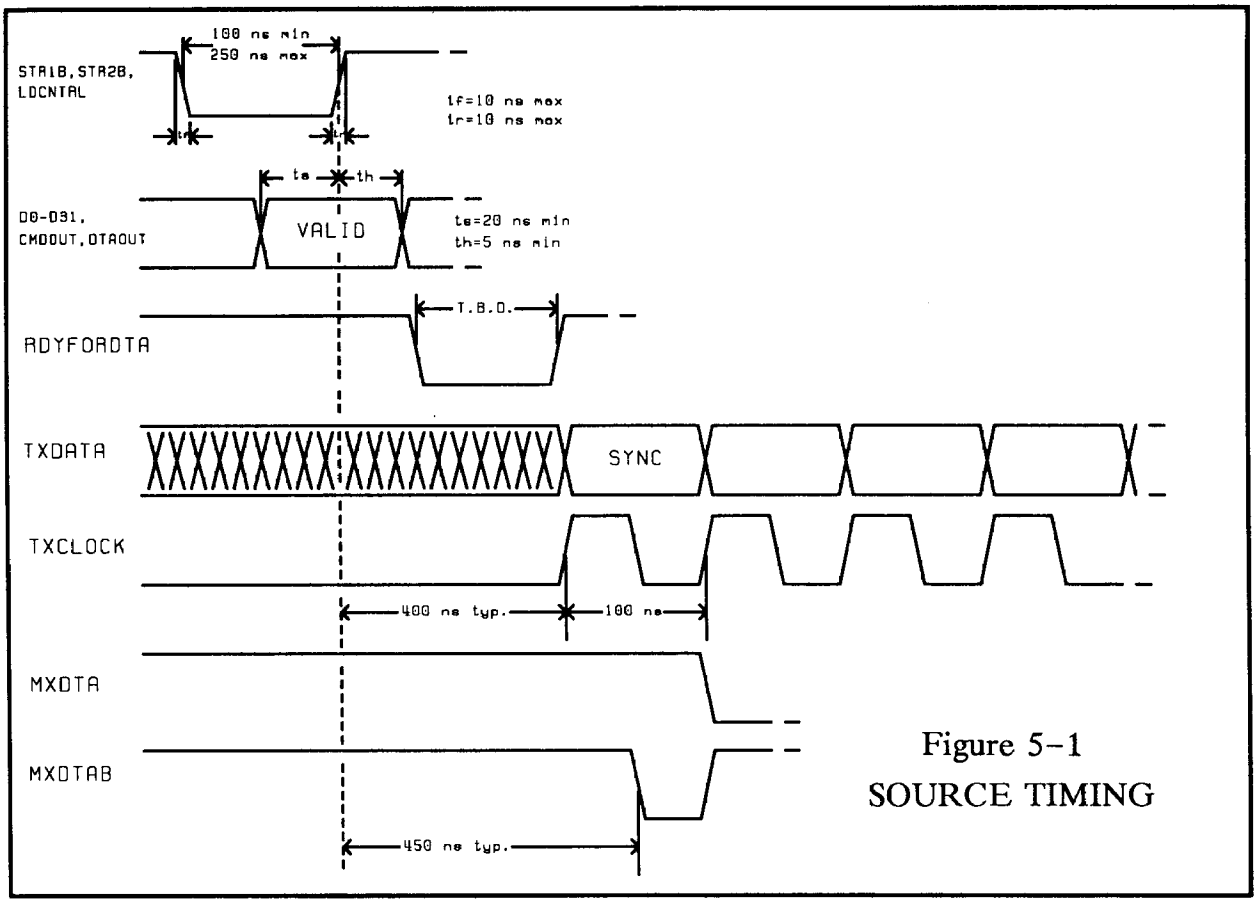


Figure 5-1
SOURCE TIMING

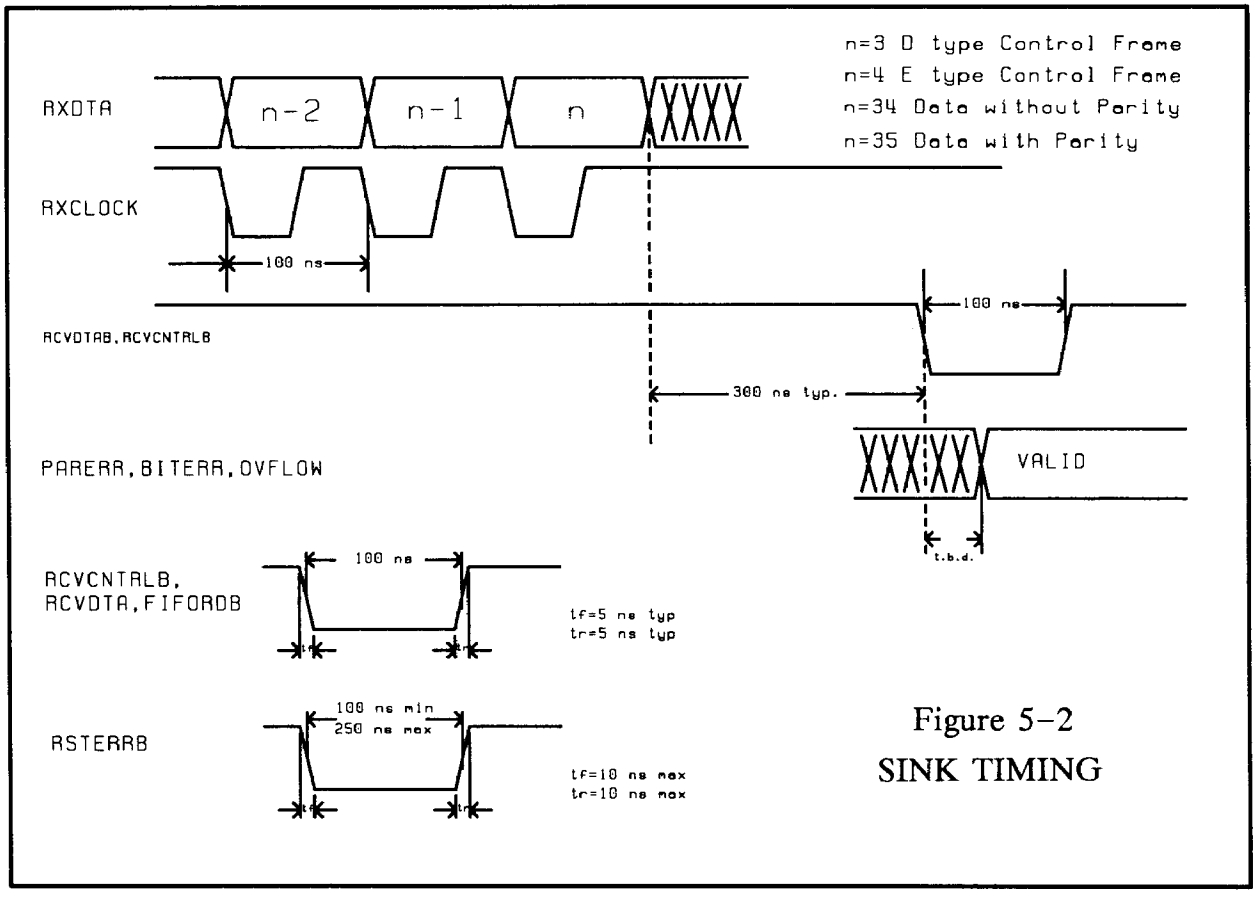


Figure 5-2
SINK TIMING

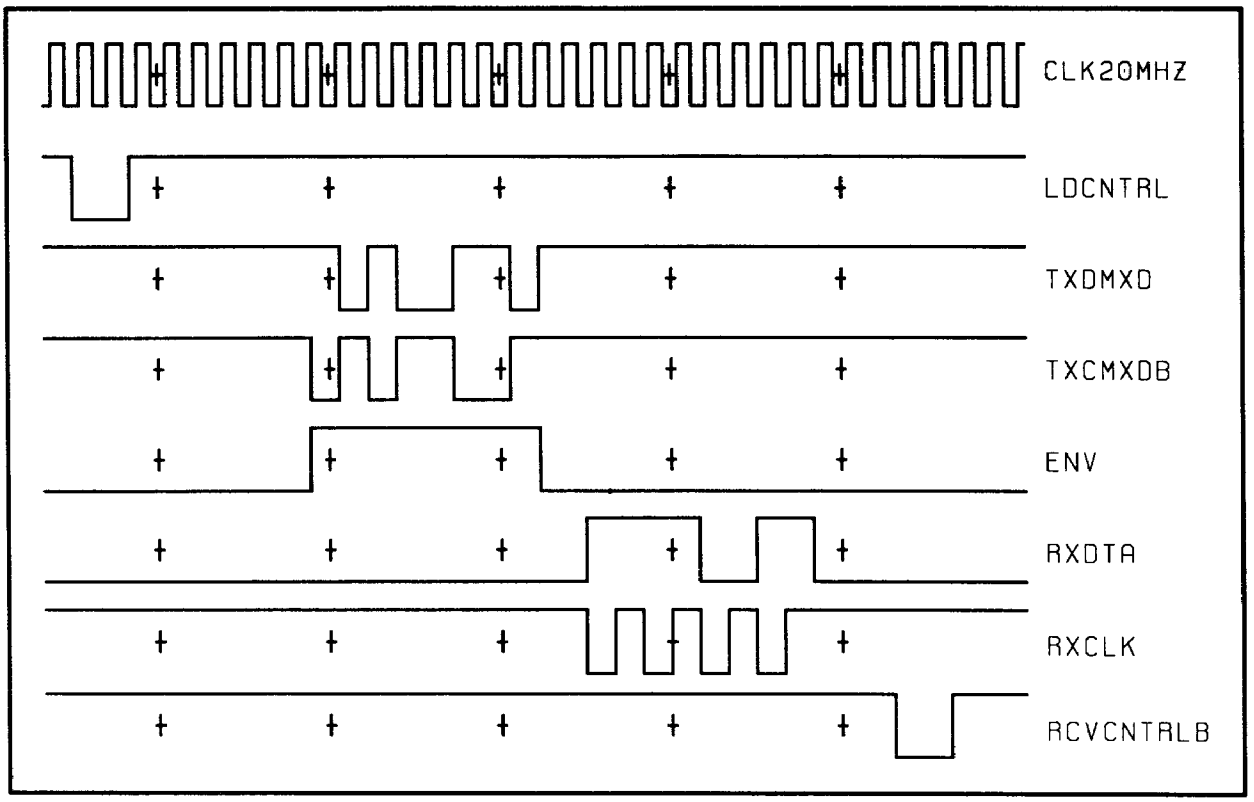


Figure 5-3 CONTROL FRAME TRANSFER

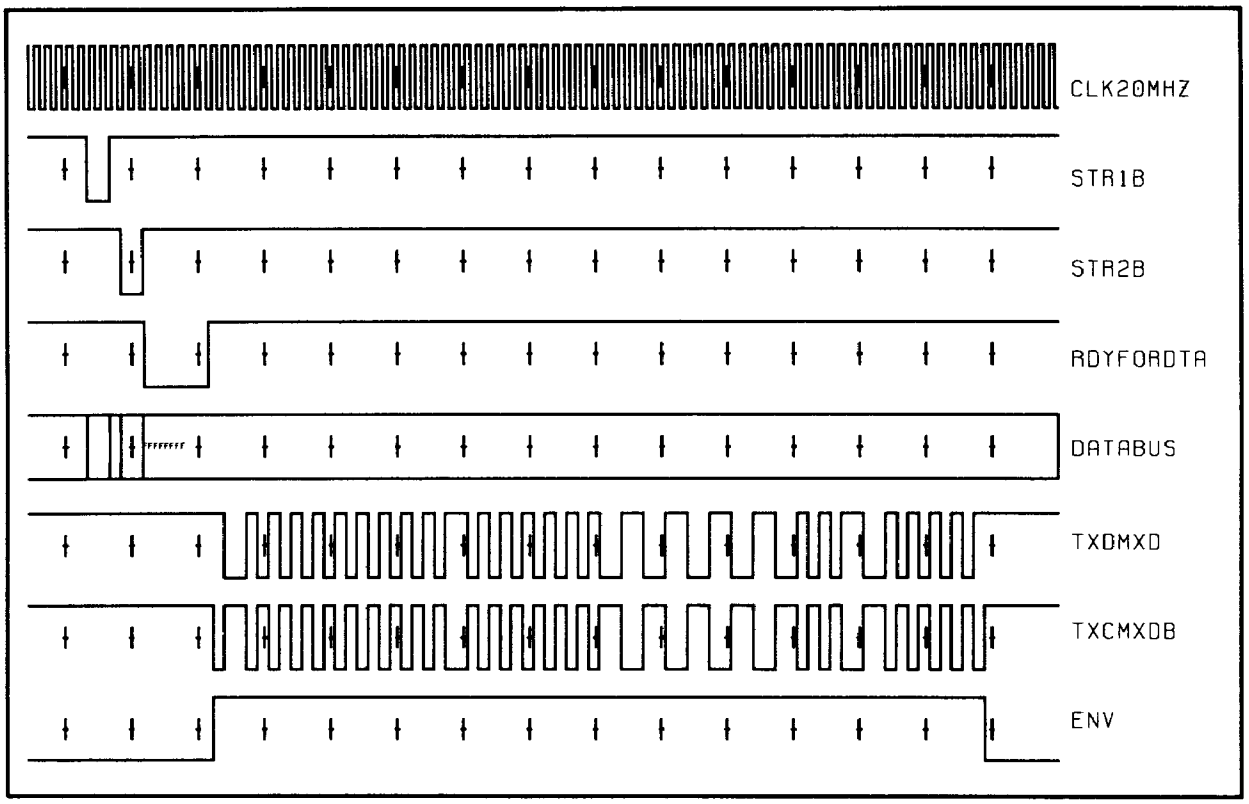


Figure 5-4 SOURCE DATA FRAME EXAMPLE

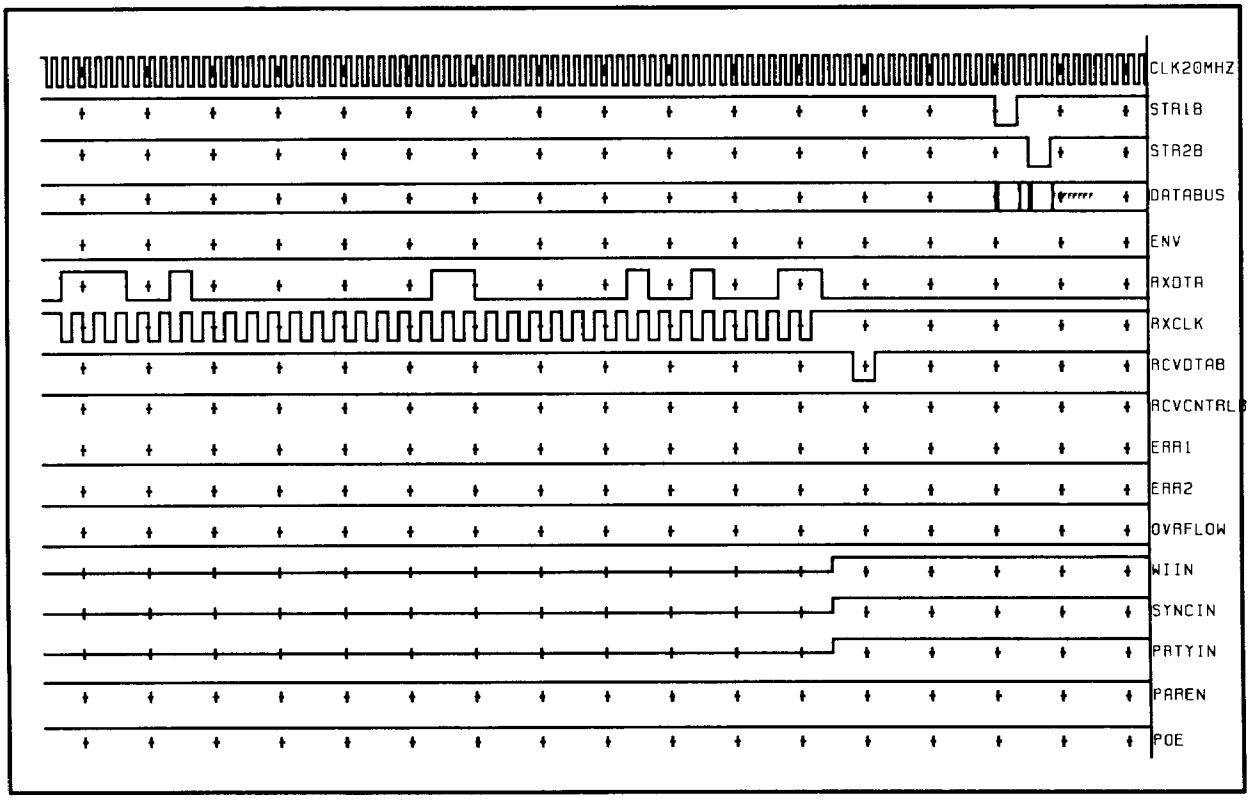


Figure 5-5 SINK DATA FRAME EXAMPLE

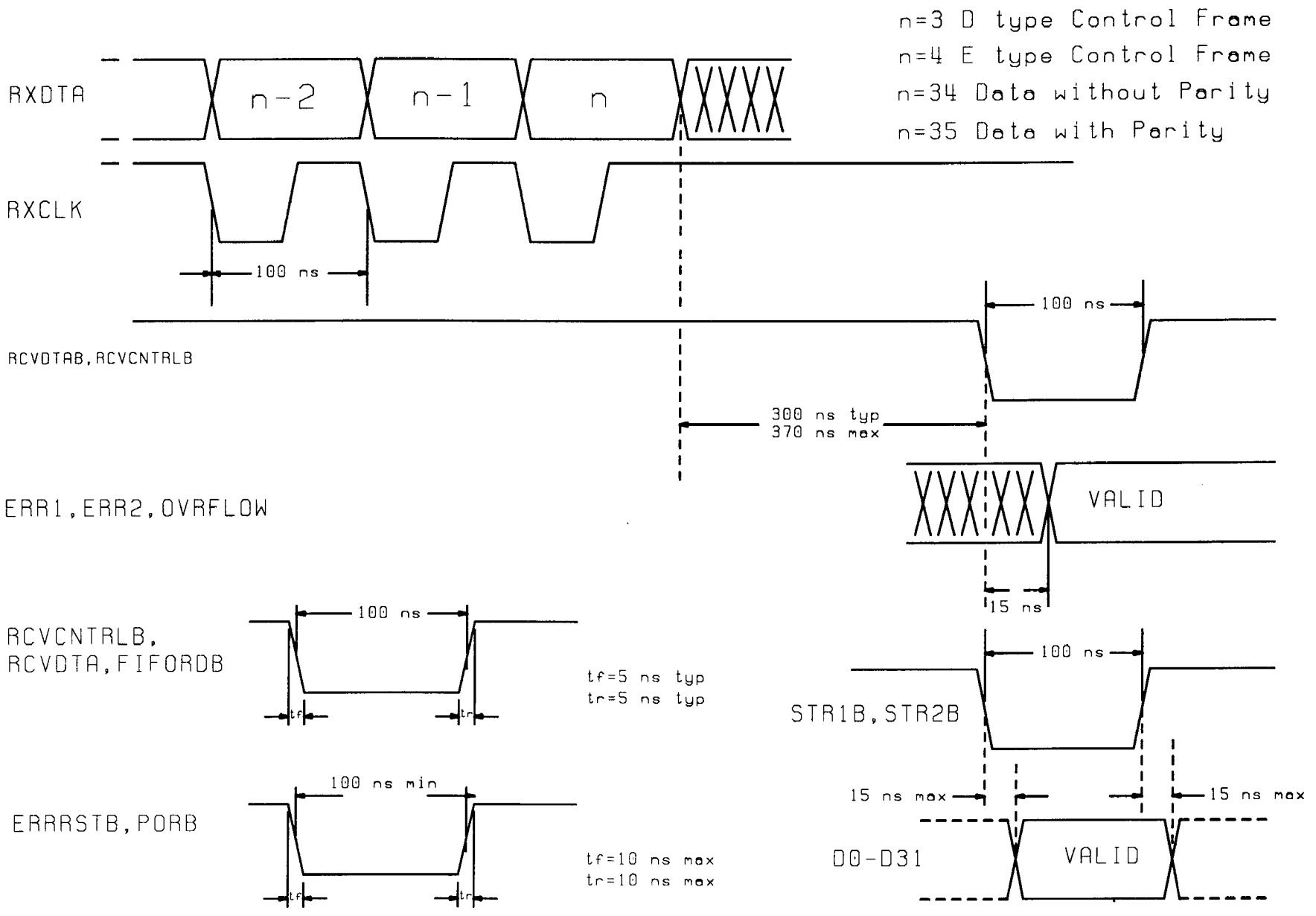


FIGURE 5-6 I/O TIMING DIAGRAM

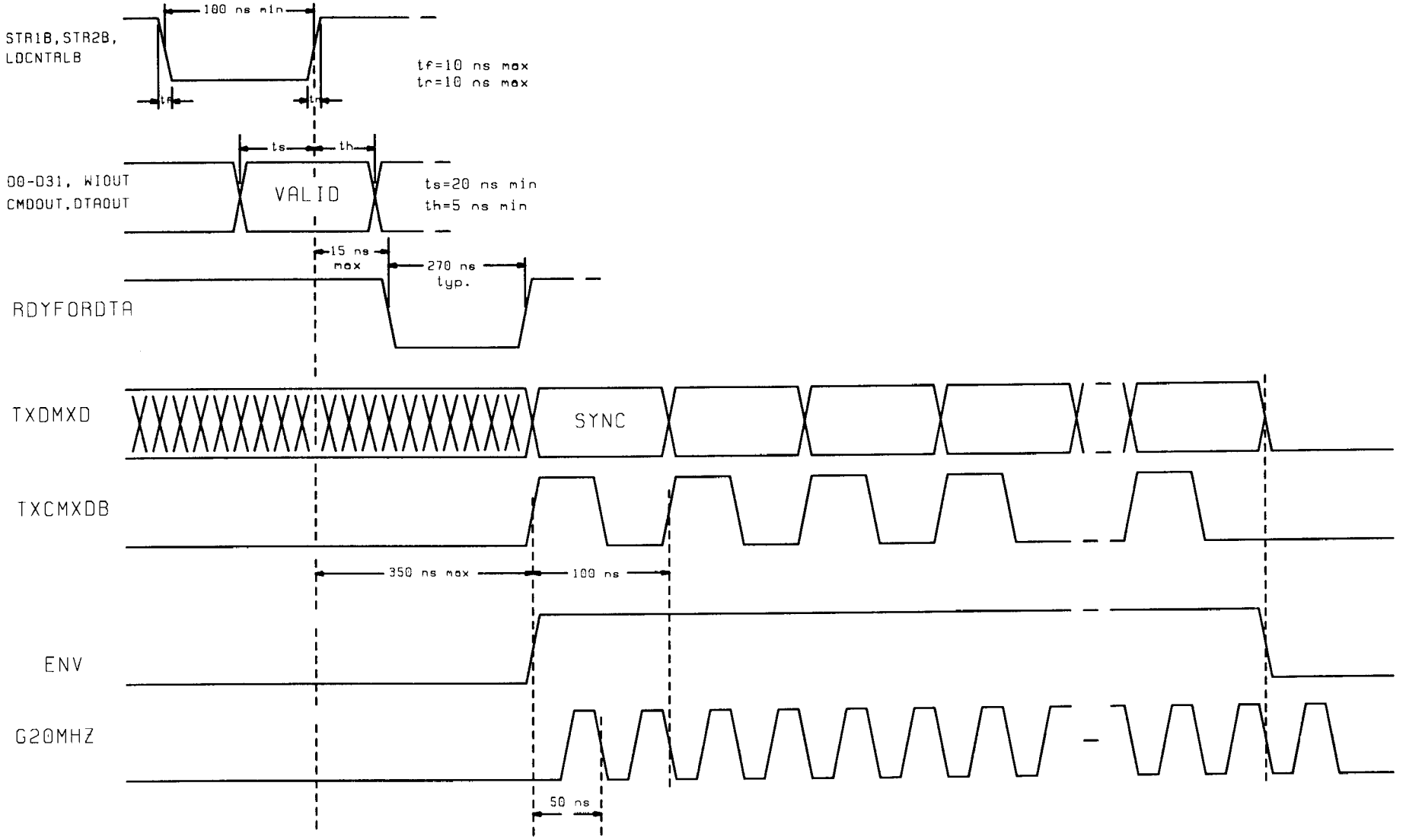


FIGURE 5-7 I/O TIMING DIAGRAM

MARCONI CIRCUIT TECHNOLOGY

CT2500 PINOUTS (84 PGA)

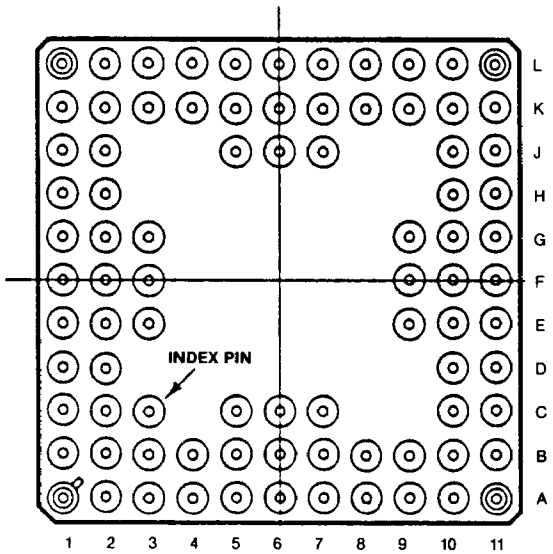
PIN	SIGNAL
B2	BURST
C2	CLK [20 MHZ]
B1	CMDOUT
C1	DTA OUT
D2	BIT4 OUT
D1	ERR RST –
E3	FIFO EN
E2	LDCNTRL –
E1	POR –
F2	GND
F3	GND
G3	SYNC IN
G1	RXCLK
G2	RXDTA
F1	SOS/SIS –
H1	STR1 –
H2	STR2 –
J1	TEST –
K1	WI OUT
J2	D31
L1	CFRMSYNC
K2	VDD [+5 VOLTS]
K3	PAREN
L2	D30
L3	D29
K4	D28
L4	D27
J5	D26
K5	D25
L5	D24
K6	BIT4
J6	VDD [+5 VOLTS]
J7	VDD [+5 VOLTS]
L7	D23
K7	D22
L6	D21
L8	D20
K8	D19
L9	D18
L10	D17
K9	D16
L11	GND
K10	GND
J10	POE
K11	D15
J11	D14
H10	D13
H11	D12
F10	D11
G10	D10
G11	D9
G9	GND
F9	GND
F11	D8

PIN	SIGNAL
E11	D7
E10	D6
E9	D5
D11	D4
D10	D3
C11	D2
B11	D1
C10	PRTYIN
A11	VDD [+5 VOLTS]
B10	VDD [+5 VOLTS]
B9	D/E –
A10	D0
A9	CMDIN
B8	DTAIN
A8	ENV
B6	ERR1
B7	ERR2
A7	FIFORD –
C7	VDD [+5 VOLTS]
C6	VDD [+5 VOLTS]
A6	TXSELECT
A5	OVRFLOW
B5	RCVCNTRL –
C5	RCVDTA –
A4	RDYFORDTA
B4	TXCMXDB
A3	TXDMXD
A2	WIIN
B3	GATED 20 MHZ CLK
A1	GND

CT2500

PACKAGE INFORMATION

84-PIN CERAMIC PIN GRID ARRAY



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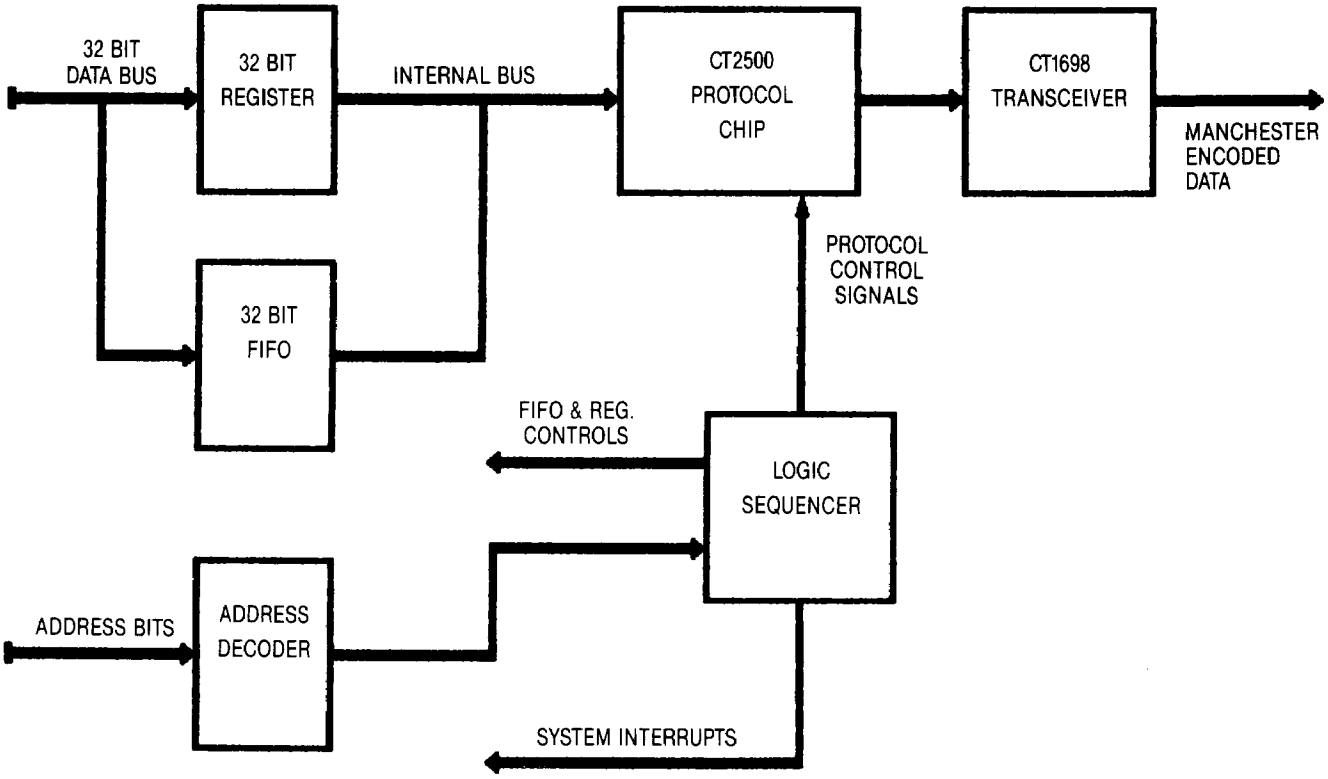
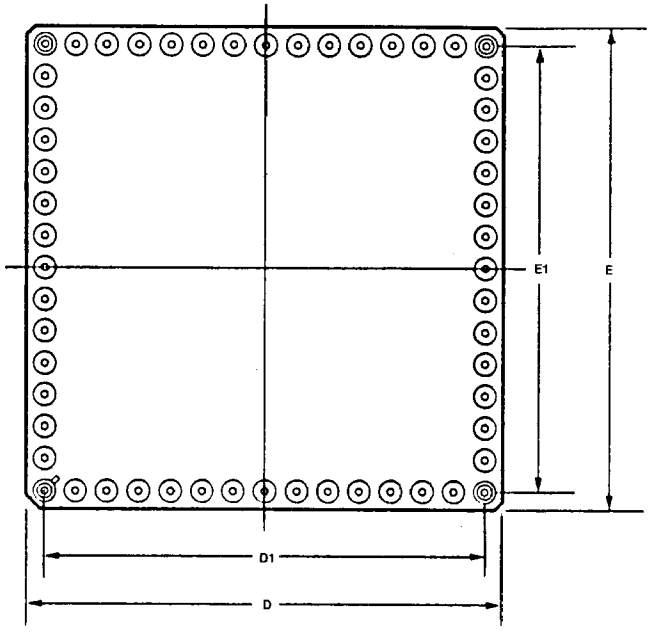
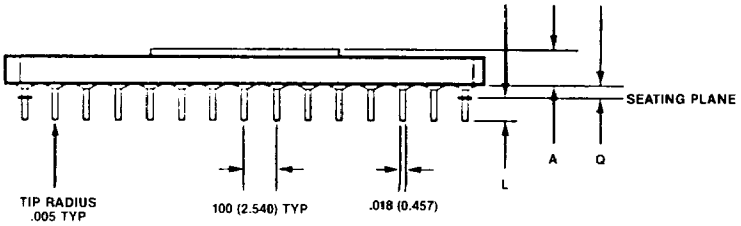
CT2500 (SOURCE AND SINK MODE)
TYPICAL I/O BOARD CONFIGURATION





PACKAGE INFORMATION

CERAMIC PIN GRID ARRAY PACKAGE OUTLINE



Dimensions in Inches (Millimeters)

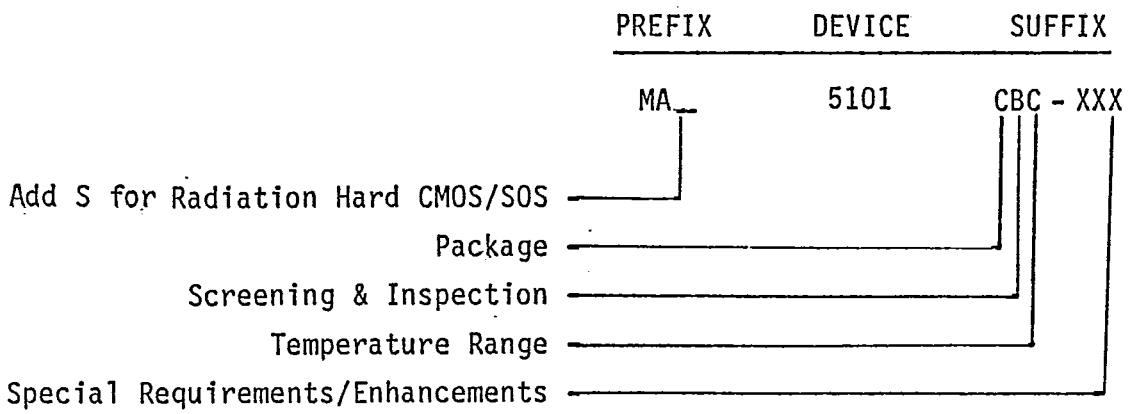
CERAMIC PIN GRID ARRAY

Pin Count	Matrix	Cavity Position	A		D (E)		D1 (E1)		Q	L
			Min	Max	Min	Max	Min	Max	Ref	Ref
84	11 x 11	Up	.0800 (2.032)	.1000 (2.540)	1.080 (27.43)	1.120 (28.45)	0.990 (25.15)	1.010 (25.65)	0.050 (1.270)	0.130 (3.302)

Marconi Circuit Technology Corporation
45 Davids Drive, Hauppauge, New York 11788
(516) 231-7710/FAX: (516) 231-7923

10/89-1M

MARCONI ELECTRONIC DEVICES, INC



PACKAGE

A. Pin Grid Array
C. Ceramic DIL
E. Epic
F. Flat Pack
G. Cerdip
L. Leadless Chip Carrier
M. Module
N. Naked Die
P. Plastic DIL
Q. Quad Plastic J-Lead
R. Qual Cerpack J-Lead
S. SO Plastic
X. Special

TEMPERATURE RANGE

A. Special
B. 0 to 70°C
C. -55 to +125°C
D. -25 to +70°C
E. -25 to +85°C
F. -40 to +85°C
G. -55 to +85°C
H. -40 to +125°C
J. -10 to +80°C
K. 0 to +200°C

SCREENING & INSPECTION

B. Mil Std-883C Class B
G. Commercial Hermetic
L. Commercial Plastic
S. Mil Std-883C Class S
T. ESA9000
X. Special

45 DAVIDS DRIVE • HAUPPAUGE, N.Y. 11788 • Phone: (516) 231-7710 • Fax: (516) 231-7923 • Telex: 275801