VM5353
DATA SEPARATOR

VTC Inc.
Value the Customer™

960801

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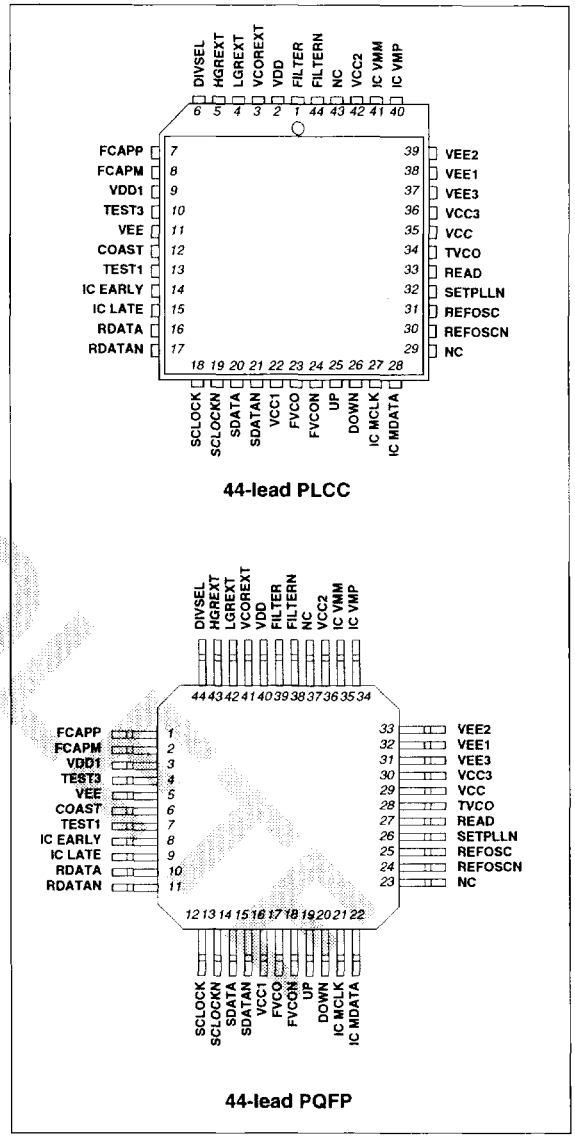
FEATURES

- Operates at Data Rates from 10 to 48 Mbits/sec (2,7) Code
- Operates at Data Rates from 10 to 64 Mbits/sec (1,7) Code and (0,3) Codes
- Static Window Error Less Than 500 pS
- Zero Phase VCO Restart for Rapid Data Lockup
- Internal Silicon Delay Line
- Compatible with Zoned Density Recording Applications
- Contains Internal Window Marginalization Circuitry
- User Determined PLL Loop Filter Network
- Dual Gain PLL With External Control of PLL Loop Bandwidth
- PLL Free Run (Coast) Control
- Power Dissipation Less Than 1W
- VM5353 has Power Supplies of +5V and +12V

DESCRIPTION

The VM5353 is an integrated circuit designed to be used in high-performance data recovery systems. The data separator is a phase locked loop which provides a stable read clock of up to 96 MHz for system timing during the disk readback operation. It tracks the slow variations in the data frequency while eliminating noise and peak shifting in the data. The circuit will operate with either the (2,7), (1,7) or (0,3) RLL codes. The VM5353 uses the high-speed CBP (Complementary Bipolar Process).

CONNECTION DIAGRAM



44-lead PLCC

44-lead PQFP

TAPE DRIVE CIRCUITS

ABSOLUTE MAXIMUM RATINGS

VM5353

Storage Temperature ..... -65° to +150°C
Ambient Operating Temperature ..... 0° to +70°C
Junction Operating Temperature ..... 0° to +125°C
Supply Voltage,
V_{CC} (V_{EE} = 0V, V_{DD} = 12V) ..... -0.5V to +6.5V
Voltage Applied to
TTL Inputs (V_{EE} = 0V) ..... -0.5V to V_{CC} +0.5V
ECL Inputs (V_{EE} = 0V) ..... 0 to V_{CC}
ECL Output Current - Continuous 25mA
- Surge 50mA
Maximum Power Dissipation 1300mW
Thermal Impedance, 44-lead PLCC
Junction-to-Case, Θ_{JC} ..... 10°C/W
Junction-to-Ambient, Θ_{JA} ..... 53°C/W

READ OPERATION

There are three states in the read PLL locking sequence:

1. Lock to the reference oscillator
2. Lock to the preamble data in high gain
3. Lock to data in low gain.

Initially, the data separator locks to the REFOSC input. This is a standby state which the data separator is in when not reading data. The VCO runs at a frequency which is very close to that required when locking to the data stream. This minimizes the frequency step when the PLL input is switched to data. In this state of operation, the phase detector is in the phase/frequency mode which guarantees non-harmonic lock up. The charge pump is sourcing high-gain currents. The higher loop gain ensures rapid lock of the PLL.

The assertion of the READ gate initiates the read operation. Internally, the part waits for the first data bit and then switches the input to the PLL from REFOSC to RDATA. At this time, the VCO is momentarily stopped and restarted in phase with the first data bit in the preamble. This allows very fast and repeatable lockup to the preamble field. The loop is still in a high gain mode so any remaining phase error is due to the zero phase restart is quickly tracked out. The phase detector is in a phase mode which allows the PLL to lock to harmonics. This also allows great flexibility in the preamble pattern. The user could actually lock up in the middle of a data field if so desired. The length of the preamble lock is controlled externally by the SETPLLN input.

After the preamble lock-up is over, the PLL switches to the lock-to-data mode and the data is read. In this mode, the charge pump is sourcing low-gain currents. This forms a low-gain loop which is desirable for reading data. The loop becomes less responsive to bit shift in the data stream.

When the read operation is complete, READ gate is brought high, a zero phase restart of the VCO is performed and the PLL locks to the reference oscillator once again. Refer to Figure 1 for Read Timing Diagrams.

CIRCUIT BLOCK DESCRIPTION

The circuit is composed of the following functional blocks: high-precision phase-frequency detector, differential charge pump, differential input VCO, filter, zero phase VCO restart, divider, data standardizer and synchronization control block. Refer to the block diagram.

SYNC Control

The sync control block controls the input multiplexer, the phase/frequency detector, the charge pump gain and the divider setting. It guarantees that the phase locked loop switches smoothly from one mode to another. The control pin setting and corresponding modes are summarized in the table below.

READ	*SETPLLN*	*GAIN*	*MUXSEL*	*DIVIDER*	*PHASE/FREQ DET*
1	X	High	REFOSC	div by 4	Phase/Freq. Mode
0	X	Low	DATA	div by 2	Phase Mode
1	X	High	REFOSC	div by 4	Phase/Freq. Mode
0	1	High	DATA	div by 2	Phas Mode
0	0	Low	DATA	div by 2	Phase Mode

1 = Logic HI, 0 = Logic LO, X = Don't Care

This table shows that the high-to-low gain switch is controlled externally by the SETPLLN pin. The above table assumes that DIVSEL is LO, meaning that the extra divide-by-two is not in the VCO feedback path.

Delay Line

The VM5353 uses an internal delay line to delay the data coming into the phase detector. The delay allows the phase detector to anticipate incoming data and enable a phase comparison to occur. The delay is nominally one half of the REFOSC period. A separate control loop regulates the propagation delay through the delay line by comparing it to the REFOSC frequency. This delay line configuration relies only on the REFOSC frequency and is insensitive to external components, supply voltage, temperature and IC processing. It requires that the reference oscillator frequency be present at all times and that there be no extended gaps in the data when READ gate is active.

Data Mux and Phase/Frequency Detector

The two highest frequency inputs to the data separator are the REFOSC and the RDATA pins. The REFOSC pin is tied to an external reference oscillator or servo reference. The PLL locks to the REFOSC input when no data is being read from the disk. The REFOSC signal must be present all times because it is used in the anticipator delay circuitry. The RDATA pin is the input for the raw data and is tied to the output of the pulse detector circuit in the disk drive. Because these two signals are the highest frequencies coming onto the chip, they are differential ECL inputs. This helps reduce unwanted coupling of these signals into the PLL. A multiplexer DATA MUX is used to select which input (REFOSC or RDATA) the PLL will lock to.

The output of the anticipator delay goes to the PLL input of the phase/frequency detector (PFD) block. The phase/ frequency detector has two modes of operation, the phase/frequency mode and phase mode. Each mode is described below.

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The phase/frequency mode allows the phase detector to detect both phase and frequency of the two incoming signals. This mode does not allow the PLL to lock to harmonics of the reference input. The phase/frequency mode is used along with the charge pump high gain mode and the filter high bandwidth mode to form a high gain-high bandwidth loop for fast lock up times. This mode is used when locking to the reference oscillator and the preamble. The reference input to the PFD initiates an UP signal to the charge pump, and the VCO feedback input initiates a DOWN signal to the charge pump. When both UP and DOWN are high, the internal flip-flops are reset and the signals return low again. The minimum pulse width of the UP and DOWN signals is determined by internal propagation delays and is approximately 5 ns. In a locked state, the rising and falling edges of the UP and DOWN signals are coincident and there is no net effect on the PLL phase and frequency.

When in the phase mode, the PFD detects only the phase of the two inputs. The phase mode is used whenever READ gate is asserted. The anticipator delay value is one half a REFOSC period window and is used to condition the phase detector for a phase comparison. The operation of the phase detector is the same as in the phase/frequency mode except that a phase comparison cannot be initiated until a data pulse is input to the phase detector. This allows to the PLL to lock to harmonics of the VCO frequency.

Charge Pump

The charge pump uses high speed NPN and PNP switches to source current in and out of the FILTER pin. The UP and DOWN signals from the phase detector feed into the charge pump and cause it to pump current in or out of the differential lead-lag filter. The high speed current switches in the charge pump sink or source current out of the FILTER pin, as determined by the UP and DOWN inputs. The FILTERN side of the filter acts as a voltage source. The high and low gain current are set by external resistors connected to the HGREXT and LGREXT pins. The high gain current can be varied from 0.5 to 2.0 mA by adjusting the HGREXT resistor. The low gain current can be varied from 100 to 400 µA by adjusting the LGREXT resistor. This allows the user to vary the high gain/low gain current ratio from 20:1 to 5:4.

Filter

The filter resides external to the chip, allowing the system designer to control the loop dynamics. It is composed of two capacitors and one resistor. Refer to the VM5351/VM5352/VM5353 Application Note.

VCO

The VCO is a multivibrator type oscillator which has good linearity over its frequency range. The differential voltage between the FILTER and FILTERN pins controls the VCO frequency. The VCO center frequency occurs when the differential voltage across FILTER and FILTERN is zero. An external resistor tied from the VCOREXT pin to VEE sets the VCO center frequency and gain.

Divider

The divider block divides down the VCO frequency. It is composed of several divide-by-two sub blocks which can be switched in and out. The VCO frequency is split into to separate signals which are divided down individually. One of the divided VCO signals is routed to the data standardizer. This is a straight divide-by-two at all times. The other divided VCO signal wraps around back into the phase-frequency detector to complete the loop. This division is switchable from a divide-by-two to a divide-by-four. The VCO divided-by-two is used when the phase-frequency detector is in the phase (harmonic) mode. The VCO divided-by-four is used when the phase-frequency detector is in the phase-frequency mode and the PLL is locking to REFOSC. This matches the REFOSC divided-by-two frequency. Refer to the block diagram.

The DIVSEL pin can be used to insert an extra divide-by-two into the front end of the divider block to extend the lower end of VCO range without changing the VCOREXT resistor. This is used when operating at lower data rates ($f \leq 15$MBS).

The divider block can be put into a test mode by forcing the TEST1 pin to a logic low. This switches an internal mux that allows an external frequency to be injected into the divider through the TVCO input pin.

Data Standardizer

The divided VCO clock and data input to the PLL contain clock and data information needed but are not synchronized to one another. For this reason, they are put through a data standardizer which takes out any bit shift in the data and puts the bit in a decode window. The data standardizer uses the falling edge of the divided VCO clock to generate the decode window. The rising edge of the clock output SCLOCK is centered in the middle of the synchronized data output SDATA. The rising edge of the SCLOCK indicates the data is valid and clocks the data bit into the decoder circuitry of a decoder IC. The SCLOCK and SDATA outputs are differential ECL signals. A Synchronized Data and Clock Timing Diagram is shown in Figure 2.

Zero Phase Restart

A zero phase restart of the VCO is performed both when switching from the reference oscillator to data and vice versa. The loop is in a high gain mode whenever a zero phase restart occurs. This allows fast lockup to the preamble field and when going back to the idle state. The zero phase restart block interfaces to several other blocks on the chip and guarantees a sequence of events when the switch happens. No spurious data or clock signals will occur when READ gate is switched. Timing diagrams for the VCO Zero-Phase Restart are shown in Figure 3.

Zoned Density Recording

The VM5353 can be used with zoned density recording. The synthesized frequency is brought into the REFOSC input. Different values for the VCOREXT resistor must be switched in and out using an external analog switch when changing the VCO center frequency. A zero temperature coefficient current DAC will not work well to set up the VCO center frequency. This is because the VCO requires a negative temperature coeficient current to give a constant VCO frequency over temperature.

PIN DESCRIPTIONS

DIGITAL INPUTS:

REFOSC, REFOSCN: Reference oscillator which the PLL locks to when in the idle state. A differential ECL input. REFOSC frequencies for the different data rates and codes are:

DATA RATE - f	*1/2 (2,7) - 2f*	*2/3 (1,7) - 1.5f*
64 Mbits/sec	—	96 MHz
48 Mbits/sec	96 MHz	72 MHz
30 Mbits/sec	60 MHz	45 MHz
25 Mbits/sec	50 MHz	37.5 MHz
20 Mbits/sec	40 MHz	30 MHz
15 Mbits/sec	30 MHz	22.5 MHz
10 Mbits/sec	20 MHz	15 MHz

REFOSC minimum pulse width high and low: 4ns. The duty cycle of REFOSC is not critical.

RDATA, RDATAN: Encoded read data from the disk drive read channel, active high. RDATA minimum pulse width: 4ns. A differential ECL input.

READ: A TTL control input which when low initiates lock up to data. When high, the PLL is in an idle state and locks to the REFOSC signal.

SETPLLN: A TTL input which when activated in conjunction with READ gate determines the bandwidth mode of the PLL.

COAST: A TTL input which controls the coast function on the data separator. When the coast input is a logic low, the phase detector is cleared and held in a reset state, allowing the VCO to coast regardless of the incoming data. This happens synchronously within the circuit. When a logical high, the phase detector operates normally.

COAST	MODE
Tied to V_{EE}	VCO coast
Floating	Normal operation

DIVSEL: An input used to switch in and out an extra divide-by-two in the VCO divider block. The extra divide by two can be used to extend the low end frequency range of the VCO.

DIVSEL	MODE
Tied to V_{EE}	Extra divide by two switched out. (f_o above 60MHz)
Floating	Extra divide by two switched in. (f_o below 60MHz)

TEST1: An input used to enable a test feature on the data separator. When enabled, it allows an external VCO frequency signal to be injected into the divider block through the TVCO pin. For test purposes only.

TEST1	MODE
Tied to V_{EE}	External VCO frequency injected into divider block.
Floating	Normal operation

TEST3: An input used to enable a test feature on the data separator. When enabled, it forces the phase detector into a phase-frequency detector at all times. For test purposes only.

TEST3	MODE
Tied to V_{EE}	Phase detector in phase frequency mode at all times.
Floating	Normal operation

TVCO: The test VCO input pin. This input is enabled by the TEST1 control pin. This is a TTL input.

DIGITAL OUTPUTS:

SDATA, SDATAN: Encoded data read from the disk which is synchronous with the falling edge of the Data Clock. SDATA is active high. These pins are open emitter differential outputs requiring an external 511Ω pull down resistor to V_{EE} when in active use. A differential ECL receiver should be used to receive the signal.

SCLOCK, SCLOCKN: Data clock output referenced to the VCO which is synchronous with the Synchronized Data. The rising edge of SCLOCK indicates the presence of valid data on SDATA. These pins are open emitter differential outputs requiring an external 511Ω pull down resistor to V_{EE} when in active use. A differential ECL receiver should be used to receive the signal.

FVCO, FVCON: Output frequency of the VCO available for data decoding. These pins are open emitter differential outputs requiring an external 511Ω pull down resistor to V_{EE} when in active use. The outputs should be allowed to float when not needed. A differential ECL receiver should be used to receive the signal.

Nominal FVCO output frequencies for the specified data rates and coding schemes are given below.

DATA RATE - f	*DIVSEL*	*1/2 (2,7) - 4f*	*2/3 (1,7) - 3f*
64 Mbits/sec	V_{EE}	———	192 MHz
48 Mbits/sec	V_{EE}	192 MHz	144 MHz
30 Mbits/sec	V_{EE}	120 MHz	90 MHz
25 Mbits/sec	V_{EE}	100 MHz	75 MHz
20 Mbits/sec	V_{EE}	80 MHz	60 MHz
15 Mbits/sec	Float	60 MHz	45 MHz
10 Mbits/sec	Float	40 MHz	30 MHz

When DIVSEL is low, the FVCO pin outputs the actual frequency of the internal VCO frequency divided by two.

UP: Active high whenever the phase detector issues a pump up to the charge pump. This pin is an open emitter ECL output requiring an external 511Ω pull down resistor to V_{EE} when in active use. The output should be allowed to float when not needed.

DOWN: Active high whenever the phase detector issues a pump down to the charge pump. This pin is an open emitter ECL output requiring an external 511Ω pull down resistor to V_{EE} when in active use. The output should be allowed to float when not needed.

ANALOG PINS:

VCOREXT: Used to bias up the current source that sets the VCO center frequency f_o. An external resistor is tied from this pin to the most negative supply voltage (V_{EE}). The voltage on the VCOREXT pin is typically V_{EE} + 2.8 volts with an ambient temperature of 25°C. The VCOREXT resistor is R6 in the typical connection diagram in Figure 4. The VCOREXT resistor value vs. VCO center frequency can be calculated from the following equation:

$$R_{VCOREXT}(k\Omega) = 0.268 + \frac{223.2}{f_o} + \frac{7632}{f_o^2}(k\Omega) \qquad (eq.\ 1)$$

where f_o is in MHz. For an example of f_o = 70MHz;

$$R_{VCOREXT}(k\Omega) = 0.268 + \frac{223.2}{70} + \frac{7632}{4900} = 5.01k\Omega \qquad (eq.\ 2)$$

The VCO is at its center frequency when there is zero differential voltage across the FILTER and FILTERN pins. The FILTER and FILTERN pins may be shorted together to measure the center frequency. Note that the frequency observed at FVCO, FVCON is either the VCO frequency or VCO frequency divided by two, depending on the DIVSEL pin setting.

HGREXT: Used to set the magnitude of the high gain current for the charge pump. Normally a resistor will be tied from this pin to the most negative supply of the IC. The voltage on the HGREXT pin is typically V_{EE} +1.18 volts. The user may vary the high gain charge pump current from 0.5mA to 2.0mA. The HGREXT resistor can be calculated from the following equation:

$$HGREXT(\Omega) = \frac{1.18(V)}{(\text{High gain charge pump current})} \qquad (eq.\ 3)$$

Refer to Figure 4, R_2 is typical HGREXT register.

LGREXT: Used to set the magnitude of the low gain current for the charge pump. Normally a resistor will be tied from this pin to the most negative supply of the IC. The voltage on the LGREXT pin is typically V_{EE} +1.18 volts. The user may vary the low gain charge pump current from 100µA to 400µA. The LGREXT resistor can be calculated from the following equation:

$$HLGREXT(\Omega) = \frac{1.18(V)}{(\text{Low gain charge pump current})} \qquad (eq.\ 4)$$

Refer to Figure 4, R_4 is typical HGREXT resistor.

FCAPP, FCAPM: Differential loop filter pins for the delay control feedback loop. A large capacitor is placed across these pins, typically 0.5µF.

FILTER, FILTERN: Differential loop filter pins for the main phase locked loop. These outputs are referenced to VDD and will therefore track with VDD. The FILTER pin is the high impedance side of filter. The FILTERN pin is always a low impedance voltage source which is inversely proportional to the voltage on the FILTER pin.

$$\Delta V_{FILTER} = (-1) \bullet \Delta V_{FILTERN} \qquad (eq.\ 5)$$

The DC voltage crossover point for FILTER and FILTERN is approximately (VDD – 4.75V). The differential range is ± 3V.

The VCO center frequency f_o is defined as the VCO frequency when the VCO control voltage is at the middle of its range. This occurs when there is zero differential voltage across FILTER and FILTERN. The VCO frequency can be controlled directly by forcing the voltage on the FILTER pin. VCO gain can then be measured by plotting the differential voltage across FILTER and FILTERN vs. FVCO frequency and calculating the slope of the line.

SUPPLY PINS:

VEE: Most negative digital supply.

VEE1: Most negative analog supply.

VEE2: Most negative VCO supply.

VEE3: Most negative supply for delay.

VCC: Digital middle supply 5 volts greater than VEE.

VCC1: ECL supply 5 volts greater than VEE.

VCC2: VCO supply 5 volts greater than VEE2.

VCC3: Delay control supply 5 volts greater than VEE3.

VDD: Most positive digital supply.

VDD1: Most positive analog supply.

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

The data separator is inherently a sensitive circuit, and thus circuit performance can be degraded significantly without careful attention to board layout. The following guidelines should be followed:

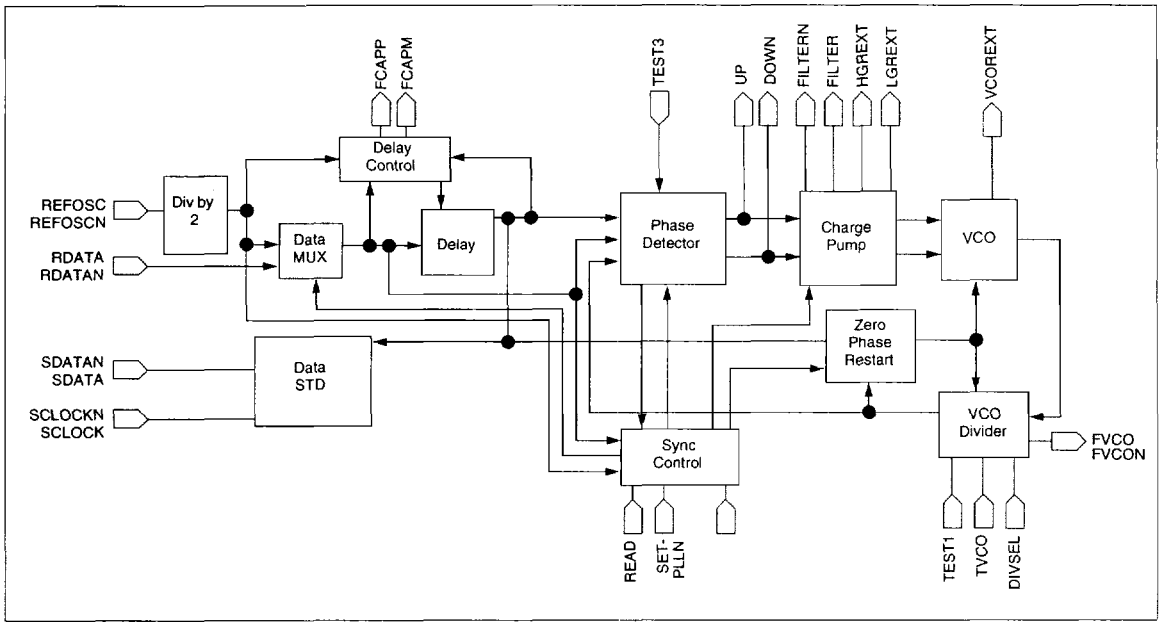
1. V_{EE}, V_{CC} and V_{DD} supply bypass filtering should be liberal and as close to the supply pins as possible. Ideally, a bypass capacitor should be soldered directly to each supply pin. The electrical lead length of the bypass capacitors between the supply and ground pins should be minimized to reduce lead inductance. Only high-quality capacitors should be used.
2. Use the main digital ground plane for all grounding associated with the device.
3. Locate all passive components associated with the chip as close to their respective device pins as possible. It is extremely critical that the PLL filters be very tightly spaced. In addition the $R_{VCOREXT}$ resistor should be tightly spaced or located closely to the VCOREXT pin. Chip capacitors and resistors work very well for these filters.
4. For best performance, the chip pins should be soldered directly to the printed circuit board. If a socket must be used, a low-profile, low-resistance, forced-insertion type socket is recommended.
5. Allow any unused digital outputs to float, unconnected to any other traces.
6. Very fast ECL edge rates should be avoided. Rise/Fall times for the differential ECL signals (REFOSC AND RDATA) should not exceed 2.5ns. If 10KH drivers are used, a 100Ω series resistor works well to reduce the edge speeds

DC CHARACTERISTICS Unless otherwise specified, ambient operating conditions shall apply, T_A = 25°C.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CC}			129.3	170	mA
	I_{DD}			22.3	40	mA
Power Dissipation	P_D	V_{DD} = 13.2V, V_{CC} = 5.5V		1.02	1.3	W
Charge Pump		High gain	0.5		2	mA
		Low gain	0.1		0.4	mA
TTL Inputs (Note 1)						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current High	I_{IH}	V_{IH} = 2.7V, V_{CC} = 5.5V			20	µA
		V_{IH} = 6V, V_{CC} = 5.5V			100	
Input Current Low	I_{IL}	V_{IN} = 0.5V, V_{CC} = 5.5V			-0.6	mA
Differential ECL Inputs (Note 2)						
			V_{CC} - 2.3			V
			200			mV
Input High Current	I_{IH}	V_{CC} = 5.5V			25	µA
Input Low Current	I_{IL}	V_{CC} = 5.5V			25	µA
Voltage Output High	V_{OH}		V_{CC} - 1.02		V_{CC} - 0.66	V
Voltage Output Low	V_{OL}		V_{CC} - 1.95		V_{CC} - 1.63	V

Note 1: TTL inputs will float to a logic HI if left unconnected.
Note 2: All inputs and outputs denoted as ECL track with the V_{CC} supply voltage.

BLOCK DIAGRAM



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EXTERNAL COMPONENT SELECTION

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
RHGREXT			590		2400	Ω
RLGREXT			2.95		12	kΩ
RVCOREXT			1.6		6	kΩ
VMP Series Resistor to Ground			2		5	kΩ
FCAPP, FCAPM Capacitor				0.5		µF

AC CHARACTERISTICS Unless otherwise specified, ambient operating conditions shall apply, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
REFOSC, REFOSCN Period	T_{REFOSC}		10			ns
REFOSC, REFOSCN Pulse Width	$t_{pwREFOSC}$		4			ns
RDATA, RDATAN Pulse Width	$t_{pwRDATA}$		4			ns
Window Center Offset	t_{WINDOW}			<300		ps
Delay Line Propagation Delay	t_{pDL}			Note 1		ns
VCO Phase Noise	ϕ_{VCO}	Locked to preamble, 1σ (note 2)		<50		ps
VCO Center Frequency Variation	Δf_o	@ f_o = 70MHz	-10		+10	%
VCO Zero Phase Restart Error	t_{ZPR}			<1		ns
VCO Maximum Center Frequency	f_{cMAX}			192		MHz
VCO Dynamic Range from f_o	f_{VCODR}	f_o = 70MHz, $R_{VCOREXT}$ = 4.9kΩ	$0.7f_o$		$1.3f_o$	MHz
VCO Gain	K_O	f_o = 70MHz, $R_{VCOREXT}$ = 4.9kΩ	$0.9f_o$	$0.105f_o$	$0.13f_o$	MHz/V
Charge Pump Output Linearity	f_{LIN}	Range is 0 to 2π	-10		+10	%
SCLOCK Duty Clock	t_{dcSCLK}			50		%
Propagation Delay from SCLOCK Negative Edge to SDATA Rising Edge	t_{pdSD}	C_{load} = 20pF		$-1.5 < t_{pdSD} < 1.5$		ns
Propagation Delay from FVCO Rising Edge to SCLOCK Rising Edge	t_{pdSCLK}	C_{load} = 20pF		$-2 < t_{pdSCLK} < 4$		ns
Marginalization Maximum Shift	$t_{MAXMARG}$			0.25 (T_{REFOSC})		ns
Marginalization Variation from Nominal	t_{MARG}	$V_{VMP} - V_{VMM}$ = 100mV		±0.02 (T_{REFOSC})		ns

Note 1: Nominal value for t_{pDL} is: $[0.5(T_{REFOSC}) - 1] < t_{pDL} < [0.5(T_{REFOSC}) + 1]$.
Note 2: VCOCLK output 1σ point measured over 10,000 samples on an HP5370B time interval counter. $\sigma_{fcl} = \sqrt{\sigma_a^2 - \sigma_b^2}$, where σ_a = rms jitter measurement and σ_b = self jitter of HP5370B (see HP app. note 191-4).

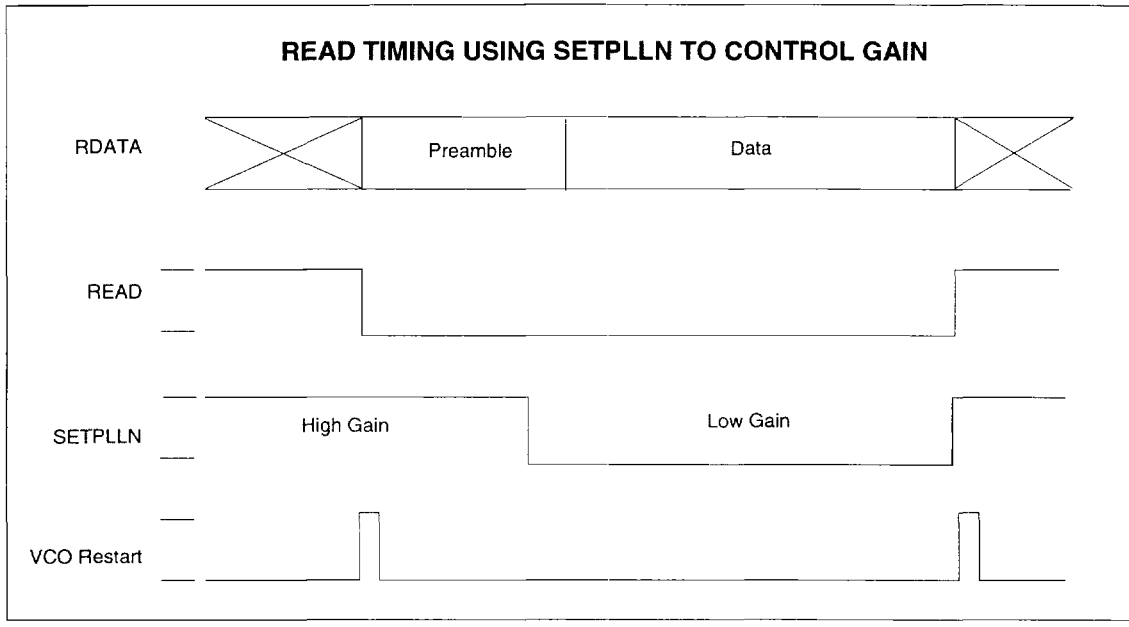


Figure 1: Read Timing Diagrams

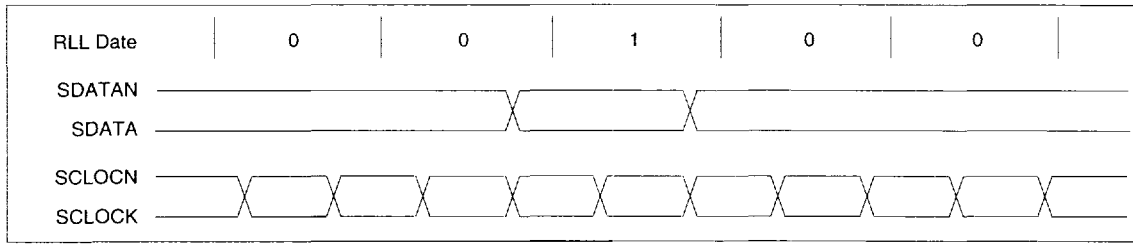


Figure 2: Synchronized Data and Clock Timing

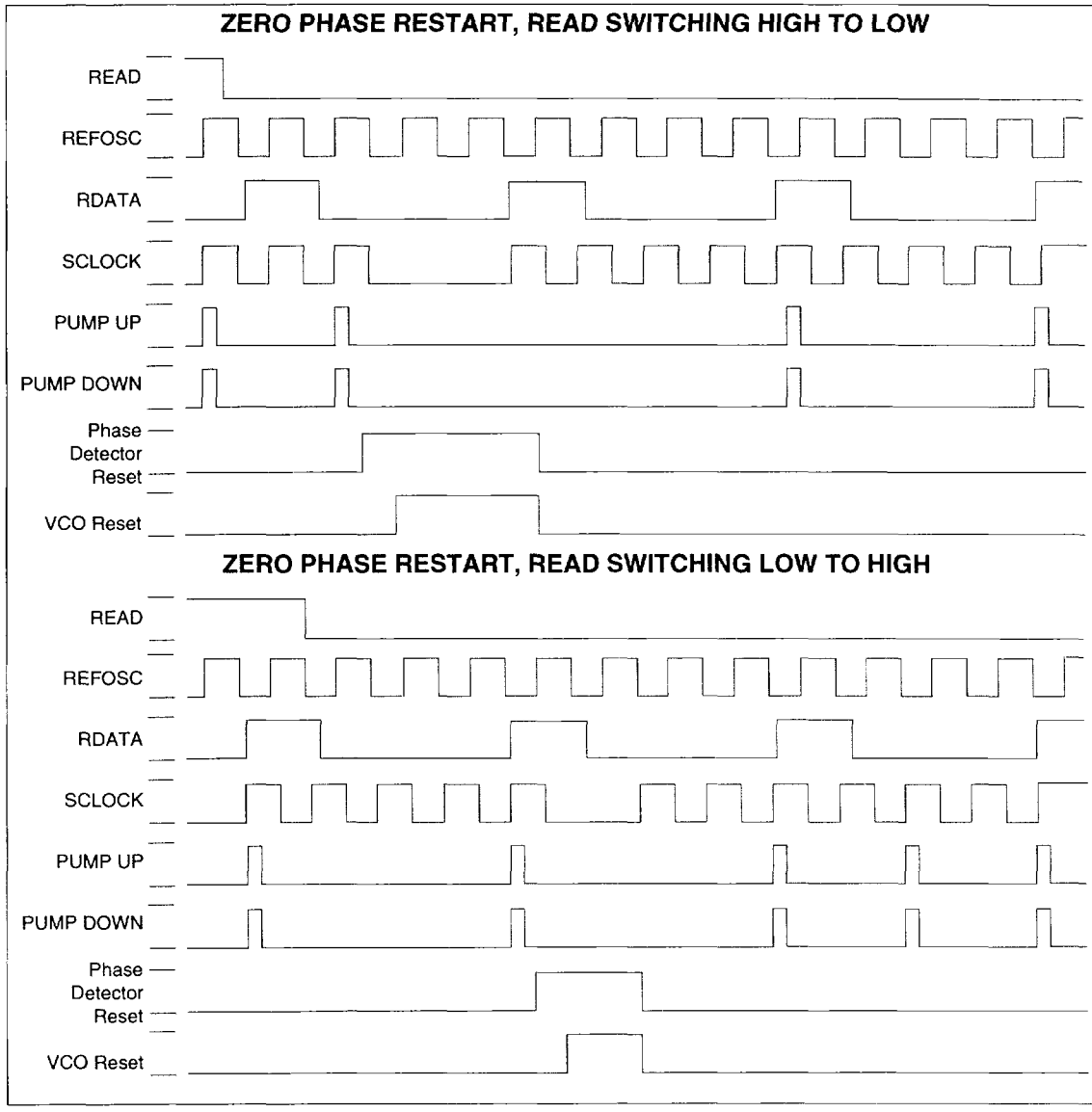
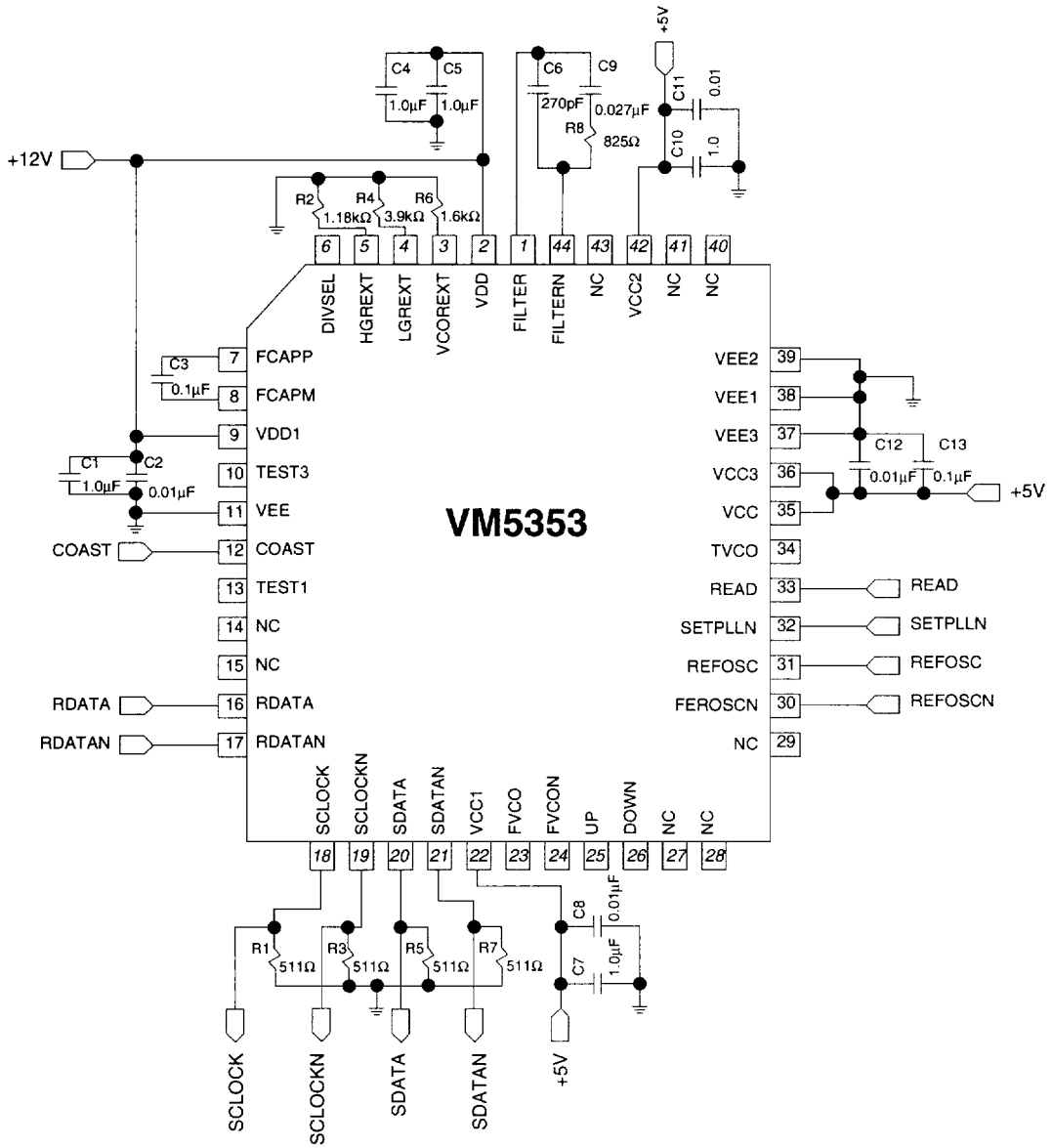


Figure 3: VCO Zero Phase Restart Timing



NOTE: This circuit is set up for 64Mbits/sec using (1,7) code. The REFOSC input frequency is a 96MHz differential ECL signal. The high and low gain charge pump currents are set to 1.0mA and 0.3mA, respectively. The VCO center frequency is set to 192MHz, giving a VCO gain of 20.2MHz/V. This is a general setup and not intended to be optimized for 4Mbits/sec.

Figure 4: VM5353 Typical Connection Diagram