WD1931/WD1933 Compatibility Application Notes

INTRODUCTION

The purpose of this document is to provide the reader with information about the WD1931 and WD1933 devices, and how to take advantage of their compatibility. Various applications examples are given showing flowcharts and timing diagrams. As the devices are designed for use in a very large range of applications, many different features are described and illustrated for the benefit of the reader.

For detailed product information such as A.C. and D.C parameters, please refer to the respective data sheets.

GENERAL DESCRIPTION

The WD1931 and the WD1933 are MOS/LSI devices which interface a parallel digital system to a serial data communication channel (and vice versa). Both circuits are capable of simplex, half duplex, and full duplex operation.

The WD1931 is designed for character-oriented asynchronous and/or synchronous (BI-SYNC) protocols. The WD1933 is designed for bit-oriented SDLC, HDLC and ADCCP protocols. The devices are programmable and compatible to most 8-bit microcomputers on the market. The pin assignments of these two devices have been chosen to allow the user to implement a one-board multiprotocol design. This board may then be used for any of the above mentioned protocols, by choosing the proper device (WD1931 or WD1933) and connecting some jumpers (see paragraph entitled "Multiprotocol Board Design"). The purpose of these circuits are to convert parallel data from a computer or terminal to a serial data stream at one end of a communication channel. At the other end of the channel, the data is converted back to the original parallel data.

Serial data communications minimizes the number of physical channels required to transfer data and therefore reduces the cost to send data between two (or more) distant points. A microcomputer could perform the same serial/parallel conversion function as these devices, but at much slower speeds. However, using the WD1931 and WD1933 devices to do this function is much more efficient. This makes the computer free to perform other tasks during transmission and reception. The only work that the computer is required to do is to initialize and write data characters to/from the WD1931 or WD1933. These devices will take care of the serialization or deserialization of this data, plus control and timing.

Some control signals on the computer side of the devices are needed for read, write, and control purposes. Additional signals can also be used for special purposes or modes for the convenience of the user. Typically, these other control signals are used to enable communication with a modem or DCE (Data Communications Equipment).

Interrupt outputs are provided to inform the microcomputer when to retrieve from, or to provide data to the holding registers. Also, interrupts can be generated to provide status information such as changes in modem control lines, or that events such as Transmission Complete or Received End of Message have occurred.

SYSTEM APPLICATIONS

WD1931/33 may be used in the following applications:
Switched network
Multipoint network
Non-switched point to point network
Simplex, half-duplex, or full duplex
Asynchronous or synchronous communication
Message switching
Multiplexing systems
Data concentrator systems
Loop data link systems
DMA applications
Parallel to serial data conversion (and vice versa)
Local Networks
Packet Switching
X.25
Multidrop line systems

A typical block diagram of a data link is shown in Figure 1. The communication media used could be a direct communication channel (such as a leased telephone line), a switched telephone line, or one of many other possibilities. Typically these applications would require the use of a modem.

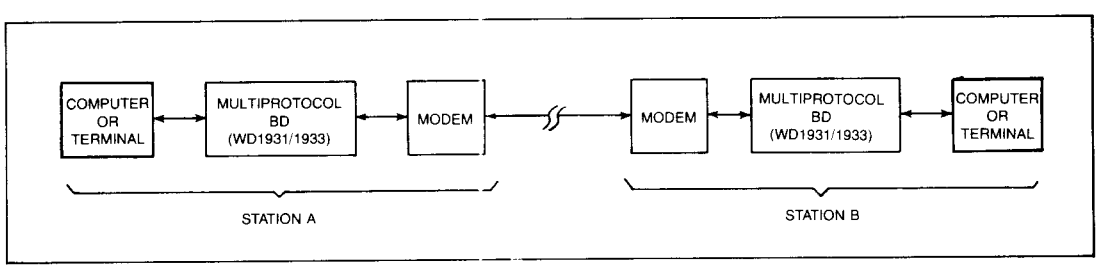


Figure 1. DATA LINK BLOCK DIAGRAM

The applications that these devices could be used in would be a combination of the previously mentioned. A modem would be needed for long distance communication lines. For shorter distance, line drivers/receivers may be sufficient. In some very well controlled environments, such as a laboratory, two devices may be connected without line drivers and receivers.

The WD1931 or WD1933 may be connected directly to a microcomputer bus, but buffers would normally be recommended. Figure 2 shows a typical schematic of an interface between a Z80 microcomputer and a modem. This is called a multiprotocol board, which is described later in this document.

Some examples of various WD1931/WD1933 systems are shown here by use of block diagrams. The station shown in Figure 3 consists of a computer or terminal, a multiprotocol board, and a modem. A station may consist of only the computer or terminal, and one WD1931 or WD1933 device. Whether the modem, line drivers and receivers, or CPU buffers are needed depends on the details of the particular design situation.

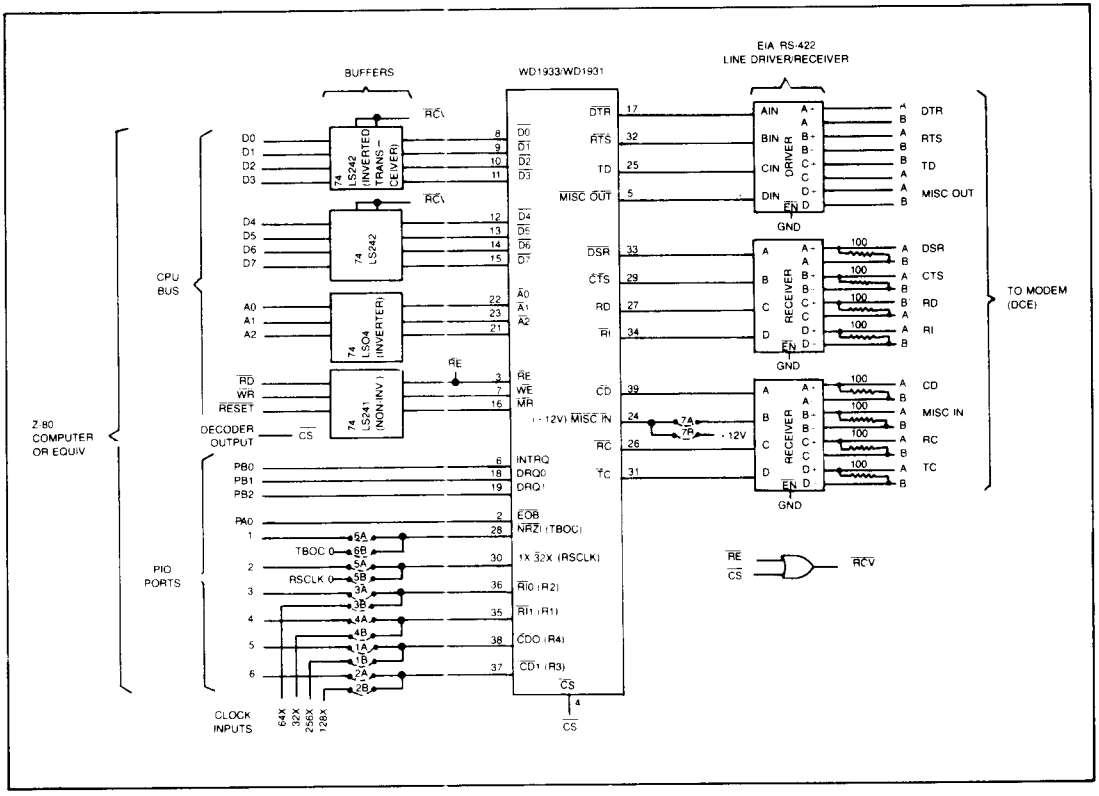
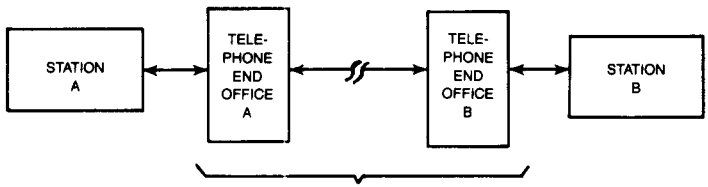
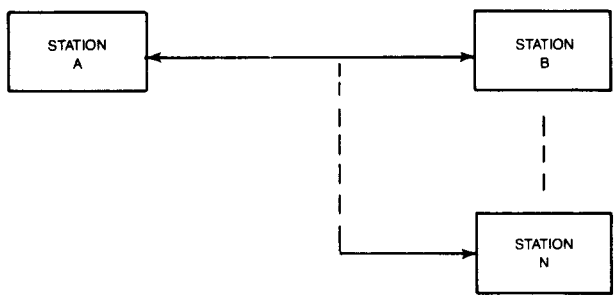


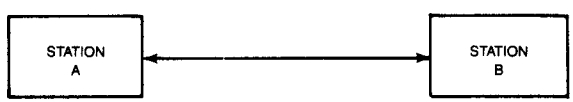
Figure 2. WD1931/1933 AND MICROCOMPUTER. (MULTIPROTOCOL BOARD)



SWITCHED NETWORK



MULTIPOINT NETWORK



NONSWITCHED POINT TO POINT NETWORK

Figure 3. TYPICAL NETWORKS

LOOP DATA LINK SYSTEM

The Loop Mode is used in SDLC only. A loop data link system consists of one primary station (Loop Controller), and a number of secondary stations all functioning normally as repeaters. Figure 4 illustrates a typical Loop Data Link system.

Any secondary station finding its address in the address field captures the frame for action at that station. All received frames are relayed to the next station down the loop.

A secondary station is allowed to suspend the repeater function and initiate its transmission when a Go-Ahead pattern is received.

DATA COMMUNICATIONS EXAMPLE NO. 1

The diagrams below (Figures 5 and 6) illustrate a typical digital system employing several processing levels and digital communications protocols. It is flexible enough to satisfy several applications. For example, the host processor and remote terminals could be located in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual cash registers. The exploded diagram of the Data Communications Controller exemplifies the use of one common circuit board design with eight multiprotocol circuits. When one port requires a character-oriented protocol (asynchronous, character oriented synchronous, or bisync), the WD1931 is installed into the appropriate socket. For SDLC, HDLC or ADCCP, the WD1933 is used.

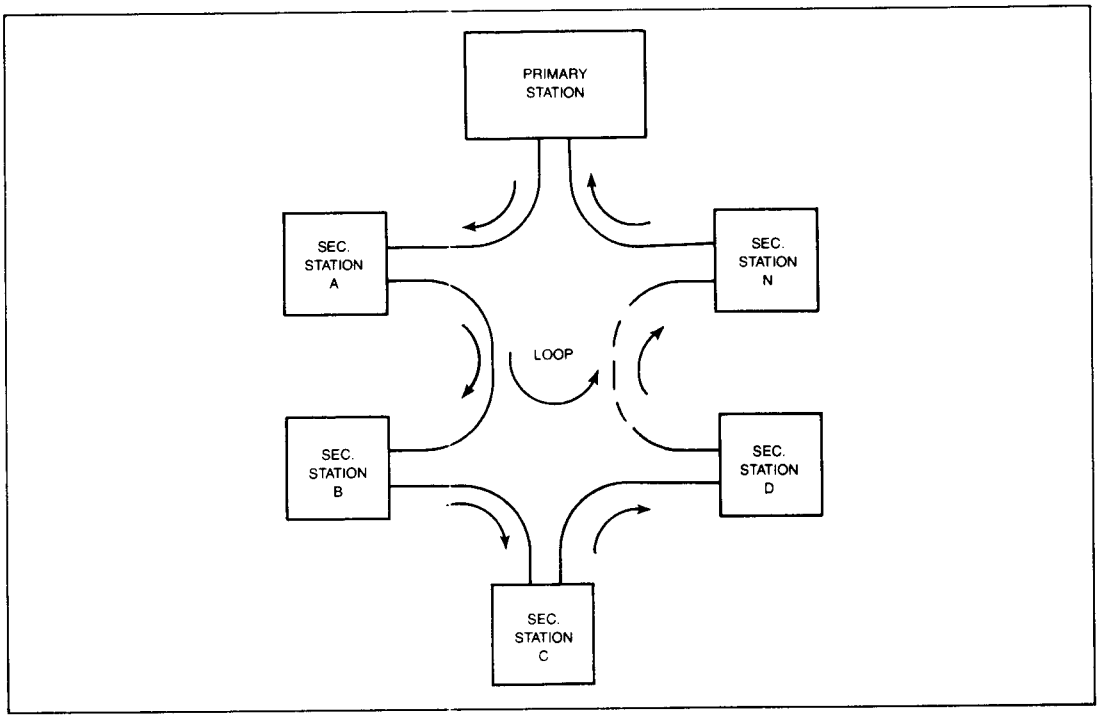


Figure 4. LOOP DATA LINK SYSTEM

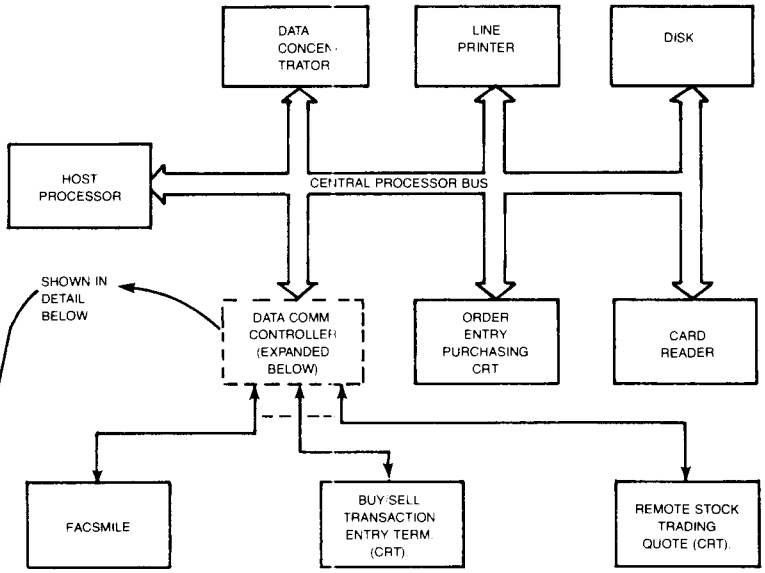


Figure 5. STOCK BROKERAGE SYSTEM

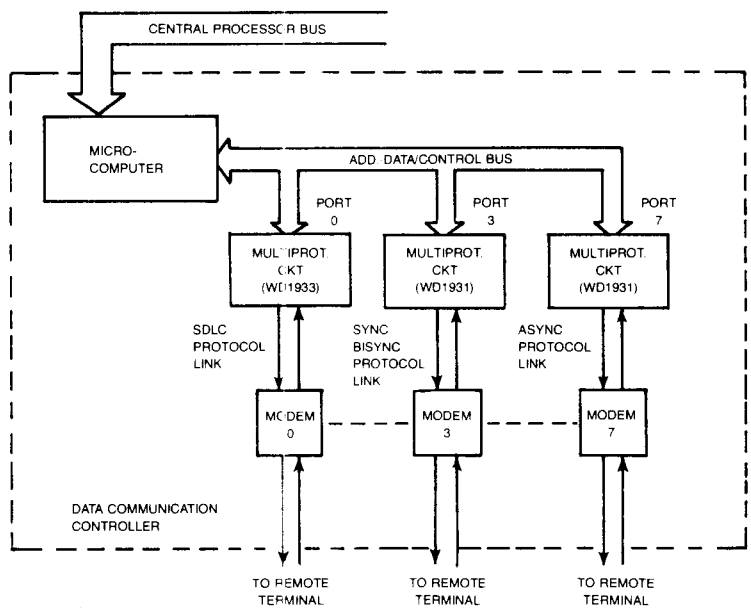


Figure 6. DATA COMMUNICATION CONTROLLER

DATA COMMUNICATIONS EXAMPLE NO. 2

Figure 7 illustrates a Host Computer that communicates through modems to a multiprotocol board. This in turn collects information from many remote stations through a Data Concentrator.

DATA COMMUNICATIONS EXAMPLE NO. 3

A simplified HDLC point to point connection is shown in Figure 8. In this example, no buffers or line drivers and receivers are used.

Figure 9 represents a more "real world" application with the use of modems through a communications channel.

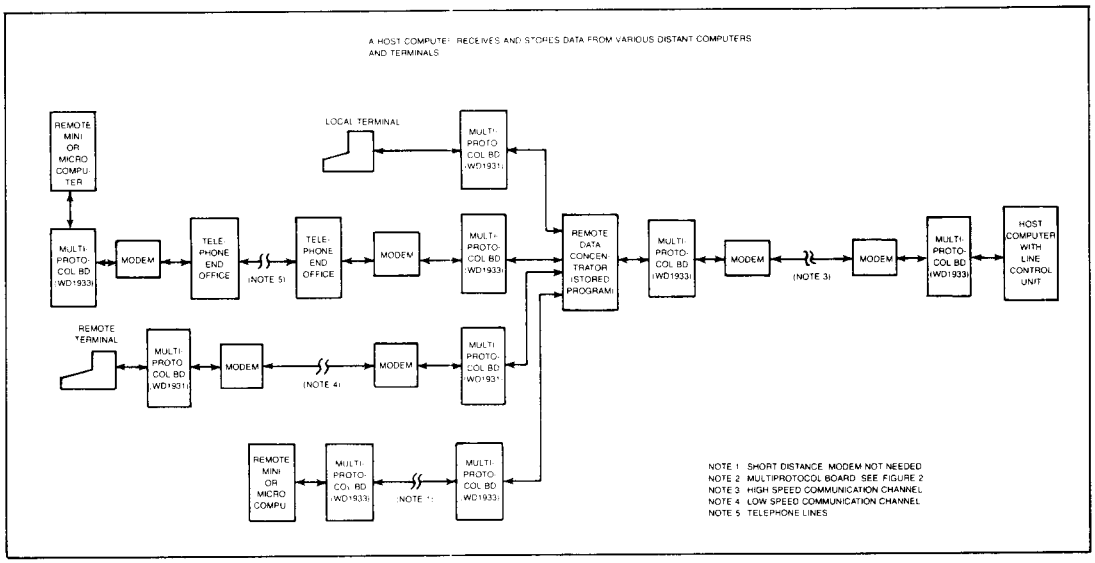


Figure 7. DATA CONCENTRATOR

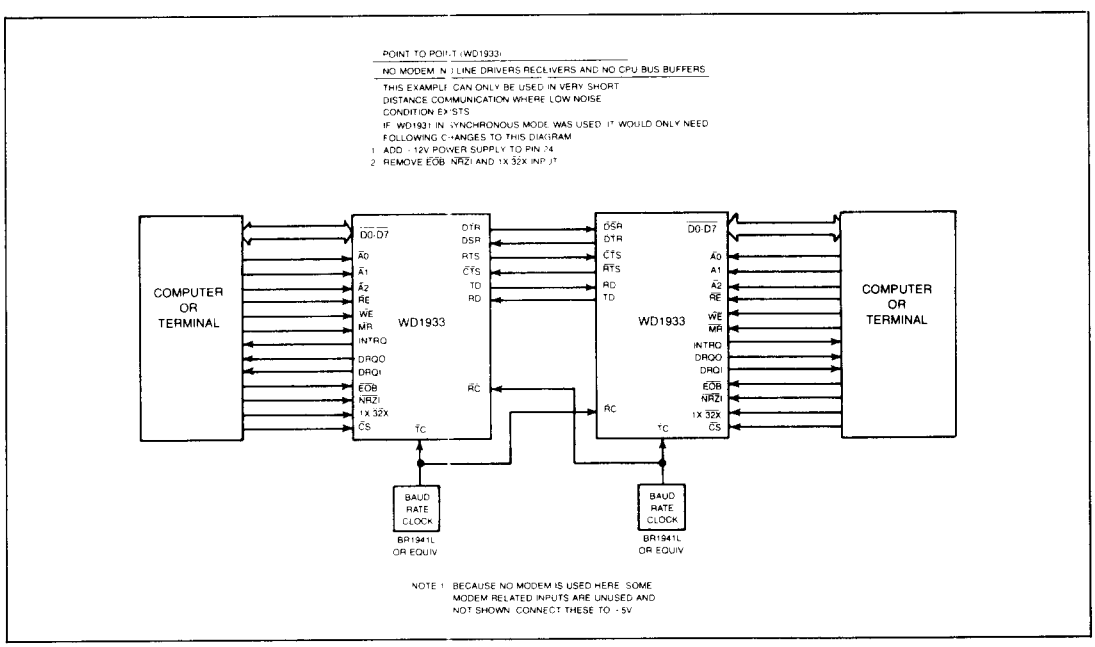


Figure 8. HDLC POINT TO POINT

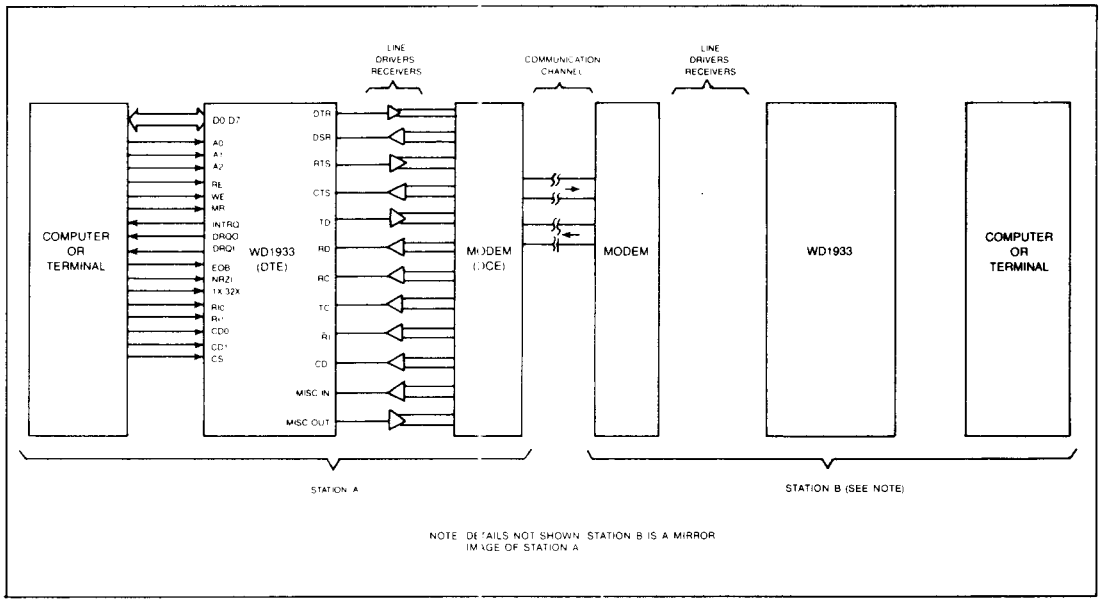


Figure 9. HDLC POINT TO POINT WITH MODEM

WD1931 AND WD1933 TECHNICAL DESCRIPTIONS

The WD1931 and WD1933 devices have been designed to provide a high degree of compatibility and interchangability. The pin-outs are similar, and the register operations are software compatible. This feature allows for the use of either device in a given socket.

WD1931 PIN-OUTS AND BLOCK DIAGRAM

The WD1931 pin assignments and the block diagram are shown in Figure 10.

WD1933 PIN-OUTS AND BLOCK DIAGRAM

The WD1933 pin assignments and the block diagram are shown in Figure 11.

SHORT FORM REGISTER FORMAT AND ADDRESSING

Information concerning operating modes and status conditions are passed to and from the WD1931 or WD1933 device through I/O addressable registers. Each register contains eight bits, where each bit represents a specific function and has its own mnemonics.

The state of each bit is represented by a "1" for TRUE and a "0" for FALSE. This may or may not correlate to a measurable voltage level at a pin, since some pins are TRUE when they are at 0 volts (this is indicated by a bar over the name, or a slash immediately preceeding the name).

The WD1931 registers are shown in Figure 12. Note that some bits are affected by the transmit clock ($\overline{TC}$) rate or the receive clock ($\overline{RC}$) rate.

The WD1933 registers are shown in Figure 13. Note that some bits are affected by the transmit clock ($\overline{TC}$) rate or the receive clock ($\overline{RC}$) rate.

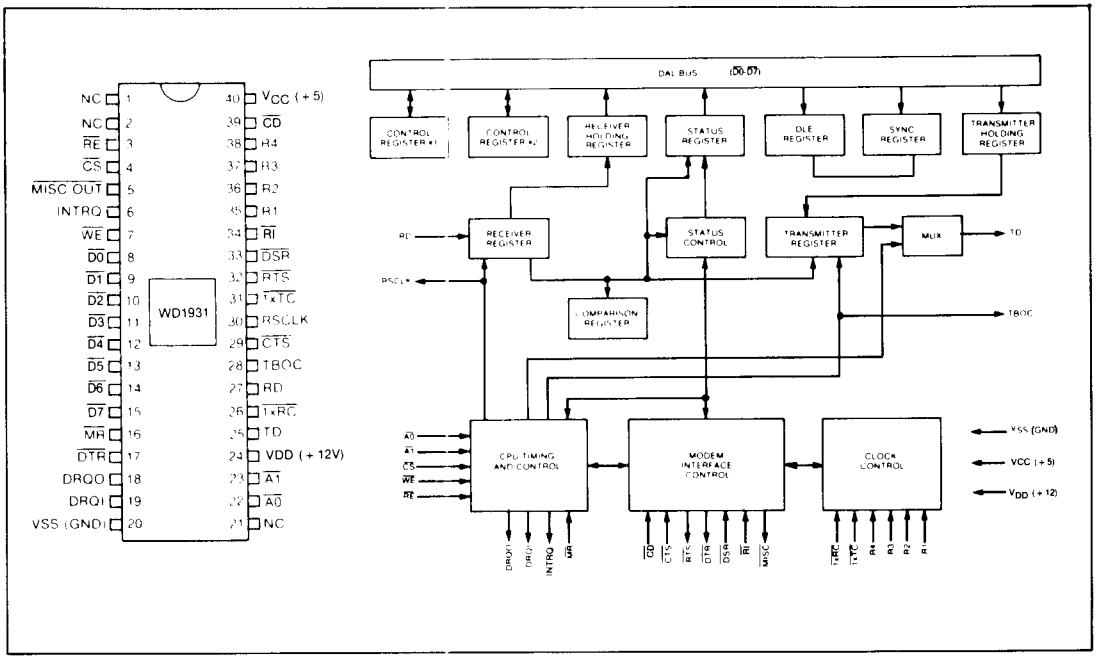


Figure 10. WD1931 PIN CONNECTIONS AND BLOCK DIAGRAM

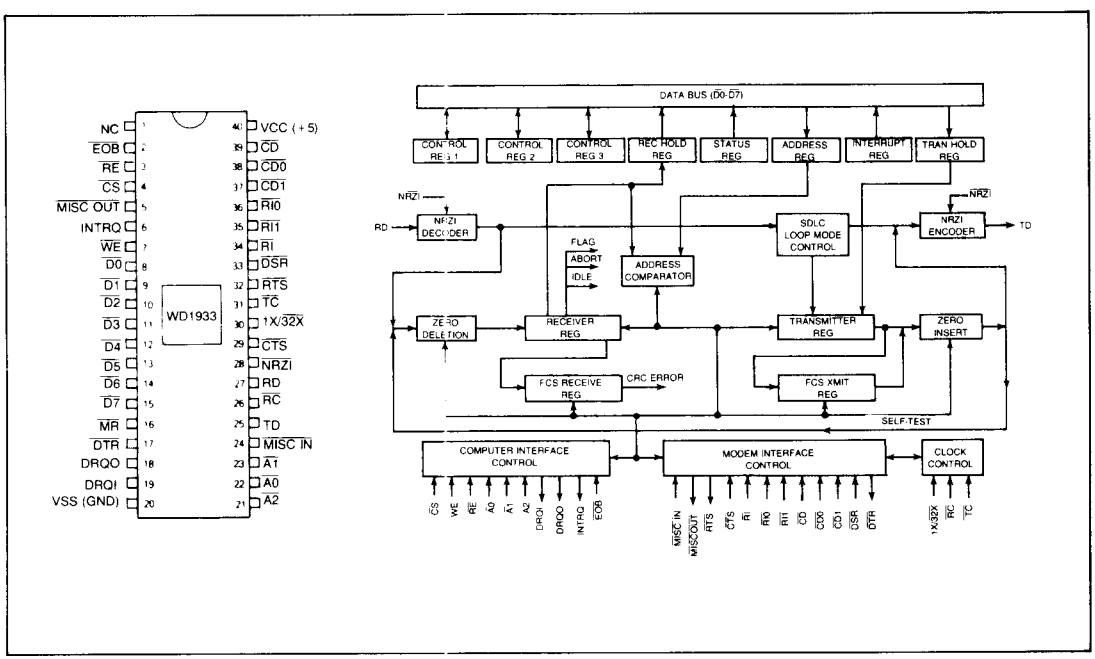
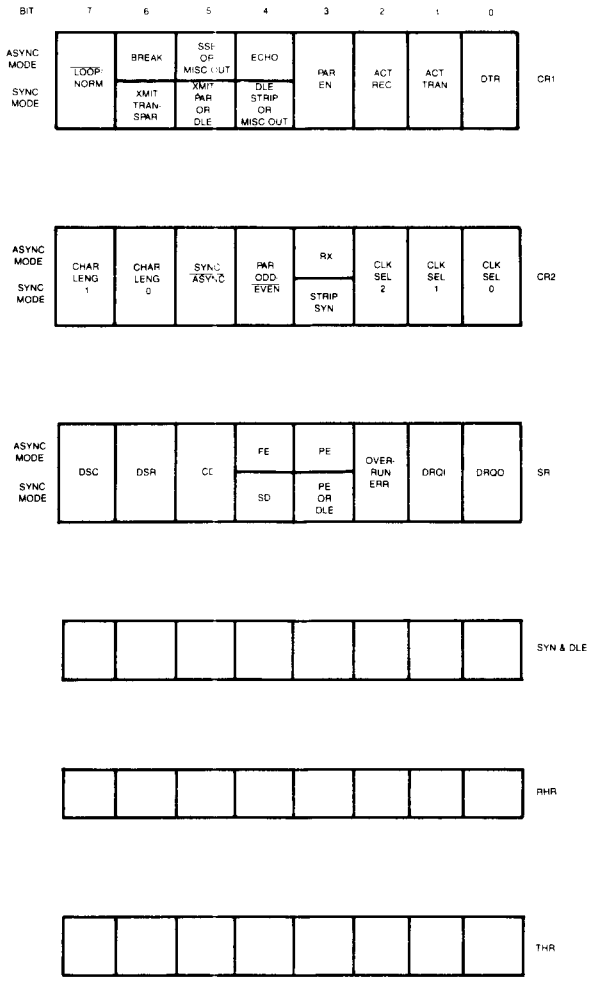


Figure 11. WD1933 PIN CONNECTIONS AND BLOCK DIAGRAM

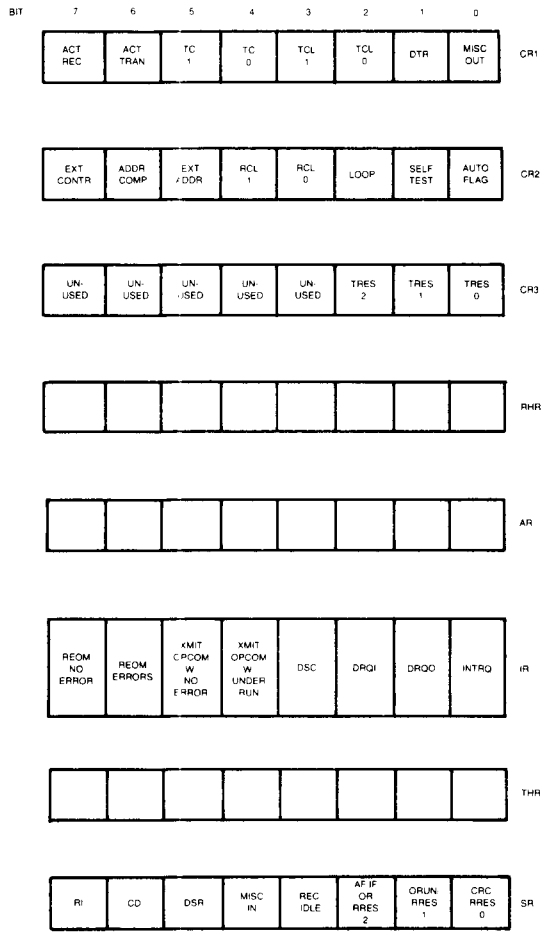


WD1931 BIT ASSIGNMENTS

$\overline{A1}$	$\overline{A0}$	READ	WRITE	CLOCK
LO	LO	CR1	CR1	NONE
LO	HI	CR2	CR2	NONE
HI	LO	SR	SYN & DLE	SR0 = $\overline{TC}$. SR1-4 = $\overline{RC}$. SR5-7, SYN, DLE = NONE
HI	HI	RHR	THR	RHR = $\overline{RC}$. THR = NONE

WD1931 REG. ADDRESSES AND CLOCKS

Figure 12. WD1931 REGISTERS



WD1933 BIT ASSIGNMENTS

$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	READ	WRITE	CLOCK
HI	HI	HI	CR1	CR1	NONE*
HI	HI	LO	CR2	CR2	NONE*
HI	LO	HI	CR3	CR3	NONE*
HI	LO	LO	RHR	AR	RHR = $\overline{RC}$. AR = NONE
LO	HI	HI	IR	THR	IR = $\overline{TC}$. THR = NONE
LO	HI	LO	SR	—	SR0-3 = $\overline{RC}$. SR4-7 = NONE

*After a master reset operation, 2.5 TC clock cycles are required.

WD1933 ADDRESSES AND CLOCKS

Figure 13. WD1933 REGISTERS

MULTIPROTOCOL BOARD DESIGN

The WD1931 and WD1933 pin assignments were chosen so that a circuit board designer may use only one 40-pin socket, but have the choice of using either device on that board. Depending on the application, a few jumper wires may be needed, or perhaps none at all. Figure 2 shows a typical example of a multiprotocol board. This board may be designed with even less components and jumpers, dependent on the particular application it is intended for.

Jumpers 1A-7A are to be connected when WD1933 and all its options are used. Jumpers 1B-7B are to be connected when WD1931 and all its options are used.

For example, if the user does not need the NRZI signal mode, the 1X clock is only used, no Ring or Carrier Detect indication is needed, TBOC, RSCLK and MISC IN are not used, and then no jumpers are needed in the design. In this case, pin 24 may be permanently connected to +12V. Pins 28 and 30 may be connected to +5V via a 10K resistor, and pins 35 through 38 may be connected directly to +5V.

TRANSMISSION EXAMPLE 1 (ONE FRAME)

A typical sequence of events is shown here to transmit a message from computer A to another computer (or terminal) B through a switched network. The message to be sent is a synchronous SDLC protocol frame as shown below in Figure 14. For simplicity, the message sent in this example is very straightforward and short.

Line drivers and receivers are used, permitting transmission to a remote DCE or modem (see schematic in Figure 2). As the SDLC frame is sent, the WD1933 is used. The jumpers required are 1A-7A. Figure 15 illustrates the functional flow, and Figure 16 details the timing of the transmitted frame. Note that the device can be programmed in several different ways to allow for various requirements.

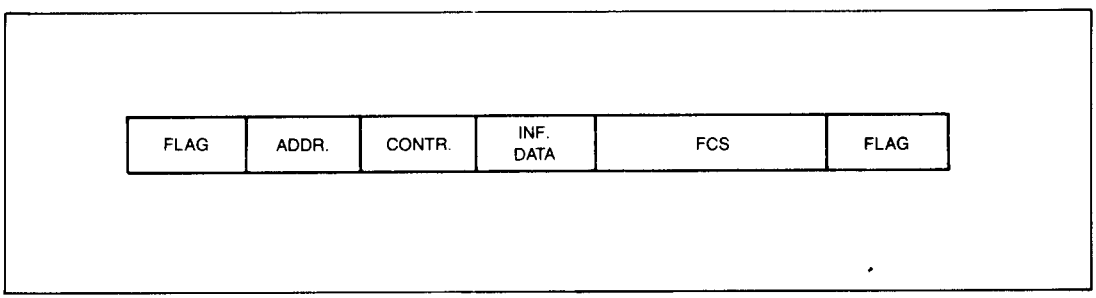


Figure 14. SDLC FRAME FORMAT

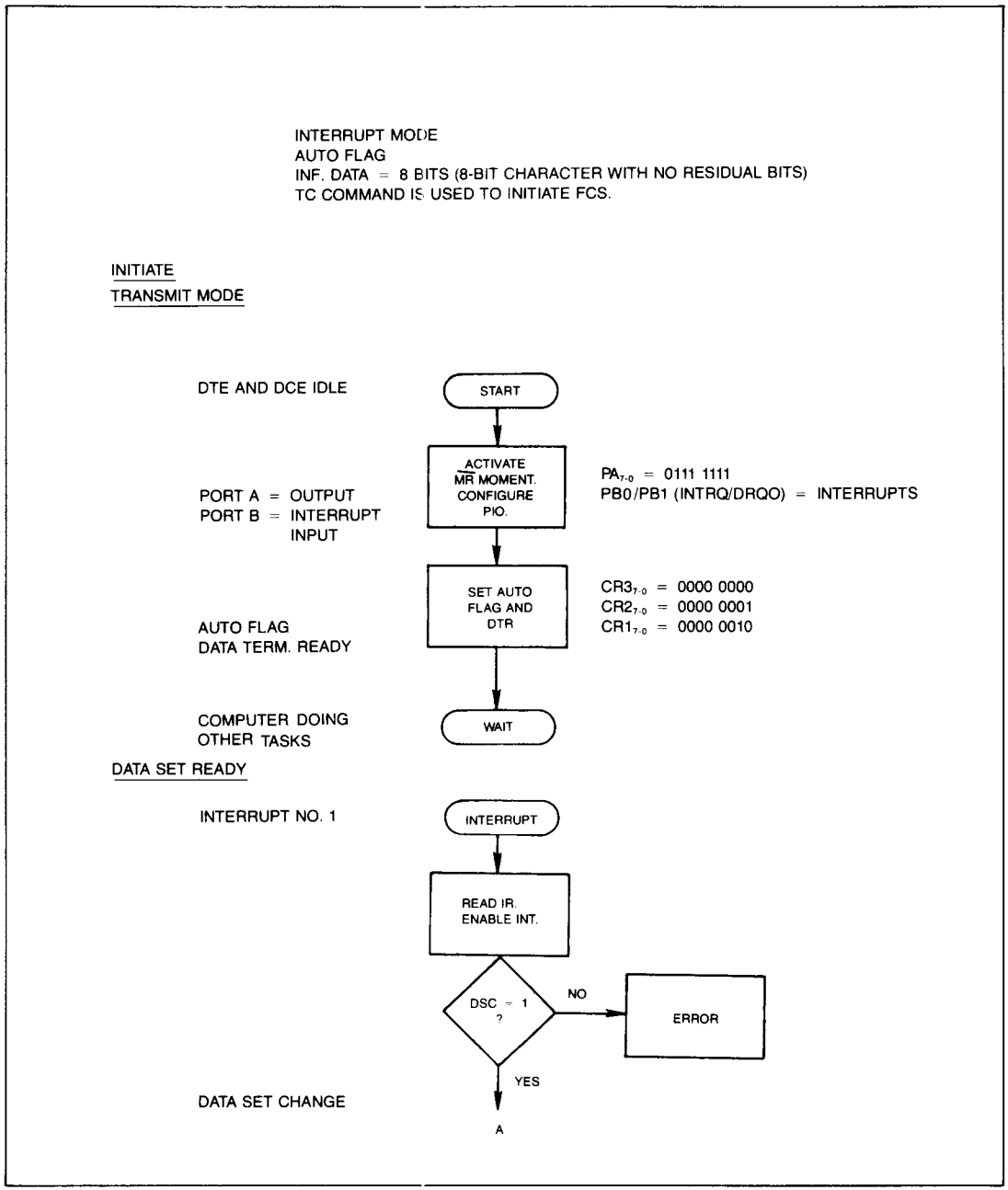


Figure 15. FLOW DIAGRAM OF FRAME TRANSMISSION

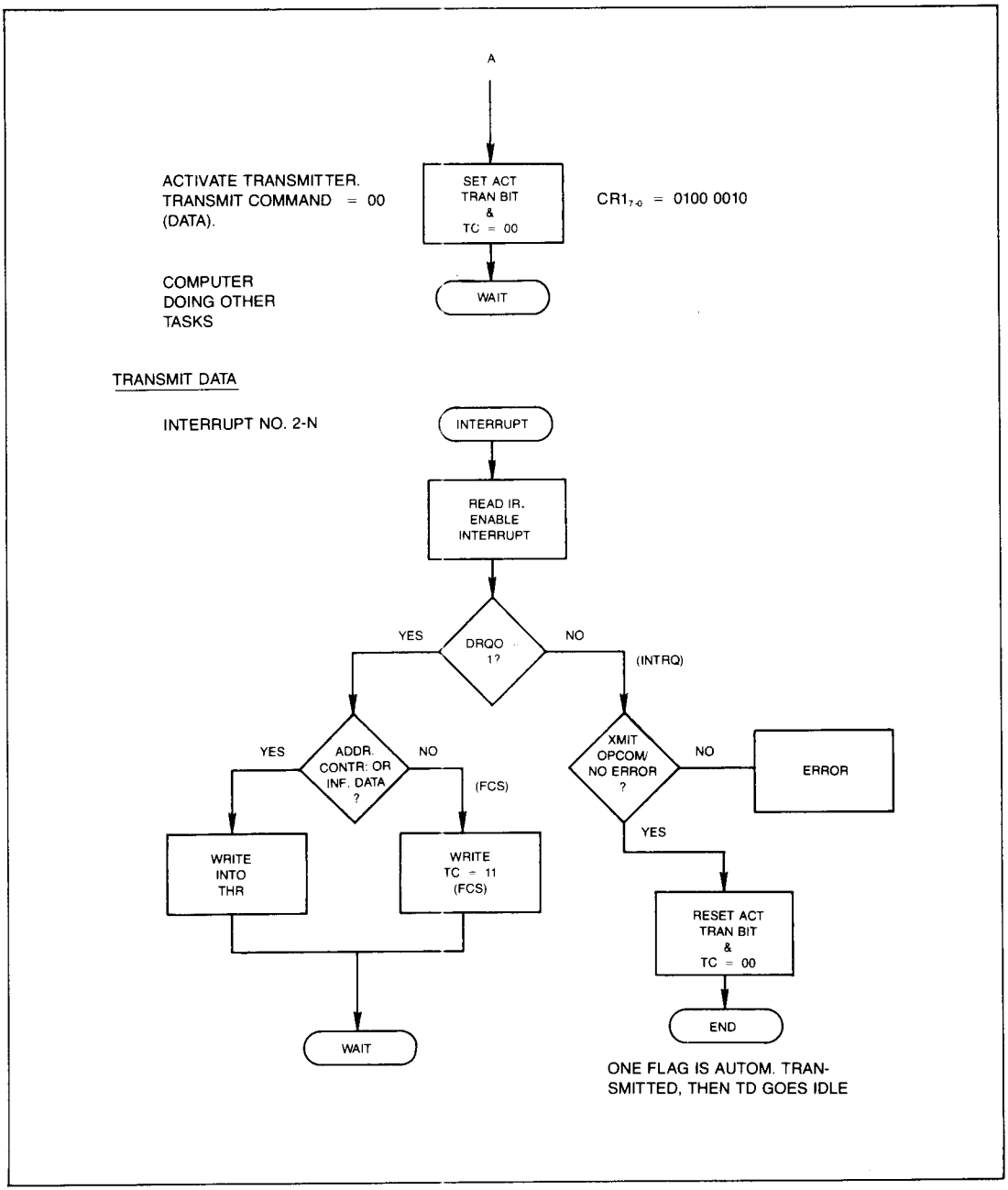


Figure 15. FLOW DIAGRAM OF FRAME TRANSMISSION

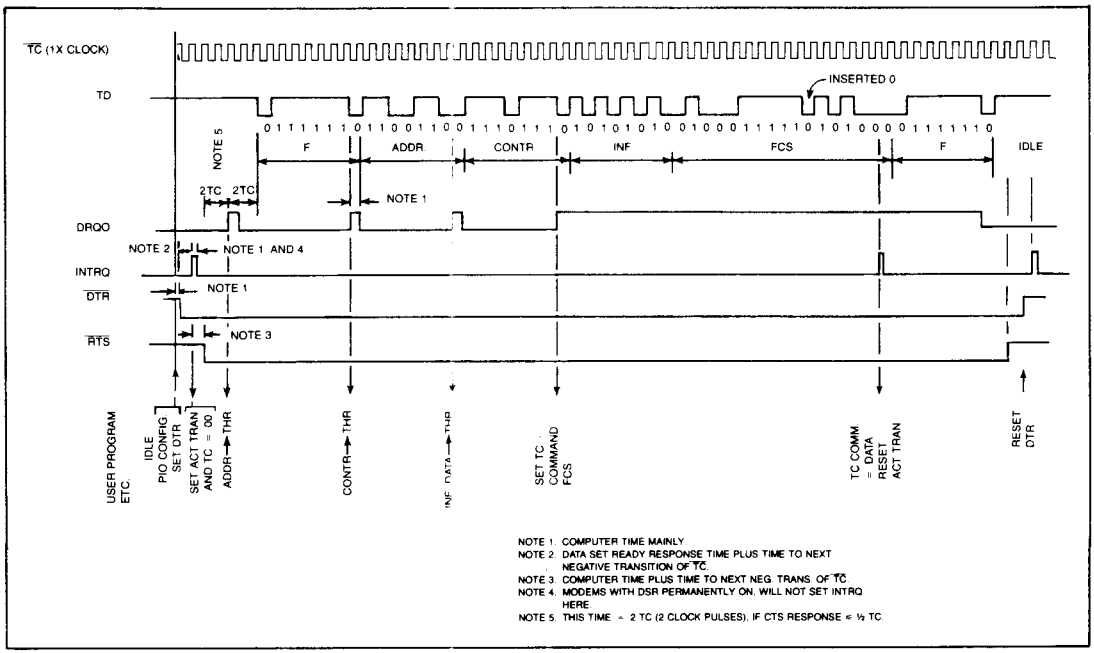


Figure 16. TIMING DIAGRAM OF FRAME TRANSMISSION

WD1933 TRANSMISSION EXAMPLE 2 (DMA APPLICATION)

The WD1933 is very efficient for DMA applications. The control registers are loaded to initiate the WD1933 for DMA mode in the same way as in Transmission Example 1. The Auto Flag bit is set, and the Transmitter Command is "DATA" (CR14 and CR15 bits = 00). The procedure to set up the link (initiate transmit mode and data set ready) is the same as in Transmission Example 1. When INTRQ is set and the Transmitter is activated, the DMA Controller Board takes over the control. From this time on, the DMA Controller Board responds on every DRQO (Data Request Out). When the last character is transmitted and the INTRQ is received, the control is switched back over to the CPU.

A very important feature of the WD1933 is the EOB (End of Block) input. Instead of using the normal (time-consuming) method of writing into a control register to start the FCS (Frame Check Sequence), the $\overline{EOB}$ input is activated at this time. At the next occurrence of INTRQ, the $\overline{EOB}$ signal is deactivated.

An example of a schematic/block diagram is shown in Figure 17, and a timing diagram is shown in Figures 18 through 20.

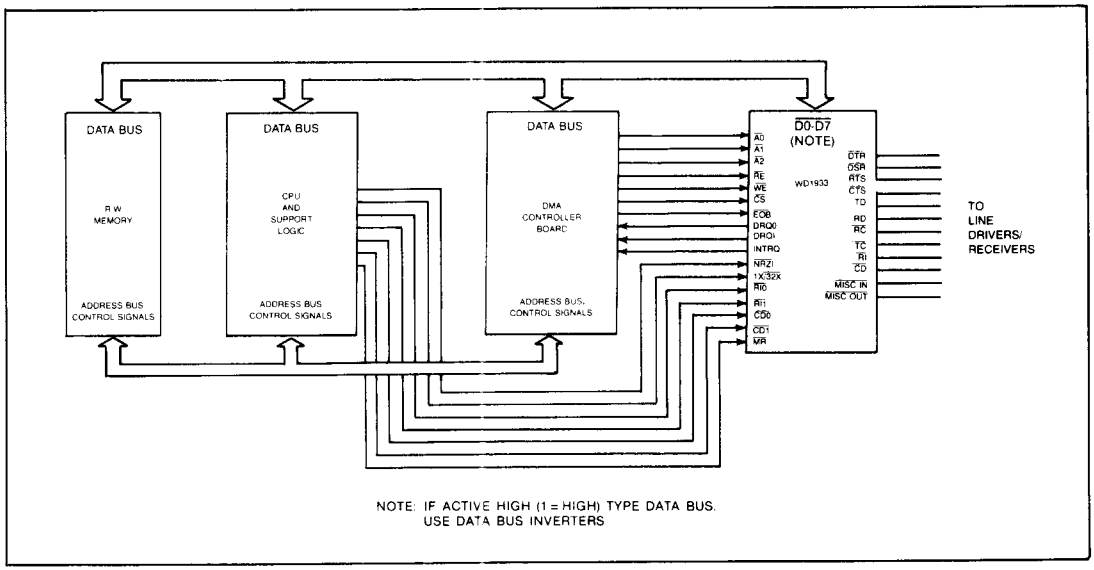


Figure 17. BLOCK DIAGRAM OF DMA APPLICATION

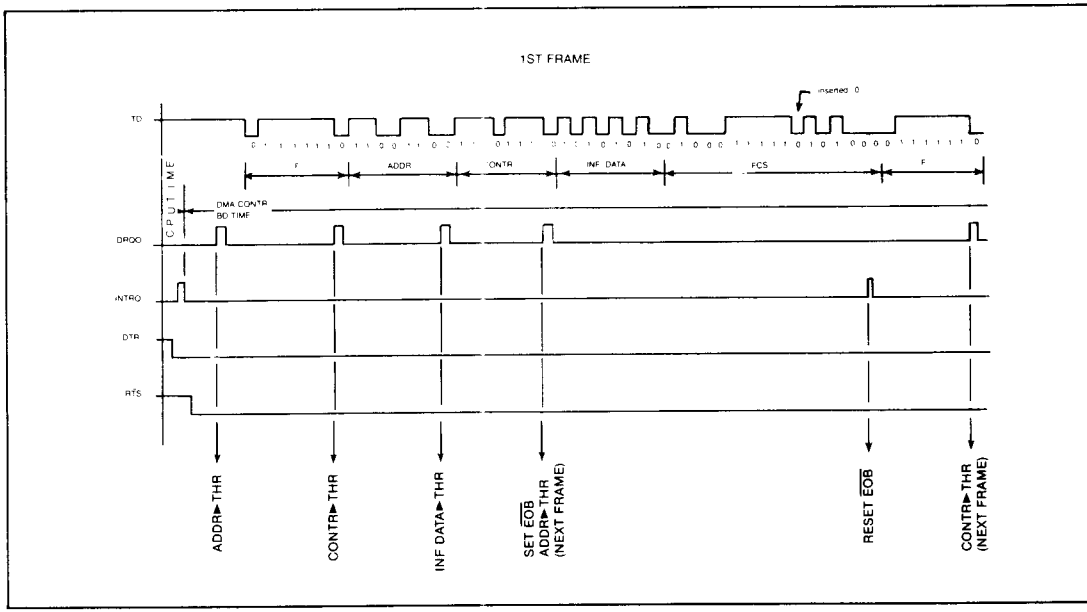


Figure 18. DMA TIMING OF FIRST FRAME

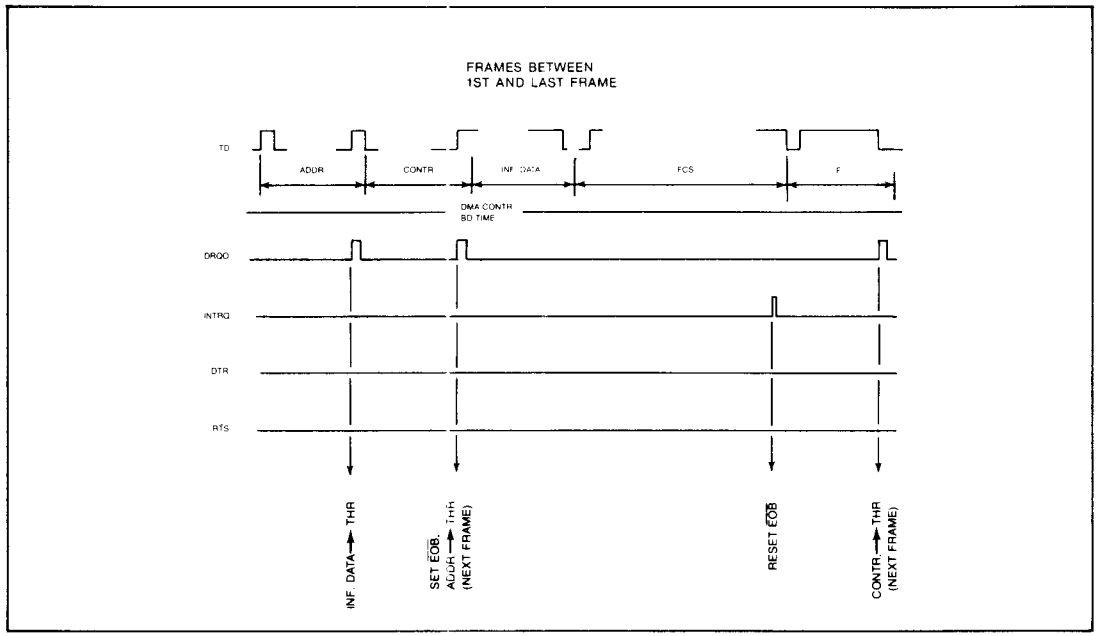


Figure 19. DMA TIMING OF MIDDLE FRAMES

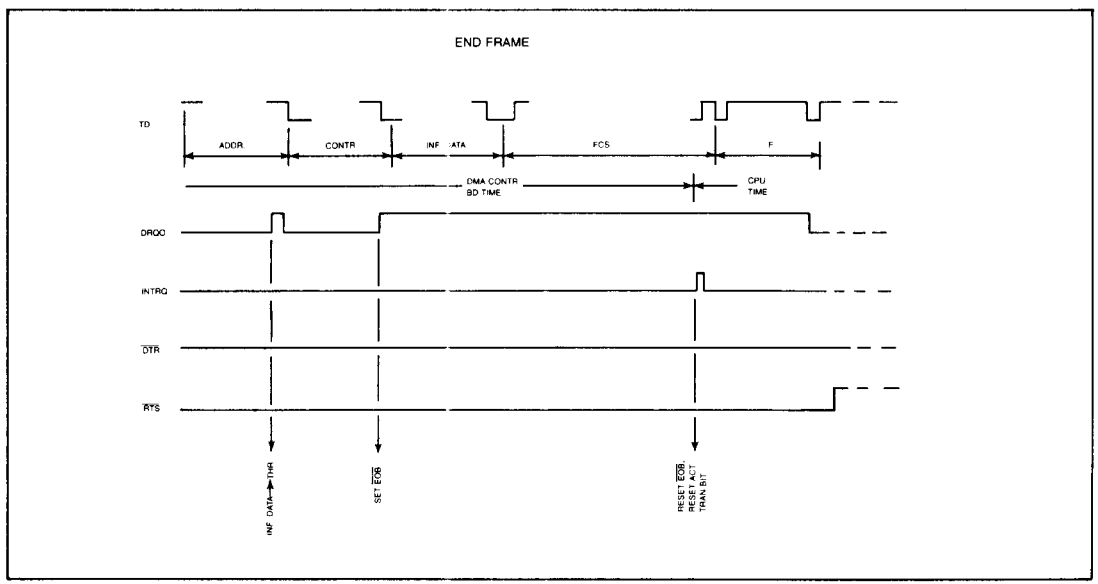


Figure 20. DMA TIMING OF LAST FRAME

WD1933 RECEPTION EXAMPLE 1

A sequence of events is shown in illustrating how to receive a message with the WD1933 device. For simplicity, the same SDLC frame structure is used as in Transmission Example 1. Also, please refer to the same interface circuitry shown in Figure 2.

Figure 21 illustrates the functional flow, and Figure 22 contains the timing information.

WD1933 RECEPTION EXAMPLE 2

This example shows a frame with two ADDRESS characters, two CONTROL characters, one 5-bit INFORMATION DATA character, and two residual bits. This example may not be a typical frame, but it shows how the WD1933 works in a wide range of frame structures.

The first FLAG and FCS are not shown in detail, and are not critical to this example.

Figure 23 illustrates the functional flow, and Figure 24 contains the timing information.

WD1933 LOOP DATA LINK EXAMPLE

This example shows how to program a secondary station to function in SDLC Loop mode. The functional flow is illustrated in Figure 25, and the interface circuit is shown in Figure 2.

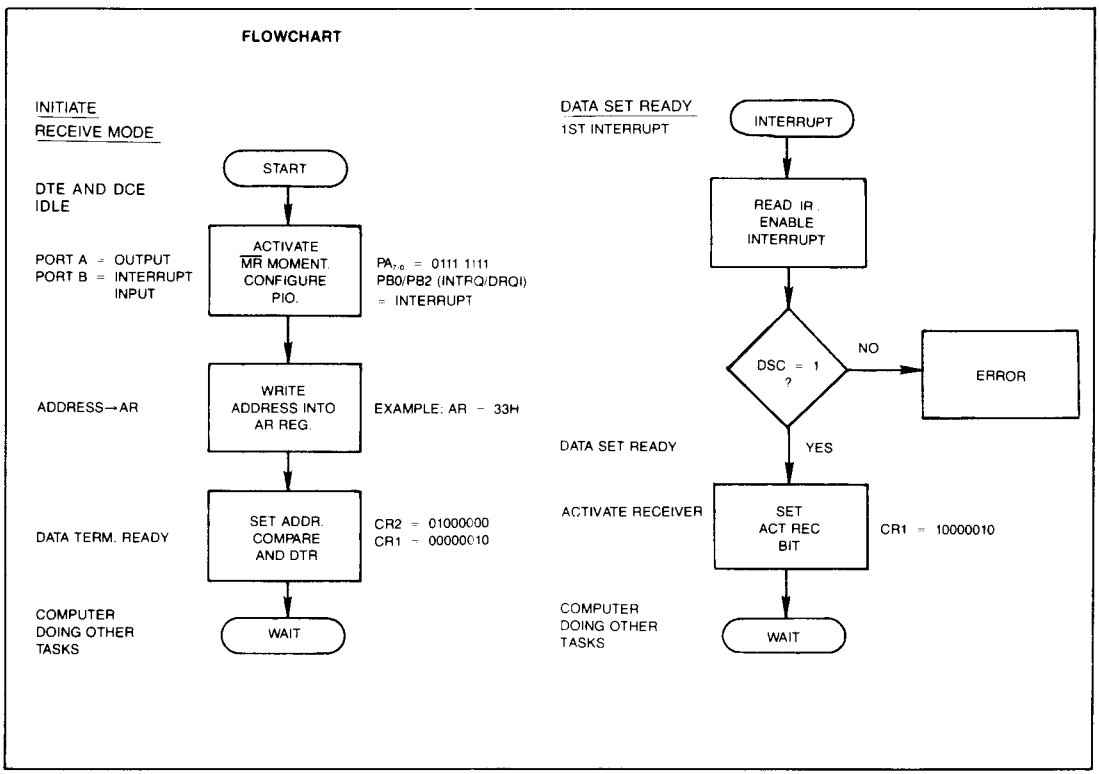


Figure 21. FLOW DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 1)

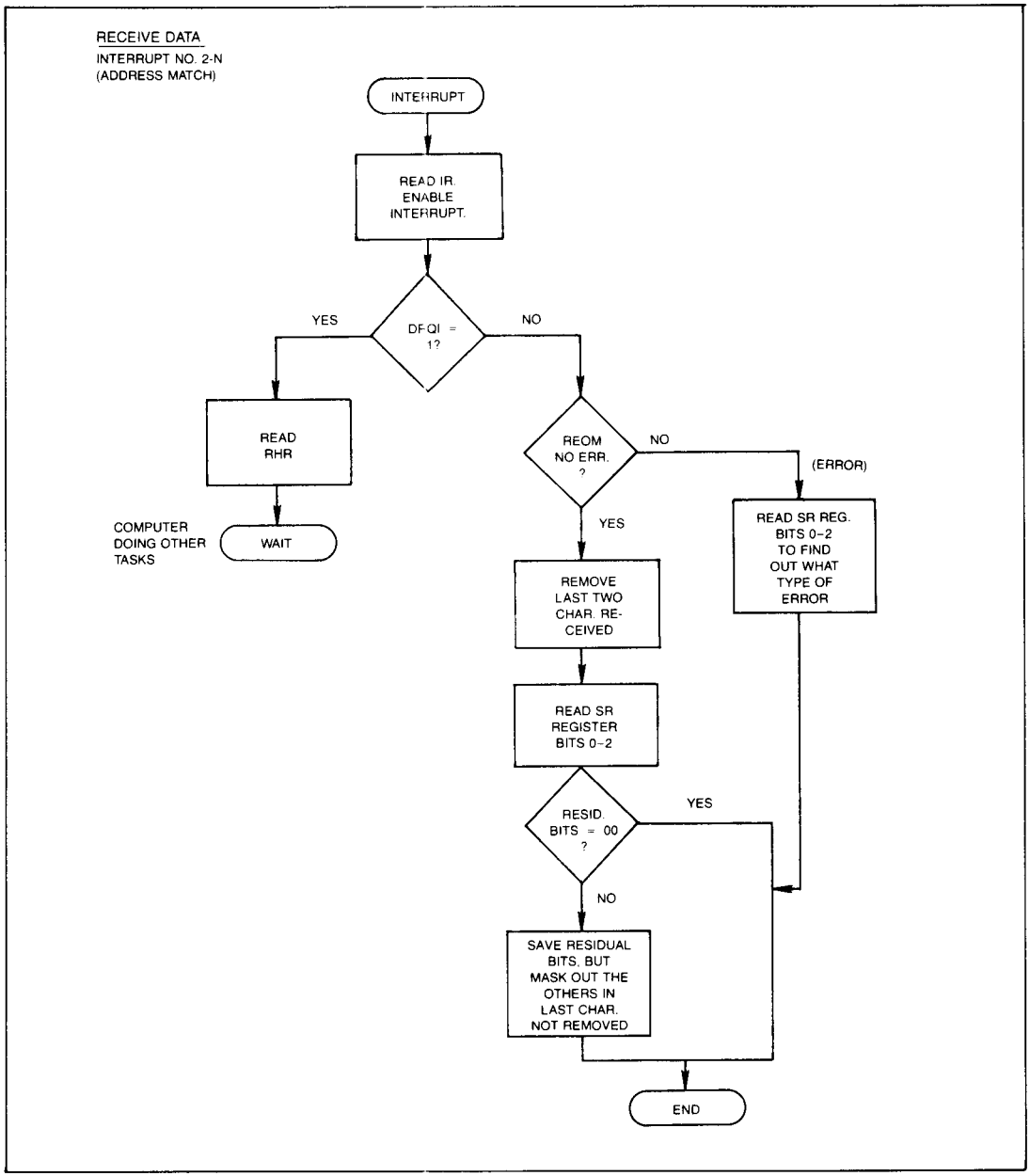


Figure 21. FLOW DIAGRAM OF FRAME RECEPTION

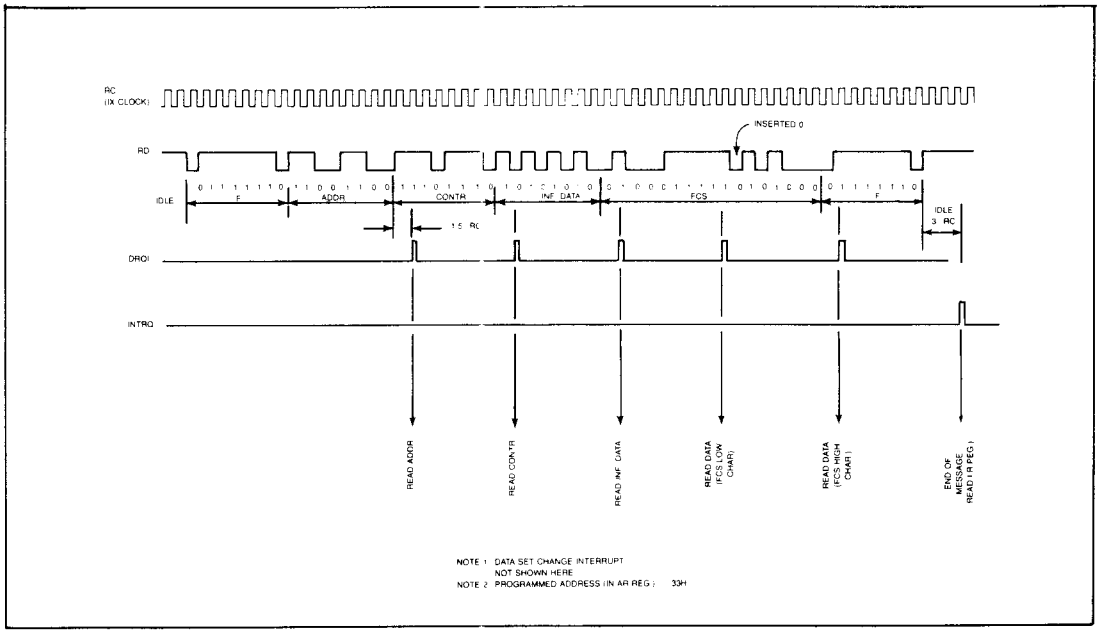


Figure 22. TIMING DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 1)

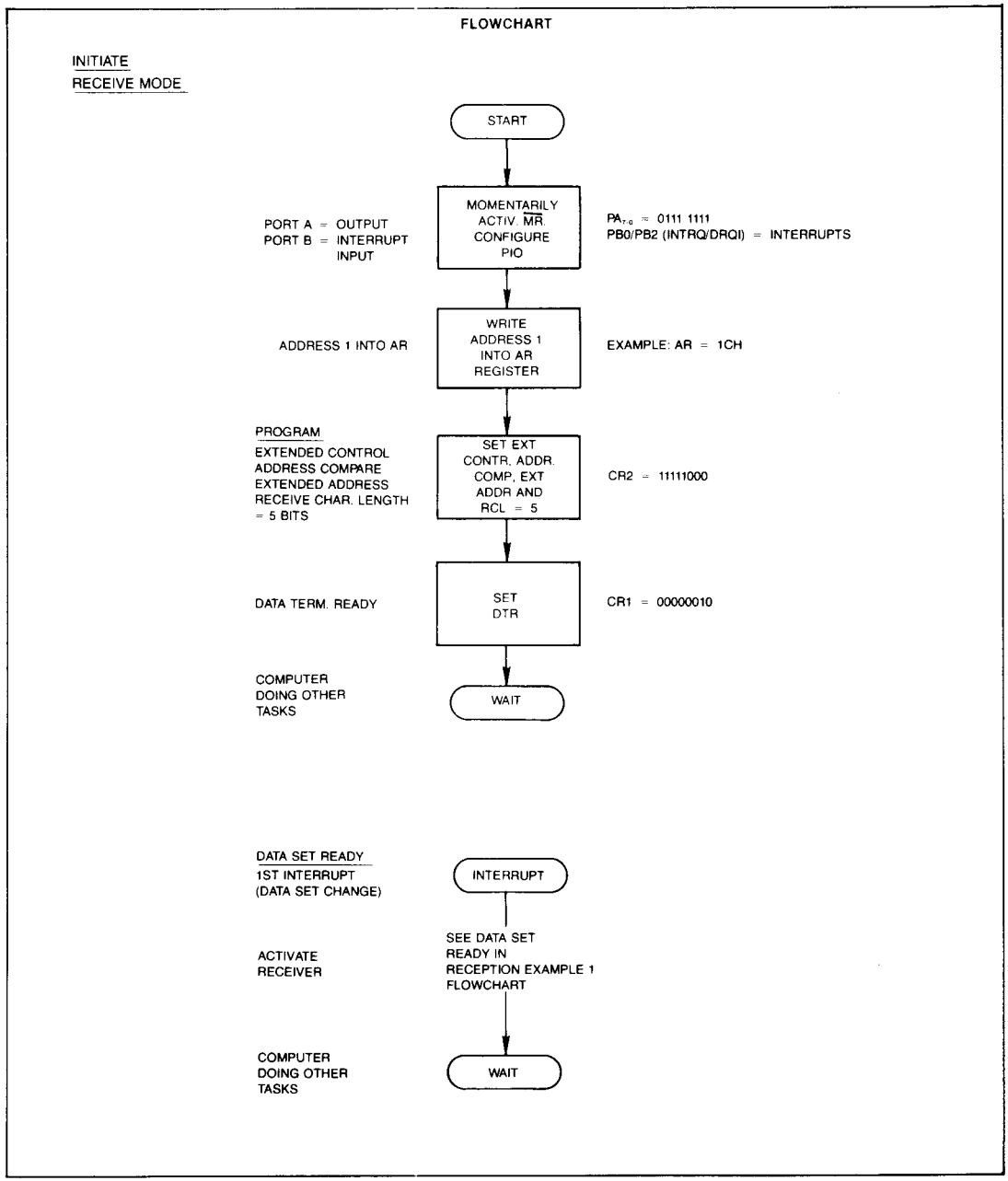


Figure 23. FLOW DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 2)

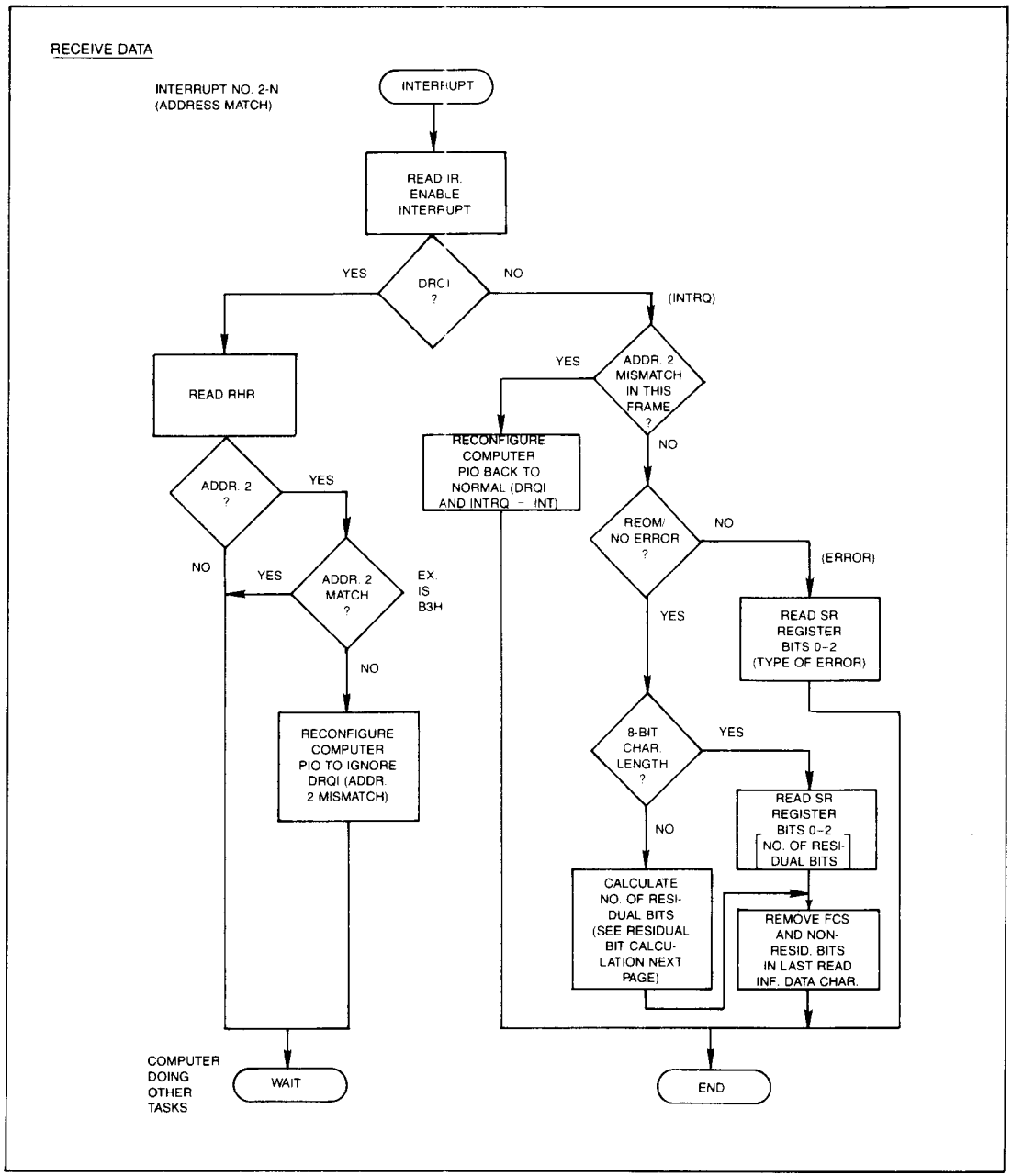


Figure 23. FLOW DIAGRAM OF FRAME RECEPTION

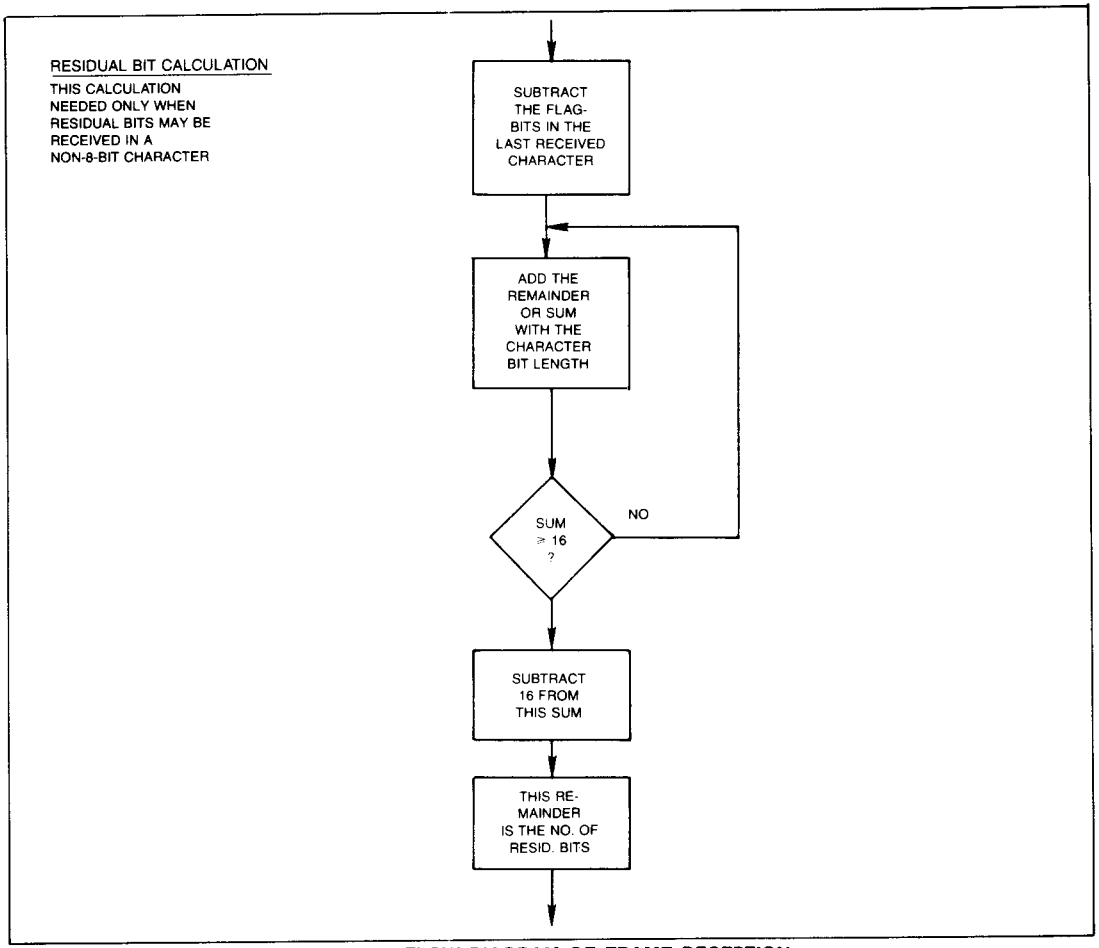


Figure 23. FLOW DIAGRAM OF FRAME RECEPTION

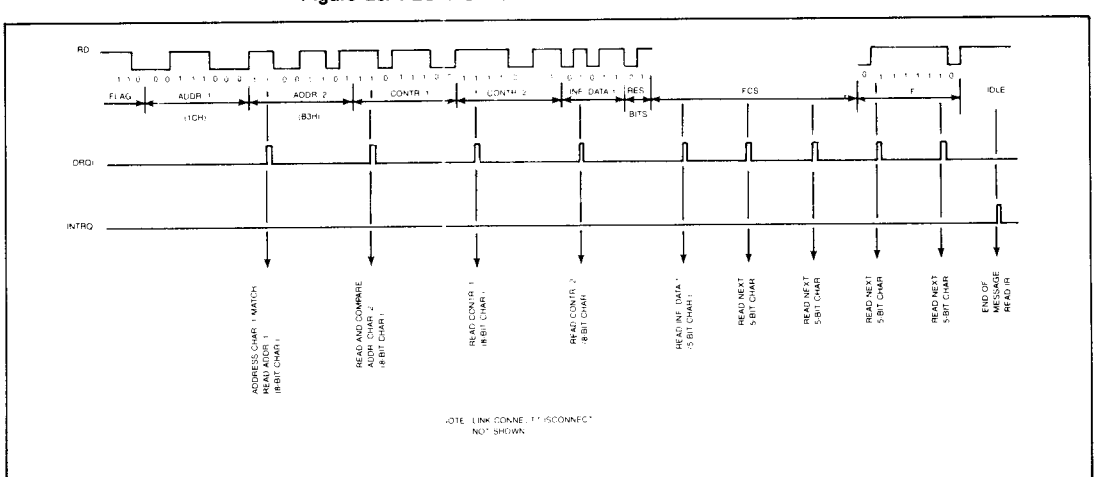


Figure 24. TIMING DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 2)

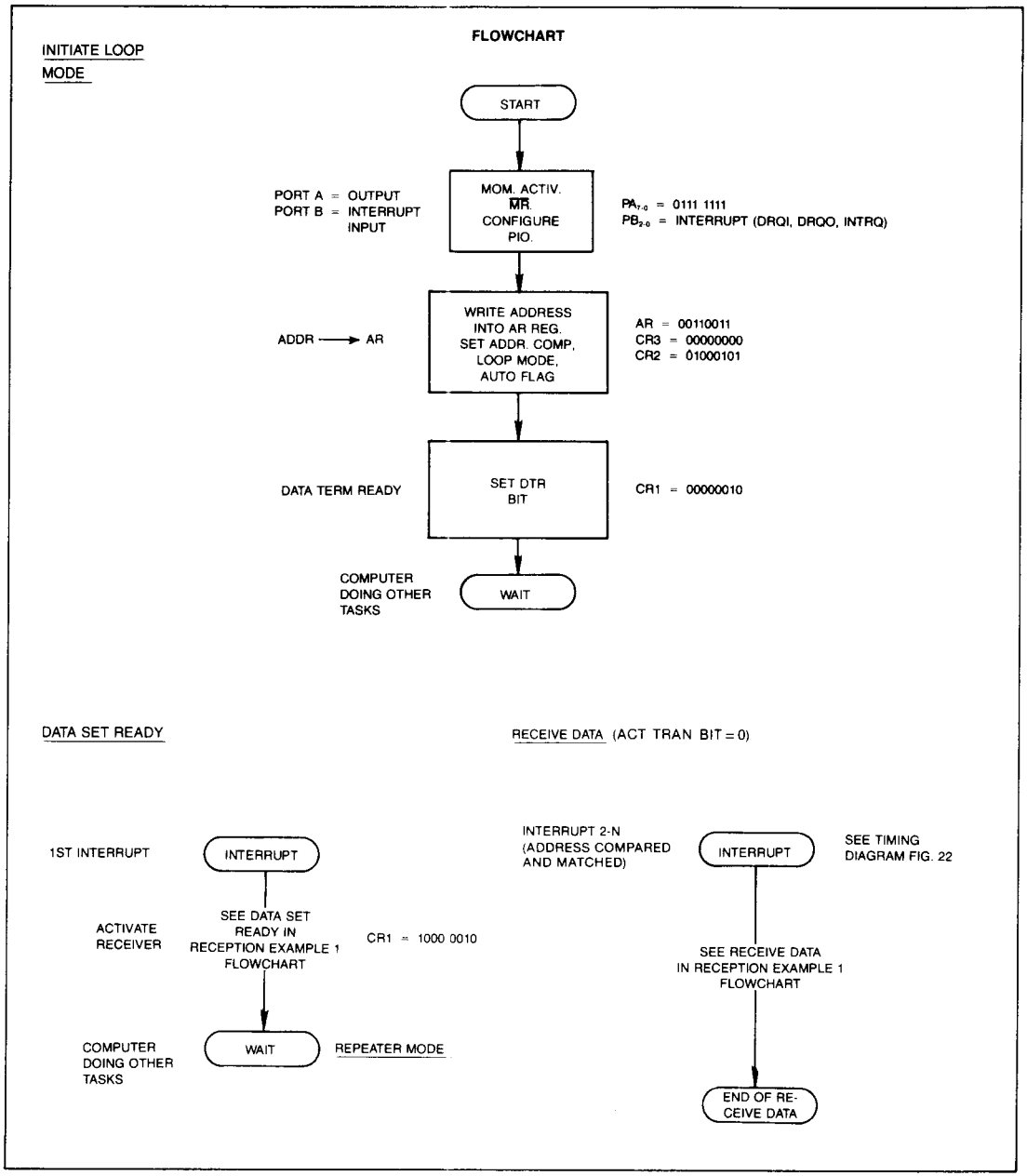


Figure 25. FLOW DIAGRAM OF SDLC LOOP MODE OPERATION

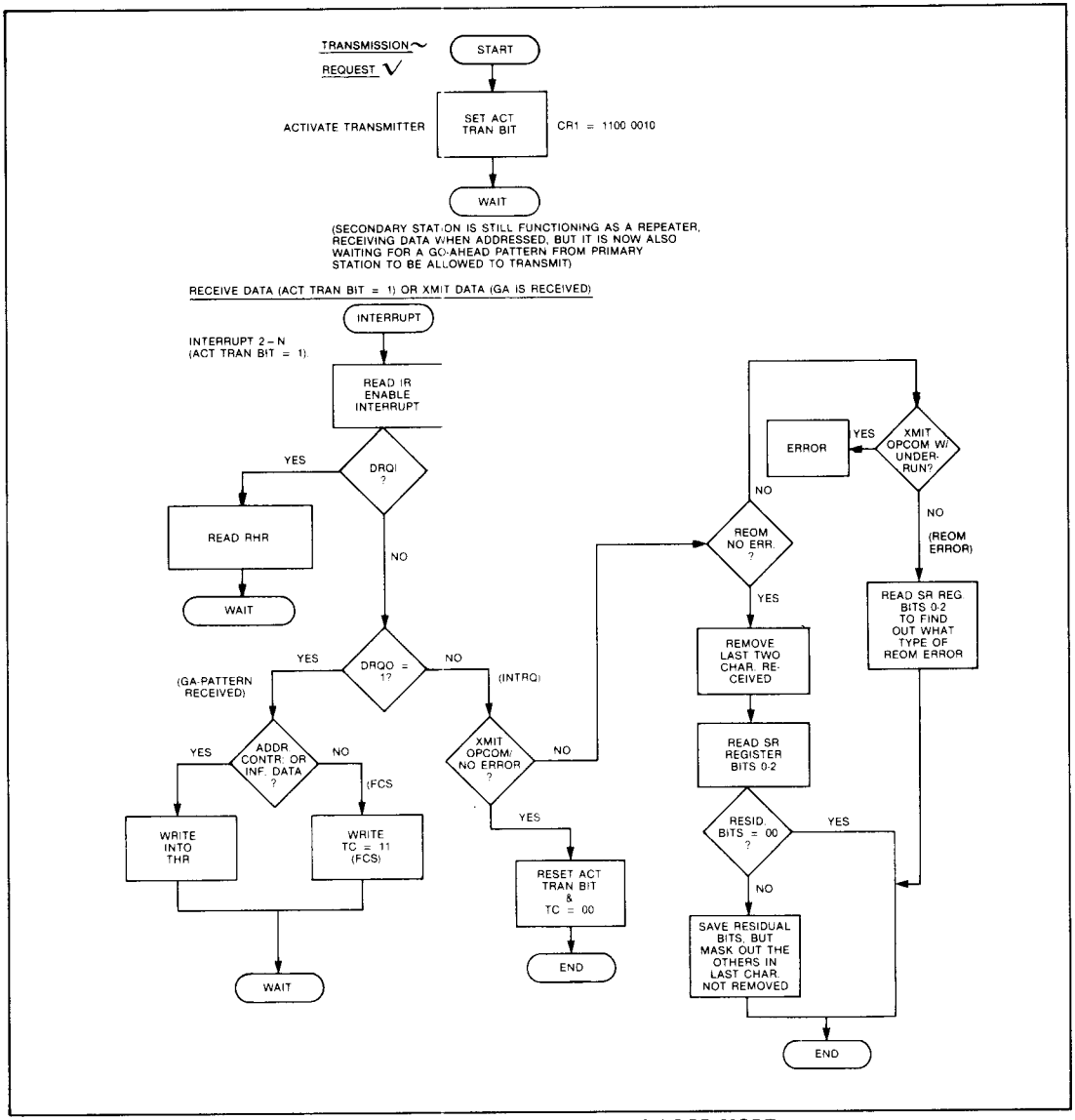


Figure 25. FLOW DIAGRAM OF SDLC LOOP MODE

CONCLUSION

The WD1931 and WD1933 devices are highly compatible, which allows the design of a multiprotocol communications board. This compatibility allows the use of asynchronous, character oriented synchronous, and bit oriented synchronous communications protocols with the same 40 pin socket.

APPENDIX

RELATED DOCUMENTS

WD1931 Data Sheet, Western Digital Corporation
WD1933 Data Sheet, Western Digital Corporation

Printed in U.S.A.