82S16
256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S16 is a Read/Write memory array which features 3-state outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

The 82S16 has fast Read access and Write cycle times, and thus is ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Ordering information can be found on the following page.

The 82S16 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

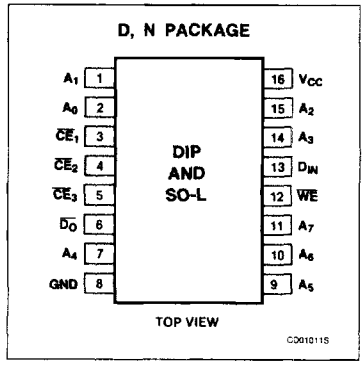
FEATURES

- **Address access time: 50ns max**
- **Write cycle time: 50ns max**
- **Power dissipation: 1.5mW/bit typ**
- **Input loading: −100μA max**
- **Output follows complement of data input during Write**
- **Three chip enable inputs**
- **On-chip address decoding**
- **Output: Three-state**
- **Schottky clamped**
- **TTL compatible**

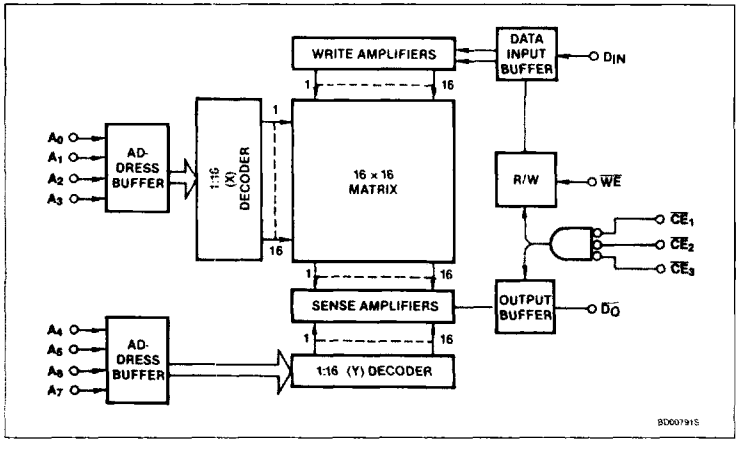
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar RAM (256 x 1) — 82S16

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82S16 N
Plastic Small outline 300mil wide 16-pin	N82S16 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	V_{dc}
V_{IN}	Input voltage	+5.5	V_{dc}
V_{OUT}	Output voltage High	+5.5	V_{dc}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = max	2.0			V
V_{IL}	Low	V_{CC} = min			0.8	
V_{IC}	Clamp[3]	V_{CC} = min, I_{IN} = −12mA		−1.0	−1.5	
Output voltage[2]		V_{CC} = min				
V_{OH}	High	I_{OH} = −3.2mA	2.6			V
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45	
Input current[3]		V_{CC} = max				
I_{IH}	High	V_{IN} = 5.5V		1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	
Output current						
I_{OZ}	Hi-Z State[6]	V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit[7]	V_{CC} = max, V_O = 0V	−15		−70	mA
Supply current[8]						
I_{CC}		V_{CC} = 5.25V		80	115	mA
Capacitance		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	Hi-Z

*"0" = All $\overline{CE}$ inputs Low; "1" = One or more $\overline{CE}$ inputs High. X = Don't care.

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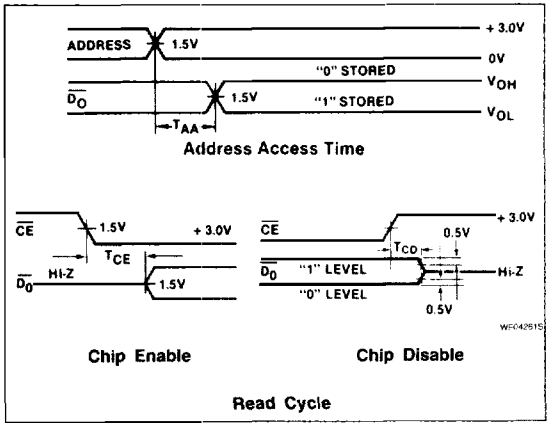
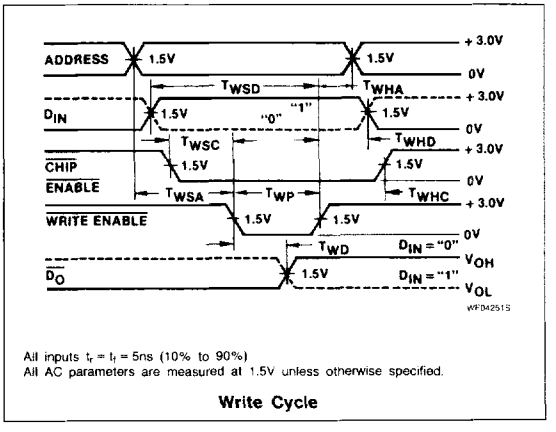
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Access time							
T_{AA}	Address	Output	Address		40	50	ns
T_{CE}	Chip enable	Output	Chip enable		30	40	
Disable time[10]							
T_{CD}		Output	Chip enable		30	40	ns
T_{WD}	Valid time	Output	Write enable		30	40	
Set-up and hold time							
T_{WSA}	Set-up time	Write enable	Address	15	5		ns
T_{WHA}	Hold time			5	0		
T_{WSD}	Set-up time	Write enable	Data in	40	30		
T_{WHD}	Hold time			5	0		
T_{WSC}	Set-up time	Write enable	$\overline{CE}$	10	0		
T_{WHC}	Hold time			5	0		
Pulse width[9]							ns
T_{WP}	Write enable			30	15		

NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, and $C_L = 5pF$.

TIMING DIAGRAMS





MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of chip enable low (with address valid) and when data output becomes valid.

T_{CD} Delay between when chip enable becomes high and data output is in off state.

T_{AA} Delay between beginning of valid address (with chip enable low) and when data output becomes valid.

T_{WSC} Required delay between beginning of valid chip enable and beginning of Write enable pulse.

T_{WHD} Required delay between end of Write enable pulse and of valid input data.

T_{WP} Width of Write enable pulse.

T_{WSA} Required delay between beginning of valid address and beginning of Write enable pulse.

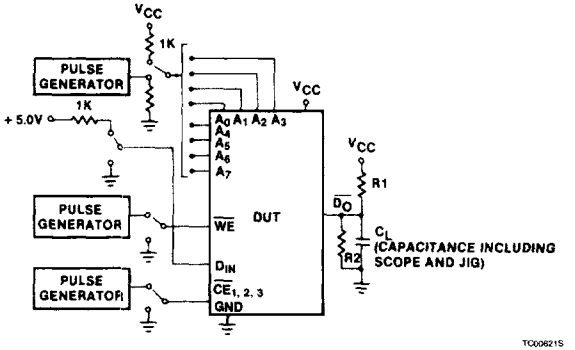
T_{WSD} Required delay between beginning of valid data input and end of Write enable pulse.

T_{WD} Delay between beginning of Write enable pulse and when data output reflects complement of data input.

T_{WHC} Required delay between end of Write enable pulse and end of chip enable.

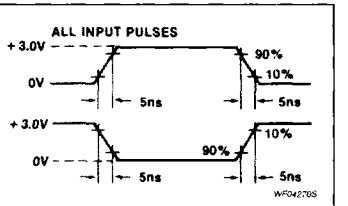
T_{WHA} Required delay between end of Write enable pulse and end of valid address.

TEST LOAD CIRCUIT



Loading Condition

VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the+ 1.5 level of inputs and output.

Input Pulses