Am25LS181 • Am54LS/74LS181

Four-Bit Arithmetic Logic Unit/Function Generator

DISTINCTIVE CHARACTERISTICS

- Performs 16 arithmetic operations including add, subtract, double and compare
- Full look-ahead capability for high speed arithmetic operation on long words
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL}
  - Twice the fan-out over military range
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am25LS181 is a 4-bit, high-speed parallel Arithmetic Logic Unit (ALU)/Digital Function Generator. When the mode control (M) is LOW the 16 arithmetic operations are performed under the control of the four select inputs. When the mode control is HIGH the sixteen logic operations are performed on an individual bit basis between the two 4-bit parallel words under the control of the four select inputs.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision is made for further look-ahead by including both carry propagate (P) and carry generate (G) outputs.

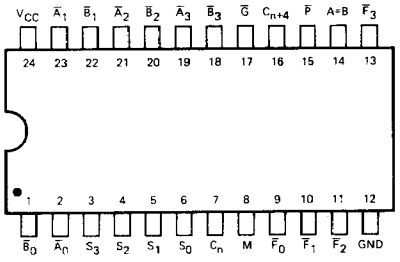
An open collector output A = B is used to signal the equivalence of the two parallel words. The open collector feature allows for the equivalence function to be expanded as a wired-AND connection for larger word lengths.

In many systems, the carry output C_{n+4} is connected to the next higher C_n to provide ripple block arithmetic. The ALU can be used with either active HIGH or active LOW inputs and can be ripple expanded or full look-ahead expanded in either mode. The connection pattern is identical for either logic representation.

The Am54LS/74LS181 is a standard performance version of the Am25LS181. See appropriate electrical characteristic tables for detailed Am25LS improvements.

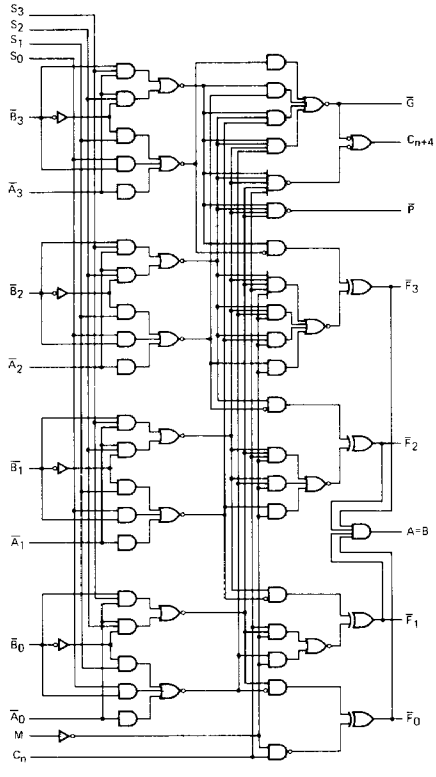
CONNECTION DIAGRAM

Top View

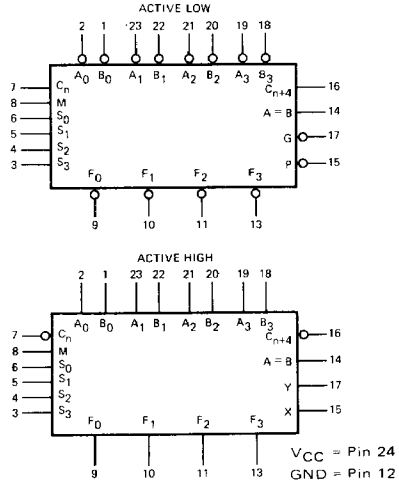


Note: Pin 1 is marked for orientation.

LOGIC DIAGRAM



LOGIC SYMBOLS



Am25LS181
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Except A = B Output)	V_{CC} = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 4mA				0.4	Volts
			I_{OL} = 8mA				0.45	
			$\overline{G}$, I_{OL} = 16mA				0.55	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{OH}	Output HIGH Current for A = B Output	V_{CC} = MIN., $V_{OH} = 5.5V$, $V_{IN} = V_{IH}$ or V_{IL}					100	μA
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$		M			−0.36	mA
				$\overline{A}_i$ or $\overline{B}_i$			−1.08	
				S_i			−1.44	
				C_n			−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$		M			20	μA
				$\overline{A}_i$ or $\overline{B}_i$			60	
				S_i			80	
				C_n			100	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5V$		M			0.1	mA
				$\overline{A}_i$ or $\overline{B}_i$			0.3	
				S_i			0.4	
				C_n			0.5	
I_{SC}	Output Short Circuit Current (Note 3) (Except A = B Output)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.	A	MIL		20	32	mA
				COM'L		20	34	
			B	MIL		21	35	
				COM'L		21	37	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured under two conditions — typ. and max. apply to both.
   A. S_i, M, A_i at 4.5V; all other inputs grounded; outputs open.
   B. S_i, M at 4.5V; all other inputs grounded; outputs open.

Am25LS • Am54LS/74LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS181

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Except A = B Output)	V_{CC} = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or V_{IL}	MIL		2.5	3.4		Volts
			COM'L		2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	All outputs, I_{OL} = 4mA			0.25	0.4	Volts
			Am74LS only All outputs, I_{OL} = 8mA			0.35	0.5	
			$\overline{G}$, I_{OL} = 16 mA			0.47	0.7	
			$\overline{P}$, I_{OL} = 8mA			0.35	0.6	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL				0.7	Volts
			COM'L				0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{OH}	Output HIGH Current for A = B Output	V_{CC} = MIN., V_{OH} = 5.5V, $V_{IN} = V_{IH}$ or V_{IL}					100	μA
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	M				−0.36	mA
			$\overline{A_i}$ or $\overline{B_i}$				−1.08	
			S_i				−1.44	
			C_n				−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	M				20	μA
			$\overline{A_i}$ or $\overline{B_i}$				60	
			S_i				80	
			C_n				100	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V	M				0.1	mA
			$\overline{A_i}$ or $\overline{B_i}$				0.3	
			S_i				0.4	
			C_n				0.5	
I_{SC}	Output Short Circuit Current (Note 3) (Except A = B Output)	V_{CC} = MAX.			−15		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.	A	MIL		20	32	mA
				COM'L		20	34	
			B	MIL		21	35	
				COM'L		21	37	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured under two conditions — typ. and max. apply to both.
   A. S_i, M, A_i at 4.5V; all other inputs grounded; outputs open.
   B. S_i, M at 4.5V; all other inputs grounded; outputs open.

Am25LS181 • Am54LS/74LS181
SWITCHING CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5.0V)
(C_L = 15pF, R_L = 2.0kΩ)

Parameter	From (Input)	To (Output)	Am25LS181 Min.	Am25LS181 Typ.	Am25LS181 Max.	Am54LS/74LS181 Min.	Am54LS/74LS181 Typ.	Am54LS/74LS181 Max.	Units	Test Conditions
t_{PLH}	C_n	C_{n+4}			25		18	27	ns	
t_{PHL}					14		13	20		
t_{PLH}	C_n	$\overline{F}_i$			19		17	26	ns	M = 0V (SUM or DIFF mode)
t_{PHL}					18		13	20		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$			25		19	29	ns	M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode)
t_{PHL}					23		15	23		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$			25		21	32	ns	M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}					25		17	26		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$			26		20	30	ns	M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode)
t_{PHL}					26		20	30		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$			26		20	30	ns	M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}					26		22	33		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$ (j ≥ i)			28		21	32	ns	M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode)
t_{PHL}					19		13	20		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$ (j ≥ i)			30		21	32	ns	M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}					19		15	23		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$			31		22	33	ns	M = 4.5V (LOGIC mode)
t_{PHL}					25		19	29		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}			33		25	38	ns	M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ =0V (SUM mode)
t_{PHL}					31		25	38		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}			35		27	41	ns	M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}					35		27	41		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	A = B			50		33	50	ns	M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}					45		41	62		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_{i+1}$			36				ns	$S_1 = S_2$ = M = 0V $S_0 = S_3$ = 4.5V (SUM mode)
t_{PHL}					53					
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_{i+1}$			36				ns	$S_0 = S_3$ = M = 0V $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}					53					

OPERATION TABLE

SELECTION				ACTIVE-HIGH DATA			ACTIVE-LOW DATA		
				M = H	M = L; Arithmetic Operations		M = H	M = L; Arithmetic Operations	
S_3	S_2	S_1	S_0	Logic Functions	C_n = H (No Carry)	C_n = L (With Carry)	Logic Functions	C_n = L (No Carry)	C_n = H (With Carry)
L	L	L	L	F = $\overline{A}$	F = $\overline{A}$	F = A Plus 1	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L	L	H	H	F = 0	F = Minus 1 (2's Compl.)	F = Zero	F = 1	F = Minus 1 (2's Compl.)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1	F = $\overline{B}$	F = AB Plus (A + $\overline{B}$)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1	F = A ⊕ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

(C_L = 50pF, R_L = 2.0kΩ)

Parameters	From (Input)	To (Output)	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	C_n	C_{n+4}		37		42	ns	
t_{PHL}				22		26		
t_{PLH}	C_n	$\overline{F}_i$		29		33	ns	M = 0V (SUM or DIFF mode)
t_{PHL}				28		32		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$		37		42	ns	M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode)
t_{PHL}				34		39		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$		37		42	ns	M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 0V (DIFF mode)
t_{PHL}				37		42		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$		38		44	ns	M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode)
t_{PHL}				38		44		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$		38		44	ns	M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}				38		44		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$ (j ≥ i)		41		47	ns	M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode)
t_{PHL}				29		33		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$ (j ≥ i)		43		50	ns	M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}				29		33		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$		44		51	ns	M = 4.5V (LOGIC mode)
t_{PHL}				37		42		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}		47		54	ns	M = 0V, S_0 = S_3 4.5V, $S_1 = S_2$ = 0V (SUM mode)
t_{PHL}				44		51		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}		50		57	ns	M = 0V, S_0 = S_3 0V, $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}				50		57		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	A = B		69		80	ns	M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}				62		72		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_{i+1}$		51		59	ns	$S_1 = S_2$ = M = 0V, $S_0 = S_3$ = 4.5V (SUM mode)
t_{PHL}				69		80		
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_{i+1}$		51		59	ns	$S_0 = S_3$ = M = 0V, $S_1 = S_2$ = 4.5V (DIFF mode)
t_{PHL}				69		80		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

$\overline{A}_0, \overline{A}_1, \overline{A}_2, \overline{A}_3$ The A data inputs.

$\overline{B}_0, \overline{B}_1, \overline{B}_2, \overline{B}_3$ The B data inputs.

S_0, S_1, S_2, S_3 The control inputs used to determine the arithmetic or logic function performed.

$\overline{F}_0, \overline{F}_1, \overline{F}_2, \overline{F}_3$ The data outputs of the ALU.

M The mode control inputs used to select either the arithmetic or logic operations.

C_n The carry-in input of the ALU.

C_{n+4} The carry-look-ahead output of the four-bit input field.

$\overline{G}$ The carry-generate output for use in multi-level look-ahead schemes.

$\overline{P}$ The carry-propagate output for use in multi-level look-ahead schemes.

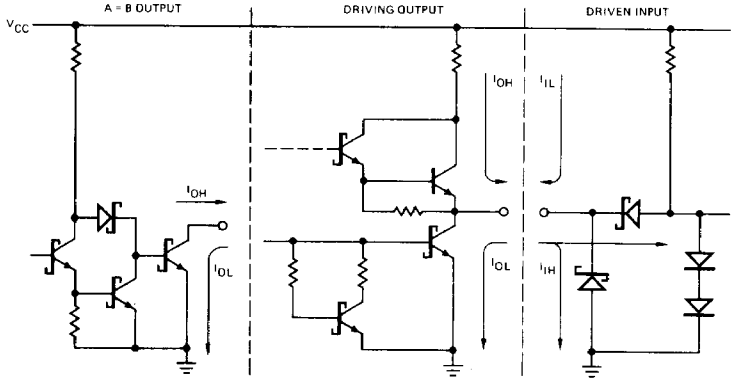
A = B The open collector comparator output that can be used to determine equivalence. This output is HIGH whenever the four $\overline{F}$ outputs are HIGH.

USER NOTES

1. Throughout this data sheet, the active LOW input and output terminology has been used. For the active HIGH definition, the nomenclautre shown under the active HIGH logic symbol should be substituted.
2. Arithmetic operations are performed on a word basis.
3. Logic operations are performed on a bit basis.
4. Arithmetic in 1's complement notation requires an end around carry.
5. Subtraction in 2's complement notation requires a carry in (C_n = HIGH) for the active LOW case and ($\overline{C}_n$ = LOW) for the active HIGH case.
6. The A = B output only indicates that the four $\overline{F}$ outputs are all HIGH.

3

LOW POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

Parameter	Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply 0V	Apply 4.5V	Apply 0V		
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}	In-Phase

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

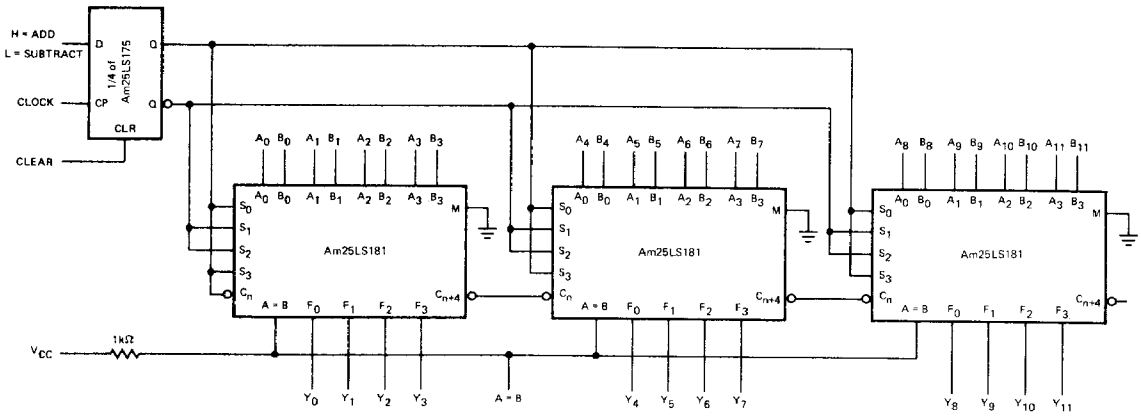
Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply 0V	Apply 4.5V	Apply 0V		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase

LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = M = 4.5V$, $S_0 = S_3 = 0V$

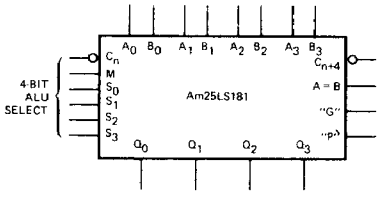
Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply 0V	Apply 4.5V	Apply 0V		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase

APPLICATIONS



12-BIT ADDER/SUBTRACTOR (2's COMPLEMENT)

If one input is defined active–HIGH and the second input is defined active–LOW, the sixteen arithmetic and logic functions of the ALU are reordered as shown in the function table.



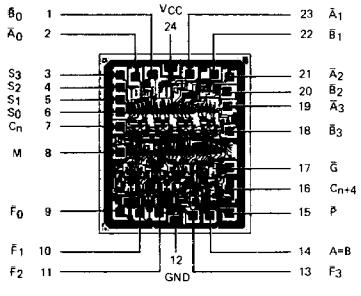
FUNCTION TABLE

A = Active HIGH B = Active LOW

S_0	S_1	S_2	S_3	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L	L	L	L	A	$\overline{A}$
H	L	L	L	A + $\overline{B}$	$\overline{A}$B
L	H	L	L	A + B	$\overline{A\overline{B}}$
H	H	L	L	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus AB	AB
H	L	H	L	AB plus [A + $\overline{B}$]	B
L	H	H	L	A plus B	$\overline{A} \oplus \overline{B}$
H	H	H	L	AB minus 1	AB
L	L	L	H	A plus A$\overline{B}$	$\overline{A} + \overline{B}$
H	L	L	H	A minus B minus 1	A $\oplus$ B
L	H	L	H	A$\overline{B}$ plus [A + B]	$\overline{B}$
H	H	L	H	A$\overline{B}$ minus 1	A$\overline{B}$
L	L	H	H	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus [A + $\overline{B}$]	A + B
L	H	H	H	A plus [A + B]	A + $\overline{B}$
H	H	H	H	A minus 1	A

L = Low Voltage Level
H = High Voltage Level

Metallization and Pad Layout



DIE SIZE: 0.078" X 0.092"