AK5420

10Bit 20MHz A/D Converter

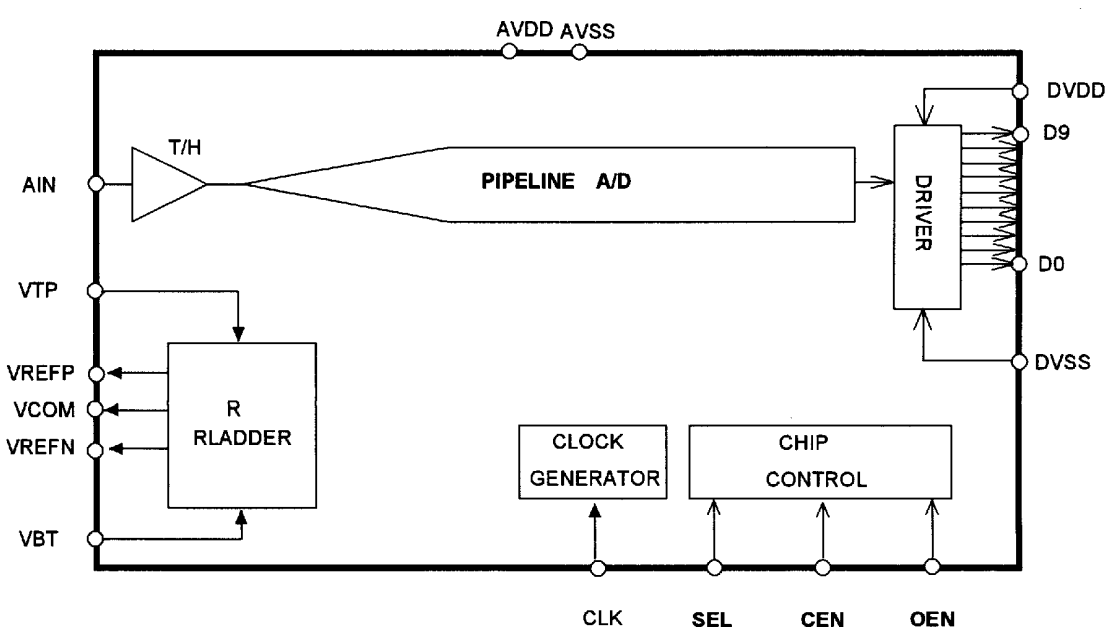
Outline

AK5420is a 3V CMOS, 20MSPS(MAX),10bit,Analog to Digital(A/D) Converter.

Features

DRAFT

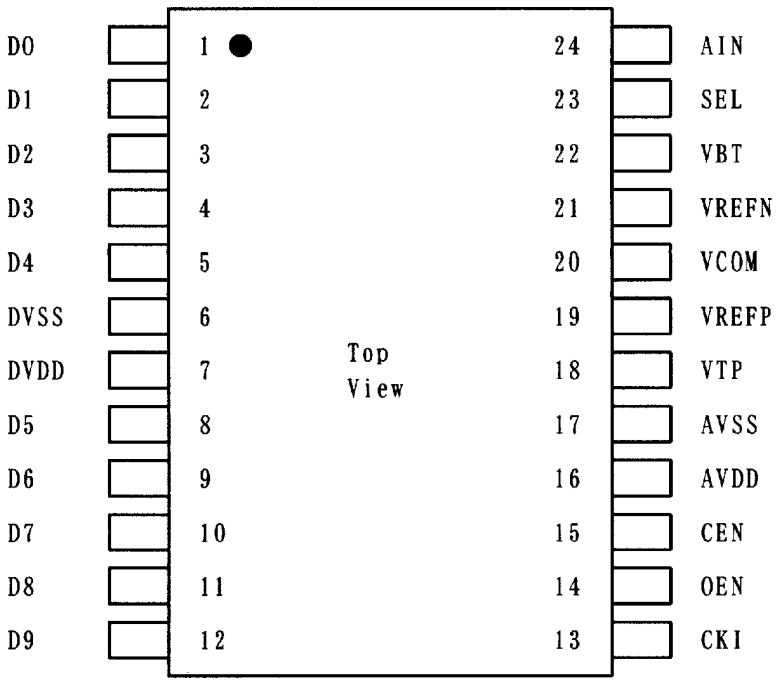
- ☐ Monolithic CMOS A/D Converter
- ☐ Sampling Rate : 20 MSPS(MAX)
- ☐ Resolution : 10 Bit
- ☐ Power Supply Voltage : 2.7V.... +3.6V
- ☐ Analog Input : Single End
- ☐ Analog Input Range,Vref Range
  - DRANGE : 1 Vpp
  - VBOT : 0.9 ~ 1.6 V
  - VTOP : 1.9 ~ 2.6 V
  - (VTOP < AVDD - 0.6V)
- ☐ Low Offset Voltage : ±30mV
- ☐ Linearity Differential(DNL) : ±0.5 LSB(TYP.)
  - Integral (INL) : ±1.5 LSB(TYP.)
- ☐ Tristate Digital Output available
- ☐ Stand-by mode
- ☐ Compact Package : 24pin VSOP
- ☐ Low Power Consumption : 30 mW (TYP.@20MHz mode)
  - 24 mW (TYP.@15MHz mode)
  - (EXCLUDING OUTPUT DRIVE CURRENT)



■ **Ordering Guide**

AK5420 -20°C ~ +85°C 24 Pin VSOP

■ **Pin Assignment**



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■ **Pin Descriptions [24VSOP]**

PIN NO.	Symbol	Type	Description & Function
1	D0	O	DIGITAL OUTPUT D0(LSB) Hi Impedance when OEN or CEN is high
2	D1	O	DISITAL OUTPUT D1 Hi Impedance when OEN or CEN is high
3	D2	O	DIGITAL OUTPUT D2 Hi Impedance when OEN or CEN is high
4	D3	O	DIGITAL OUTPUT D3 Hi Impedance when OEN or CEN is high
5	D4	O	DIGITAL OUTPUT D4 Hi Impedance when OEN or CEN is high
6	DVSS	P	Digital Ground Pin
7	DVDD	P	Digital Power Supply Pin (2.7 ... 3.6V)
8	D5	O	DIGITAL OUTPUT D5 Hi Impedance when OEN or CEN is high
9	D6	O	DIGITAL OUTPUT D6 Hi Impedance when OEN or CEN is high
10	D7	O	DIGITAL OUTPUT D7 Hi Impedance when OEN or CEN is high
11	D8	O	DIGITAL OUTPUT D8 Hi Impedance when OEN or CEN is high
12	D9	O	DIGITAL OUTPUT D9(MSB) Hi Impedance when OEN or CEN is high
13	CKI	I	CLOCK Input Input Pin for Sampling Clock
14	OEN	I	OUTPUT ENABLE Output(D0…D9) is active at OEN=LOW, Hi-impedance when HIGH
15	CEN	I	CHIP ENABLE(Power Down Control) LOW:Normal Operating Mode High: Power down & All Digital Output= High-Z
16	AVDD	P	Analog Power Supply Pin (2.7 ... 3.6V)
17	AVSS	P	Analog Ground Pin
18	VTP	I	VREF Top Voltage Input Pin[To set Analog Input Range] VIN Full Scale Reference pin.
19	VREFP	O	VREF Voltage for internal circuit Place 0.1uF Ceramic Cap. between AVSS.
20	VCOM	O	VREF Voltage for internal circuit Place 0.1uF Ceramic Cap. between AVSS.
21	VREFN	O	VREF Voltage for internal circuit Place 0.1uF Ceramic Cap. between AVSS.
22	VBT	I	VREF Bottom Voltage Input Pin[To set Analog Input Range] VIN Zero Scale Reference pin.
23	SEL	I	Sampling Frequency SELECT Upper Limit of Sampling Clock(CKI) Frequency is determined by this pin. VSS : 20MHz mode VDD : 15MHz mode
24	AIN	I	Analog Input

ABSOLUTE MAXIMUM RATINGS

(AVSS,DVSS=0V,All voltages are with respect to GND)

Parameter	Symbol	Conditions	Ratings	Units
Power Supply Voltage				
	AVDD		-0.3 ~ 4.5	V
	DVDD		-0.3 ~ 4.5	V
		(#1)	or (AVDD+0.3)	V
Voltage Difference	Vdlt	DVDD - AVDD	0.3	V
Input Current	IIN	Except Power Pins	+-10	mA
Analog Input Voltage Range	VINA		AVSS - 0.3 ~ AVDD + 0.3	V
Digital Input Voltage [Input Pins]	VINL		AVSS - 0.3 ~ AVDD + 0.3	V
Digital Input Voltage [Output Pins]	VONL	(#2)	AVSS - 0.3 ~ AVDD + 0.3	V
Ambient Temperature	TA		-20~85	°C
Storage Temperature	Tstg		-40~+125	°C

(# 1) The higher voltage of 4.5V and AVDD + 0.3V specifies Max. value of DVDD absolute maximum rating.

(# 2) The VONL limits the excess voltage applied to digital output pins.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal Operating Specifications are not guaranteed at these extremes.

Recommended Operating Conditions

1. Power Supply Requirements

(DVSS,AVSS=0V,(#1))

Parameter		Symbol	Condition	min	typ	max	Units
Supply Voltage	[Analog]	AVDD	(# 2)	2.7	3.0	3.6	V
	[Digital]	DVDD		2.7	3.0	AVDD	V

(# 1) All voltages are with respect to GND

(# 2) At start-up , power-on AVDD before(or at the same time to) DVDD power-on.

2. Reference Input

Applicable Voltage to Top/Bottom Reference Voltage(VTOP,VBOT)changes according to Power Supply Voltage[AVDD].

The Analog Input Range[Conversion D-range] is determined based on VTOP & VBOT Voltage [which is applied to VTP/VBT pins] . Note that the AINFS[Analog Input Range] must satisfy the following range.

Parameter	Symbol	Conditions	min	typ	max	Units
Analog Input Range	AINFS	(#1)	0.9	1.0	1.1	Vpp
Reference Bottom Voltage	VBTE	(#2)	0.9	1.3	1.6	V
Reference Top Voltage	VTPE	(#2) (#3)	1.9	2.3	2.6	V
Reference Input Impedance	ZTBE	VBT-VTP		100		KOHM

(#1) : AINFS=VTPE – VBTE
Note that AFINFS is the ADC operating input voltage range (Analog Characteristics are not always guaranteed.)

(#2) : Adjust both of these voltages[VBTE/VTPE] to satisfy the AINFS spec. The voltage difference VTPE-VBTE must meet the above AINFS spec.

(#3) : Acceptable external VREF voltage varies according to the Power Supply Voltage[AVDD].
VTPE < AVDD - 0.6V

Specifications

1)Analog Specifications

(AVDD=DVDD=3.0V, VBT=1.3V,VTP=2.3V, Ta=25°C,
Fs=20MHz, Signal frequency Fin=1MHz,Signal level =-1dB , unless otherwise noted)

Parameter	Symbol	Conditions	min	typ	max	Units	
Resolution	RES				10	BITS	
Integral Nonlinearity[INL]	INL	Fs=20MHz (@20MHz mode)		±1.5	TBD	LSB	
Differential Nonlinearity[DNL]	DNL	Fs=15MHz (@15MHz mode)		±0.5	TBD	LSB	
Offset Voltage	EOB	TO VBT	-30		+30	mV	
	EOT	TO VTP (#1)	-30		+30	mV	
Input Resistance	RIN	@Fs=20MHz(#2)		70		KOHM	
Input Capacitance	CIN			10		pF	
Input Bandwidth	BW	-3dB		TBD		MHz	**

(#1) Offset Voltage is the difference of Transition input voltage to All Zero [All One] and VBT[VTP].
(#2) Input Resistance[RIN] is specified as the equivalent impedance from Analog Input Pins[AIN] to ADC common voltage[center voltage between VTP & VBT]. RIN is proportional to 1/FS.

2) Power Supply

(Ta=25 °C ;AVDD=DVDD=3.0V; VTP=2.3V, VBT=1.3V)

Parameter	Symbol	Conditions	min	typ	max	Units
Analog Operating Current (@CEN=LOW)	IA+	Fin=1MHz @Fs=20MHz @Fs=15MHz(#1)		10 8	15 12	mA mA
Digital Output Driver Operating Current (@CEN=LOW)	ID+	Fin=1MHz (#2) @Fs=20MHz @Fs=15MHz(#1)		5.0 3.5	8.0 7.0	mA mA
Stand-by Current (@CEN=HIGH)	IAS IDS	Analog (#3) Digital			0.1 0.1	mA mA

(#1) 15MHz mode is selected by SEL=Low.

(#2) Capacitor Loads [CL=10pF] are attached to all digital output pins[D0..D9].
Analog Input Signal is 1MHz Sine Wave.

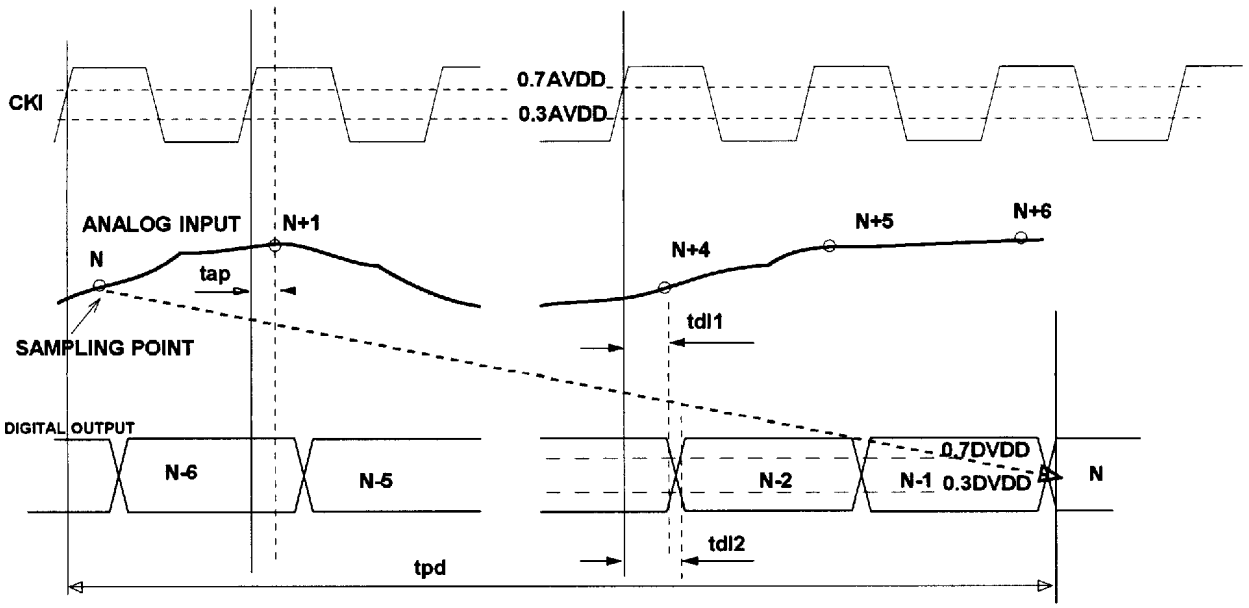
(#3) The Stand-by Current is measured under
*No Analog Input *CKI= Low fixed

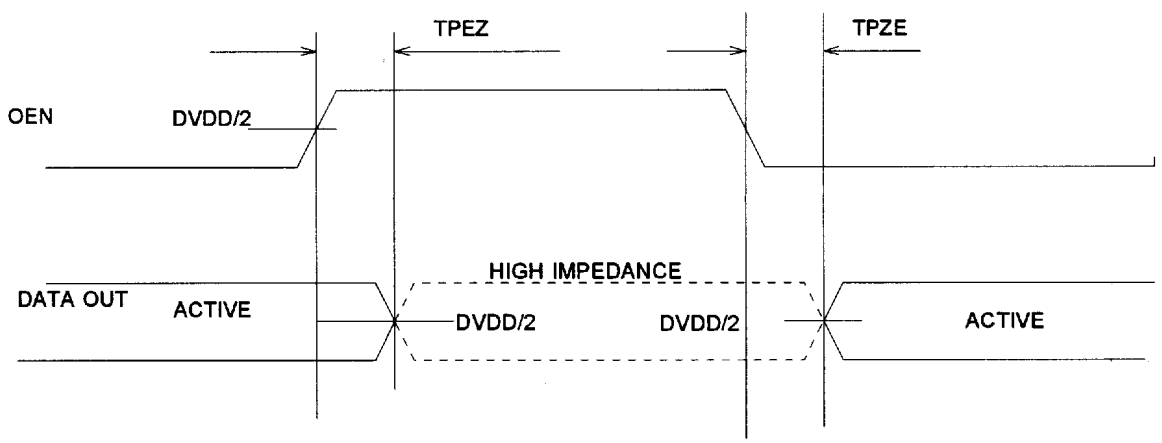
3) Timing Specifications

(AVDD,DVDD=2.7V....3.6 V, AVSS,DVSS=0V, Ta=TAMIN ~TAMAX°C,CL<10pF)

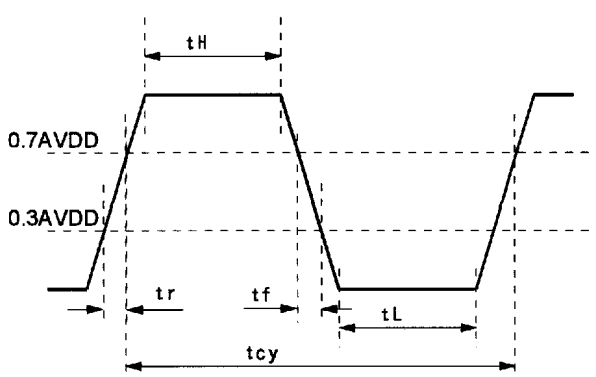
Parameters	Symbol	Conditions	min	typ	max	Units
Conversion Speed	Fc		0.5		20	MHz
Clock Cycle	tcy		50			ns
Clock Rise Time	tr	[30%->70%]VDD			2	ns
Clock Fall Time	tf	[70%->30%]VDD			2	ns
Clock Duty Cycle	DUTY		45	50	55	%
Clock Low Period	tL		23			ns
Clock High Period	tH		23			ns
Pipeline Delay	tpd			6		CLKIN
Sampling Delay	tap			3		ns
Three State Output Disable Delay	TPEZ	ACTIVE -> HI Z		20		ns ns
Three State Output Enable Delay	TPZE	HI Z -> ACTIVE		20		ns ns
Data Output Delay	tdl1 tdl2		2		 32	ns ns

Timing Diagram





Clock Timing Chart



4)Digital DC Specifications

(AVDD=DVDD=2.7..3.6V , AVSS=DVSS=0V, Ta=TAMIN~TAMAX°C
Specified as static characteristics)

Parameter	Symbol	Condition	min	typ	max	Units
High Input Voltage	VIH		0.7AVDD			V
Low Input Voltage	VIL				0.3AVDD	V
High Output Voltage	VOH	IOH=-1mA	0.7DVDD			V
Low Output Voltage	VOL	IOL=1mA			0.3DVDD	V
High Level Input Current (CKI,CEN)	ILIKG				±10	uA
HIGH-Z Output Current (D0:9)	IOZ	CEN= HIGH			±10	uA

Theory of operation

■ Analog Input Range

External Reference Voltage fed through VTP/VBT voltage(VTOP/VBOT) determine the analog input range of AK5420 10 Bit AD converter.

The Zero level of analog input(AIN) is VBT and the Full Scale is VTP.

■ Converted Digital Output Code

The converted Digital Output Code is Binary format.

For Zero Scale(AIN=VBT), the output code is all zero.

For Full Scale(AIN=VTP), the output code is all one.

The deviation from these ideal voltage is specified by Offset[EOB,EOT].

■ Chip Enable Function

By setting CEN=High, whole chip of AK5420 powers down.

Under the power down state, all digital output are High-Impedance and Vref related circuit also powers down.

The chip operates with input of CEN=LOW & supply of external VREF voltage.

Depending on the state of external capacitors, some period is required to charge them.

■ CKI,Pipeline delay,Data Output Timing

Feed A/D converter sampling clock to CKI pin.

Rising edges of CKI track and hold the analog input signal.

After 6clock pipeline delay, 10 bit digital output code is obtained.

■ Caution for Power Supply

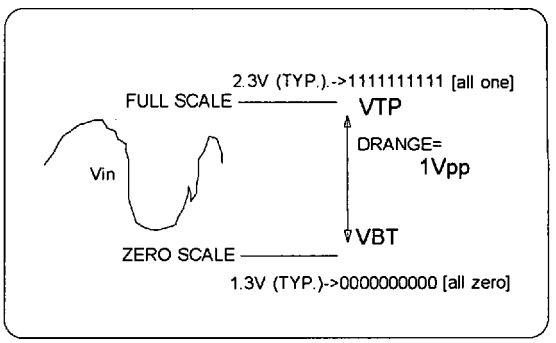
It is recommended to supply both AVDD and DVDD supply from single regulator.

(Please observe absolute maximum rating spec.:DVDD≤(AVDD+0.3V) even at the power-up and power-down sequence.)

Control Logic

Digital Output
The following chart described relation between analog input and the digital Output

AIN		Digital Output Code									
		MSB									LSB
VTP		1	1	1	1	1	1	1	1	1	1
:						:					
:		1	0	0	0	0	0	0	0	0	0
:		0	1	1	1	1	1	1	1	1	1
:						:					
VBT		0	0	0	0	0	0	0	0	0	0

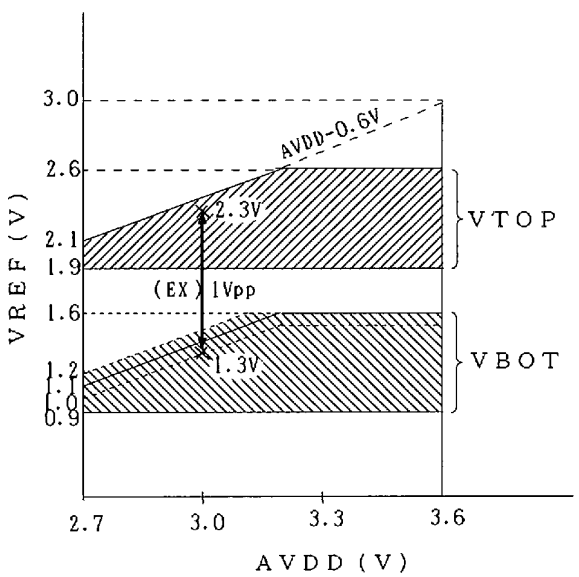


The output code by CE&CE is as follows

OEN	CEN	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
LO	LO	P	P	P	P	P	P	P	P	P	P
HI	LO	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
LO	HI	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
HI	HI	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTE: P:Normal Output code
Z:High Impedance

Full Scale

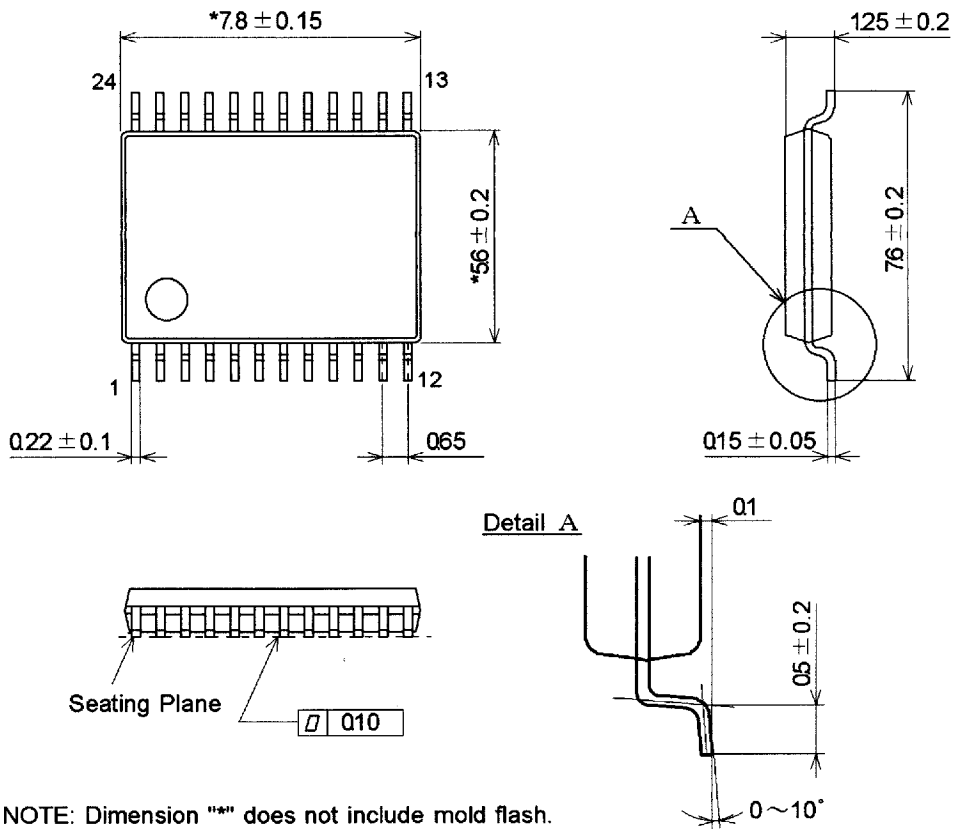


Frequency mode Select by SEL

SEL	MODE	Operation
VSS	20MHz MODE	20MHz Mode is Selected Fcmax is 20MHz
VDD	15MHz MODE	15MHz Mode is selected Fcmax is 15MHz Power consumption is lower than 20MHz mode

Outline Dimensions

● 24pin VSOP (Unit: mm)

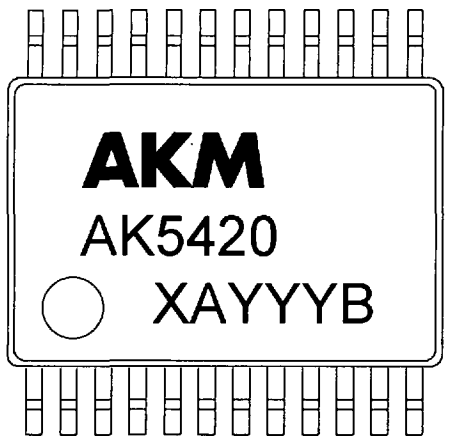


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

Marking



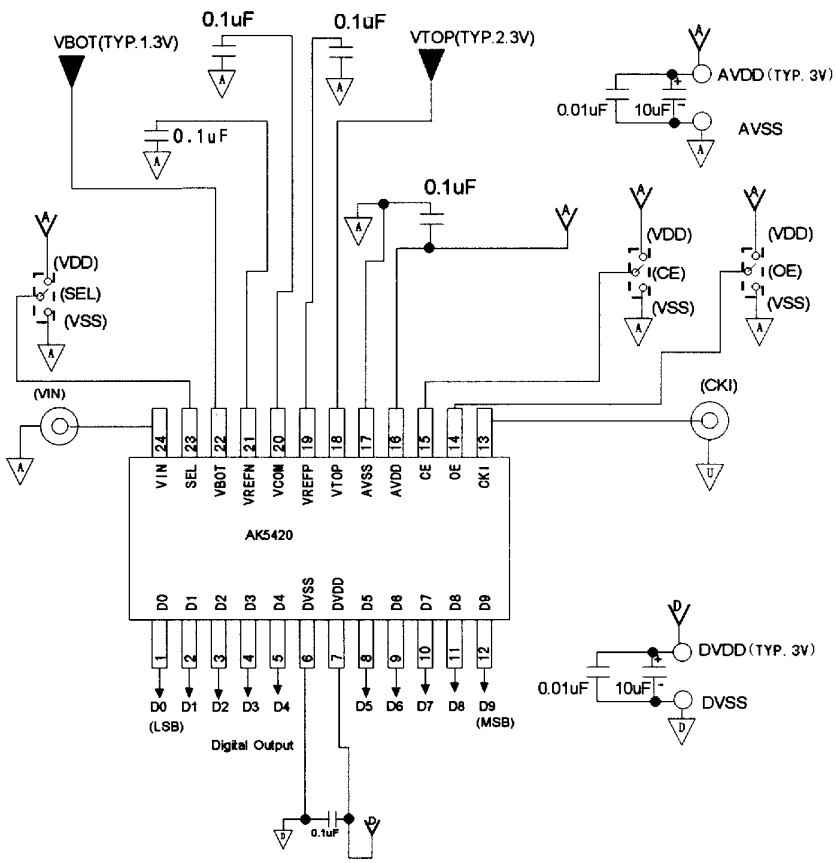
Contents of XAYYYB

XA : lot#(X:numbers,A:alphabet)

YYYB : Date Code(Y:numbers, B:alphabet)

Reference Circuit

The following schematic is the Reference circuit for system design.
Please optimize capacitance/resistance according to the system environment.



(note) Place the capacitors for VREF pins(VCOM,VREFN,VREFP) as close as possible to the device pins to obtain good performance.

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