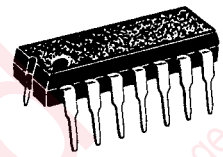
# MN4002B/MN4002BS

## Dual 4-Input NOR Gate

### ■ Outline

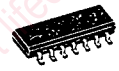
The MN4002B/S is 4-input positive logic NOR gate having two built-in circuits in one chip. The inverter buffer added to the gate output improves the input/output transfer chracteristic and minimizes the transfer time fluctuation caused by the load capacity increase. This NOR gate of low power consumption with high noise immunity is equivalent to Motorola's MC14002B and RCA's CD4002B.

P-1



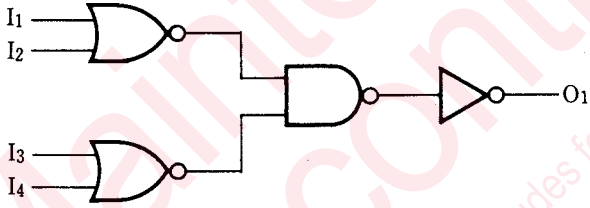
14-pin plastic DIL package

P-2

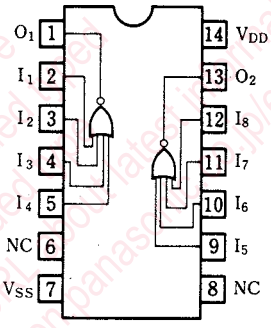


14-pin PANAFLAT package (SO-14D)

### ■ Logic diagram




Pin Configuration




### ■ Absolute Maximum Ratings (Ta=25°C)

| Item | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | | $V_{DD}$ | −0.5~+18 | V |
| Input voltage | | $V_I$ | −0.5~$V_{DD}$+0.5* | V |
| Output pin voltage | | $V_O$ | −0.5~$V_{DD}$+0.5* | V |
| Peak input · output pin current | | $\pm I_I$ | max. 10 | mA |
| Power dissipation (per package) | Ta=−40~+60°C | $P_D$ | max. 400 | mW |
| | Ta=+60~+80°C | | Decrease to 200mW at the rate of 8mW/°C | |
| Power dissipation (per output pin) | | $P_D$ | max. 100 | mW |
| Operating ambient temperature | | $T_{opr}$ | −40~+85 | °C |
| Storage temperature | | $T_{stg}$ | −65~+150 | °C |

* $V_{DD}$+0.5V should be lower than 18V.

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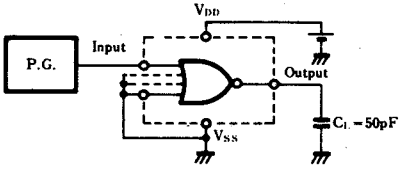
## ■ DC Characteristics ($V_{SS}$=0V)

| Item | $V_{DD}$ (V) | Symbol | Condition | | Ta=−40°C min. | Ta=−40°C max. | Ta=25°C min. | Ta=25°C max. | Ta=85°C min. | Ta=85°C max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Static supply current | 5 | $I_{DD}$ | $V_I=V_{SS}$ or $V_{DD}$ | | — | 1 | — | 1 | — | 7.5 | μA |
| | 10 | | | | — | 2 | — | 2 | — | 15 | |
| | 15 | | | | — | 4 | — | 4 | — | 30 | |
| Output voltage low level | 5 | $V_{OL}$ | $V_I=V_{SS}$ or $V_{DD}$ $\lvert I_O\rvert<1\mu A$ | | — | 0.05 | — | 0.05 | — | 0.05 | V |
| | 10 | | | | — | 0.05 | — | 0.05 | — | 0.05 | |
| | 15 | | | | — | 0.05 | — | 0.05 | — | 0.05 | |
| Output voltage high level | 5 | $V_{OH}$ | $V_I=V_{SS}$ or $V_{DD}$ $\lvert I_O\rvert<1\mu A$ | | 4.95 | — | 4.95 | — | 4.95 | — | V |
| | 10 | | | | 9.95 | — | 9.95 | — | 9.95 | — | |
| | 15 | | | | 14.95 | — | 14.95 | — | 14.95 | — | |
| Input voltage low level | 5 | $V_{IL}$ | $\lvert I_O\rvert<1\mu A$ | $V_O$=0.5V or 4.5V | — | 1.5 | — | 1.5 | — | 1.5 | V |
| | 10 | | | $V_O$=1V or 9V | — | 3 | — | 3 | — | 3 | |
| | 15 | | | $V_O$=1.5V or 13.5V | — | 4 | — | 4 | — | 4 | |
| Input voltage high level | 5 | $V_{IH}$ | $\lvert I_O\rvert<1\mu A$ | $V_O$=0.5V or 4.5V | 3.5 | — | 3.5 | — | 3.5 | — | V |
| | 10 | | | $V_O$=1V or 9V | 7 | — | 7 | — | 7 | — | |
| | 15 | | | $V_O$=1.5V or 13.5V | 11 | — | 11 | — | 11 | — | |
| Output current low level | 5 | $I_{OL}$ | $V_O$=0.4V, $V_I$=0 or 5V | | 0.52 | — | 0.44 | — | 0.36 | — | mA |
| | 10 | | $V_O$=0.5V, $V_I$=0 or 10V | | 1.3 | — | 1.1 | — | 0.9 | — | |
| | 15 | | $V_O$=1.5V, $V_I$=0 or 15V | | 3.6 | — | 3 | — | 2.4 | — | |
| Output current high level | 5 | $-I_{OH}$ | $V_O$=4.6V, $V_I$=0 or 5V | | 0.52 | — | 0.44 | — | 0.36 | — | mA |
| | 10 | | $V_O$=9.5V, $V_I$=0 or 10V | | 1.3 | — | 1.1 | — | 0.9 | — | |
| | 15 | | $V_O$=13.5V, $V_I$=0 or 15V | | 3.6 | — | 3 | — | 2.4 | — | |
| Output current high level | 5 | $-I_{OH}$ | $V_O$=2.5V, $V_I$=0 or 5V | | 1.7 | — | 1.4 | — | 1.1 | — | mA |
| Input leakage current | 15 | $\pm I_I$ | $V_I$=0 or 15V | | — | 0.3 | — | 0.3 | — | 1 | μA |

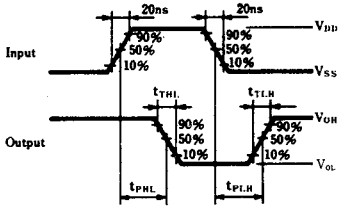
## ■ Switching Characteristics (Ta=25°C, $V_{SS}$=0V, $C_L$=50pF)

| Item | $V_{DD}$(V) | Symbol | min. | typ. | max. | Unit |
|---|---|---|---|---|---|---|
| Output rise time | 5 | $t_{TLH}$ | — | 60 | 180 | ns |
| | 10 | | — | 30 | 90 | |
| | 15 | | — | 20 | 60 | |
| Output fall time | 5 | $t_{THL}$ | — | 60 | 180 | ns |
| | 10 | | — | 30 | 90 | |
| | 15 | | — | 20 | 60 | |
| Propagation time | 5 | $t_{PLH}$ | — | 60 | 180 | ns |
| | 10 | | — | 25 | 75 | |
| | 15 | | — | 20 | 60 | |
| Propagation time | 5 | $t_{PHL}$ | — | 60 | 180 | ns |
| | 10 | | — | 25 | 75 | |
| | 15 | | — | 20 | 60 | |
| Input capacitance | | $C_I$ | — | — | 7.5 | pF |

1. Switching Time Measuring Circuit




2. Switching Waveforms

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