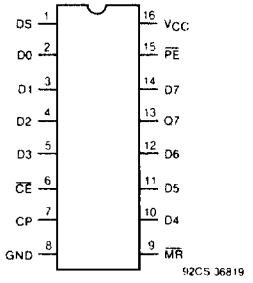
CD54/74HC166
CD54/74HCT166

File Number **1501**

High-Speed CMOS Logic



TERMINAL ASSIGNMENT

8-Bit Parallel-In/Serial-Out Shift Register

Type Features:

- *Buffered inputs*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC166 and CD54/74HCT166 8-bit shift register is fabricated with silicon gate CMOS technology. It possesses the low power consumption of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device.

The CD54/74HCT166 is functionally as well as pin compatible with the standard 54LS/74LS166.

The 166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into internal bit position Q_0 from Serial Data Input (DS), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q_7 output is connected to the DS input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation.

A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

The CD54HC166 and CD54HCT166 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC166 and CD74HCT166 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

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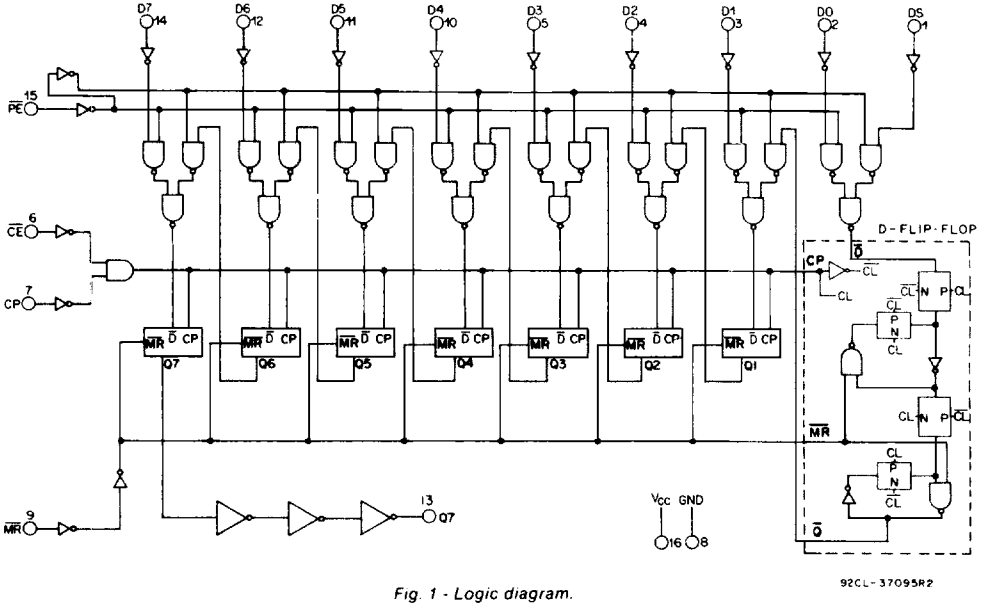

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Fig. 1 - Logic diagram.

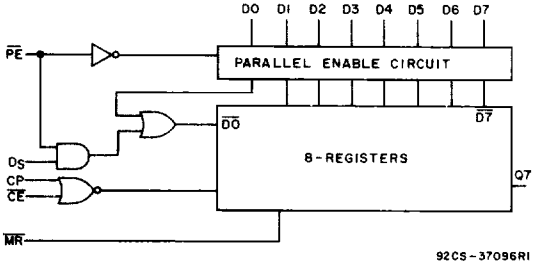

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Fig. 2 - Functional diagram.

TRUTH TABLE

Inputs						Internal Q States		Output
Master Reset	Parallel Enable	Clock Enable	Clock	Serial	Parallel D0 D7	Q0	Q1	Q7
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{00}	Q_{10}	Q_0
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{0n}	Q_{6n}
H	H	L	↑	L	X	L	Q_{0n}	Q_{6n}
H	X	H	↑	X	X	Q_{00}	Q_{10}	Q_{70}

H = high level (steady state).
L = low level (steady state).
X = irrelevant (any input, including transitions).
↑ = transition from low to high level.
a . . . h = the level of steady-state input at inputs D0 thru D7, respectively.
Q_{00}, Q_{10}, Q_{70} = the level of Q_0, Q_1, or Q_7, respectively, before the indicated steady-state input conditions were established.
Q_{0n}, Q_{6n} = the level of Q_0 or Q_6, respectively, before the most recent ↑ transition of the clock.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC166/CD54HC166										CD74HCT166/CD54HCT166									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
DS, D0-D7	0.2
$\overline{PE}$	0.35
CP, $\overline{CE}$	0.5
$\overline{MR}$	0.2

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\ V < V_o < V_{CC} + 0.5V$) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125° C
PACKAGE TYPE E, M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	Typical HC	Typical HCT	Units
Propagation Delay-Clock to Q	t_{PLH} t_{PHL}	15	13	17	ns
Maximum Clock Frequency	f_{MAX}	15	50	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	41	41	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i=input frequency
f_o=output frequency
C_L=output load capacitance
V_{CC}=supply voltage

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PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION Vcc V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Clock Frequency	f_{max}	2	6		—		5		—		4		—		
Fig. 3		4.5	30		25		25		20		20		16		MHz
		6	35		—		29		—		23		—		
$\overline{MR}$ Pulse Width	t_w	2	100		—		125		—		150		—		
Fig. 4		4.5	20		35		25		44		30		53		ns
		6	17		—		21		—		26		—		
Clock Pulse Width	t_w	2	80		—		100		—		120		—		
Fig. 3		4.5	16		20		20		25		24		30		ns
		6	14		—		17		—		20		—		
Set-up Time	t_{SU}	2	80		—		100		—		120		—		
Data and $\overline{CE}$ to		4.5	16		16		20		20		24		24		ns
Clock, Fig. 5, 6		6	14		—		17		—		20		—		
Hold Time	t_H	2	1		—		1		—		1		—		
Data to Clock,		4.5	1		0		1		0		1		0		ns
Fig. 5		6	1		—		1		—		1		—		
Removal Time	t_{REM}	2	0		—		0		—		0		—		
$\overline{MR}$ to Clock		4.5	0		0		0		0		0		0		ns
Fig. 4		6	0		—		0		—		0		—		
Set-up Time	t_{SU}	2	145		—		180		—		220		—		
$\overline{PE}$ to CP		4.5	29		30		36		38		44		45		ns
Fig. 6		6	25		—		31		—		38		—		
Hold Time	t_H	2	0		—		0		—		0		—		
$\overline{PE}$ to CP or $\overline{CE}$		4.5	0		0		0		0		0		0		ns
Fig. 6		6	0		—		0		—		0		—		

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION Vcc V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay	t_{PLH}	2		160		—		200		—		240		—	
Clock to Output	t_{PHL}	4.5		32		40		40		50		48		60	ns
Fig. 3		6		27		—		34		—		41		—	
Output Transition	t_{TLH}	2		75		—		95		—		110		—	
Time	t_{THL}	4.5		15		15		19		19		22		22	ns
Fig. 3		6		13		—		16		—		19		—	
Propagation Delay	t_{PHL}	2		160		—		200		—		240		—	
$\overline{MR}$ to Output		4.5		32		40		40		50		48		60	ns
Fig. 4		6		27		—		34		—		41		—	
Input Capacitance	C_I			10		10		10		10		10		10	pF

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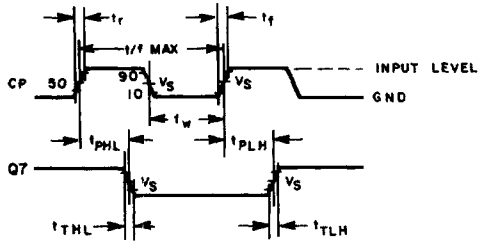
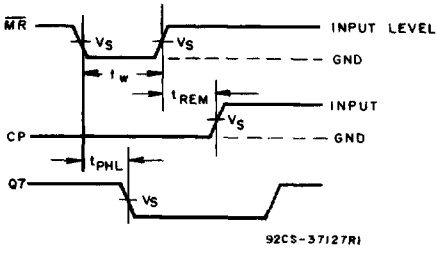


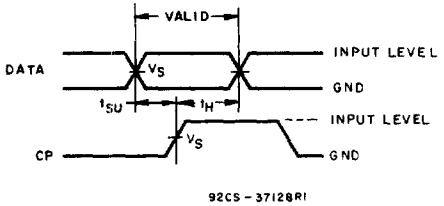
	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3.0 V
V_S	50% V_{CC}	1.3 V

Fig. 3 - Clock pre-requisite times and propagation and output transition times.



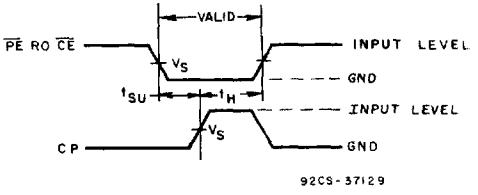
	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3.0 V
V_S	50% V_{CC}	1.3 V

Fig. 4 - Master reset pre-requisite times and propagation delays.



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3.0 V
V_S	50% V_{CC}	1.3 V

Fig. 5 - Data pre-requisite times.



	54/74 HC	54/74 HCT
INPUT LEVEL	V_{CC}	3.0 V
V_S	50% V_{CC}	1.3 V

Fig. 6 - Parallel enable or clock enable pre-requisite times.