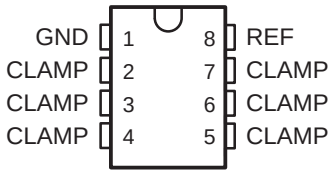
- **Protects Against Latch-Up**
- **25-mA Current Sink in Active State**
- **Less Than 1-mW Dissipation in Standby Condition**
- **Ideal for Applications in Environments Where Large Transient Spikes Occur**
- **Stable Operation for All Values of Capacitive Load**
- **No Output Overshoot**

D OR P PACKAGE
(TOP VIEW)



description

The TL7726 consists of six identical clamping circuits that monitor an input voltage with respect to a reference value, REF. For an input voltage (V_I) in the range of GND to < REF, the clamping circuits present a very high impedance to ground, drawing current of less than 10 μA. The clamping circuits are active for V_I < GND or V_I > REF when they have a very low impedance and can sink up to 25 mA.

These characteristics make the TL7726 ideal as protection devices for CMOS semiconductor devices in environments where there are large positive or negative transients to protect analog-to-digital converters in automotive or industrial systems. The use of clamping circuits provides a safeguard against potential latch-up.

The TL7726C is characterized for operation over the temperature range of 0°C to 70°C. The TL7726I is characterized for operation over the temperature range of –40°C to 85°C. The TL7726Q is characterized for operation over the temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_A	SOIC (D)	PLASTIC DIP (P)
0°C to 70°C	TL7726CD	TL7726CP
–40°C to 85°C	TL7726ID	TL7726IP
–40°C to 125°C	TL7726QD	TL7726QP

The D package is available taped and reeled. Add the suffix R to the device type (i.e., TL7726CDR).

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Reference voltage, V_{ref} . . . . . 6 V
Clamping current, I_{IK} . . . . . ±50 mA
Junction temperature, T_J . . . . . 150°C
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package . . . . . 97°C/W
P package . . . . . 127°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Reference voltage, V_{ref}		4.5	5.5	V
Input clamping current, I_{IK}	$V_I \geq V_{ref}$		25	mA
	$V_I \leq$ GND	–25		
Operating free-air temperature range, T_A	TL7726C	0	70	°C
	TL7726I	–40	85	
	TL7726Q	–40	125	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

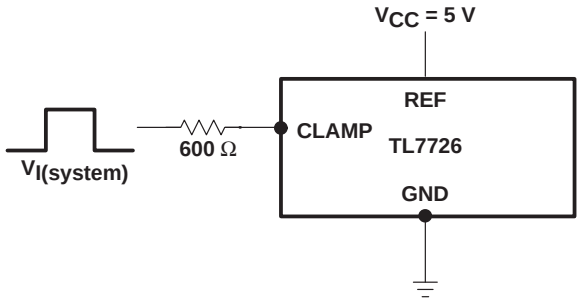
PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK+}	Positive clamp voltage	I_I = 20 mA	V_{ref}		V_{ref} + 200	mV
$V_{IK–}$	Negative clamp voltage	I_I = 20 mA	–200		0	mV
I_Z	Reference current	V_{ref} = 5 V		25	60	µA
I_I	Input current	V_{ref} – 50 mV ≤ V_I ≤ V_{ref}			10	µA
		GND ≤ V_I ≤ 50 mV	–10			
		50 mV ≤ V_I ≤ V_{ref} – 50 mV	–1		1	

‡ All typical values are at T_A = 25°C.

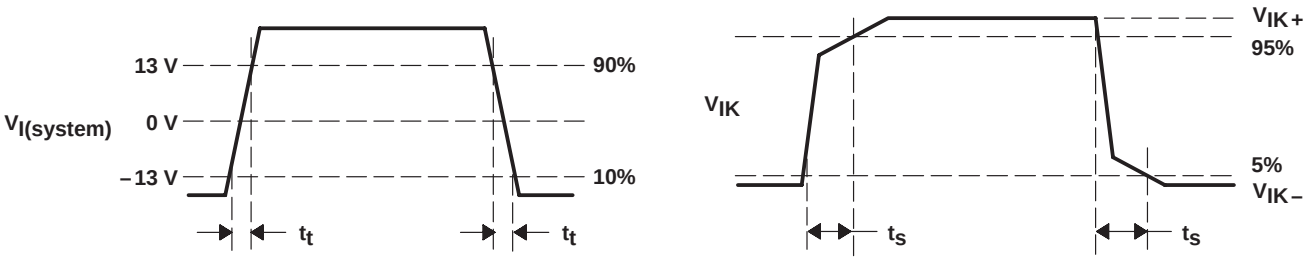
switching characteristics specified at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_s	Settling time	$V_{I(system)}$ = ±13 V, R_I = 600 Ω, t_t < 1 µs, Measured at 10% to 90%, See Figure 1		30	µs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



INPUT WAVEFORM

CLAMP WAVEFORM

Figure 1. Switching Characteristics

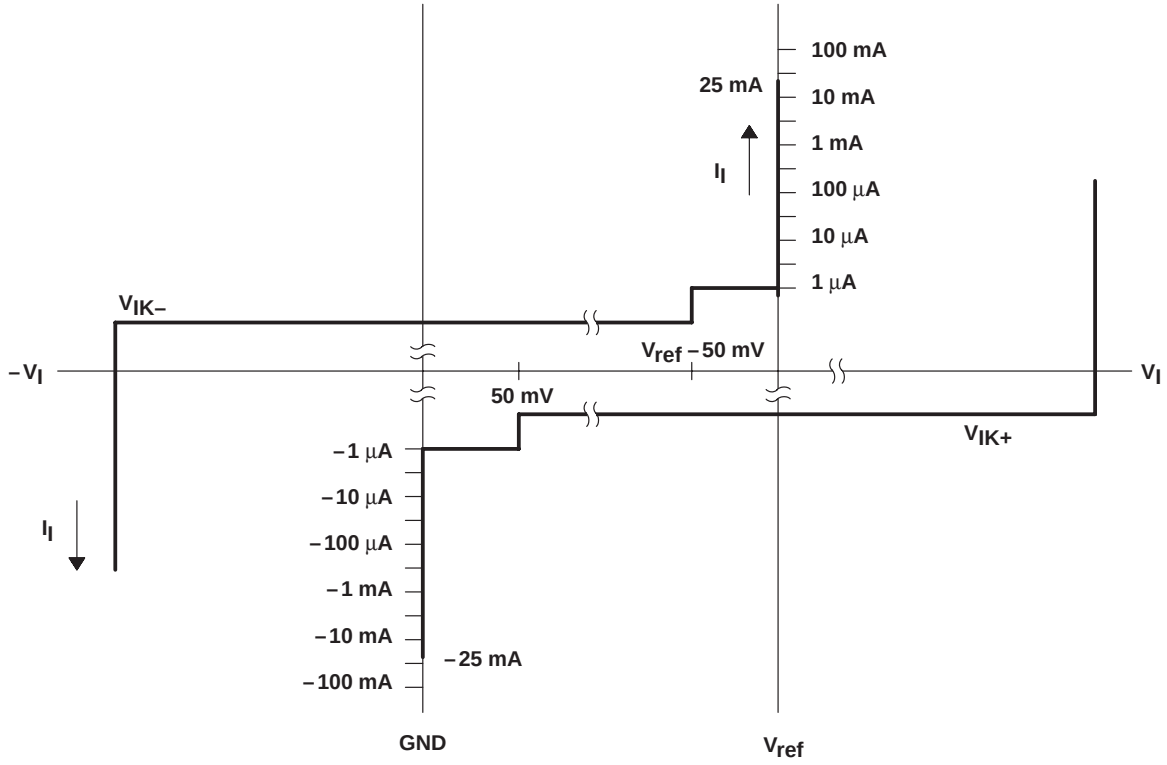
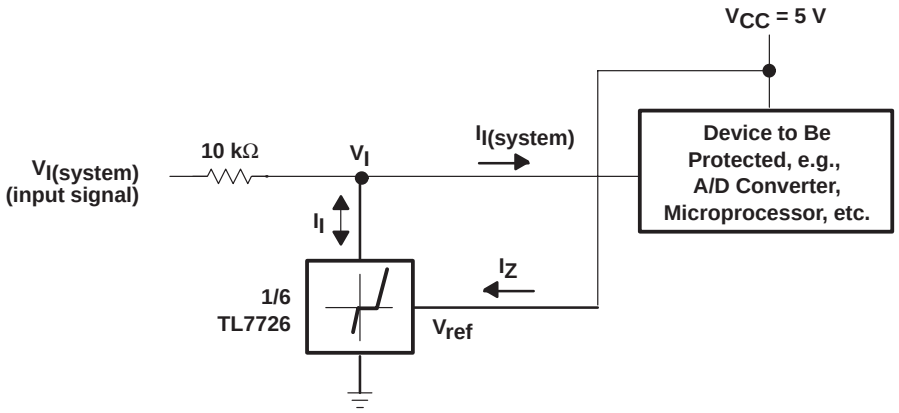


Figure 2. Tolerance Band for Clamping Circuit

APPLICATION INFORMATION



Example: If $I_I >> I_{I(system)}$, i.e., $V_{I(system)} > V_{ref}$ + 200 mV
where:

$I_{I(system)}$ = Input current to the device being protected
$V_{I(system)}$ = Input voltage to the device being protected

then the maximum input voltage

$V_{I(system)max} = V_{ref} + I_I max(10k\Omega)$
$= 5\ V + 25\ mA(10k\Omega)$
$= 5\ V + 250\ V$
$= 255\ V$

Figure 3. Typical Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7726CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7726C	Samples
TL7726CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7726C	Samples
TL7726CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL7726CP	Samples
TL7726ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7726I	Samples
TL7726IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7726I	Samples
TL7726IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL7726IP	Samples
TL7726IPE4	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL7726IP	
TL7726QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7726Q	Samples
TL7726QDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		7726Q	Samples
TL7726QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7726Q	Samples
TL7726QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		7726Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

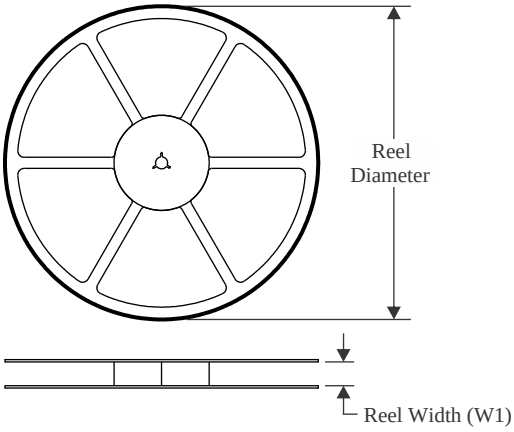
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

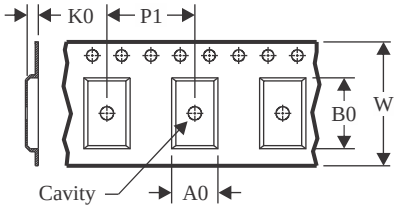
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

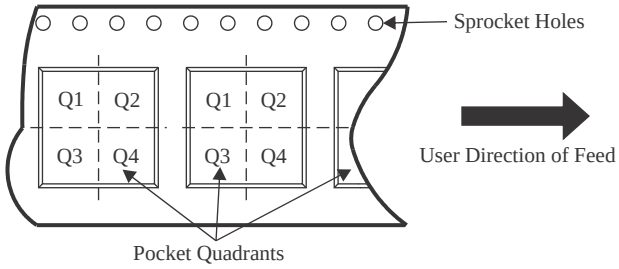


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

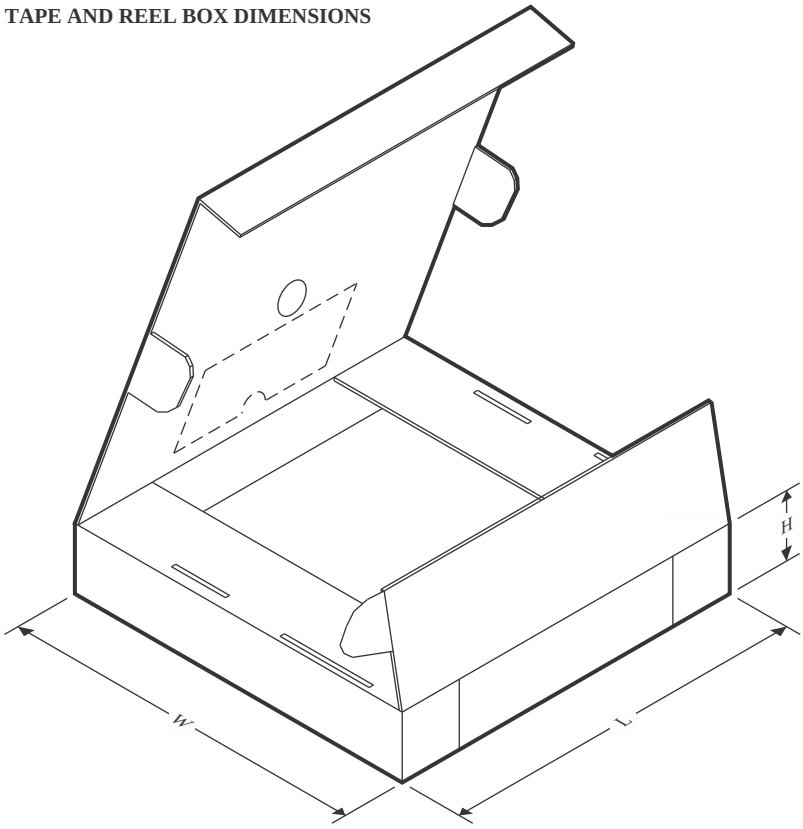
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7726CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7726IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7726QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7726QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

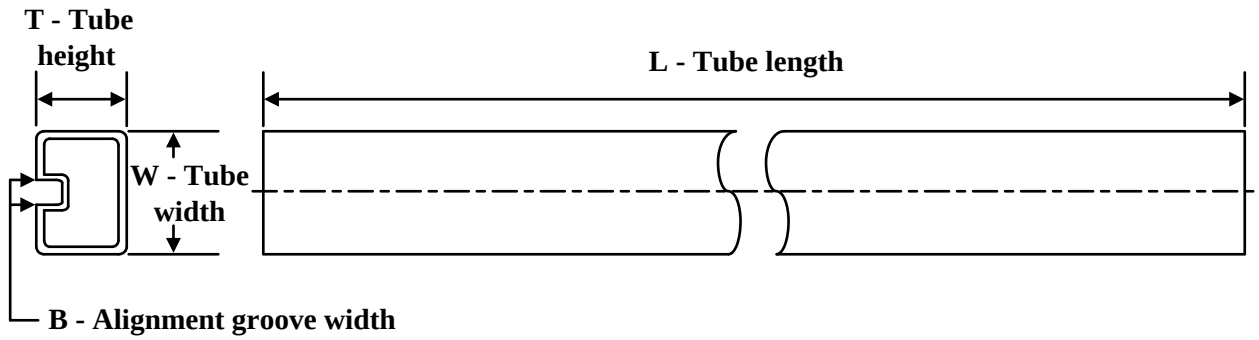
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

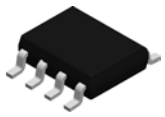
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7726CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7726IDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7726QDR	SOIC	D	8	2500	350.0	350.0	43.0
TL7726QDRG4	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL7726CD	D	SOIC	8	75	507	8	3940	4.32
TL7726CP	P	PDIP	8	50	506	13.97	11230	4.32
TL7726ID	D	SOIC	8	75	507	8	3940	4.32
TL7726IP	P	PDIP	8	50	506	13.97	11230	4.32
TL7726IPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL7726QD	D	SOIC	8	75	505.46	6.76	3810	4
TL7726QDG4	D	SOIC	8	75	505.46	6.76	3810	4

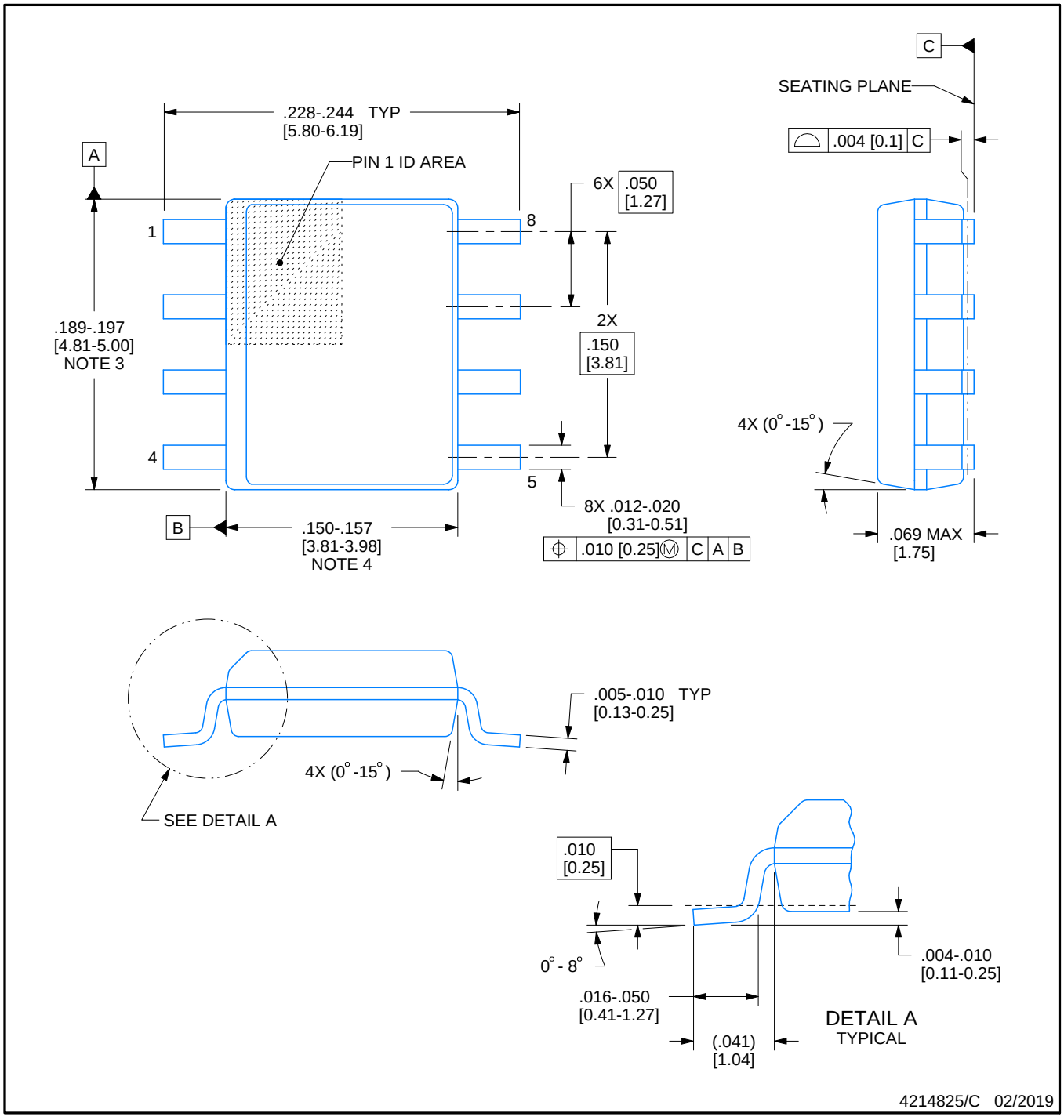


PACKAGE OUTLINE

D0008A

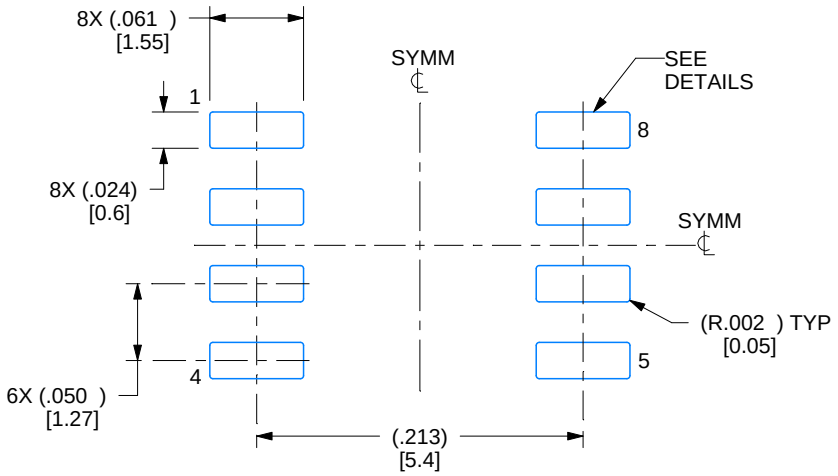
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

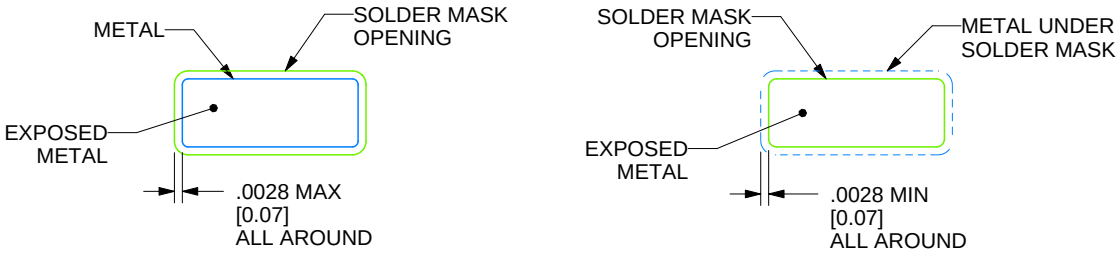


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

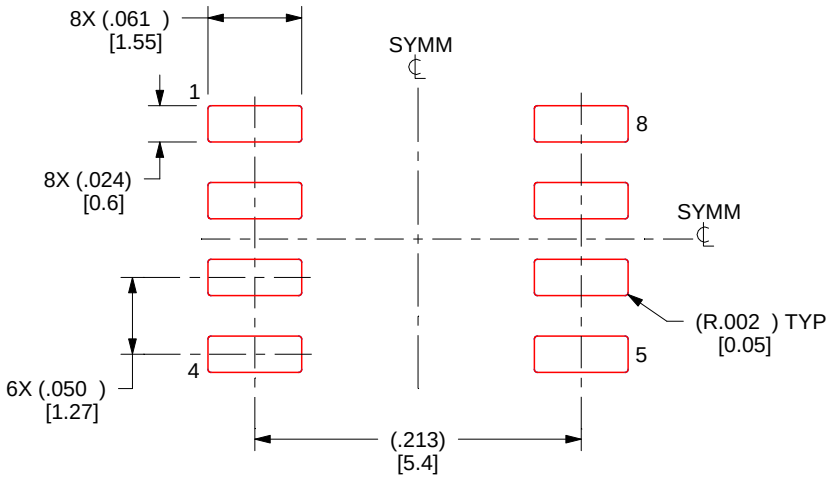
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



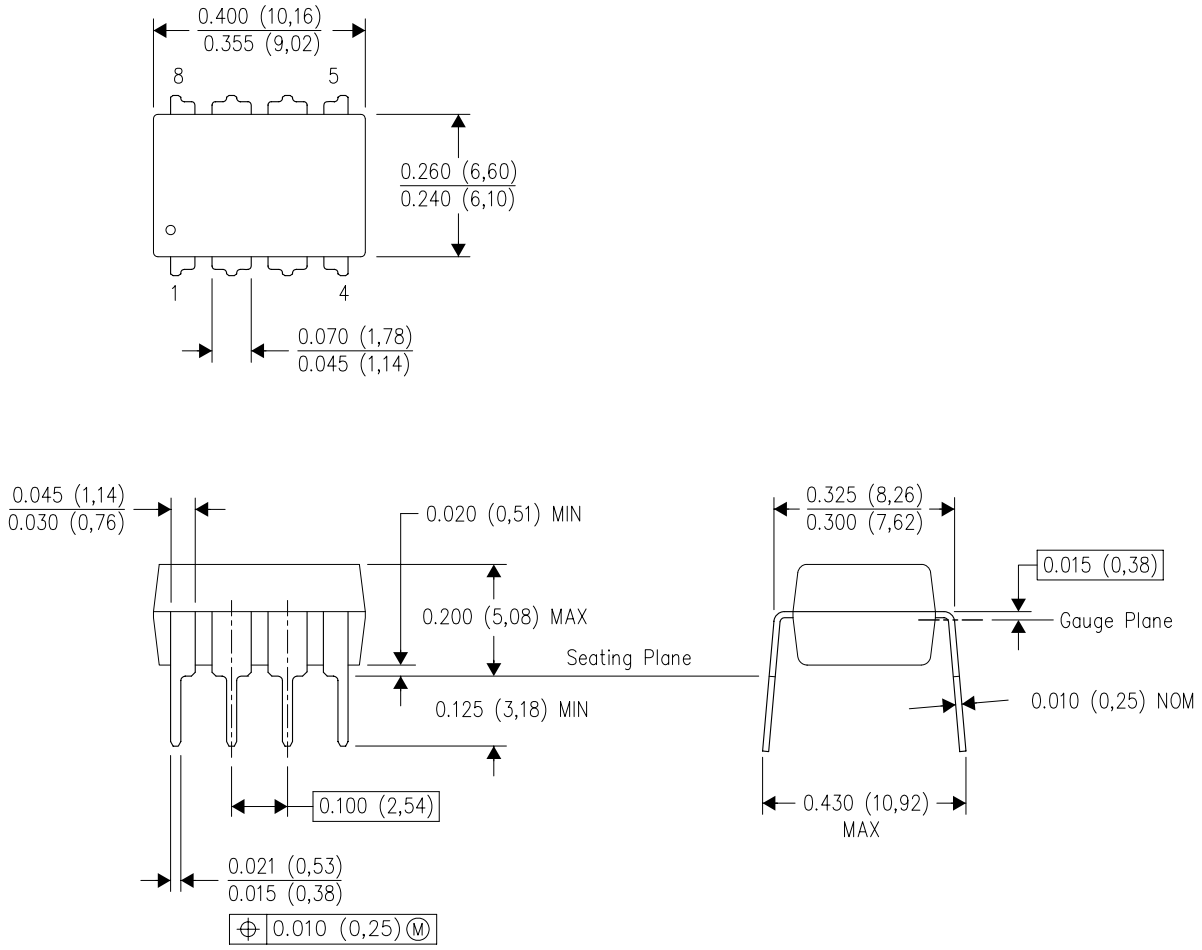
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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