

**SM536256**  
**1MByte (256K x 36) CMOS DRAM Module**

**General Description**

The SM536256 is a high performance, 1-megabyte dynamic RAM module organized as 256K words by 36 bits, in a 72-pin, leadless single-in-line memory module (SIMM) package.

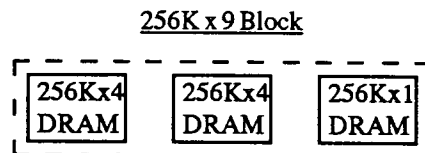
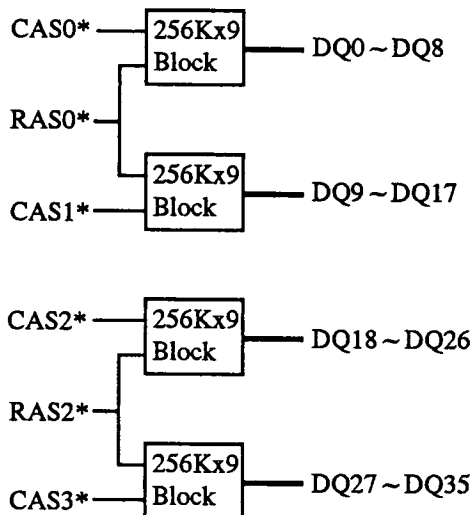
The module utilizes eight CMOS 256K x 4 and four 256K x 1 dynamic RAMs in surface mount package on an epoxy laminate substrate. The 256K x 1 DRAMs are for parity. Each device is accompanied by a 0.22μf decoupling capacitor for improved noise immunity.

Control lines are provided such that byte control is possible.

**Features**

- High Density : 1Mbyte
- Fast Access Time of 70/80/100ns (max.)
- Low Power :  
4.95/4.12/3.41W (max.) - Active (70/80/100ns)  
0.132W (max.) - Standby (TTL)  
0.066W(max.) - Standby (CMOS)
- TTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 5V ± 10%
- PCB footprint of less than 0.86 sq. in. (Height:1")

**Functional Diagram**



A0 ~ A8 : To all devices  
WE\* : To all devices  
OE\* of all 256Kx4 devices  
are grounded



0.22μf to all devices

Note: All specifications of this device are subject to change without notice  
"\*" signifies complement

### Pin Name

A0 ~ A8	Address
DQ0 ~ DQ35	Data Input/Output
CAS0* ~ CAS3*	Column Address Strobe
RAS0*, RAS2*	Row Address Strobe
WE*	Read/Write
PD1 ~ PD4	Presence Detect
VCC	Power Supply
VSS	Ground
NC	No Connection

### Presence Detect Pins

Pin	70ns	80ns	100ns
PD1	VSS	VSS	VSS
PD2	NC	NC	NC
PD3	VSS	NC	VSS
PD4	NC	VSS	VSS

### Ordering Information

Part Number	Speed
SM536256-7	70ns
SM536256-8	80ns
SM536256-10	100ns

Pin No.	Pin Designation	Pin No.	Pin Designation
1	VSS	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	VSS
4	DQ1	40	CAS0*
5	DQ19	41	CAS2*
6	DQ2	42	CAS3*
7	DQ20	43	CAS1*
8	DQ3	44	RAS0*
9	DQ21	45	NC
10	VCC	46	NC
11	NC	47	WE*
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	NC	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	VCC
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	VCC	66	NC
31	A8	67	PD1
32	NC	68	PD2
33	NC	69	PD3
34	RAS2*	70	PD4
35	DQ26	71	NC
36	DQ8	72	VSS

**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Voltage on any pin relative to VSS	VT	- 1 to +7.0	V
Power Dissipation	PT	12	W
Operating Temperature	TA	0 to +70	°C
Storage Temperature	Tstg	- 55 to +125	°C
Short Circuit Output Current	IOS	50	mA

**Recommended DC Operating Conditions**  
( Ta = 0 to +70 °C )

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	2.4	-	6.0	V
VIL	Input Low Voltage	-1	-	0.8	V

**DC Characteristics**

(VCC = 5V ± 10%, VSS = 0V, Ta = 0 to +70 °C)

Parameter	Symbol	Test Conditions	SM536256-7		SM536256-8		SM536256-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	ICC1	<u>tRC = min.</u> TTL Interface RAS*, CAS* = VIH , DOUT = High Z	-	900	-	748	-	620	mA	1, 2
Standby Current	ICC2	<u>DOUT = High Z</u> CMOS Interface RAS*, CAS* ≥ VCC - 0.2V DOUT = High Z	-	24	-	24	-	24	mA	
RAS*-Only Refresh Current	ICC3	<u>tRC = min.</u>	-	900	-	748	-	620	mA	2
Standby Current	ICC5	<u>RAS* = VH ,</u> CAS* = VIL , DOUT = Enable	-	60	-	60	-	60	mA	1
CAS*-Before-RAS* Refresh Current	ICC6	<u>tRC = Min.</u>	-	820	-	748	-	620	mA	1
Fast Page Mode Current	ICC7	<u>tPC = Min.</u>	-	720	-	580	-	560	mA	1,3

DC Characteristics (contd.)

Parameter	Symbol	Test Conditions	SM536256-7		SM536256-8		SM536256-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Input Leakage Current	ILI	0V ≤ VIN ≤ 7V	-120	120	-120	120	-120	120	μA
Output Leakage Current	ILO	0V ≤ VOUT ≤ 7V	-10	10	-10	10	-10	10	μA
Output High Voltage	VOH	High IOUT = -5mA	2.4	VCC	2.4	VCC	2.4	VCC	V
Output Low Voltage	VOL	Low IOUT = 4.2mA	0	0.4	0	0.4	0	0.4	V

- Notes: 1. ICC depends on output load condition when the device is selected, ICC max. is specified at the output open condition.  
 2. Address can be changed less than three times while RAS\* = VIL .  
 3. Address can be changed once or less while CAS\* = VIH .

Capacitance

(Ta = +25°C, VCC = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	CI1	-	67	pF	1
Input Capacitance (WE*)	CI2	-	87	pF	1
Input Capacitance (RAS0*, RAS2*)	CI3	-	45	pF	1
Input Capacitance (CAS0* ~ CAS3*)	CI4	-	24	pF	1
Output Capacitance (DQ8,17,26,35)	CI/O1	-	31	pF	1, 2
Output Capacitance (Remaining DQs)	CI/O2	-	83	pF	1, 2

- Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.  
 2. CAS\* = VIH to disable DOUT.

AC Characteristics

(Ta = 0 to +70 °C, VCC = 5.0V ± 10%, VSS = 0V)

Parameter	Symbol	SM536256-7		SM536256-8		SM536256-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	130	-	160	-	190	-	ns	
Access time from RAS*	tRAC	-	70	-	80	-	100	ns	3, 4
Access time from CAS*	tCAC	-	20	-	25	-	25	ns	3, 4, 5
Access time from column address	tAA	-	35	-	40	-	45	ns	3, 10
Output buffer turn-off time	tOFF	0	20	0	20	0	25	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
RAS* precharge time	tRP	50	-	70	-	80	-	ns	
RAS* pulse width	tRAS	70	10000	80	10000	100	10000	ns	

AC Characteristics (contd.)

Parameter	Symbol	SM536256-7		SM536256-8		SM536256-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
RAS* hold time	<i>tRSH</i>	20	-	25	-	25	-	ns	
CAS* hold time	<i>tCSH</i>	70	-	80	-	100	-	ns	
CAS* pulse width	<i>tCAS</i>	20	10000	25	10000	25	10000	ns	
RAS* to CAS* delay time	<i>tRCD</i>	20	50	25	60	25	75	ns	4
RAS* to column address delay time	<i>tRAD</i>	15	35	20	40	20	55	ns	10
CAS* to RAS* precharge time	<i>tCRP</i>	10	-	10	-	10	-	ns	
Row address set-up time	<i>tASR</i>	0	-	0	-	0	-	ns	
Row address hold time	<i>tRAH</i>	10	-	15	-	15	-	ns	
Column address set-up time	<i>tASC</i>	0	-	0	-	0	-	ns	
Column address hold time	<i>tCAH</i>	15	-	20	-	20	-	ns	
Column address to RAS* lead time	<i>tRAL</i>	35	-	40	-	50	-	ns	
Read command set-up time	<i>tRCS</i>	0	-	0	-	0	-	ns	
Read command hold time to CAS*	<i>tRCH</i>	0	-	0	-	0	-	ns	8
Read command hold time to RAS*	<i>tRRH</i>	10	-	10	-	10	-	ns	
Write command hold time	<i>tWCH</i>	15	-	20	-	20	-	ns	
Write command pulse width	<i>tWP</i>	15	-	15	-	20	-	ns	
Write command to RAS* lead time	<i>tRWL</i>	20	-	25	-	25	-	ns	
Write command to CAS* lead time	<i>tCWL</i>	20	-	25	-	25	-	ns	
Data-in set-up time	<i>tDS</i>	0	-	0	-	0	-	ns	9
Data-in hold time	<i>tDH</i>	15	-	15	-	20	-	ns	9
Refresh period (512 cycles)	<i>tREF</i>	-	8	-	8	-	8	ns	
Write command set-up time	<i>tWCS</i>	0	-	0	-	0	-	ns	7
CAS* set-up time (CBR refresh)	<i>tCSR</i>	10	-	10	-	10	-	ns	
CAS* hold time (CBR refresh)	<i>tCHR</i>	20	-	25	-	30	-	ns	
RAS* precharge to CAS* hold time	<i>tRPC</i>	10	-	10	-	10	-	ns	
Access time from CAS* precharge	<i>tACP</i>	-	45	-	45	-	55	ns	3
Fast page mode cycle time	<i>tPC</i>	50	-	55	-	60	-	ns	
CAS* precharge time (Fast page)	<i>tCP</i>	10	-	10	-	10	-	ns	
RAS* pulse width (Fast page)	<i>tRASC</i>	-	100000	-	100000	-	100000	ns	

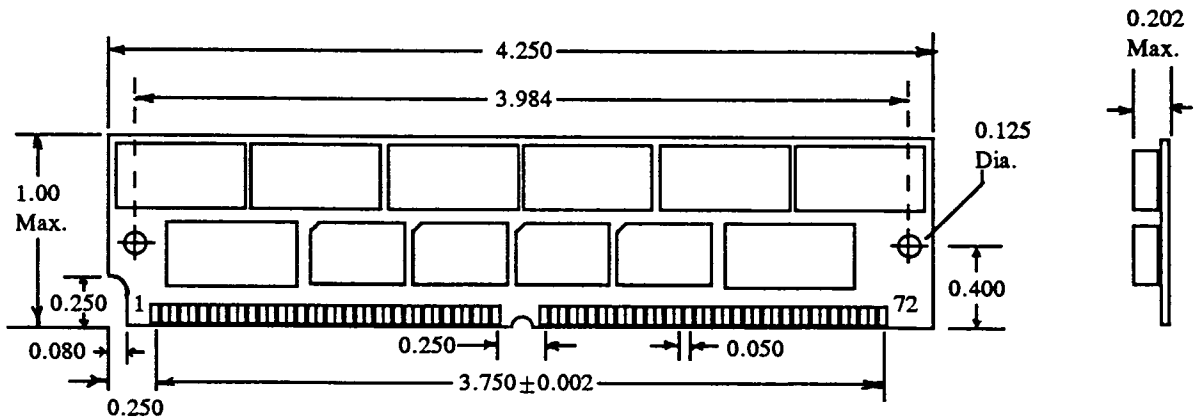
- Notes:
1. An initial pause of 200 $\mu$ s is required after power-up followed by any eight RAS\* cycles before device operation is achieved.
  2. *VIH* (min) and *VIL* (max) are reference levels for measuring timing of input signals. Transition times are measured between *VIH* (min) and *VIL* (max) and are assumed to be 5ns for all inputs.
  3. Measure with a load equivalent to 2 TTL loads and 100pF.
  4. Operation within the *tRCD* (max) limit ensures that *tRAC* (max) limit can be met. *tRCD* (max) is specified as a reference point only. If *tRCD* (max) is greater than the specified limit, then access time is controlled exclusively by *tCAC*.
  5. Assumes that  $tRCD \geq tRCD$  (max).

Notes (contd.):

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
7.  $t_{WCS}$  is non restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If  $t_{WCS} > t_{WCS}(\min)$  the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
9. These parameters are referenced to the CAS\* leading edge in early write cycles.
10. Operation within the  $t_{RAD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, then access time is controlled by  $t_{AA}$ .

Physical Dimensions

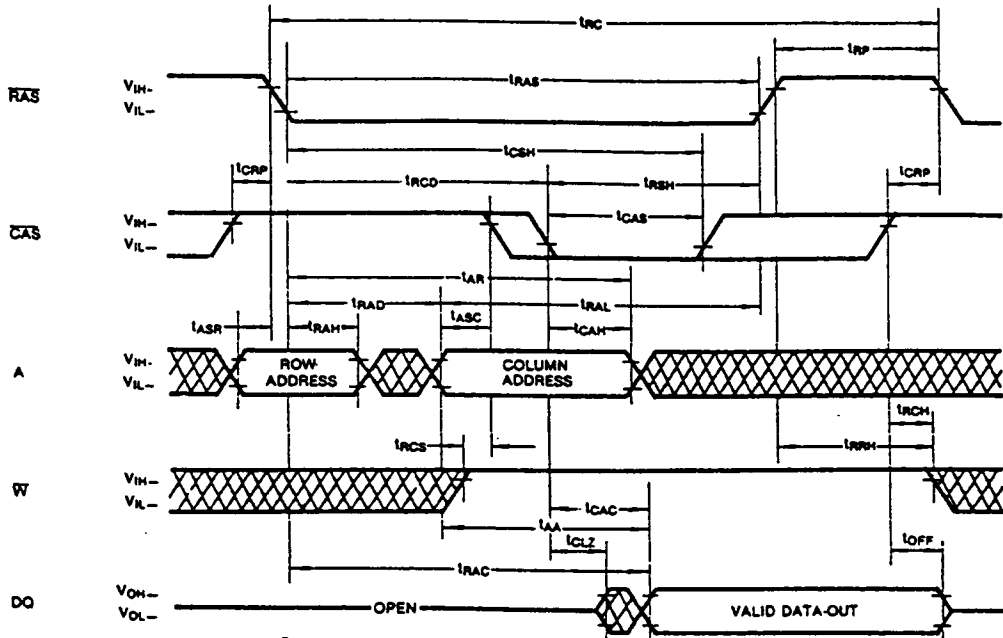
72-pin SIMM



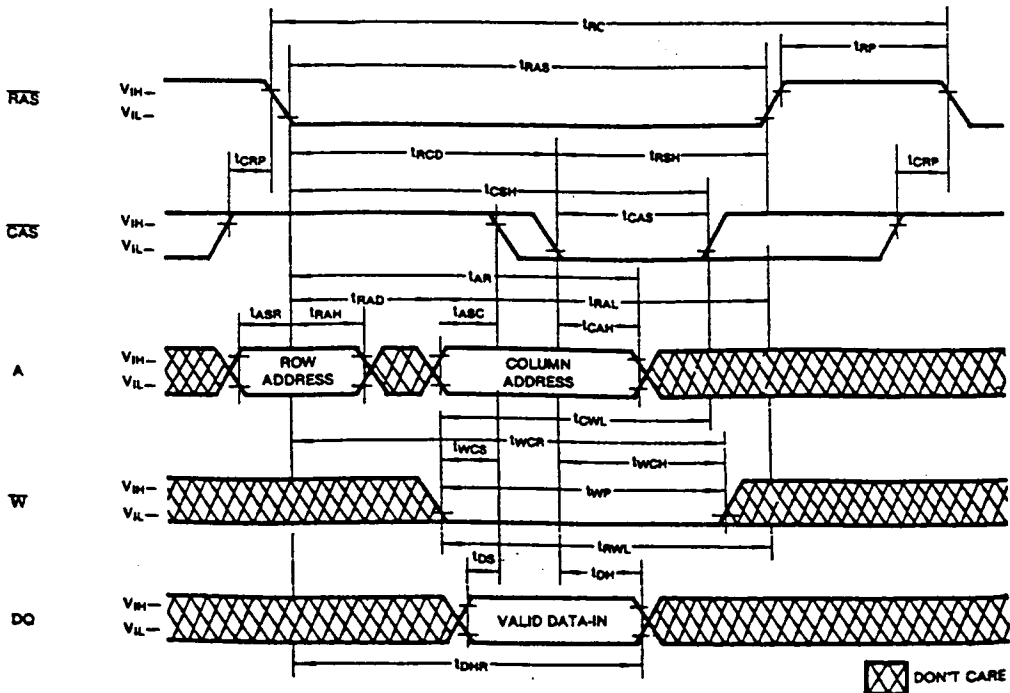
(All dimensions are in inches with a tolerance of  $\pm 0.005$ " unless otherwise specified)

**TIMING WAVEFORMS**

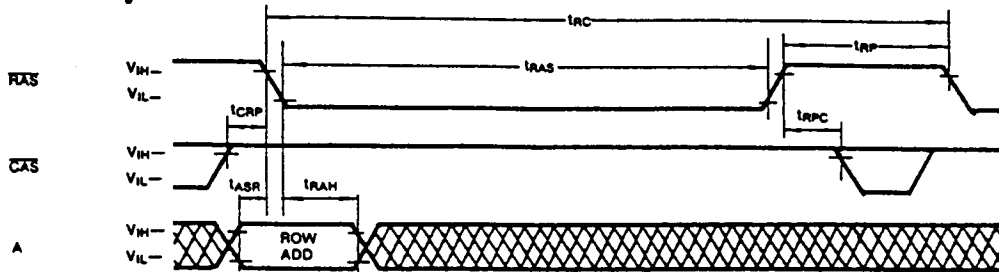
**Read Cycle**



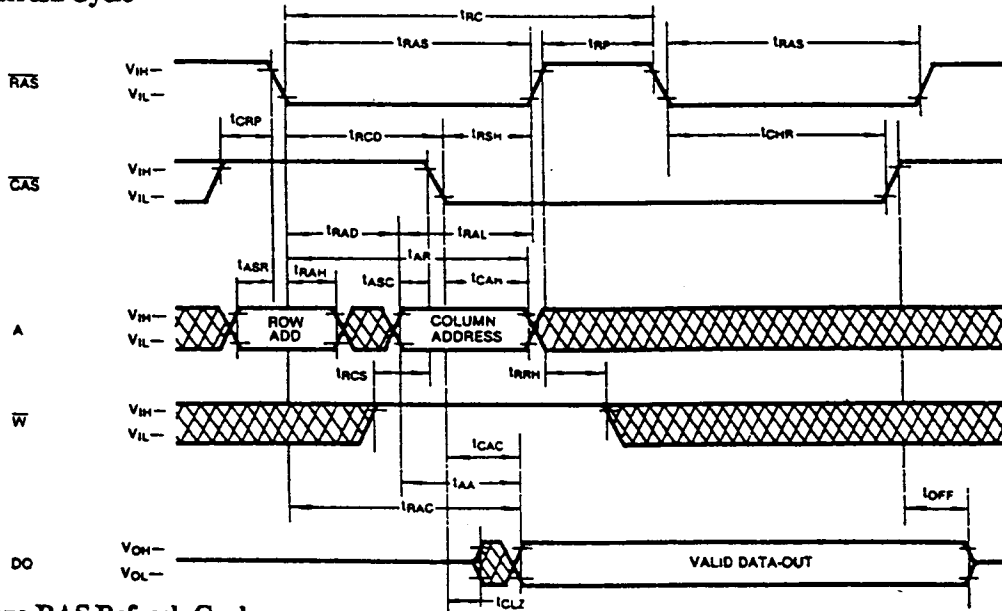
**Write Cycle (Early Write)**



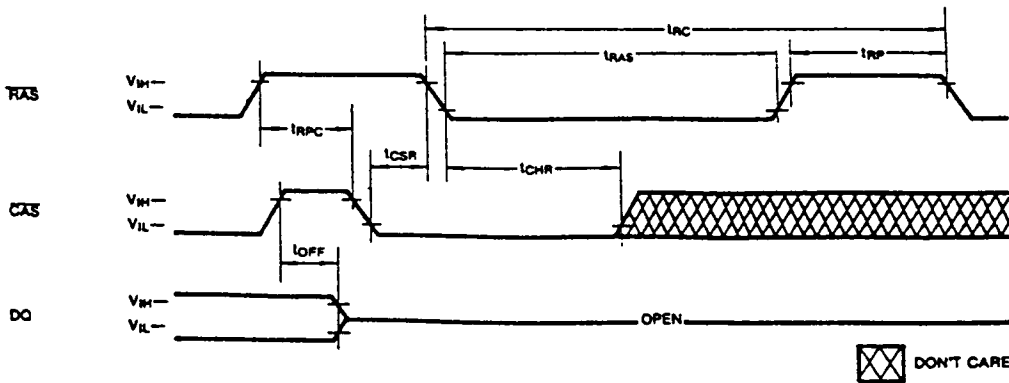
**RAS Only Refresh Cycle**



**Hidden Refresh Cycle**



**CAS-Before-RAS Refresh Cycle**



 DON'T CARE

