

DRAM

4M x 4 DRAM EDO PAGE MODE

FEATURES

- x4 organization
- EDO(Extended Data-Out) access mode
- Single power supply :
2.5V ± 10% Vcc for S-ver product
2.0V ± 10% Vcc for D-ver product
- LVTTTL Interface for inputs and outputs
- 2048-cycle refresh in 32ms
- Refresh modes : $\overline{\text{RAS}}$ only, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ (CBR) and HIDDEN capabilities
- Extended and Self-Refresh capabilities
- Key AC Parameter
-

	t _{RAC}	t _{CAC}	t _{RC}	t _{PC}
-50	50	13	84	20
-60	60	15	104	25
-80	80	20	134	35
-100	100	25	164	45

ORDERING INFORMATION - PACKAGE

JEDEC standard pinout :
24/26-pin 300mil SOJ
24/26-pin 300mil TSOP (Typell)

PRODUCT NO.	Vcc	PACKING TYPE
M11S1644SA-50J/60J/80J	2.5V	SOJ
M11D1644SA-60J/80J/100J	2.0V	
M11S1644SA-50T/60T/80T	2.5V	TSOP
M11D1644SA-60T/80T/100T	2.0V	

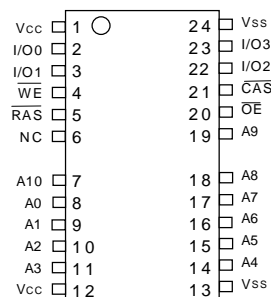
GENERAL DESCRIPTION

The M11S1644SA / M11D1644SA series is a randomly accessed solid state memory, organized as 4,194,304 x 4 bits device. It offers Extended Data-Out access mode. Single power supply (2.5V ± 10%, 2.0V ± 10%), access time (-50,-60,-80, -100) and package type (SOJ, TSOP) are optional features of this family. All these family have $\overline{\text{CAS}}$ - before - $\overline{\text{RAS}}$, $\overline{\text{RAS}}$ -only refresh, Hidden refresh, Extended and Self-Refresh capabilities.

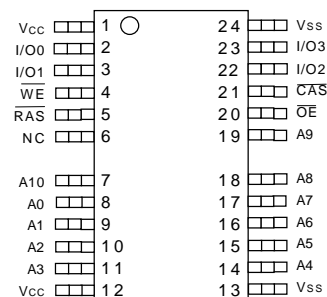
The primary advantage of EDO is the availability of data-out even after $\overline{\text{CAS}}$ returns high. EDO allows $\overline{\text{CAS}}$ precharge time (T_{pc}) to occur without the output data going invalid. This elimination of $\overline{\text{CAS}}$ output control allows pipeline Read.

PIN ASSIGNMENT

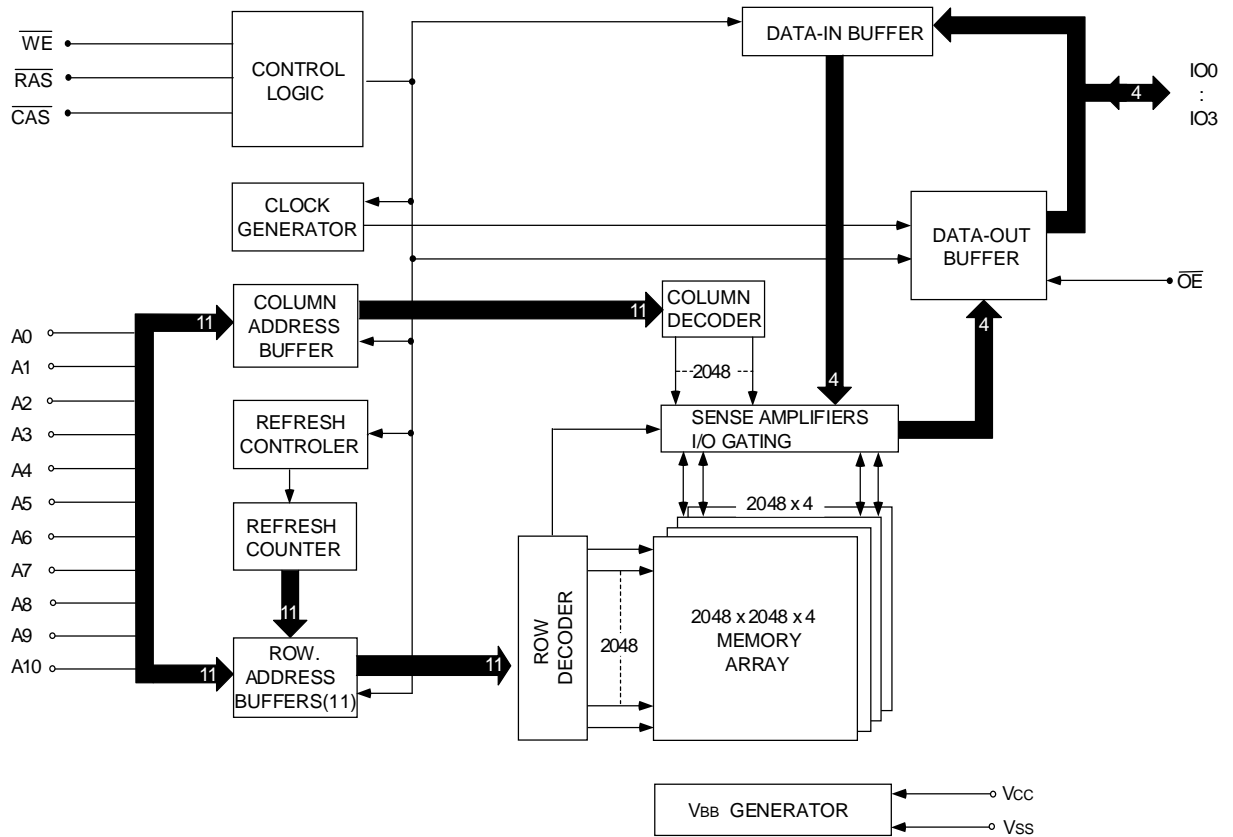
SOJ Top View



TSOP (Typell) Top View



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	PIN NAME	TYPE	DESCRIPTION
8~11,14~19,7	A0~A10	Input	Address Input Row Address : A0~A10 Column Address : A0~A10
5	\overline{RAS}	Input	Row Address Strobe
21	\overline{CAS}	Input	Column Address Strobe
4	\overline{WE}	Input	Write Enable
20	\overline{OE}	Input	Output Enable
2,3,22,23	I/O0 ~ I/O3	Input / Output	Data Input / Output
1,12	Vcc	Supply	Power, (2.5V or 2.0V)
13,24	Vss	Ground	Ground
6	NC	-	No Connect

ABSOLUTE MAXIMUM RATINGS

Voltage on Any pin Relative to Vss-0.5V to Vcc+0.5V
 Operating Temperature, T_A (ambient)0 °C to +70 °C
 Storage Temperature (plastic)-55 °C to +150 °C
 Power Dissipation1.0W
 Short Circuit Output Current50Ma

Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only, and functional operation of the device above those conditions indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED

OPERATING CONDITIONS (0 °C ≤ T_A ≤ 70 °C , V_{CC} = 2.5V ± 10% or V_{CC} = 2.0V ± 10%)

PARAMETER	CONDITIONS	SYMBOL	2.5V		2.0V		UNITS	NOTES
			MIN	MAX	MIN	MAX		
Supply Voltage		V _{CC}	2.25	2.75	1.8	2.2	V	1
Supply Voltage		V _{SS}	0	0	0	0	V	
Input High Voltage		V _{IH}	1.8	V _{CC} +0.2	1.4	V _{CC} +0.2	V	1
Input Low Voltage		V _{IL}	-0.3	0.8	-0.3	0.6	V	1
Input Leakage Current	0V ≤ V _{IN} ≤ V _{IH} (max)	I _{LI}	-5	5	-5	5	μA	
Output Leakage Current	0V ≤ V _{OUT} ≤ V _{CC} + 0.2V Output(s) disable	I _{LO}	-5	5	-5	5	μA	
Output High Voltage	I _{OH} = -2 Ma	V _{OH}	2.0	-	1.4	-	V	
Output Low Voltage	I _{OL} = 2 Ma	V _{OL}	-	0.4	-	0.4	V	

Note : 1.All Voltages referenced to Vss

PARAMETER	CONDITIONS	SYMBOL	MAX						UNITS	NOTES
			2.5V			2.0V				
			-50	-60	-80	-60	-80	-100		
Operating Current	RAS , CAS cycling , t _{RC} =min	I _{CC1}	90	70	50	60	40	30	mA	1,2
Standby Current	TTL interface , RAS , CAS = V _{IH} , D _{OUT} =High-Z	I _{CC2}	1.5	1.5	1.5	1.5	1.5	1.5	mA	
	CMOS interface, RAS , CAS ≥ V _{CC} -0.2V		1	1	1	1	1	1	mA	
RAS only refresh Current	t _{RC} = min	I _{CC3}	90	70	50	60	40	30	mA	2
EDO Page Mode Current	t _{PC} = min	I _{CC4}	90	70	50	60	40	30	mA	1,3
CAS Before RAS Refresh Current	t _{RC} = min	I _{CC6}	90	70	50	60	40	30	mA	
Battery Backup Current (S-ver. Only)	Standby with CBR refresh, t _{RC} =31.2μs t _{RAS} ≤ 300ns, D _{OUT} =Hi-Z, CMOS interface	I _{CC7}	1	1	1	1	1	1	mA	
Self Refresh Current	RAS , CAS ≤ 0.2V, D _{OUT} =Hi-Z, CMOS interface	I _{CC8}	1	1	1	1	1	1	mA	

- Note : 1. I_{CC} max is specified at the output open condition.
 2. Address can be changed twice or less while RAS =V_{IL} .
 3. Address can be changed once or less while CAS =V_{IH} .

CAPACITANCE (Ta = 25 °C , Vcc = 2.5V ± 10% or Vcc = 2.0V ± 10%)

PARAMETER	SYMBOL	TYP	MAX	UNIT
Input Capacitance (address)	C _{i1}	-	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{i2}	-	7	pF
Output capacitance (I/O0~I/O3)	C _{i/o}	-	10	pF

AC ELECTRICAL CHARACTERISTICS (Ta = 0 to 70 °C , Vcc = 2.5V ± 10% or Vcc = 2.0 ± 10%, Vss = 0V) (note 14)

Test Conditions

Input timing reference levels : V_{IL}=0.8V, V_{IH}=1.8V (for 2.5V product), V_{IL}=0.6V, V_{IH}=1.4V (for 2.0V product)

Output reference level : V_{OL}= 0.8V, V_{OH}=1.6V (for 2.5V product), V_{OL}= 0.6V, V_{OH}=1.2V (for 2.0V product),

Output Load : 1TTL gate + CL (100pF)

Assumed t_r = 2ns

PARAMETER	SYMBOL	-50		-60		-80		-100		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read or Write Cycle Time	t _{RC}	84		104		134		164		ns	
Read Write Cycle Time	t _{RWC}	110		135		180		225		ns	
EDO-Page-Mode Read or Write Cycle Time	t _{PC}	20		25		35		45		ns	
EDO-Page-Mode Read-Write Cycle Time	t _{PCM}	58		68		80		100		ns	
Access Time From $\overline{\text{RAS}}$	t _{RAC}		50		60		80		100	ns	4
Access Time From $\overline{\text{CAS}}$	t _{CAC}		13		15		20		25	ns	5
Access Time From $\overline{\text{OE}}$	t _{OAC}		13		15		20		25	ns	13
Access Time From Column Address	t _{AA}		25		30		40		50	ns	
Access Time From $\overline{\text{CAS}}$ Precharge	t _{ACP}		28		33		45		60	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10,000	60	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (EDO Page Mode)	t _{RASC}	50	100,000	60	100,000	80	100,000	100	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	7		10		10		15		ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30		40		50		60		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	7	10,000	10	10,000	15	10,000	20	10,000	ns	18
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	40		50		60		75		ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	7		10		10		15		ns	6
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	11	37	14	45	20	60	20	75	ns	7
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		10		ns	
Row Address Setup Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	7		10		10		15		ns	
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	9	25	12	30	15	40	20	50	ns	8
Column Address Setup Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	t _{CAH}	7		10		10		15		ns	
Column Address Hold Time (Reference to $\overline{\text{RAS}}$)	t _{AR}	44		55		70		85		ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	25		30		40		50		ns	

(Continued)

PARAMETER	SYMBOL	-50		-60		-80		-100		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read Command Setup Time	tRCS	0		0		0		0		ns	15
Read Command Hold Time Reference to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9,15,
Read Command Hold Time Reference to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	9
$\overline{\text{CAS}}$ to Output in Low-Z	tCLZ	0		0		0		0		ns	
Output Buffer Turn-off Delay From $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$	tOFF1	0	13	0	15	0	20	0	25	ns	10,17
Output Buffer Turn-off to $\overline{\text{OE}}$	tOFF2	0	13	0	15	0	20	0	25	ns	17,19
Write Command Setup Time	tWCS	0		0		0		0		ns	11,15,
Write Command Hold Time	tWCH	7		10		10		15		ns	15
Write Command Hold Time(Reference to $\overline{\text{RAS}}$)	tWCR	44		55		70		85		ns	15
Write Command Pulse Width	tWP	7		10		10		15		ns	15
Write Command to $\overline{\text{RAS}}$ Lead Time	trWL	13		15		20		25		ns	15
Write Command to $\overline{\text{CAS}}$ Lead Time	tcWL	7		10		10		15		ns	15
Data-in Setup Time	tDS	0		0		0		0		ns	12
Data-in Hold Time	tDH	7		10		15		15		ns	12
Data-in Hold Time (Reference to $\overline{\text{RAS}}$)	tDHR	44		55		70		90		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trWD	67		79		107		135		ns	11
Column Address to $\overline{\text{WE}}$ Delay Time	tAWD	42		49		67		85		ns	11
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcWD	30		34		47		60		ns	11
Transition Time (rise or fall)	tT	1	50	1	50	1	50	1	50	ns	2,3
Refresh Period (2048 cycles)	tREF		32		32		32		32	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	trPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ Setup Time(CBR REFRESH)	tCSR	5		5		5		5		ns	1
$\overline{\text{CAS}}$ Hold Time(CBR REFRESH)	tCHR	10		10		15		15		ns	1
$\overline{\text{OE}}$ Hold Time From $\overline{\text{WE}}$ During Read-Mode-Write Cycle	toEH	7		10		20		20		ns	16
$\overline{\text{OE}}$ Low to $\overline{\text{CAS}}$ High Setup Time	toES	5		5		10		10		ns	
$\overline{\text{OE}}$ High Hold Time From $\overline{\text{CAS}}$ High	toEHC	5		5		5		5		ns	
$\overline{\text{OE}}$ Precharge Time	toEP	5		5		5		5		ns	
$\overline{\text{OE}}$ Setup Prior to $\overline{\text{RAS}}$ During Hidden Refresh Cycle	tORD	0		0		0		0		ns	
Data Output Hold After $\overline{\text{CAS}}$ Returning Low	tCOH	3		3		3		3		ns	
Output Disable Delay From $\overline{\text{WE}}$	tWHZ	0	13	0	15	0	20	0	25	ns	
Self Refresh $\overline{\text{RAS}}$ Low Pulse width	trASS	100		100		100		100		us	20,21
Self Refresh $\overline{\text{RAS}}$ High Precharge Time	trPS	84		104		134		164		ns	20,21
Self Refresh $\overline{\text{CAS}}$ Hold Time	tCHS	-50		-50		-50		-50		ns	20,21
Read Setup Time Reference to $\overline{\text{RAS}}$ in CBR/SR	trSR	0		0		0		0		ns	20,21
Read Hold Time Reference to $\overline{\text{RAS}}$ in CBR/SR	trHR	7		10		10		15		ns	20,21

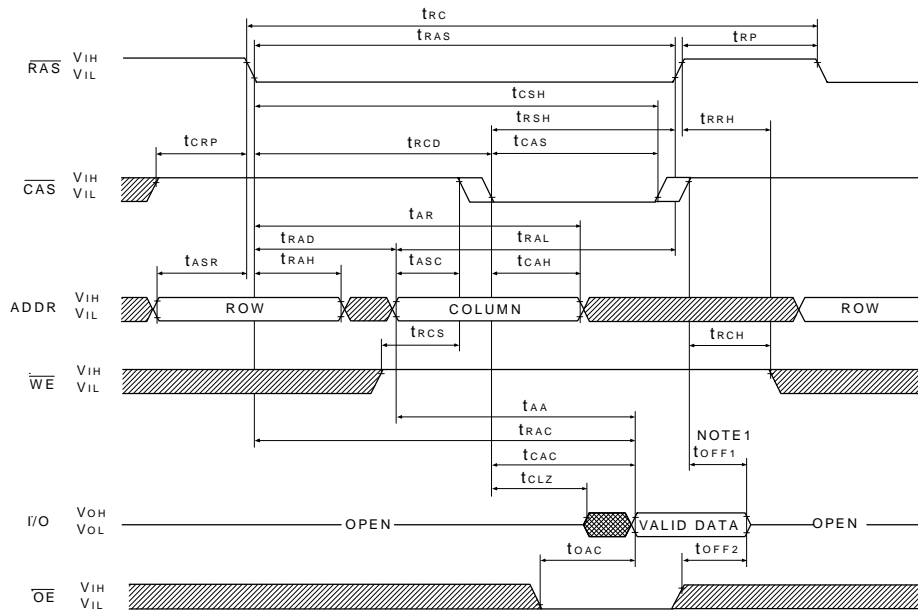
Notes :

1. Enables on-chip refresh and address counters.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
3. In addition to meet the transition rate specification, all input signals must transit between V_{IH} and V_{IL} in a monotonic manner.
4. Assume that $t_{RCD} < t_{RCD}(\max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assume that $t_{RCD} \geq t_{RCD}(\max)$
6. If \overline{CAS} is low at the falling edge of \overline{RAS} , data-out will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, \overline{CAS} and \overline{RAS} must be pulsed high.
7. Operation within the t_{RCD} limit ensures that $t_{RCD}(\max)$ can be met, $t_{RCD}(\max)$ is specified as a reference point only ; if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, access time is controlled by t_{CAC} .
8. Operation within the t_{RAD} limit ensures that $t_{RAD}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only ; if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, access time is controlled by t_{AA} .
9. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
10. $t_{OFF1}(\max)$ defines the time at which the output achieves the open circuit condition ; it is not a reference to V_{OH} or V_{OL} .
11. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\min)$, $t_{AWD} \geq t_{AWD}(\min)$ and $t_{CWD} \geq t_{CWD}(\min)$, the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until \overline{CAS} and \overline{RAS} or \overline{OE} go back to V_{IH}) is indeterminate. \overline{OE} held high and \overline{WE} taken low after \overline{CAS} goes low result in a LATE WRITE (\overline{OE} - controlled) cycle.
12. Those parameters are referenced to \overline{CAS} leading edge in EARLY WRITE cycles and \overline{WE} leading edge in LATE WRITE or READ-MODIFY- WRITE cycles.
13. During a READ cycle, if \overline{OE} is low then taken HIGH before \overline{CAS} goes high, I/O goes open, if \overline{OE} is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. An initial pause of $200\mu s$ is required after power-up followed by eight \overline{RAS} refresh cycles (\overline{RAS} only or CBR) before proper device operation is assured. The eight \overline{RAS} cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
15. WRITE command is defined as \overline{WE} going low.
16. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OFF2} and t_{OEH} met (\overline{OE} high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
17. The I/Os open during READ cycles once t_{OFF1} or t_{OFF2} occur.
18. Each \overline{CAS} must meet minimum pulse width.
19. All IOs controlled by \overline{OE} , regardless \overline{CAS} .
20. Self refresh mode is initiated by performing a CBR refresh cycle and holding \overline{RAS} low for the specified t_{RASS} . Self refresh mode is terminated by rising \overline{RAS} high for a minimum time of t_{RPS} .
21. For all of the refresh mode expect the distributed CBR refresh mode, all rows must be refreshed within the refresh rate before and after self refresh.

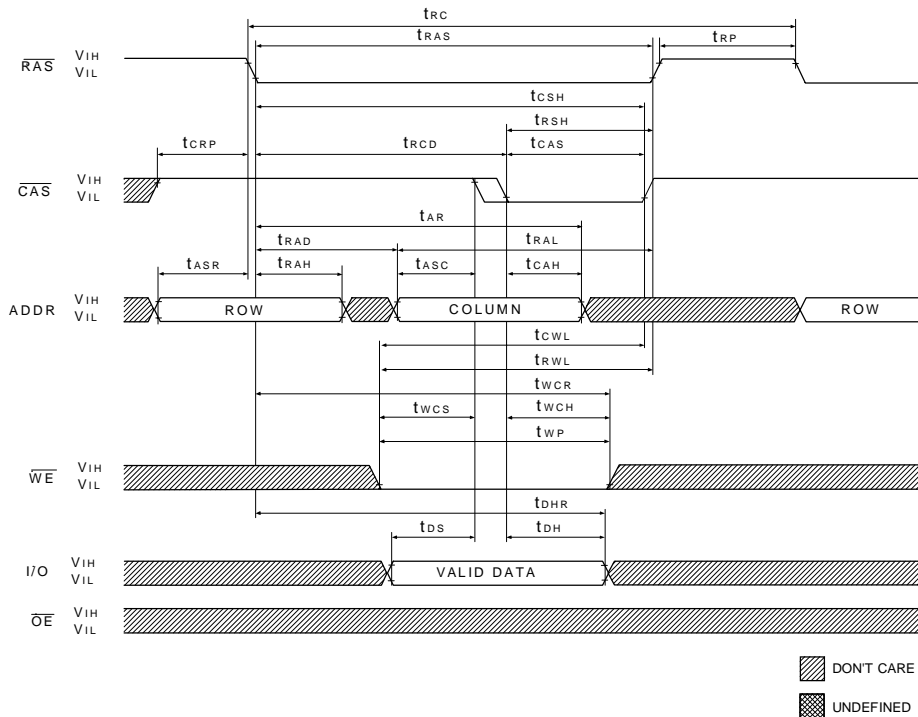
TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DQs
						ROW	COL	
Standby		H	H→X	X	X	X	X	High-Z
Read		L	L	H	L	ROW	COL	Data-Out
Write (Early Write)		L	L	L	X	ROW	COL	Data-In
Read-Write		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-Page-Mode Read	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	X	COL	Data-Out
	Any Cycle	L	L→H	H	L	X	X	Data-Out
EDO-Page-Mode Write (Early)	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	X	COL	Data-In
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	X	COL	Data-Out, Data-In
Hidden Refresh		L→H→L	L	H	L	ROW	COL	Data-Out
RAS -Only Refresh		L	H	X	X	ROW	X	High-Z
CBR Refresh		H→L	L	H	X	X	X	High-Z
Self Refresh		H→L	L	H	X	X	X	High-Z

READ CYCLE



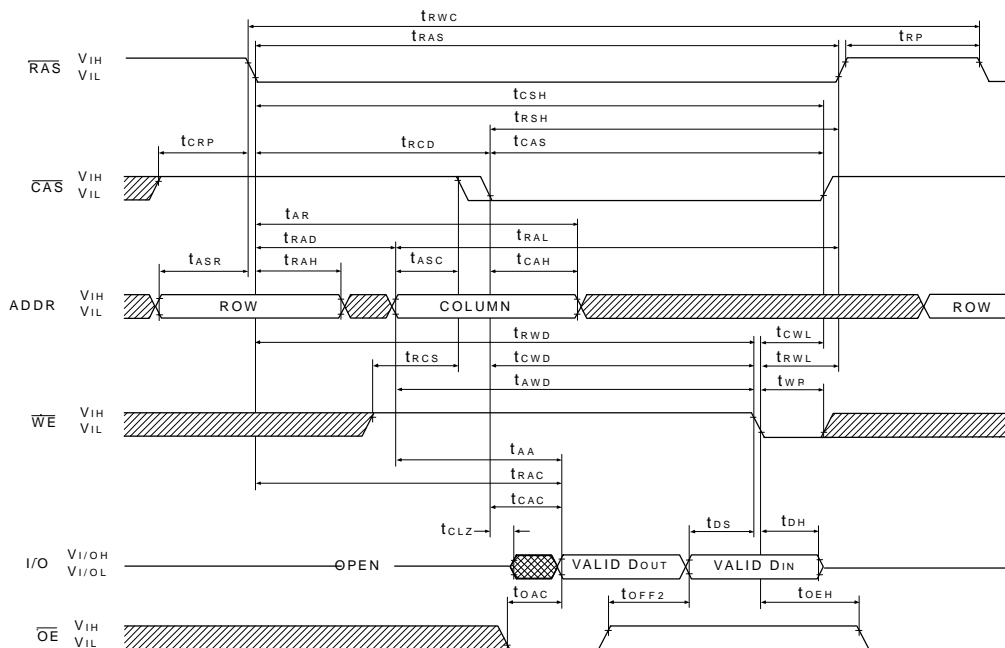
EARLY WRITE CYCLE



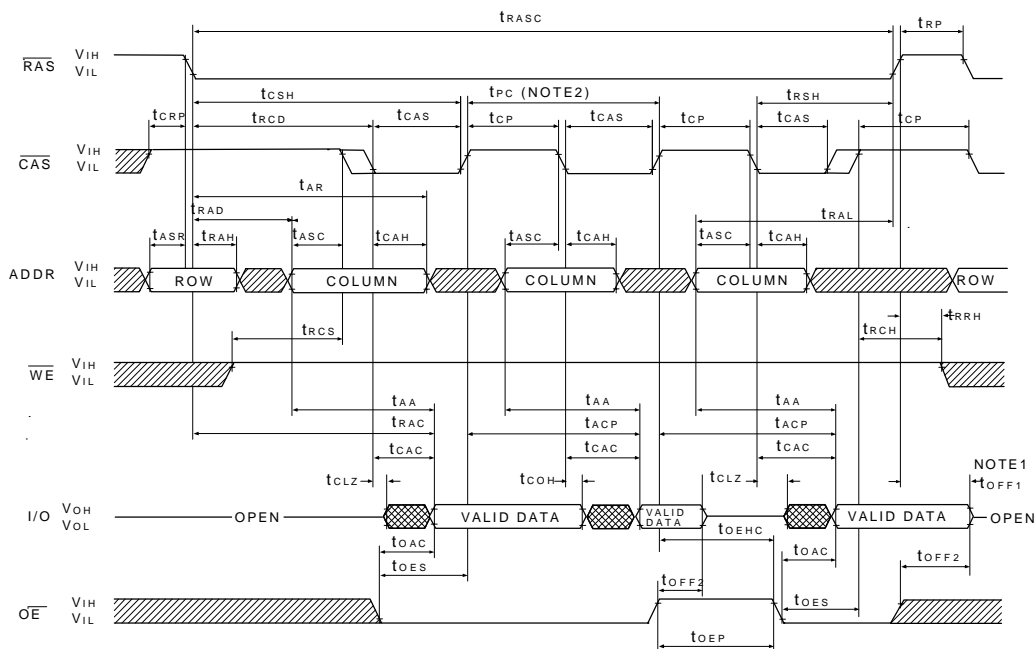
 DONT CARE
 UNDEFINED

Note: 1. t_{OFF1} is referenced from the rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.

**READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)**



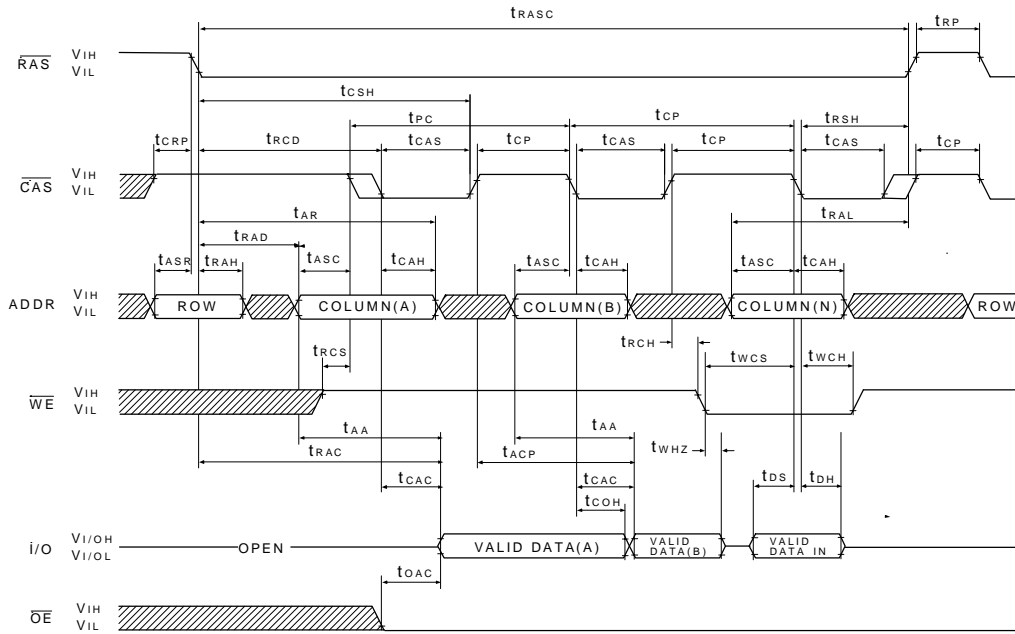
EDO-PAGE-MODE READ CYCLE



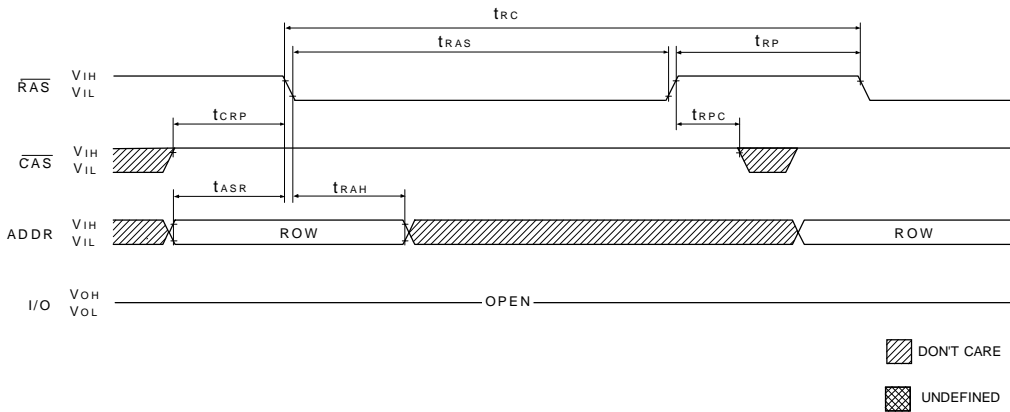
▨ DONT CARE
▩ UNDEFINED

- *NOTE : 1. t_{OFF1} is referenced from the rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.
 2. t_{PC} can be measured from falling edge of \overline{CAS} to falling edge of \overline{CAS} , or from rising edge of \overline{CAS} to rising edge of \overline{CAS} . Both measurements must meet the t_{PC} specification.

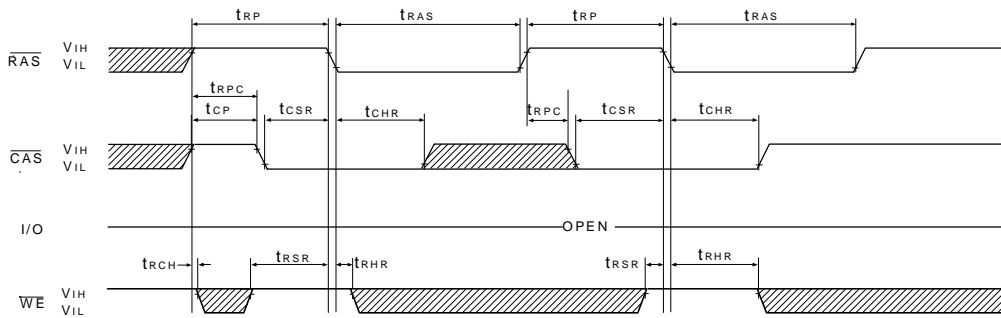
**EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)**



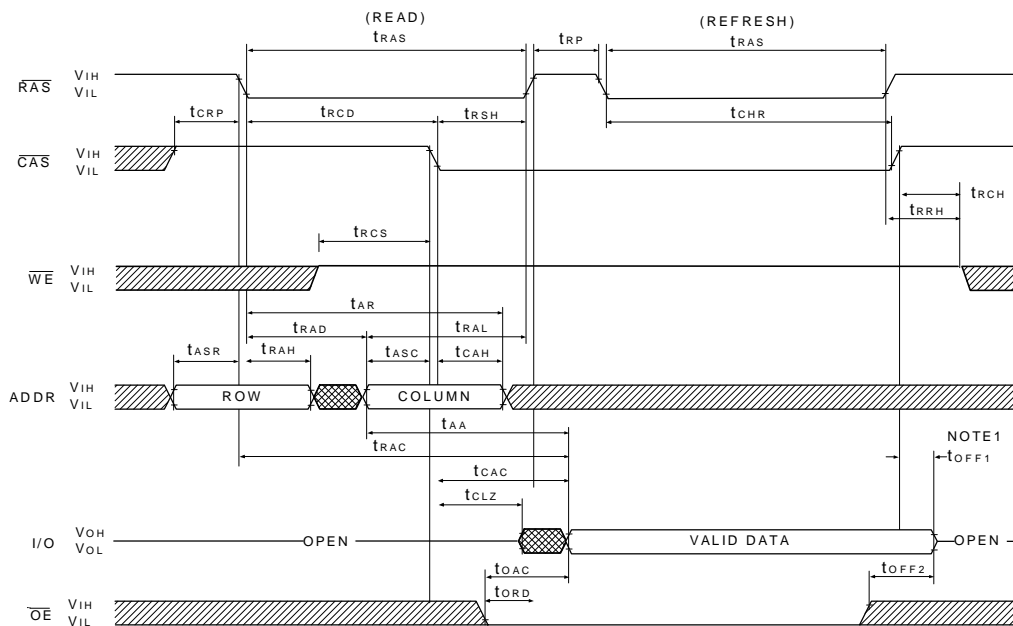
**RAS ONLY REFRESH CYCLE
(ADDR = A0~A10 ; OE , WE = DON'T CARE)**



**CBR REFRESH CYCLE
(A0~A10 ; \overline{OE} = DON'T CARE)**



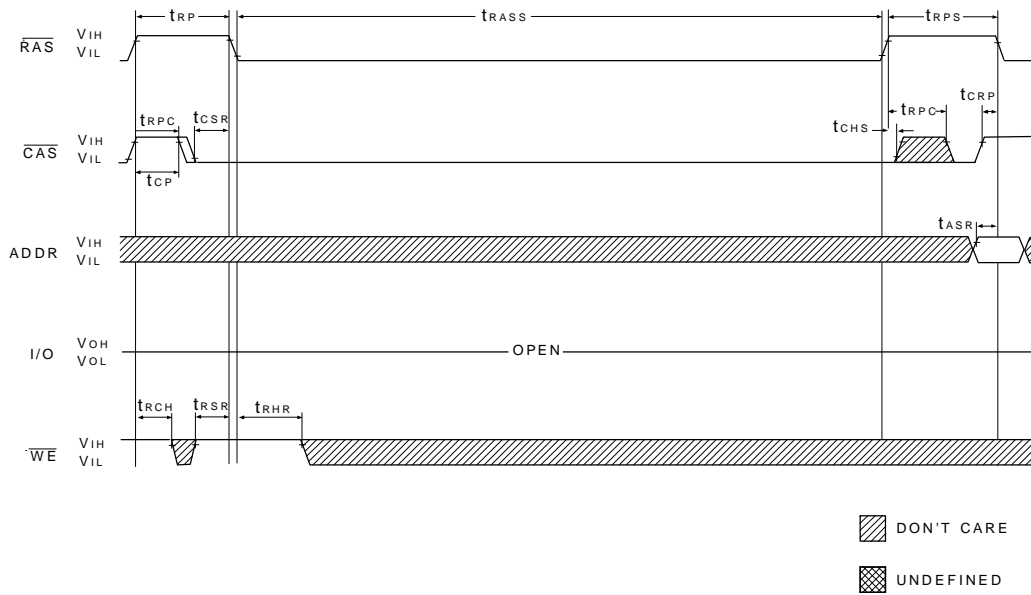
**HIDDEN REFRESH CYCLE
(\overline{WE} = HIGH ; \overline{OE} = LOW)**



 DON'T CARE
 UNDEFINED

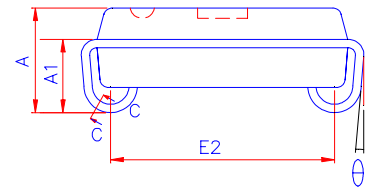
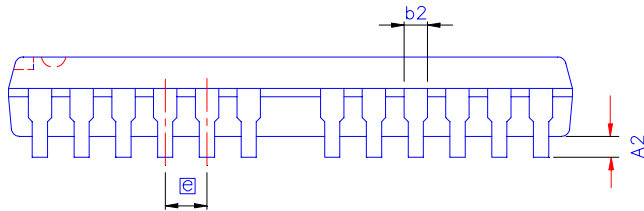
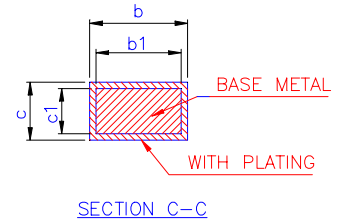
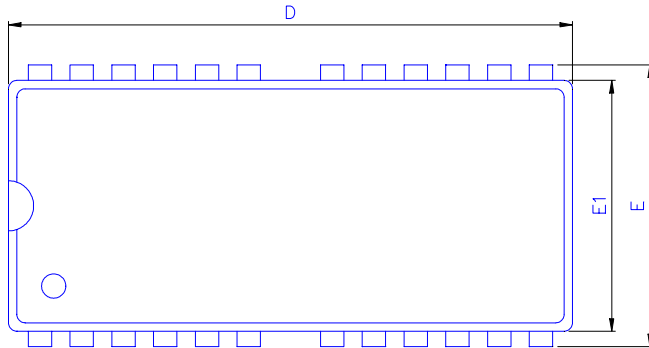
Note : 1. t_{OFF1} is reference from the rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.

**SELF REFRESH CYCLE
(\overline{OE} = DON'T CARE)**



PACKING DIMENSIONS

24 / 26-LEAD SOJ(300mil)



Symbol	Dimension mm			Dimension inch		
	Min	Nom	Max	Min	Nom	Max
A	3.25	3.51	3.76	0.128	0.138	0.148
A1	2.08	-	-	0.082	-	-
A2	0.635	-	-	0.025	-	-
B	0.41		0.51	0.016		0.020
B1	0.41	0.46	0.48	0.016	0.018	0.019
B2	0.66	0.71	0.81	0.026	0.028	0.032
C	0.18	0.20	0.28	0.007	0.008	0.012
C1	0.18		0.28	0.007		0.011
D	17.02	17.15	17.27	0.670	0.675	0.680
E		8.51			0.335	
E1	7.49	7.62	7.75	0.295	0.300	0.305
θ	0°		10°	0°		10°
e	1.27 BASIC			0.050 BASIC		

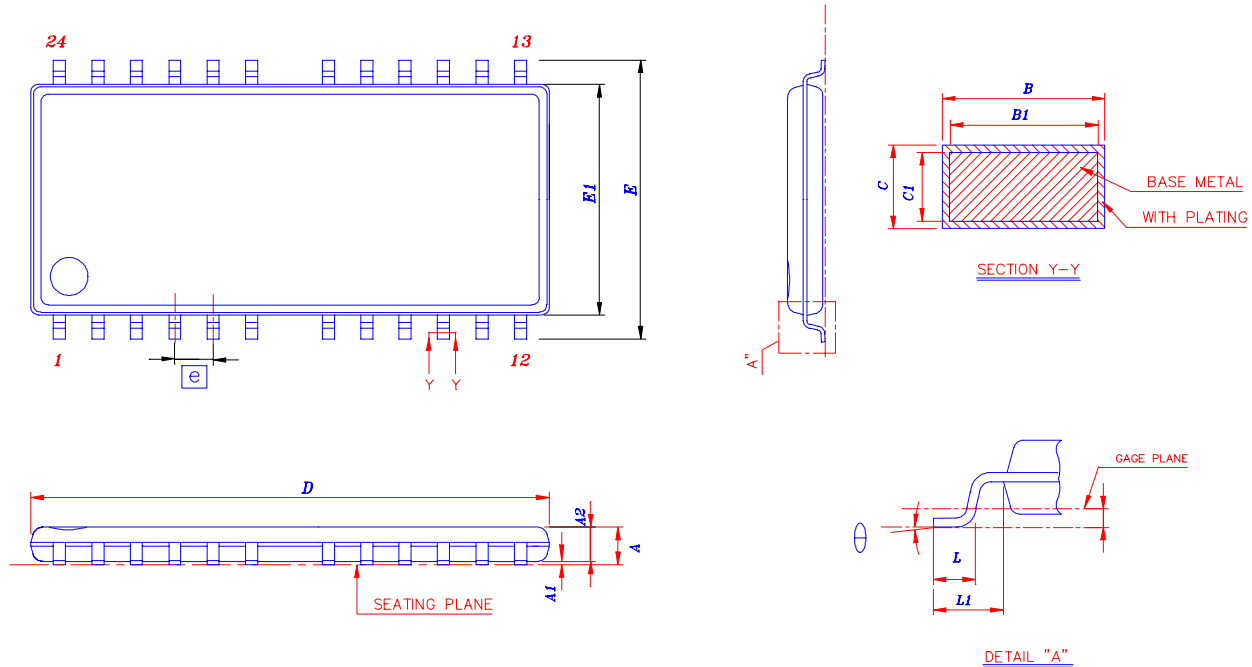
PACKING

DIMENSIONS

24 / 26-LEAD

TSOP(II)

DRAM(300mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
B	0.30	-	0.52	0.012	-	0.02
B1	0.30	0.40	0.45	0.012	0.016	0.018
C	0.12	-	0.21	0.005	-	0.008
C1	0.12	0.15	0.16	0.005	0.006	0.0063
D	17.01	17.14	17.27	0.67	0.675	0.68
ZD	0.95 REF			0.374 REF		
E	9.02	9.22	9.42	0.355	0.363	0.371
E1	7.49	7.62	7.75	0.295	0.3	0.305
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.031 REF			0.080 REF		
e	1.27 BSC			0.05 BSC		
R	0.12	-	0.25	0.005	-	0.01
R1	0.12	-	-	0.005	-	-
θ	0°	-	5°	0°	-	5°
y	-	-	0.10	-	-	0.004

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