AT&T Microelectronics

ATT1700A Series Serial ROM

Features

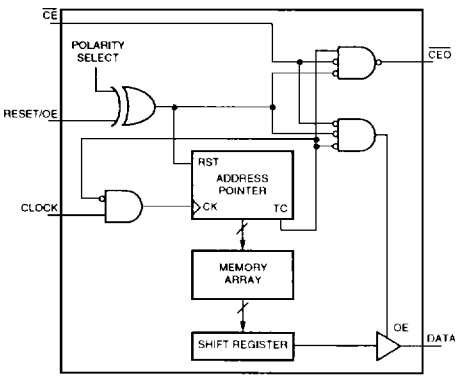
- 32K, 64K, and 128K x 1 Serial ROMs for configuration of ATT3000 and *ORCA* Series FPGAs
- Pinout and functional replacement of *Xilinx XC1700* series
- Simple 4-wire interface
- Cascadable to support large FPGAs, multiple configurations, and multiple FPGAs
- 8-pin, plastic DIP; 8-pin SOIC; and 20-pin PLCC packages
- Programming support from leading programmer manufacturers
- Programmable polarity on RESET/OE pin
- Full static operation
- Standby current—100 µA typical
- Operating current—10 mA maximum
- 10 MHz maximum clock rate
- Electrostatic discharge protection > 4000 V
- Temperature ranges:
  Commercial: 0 °C to 70 °C
  Industrial: –40 °C to +85 °C

Description

The ATT1700A Series Serial ROM family provides easy-to-use, cost-effective, nonvolatile memory for configuring ATT3000 and *ORCA* Series FPGAs. The ATT1700A Series consists of one-time programmable (OTP) devices. The ATT1700A devices are available in 8-pin plastic DIP, 8-pin SOIC, and 20-pin PLCC packages.

The ATT1700A Series is a pinout and functional replacement for the ATT1700 and *Xilinx XC1700* families and can be programmed by most commercially available programmers. FPGA development tools, such as *ORCA* Foundry, generate configuration files in *Intel*, *Motorola*, and *Tektronix* formats for use in programmers.

The ATT1700A Series is most often used when the ATT3000 Series and *ORCA* Series FPGAs are configured in the master serial mode. The primary advantage of this configuration mode is that it provides a simple, four-wire interface between the FPGA and configuration memory (as in Figure 1, where $\overline{CEO}$ does not connect to the FPGA).



5-3977(C)

Figure 1. Block Diagram

Pin Information

Table 1. Pin Descriptions

Symbol	Pin Numbers		I/O	Function
	8-Pin	20-Pin		
DATA	1	2	O	DATA output from the serial ROM to FPGA synchronous with the CLOCK input. DATA is 3-stated when either $\overline{CE}$ or OE is inactive.
CLOCK	2	4	I	CLOCK is an input used to increment the address pointer which strobes data out of the DATA pin.
RESET/OE	3	6	I	RESET/OUTPUT ENABLE is a dual-function pin used to reset and enable the ATT1700A Series device. An active level on both $\overline{CE}$ and OE inputs enables data out of the DATA pin. An active level on RESET resets the address pointer. When the serial ROM is programmed, the polarity of RESET/OE is set either with RESET active-high and OE active-low or with RESET active-low and OE active-high.
$\overline{CE}$	4	8	I	$\overline{\text{CHIP ENABLE}}$ is an input used to select the device. An active level on both $\overline{CE}$ and OE enables data out of the device. A high on $\overline{CE}$ disables the address pointer and forces the serial ROM into a low-power mode.
VSS	5	10	I	Ground.
$\overline{CEO}$	6	14	O	$\overline{\text{CHIP ENABLE OUT}}$ is asserted low on the clock cycle following the last bit read from the device. $\overline{CEO}$ remains low as long as $\overline{CE}$ and OE are both active.
VPP	7	17	I	VPP is an input used by programmers when programming the serial ROM. The programming operations, voltages, and timing are defined later in this data sheet. For read operations, VPP must be tied directly to VDD.
VDD	8	20	I	Power supply.

FPGA Configuration

The functionality of the AT&T FPGAs is determined by the contents of the FPGA's configuration memory. The configuration memory is loaded either automatically at powerup or with a configuration command by pulsing the $\overline{PRGM}$ pin low. The FPGAs can be programmed in a variety of modes, and the mode used is determined by the inputs into the FPGA's M[2:0] pins. The configuration modes allow the FPGA to act as a master or a slave and also allow configuration data to be transmitted either serially or in parallel. The ATT1700A Series is targeted for use when the FPGA is configured serially, primarily in the master serial mode. Table 2 provides the configuration memory requirements for AT&T FPGAs.

FPGA Master Serial Mode

The master serial mode provides a simple interface between the FPGA and the serial ROM. Four interface lines, DATA, CLOCK, $\overline{CE}$, and RESET/OE, are required to configure the FPGA. Upon powerup or a configure command, the FPGA configures in the master serial mode when the FPGA's M[2:0] pins are low. The configuration data is transmitted serially into the FPGA's DIN pin from the serial ROM's DATA pin. To synchronize to the data, the FPGA's CCLK output is routed into the serial ROM's CLOCK input.

Since the clock and data lines of the FPGA are directly connected, the primary interface issues are controlling the serial ROM's $\overline{CE}$ and RESET/OE pins. It is necessary to avoid contention on the FPGA CCLK and DIN pins after configuration. If user-programmable, dual-function pins such as DIN are used only for the configuration process, they should be configured so that they do not float and are not in contention with other signals.

FPGA Configuration (continued)

For example, DIN can be programmed as an output during normal operation. An alternate method is to program DIN as an input, with an internal pull-up resistor enabled.

If DIN is used for another function after configuration, the designer must avoid contention. The low during configuration $\overline{LDC}$ pin can be used to control the serial ROM's $\overline{CE}$ and OE inputs to disable the serial ROM's DATA pin, one clock cycle before the FPGA's DONE signal is active. If the $\overline{LDC}$ pin is used, it must be configured to output a constant logic "1" after configuration.

Table 2. Configuration Requirements

AT&T FPGA	Memory Requirements
ATT3020	14,819
ATT3030	22,216
ATT3042	30,824
ATT3064	46,104
ATT3090	64,200
ATT1C03	57,144
ATT1C05	76,376
ATT1C07	98,296
ATT1C09	122,904
ATT2C04	65,424
ATT2C06	91,024
ATT2C08	115,600
ATT2C10	148,944
ATT2C12	179,856
ATT2C15	220,944
ATT2C26	307,024
ATT2C40	474,176

The FPGA-serial ROM interface used depends upon the system configuration and configuration requirements. The following are some typical system configurations:

- Configuring an FPGA at powerup
- Configuring an FPGA in response to a configure command
- One serial ROM configures an FPGA with multiple configuration programs
- Cascaded serial ROMs configure daisy-chained FPGAs

In addition to the clock and data lines, the FPGA pins used in configuration/start-up are $\overline{RESET}$, DONE, $\overline{PRGM}$, $\overline{LDC}$, HDC, and $\overline{INIT}$. Normally, only a small subset of these pins is used to control the serial ROM's $\overline{CE}$ and RESET/OE pins. In some applications, the RESET/OE signal is generated by the system host, not the FPGA. For example, the host may generate a system reset, allowing the FPGA and the serial ROM to be synchronously reset.

ATT3000 Series/*ORCA* Series Differences

While both the ATT3000 and *ORCA* Series have $\overline{RESET}$, $\overline{LDC}$, HDC, $\overline{INIT}$, DIN, CCLK, and DOUT pins, there are some configuration differences in the FPGAs. The ATT3000 Series DONE/$\overline{PROG}$ pin is a shared open-drain I/O while the *ORCA* Series has discrete DONE and $\overline{PRGM}$ pins. When the system generates a configure command to the ATT3000, the DONE/$\overline{PROG}$ pin is held low throughout the configuration cycle. For the *ORCA* Series, the $\overline{PRGM}$ pin is pulsed low and returned high to initiate configuration. A second difference is the internal pull-ups on the mode select pins. For the ATT3000 Series, only M2 has an internal pull-up during configuration, but for the *ORCA* Series, M[3:0] have pull-ups.

Configuring the FPGA at Powerup

The ATT1700A series can configure FPGAs at powerup. There is level-sensitive power-on-reset circuitry included in the device which resets the address pointer during powerup. The ATT3000 and *ORCA* FPGAs enable the serial ROM using either the DONE or $\overline{LDC}$ pins, with a low level on these signals at powerup connected to the $\overline{CE}$ and RESET/$\overline{OE}$ pins on the serial ROM. With this interface, when these FPGA signals go high at the end of configuration, the serial ROM is disabled.

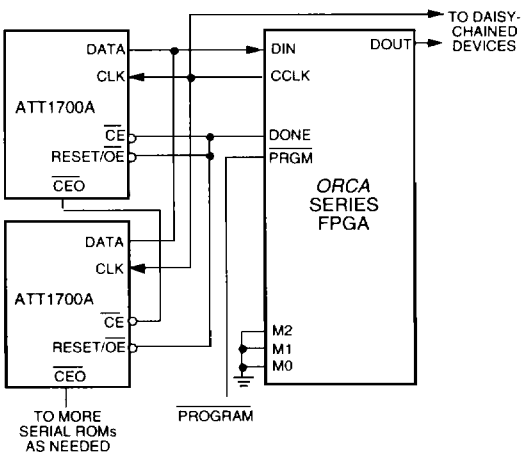


Figure 2. *ORCA* Master Serial Configuration

FPGA Configuration (continued)

Configuring the *ORCA* Series FPGA with a Configure Command

The FPGA needs to enable the serial ROM's RESET/OE and $\overline{CE}$ inputs. The polarity of the RESET/OE input is programmable in the ATT1700A series. In the method shown in Figure 2, the system generates an active-low configure pulse to the FPGA's $\overline{PRGM}$ pin. In this case, the RESET/OE pin of the serial ROM is programmed so that RESET is active-high and OE is active-low.

The FPGA's DONE pin is then routed to the serial ROM's $\overline{CE}$ and RESET/OE pins. At the end of configuration, DONE returns high, disabling, and resetting the serial ROM. Alternatively, the $\overline{LDC}$ pin can be used instead of the DONE pin to enable the serial ROM.

Configuring the ATT3000 Series FPGA with a Configure Command

In the method illustrated in Figure 3, the system generates an active-low configure pulse on the FPGA's DONE/$\overline{PROG}$ pin. The system then releases the open-drain DONE/$\overline{PROG}$ pin, allowing the FPGA to control it and drive it low during configuration. DONE/$\overline{PROG}$ is generally connected to both the $\overline{CE}$ and RESET/OE pins of the serial ROM, which has been programmed so that RESET is active-high and OE is active-low. At the end of configuration, the DONE/$\overline{PROG}$ pin returns high, disabling, and resetting the serial ROM. The $\overline{LDC}$ pin may be used instead of the DONE/$\overline{PROG}$ pin to enable the serial ROM, as shown.

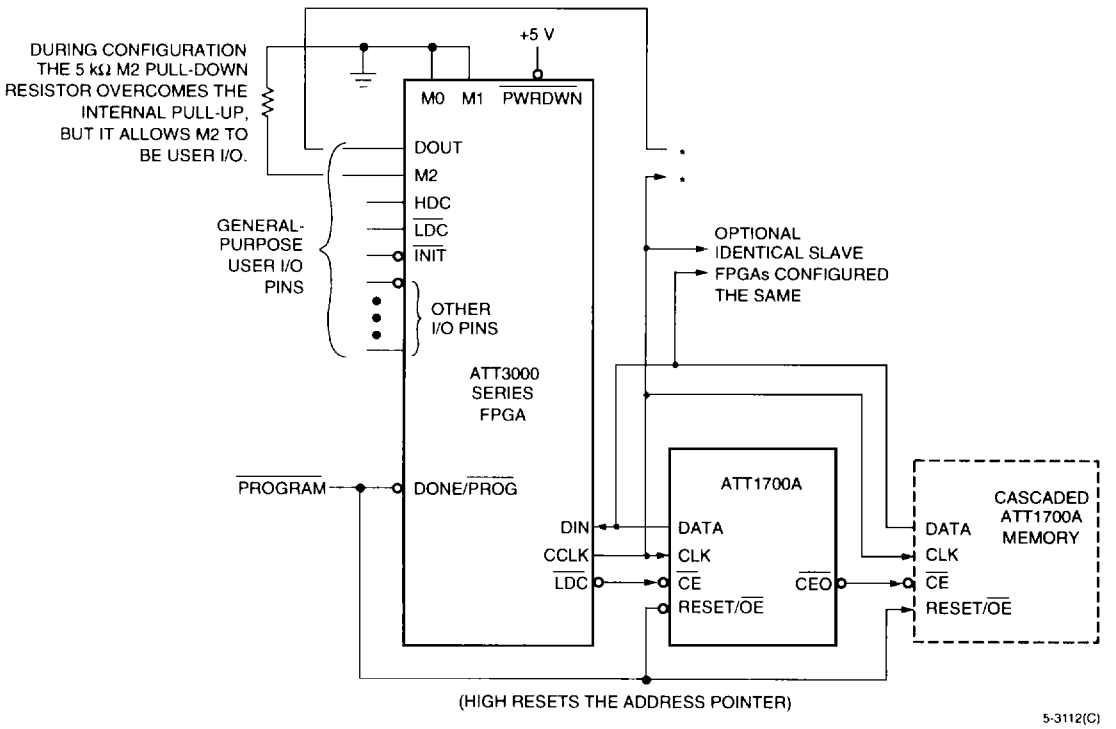


Figure 3. ATT3000 Master Serial Configuration

FPGA Configuration (continued)

Programming the FPGA with the Address Pointer Unchanged Upon Completion

In the two interfaces discussed above, the serial ROM is reset at the completion of configuration. This is typically the case when one or more serial ROMs is used to configure one or more FPGAs with one configuration program. In applications in which a serial ROM is used to configure an FPGA with multiple configuration programs, the address pointer should not be reset. This allows the next configuration program to be loaded at the next internal ROM address.

When multiple FPGA configurations are stored in a serial ROM, the OE pin of the serial ROM should be tied low. Upon powerup, the internal address pointer is reset and configuration begins with the first set of configuration data stored in memory. Since the OE pin is held low, the address pointer is left unchanged after configuration is complete. To reprogram the FPGA with another program, the DONE/$\overline{\text{PROG}}$ or $\overline{\text{PRGM}}$ pin is pulled low, and configuration begins at the last value of the address pointer.

Cascading Serial ROMs

Figure 2 and Figure 3 also illustrate the cascading of serial ROMs. This is done to provide additional memory for large FPGAs and/or for configuring multiple FPGAs in a daisy chain. The serial ROMs are cascaded with the next ROM's $\overline{\text{CE}}$ input connected to the $\overline{\text{CEO}}$ output of the previous serial ROM. All of the cascaded serial ROM's DATA lines are routed to the FPGA's DIN input, and the FPGA's CCLK output is routed in parallel to all of the serial ROMs' CLOCK inputs.

After the last bit from the first serial ROM is read, the first serial ROM asserts $\overline{\text{CEO}}$ low and disables its DATA output. The next serial ROM recognizes the low on its $\overline{\text{CE}}$ input and enables its DATA output. The inactive $\overline{\text{CE}}$ into all serial ROMs causes the inactive DATA pins to be 3-stated after configuration is finished.

The ATT3000 DONE/$\overline{\text{PROG}}$ signal and the *ORCA* DONE signal are open-drain outputs with optional internal pull-ups and can be used to control the output enable of multiple serial ROMs. Extremely large, cascaded serial memories may require additional logic if the DONE/$\overline{\text{PROG}}$ or DONE signals are too slow to activate many serial ROMs.

Standby Mode

The ATT1700A Series enters a low-power standby mode when $\overline{\text{CE}}$ is high. In standby mode, the serial ROM consumes less than 100 µA of current. The DATA pin remains in the high-impedance state regardless of the state of the RESET/OE input.

RESET/OE Polarity

The ATT1700A Series allows the user to select the polarity of the dual-function RESET/OE pin. The PROM programmer software is used to program the desired polarity. The method used to select a polarity depends on the prom programmer user interface.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Supply Voltage Relative to GND	V_{DD}	–0.6	6.6	V
Programming Voltage Relative to GND	V_{PP}	–0.6	14.0	V
Input Voltage with Respect to GND	V_{IN}	–0.6	V_{DD} + 0.6	V
Voltage Applied to 3-state Output	V_{TS}	–0.6	V_{DD} + 0.6	V
Ambient Storage Temperature	T_{stg}	–65	150	°C
Maximum Soldering Temperature	T_{SOL}	—	300	°C
Maximum Junction Temperature	T_J	—	125	°C

Electrical Characteristics

Table 3. dc Electrical Characteristics

Commercial: 0 °C ≤ T_A ≤ 70 °C, V_{DD} = 5.0 V ± 5%; Industrial: –40 °C ≤ T_A ≤ +85 °C, V_{DD} = 5.0 V ± 10%.

Parameter	Symbol	Conditions	Min	Max	Unit
High-level Input Voltage	V_{IH}	—	2.0	V_{DD}	V
Low-level Input Voltage	V_{IL}	—	–0.3	0.8	V
High-level Output Voltage	V_{OH}	V_{DD} = 3.0 V, I_{OH} = –4.0 mA	2.40	—	V
	V_{OH}	V_{DD} = 4.5 V, I_{OH} = –4.0 mA	3.86	—	V
Low-level Output Voltage	V_{OL}	V_{DD} = 5.5 V, I_{OL} = 4.0 mA	—	0.32	V
Supply Voltage Relative to V_{SS}:					
Commercial	—	—	4.75	5.25	V
Industrial	—	—	4.50	5.50	V
Standby Supply Current	I_{DDSB}	V_{IN} = V_{DD} = 5.5 V	—	100	µA
		V_{IN} = V_{DD} = 3.6 V	—	50	µA
Operating Supply Current	I_{DD}	V_{DD} = 5.5 V, Clock = 10 MHz	—	10	mA
		V_{DD} = 3.6 V, Clock = 2.5 MHz	—	2	mA
Input Leakage Current	I_{IL}	V_{DD} = 5.5 V, V_{IN} = V_{DD} and 0 V	–10	10	µA
Output Leakage Current	I_{IL}	V_{DD} = 5.5 V, V_{IN} = V_{DD} and 0 V	–10	10	µA
Pin Capacitance	C_{IN}	V_{CC} = 5 V, T_A = 25 °C, F_{CLK} = 1 MHz	—	10	pF

Electrical Characteristics (continued)

Table 4. ac Characteristics During Read

Commercial: 0 °C ≤ T_A ≤ 70 °C, V_{DD} = 5.0 V ± 5%; Industrial: –40 °C ≤ T_A ≤ +85 °C, V_{DD} = 5.0 V ± 10%.

Parameter	Symbol	Test Conditions	Limits 3.0 V ≤ V_{DD} ≤ 6.0 V		Limits 4.5 V ≤ V_{DD} ≤ 6.0 V		Unit
			Min	Max	Min	Max	
OE to Data Delay	T_{OE}	—	—	45	—	45	ns
$\overline{CE}$ to Data Delay	T_{CE}	—	—	60	—	50	ns
CLOCK to DATA Delay	T_{CAC}	—	—	200	—	60	ns
DATA Hold from $\overline{CE}$, OE, or CLOCK	T_{OH}	—	0	—	0	—	ns
$\overline{CE}$ or OE to DATA Float Delay	T_{DF}	—	—	50	—	50	ns
CLOCK Frequency	T_{CLK}	—	—	2.5	—	10	MHz
CLOCK Low Time	T_{CL}	—	100	—	25	—	ns
CLOCK High Time	T_{CH}	—	100	—	25	—	ns
$\overline{CE}$ Setup Time to CLOCK (Guarantees correct counting.)	T_{SCE}	—	40	—	25	—	ns
$\overline{CE}$ Hold Time from CLOCK (Guarantees correct counting.)	T_{HCE}	—	0	—	0	—	ns
OE High Time (Guarantees counters are reset.)	T_{HOE}	$\overline{CE}$ high or low	100	—	20	—	ns

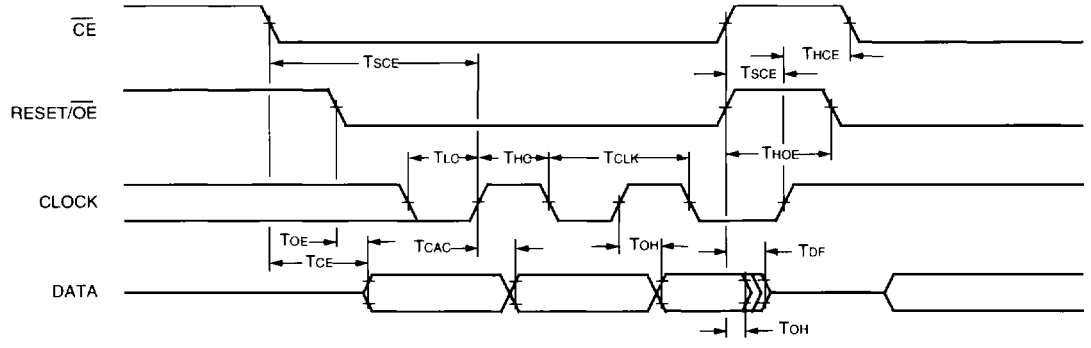


Figure 4. Read Characteristics

Electrical Characteristics (continued)

Table 5. ac Characteristics at End of Read

Commercial: 0 °C ≤ T_A ≤ 70 °C, V_{DD} = 5.0 V ± 5%; Industrial: –40 °C ≤ T_A ≤ +85 °C, V_{DD} = 5.0 V ± 10%.

Parameter	Symbol	Limits 3.0 V ≤ V_{DD} ≤ 6.0 V		Limits 4.5 V ≤ V_{DD} ≤ 6.0 V		Unit
		Min	Max	Min	Max	
CLOCK to DATA Disable Delay	T_{CDF}	—	50	—	50	ns
CLOCK to $\overline{CEO}$ Delay	T_{OCK}	—	65	—	40	ns
$\overline{CE}$ to $\overline{CEO}$ Delay	T_{OCE}	—	45	—	40	ns
$\overline{OE}$ to $\overline{CEO}$ Delay	T_{OOE}	—	40	—	40	ns

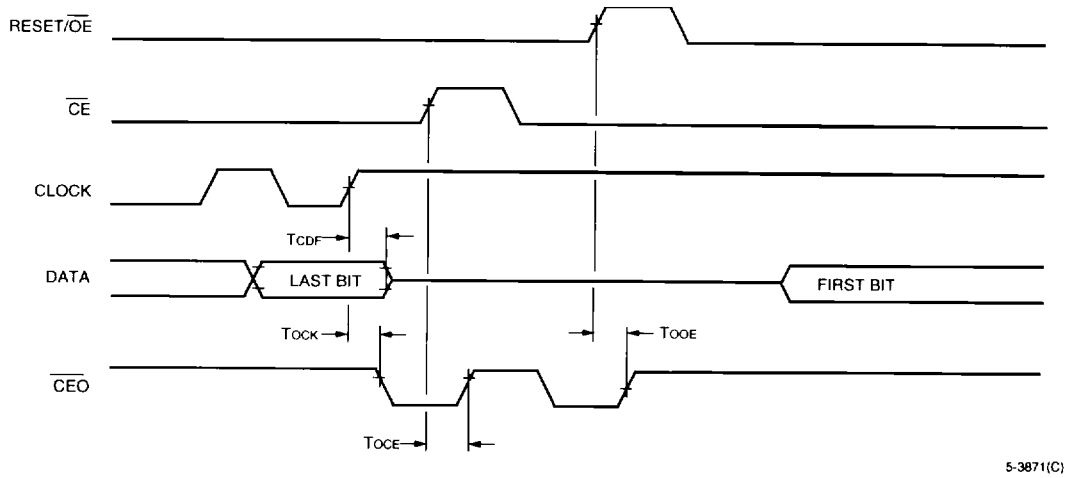


Figure 5. Read Characteristics at End of Array

Electrical Characteristics (continued)

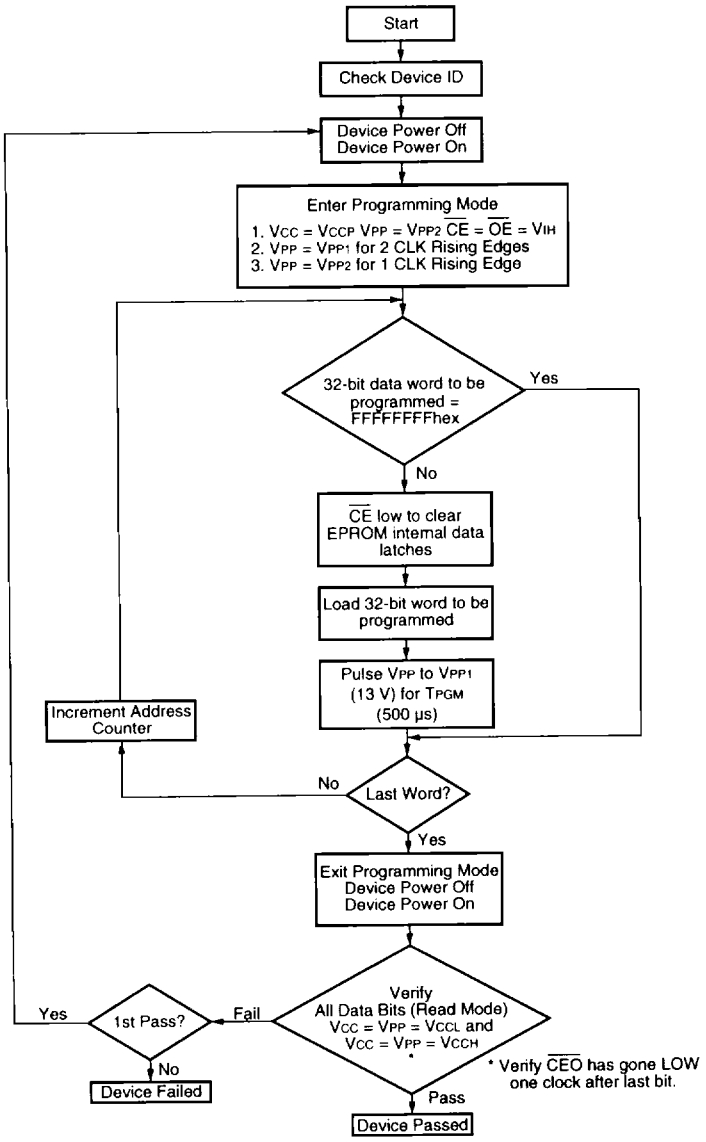


Figure 6. ATT1700A Programming

Electrical Characteristics (continued)

Table 6. dc Programming Specifications

Commercial: 0 °C ≤ T_A ≤ 70 °C, V_{DD} = 5.0 V ± 5%; Industrial: –40 °C ≤ T_A ≤ +85 °C, V_{DD} = 5.0 V ± 10%.

Parameter	Symbol	Min	Max	Unit
Supply Voltage During Programming	V_{CCP}	5.0	6.0	V
Low-level Input Voltage	V_{IL}	0.0	0.5	V
High-level Input Voltage	V_{IH}	2.4	V_{CC}	V
Low-level Output Voltage	V_{OL}	—	0.4	V
High-level Output Voltage	V_{OH}	3.7	—	V
Programming Voltage*	V_{PP1}	12.5	13.5	V
Programming Mode Access Voltage	V_{PP2}	V_{CCP}	V_{CCP} + 1	V
Supply Current in Programming Mode	I_{PPP}	—	100	mA
Input or Output Leakage Current	I_L	–10	10	µA
First Pass Low-level Supply Voltage for Final Verification	V_{DDL}	2.8	3.0	V
Second Pass High-level Supply Voltage for Final Verification	V_{DDH}	6.0	8.2	V

* No overshoot is permitted on this signal. V_{PP} must not be allowed to exceed 14 V.

Electrical Characteristics (continued)

Table 7. ac Programming Specifications

Commercial: 0 °C ≤ T_A ≤ 70 °C, V_{DD} = 5.0 V ± 5%; Industrial: –40 °C ≤ T_A ≤ +85 °C, V_{DD} = 5.0 V ± 10%.

Parameter	Test Conditions	Symbol	Min	Max	Unit
10% to 90% Rise Time of V_{PP}	*	T_{RPP}	1	—	µs
90% to 10% Fall Time of V_{PP}	*	T_{FPP}	1	—	µs
V_{PP} Programming Pulse Width	—	T_{PGM}	0.5	1.05	ms
V_{PP} Setup to Clock for Entering Programming Mode	*	T_{SVC}	100	—	ns
$\overline{CE}$ Setup to Clock for Entering Programming Mode	*	T_{SVCE}	100	—	ns
$\overline{OE}$ Setup to Clock for Entering Programming Mode	*	T_{SVOE}	100	—	ns
V_{PP} Hold from Clock for Entering Programming Mode	*	T_{HVC}	300	—	ns
Data Setup to Clock for Programming	—	T_{SDP}	50	—	ns
Data Hold from Clock for Programming	—	T_{HDP}	0	—	ns
$\overline{CE}$ Low Time to Clear Data Latches	—	T_{LCE}	100	—	ns
$\overline{CE}$ Setup to Clock for Programming/Verifying	—	T_{SCC}	100	—	ns
$\overline{OE}$ Setup to Clock for Incrementing Address Counter	—	T_{SIC}	100	—	ns
$\overline{OE}$ Hold from Clock for Incrementing Address Counter	—	T_{HIC}	0	—	ns
$\overline{OE}$ Hold from V_{PP}	*	T_{HOV}	200	—	ns
Clock to Data Valid	—	T_{PCAC}	—	400	ns
Data Hold from Clock	—	T_{POH}	0	—	ns
$\overline{CE}$ Low to Data Valid	—	T_{PCE}	—	250	ns

* This parameter is periodically sampled and is not 100% tested.

Note: While in programming mode, $\overline{CE}$ should only be changed while $\overline{OE}$ is HIGH and has been HIGH for 200 ns, and $\overline{OE}$ should only be changed while $\overline{CE}$ is HIGH and has been HIGH for 200 ns.

Electrical Characteristics (continued)

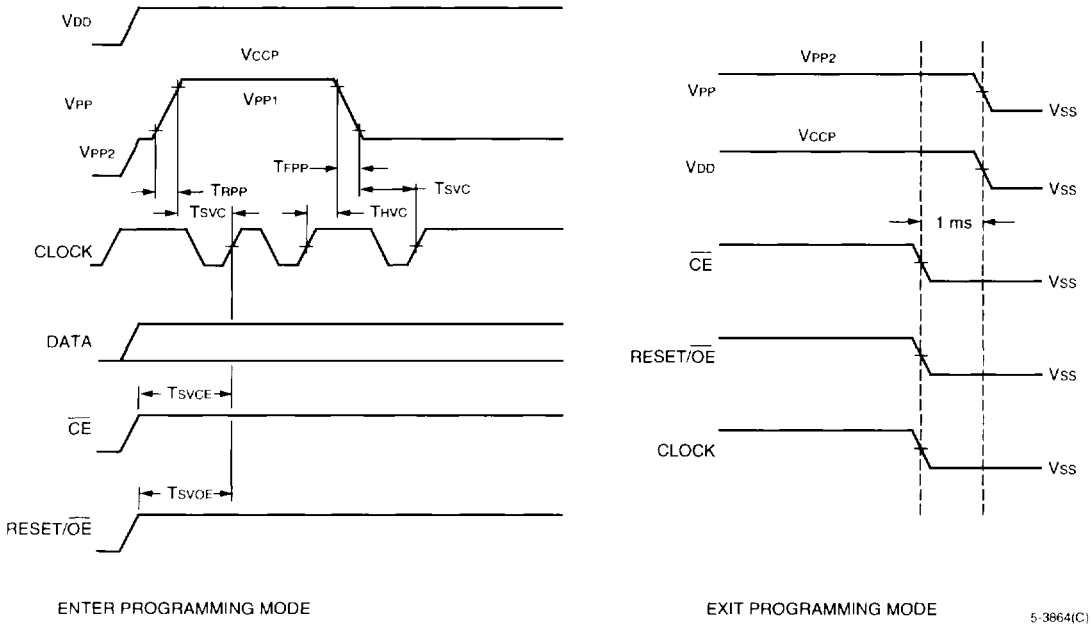
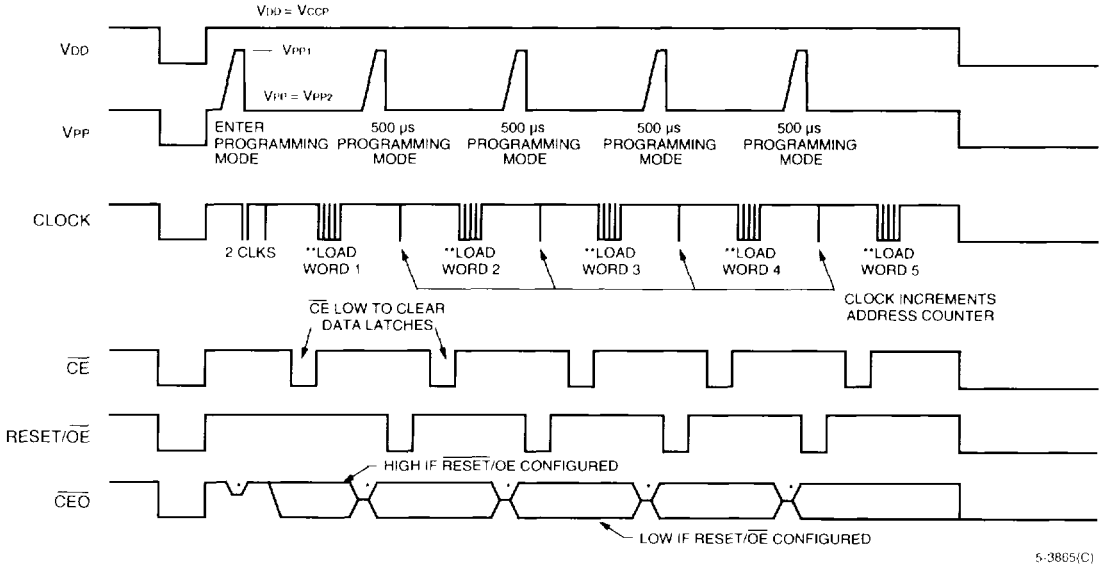


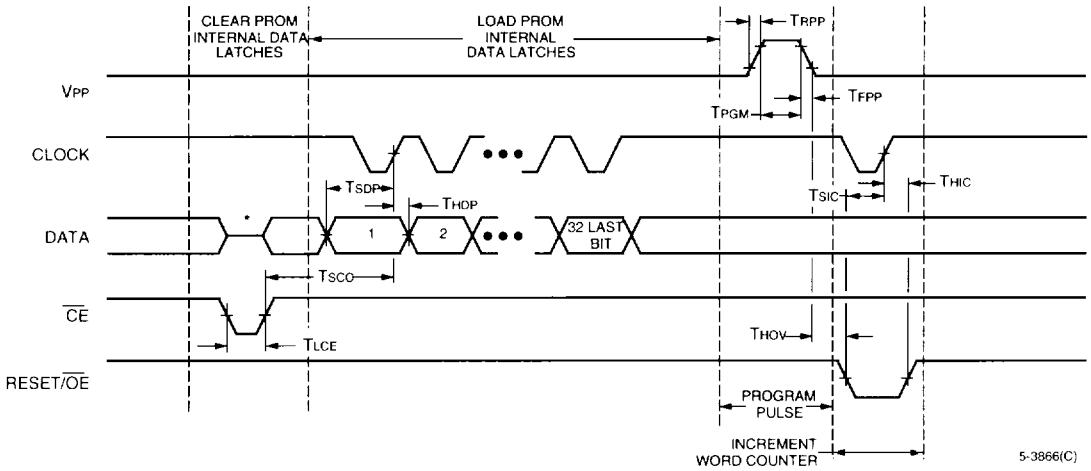
Figure 7. Entering and Exiting Programming Mode



* The CEO pin is high impedance when VPP = VPP1.
** 32 clocks.

Figure 8. Programming Cycle Overview

Electrical Characteristics (continued)



* The programmer must float the data pin while $\overline{CE}$ is low to avoid bus contention.

Figure 9. Details of Programming Cycle

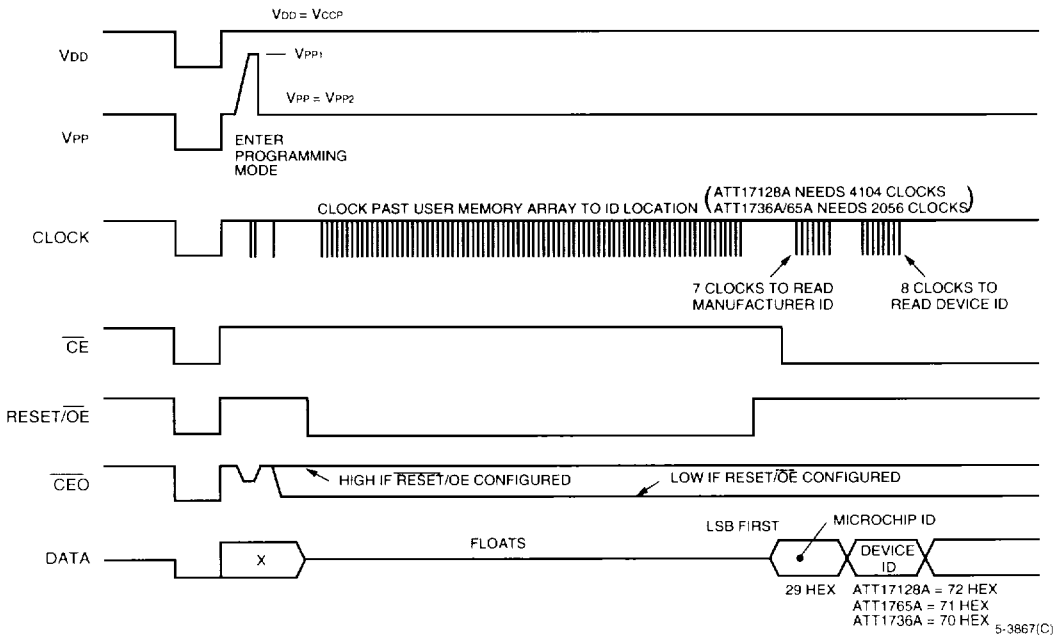


Figure 10. Read Manufacturer and Device ID Overview

Electrical Characteristics (continued)

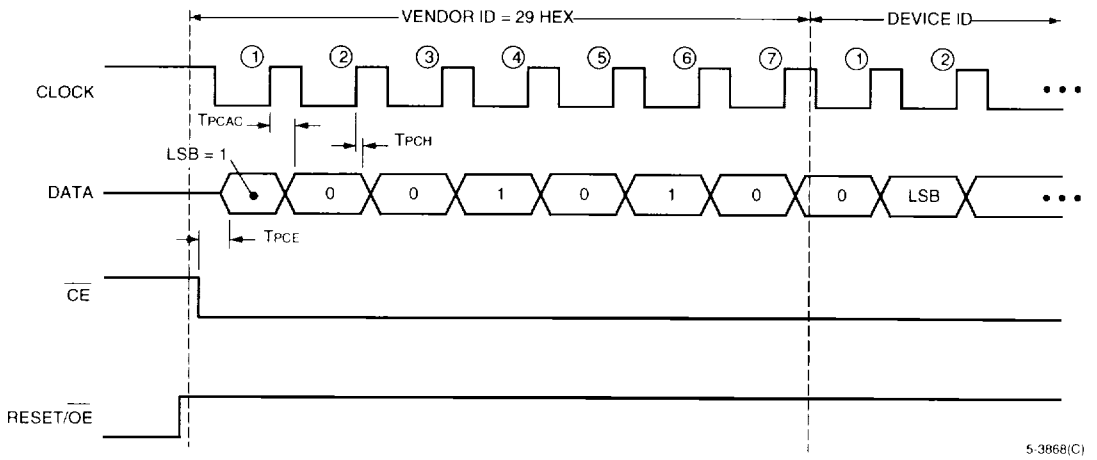
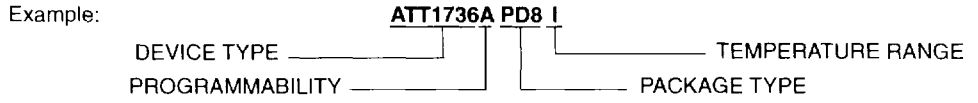


Figure 11. Details of Read Manufacturer and Device ID

Ordering Information



ATT1736A; One-Time Programmable; 8-pin, Plastic DIP; Industrial Temperature

Table 8. Device Type

Device	Size
ATT1736A	36,288
ATT1765A	65,536
ATT17128A	131,072

Table 9. Programmability

Designation	Programmability
Blank	One-Time Programmable
A	One-Time Programmable

Table 10. Package Type

Designation	Package
PD8	8-pin, plastic DIP
SO8	8-pin SOIC
M20	20-pin PLCC

Table 11. Temperature Range

Designation	Type	Operating Range
Blank	Commercial	0 °C to 70 °C
I	Industrial	–40 °C to +85 °C