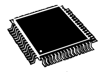
STM32L471xx

Ultra-low-power ARM® Cortex®-M4 32-bit MCU+FPU, 100DMIPS, up to 1MB Flash, 128 KB SRAM, analog, audio

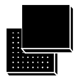
Datasheet - production data

Features

- Ultra-low-power with FlexPowerControl
  - 1.71 V to 3.6 V power supply
  - -40 °C to 85/105/125 °C temperature range
  - 300 nA in V_{BAT} mode: supply for RTC and 32x32-bit backup registers
  - 30 nA Shutdown mode (5 wakeup pins)
  - 120 nA Standby mode (5 wakeup pins)
  - 420 nA Standby mode with RTC
  - 1.1 µA Stop 2 mode, 1.4 µA Stop 2 with RTC
  - 100 µA/MHz run mode
  - Batch acquisition mode (BAM)
  - 4 µs wakeup from Stop mode
  - Brown out reset (BOR) in all modes except shutdown
  - Interconnect matrix
- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 80 MHz, MPU, 100DMIPS/1.25DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Clock Sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal 16 MHz factory-trimmed RC (±1%)
  - Internal low-power 32 kHz RC (±5%)
  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
  - 3 PLLs for system clock, audio, ADC
- RTC with HW calendar, alarms and calibration
- Up to 24 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- 16x timers: 2 x 16-bit advanced motor-control, 2 x 32-bit and 5 x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Up to 114 fast I/Os, most 5 V-tolerant, up to 14 I/Os with independent supply down to 1.08 V



LQFP144 (20 × 20)
LQFP100 (14 x 14)
LQFP64 (10 x 10)



UFBGA132
(7 × 7)

- Memories
  - Up to 1 MB Flash, 2 banks read-while-write, proprietary code readout protection
  - Up to 128 KB of SRAM including 32 KB with hardware parity check
  - External memory interface for static memories supporting SRAM, PSRAM, NOR and NAND memories
  - Quad SPI memory interface
- 4x digital filters for sigma delta modulator
- Rich analog peripherals (independent supply)
  - 3× 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 2x 12-bit DAC, low-power sample and hold
  - 2x operational amplifiers with built-in PGA
  - 2x ultra-low-power comparators
- 17x communication interfaces
  - 2x SAIs (serial audio interface)
  - 3x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 6x USARTs (ISO 7816, LIN, IrDA, modem)
  - 3x SPIs (4x SPIs with the Quad SPI)
  - CAN (2.0B Active) and SDMMC interface
  - SWPMI single wire protocol master I/F
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™

Table 1. Device summary

Reference	Part number
STM32L471xx	STM32L471RG, STM32L471VG, STM32L471QG, STM32L471ZG, STM32L471RE, STM32L471VE, STM32L471QE, STM32L471ZE

This is information on a product in full production. www.st.com

Contents

List of tables

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L471xx microcontrollers.

This document should be read in conjunction with the STM32L4x1 reference manual (RM0392). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

2 Description

The STM32L471xx devices are the ultra-low-power microcontrollers based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L471xx devices embed high-speed memories (Flash memory up to 1 Mbyte, up to 128 Kbyte of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L471xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer up to three fast 12-bit ADCs (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM).

In addition, up to 24 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces.

- Three I2Cs
- Three SPIs
- Three USARTs, two UARTs and one Low-Power UART.
- Two SAIs (Serial Audio Interfaces)
- One SDMMC
- One CAN
- One SWPMI (Single Wire Protocol Master Interface)

The STM32L471xx operates in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMPs and comparators, and up to 14 I/Os can be supplied independently down to 1.08V. A VBAT input allows to backup the RTC and backup registers.

The STM32L471xx family offers four packages from 64-pin to 144-pin packages.

Table 2. STM32L471xx family device features and peripheral counts

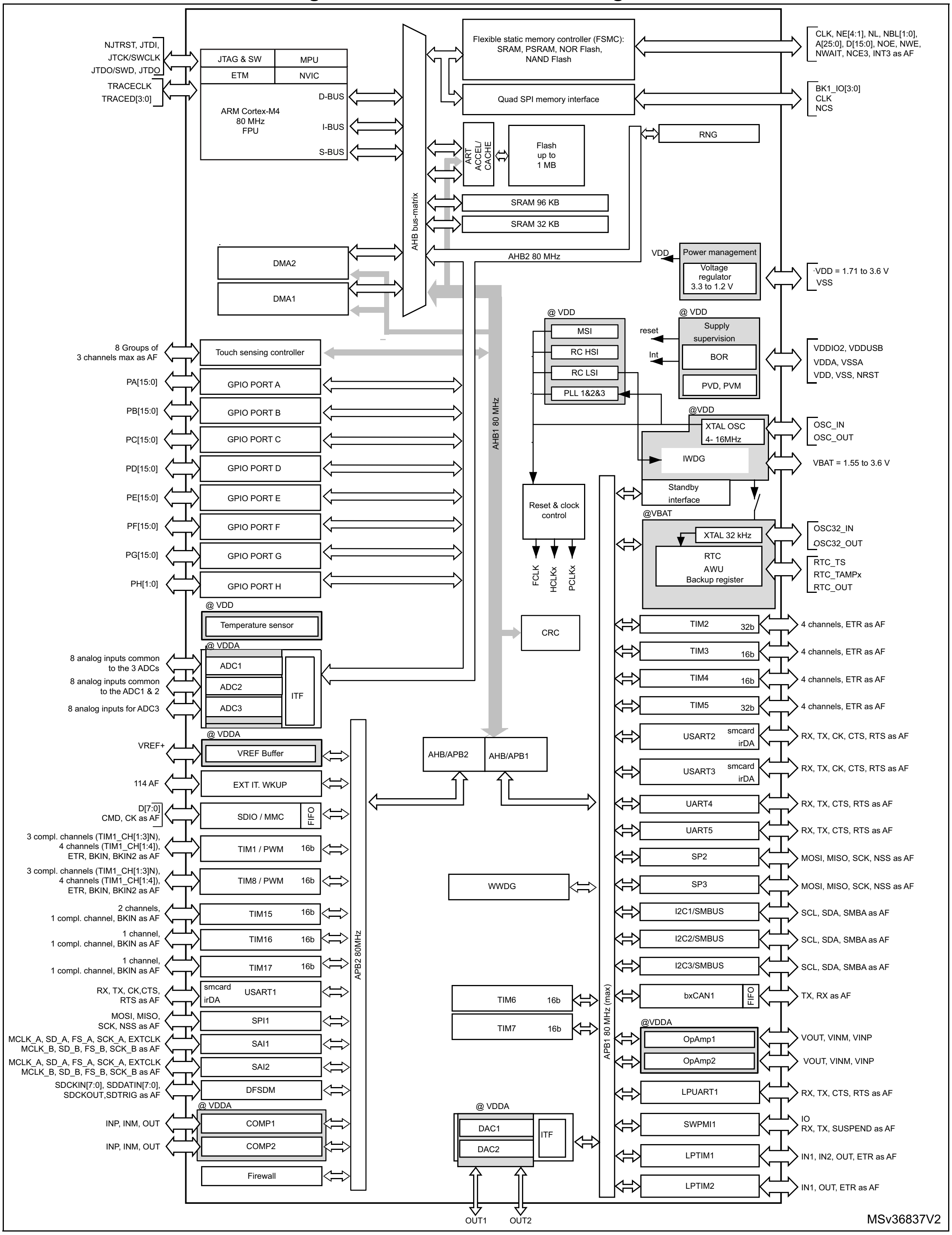
Peripheral		STM32L471Zx		STM32L471Qx		STM32L471Vx		STM32L471Rx	
Flash memory		512KB	1MB	512KB	1MB	512KB	1MB	512KB	1MB
SRAM		128KB							
External memory controller for static memories		Yes		Yes		Yes(1)		No	
Quad SPI		Yes							
Timers	Advanced control	2 (16-bit)							
	General purpose	5 (16-bit) 2 (32-bit)							
	Basic	2 (16-bit)							
	Low -power	2 (16-bit)							
	SysTick timer	1							
	Watchdog timers (independent, window)	2							
Comm. interfaces	SPI	3							
	I^2C	3							
	USART UART LPUART	3 2 1							
	SAI	2							
	CAN	1							
	SDMMC	Yes							
	SWPMI	Yes							
Digital filters for sigma-delta modulators		Yes (4 filters)							
Number of channels		8							
RTC		Yes							
Tamper pins		3 2							
Random generator		Yes							
GPIOs Wakeup pins Nb of I/Os down to 1.08 V		114 5 14		109 5 14		82 5 0		51 4 0	
Capacitive sensing Number of channels		24		24		21		12	
12-bit ADCs Number of channels		3 24		3 19		3 16		3 16	
12-bit DAC channels		2							
Internal voltage reference buffer		Yes						No	
Analog comparator		2							
Operational amplifiers		2							
Max. CPU frequency		80 MHz							
Operating voltage		1.71 to 3.6 V							

Table 2. STM32L471xx family device features and peripheral counts (continued)

Peripheral	STM32L471Zx	STM32L471Qx	STM32L471Vx	STM32L471Rx
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C			
Packages	LQFP144	UFBGA132	LQFP100	LQFP64

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.

Figure 1. STM32L471xx block diagram



Note: AF: alternate function on I/O pins.

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32L471xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32L471xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

STM32L471xx devices feature up to 1 Mbyte of embedded Flash memory available for storing programs and data. The Flash memory is divided into two banks allowing read-while-write operations. This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. One area per bank can be selected, with 64-bit granularity. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection.
- The address of the ECC fail can be read in the ECC register

3.5 Embedded SRAM

STM32L471xx devices feature up to 128 Kbyte of embedded SRAM. This SRAM is split into two blocks:

- 96 Kbyte mapped at address 0x2000 0000 (SRAM1)
- 32 Kbyte located at address 0x1000 0000 with hardware parity check (SRAM2).

  This block is accessed through the ICode/DCode buses for maximum performance. These 32 Kbyte SRAM can also be retained in Standby mode.

  The SRAM2 can be write-protected with 1 Kbyte granularity.

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Firewall

The device embeds a Firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The Firewall main features are the following:

- Three segments can be protected and defined thanks to the Firewall registers:
  - Code segment (located in Flash or SRAM1 if defined as executable protected area)
  - Non-volatile data segment (located in Flash)
  - Volatile data segment (located in SRAM1)
- The start address and the length of each segments are configurable:
  - code segment: up to 1024 Kbyte with granularity of 256 bytes
  - Non-volatile data segment: up to 1024 Kbyte with granularity of 256 bytes
  - Volatile data segment: up to 96 Kbyte with a granularity of 64 bytes
- Specific mechanism implemented to open the Firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the Firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.7 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI and CAN in Device mode through DFU (device firmware upgrade).

3.8 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.9 Power supply management

3.9.1 Power supply schemes

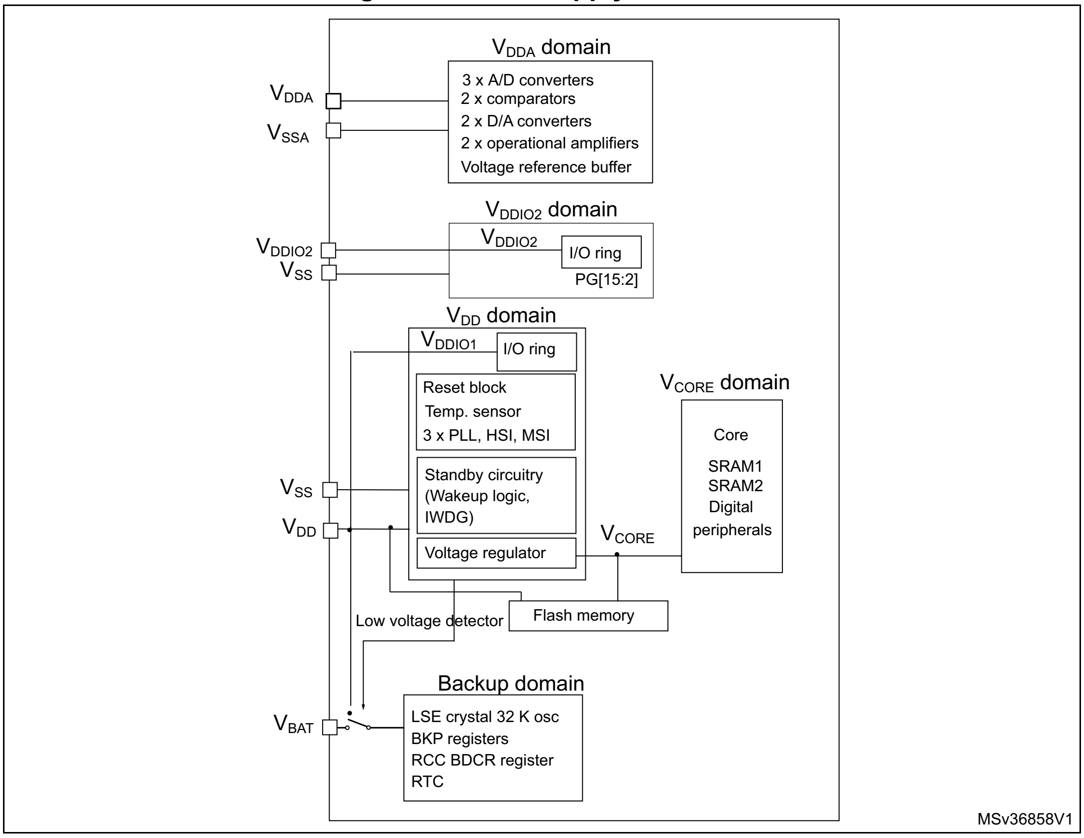
- V_{DD} = 1.71 to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through V_{DD} pins.
- V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 (DACs/OPAMPs) to 3.6 V: external analog power supply for ADCs, DACs, OPAMPs, Comparators and Voltage reference buffer. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- V_{DDIO2} = 1.08 to 3.6 V: external power supply for 14 I/Os (PG[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage.
- V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: *When the functions supplied by V_{DDA} or V_{DDIO2} are not used, these supplies should preferably be shorted to V_{DD}.*

Note: *If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant (refer to Table 19: Voltage characteristics).*

Note: *V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1} or V_{DDIO2}, with V_{DDIO1} = V_{DD}. V_{DDIO2} supply voltage level is independent from V_{DDIO1}.*

Figure 2. Power supply overview



3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embeds a Peripheral Voltage Monitor which compares the independent supply voltages V_{DDA}, V_{DDIO2} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.9.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 32 Kbyte SRAM2 in Standby with RAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L471xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The VCORE can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

3.9.4 Low-power modes

The ultra-low-power STM32L471xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources:

Table 4. STM32L471 modes overview

Mode	Regulator (1)	CPU	Flash	SRAM	Clocks	DMA & Peripherals(2)	Wakeup source	Consumption(3)	Wakeup time
Run	Range 1	Yes	ON(4)	ON	Any	All	N/A	112 µA/MHz	N/A
	Range2					All except RNG		100 µA/MHz	
LPRun	LPR	Yes	ON(4)	ON	Any except PLL	All except RNG	N/A	136 µA/MHz	to Range 1: 4 µs to Range 2: 64 µs
Sleep	Range 1	No	ON(4)	ON(5)	Any	All	Any interrupt or event	37 µA/MHz	6 cycles
	Range 2					All except RNG		35 µA/MHz	6 cycles
LPSleep	LPR	No	ON(4)	ON(5)	Any except PLL	All except RNG	Any interrupt or event	40 µA/MHz	6 cycles
Stop 0	Range 1	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC,IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)(6) LPUART1(6) I2Cx (x=1...3)(7) LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC,IWDG COMPx (x=1..2) USARTx (x=1...5)(6) LPUART1(6) I2Cx (x=1...3)(7) LPTIMx (x=1,2) SWPMI1(8)	108 µA	0.7 µs in SRAM 4.5 µs in Flash
	Range 2								

Table 4. STM32L471 modes overview (continued)

Mode	Regulator (1)	CPU	Flash	SRAM	Clocks	DMA & Peripherals(2)	Wakeup source	Consumption(3)	Wakeup time
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC,IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)(6) LPUART1(6) I2Cx (x=1...3)(7) LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC,IWDG COMPx (x=1..2) USARTx (x=1...5)(6) LPUART1(6) I2Cx (x=1...3)(7) LPTIMx (x=1,2) SWPMI1(8)	6.6 µA w/o RTC 6.9 µA w RTC	4 µs in SRAM 6 µs in Flash
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC,IWDG COMPx (x=1..2) I2C3(7) LPUART1(6) LPTIM1 *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC,IWDG COMPx (x=1..2) I2C3(7) LPUART1(6) LPTIM1	1.1 µA w/o RTC 1.4 µA w/RTC	5 µs in SRAM 7 µs in Flash

Table 4. STM32L471 modes overview (continued)

Mode	Regulator (1)	CPU	Flash	SRAM	Clocks	DMA & Peripherals(2)	Wakeup source	Consumption(3)	Wakeup time
Standby	LPR	Powered Off	Off	SRAM2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx)(9) BOR, RTC, IWDG	0.35 µA w/o RTC 0.65 µA w/ RTC	14 µs
	OFF			Powered Off				0.12 µA w/o RTC 0.42 µA w/ RTC	
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down(10)	Reset pin 5 I/Os (WKUPx)(9) RTC	0.03 µA w/o RTC 0.33 µA w/ RTC	256 µs

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. Typical current at V_{DD} = 1.8 V, 25°C. Consumptions values provided running from SRAM, Flash memory Off, 80 MHz in Range 1, 26 MHz in Range 2, 2 MHz in LPRun/LPSleep.
4. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
5. The SRAM1 and SRAM2 clocks can be gated on or off independently.
6. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. SWPMI1 wakeup by resume from suspend.
9. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
10. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

By default, the microcontroller is in Run mode after a system or a power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.
- **Low-power sleep** mode

  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode.
- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode to detect their wakeup condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop1 or Stop2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.
- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The brown-out reset (BOR) always remains active in Standby mode.

  The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be retained in

Standby mode, supplied by the low-power Regulator (Standby with RAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

Table 5. Functionalities depending on the working mode[(1)]

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (up to 1 MB)	O[(2)]	O[(2)]	O[(2)]	O[(2)]	-	-	-	-	-	-	-	-	-
SRAM1 (up to 96 KB)	Y	Y[(3)]	Y	Y[(3)]	Y	-	Y	-	-	-	-	-	-
SRAM2 (32 KB)	Y	Y[(3)]	Y	Y[(3)]	Y	-	Y	-	O[(4)]	-	-	-	-
FSMC	O	O	O	O	-	-	-	-	-	-	-	-	-
Quad SPI	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup Registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brown-out reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral Voltage Monitor (PVMx; x=1,2,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
High Speed Internal (HSI16)	O	O	O	O	[(5)]	-	[(5)]	-	-	-	-	-	-
High Speed External (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low Speed Internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low Speed External (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi-Speed Internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock Security System (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock Security System on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	3	3	3	3	3	O	3	O	3	O	3	O	3

Table 5. Functionalities depending on the working mode[1] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
USARTx (x=1,2,3,4,5)	O	O	O	O	O(6)	O(6)	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O(6)	O(6)	O(6)	O(6)	-	-	-	-	-
I2Cx (x=1,2)	O	O	O	O	O(7)	O(7)	-	-	-	-	-	-	-
I2C3	O	O	O	O	O(7)	O(7)	O(7)	O(7)	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
CAN	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SWPMI1	O	O	O	O	-	O	-	-	-	-	-	-	-
SAIx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DFSDM	O	O	O	O	-	-	-	-	-	-	-	-	-
ADCx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
DACx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O(8)	O(8)	-	-	-	-	-	-	-	-	-	-	-

Table 5. Functionalities depending on the working mode[(1)] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

3.10 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, low-power run and sleep, Stop 0, Stop 1 and Stop 2 modes.

Table 6. STM32L471xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADCx DACx DFSDM	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
COMPx	TIM1, 8 TIM2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y (1)
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y (1)
All clocks sources (internal and external)	TIM2 TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD DFSDM (analog watchdog, short circuit detection)	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-	-

Table 6. STM32L471xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y (1)
	ADCx DACx DFSDM	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

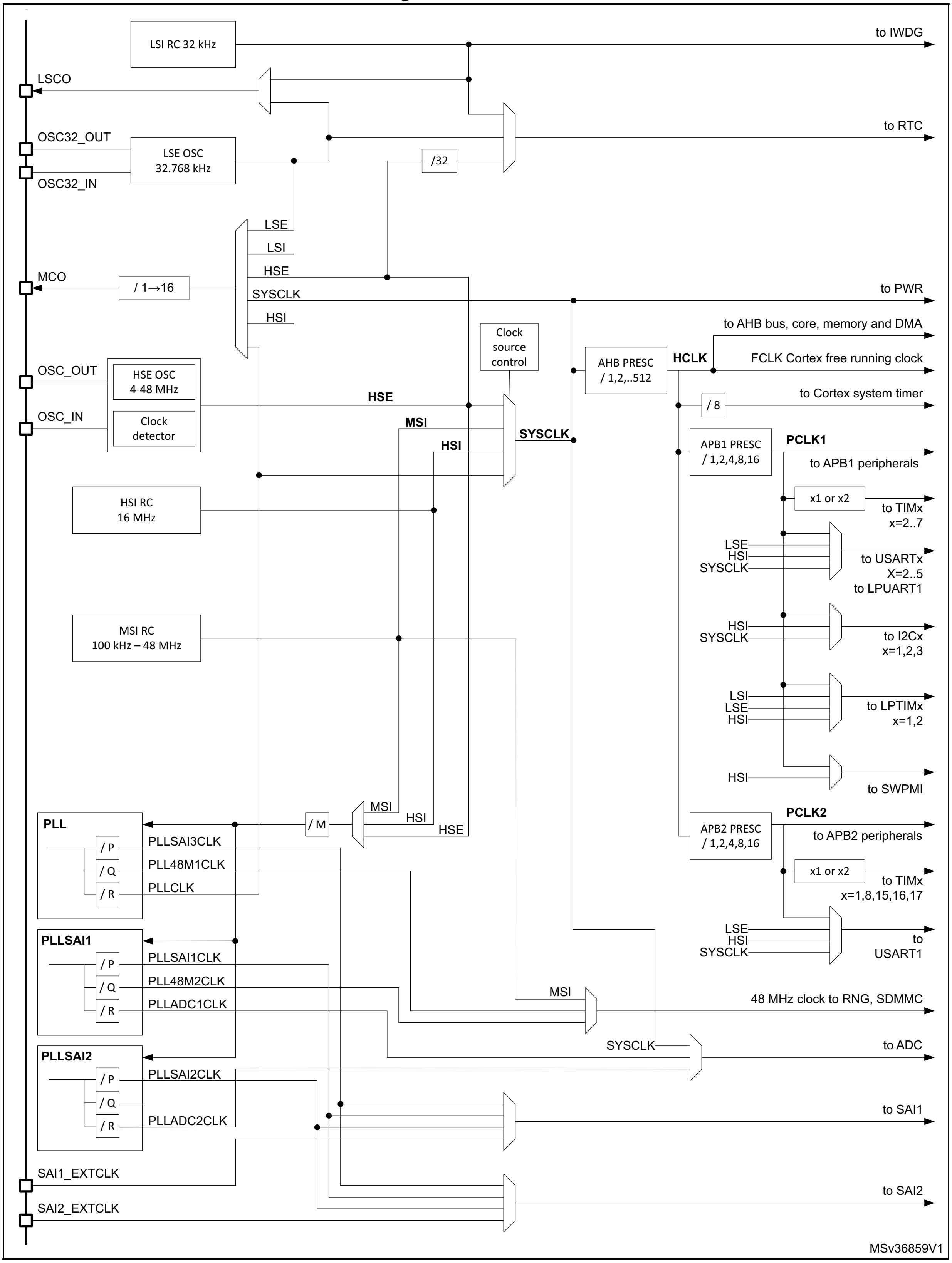
3.11 Clocks and startup

The clock controller (see *Figure 3*) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4-48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 80 MHz.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** Several peripherals (SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC, SWPMI) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the SDMMC/RNG and the two SAIs.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.
- Clock-out capability:
  - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes (except VBAT).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 80 MHz.

Figure 3. Clock tree



3.12 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.13 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 7: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each dedicated to managing memory access requests from one or more peripherals. Each has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
- Each channel is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA Half Transfer, DMA Transfer complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 7. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

3.14 Interrupts and events

3.14.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.14.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 36 edge detector lines used to generate interrupt/event requests and wake-up the system from Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

3.15 Analog to digital converter (ADC)

The device embeds 3 successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 24 external channels, some of them shared between ADC1 and ADC2, or ADC1, ADC2 and ADC3.
- 5 Internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs.
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Handles two ADC converters for dual mode operation (simultaneous or interleaved sampling modes)
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into 3 data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.15.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 and ADC3_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 8. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.15.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and Comparators. VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 9. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.15.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN18 or ADC3_IN18. As the V_{BAT} voltage may be higher than VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third the V_{BAT} voltage.

3.16 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability

- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.17 Voltage reference buffer (VREFBUF)

The STM32L471xx devices embed an voltage reference buffer which can be used as voltage reference for ADCs, DACs and also as voltage reference for external components through the VREF+ pin.

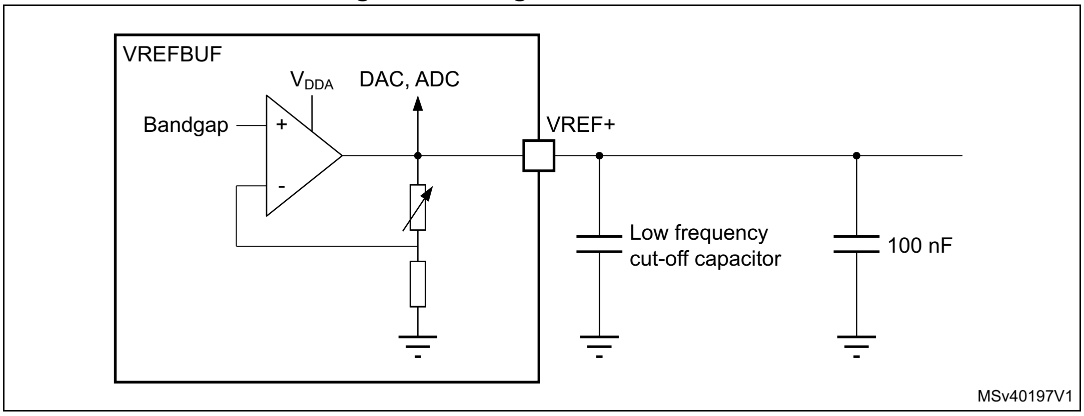
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V.

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 4. Voltage reference buffer



3.18 Comparators (COMP)

The STM32L471xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.19 Operational amplifier (OPAMP)

The STM32L471xx embeds two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.20 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 24 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.21 Digital filter for Sigma-Delta Modulators (DFSDM)

The device embeds one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0..20 MHz
- alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: device memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM0)
- analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion
- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1..256 consecutive 0’s or 1’s on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- “regular” or “injected” conversions:
  - “regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions
  - “injected” conversions for precise timing and with high conversion priority

3.22 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.23 Timers and watchdogs

The STM32L471 includes two advanced control timers, up to nine general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 10. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.23.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.23.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.23.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the STM32L471 (see *Table 10* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:
  - TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler
  - TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.
- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.
  - TIM15 has 2 channels and 1 complementary channel
  - TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.23.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.23.4 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.23.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.23.6 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.23.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.24 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.25 Inter-integrated circuit interface (I2C)

The device embeds 3 I2C. Refer to *Table 11: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 3: Clock tree*.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 11. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3
Standard-mode (up to 100 kbit/s)	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Programmable analog and digital noise filters	X	X	X
SMBus/PMBus hardware support	X	X	X
Independent clock	X	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X

1. X: supported

3.26 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L471xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, UART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2 and USART3 also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode.The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 12. STM32L4x1 USART/UART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	-	-	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver Enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

1. X = supported.

3.27 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.28 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to 40 Mbits/s in master and up to 24 Mbits/s slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation.

All SPI interfaces can be served by the DMA controller.

3.29 Serial audio interfaces (SAI)

The device embeds 2 SAI. Refer to *Table 13: SAI implementation* for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection.
  - Anticipated frame synchronization signal detection in slave mode.
  - Late frame synchronization signal detection in slave mode.
  - Codec not ready for the AC’97 mode in reception.
- Interruption sources when enabled:
  - Errors.
  - FIFO requests.
- DMA interface with 2 dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 13. SAI implementation

SAI features[1]	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO Size	X (8 Word)	X (8 Word)
SPDIF	X	X

1. X: supported

3.30 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.31 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s

- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - 14 Scalable filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

3.32 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The card host interface (SDMMC) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

3.33 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbyte of data
- 8-,16- bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- The Maximum FMC_CLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.34 Quad SPI memory interface (QUADSPI)

The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external flash is memory mapped and is seen by the system as if it were an internal memory

The Quad SPI interface supports:

- Three functional modes: indirect, status-polling, and memory-mapped
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.35 Development support

3.35.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

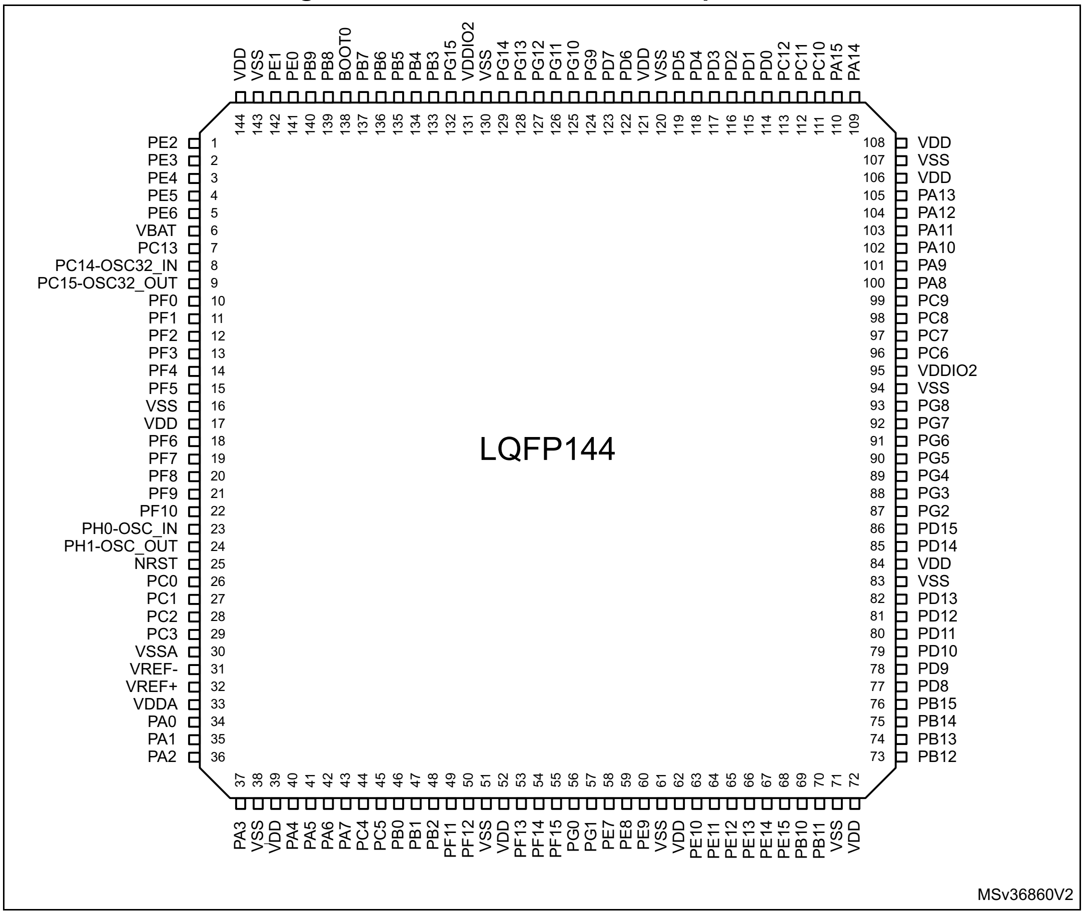
3.35.2 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L471xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

4 Pinouts and pin description

Figure 5. STM32L471Zx LQFP144 pinout(1)



1. The above figure shows the package top view.

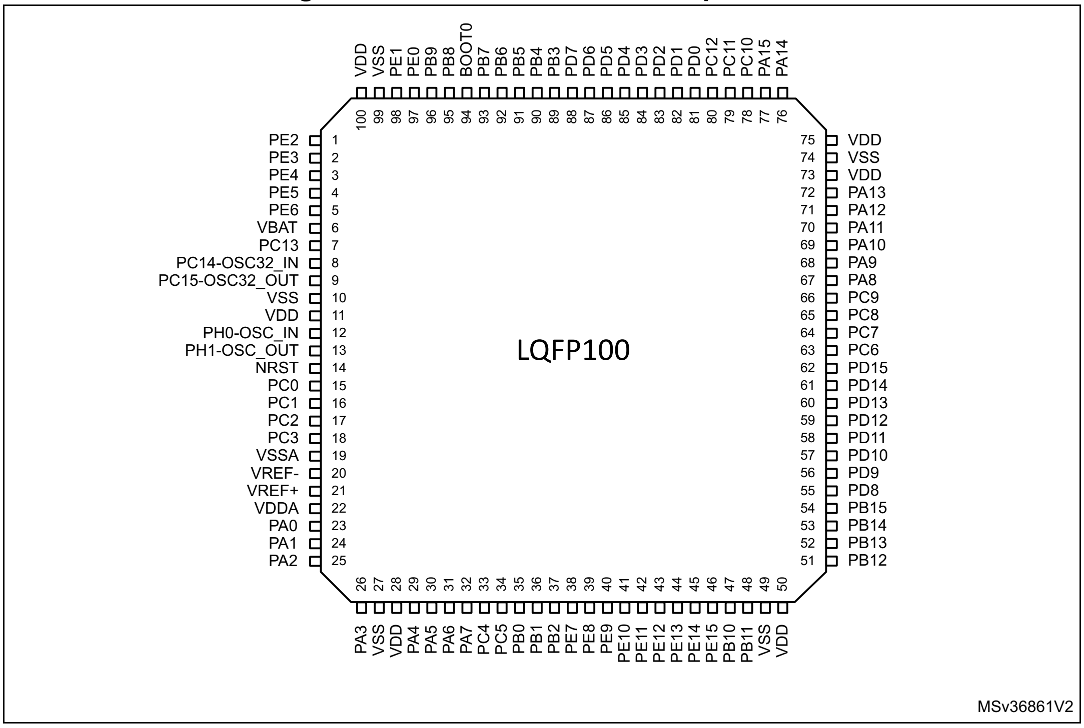
Figure 6. STM32L471Qx UFBGA132 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5	PG14	PG13	PD2	PD0	PC11	VDD	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSS		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO2		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	PB11	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

MSv36862V6

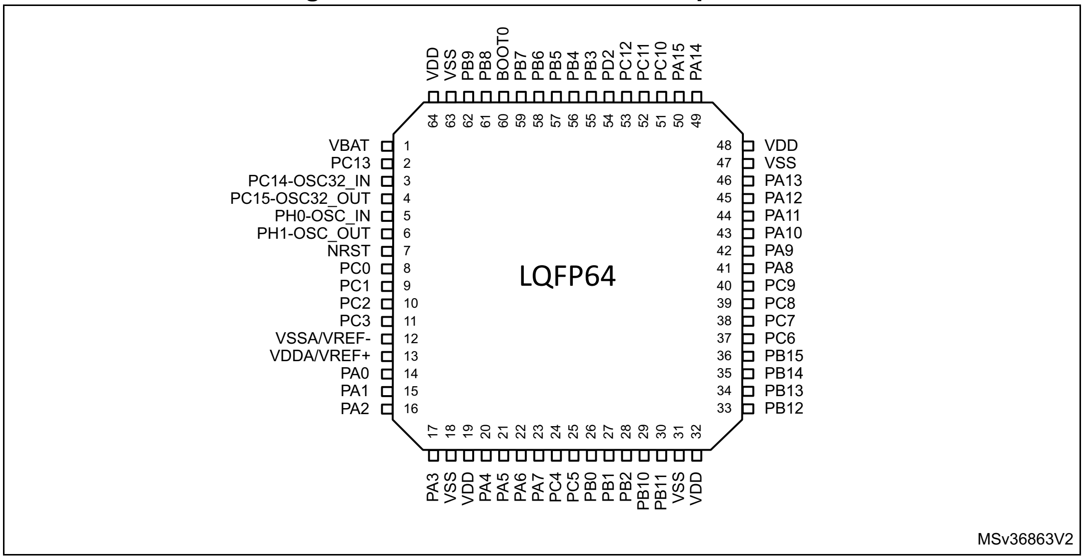
1. The above figure shows the package top view.

Figure 7. STM32L471Vx LQFP100 pinout(1)



1. The above figure shows the package top view.

Figure 8. STM32L471Rx LQFP64 pinout[1]



1. The above figure shows the package top view.

Table 14. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os	
		_f [1]	I/O, Fm+ capable
		_a [2]	I/O, with Analog switch function supplied by V_{DDA}
		_s [3]	I/O supplied only by V_{DDIO2}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 15* are: FT_f, FT_fa.
2. The related I/O structures in *Table 15* are: FT_a, FT_fa, TT_a.
3. The related I/O structures in *Table 15* are: FT_s, FT_fs.

Table 15. STM32L471xx pin definitions

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	1	B2	1	PE2	I/O	FT	-	TRACECK, TIM3_ETR, TSC_G7_IO1, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
-	2	A1	2	PE3	I/O	FT	-	TRACED0, TIM3_CH1, TSC_G7_IO2, FMC_A19, SAI1_SD_B, EVENTOUT	-
-	3	B1	3	PE4	I/O	FT	-	TRACED1, TIM3_CH2, DFSDM_DATIN3, TSC_G7_IO3, FMC_A20, SAI1_FS_A, EVENTOUT	-
-	4	C2	4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, DFSDM_CKIN3, TSC_G7_IO4, FMC_A21, SAI1_SCK_A, EVENTOUT	-
-	5	D2	5	PE6	I/O	FT	-	TRACED3, TIM3_CH4, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_TAMP3/ WKUP3
1	6	E2	6	VBAT	S	-	-	-	-
2	7	C1	7	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1/ RTC_TS/ RTC_OUT/ WKUP2
3	8	D1	8	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
4	9	E1	9	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	-	D6	10	PF0	I/O	FT_f	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	D5	11	PF1	I/O	FT_f	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	D4	12	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	E4	13	PF3	I/O	FT_a	-	FMC_A3, EVENTOUT	ADC3_IN6
-	-	F3	14	PF4	I/O	FT_a	-	FMC_A4, EVENTOUT	ADC3_IN7
-	-	F4	15	PF5	I/O	FT_a	-	FMC_A5, EVENTOUT	ADC3_IN8
-	10	F2	16	VSS	S	-	-	-	-
-	11	G2	17	VDD	S	-	-	-	-

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	-	18	PF6	I/O	FT_a	-	TIM5_ETR, TIM5_CH1, SAI1_SD_B, EVENTOUT	ADC3_IN9
-	-	-	19	PF7	I/O	FT_a	-	TIM5_CH2, SAI1_MCLK_B, EVENTOUT	ADC3_IN10
-	-	-	20	PF8	I/O	FT_a	-	TIM5_CH3, SAI1_SCK_B, EVENTOUT	ADC3_IN11
-	-	-	21	PF9	I/O	FT_a	-	TIM5_CH4, SAI1_FS_B, TIM15_CH1, EVENTOUT	ADC3_IN12
-	-	-	22	PF10	I/O	FT_a	-	TIM15_CH2, EVENTOUT	ADC3_IN13
5	12	F1	23	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	13	G1	24	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	14	H2	25	NRST	I/O	RST	-	-	-
8	15	H1	26	PC0	I/O	FT_fa	-	LPTIM1_IN1, I2C3_SCL, DFSDM_DATIN4, LPUART1_RX, LPTIM2_IN1, EVENTOUT	ADC123_IN1
9	16	J2	27	PC1	I/O	FT_fa	-	LPTIM1_OUT, I2C3_SDA, DFSDM_CKIN4, LPUART1_TX, EVENTOUT	ADC123_IN2
10	17	J3	28	PC2	I/O	FT_a	-	LPTIM1_IN2, SPI2_MISO, DFSDM_CKOUT, EVENTOUT	ADC123_IN3
11	18	K2	29	PC3	I/O	FT_a	-	LPTIM1_ETR, SPI2_MOSI, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC123_IN4
-	19	-	30	VSSA	S	-	-	-	-
-	20	-	31	VREF-	S	-	-	-	-
12	-	J1	-	VSSA/VREF-	-	-	-	-	-
-	21	L1	32	VREF+	S	-	-	-	VREFBUF_OUT
-	22	M1	33	VDDA	S	-	-	-	-
13	-	-	-	VDDA/VREF+	S	-	-	-	-

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
14	23	L2	34	PA0	I/O	FT_a	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, ADC12_IN5, RTC_TAMP2/WKUP1
-	-	M3	-	OPAMP1_VINM	I	TT	-	-	-
15	24	M2	35	PA1	I/O	FT_a	-	TIM2_CH2, TIM5_CH2, USART2_RTS_DE, UART4_RX, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, ADC12_IN6
16	25	K3	36	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, USART2_TX, SAI2_EXTCLK, TIM15_CH1, EVENTOUT	ADC12_IN7, WKUP4/LSCO
17	26	L3	37	PA3	I/O	TT	-	TIM2_CH4, TIM5_CH4, USART2_RX, TIM15_CH2, EVENTOUT	OPAMP1_ VOUT, ADC12_IN8
18	27	E3	38	VSS	S	-	-	-	-
19	28	H3	39	VDD	S	-	-	-	-
20	29	J4	40	PA4	I/O	TT_a	-	SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	ADC12_IN9, DAC1_OUT1
21	30	K4	41	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, TIM8_CH1N, SPI1_SCK, LPTIM2_ETR, EVENTOUT	ADC12_IN10, DAC1_OUT2
22	31	L4	42	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, USART3_CTS, QUADSPI_BK1_IO3, TIM1_BKIN_COMP2, TIM8_BKIN_COMP2, TIM16_CH1, EVENTOUT	OPAMP2_VINP, ADC12_IN11
-	-	M4	-	OPAMP2_VINM	I	TT	-	-	-
23	32	J5	43	PA7	I/O	FT_a	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, QUADSPI_BK1_IO2, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC12_IN12
24	33	K5	44	PC4	I/O	FT_a	-	USART3_TX, EVENTOUT	COMP1_INM, ADC12_IN13

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
25	34	L5	45	PC5	I/O	FT_a	-	USART3_RX, EVENTOUT	COMP1_INP, ADC12_IN14, WKUP5
26	35	M5	46	PB0	I/O	TT_a	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, USART3_CK, QUADSPI_BK1_IO1, COMP1_OUT, EVENTOUT	OPAMP2_ VOUT, ADC12_IN15
27	36	M6	47	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM_DATIN0, USART3_RTS_DE, QUADSPI_BK1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC12_IN16
28	37	L6	48	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM_CKIN0, EVENTOUT	COMP1_INP
-	-	K6	49	PF11	I/O	FT	-	EVENTOUT	-
-	-	J7	50	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	-	51	VSS	S	-	-	-	-
-	-	-	52	VDD	S	-	-	-	-
-	-	K7	53	PF13	I/O	FT	-	DFSDM_DATIN6, FMC_A7, EVENTOUT	-
-	-	J8	54	PF14	I/O	FT	-	DFSDM_CKIN6, TSC_G8_IO1, FMC_A8, EVENTOUT	-
-	-	J9	55	PF15	I/O	FT	-	TSC_G8_IO2, FMC_A9, EVENTOUT	-
-	-	H9	56	PG0	I/O	FT	-	TSC_G8_IO3, FMC_A10, EVENTOUT	-
-	-	G9	57	PG1	I/O	FT	-	TSC_G8_IO4, FMC_A11, EVENTOUT	-
-	38	M7	58	PE7	I/O	FT	-	TIM1_ETR, DFSDM_DATIN2, FMC_D4, SAI1_SD_B, EVENTOUT	-
-	39	L7	59	PE8	I/O	FT	-	TIM1_CH1N, DFSDM_CKIN2, FMC_D5, SAI1_SCK_B, EVENTOUT	-

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	40	M8	60	PE9	I/O	FT	-	TIM1_CH1, DFSDM_CKOUT, FMC_D6, SAI1_FS_B, EVENTOUT	-
-	-	F6	61	VSS	S	-	-	-	-
-	-	G6	62	VDD	S	-	-	-	-
-	41	L8	63	PE10	I/O	FT	-	TIM1_CH2N, DFSDM_DATIN4, TSC_G5_IO1, QUADSPI_CLK, FMC_D7, SAI1_MCLK_B, EVENTOUT	-
-	42	M9	64	PE11	I/O	FT	-	TIM1_CH2, DFSDM_CKIN4, TSC_G5_IO2, QUADSPI_NCS, FMC_D8, EVENTOUT	-
-	43	L9	65	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM_DATIN5, TSC_G5_IO3, QUADSPI_BK1_IO0, FMC_D9, EVENTOUT	-
-	44	M10	66	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM_CKIN5, TSC_G5_IO4, QUADSPI_BK1_IO1, FMC_D10, EVENTOUT	-
-	45	M11	67	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, FMC_D11, EVENTOUT	-
-	46	M12	68	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, FMC_D12, EVENTOUT	-

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
29	47	L10	69	PB10	I/O	FT_f	-	TIM2_CH3, I2C2_SCL, SPI2_SCK, DFSDM_DATIN7, USART3_TX, LPUART1_RX, QUADSPI_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
30	48	L11	70	PB11	I/O	FT_f	-	TIM2_CH4, I2C2_SDA, DFSDM_CKIN7, USART3_RX, LPUART1_TX, QUADSPI_NCS, COMP2_OUT, EVENTOUT	-
31	49	F12	71	VSS	S	-	-	-	-
32	50	G12	72	VDD	S	-	-	-	-
33	51	L12	73	PB12	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP2, I2C2_SMBA, SPI2_NSS, DFSDM_DATIN1, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, SWPMI1_IO, SAI2_FS_A, TIM15_BKIN, EVENTOUT	-
34	52	K12	74	PB13	I/O	FT_f	-	TIM1_CH1N, I2C2_SCL, SPI2_SCK, DFSDM_CKIN1, USART3_CTS, LPUART1_CTS, TSC_G1_IO2, SWPMI1_TX, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
35	53	K11	75	PB14	I/O	FT_f	-	TIM1_CH2N, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM_DATIN2, USART3_RTS_DE, TSC_G1_IO3, SWPMI1_RX, SAI2_MCLK_A, TIM15_CH1, EVENTOUT	-

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
36	54	K10	76	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM_CKIN2, TSC_G1_IO4, SWPMI1_SUSPEND, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	55	K9	77	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
-	56	K8	78	PD9	I/O	FT	-	USART3_RX, FMC_D14, SAI2_MCLK_A, EVENTOUT	-
-	57	J12	79	PD10	I/O	FT	-	USART3_CK, TSC_G6_IO1, FMC_D15, SAI2_SCK_A, EVENTOUT	-
-	58	J11	80	PD11	I/O	FT	-	USART3_CTS, TSC_G6_IO2, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	-
-	59	J10	81	PD12	I/O	FT	-	TIM4_CH1, USART3_RTS_DE, TSC_G6_IO3, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	-
-	60	H12	82	PD13	I/O	FT	-	TIM4_CH2, TSC_G6_IO4, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	-	-	83	VSS	S	-	-	-	-
-	-	-	84	VDD	S	-	-	-	-
-	61	H11	85	PD14	I/O	FT	-	TIM4_CH3, FMC_D0, EVENTOUT	-
-	62	H10	86	PD15	I/O	FT	-	TIM4_CH4, FMC_D1, EVENTOUT	-
-	-	G10	87	PG2	I/O	FT_s	-	SPI1_SCK, FMC_A12, SAI2_SCK_B, EVENTOUT	-
-	-	F9	88	PG3	I/O	FT_s	-	SPI1_MISO, FMC_A13, SAI2_FS_B, EVENTOUT	-
-	-	F10	89	PG4	I/O	FT_s	-	SPI1_MOSI, FMC_A14, SAI2_MCLK_B, EVENTOUT	-

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	E9	90	PG5	I/O	FT_s	-	SPI1_NSS, LPUART1_CTS, FMC_A15, SAI2_SD_B, EVENTOUT	-
-	-	G4	91	PG6	I/O	FT_s	-	I2C3_SMBA, LPUART1_RTS_DE, EVENTOUT	-
-	-	H4	92	PG7	I/O	FT_fs	-	I2C3_SCL, LPUART1_TX, FMC_INT3, EVENTOUT	-
-	-	J6	93	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	94	VSS	S	-	-	-	-
-	-	-	95	VDDIO2	S	-	-	-	-
37	63	E12	96	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, DFSDM_CKIN3, TSC_G4_IO1, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-
38	64	E11	97	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, DFSDM_DATIN3, TSC_G4_IO2, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT	-
39	65	E10	98	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, TSC_G4_IO3, SDMMC1_D0, EVENTOUT	-
40	66	D12	99	PC9	I/O	FT	-	TIM8_BKIN2, TIM3_CH4, TIM8_CH4, TSC_G4_IO4, SDMMC1_D1, SAI2_EXTCLK, TIM8_BKIN2_COMP1, EVENTOUT	-
41	67	D11	100	PA8	I/O	FT	-	MCO, TIM1_CH1, USART1_CK, LPTIM2_OUT, EVENTOUT	-
42	68	D10	101	PA9	I/O	FT	-	TIM1_CH2, USART1_TX, TIM15_BKIN, EVENTOUT	
43	69	C12	102	PA10	I/O	FT	-	TIM1_CH3, USART1_RX TIM17_BKIN, EVENTOUT	-

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
44	70	B12	103	PA11	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, USART1_CTS, CAN1_RX, TIM1_BKIN2_COMP1, EVENTOUT	-
45	71	A12	104	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS_DE, CAN1_TX, EVENTOUT	-
46	72	A11	105	PA13 (JTMS-SWDIO)	I/O	FT	(3)	JTMS-SWDIO, IR_OUT, EVENTOUT	-
47	-	-	-	VSS	S	-	-	-	-
48	73	C11	106	VDD	S	-	-	-	-
-	74	F11	107	VSS	S	-	-	-	-
-	75	G11	108	VDD	S	-	-	-	-
49	76	A10	109	PA14 (JTCK-SWCLK)	I/O	FT	(3)	JTCK-SWCLK, EVENTOUT	-
50	77	A9	110	PA15 (JTDI)	I/O	FT	(3)	JTDI, TIM2_CH1, TIM2_ETR, SPI1_NSS, SPI3_NSS, UART4_RTS_DE, TSC_G3_IO1, SAI2_FS_B, EVENTOUT	-
51	78	B11	111	PC10	I/O	FT	-	SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, SDMMC1_D2, SAI2_SCK_B, EVENTOUT	-
52	79	C10	112	PC11	I/O	FT	-	SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT	-
53	80	B10	113	PC12	I/O	FT	-	SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, SDMMC1_CK, SAI2_SD_B, EVENTOUT	-
-	81	C9	114	PD0	I/O	FT	-	SPI2_NSS, DFSDM_DATIN7, CAN1_RX, FMC_D2, EVENTOUT	-

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	82	B9	115	PD1	I/O	FT	-	SPI2_SCK, DFSDM_CKIN7, CAN1_TX, FMC_D3, EVENTOUT	-
54	83	C8	116	PD2	I/O	FT	-	TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, SDMMC1_CMD, EVENTOUT	-
-	84	B8	117	PD3	I/O	FT	-	SPI2_MISO, DFSDM_DATIN0, USART2_CTS, FMC_CLK, EVENTOUT	-
-	85	B7	118	PD4	I/O	FT	-	SPI2_MOSI, DFSDM_CKIN0, USART2_RTS_DE, FMC_NOE, EVENTOUT	-
-	86	A6	119	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	-	-	120	VSS	S	-	-	-	-
-	-	-	121	VDD	S	-	-	-	-
-	87	B6	122	PD6	I/O	FT	-	DFSDM_DATIN1, USART2_RX, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
-	88	A5	123	PD7	I/O	FT	-	DFSDM_CKIN1, USART2_CK, FMC_NE1, EVENTOUT	-
-	-	D9	124	PG9	I/O	FT_s	-	SPI3_SCK, USART1_TX, FMC_NCE3/FMC_NE2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
-	-	D8	125	PG10	I/O	FT_s	-	LPTIM1_IN1, SPI3_MISO, USART1_RX, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-
-	-	G3	126	PG11	I/O	FT_s	-	LPTIM1_IN2, SPI3_MOSI, USART1_CTS, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	D7	127	PG12	I/O	FT_s	-	LPTIM1_ETR, SPI3_NSS, USART1_RTS_DE, FMC_NE4, SAI2_SD_A, EVENTOUT	-
-	-	C7	128	PG13	I/O	FT_fs	-	I2C1_SDA, USART1_CK, FMC_A24, EVENTOUT	-
-	-	C6	129	PG14	I/O	FT_fs	-	I2C1_SCL, FMC_A25, EVENTOUT	-
-	-	F7	130	VSS	S	-	-	-	-
-	-	G7	131	VDDIO2	S	-	-	-	-
-	-	K1	132	PG15	I/O	FT_s	-	LPTIM1_OUT, I2C1_SMBA, EVENTOUT	-
55	89	A8	133	PB3 (JTDO-TRACESWO)	I/O	FT_a	(3)	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, SAI1_SCK_B, EVENTOUT	COMP2_INM
56	90	A7	134	PB4 (NJTRST)	I/O	FT_a	(3)	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, USART1_CTS, UART5_RTS_DE, TSC_G2_IO1, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT	COMP2_INP
57	91	C5	135	PB5	I/O	FT_a	-	LPTIM1_IN1, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, UART5_CTS, TSC_G2_IO2, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	-
58	92	B5	136	PB6	I/O	FT_fa	-	LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL, DFSDM_DATIN5, USART1_TX, TSC_G2_IO3, TIM8_BKIN2_COMP2, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP

Table 15. STM32L471xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
59	93	B4	137	PB7	I/O	FT_fa	-	LPTIM1_IN2, TIM4_CH2, TIM8_BKIN, I2C1_SDA, DFSDM_CKIN5, USART1_RX, UART4_CTS, TSC_G2_IO4, FMC_NL, TIM8_BKIN_COMP1, TIM17_CH1N, EVENTOUT	COMP2_INM, PVD_IN
60	94	A4	138	BOOT0	I	-	-	-	-
61	95	A3	139	PB8	I/O	FT_f	-	TIM4_CH3, I2C1_SCL, DFSDM_DATIN6, CAN1_RX, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	-
62	96	B3	140	PB9	I/O	FT_f	-	IR_OUT, TIM4_CH4, I2C1_SDA, SPI2_NSS, DFSDM_CKIN6, CAN1_TX, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT	-
-	97	C3	141	PE0	I/O	FT	-	TIM4_ETR, FMC_NBL0, TIM16_CH1, EVENTOUT	-
-	98	A2	142	PE1	I/O	FT	-	FMC_NBL1, TIM17_CH1, EVENTOUT	-
63	99	D3	143	VSS	S	-	-	-	-
64	100	C4	144	VDD	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF
 - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0392 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see Table 17)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	USART3_CTS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	-	-	-	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	-	-	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS_ DE
	PA13	JTMS-SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	-	SPI1_NSS	SPI3_NSS	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM_DATIN0	USART3_RTS_ DE
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM_CKIN0	-
	PB3	JTDO- TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_ DE
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	USART1_CTS
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	-	DFSDM_DATIN5	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	-	DFSDM_CKIN5	USART1_RX
	PB8	-	-	TIM4_CH3	-	I2C1_SCL	-	DFSDM_DATIN6	-
	PB9	-	IR_OUT	TIM4_CH4	-	I2C1_SDA	SPI2_NSS	DFSDM_CKIN6	-
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK	DFSDM_DATIN7	USART3_TX
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	DFSDM_CKIN7	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN_ COMP2	I2C2_SMBA	SPI2_NSS	DFSDM_DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM_CKIN1	USART3_CTS
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2C2_SDA	SPI2_MISO	DFSDM_DATIN2	USART3_RTS_ DE
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	DFSDM_CKIN2	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/TIM5/TIM8/LPTIM1	TIM1/TIM2/TIM3/TIM4/TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/USART2/USART3
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	DFSDM_DATIN4	-
	PC1	-	LPTIM1_OUT	-	-	I2C3_SDA	-	DFSDM_CKIN4	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	DFSDM_CKOUT	-
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	-	-	-	-	-	-	USART3_RX
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-	DFSDM_CKIN3	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	DFSDM_DATIN3	-
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	-	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	-	-	-	-
	PC10	-	-	-	-	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX
	PC12	-	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port D	PD0	-	-	-	-	-	SPI2_NSS	DFSDM_DATIN7	-
	PD1	-	-	-	-	-	SPI2_SCK	DFSDM_CKIN7	-
	PD2	-	-	TIM3_ETR	-	-	-	-	USART3_RTS_ DE
	PD3	-	-	-	-	-	SPI2_MISO	DFSDM_DATIN0	USART2_CTS
	PD4	-	-	-	-	-	SPI2_MOSI	DFSDM_CKIN0	USART2_RTS_ DE
	PD5	-	-	-	-	-	-	-	USART2_TX
	PD6	-	-	-	-	-	-	DFSDM_DATIN1	USART2_RX
	PD7	-	-	-	-	-	-	DFSDM_CKIN1	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	-	-	-	-	USART3_CK
	PD11	-	-	-	-	-	-	-	USART3_CTS
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS_ DE
	PD13	-	-	TIM4_CH2	-	-	-	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see Table 17) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	-	-	-	DFSDM_DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	-	-	-	DFSDM_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM_DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM_CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM_DATIN4	-
	PE11	-	TIM1_CH2	-	-	-	-	DFSDM_CKIN4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	DFSDM_DATIN5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	DFSDM_CKIN5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/TIM5/TIM8/LPTIM1	TIM1/TIM2/TIM3/TIM4/TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/USART2/USART3
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-
	PF1	-	-	-	-	I2C2_SCL	-	-	-
	PF2	-	-	-	-	I2C2_SMBA	-	-	-
	PF3	-	-	-	-	-	-	-	-
	PF4	-	-	-	-	-	-	-	-
	PF5	-	-	-	-	-	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	-	-	-	-	-
	PF11	-	-	-	-	-	-	-	-
	PF12	-	-	-	-	-	-	-	-
	PF13	-	-	-	-	-	-	DFSDM_DATIN6	-
	PF14	-	-	-	-	-	-	DFSDM_CKIN6	-
	PF15	-	-	-	-	-	-	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port G	PG0	-	-	-	-	-	-	-	-
	PG1	-	-	-	-	-	-	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	-	I2C3_SMBA	-	-	-
	PG7	-	-	-	-	I2C3_SCL	-	-	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	-	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	-	-	-	SPI3_MOSI	USART1_CTS
	PG12	-	LPTIM1_ETR	-	-	-	-	SPI3_NSS	USART1_RTS_ DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port A	PA0	UART4_TX	-	-	-	-	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	-	-	-	-	TIM15_CH1N	EVENTOUT
	PA2	-	-	-	-	-	SAI2_EXTCLK	TIM15_CH1	EVENTOUT
	PA3	-	-	-	-	-	-	TIM15_CH2	EVENTOUT
	PA4	-	-	-	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	-	-	QUADSPI_BK1_IO3	-	TIM1_BKIN_ COMP2	TIM8_BKIN_ COMP2	TIM16_CH1	EVENTOUT
	PA7	-	-	QUADSPI_BK1_IO2	-	-	-	TIM17_CH1	EVENTOUT
	PA8	-	-	-	-	-	-	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	-	-	-	TIM15_BKIN	EVENTOUT
	PA10	-	-	-	-	-	-	TIM17_BKIN	EVENTOUT
	PA11	-	CAN1_RX	-	-	TIM1_BKIN2_ COMP1	-	-	EVENTOUT
	PA12	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PA13	-	-	-	-	-	-	-	EVENTOUT
	PA14	-	-	-	-	-	-	-	EVENTOUT
	PA15	UART4_RTS _DE	TSC_G3_IO1	-	-	-	SAI2_FS_B	-	EVENTOUT

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see Table 16) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port B	PB0	-	-	QUADSPI_BK1_IO1	-	COMP1_OUT	-	-	EVENTOUT
	PB1	-	-	QUADSPI_BK1_IO0	-	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	-	-	-	-	-	EVENTOUT
	PB3	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS_DE	TSC_G2_IO1	-	-	-	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	-	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	-	-	TIM8_BKIN2_COMP2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	-	-	FMC_NL	TIM8_BKIN_COMP1	TIM17_CH1N	EVENTOUT
	PB8	-	CAN1_RX	-	-	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	-	CAN1_TX	-	-	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	-	QUADSPI_CLK	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	QUADSPI_NCS	-	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RTS_DE	TSC_G1_IO1	-	-	SWPMI1_IO	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CTS	TSC_G1_IO2	-	-	SWPMI1_TX	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	-	SWPMI1_RX	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	-	SWPMI1_SUSPEND	SAI2_SD_A	TIM15_CH2	EVENTOUT

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	**CAN1, TSC**	**QUADSPI**	**-**	**SDMMC1, COMP1, COMP2, FMC, SWPMI1**	**SAI1, SAI2**	**TIM2, TIM15, TIM16, TIM17, LPTIM2**	**EVENTOUT**
Port C	PC0	LPUART1_RX	-	-	-	-	-	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	-	-	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	-	-	EVENTOUT
	PC3	-	-	-	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	-	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	EVENTOUT
	PC6	-	TSC_G4_IO1	-	-	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	-	TSC_G4_IO2	-	-	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	-	-	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	-	-	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2_COMP1	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	-	-	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	-	-	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	-	-	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see Table 16) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port D	PD0	-	CAN1_RX	-	-	FMC_D2	-	-	EVENTOUT
	PD1	-	CAN1_TX	-	-	FMC_D3	-	-	EVENTOUT
	PD2	UART5_RX	TSC_SYNC	-	-	SDMMC1_CMD	-	-	EVENTOUT
	PD3	-	-	-	-	FMC_CLK	-	-	EVENTOUT
	PD4	-	-	-	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	FMC_NWAIT	SAI1_SD_A	-	EVENTOUT
	PD7	-	-	-	-	FMC_NE1	-	-	EVENTOUT
	PD8	-	-	-	-	FMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	FMC_D14	SAI2_MCLK_A	-	EVENTOUT
	PD10	-	TSC_G6_IO1	-	-	FMC_D15	SAI2_SCK_A	-	EVENTOUT
	PD11	-	TSC_G6_IO2	-	-	FMC_A16	SAI2_SD_A	LPTIM2_ETR	EVENTOUT
	PD12	-	TSC_G6_IO3	-	-	FMC_A17	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PD13	-	TSC_G6_IO4	-	-	FMC_A18	-	LPTIM2_OUT	EVENTOUT
	PD14	-	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	-	-	FMC_D1	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port E	PE0	-	-	-	-	FMC_NBL0	-	TIM16_CH1	EVENTOUT
	PE1	-	-	-	-	FMC_NBL1	-	TIM17_CH1	EVENTOUT
	PE2	-	TSC_G7_IO1	-	-	FMC_A23	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO2	-	-	FMC_A19	SAI1_SD_B	-	EVENTOUT
	PE4	-	TSC_G7_IO3	-	-	FMC_A20	SAI1_FS_A	-	EVENTOUT
	PE5	-	TSC_G7_IO4	-	-	FMC_A21	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	-	-	FMC_A22	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	-	-	FMC_D4	SAI1_SD_B	-	EVENTOUT
	PE8	-	-	-	-	FMC_D5	SAI1_SCK_B	-	EVENTOUT
	PE9	-	-	-	-	FMC_D6	SAI1_FS_B	-	EVENTOUT
	PE10	-	TSC_G5_IO1	QUADSPI_CLK	-	FMC_D7	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	TSC_G5_IO2	QUADSPI_NCS	-	FMC_D8	-	-	EVENTOUT
	PE12	-	TSC_G5_IO3	QUADSPI_BK1_IO0	-	FMC_D9	-	-	EVENTOUT
	PE13	-	TSC_G5_IO4	QUADSPI_BK1_IO1	-	FMC_D10	-	-	EVENTOUT
	PE14	-	-	QUADSPI_BK1_IO2	-	FMC_D11	-	-	EVENTOUT
	PE15	-	-	QUADSPI_BK1_IO3	-	FMC_D12	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see Table 16) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	-	-	-	SAI1_SD_B	-	EVENTOUT
	PF7	-	-	-	-	-	SAI1_MCLK_B	-	EVENTOUT
	PF8	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PF9	-	-	-	-	-	SAI1_FS_B	TIM15_CH1	EVENTOUT
	PF10	-	-	-	-	-	-	TIM15_CH2	EVENTOUT
	PF11	-	-	-	-	-	-	-	EVENTOUT
	PF12	-	-	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	TSC_G8_IO1	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	TSC_G8_IO2	-	-	FMC_A9	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see Table 16) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port G	PG0	-	TSC_G8_IO3	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	TSC_G8_IO4	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	FMC_A12	SAI2_SCK_B	-	EVENTOUT
	PG3	-	-	-	-	FMC_A13	SAI2_FS_B	-	EVENTOUT
	PG4	-	-	-	-	FMC_A14	SAI2_MCLK_B	-	EVENTOUT
	PG5	LPUART1_CTS	-	-	-	FMC_A15	SAI2_SD_B	-	EVENTOUT
	PG6	LPUART1_RTS_DE	-	-	-	-	-	-	EVENTOUT
	PG7	LPUART1_TX	-	-	-	FMC_INT3	-	-	EVENTOUT
	PG8	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
	PG9	-	-	-	-	FMC_NCE3/ FMC_NE2	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PG10	-	-	-	-	FMC_NE3	SAI2_FS_A	TIM15_CH1	EVENTOUT
	PG11	-	-	-	-	-	SAI2_MCLK_A	TIM15_CH2	EVENTOUT
	PG12	-	-	-	-	FMC_NE4	SAI2_SD_A	-	EVENTOUT
	PG13	-	-	-	-	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	FMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see Table 16) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	QUADSPI	-	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT

5 Memory mapping

Figure 9. STM32L471 memory map

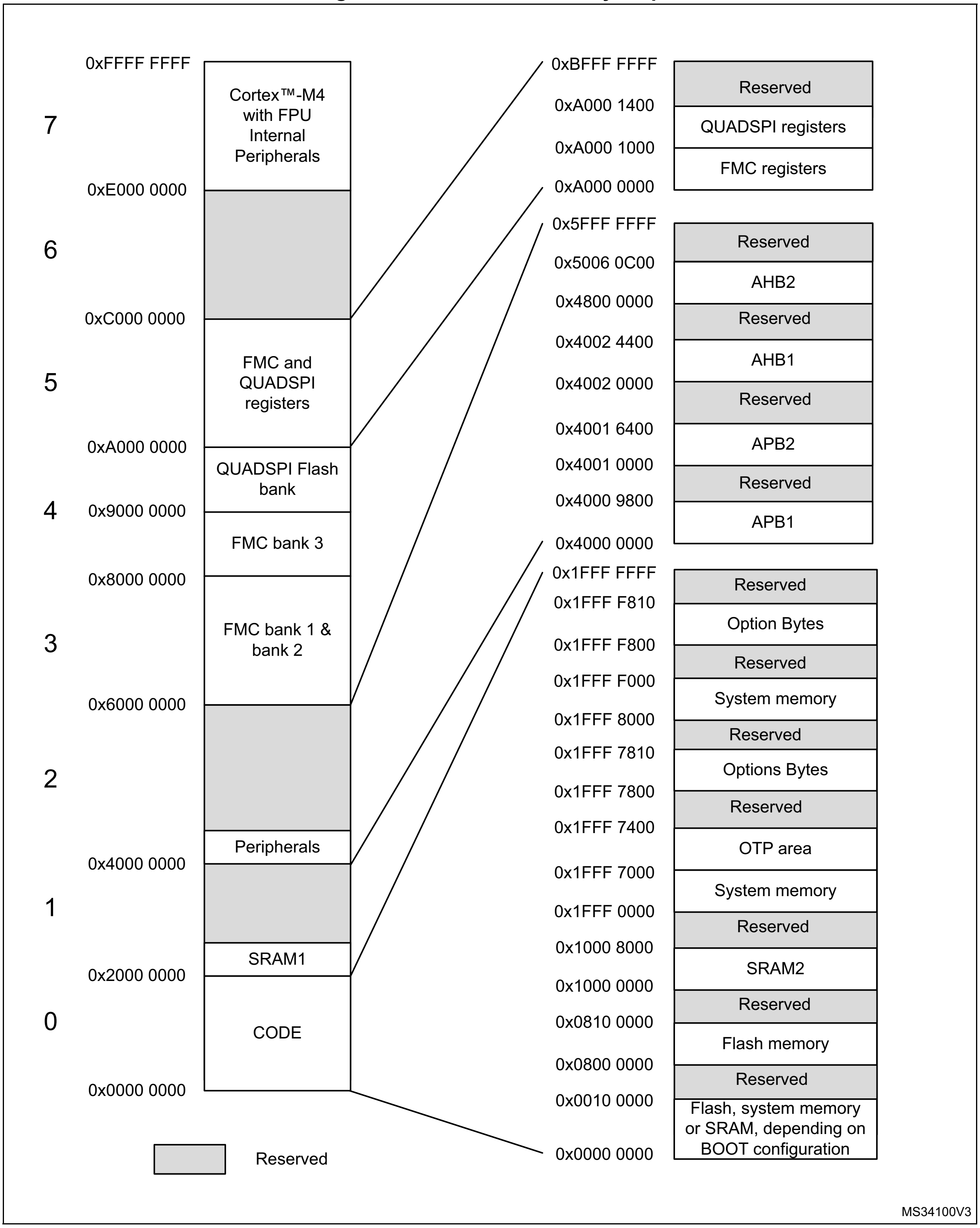


Table 18. STM32L471xx memory map and peripheral register boundary addresses (1)

Bus	Boundary address	Size (bytes)	Peripheral
AHB3	0xA000 1000 - 0xA000 13FF	1 KB	QUADSPI
	0xA000 0000 - 0xA000 0FFF	4 KB	FMC
AHB2	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5004 0400 - 0x5006 07FF	129 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	Reserved
	0x4800 2000 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 1800 - 0x4800 1BFF	1 KB	GPIOG
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~127 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH registers
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1

Table 18. STM32L471xx memory map and peripheral register boundary addresses (continued)[(1)]

Bus	Boundary address	Size (bytes)	Peripheral
APB2	0x4001 6400 - 0x4001 FFFF	39 KB	Reserved
	0x4001 6000 - 0x4000 63FF	1 KB	DFSDM
	0x4001 5C00 - 0x4000 5FFF	1 KB	Reserved
	0x4001 5800 - 0x4000 5BFF	1 KB	SAI2
	0x4001 5400 - 0x4000 57FF	1 KB	SAI1
	0x4001 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
APB2	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	TIM8
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	SDMMC1
	0x4001 2000 - 0x4001 27FF	2 KB	Reserved
	0x4001 1C00 - 0x4001 1FFF	1 KB	FIREWALL
	0x4001 0800- 0x4001 1BFF	5 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0200 - 0x4001 03FF	1 KB	COMP
	0x4001 0030 - 0x4001 01FF		VREFBUF
	0x4001 0000 - 0x4001 002F		SYSCFG

Table 18. STM32L471xx memory map and peripheral register boundary addresses (continued)(1)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	Reserved
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved
	0x4000 5C00- 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2

Table 18. STM32L471xx memory map and peripheral register boundary addresses (continued)[1]

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 1800 - 0x4000 27FF	4 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00- 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

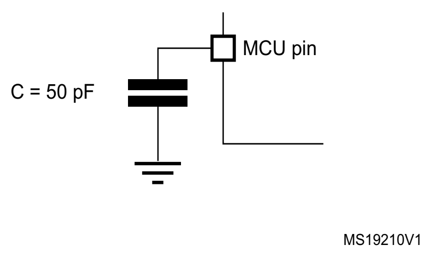
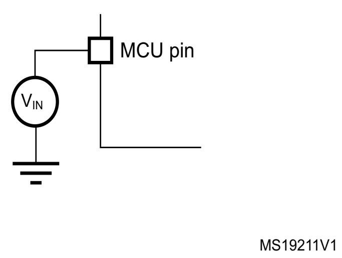
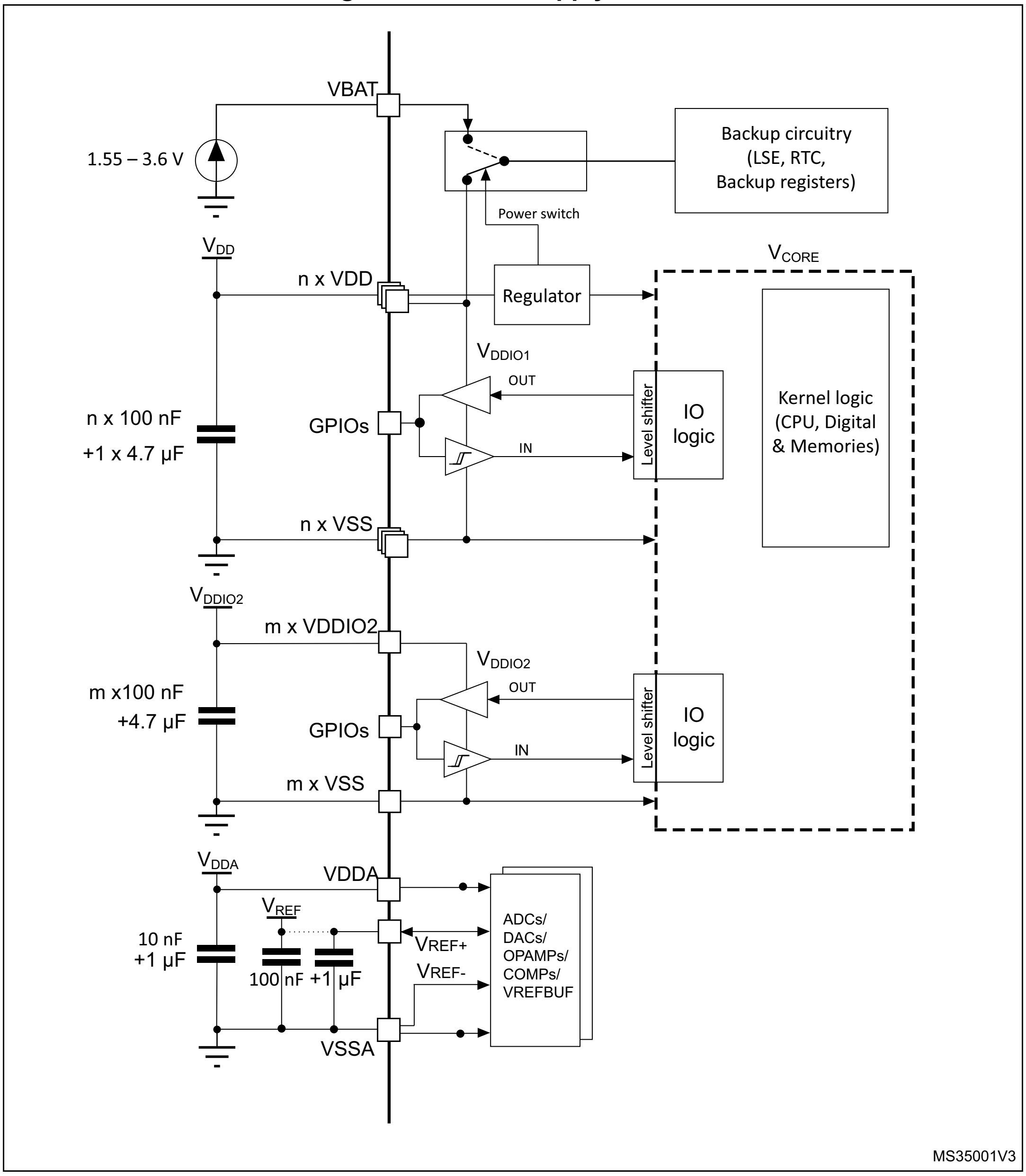


Figure 11. Pin input voltage



6.1.6 Power supply scheme

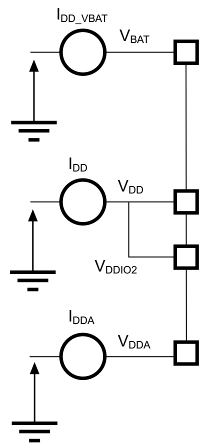
Figure 12. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics* and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
$V_{DDX} - V_{SS}$	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDIO2}, V_{BAT})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDIO2}) + 4.0(3)(4)	V
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on BOOT0 pin	V_{SS}	9.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins(5)	-	50	mV

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 20. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)	150	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(4)	
	Injected current on PA4, PA5	-5/0	
$\sum \lvert I_{INJ(PIN)} \rvert$	Total injected current (sum of all I/Os and control pins)(5)	25	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the minimum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum \lvert I_{INJ(PIN)} \rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-		0	80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-		0	80	
f_{PCLK2}	Internal APB2 clock frequency	-		0	80	
V_{DD}	Standard operating voltage	-		1.71 (1)	3.6	V
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used		1.08	3.6	V
		PG[15:2] not used		0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used		1.62	3.6	V
		DAC or OPAMP used		1.8		
		VREFBUF used		2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used		0		
V_{BAT}	Backup operating voltage	-		1.55	3.6	V
V_{IN}	I/O input voltage	TT_xx I/O		-0.3	V_{DDIOx}+0.3	V
		BOOT0		0	9	
		All I/O except BOOT0 and TT_xx		-0.3	MIN(MIN(V_{DD}, V_{DDA}, V_{DDIO2})+3.6 V, 5.5 V)(2)(3)	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP144	-	-	625	mW
		LQFP100	-	-	476	
		LQFP64	-	-	444	
		UFBGA132	-	-	363	
TA	Ambient temperature for the suffix 6 version	Maximum power dissipation		–40	85	°C
		Low-power dissipation(5)		–40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation		–40	105	
		Low-power dissipation(5)		–40	125	
	Ambient temperature for the suffix 3 version	Maximum power dissipation		–40	125	
		Low-power dissipation(5)		–40	130	
TJ	Junction temperature range	Suffix 6 version		–40	105	°C
		Suffix 7 version		–40	125	
		Suffix 3 version		–40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA}, V_{DDIO2})+3.6 V and 5.5V.

3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDIO2}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.5: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.5: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 23* are derived from tests performed under the ambient temperature condition summarized in *Table 22*.

Table 23. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DDA} fall time rate		10	∞	
t_{VDDIO2}	V_{DDIO2} rise time rate	-	0	∞	µs/V
	V_{DDIO2} fall time rate		10	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 24* are derived from tests performed under the ambient temperature conditions summarized in *Table 22: General operating conditions*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	

Table 24. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[(1)]	Min	Typ	Max	Unit
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)[(2)]	BOR[(3)] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM2}	V_{DDIO2} peripheral voltage monitoring	-	0.92	0.96	1	V
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1/PVM2) [(2)]	PVM1 and PVM2 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4) [(2)]	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

6.3.4 Embedded voltage reference

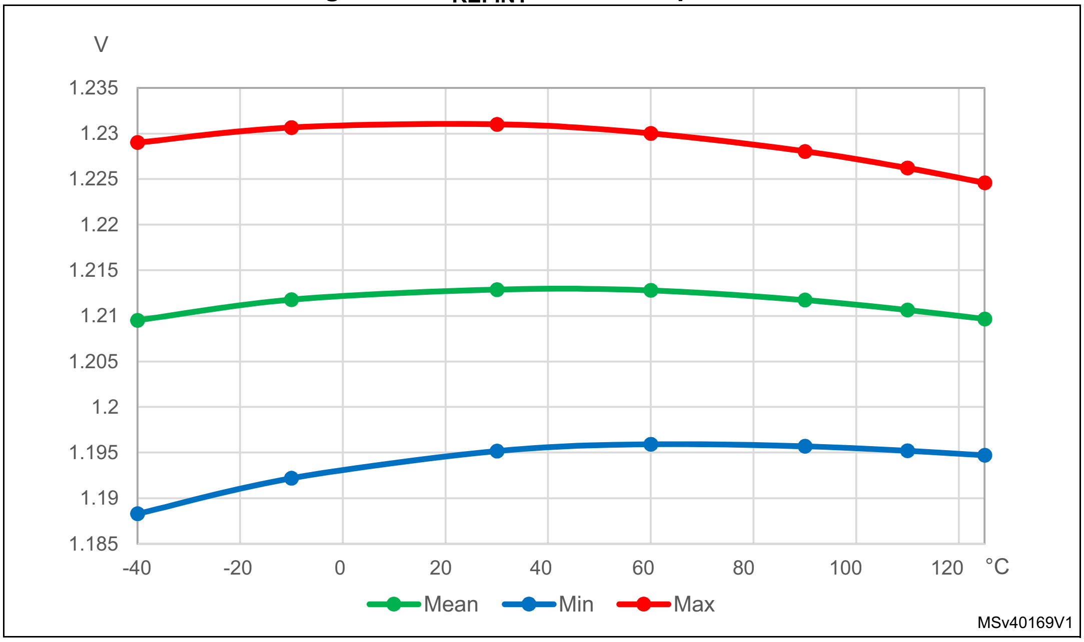
The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 25. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	-	TBD(2)	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Figure 14. V_{REFINT} versus temperature



6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0392 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 26* to *Table 39* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
$I_{DD}(Run)$	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.88	2.93	3.05	3.23	3.58	3.20	3.37	3.51	3.93	4.76	mA
				16 MHz	1.83	1.87	1.98	2.16	2.49	2.01	2.16	2.30	2.72	3.34	
				8 MHz	0.98	1.02	1.12	1.29	1.62	1.10	1.17	1.31	1.73	2.56	
				4 MHz	0.55	0.59	0.69	0.85	1.18	0.61	0.70	0.89	1.24	1.95	
				2 MHz	0.34	0.37	0.47	0.64	0.96	0.37	0.46	0.64	0.98	1.71	
				1 MHz	0.23	0.26	0.36	0.53	0.85	0.27	0.33	0.50	0.86	1.57	
				100 kHz	0.14	0.17	0.27	0.43	0.75	0.17	0.21	0.38	0.74	1.44	
			Range 1	80 MHz	10.2	10.3	10.5	10.7	11.1	11.22	11.8	12.1	12.5	13.3	
				72 MHz	9.24	9.31	9.47	9.69	10.1	10.16	10.7	11.0	11.4	12.2	
				64 MHz	8.25	8.32	8.46	8.68	9.09	9.08	9.6	9.9	10.3	11.1	
				48 MHz	6.28	6.35	6.5	6.72	7.11	6.91	7.3	7.6	8.0	8.8	
				32 MHz	4.24	4.30	4.44	4.65	5.04	4.66	4.97	5.26	5.67	6.51	
				24 MHz	3.21	3.27	3.4	3.61	3.98	3.53	3.76	4.05	4.46	5.30	
				16 MHz	2.19	2.24	2.36	2.56	2.94	2.41	2.66	2.95	3.16	3.99	
$I_{DD}(LPRun)$	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	272	303	413	592	958	330	393	579	954	1704	µA
				1 MHz	154	184	293	473	835	195	265	457	822	1572	
				400 kHz	78	108	217	396	758	110	180	380	755	1505	
				100 kHz	42	73	182	360	723	75	138	331	706	1456	

1. Guaranteed by characterization results, unless otherwise specified.

Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
$I_{DD}(Run)$	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.15	3.19	3.31	3.50	3.85	3.47	3.70	3.84	4.26	4.88	mA
				16 MHz	2.24	2.28	2.39	2.57	2.90	2.46	2.60	2.74	3.16	3.78	
				8 MHz	1.26	1.29	1.40	1.57	1.89	1.40	1.50	1.64	2.06	2.68	
				4 MHz	0.71	0.75	0.85	1.02	1.34	0.79	0.88	1.06	1.38	2.21	
				2 MHz	0.42	0.45	0.55	0.72	1.04	0.46	0.55	0.73	1.09	1.88	
				1 MHz	0.27	0.30	0.40	0.57	0.89	0.30	0.38	0.57	0.90	1.61	
				100 kHz	0.14	0.17	0.27	0.43	0.75	0.17	0.22	0.40	0.74	1.44	
			Range 1	80 MHz	10.0	10.1	10.3	10.6	11.0	11.00	11.35	11.64	12.26	13.10	
				72 MHz	9.06	9.13	9.28	9.51	9.92	9.97	10.36	10.65	11.06	11.69	
				64 MHz	8.96	9.04	9.22	9.48	9.92	9.86	10.25	10.54	10.95	11.79	
				48 MHz	7.64	7.72	7.91	8.17	8.62	8.40	8.76	8.90	9.52	10.36	
				32 MHz	5.49	5.57	5.74	5.98	6.40	6.04	6.40	6.69	7.10	7.94	
				24 MHz	4.16	4.22	4.36	4.57	4.96	4.60	4.86	5.15	5.56	6.19	
				16 MHz	2.93	2.99	3.13	3.35	3.75	3.22	3.43	3.72	4.13	4.97	
$I_{DD}(LPRun)$	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	358	392	503	683	1050	435	501	694	1069	1819	µA
				1 MHz	197	230	340	519	880	245	312	512	887	1637	
				400 kHz	97	126	235	414	778	130	202	402	777	1527	
				100 kHz	47	77	186	365	726	85	147	347	711	1472	

1. Guaranteed by characterization results, unless otherwise specified.

Table 28. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.88	2.94	3.05	3.23	3.58	3.18	3.26	3.40	4.02	4.65	mA
				16 MHz	1.83	1.87	1.98	2.15	2.50	2.01	2.16	2.30	2.72	3.34	
				8 MHz	0.97	1.00	1.11	1.27	1.62	1.07	1.16	1.32	1.73	2.36	
				4 MHz	0.54	0.57	0.67	0.84	1.18	0.59	0.69	0.88	1.23	1.96	
				2 MHz	0.33	0.36	0.46	0.62	0.96	0.37	0.45	0.63	0.98	1.70	
				1 MHz	0.22	0.25	0.35	0.51	0.85	0.25	0.33	0.50	0.86	1.57	
				100 kHz	0.12	0.15	0.25	0.41	0.75	0.15	0.21	0.39	0.74	1.45	
			Range 1	80 MHz	10.2	10.3	10.5	10.7	11.1	11.22	11.57	11.86	12.07	13.11	
				72 MHz	9.25	9.31	9.46	9.68	10.1	10.18	10.41	10.55	10.76	11.80	
				64 MHz	8.25	8.31	8.46	8.67	9.08	9.08	9.37	9.66	9.87	10.91	
				48 MHz	6.26	6.33	6.48	6.69	7.11	6.89	7.11	7.25	7.67	8.50	
				32 MHz	4.22	4.28	4.42	4.63	5.03	4.64	4.86	5.15	5.56	6.19	
				24 MHz	3.20	3.25	3.38	3.59	3.99	3.52	3.70	3.84	4.26	5.09	
				16 MHz	2.18	2.22	2.35	2.55	2.94	2.40	2.55	2.84	3.25	4.09	
I_{DD}(LPRun)	Supply current in low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable FLASH in power-down		2 MHz	242	275	384	562	924	300	380	573	927	1677	µA
				1 MHz	130	162	269	445	809	180	243	435	810	1560	
				400 kHz	61	90	197	374	734	95	160	353	728	1478	
				100 kHz	26	56	163	339	702	55	122	314	679	1429	

1. Guaranteed by characterization results, unless otherwise specified.

Table 29. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions -	Voltage scaling	Code	TYP 25 °C	Unit	TYP 25 °C	Unit
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	2.9	mA	111	µA/MHz
				Coremark	3.1		118	
				Dhrystone 2.1	3.1		119	
				Fibonacci	2.9		112	
				While(1)	2.8		108	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	10.2	mA	127	µA/MHz
				Coremark	10.9		136	
				Dhrystone 2.1	11.0		137	
				Fibonacci	10.5		131	
				While(1)	9.9		124	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz all peripherals disable		Reduced code(1)	272	µA	136	µA/MHz
				Coremark	291		145	
				Dhrystone 2.1	302		151	
				Fibonacci	269		135	
				While(1)	269		135	

1. Reduced code used for characterization results provided in *Table 26*, *Table 27*, *Table 28*.

Table 30. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	3.1	mA	119	µA/MHz
				Coremark	2.9		111	
				Dhrystone 2.1	2.8		111	
				Fibonacci	2.7		104	
				While(1)	2.6		100	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	10.0	mA	125	µA/MHz
				Coremark	9.4		117	
				Dhrystone 2.1	9.1		114	
				Fibonacci	9.0		112	
				While(1)	9.3		116	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz all peripherals disable		Reduced code(1)	358	µA	179	µA/MHz
				Coremark	392		196	
				Dhrystone 2.1	390		195	
				Fibonacci	385		192	
				While(1)	385		192	

1. Reduced code used for characterization results provided in *Table 26*, *Table 27*, *Table 28*.

Table 31. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	2.9	mA	111	µA/MHz
				Coremark	2.9		111	
				Dhrystone 2.1	2.9		111	
				Fibonacci	2.6		100	
				While(1)	2.6		100	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	10.2	mA	127	µA/MHz
				Coremark	10.4		130	
				Dhrystone 2.1	10.3		129	
				Fibonacci	9.6		120	
				While(1)	9.3		116	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz all peripherals disable		Reduced code(1)	242	µA	121	µA/MHz
				Coremark	242		121	
				Dhrystone 2.1	242		121	
				Fibonacci	225		112	
				While(1)	242		121	

1. Reduced code used for characterization results provided in *Table 26*, *Table 27*, *Table 28*.

Table 32. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.92	0.96	1.07	1.25	1.59	1.012	1.14	1.36	1.77	2.40	mA
				16 MHz	0.61	0.65	0.75	0.92	1.27	0.69	0.78	0.97	1.32	2.04	
				8 MHz	0.36	0.40	0.50	0.66	1.01	0.42	0.50	0.68	1.03	1.75	
				4 MHz	0.24	0.27	0.37	0.53	0.87	0.28	0.36	0.54	0.89	1.60	
				2 MHz	0.18	0.20	0.30	0.47	0.81	0.215	0.29	0.46	0.82	1.53	
				1 MHz	0.15	0.17	0.27	0.43	0.77	0.18	0.25	0.44	0.78	1.49	
				100 kHz	0.12	0.14	0.24	0.41	0.74	0.15	0.21	0.39	0.74	1.44	
			Range 1	80 MHz	2.96	3.00	3.13	3.33	3.73	3.26	3.43	3.72	4.13	4.97	
				72 MHz	2.69	2.73	2.85	3.05	3.45	2.96	3.21	3.50	3.71	4.54	
				64 MHz	2.41	2.45	2.58	2.77	3.17	2.65	2.88	3.17	3.58	4.21	
				48 MHz	1.88	1.93	2.07	2.27	2.67	2.10	2.27	2.41	2.83	3.66	
				32 MHz	1.30	1.35	1.48	1.68	2.08	1.43	1.56	1.85	2.26	3.10	
				24 MHz	1.01	1.05	1.17	1.37	1.76	1.11	1.23	1.52	1.93	2.77	
				16 MHz	0.71	0.75	0.87	1.07	1.45	0.80	0.90	1.19	1.60	2.44	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	96	126	233	412	775	130	202	402	777	1527	µA
				1 MHz	65	94	202	381	742	95	166	358	733	1483	
				400 kHz	43	73	181	359	718	75	138	331	706	1456	
				100 kHz	33	63	171	348	708	65	128	322	691	1441	

1. Guaranteed by characterization results, unless otherwise specified.

Table 33. Current consumption in Low-power sleep modes, Flash in power-down

Symbol	Parameter	Conditions			TYP					MAX[1]					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	81	110	217	395	754	115	182	375	750	1500	µA
				1 MHz	50	78	185	362	720	80	149	342	717	1456	
				400 kHz	28	57	163	340	698	60	122	314	689	1429	
				100 kHz	18	47	155	332	686	50	114	313	688	1438	

1. Guaranteed by characterization results, unless otherwise specified.

Table 34. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	1.14	3.77	14.7	34.7	77	2.7	9	37	87	193	µA
			2.4 V	1.15	3.86	15	35.5	79.1	2.7	10	38	89	198	
			3 V	1.18	3.97	15.4	36.4	81.3	2.8	10	39	91	203	
			3.6 V	1.26	4.11	16	38	85.1	3.0	10	40	95[2]	213	
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	1.42	4.04	15	34.9	77.2	3.1	10	38	87	193	µA
			2.4 V	1.5	4.22	15.4	35.7	79.2	3.2	11	39	89	198	
			3 V	1.64	4.37	15.8	36.7	81.4	3.4	11	40	92	204	
			3.6 V	1.79	4.65	16.6	38.4	85.4	3.6	12	42	96	214	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	1.5	4.13	15.2	35.3	77.6	3.2	10	38	88	194	
			2.4 V	1.63	4.33	15.6	36	79.6	3.4	11	39	90	199	
			3 V	1.79	4.55	16.1	37	81.8	3.6	11	40	93	205	
			3.6 V	2.04	4.9	16.8	38.7	85.6	3.9	12	42	97	214	
		RTC clocked by LSE quartz[3] in low drive mode	1.8 V	1.43	3.99	14.7	35	-	3.2	10	37	88	-	
			2.4 V	1.54	4.11	15	35.8	-	3.3	10	38	90	-	
			3 V	1.67	4.29	15.5	36.7	-	3.4	11	39	92	-	
			3.6 V	1.87	4.57	16.2	38.3	-	3.7	11	41	96	-	

Table 34. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (wakeup from Stop2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1. See [4].	3 V	1.9	-	-	-	-	-					mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See [4].	3 V	2.24	-	-	-	-						
		Wakeup clock is HSI16 = 16 MHz, voltage Range 1. See [4].	3 V	2.1	-	-	-	-						

1. Guaranteed based on test during characterization, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 41: Low-power mode wakeup timings*.

Table 35. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	1.8 V	6.59	24.7	92.7	208	437	16	62	232	520	1093	µA
			2.4 V	6.65	24.8	92.9	209	439	17	62	232	523	1098	
			3 V	6.65	24.9	93.3	210	442	17	62	233	525	1105	
			3.6 V	6.70	25.1	93.8	212	447	17	63	235	530	1118	
I_{DD} (Stop 1 with RTC)	Supply current in stop 1 mode, RTC enabled	RTC clocked by LSI	1.8 V	6.88	25.0	93.1	209	439	17	63	233	523	1098	µA
			2.4 V	7.02	25.2	93.7	210	441	18	63	234	525	1103	
			3 V	7.12	25.4	94.2	212	444	18	64	236	530	1110	
			3.6 V	7.25	25.7	95.2	214	449	18	64	238	535	1123	
		RTC clocked by LSE bypassed, at 32768 Hz	1.8 V	6.91	25.2	93.4	210	440	17	63	234	525	1100	
			2.4 V	7.04	25.3	94.2	211	443	18	63	236	528	1108	
			3 V	7.19	25.7	95.0	212	446	18	64	238	530	1115	
			3.6 V	7.97	26.0	96.1	215	451	20	65	240	538	1128	
		RTC clocked by LSE quartz(2) in low drive mode	1.8 V	6.85	25.0	93.0	208.3	-	17	63	233	521	-	
			2.4 V	6.94	25.1	93.2	209.3	-	17	63	233	523	-	
			3 V	7.10	25.2	93.6	210.3	-	18	63	234	526	-	
			3.6 V	7.34	25.4	94.1	212.3	-	18	64	235	531	-	
I_{DD} (wakeup from Stop1)	Supply current during wakeup from Stop 1	Wakeup clock MSI = 48 MHz, voltage Range 1, See (3).	3 V	1.47	-	-	-	-	-					mA
		Wakeup clock MSI = 4 MHz, voltage Range 2, See (3).	3 V	1.7	-	-	-	-						
		Wakeup clock HSI16 = 16 MHz, voltage Range 1, See (3).	3 V	1.62	-	-	-	-						

1. Guaranteed based on test during characterization, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 41: Low-power mode wakeup timings*.

Table 36. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions	TYP					MAX[1]					Unit
		V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (Stop 0)	Supply current in Stop 0 mode, RTC disabled	1.8 V	108	132	217	356	631	153	213	426	773	1461	µA
		2.4 V	110	134	219	358	634	158	218	431	778	1468	
		3 V	111	135	220	360	637	161	221	433	783	1476	
		3.6 V	113	137	222	363	642	166	226	438	791[2]	1488	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 37. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	no independent watchdog	1.8 V	114	355	1540	4146	10735	176	888	3850	10365	26838	nA
			2.4 V	138	407	1795	4828	12451	223	1018	4488	12070	31128	
			3 V	150	486	2074	5589	14291	263	1215	5185	13973	35728	
			3.6 V	198	618	2608	6928	17499	383	1545	6520	17320 (2)	43748	
		with independent watchdog	1.8 V	317	-	-	-	-	-	-	-	-	-	
			2.4 V	391	-	-	-	-	-	-	-	-	-	
			3 V	438	-	-	-	-	-	-	-	-	-	
			3.6 V	566	-	-	-	-	-	-	-	-	-	
I_{DD}(Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	377	621	1873	4564	11318	491	1207	4250	10867	27537	nA
			2.4 V	464	756	2210	5348	13166	614	1436	4986	12694	31986	
			3 V	572	913	2599	6219	15197	770	1727	5815	14729	36815	
			3.6 V	722	1144	3253	7724	18696	1012	2176	7294	18275	45184	
		RTC clocked by LSI, with independent watchdog	1.8 V	456	-	-	-	-	-	-	-	-	-	
			2.4 V	557	-	-	-	-	-	-	-	-	-	
			3 V	663	-	-	-	-	-	-	-	-	-	
			3.6 V	885	-	-	-	-	-	-	-	-	-	
		RTC clocked by LSE bypassed at 32768Hz	1.8 V	289	527	1747	4402	11009	-	-	-	-	-	nA
			2.4 V	396	671	2108	5202	12869	-	-	-	-	-	
			3 V	528	853	2531	6095	14915	-	-	-	-	-	
			3.6 V	710	1111	3115	7470	18221	-	-	-	-	-	
		RTC clocked by LSE quartz (3) in low drive mode	1.8 V	416	640	1862	4479	11908	-	-	-	-	-	
			2.4 V	514	796	2193	5236	13689	-	-	-	-	-	
			3 V	652	961	2589	6103	15598	-	-	-	-	-	
			3.6 V	821	1226	3235	7551	17947	-	-	-	-	-	

Table 37. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(SRAM2) (4)	Supply current to be added in Standby mode when SRAM2 is retained	-	1.8 V	235	641	2293	5192	11213	588	1603	5733	12980	28033	nA
			2.4 V	237	645	2303	5213	11246	593	1613	5758	13033	28115	
			3 V	236	647	2306	5221	11333	593	1618	5765	13053	28333	
			3.6 V	235	646	2308	5200	11327	595	1620	5770	13075	28350	
I_{DD}(wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is MSI = 4 MHz. See (5).	3 V	1.7	-	-	-	-	-					mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. The supply current in Standby with SRAM2 mode is: I_{DD}(Standby) + I_{DD}(SRAM2). The supply current in Standby with RTC with SRAM2 mode is: I_{DD}(Standby + RTC) + I_{DD}(SRAM2).
5. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 41: Low-power mode wakeup timings*.

Table 38. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	29.8	194	1110	3250	9093	75	485	2775	8125	22733	nA
			2.4 V	44.3	237	1310	3798	10473	111	593	3275	9495	26183	
			3 V	64.1	293	1554	4461	12082	160	733	3885	11153	30205	
			3.6 V	112	420	2041	5689	15186	280	1050	5103	14223	37965	

Table 38. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	210	378	1299	3437	9357	-	-	-	-	-	nA
			2.4 V	303	499	1577	4056	10825	-	-	-	-	-	
			3 V	422	655	1925	4820	12569	-	-	-	-	-	
			3.6 V	584	888	2511	6158	15706	-	-	-	-	-	
		RTC clocked by LSE quartz [2] in low drive mode	1.8 V	329	499	1408	3460	-	-	-	-	-	-	
			2.4 V	431	634	1688	4064	-	-	-	-	-	-	
			3 V	554	791	2025	4795	-	-	-	-	-	-	
			3.6 V	729	1040	2619	6129	-	-	-	-	-	-	
I_{DD}(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz. See [3].	3 V	0.6	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 41: Low-power mode wakeup timings*.

Table 39. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{BAT}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(VBAT)	Backup domain supply current	RTC disabled	1.8 V	4	29	196	587	1663	10.8	73	490	1468	4158	nA
			2.4 V	5.27	36	226	673	1884	13.2	90	565	1683	4710	
			3 V	6	42	264	775	2147	15.5	106	660	1938	5368	
			3.6 V	10	58	323	919	2488	25.8	144	808	2298	6220	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	183	201	367	729	-	-	-	-	-	-	
			2.4 V	268	295	486	901	-	-	-	-	-	-	
			3 V	376	412	602	1075	-	-	-	-	-	-	
			3.6 V	508	558	752	1299	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz[2]	1.8 V	302	344	521	915	1978	-	-	-	-	-	
			2.4 V	388	436	639	1091	2289	-	-	-	-	-	
			3 V	494	549	784	1301	2656	-	-	-	-	-	
			3.6 V	630	692	971	1571	3115	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 58: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 40: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 40*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 19: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 40*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 40. Peripheral current consumption

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix(1)	4.5	3.7	4.1	µA/MHz
	ADC independent clock domain	0.4	0.1	0.2	
	ADC AHB clock domain	5.5	4.7	5.5	
	CRC	0.4	0.2	0.3	
	DMA1	1.4	1.3	1.4	
	DMA2	1.5	1.3	1.4	
	FLASH	6.2	5.2	5.8	
	FMC	8.9	7.5	8.4	
	GPIOA(2)	4.8	3.8	4.4	
	GPIOB(2)	4.8	4.0	4.6	
	GPIOC(2)	4.5	3.8	4.3	
	GPIOD(2)	4.6	3.9	4.4	
	GPIOE(2)	5.2	4.5	4.9	
	GPIOF(2)	5.9	4.9	5.7	
	GPIOG(2)	4.3	3.8	4.2	
	GPIOH(2)	0.7	0.6	0.8	
	QUADSPI	7.8	6.7	7.3	
	RNG independent clock domain	2.2	NA	NA	
	RNG AHB clock domain	0.6	NA	NA	
	SRAM1	0.9	0.8	0.9	
AHB	SRAM2	1.6	1.4	1.6	µA/MHz
	TSC	1.8	1.4	1.6	
	All AHB Peripherals	118.5	77.3	87.6	

Table 40. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	AHB to APB1 bridge(3)	0.9	0.7	0.9	µA/MHz
	CAN1	4.6	4.0	4.4	
	DAC1	2.4	1.9	2.2	
	I2C1 independent clock domain	3.7	3.1	3.2	
	I2C1 APB clock domain	1.3	1.1	1.5	
	I2C2 independent clock domain	3.7	3.0	3.2	
	I2C2 APB clock domain	1.4	1.1	1.5	
	I2C3 independent clock domain	2.9	2.3	2.5	
	I2C3 APB clock domain	0.9	0.9	1.1	
	LPUART1 independent clock domain	2.1	1.6	2.0	
	LPUART1 APB clock domain	0.6	0.6	0.6	
	LPTIM1 independent clock domain	3.3	2.6	2.9	
	LPTIM1 APB clock domain	0.9	0.8	1.0	
	LPTIM2 independent clock domain	3.1	2.7	2.9	
	LPTIM2 APB clock domain	0.8	0.6	0.7	
	OPAMP	0.4	0.4	0.3	
	PWR	0.5	0.5	0.4	
	SPI2	1.8	1.6	1.6	
	SPI3	2.1	1.7	1.8	
	SWPMI1 independent clock domain	2.3	1.8	2.2	
	SWPMI1 APB clock domain	1.1	1.1	1.0	
	TIM2	6.8	5.7	6.3	
	TIM3	5.4	4.6	5.0	
	TIM4	5.2	4.4	4.9	
	TIM5	6.5	5.5	6.1	
	TIM6	1.1	1.0	1.0	
	TIM7	1.1	0.9	1.0	

Table 40. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	USART2 independent clock domain	4.1	3.6	3.8	µA/MHz
	USART2 APB clock domain	1.4	1.1	1.5	
	USART3 independent clock domain	4.7	4.1	4.2	
	USART3 APB clock domain	1.5	1.3	1.7	
	UART4 independent clock domain	3.9	3.2	3.5	
	UART4 APB clock domain	1.5	1.3	1.6	
	UART5 independent clock domain	3.9	3.2	3.5	
	UART5 APB clock domain	1.3	1.2	1.4	
	WWDG	0.5	0.5	0.5	
	All APB1 on	84.2	70.7	80.2	
APB2	AHB to APB2 bridge(4)	1.0	0.9	0.9	
	DFSDM	5.6	4.6	5.3	
	FW	0.7	0.5	0.7	
	SAI1 independent clock domain	2.6	2.1	2.3	
	SAI1 APB clock domain	2.1	1.8	2.0	
	SAI2 independent clock domain	3.3	2.7	3.0	
	SAI2 APB clock domain	2.4	2.1	2.2	
	SDMMC1 independent clock domain	4.7	3.9	4.2	
	SDMMC1 APB clock domain	2.5	1.9	2.1	
	SPI1	2.0	1.6	1.9	
	SYSCFG/VREFBUF/COMP	0.6	0.4	0.5	
	TIM1	8.3	6.9	7.9	
	TIM8	8.6	7.1	8.1	
	TIM15	4.1	3.4	3.9	
	TIM16	3.0	2.5	2.9	
	TIM17	3.0	2.4	2.9	
	USART1 independent clock domain	4.9	4.0	4.4	
	USART1 APB clock domain	1.5	1.3	1.7	
	All APB2 on	56.8	43.3	48.2	
ALL		256.8	189.6	215.5	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The GPIOx (x= A…H) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).
3. The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.
4. The AHB to APB2 Bridge is automatically active when at least one peripheral is ON on the APB2.

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 41* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 41. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		6	9.3	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	5.6	10.9	µs
			Wakeup clock HSI16 = 16 MHz	4.7	10.4	
		Range 2	Wakeup clock MSI = 24 MHz	5.7	11.1	
			Wakeup clock HSI16 = 16 MHz	4.5	10.5	
			Wakeup clock MSI = 4 MHz	6.6	14.2	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	0.7	2.05	
			Wakeup clock HSI16 = 16 MHz	1.7	2.8	
		Range 2	Wakeup clock MSI = 24 MHz	0.8	2.72	
			Wakeup clock HSI16 = 16 MHz	1.7	2.8	
			Wakeup clock MSI = 4 MHz	2.4	11.32	

Table 41. Low-power mode wakeup timings[1] (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	6.2	10.2	µs
			Wakeup clock HSI16 = 16 MHz	6.3	8.99	
		Range 2	Wakeup clock MSI = 24 MHz	6.3	10.46	
			Wakeup clock HSI16 = 16 MHz	6.3	8.87	
			Wakeup clock MSI = 4 MHz	8.0	13.23	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	4.5	5.78	
			Wakeup clock HSI16 = 16 MHz	5.5	7.1	
		Range 2	Wakeup clock MSI = 24 MHz	5.0	6.5	
			Wakeup clock HSI16 = 16 MHz	5.5	7.1	
			Wakeup clock MSI = 4 MHz	8.2	13.5	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	12.7	20	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			10.7	21.5	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	8.0	9.4	µs
			Wakeup clock HSI16 = 16 MHz	7.3	9.3	
		Range 2	Wakeup clock MSI = 24 MHz	8.2	9.9	
			Wakeup clock HSI16 = 16 MHz	7.3	9.3	
			Wakeup clock MSI = 4 MHz	10.6	15.8	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.1	6.7	
			Wakeup clock HSI16 = 16 MHz	5.7	8	
		Range 2	Wakeup clock MSI = 24 MHz	5.5	6.65	
			Wakeup clock HSI16 = 16 MHz	5.7	7.53	
			Wakeup clock MSI = 4 MHz	8.2	16.6	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	14.3	20.8	µs
			Wakeup clock MSI = 4 MHz	20.1	35.5	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	14.3	24.3	µs
			Wakeup clock MSI = 4 MHz	20.1	38.5	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	256	330.6	µs

1. Guaranteed by characterization results.

Table 42. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low-power run mode to Run mode(2)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

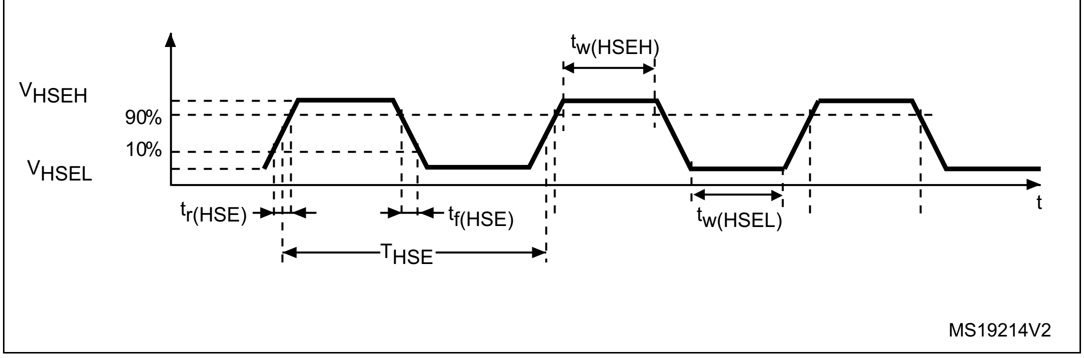
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15: High-speed external clock source AC timing diagram*.

Table 43. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

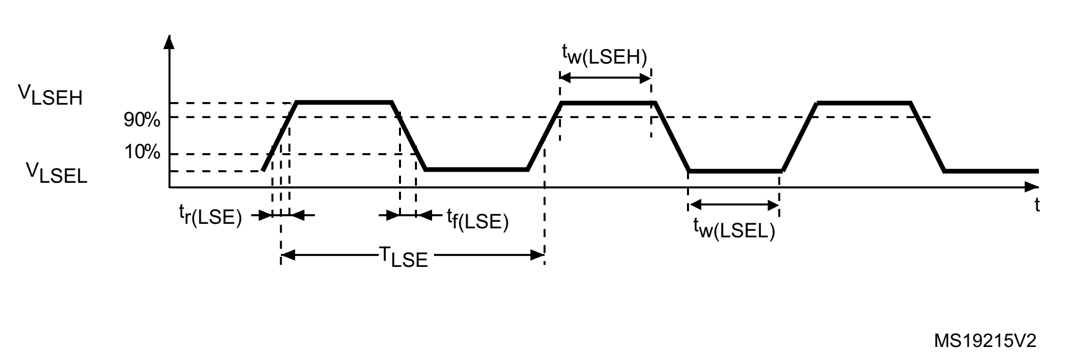
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 16*.

Table 44. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	V
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 16. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 45*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 45. HSE oscillator characteristics(1)

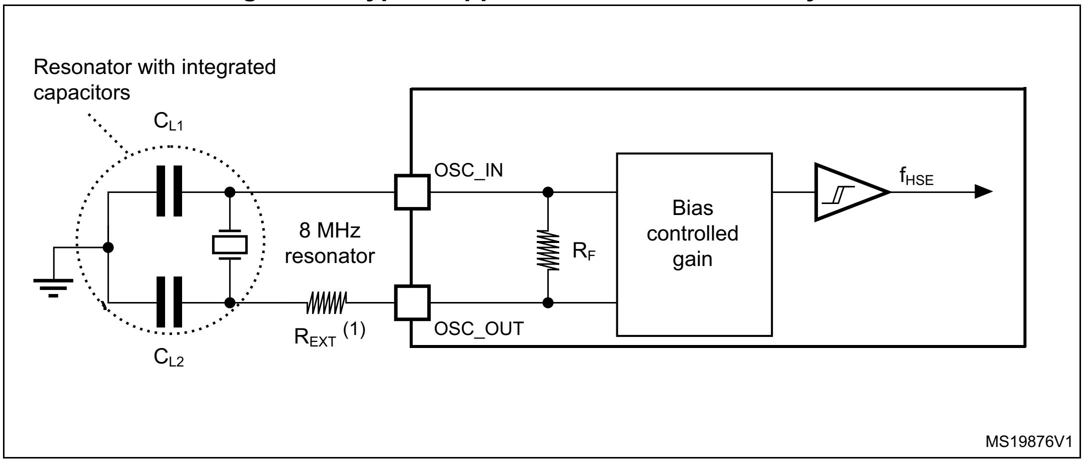
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 46*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

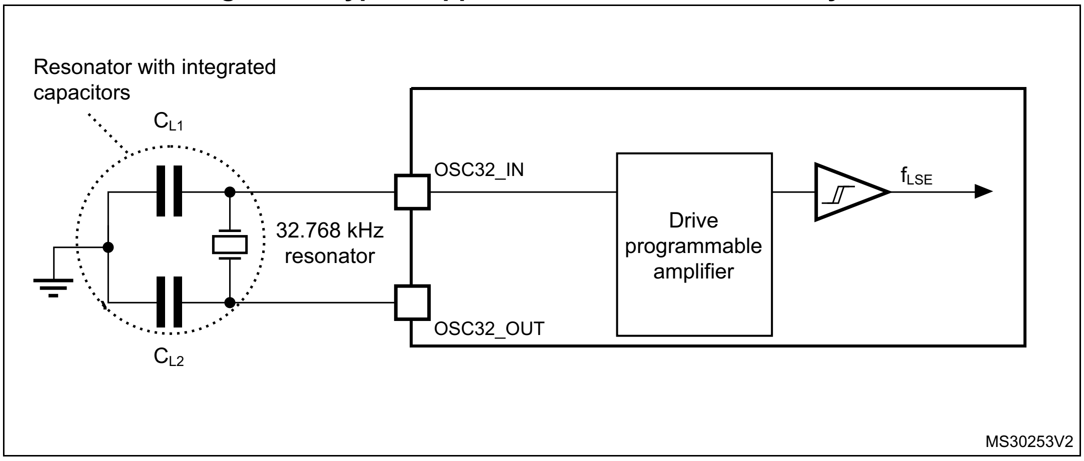
Table 46. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 47* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. The provided curves are characterization results, not tested in production.

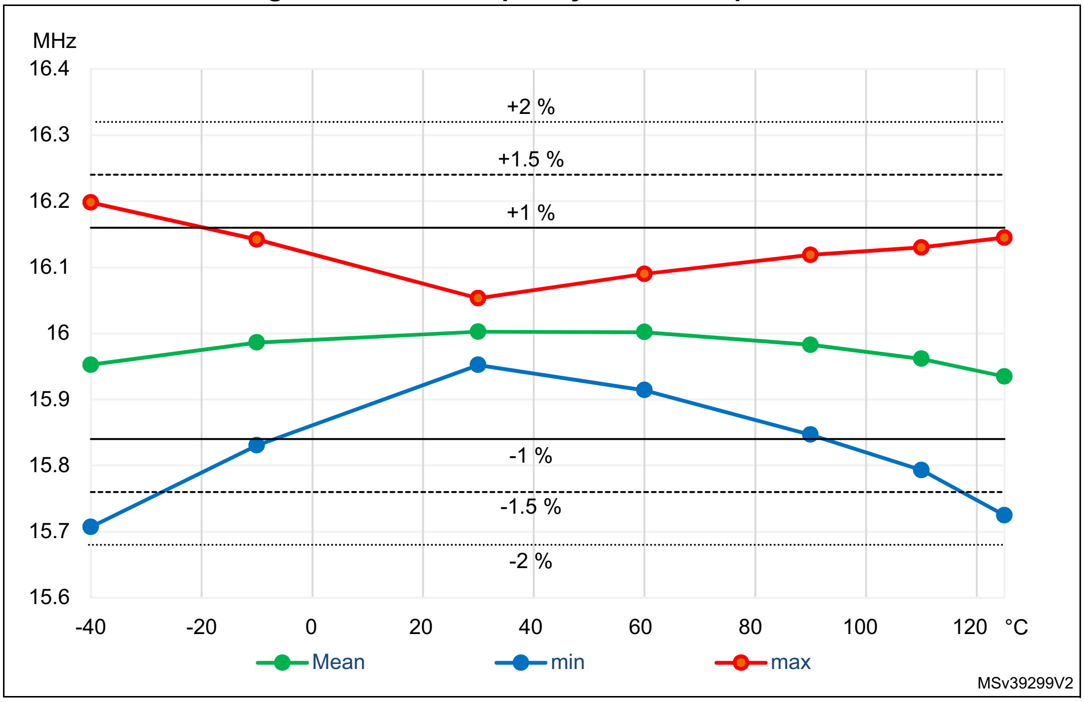
High-speed internal (HSI16) RC oscillator

Table 47. HSI16 oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)[2]	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)[2]	HSI16 oscillator start-up time	-	-	0.8	1.2	μs
t_{stab}(HSI16)[2]	HSI16 oscillator stabilization time	-	-	3	5	μs
I_{DD}(HSI16)[2]	HSI16 oscillator power consumption	-	-	155	190	μA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 19. HSI16 frequency versus temperature



Multi-speed internal (MSI) RC oscillator

Table 48. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}=3 V and T_A=30 °C	MSI mode	Range 0	99	100	101	kHz
			Range 1	198	200	202	
			Range 2	396	400	404	
			Range 3	792	800	808	
			Range 4	0.99	1	1.01	MHz
			Range 5	1.98	2	2.02	
			Range 6	3.96	4	4.04	
			Range 7	7.92	8	8.08	
			Range 8	15.8	16	16.16	
			Range 9	23.8	24	24.4	
			Range 10	31.7	32	32.32	
			Range 11	47.5	48	48.48	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
$\Delta_{TEMP}(MSI)$(2)	MSI oscillator frequency drift over temperature	MSI mode	T_A= -0 to 85 °C	-3.5	-	3	%
			T_A= -40 to 125 °C	-8	-	6	

Table 48. MSI oscillator characteristics[1] (continued)

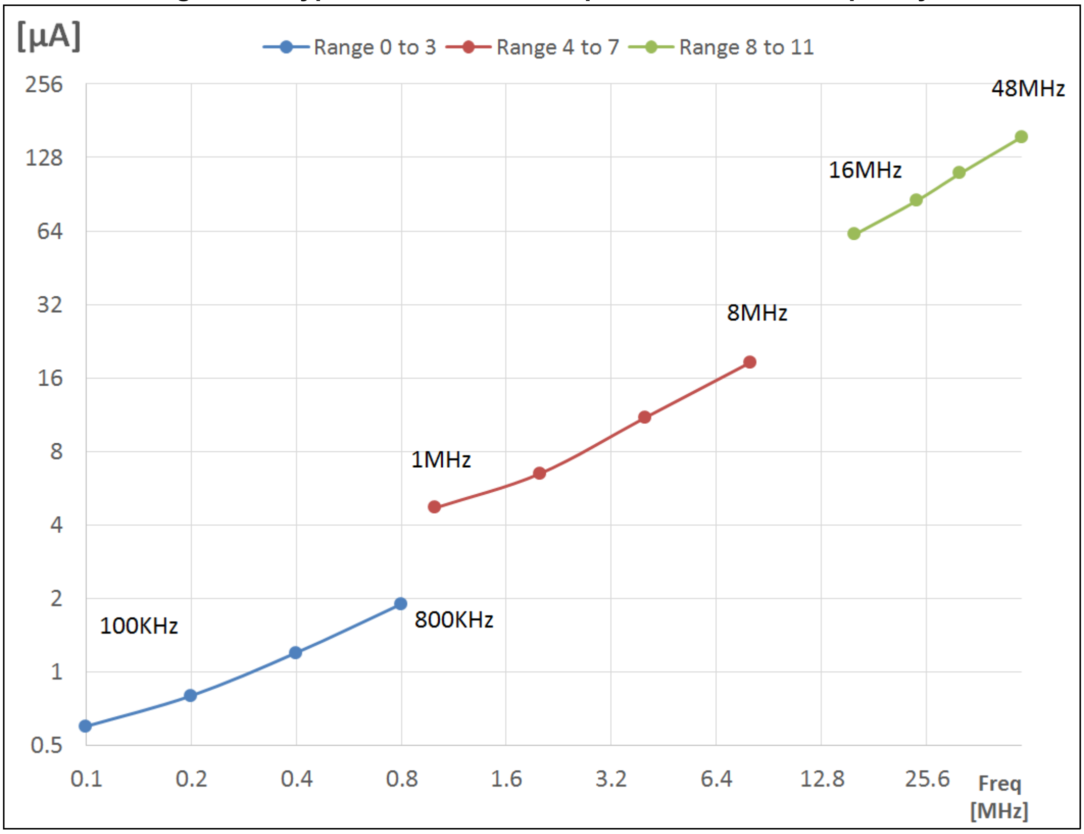
Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta_{VDD}(MSI)$[2]	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD}=1.62 V to 3.6 V	-1.2	-	0.5	%
				V_{DD}=2.4 V to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD}=1.62 V to 3.6 V	-2.5	-	0.7	
				V_{DD}=2.4 V to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD}=1.62 V to 3.6 V	-5	-	1	
				V_{DD}=2.4 V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}$ (MSI)[2][4]	Frequency variation in sampling mode[3]	MSI mode	T_A= -40 to 85 °C		-	1	2	%
			T_A= -40 to 125 °C		-	2	4	
CC jitter(MSI)[4]	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)[4]	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
$t_{SU}(MSI)$[4]	MSI oscillator start-up time	Range 0		-	-	10	20	us
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)$[4]	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

Table 48. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DD}(MSI)$(4)	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	0.6	1	µA
			Range 1	-	0.8	1.2	
			Range 2	-	1.2	1.7	
			Range 3	-	1.9	2.5	
			Range 4	-	4.7	6	
			Range 5	-	6.5	9	
			Range 6	-	11	15	
			Range 7	-	18.5	25	
			Range 8	-	62	80	
			Range 9	-	85	110	
			Range 10	-	110	130	
			Range 11	-	155	190	

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Guaranteed by design.

Figure 20. Typical current consumption versus MSI frequency



Low-speed internal (LSI) RC oscillator

Table 49. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, TA = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI)$(2)	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB}(LSI)$(2)	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD}(LSI)$(2)	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in *Table 50* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 50. PLL, PLLSAI1, PLLSAI2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	4	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	2.0645	-	80	MHz
		Voltage scaling Range 2	2.0645	-	26	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	8	-	80	MHz
		Voltage scaling Range 2	8	-	26	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	8	-	80	MHz
		Voltage scaling Range 2	8	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	64	-	344	MHz
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	-	40	-	±ps
	RMS period jitter		-	30	-	
$I_{DD}(PLL)$	PLL power consumption on V_{DD}(1)	VCO freq = 64 MHz	-	150	200	µA
		VCO freq = 96 MHz	-	200	260	
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.

2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

6.3.10 Flash memory characteristics

Table 51. Flash memory characteristics[1]

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.69	90.76	µs
t_{prog_row}	one row (32 double word) programming time	normal programming	2.61	2.90	ms
		fast programming	1.91	2.12	
t_{prog_page}	one page (2 Kbyte) programming time	normal programming	20.91	23.24	
		fast programming	15.29	16.98	
t_{ERASE}	Page (2 KB) erase time	-	22.02	24.47	
t_{prog_bank}	one bank (512 Kbyte) programming time	normal programming	5.35	5.95	s
		fast programming	3.91	4.35	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.59	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 2 µs)	-	
		Erase mode	7 (for 41 µs)	-	

1. Guaranteed by design.

Table 52. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min[1]	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	30	Years
		1 kcycle[2] at T_A = 105 °C	15	
		1 kcycle[2] at T_A = 125 °C	7	
		10 kcycles[2] at T_A = 55 °C	30	
		10 kcycles[2] at T_A = 85 °C	15	
		10 kcycles[2] at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 53*. They are based on the EMS levels and classes defined in application note AN1709.

Table 53. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 80 MHz, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 80 MHz, conforming to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 54. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				f_{MSI} = 24 MHz	8 MHz/ 80 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP144 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	-9	2	dBµV
			30 MHz to 130 MHz	-8	3	
			130 MHz to 1 GHz	-10	14	
			EMI Level	1.5	3.5	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 55. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 56. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A(1)

1. Negative injection is limited to -30 mA for PF0, PF1, PG6, PG7, PG8, PG12, PG13, PG14.

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 57*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 57. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	-0	NA(1)	mA
	Injected current on pins except PA4, PA5, BOOT0	-5	NA(1)	
	Injected current on PA4, PA5 pins	-5	0	

1. NA: not applicable

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the conditions summarized in *Table 22: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 58. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	0.3xV_{DDIOx} (2)	V
	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	0.39xV_{DDIOx}-0.06 (3)	
	I/O input low level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	-	-	0.43xV_{DDIOx}-0.1 (3)	
	BOOT0 I/O input low level voltage	1.62 V<V_{DDIOx}<3.6 V	-	-	0.17xV_{DDIOx} (3)	
V_{IH}(1)	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.7xV_{DDIOx} (2)	-	-	V
	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.49xV_{DDIOX}+0.26 (3)	-	-	
	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	0.61xV_{DDIOX}+0.05 (3)	-	-	
	BOOT0 I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	0.77xV_{DDIOX} (3)	-	-	
V_{hys}(3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	150	-	
	BOOT0 I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	

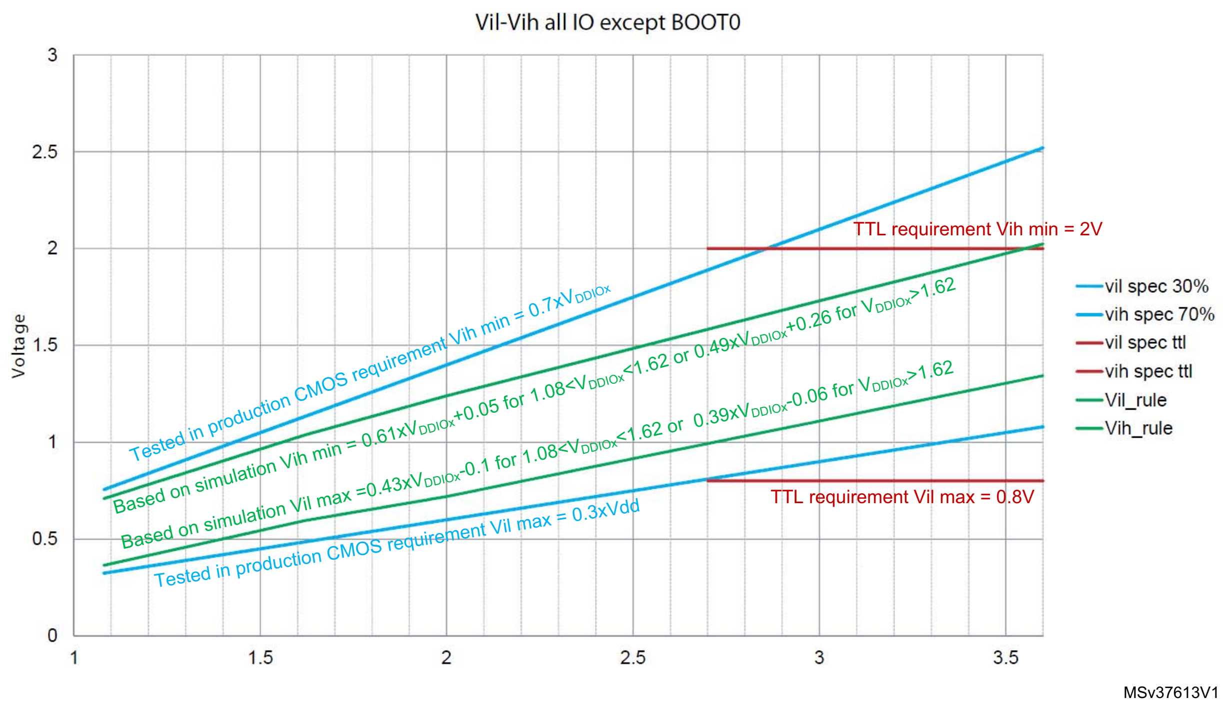
Table 58. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	FT_xx input leakage current(3)	$V_{IN} \leq Max(V_{DDXXX})$(4)	-	-	±100	nA
		$Max(V_{DDXXX}) \leq V_{IN} \leq Max(V_{DDXXX})+1$ V(4)(5)	-	-	650(3)(6)	
		$Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(3)(5)	-	-	200(6)	
	FT_lu, FT_u and PC3 IO	$V_{IN} \leq Max(V_{DDXXX})$ (4)	-	-	±150	
		$Max(V_{DDXXX}) \leq V_{IN} \leq Max(V_{DDXXX})+1$ V(4)	-	-	2500(3)(7)	
		$Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(4)(5)(7)	-	-	250(7)	
	TT_xx input leakage current	$V_{IN} \leq Max(V_{DDXXX})$(6)	-	-	±150	
		$Max(V_{DDXXX}) \leq V_{IN} <$ 3.6 V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current (UFBGA132 only)	T_J = 75 °C	-	-	1	
R_{PU}	Weak pull-up equivalent resistor (8)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(8)	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to *Figure 21: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. $Max(V_{DDXXX})$ is the maximum value of all the I/O supplies. Refer to *Table: Legend/Abbreviations used in the pinout table.*
5. All TX_xx IO except FT_lu, FT_u and PC3.
6. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x $I_{lkg}(Max)$.
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, V_{DDIO2}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 21* for standard I/Os, and in *Figure 21* for 5 V tolerant I/Os.

Figure 21. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 19: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 19: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 59. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\| = 8$ mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\| = 8$ mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\| = 20$ mA $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\| = 4$ mA $V_{DDIOx} \geq 1.62$ V	-	0.45	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-0.45	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\| = 2$ mA 1.62 V $\geq V_{DDIOx} \geq$ 1.08 V	-	0.35xV_{DDIOx}	
V_{OH}(3)	Output high level voltage for an I/O pin		0.65xV_{DDIOx}	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\| = 20$ mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\| = 10$ mA $V_{DDIOx} \geq 1.62$ V	-	0.4	
		$\|I_{IO}\| = 2$ mA 1.62 V $\geq V_{DDIOx} \geq$ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 19: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 22* and *Table 60*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 60. I/O AC characteristics(1)(2)

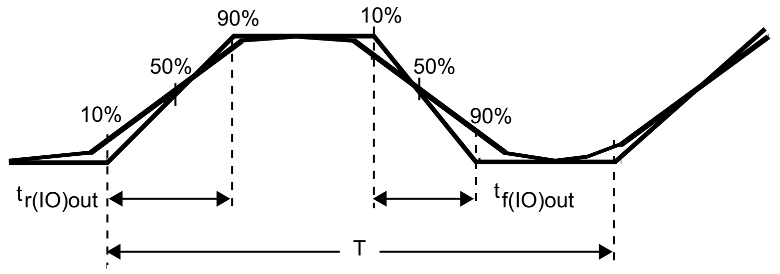
Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	140	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	110	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	40	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	21	

Table 60. I/O AC characteristics[1][2] (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100[3]	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	28	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120[3]	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180[3]	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time[4]		-	5	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0392 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

Figure 22. I/O AC characteristics definition(1)



1. Refer to *Table 60: I/O AC characteristics*.

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

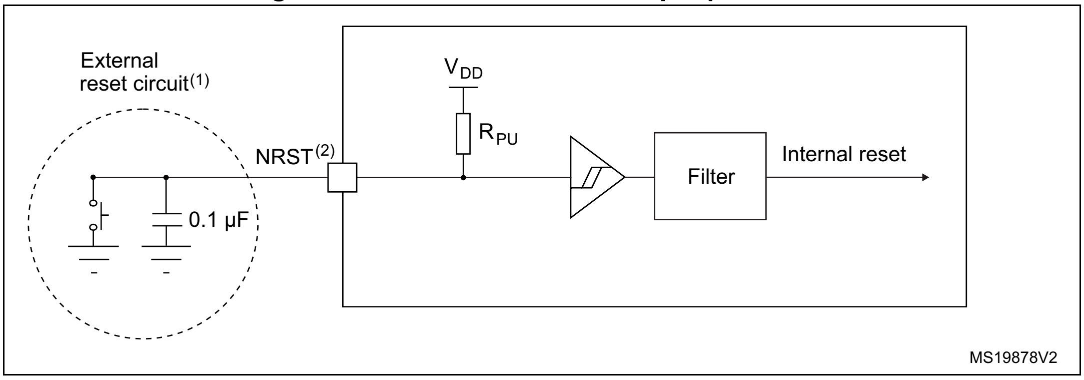
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 61. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3_x V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7_x V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 23. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 61: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

6.3.16 Analog switches booster

Table 62. Analog switches booster characteristics[1]

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
V_{BOOST}	Boost supply	2.7	-	4	
$t_{SU(BOOST)}$	Booster startup time	-	-	240	μs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	μA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

6.3.17 Analog-to-Digital converter characteristics

Unless otherwise specified, the parameters given in *Table 63* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 22: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 63. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	-	-	80	MHz
		Range 2	-	-	26	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	Msps
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	f_{ADC} = 80 MHz Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{AIN} (3)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	1.45			µs
		-	116			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	

Table 63. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
$I_{DDA}(ADC)$	ADC consumption from the V_{DDA} supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
$I_{DDV\_S}(ADC)$	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
$I_{DDV\_D}(ADC)$	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 64. Maximum ADC RAIN(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	RAIN max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000

Table 64. Maximum ADC RAIN(1)(2) (continued)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	RAIN max (Ω)	
			Fast channels(3)	Slow channels(4)
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

1. Guaranteed by design.
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0, PA1.
4. Slow channels are: all ADC inputs except the fast channels.

Table 65. ADC accuracy - limited test conditions 1(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 65. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)

<table>
<tr><th>Sym-bol</th><th>Parameter</th><th colspan="3">Conditions(4)</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="4">THD</td><td rowspan="4">Total harmonic distortion</td><td rowspan="4">ADC clock frequency ≤ 80 MHz,
Sampling rate ≤ 5.33 Msps,
$V_{DDA} = V_{REF+} = 3$ V,
TA = 25 °C</td><td rowspan="2">Single ended</td><td>Fast channel (max speed)</td><td>-</td><td>-74</td><td>-73</td><td rowspan="4">dB</td></tr>
<tr><td>Slow channel (max speed)</td><td>-</td><td>-74</td><td>-73</td></tr>
<tr><td rowspan="2">Differential</td><td>Fast channel (max speed)</td><td>-</td><td>-79</td><td>-76</td></tr>
<tr><td>Slow channel (max speed)</td><td>-</td><td>-79</td><td>-76</td></tr>
</table>

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 66. ADC accuracy - limited test conditions 2[(1)(2)(3)]

Sym-bol	Parameter	Conditions[(4)]			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	4	6.5	LSB
				Slow channel (max speed)	-	4	6.5	
			Differential	Fast channel (max speed)	-	3.5	5.5	
				Slow channel (max speed)	-	3.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	4.5	
				Slow channel (max speed)	-	1	5	
			Differential	Fast channel (max speed)	-	1.5	3	
				Slow channel (max speed)	-	1.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	2.5	6	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	3.5	
				Slow channel (max speed)	-	1.5	3.5	
			Differential	Fast channel (max speed)	-	1	3	
				Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.5	-	bits
				Slow channel (max speed)	10	10.5	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65	-	dB
				Slow channel (max speed)	62	65	-	
			Differential	Fast channel (max speed)	66	67.4	-	
				Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66	-	
				Slow channel (max speed)	64	66	-	
			Differential	Fast channel (max speed)	66.5	68	-	
				Slow channel (max speed)	66.5	68	-	

Table 66. ADC accuracy - limited test conditions 2(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $2\ V \leq V_{DDA}$	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
			Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 67. ADC accuracy - limited test conditions 3[(1)(2)(3)]

Sym-bol	Parameter	Conditions[(4)]			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 67. ADC accuracy - limited test conditions 3(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $1.65\ V \leq V_{DDA} = V_{REF+} \leq 3.6\ V$, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 68. ADC accuracy - limited test conditions 4(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	5	5.4	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	4	5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	4	
				Slow channel (max speed)	-	2	4	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2	3.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	4	4.5	
				Slow channel (max speed)	-	4	4.5	
			Differential	Fast channel (max speed)	-	3	4	
				Slow channel (max speed)	-	3	4	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	3	
				Slow channel (max speed)	-	2.5	3	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.2	10.5	-	bits
				Slow channel (max speed)	10.2	10.5	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	63	65	-	dB
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	65	-	
				Slow channel (max speed)	64	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 68. ADC accuracy - limited test conditions 4[1][2][3] (continued)

Sym-bol	Parameter	Conditions[4]			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Figure 24. ADC accuracy characteristics

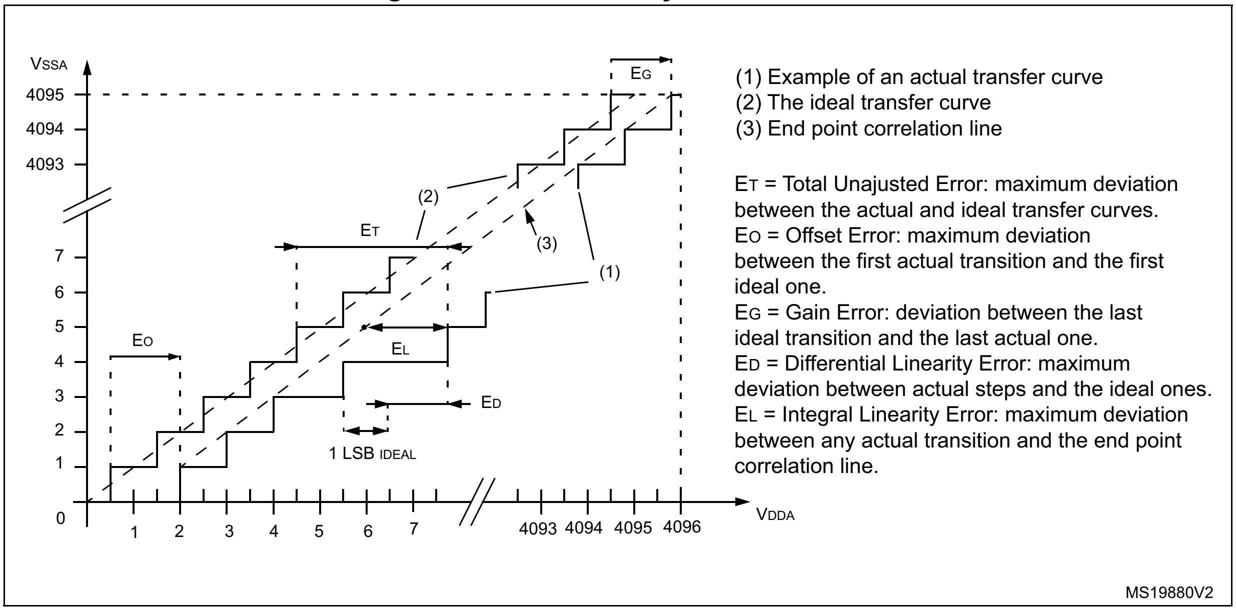
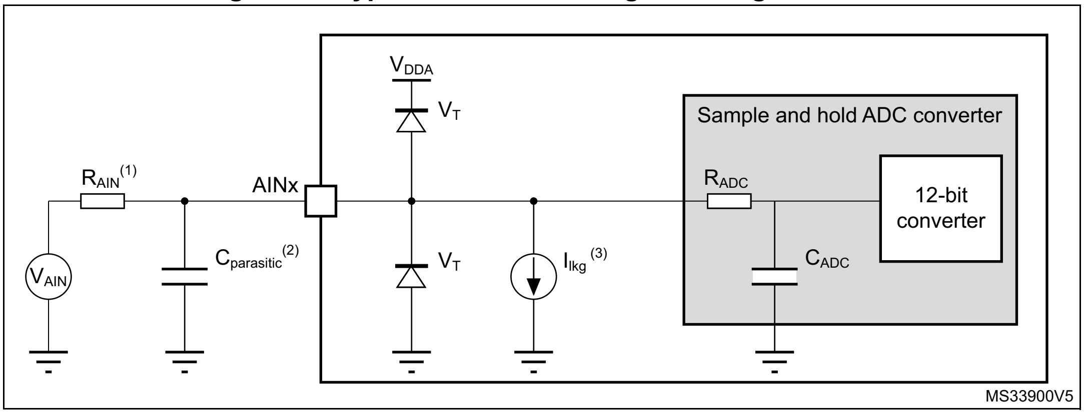


Figure 25. Typical connection diagram using the ADC



1. Refer to *Table 63: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 58: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 58: I/O static characteristics* for the values of I_{lkg}.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 12: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.18 Digital-to-Analog converter characteristics

Table 69. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	-		1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-		1.8	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-		V_{SSA}			V
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

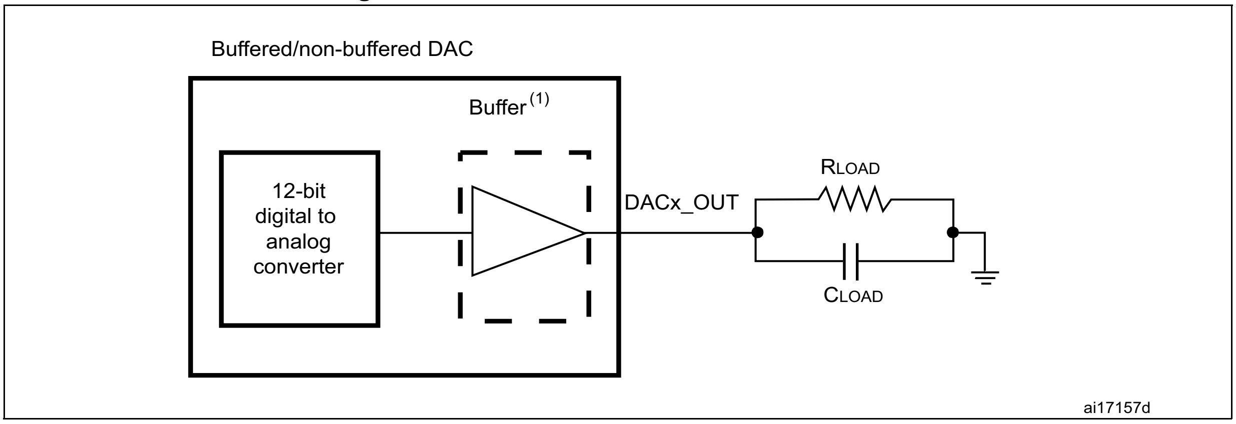
Table 69. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x Ton/(Ton +Toff) (4)	400 x Ton/(Ton +Toff) (4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x Ton/(Ton +Toff) (4)	205 x Ton/(Ton +Toff) (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

3. Refer to *Table 58: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to RM0392 reference manual for more details.

Figure 26. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 70. DAC accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	

Table 70. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain	Gain error(5)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL	-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL	-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz	-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz	-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	-79	-	
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

6.3.19 Voltage reference buffer characteristics

Table 71. VREFBUF characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V
			V_{RS} = 1	2.8	-	3.6	
		Degraded mode[2]	V_{RS} = 0	1.65	-	2.4	
			V_{RS} = 1	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	V_{RS} = 0	2.046[3]	2.048	2.049[3]	
			V_{RS} = 1	2.498[3]	2.5	2.502[3]	
		Degraded mode[2]	V_{RS} = 0	V_{DDA}-150 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent Serial Resistor of Cload	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < TJ < +125 °C		-	-	$T_{coeff\_vrefint}$ + 50	ppm/ °C
		0 °C < TJ < +50 °C		-	-	$T_{coeff\_vrefint}$ + 50	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF[4]		-	300	350	µs
		CL = 1.1 µF[4]		-	500	650	
		CL = 1.5 µF[4]		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase[5]	-	-	-	8	-	mA

Table 71. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREF BUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

6.3.20 Comparator characteristics

Table 72. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			V
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	0.55	0.9	µs
			$V_{DDA} < 2.7$ V	-	0.65	1	
		Ultra-low-power mode		-	5	12	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 25: Embedded internal voltage reference*.
3. Guaranteed by characterization results.

6.3.21 Operational amplifiers characteristics

Table 73. OPAMP characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage[2]	-		1.8	-	3.6	V
CMIR	Common mode input range	-		0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	25 °C, No Load on output.		-	-	±1.5	mV
		All voltage/Temp.		-	-	±3	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode		-	±5	-	μV/°C
		Low-power mode		-	±10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-		-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-		-	1	1.35	
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	μA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	

Table 73. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PSRR	Power supply rejection ratio	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ DC	70	85	-	dB
		Low-power mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	V_{DDA} ≥ 2.4 V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	V_{DDA} < 2.4 V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(3)	Slew rate (from 10 and 90% of output voltage)	Normal mode	V_{DDA} ≥ 2.4 V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	V_{DDA} < 2.4 V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(3)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(3)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ follower configuration	-	5	10	µs
		Low-power mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	Dedicated input (BGA132 only)		-	-	-(4)	nA
		General purpose input (all packages except BGA132)		-	-	-(4)	
PGA gain(3)	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	

Table 73. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{network}$	R2/R1 internal resistance values in PGA mode(5)	PGA Gain = 2		-	80/80	-	kΩ/kΩ
		PGA Gain = 4		-	120/ 40	-	
		PGA Gain = 8		-	140/ 20	-	
		PGA Gain = 16		-	150/ 10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/ 2	-	MHz
		Gain = 4	-	-	GBW/ 4	-	
		Gain = 8	-	-	GBW/ 8	-	
		Gain = 16	-	-	GBW/ 16	-	
en	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	-	500	-	nV/√Hz
		Low-power mode	at 1 kHz, Output loaded with 20 kΩ	-	600	-	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	-	180	-	
		Low-power mode	at 10 kHz, Output loaded with 20 kΩ	-	290	-	
I_{DDA}(OPAMP)(3)	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode	-	120	260	µA
		Low-power mode		-	45	100	

1. Guaranteed by design, unless otherwise specified.
2. The temperature range is limited to 0 °C-125 °C when V_{DDA} is below 2 V
3. Guaranteed by characterization results.
4. Mostly I/O leakage, when used in analog mode. Refer to I_{lkg} parameter in *Table 58: I/O static characteristics*.
5. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1

6.3.22 Temperature sensor characteristics

Table 74. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(3)	0.742	0.76	0.785	V
t_{START} (TS_BUF)(1)	Sensor Buffer Start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 8: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.23 V_{BAT} monitoring characteristics

Table 75. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 76. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.24 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 77* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x VDD

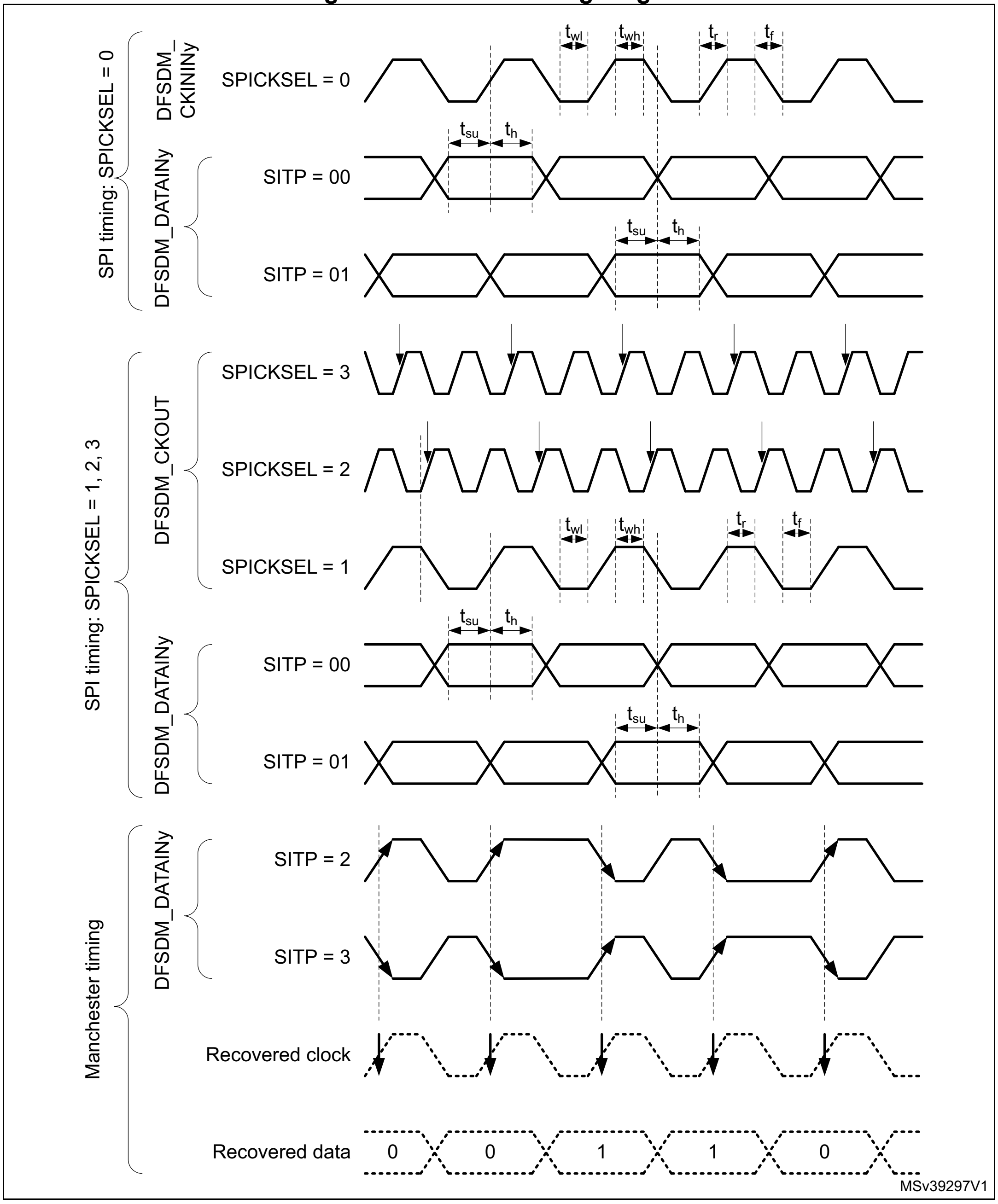
Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM_CKINy, DFSDM_DATINy, DFSDM_CKOUT for DFSDM).

Table 77. DFSDM characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	-	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 01)	-	-	20 ($f_{DFSDMCLK}/4$)	MHz
f_{CKOUT}	Output clock frequency	-	-	-	20	MHz
$DuCy_{CKOUT}$	Output clock frequency duty cycle	-	45	50	55	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)	$T_{CKIN}/2$-0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	0	-	-	ns
t_h	Data input hold time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	2	-	-	ns
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0)	(CKOUT DIV+1) x $T_{DFSDMCLK}$	-	(2 x CKOUTDIV) x $T_{DFSDMCLK}$	ns

1. Data based on characterization results, not tested in production.

Figure 16: DFSDM timing diagram



6.3.25 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 78. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	12.5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 80 MHz	0	40	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	0.0125	819.2	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	-	53.68	s

1. TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 79. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 80. WWDG min/max timeout value at 80 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0512	3.2768	ms
2	1	0.1024	6.5536	
4	2	0.2048	13.1072	
8	3	0.4096	26.2144	

6.3.26 Communication interfaces characteristics

I^2C interface characteristics

The I2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0392 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 81. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in *Table 82* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 22: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 82. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode receiver/full duplex $2.7 < V_{DD} < 3.6$ V Voltage Range 1	-	-	24	MHz
		Master mode receiver/full duplex $1.71 < V_{DD} < 3.6$ V Voltage Range 1			13	
		Master mode transmitter $1.71 < V_{DD} < 3.6$ V Voltage Range 1			40	
		Slave mode receiver $1.71 < V_{DD} < 3.6$ V Voltage Range 1			40	
		Slave mode transmitter/full duplex $2.7 < V_{DD} < 3.6$ V Voltage Range 1			26(2)	
		Slave mode transmitter/full duplex $1.71 < V_{DD} < 3.6$ V Voltage Range 1			16(2)	
		Voltage Range 2			13	
		$1.08 < V_{DDIO2} < 1.32$ V(3)			8	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	$4 \times T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	$2 \times T_{PCLK}$	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	$T_{PCLK}-2$	T_{PCLK}	$T_{PCLK}+2$	ns
$t_{su(MI)}$	Data input setup time	Master mode	3.5	-	-	ns
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	ns
$t_{h(SI)}$		Slave mode	3	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	36	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns

Table 82. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 < V_{DD} < 3.6 V Voltage Range 1	-	12.5	19	ns
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 1	-	12.5	30	
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 2	-	12.5	33	
-		Slave mode 1.08 < V_{DDIO2} < 1.32 V(3)	-	25	62.5	
$t_{v(MO)}$		Master mode	-	2.5	12.5	
$t_{h(SO)}$	Data output hold time	Slave mode	9	-	-	ns
-		Slave mode 1.08 < V_{DDIO2} < 1.32 V(3)	24	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.
3. SPI mapped on Port G.

Figure 27. SPI timing diagram - slave mode and CPHA = 0

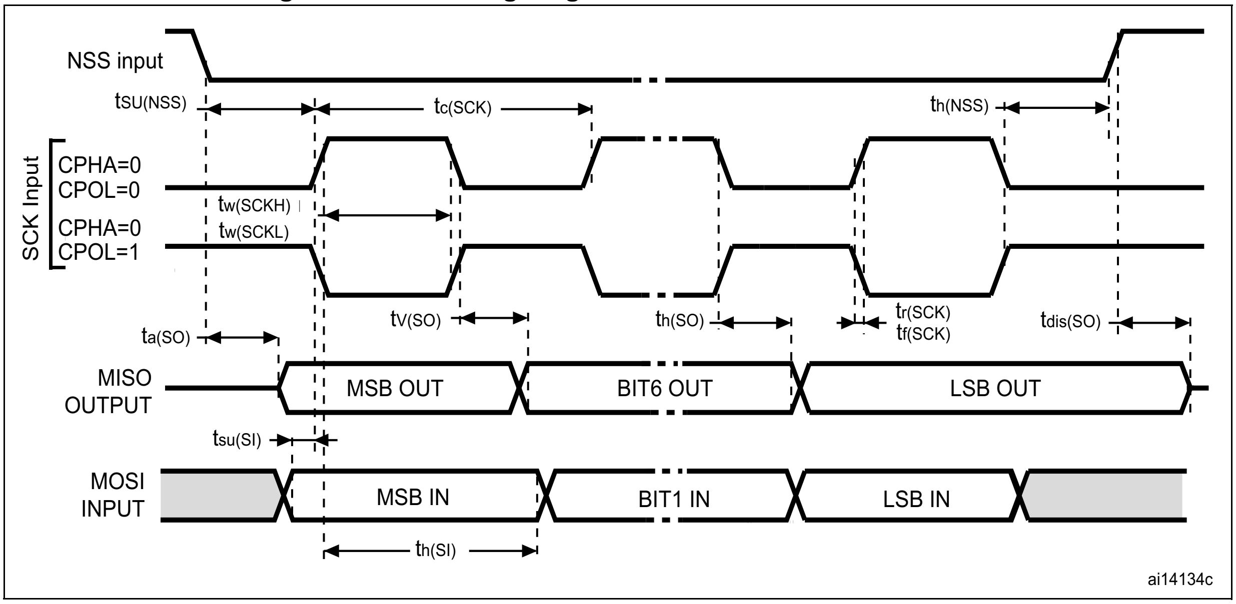
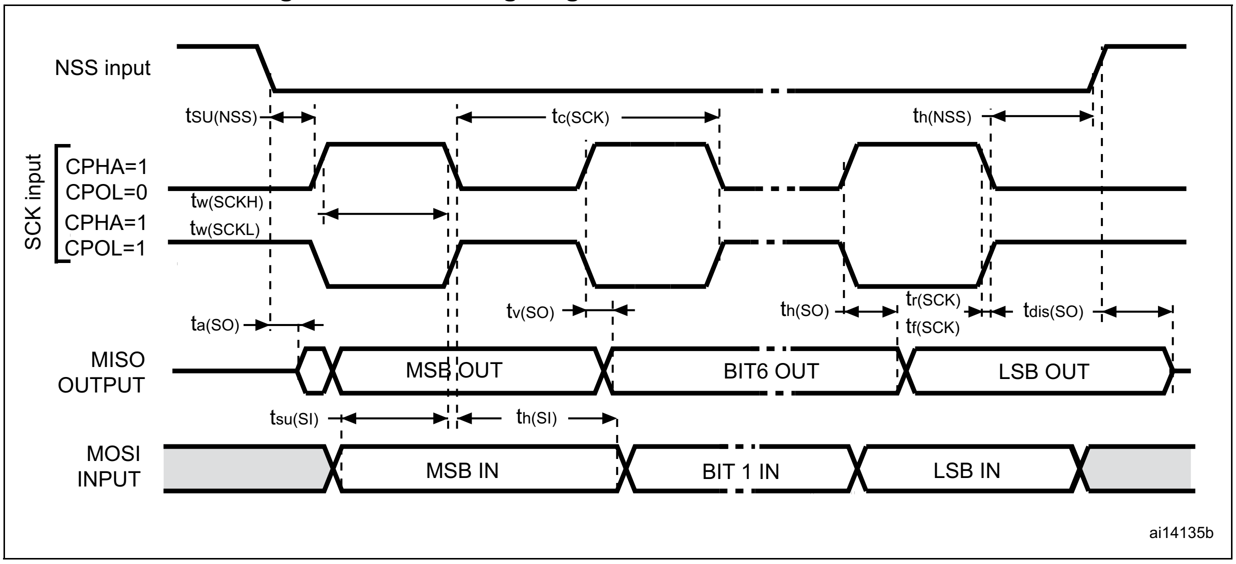
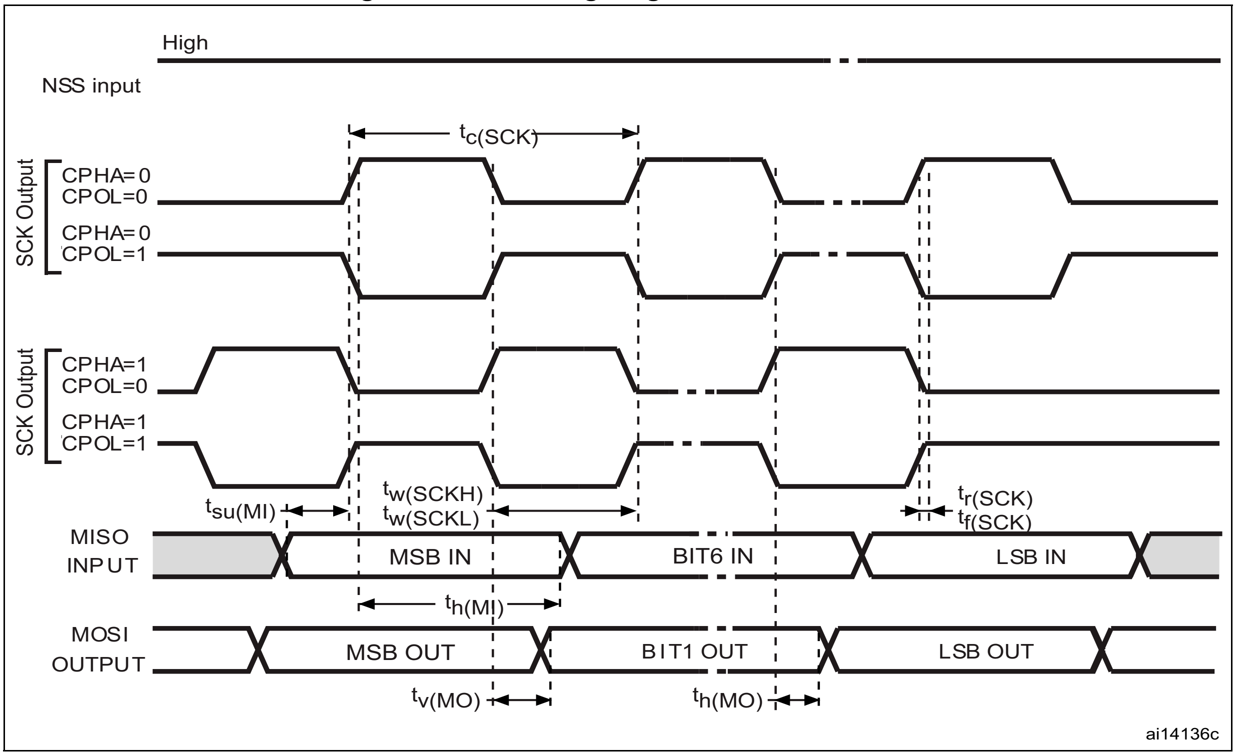


Figure 28. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 29. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Quad SPI characteristics

Unless otherwise specified, the parameters given in *Table 83* and *Table 84* for Quad SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 15 or 20 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 83. Quad SPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 < V_{DD}< 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		1.71 < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		2.7 < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	60	
		1.71 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK}= 48 MHz, presc=0	$t_{(CK)}/2-2$	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2+2$	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	4	-	-	
		Voltage Range 2	3.5	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	5.5	-	-	
		Voltage Range 2	6.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	2.5	5	
		Voltage Range 2	-	3	5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	1.5	-	-	
		Voltage Range 2	2	-	-	

1. Guaranteed by characterization results.

Table 84. QUADSPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		2 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	48	
		1.71 < V_{DD} < 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		1.71 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK} = 48 MHz, presc=0	$t_{(CK)}/2$-2	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2$+2	
$t_{sf(IN)}$;$t_{sr(IN)}$	Data input setup time	Voltage Range 1 and 2	3.5	-	-	
$t_{hf(IN)}$; $t_{hr(IN)}$	Data input hold time		6.5	-	-	
$t_{vf(OUT)}$;$t_{vr(OUT)}$	Data output valid time	Voltage Range 1	-	11	12	
		Voltage Range 2		15	19	
$t_{hf(OUT)}$; $t_{hr(OUT)}$	Data output hold time	Voltage Range 1	6	-	-	
		Voltage Range 2	8	-		

1. Guaranteed by characterization results.

Figure 30. Quad SPI timing diagram - SDR mode

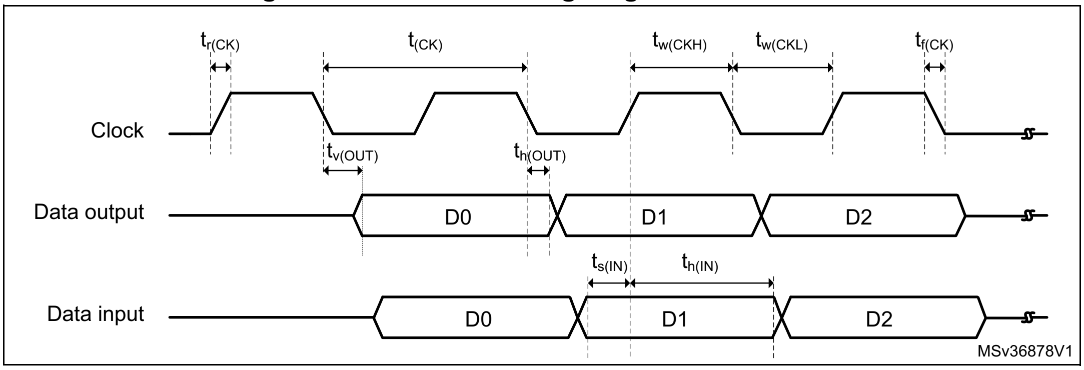
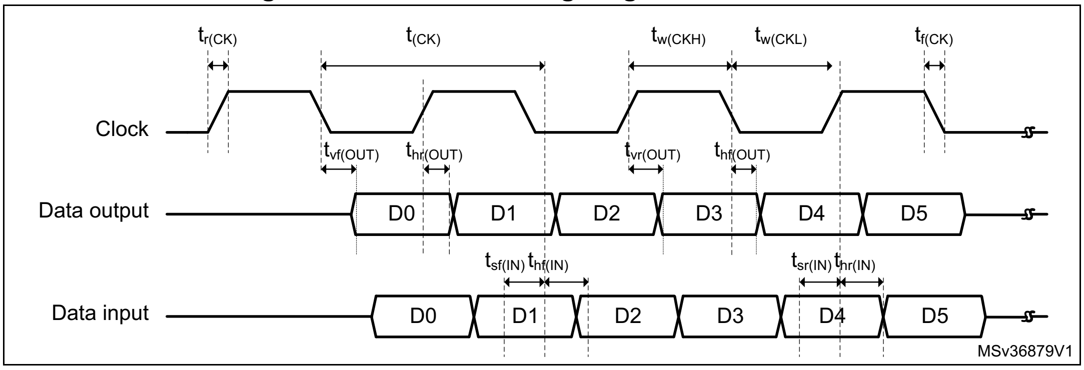


Figure 31. Quad SPI timing diagram - DDR mode



SAI characteristics

Unless otherwise specified, the parameters given in *Table 85* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 85. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter $2.7 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	18.5	MHz
		Master transmitter $1.71 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	12.5	
		Master receiver Voltage Range 1	-	25	
		Slave transmitter $2.7 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	22.5	
		Slave transmitter $1.71 \leq V_{DD} \leq 3.6$ Voltage Range 1	-	14.5	
		Slave receiver Voltage Range 1	-	25	
		Voltage Range 2	-	12.5	
$t_{v(FS)}$	FS valid time	Master mode $2.7 \leq V_{DD} \leq 3.6$	-	22	ns
		Master mode $1.71 \leq V_{DD} \leq 3.6$	-	40	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	1	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	2	-	ns
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	2.5	-	ns
$t_{su(SD\_B\_SR)}$		Slave receiver	3	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	8	-	ns
$t_{h(SD\_B\_SR)}$		Slave receiver	4	-	

Table 85. SAI characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) $2.7 \leq V_{DD} \leq 3.6$	-	22	ns
		Slave transmitter (after enable edge) $1.71 \leq V_{DD} \leq 3.6$	-	34	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	ns
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) $2.7 \leq V_{DD} \leq 3.6$	-	27	ns
		Master transmitter (after enable edge) $1.71 \leq V_{DD} \leq 3.6$	-	40	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	ns

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 32. SAI master timing waveforms

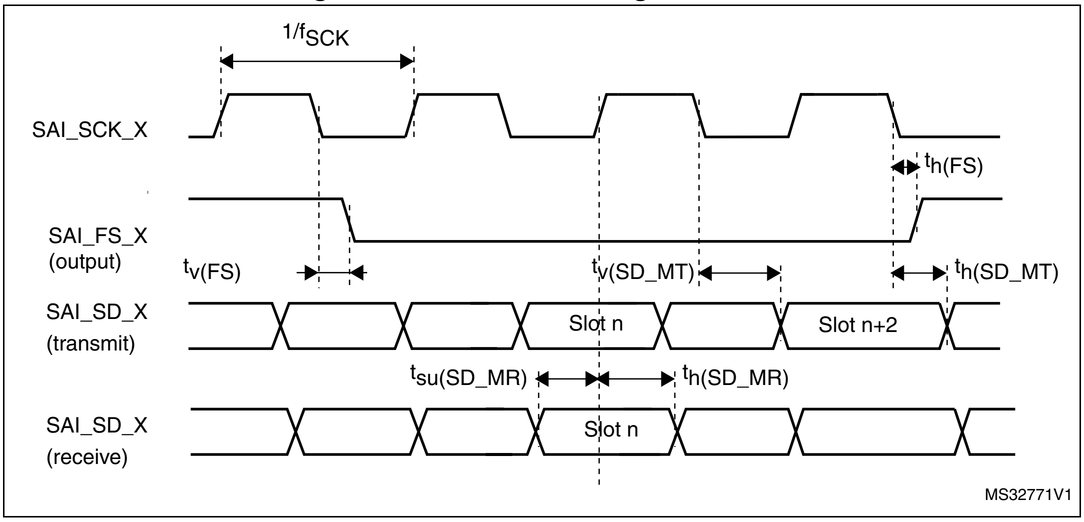
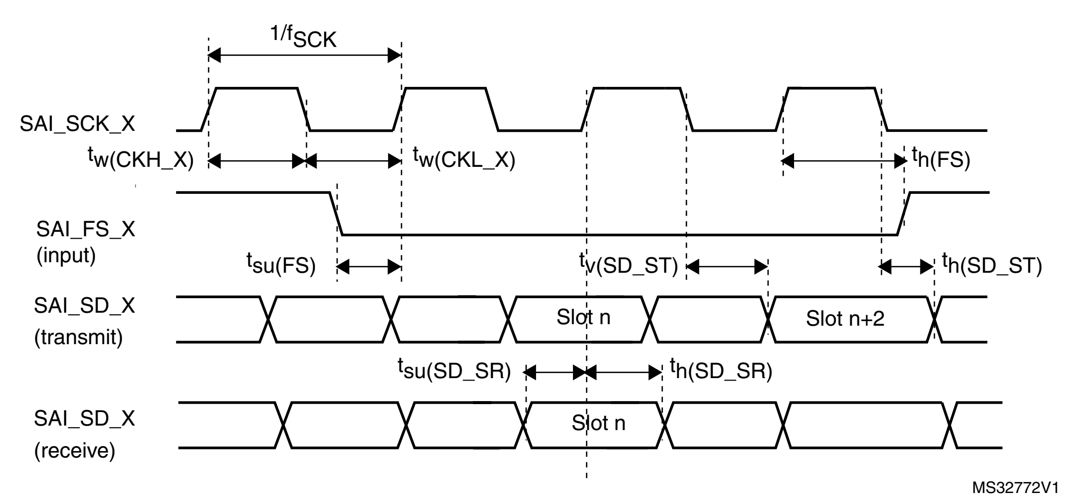


Figure 33. SAI slave timing waveforms



SDMMC characteristics

Unless otherwise specified, the parameters given in *Table 86* for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Table 86. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	2	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	4.5	-	-	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	12	14	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	9	-	-	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} = 50 MHz	2	-	-	ns
t_{IHD}	Input hold time SD	f_{PP} = 50 MHz	4.5	-	-	ns

Table 86. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V[(1)] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} = 50 MHz	-	4.5	5	ns
t_{OHD}	Output hold default time SD	f_{PP} = 50 MHz	0	-	-	ns

1. Guaranteed by characterization results.

Table 87. eMMC dynamic characteristics, V_{DD} = 1.71 V to 1.9 V[(1)(2)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	0	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	5	-	-	ns
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	13.5	15.5	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	9	-	-	ns

1. Guaranteed by characterization results.
2. C_{LOAD} = 20pF.

Figure 34. SDIO high-speed mode

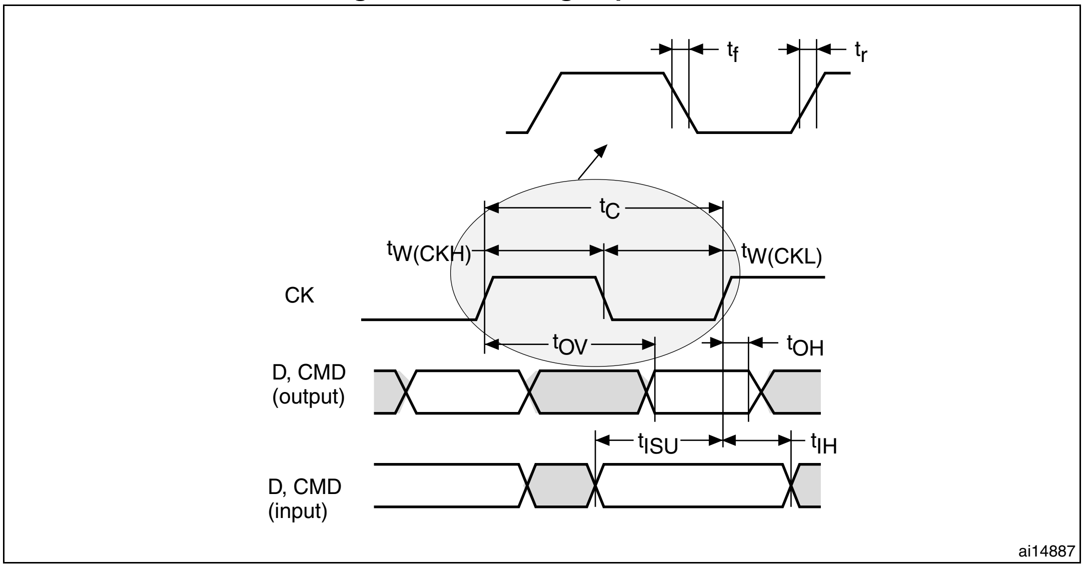
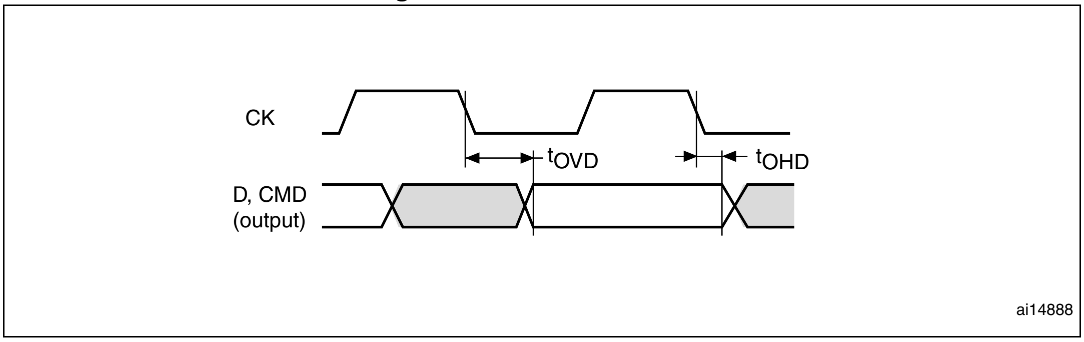


Figure 35. SD default mode



CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.27 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 88* to *Table 101* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 36 through *Figure 39* represent asynchronous waveforms and *Table 88* through *Table 95* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the THCLK is the HCLK clock period.

Figure 36. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

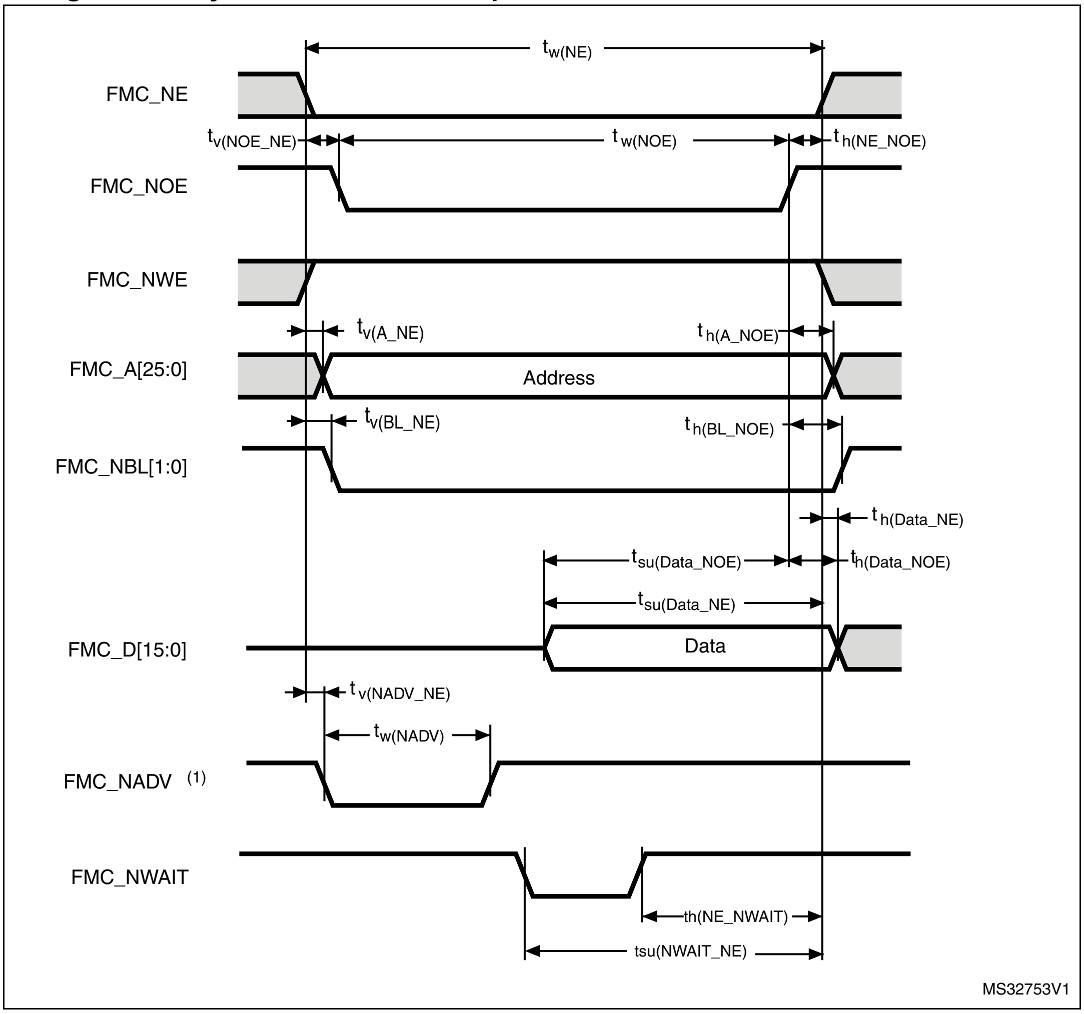


Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK}$-0.5	$2T_{HCLK}$+0.5	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}$-0.5	$2T_{HCLK}$+1	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	T_{HCLK}-1	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	T_{HCLK}-0.5	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	1	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+0.5	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{HCLK}$-0.5	$7T_{HCLK}$+0.5	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK}$-0.5	$5T_{HCLK}$+0.5	
$t_{w(NWAIT)}$	FMC_NWAIT low time	T_{HCLK}-0.5	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}$+2	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 37. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

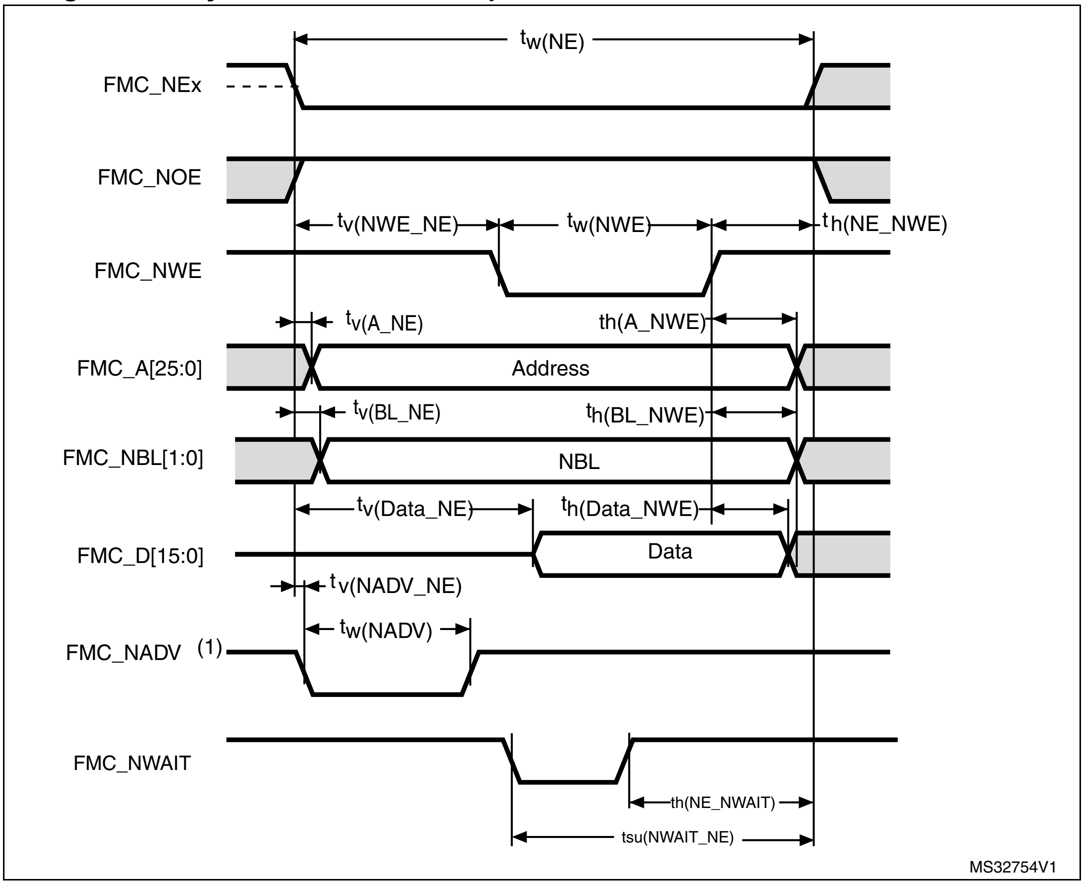


Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$-1	$3T_{HCLK}$+2	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-0.5	T_{HCLK}+1.5	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}-1	T_{HCLK}+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}-1	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK}-0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	T_{HCLK}+4	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK}+1	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	1	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+0.5	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}$+0.5	$8T_{HCLK}$+0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK}$-0.5	$6T_{HCLK}$+0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}$+2	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$+2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 38. Asynchronous multiplexed PSRAM/NOR read waveforms

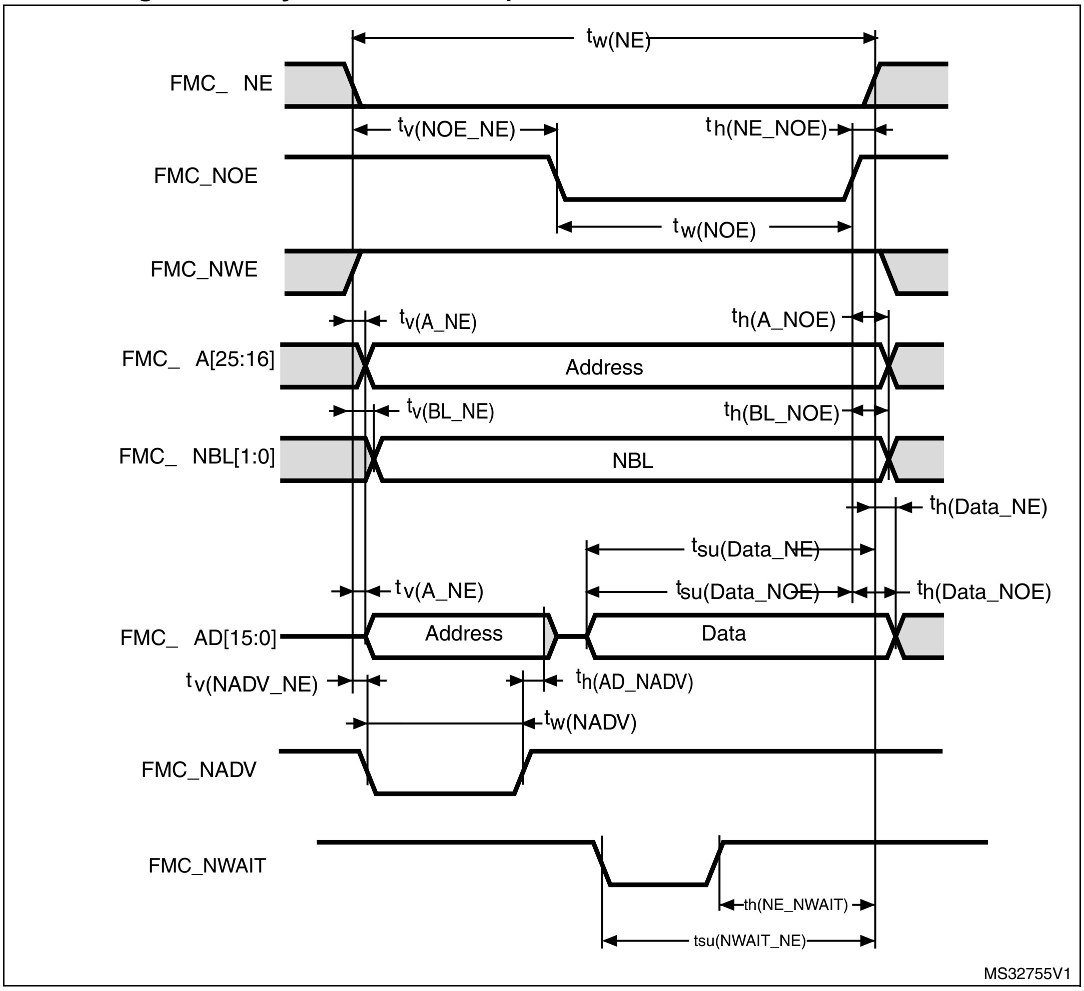


Table 92. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$-0.5	$3T_{HCLK}$+2	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK}$-0.5	$2T_{HCLK}$+0.5	
$t_{w(NOE)}$	FMC_NOE low time	T_{HCLK}+0.5	T_{HCLK}+1	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	0	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	T_{HCLK}-0.5	-	
$t_{h(BL\_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	T_{HCLK}-2	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	T_{HCLK}-1	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 93. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}$+2	$8T_{HCLK}$+4	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK}$-1	$5T_{HCLK}$+1.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}$+1.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$+1	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 39. Asynchronous multiplexed PSRAM/NOR write waveforms

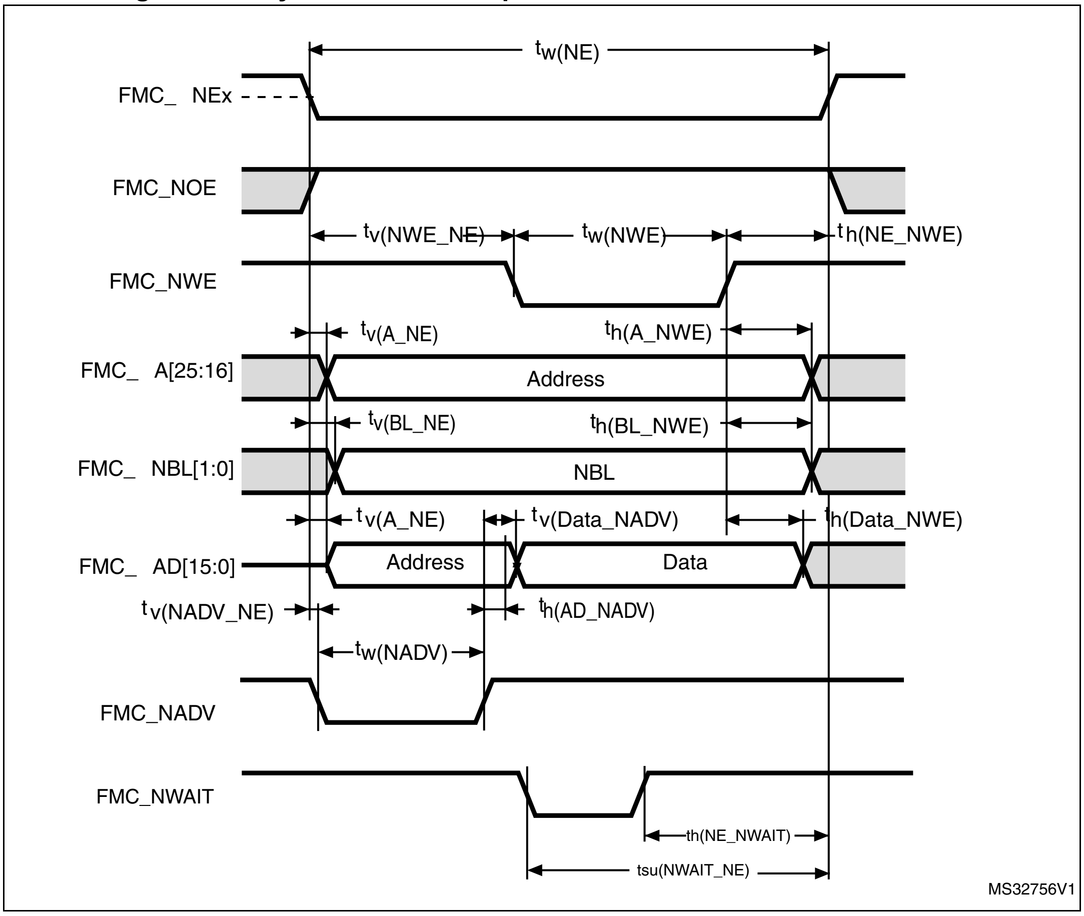


Table 94. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$-0.5	$4T_{HCLK}$+2	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{w(NWE)}$	FMC_NWE low time	$2xT_{HCLK}$-1.5	$2xT_{HCLK}$+1.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high	T_{HCLK}-2	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}-1	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK}+0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	T_{HCLK} +4	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK} +0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 95. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$-0.5	$9T_{HCLK}$+2	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$-1.5	$7T_{HCLK}$+1.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}$+2	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$-3	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 40 through *Figure 43* represent synchronous waveforms and *Table 96* through *Table 99* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 40. Synchronous multiplexed NOR/PSRAM read timings

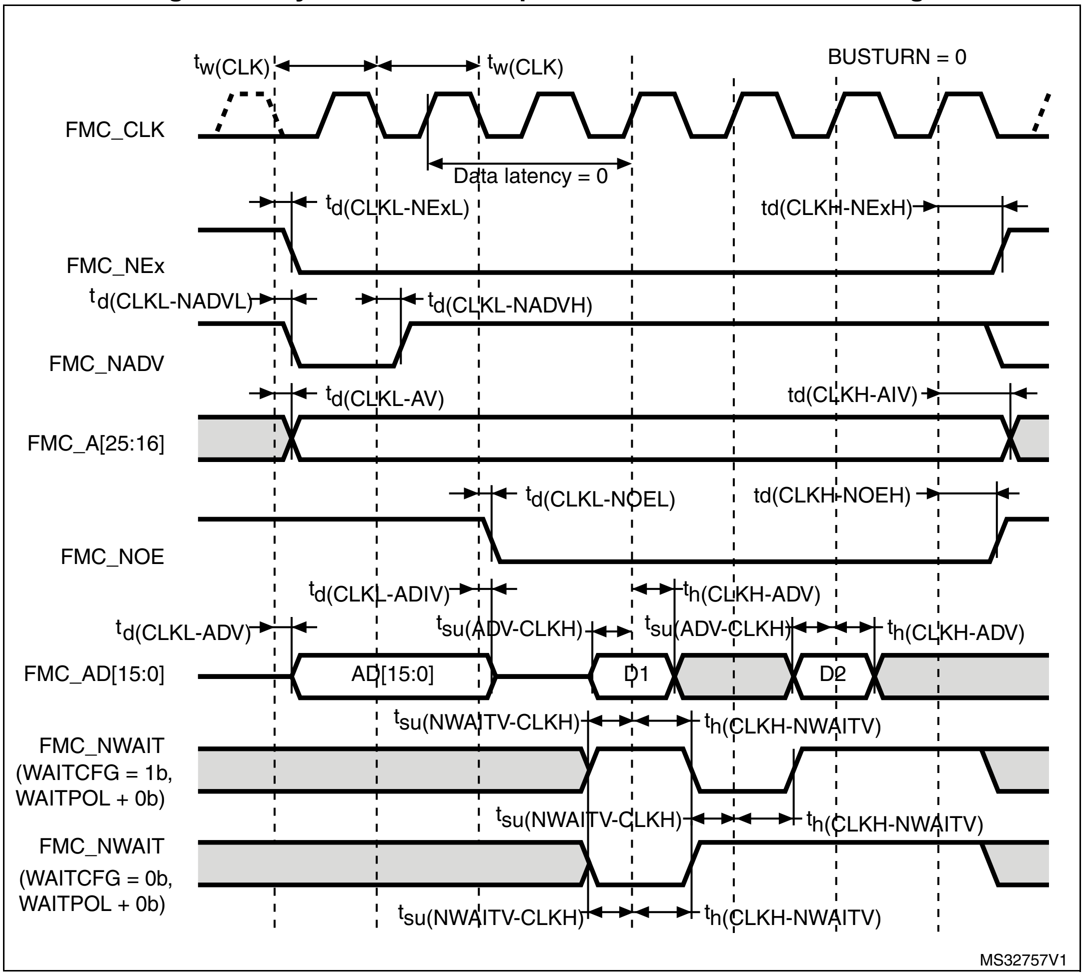


Table 96. Synchronous multiplexed NOR/PSRAM read timings[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK}+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	4	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	0	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	2.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	0	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 41. Synchronous multiplexed PSRAM write timings

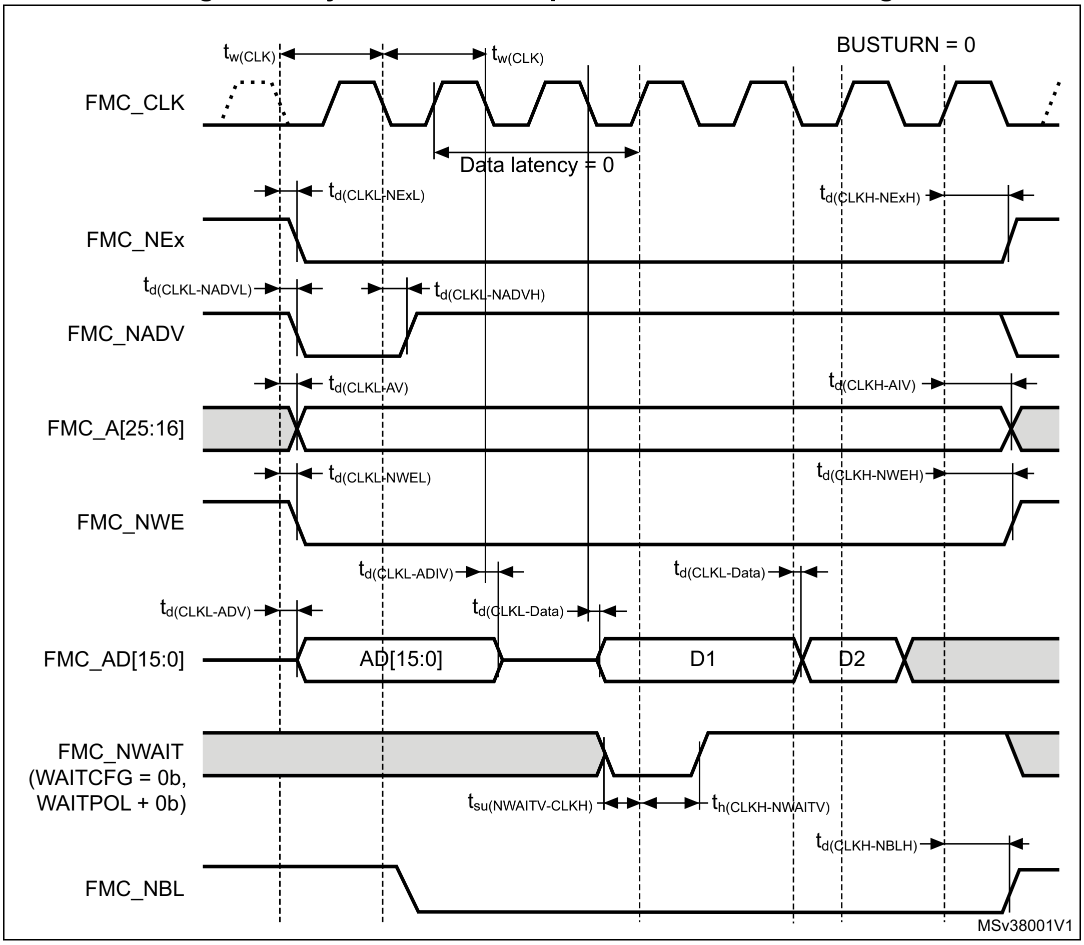


Table 97. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	T_{HCLK}+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	4	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	5.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2.5	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	T_{HCLK}+1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	0	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 42. Synchronous non-multiplexed NOR/PSRAM read timings

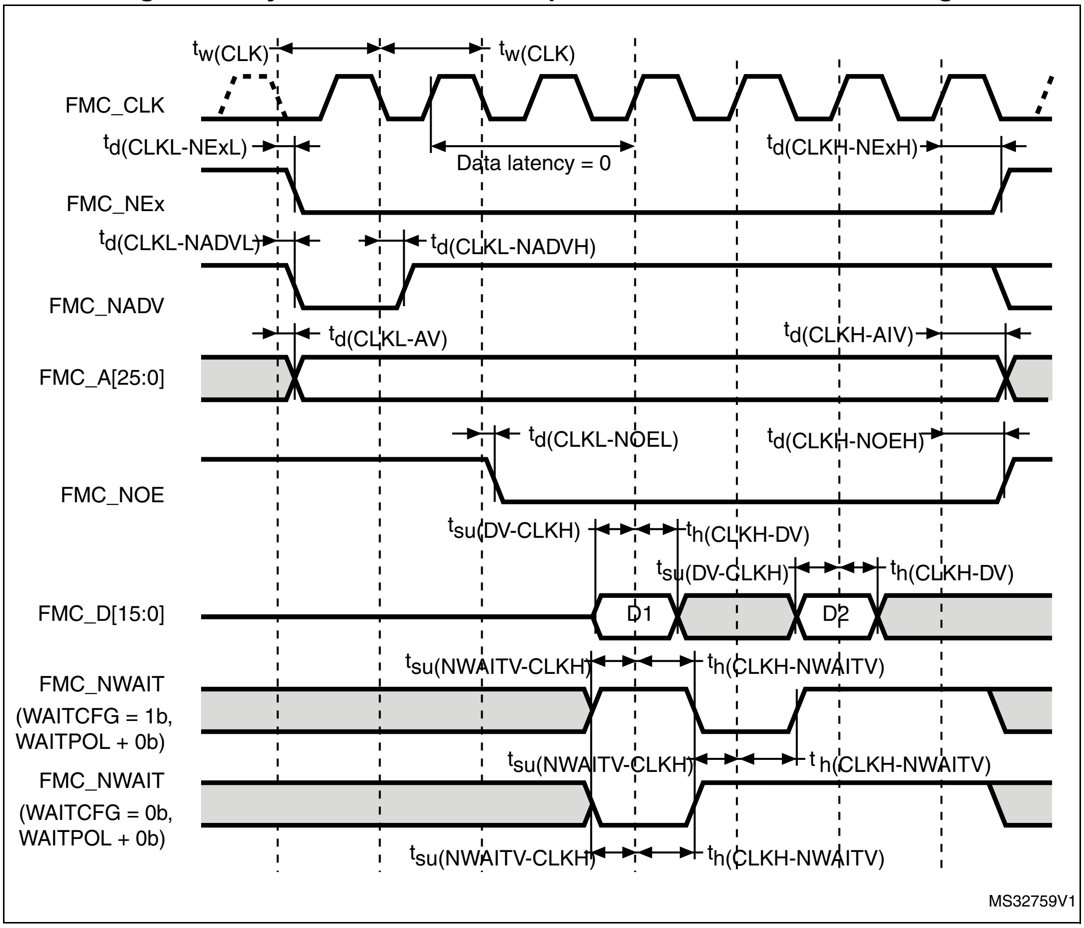


Table 98. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}-0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK}-0.5	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	0	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	0	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 43. Synchronous non-multiplexed PSRAM write timings

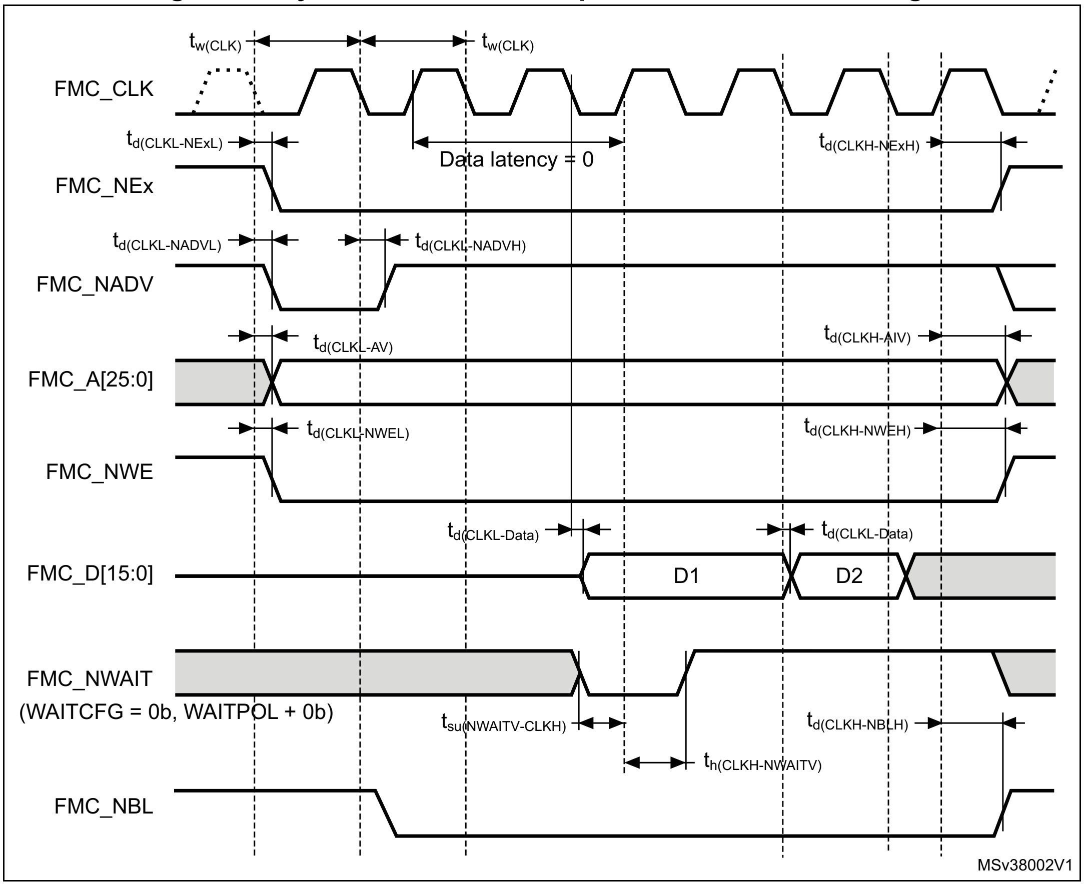


Table 99. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$-0.5	-	ns
$t_{d(CLKL\text{-}NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH\text{-}NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL\text{-}NADVL)}$	FMC_CLK low to FMC_NADV low	-	2	
$t_{d(CLKL\text{-}NADVH)}$	FMC_CLK low to FMC_NADV high	2.5	-	
$t_{d(CLKL\text{-}AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5	
$t_{d(CLKH\text{-}AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}-1	-	
$t_{d(CLKL\text{-}NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH\text{-}NWEH)}$	FMC_CLK high to FMC_NWE high	T_{HCLK}-1	-	
$t_{d(CLKL\text{-}Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	4.5	
$t_{d(CLKL\text{-}NBLL)}$	FMC_CLK low to FMC_NBL low	1.5	-	
$t_{d(CLKH\text{-}NBLH)}$	FMC_CLK high to FMC_NBL high	T_{HCLK}+1	-	
$t_{su(NWAIT\text{-}CLKH)}$	FMC_NWAIT valid before FMC_CLK high	0	-	
$t_{h(CLKH\text{-}NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 44 through *Figure 47* represent synchronous waveforms, and *Table 100* and *Table 101* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x02
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x03
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x03
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 44. NAND controller waveforms for read access

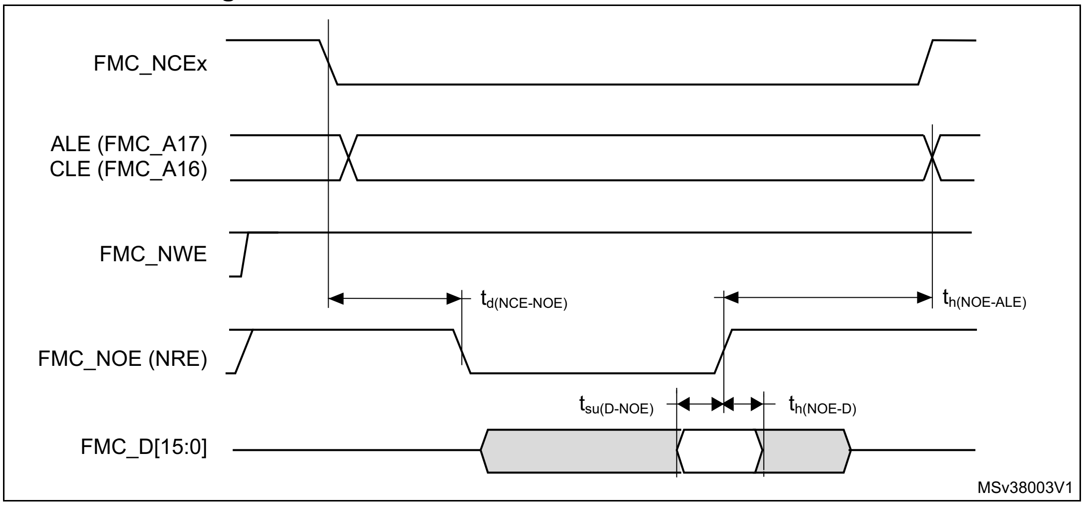


Figure 45. NAND controller waveforms for write access

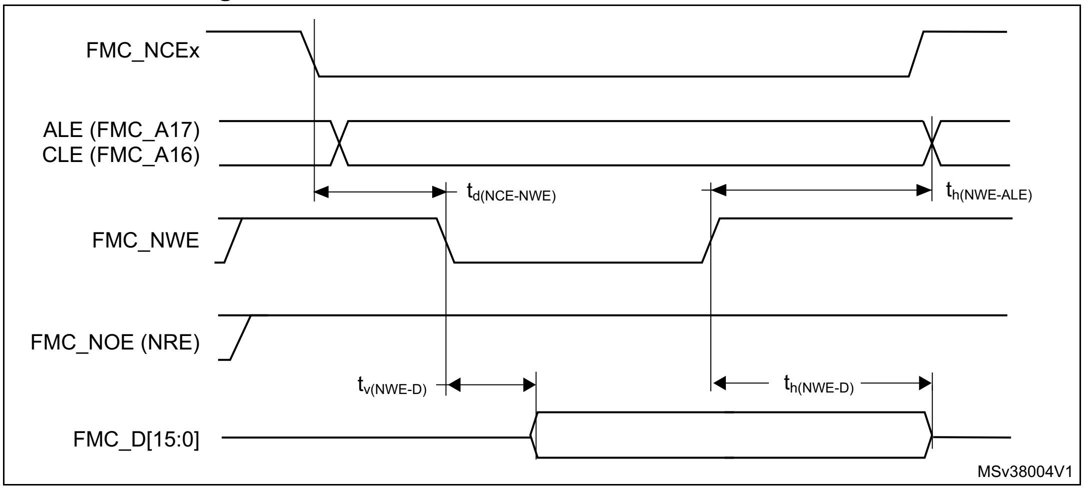


Figure 46. NAND controller waveforms for common memory read access

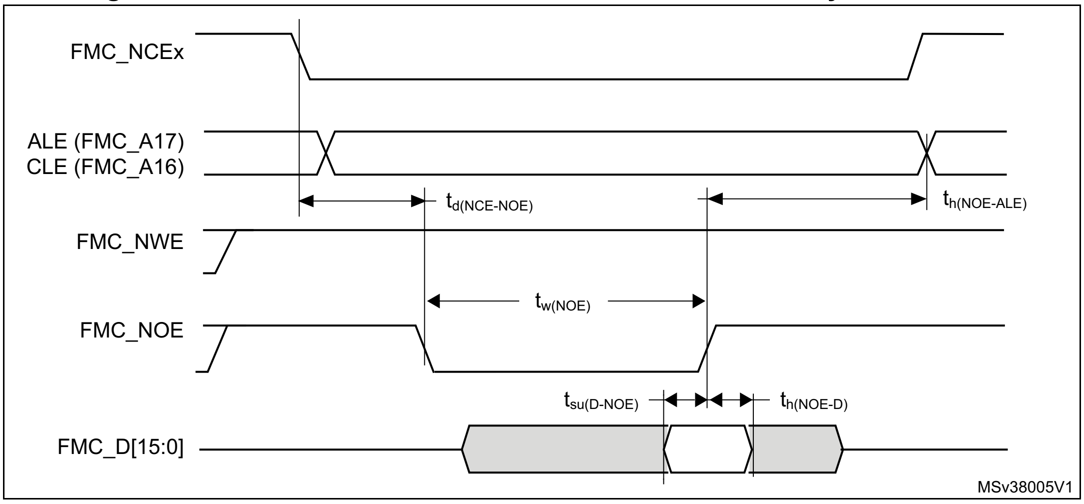


Figure 47. NAND controller waveforms for common memory write access

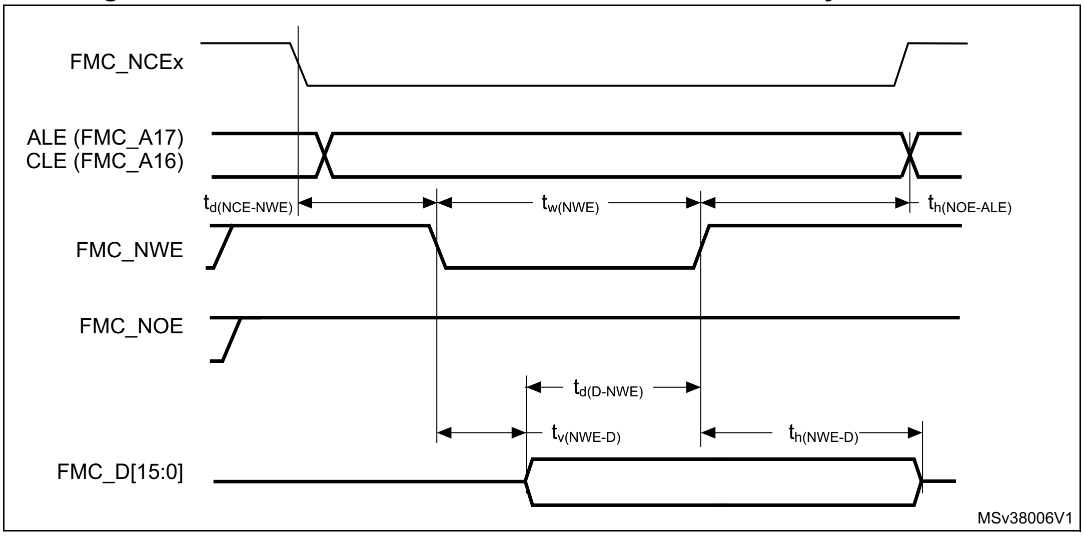


Table 100. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK}$-1	$4T_{HCLK}$+1	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	16	-	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	6	-	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	-	$3T_{HCLK}$+1	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	$2T_{HCLK}$-2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 101. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	$4T_{HCLK}$-1	$4T_{HCLK}$+1	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	-	2.5	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$3T_{HCLK}$-4	-	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}$-3	-	
$T_{d(NCE\_NWE)}$	FMC_NCE valid before FMC_NWE low	-	$3T_{HCLK}$+1	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{HCLK}$-2	-	

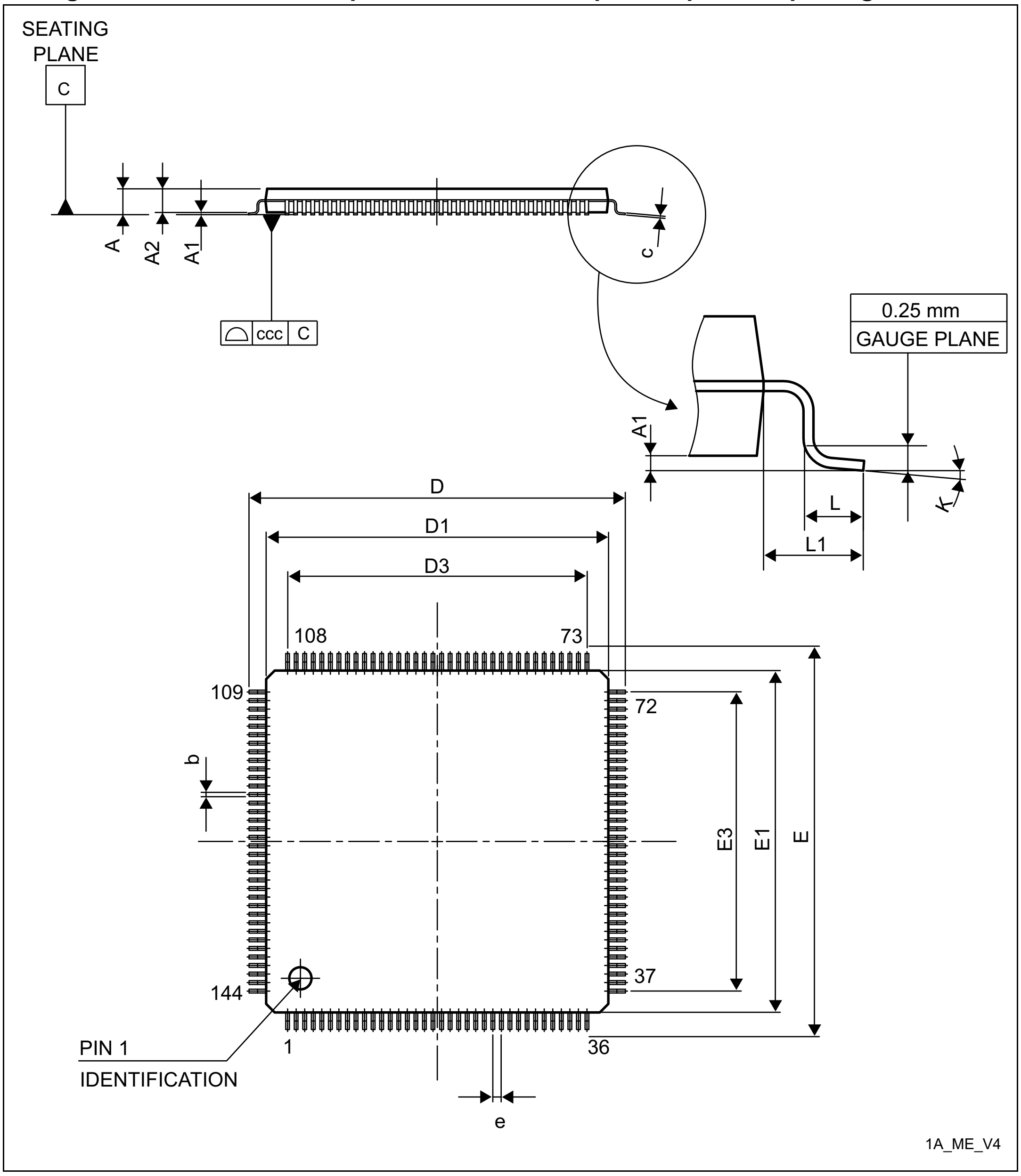
1. CL = 30 pF.
2. Guaranteed by characterization results.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP144 package information

Figure 48. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



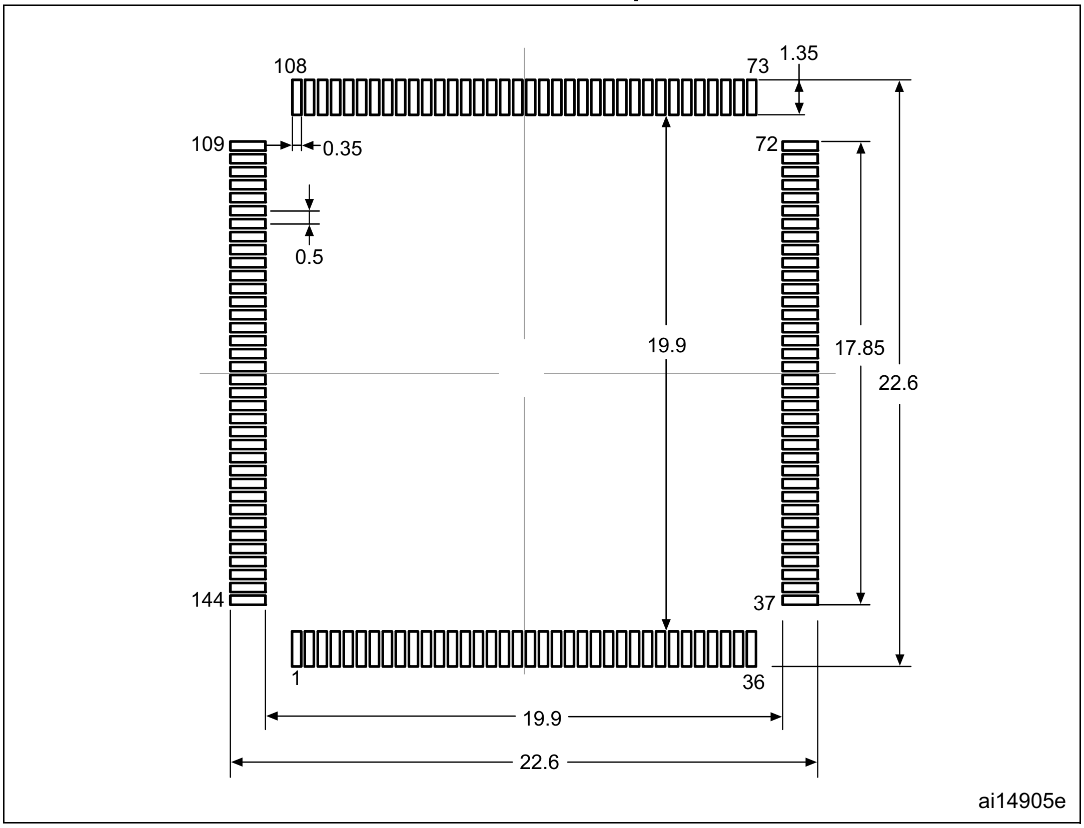
1. Drawing is not to scale.

Table 102. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint

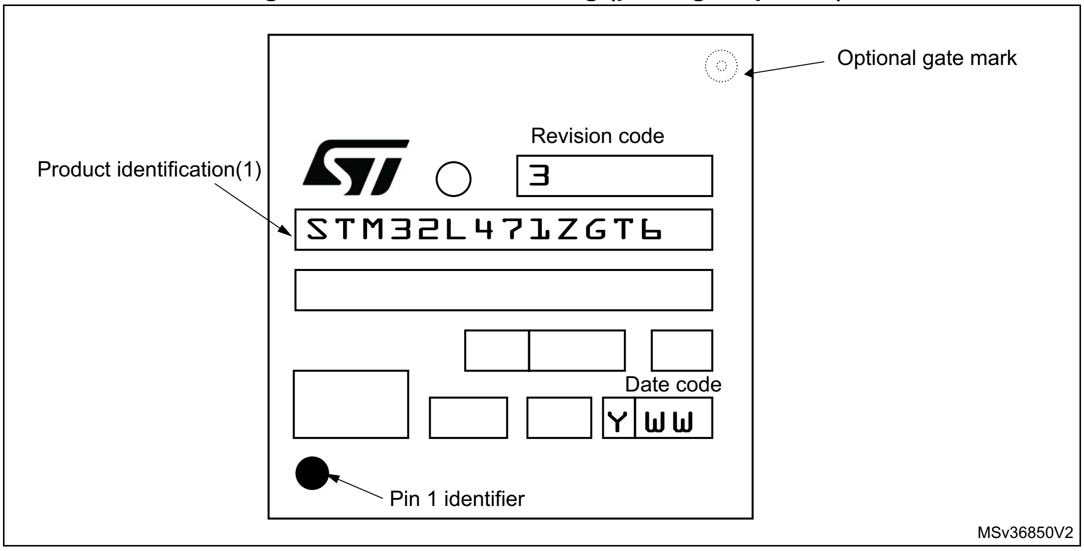


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

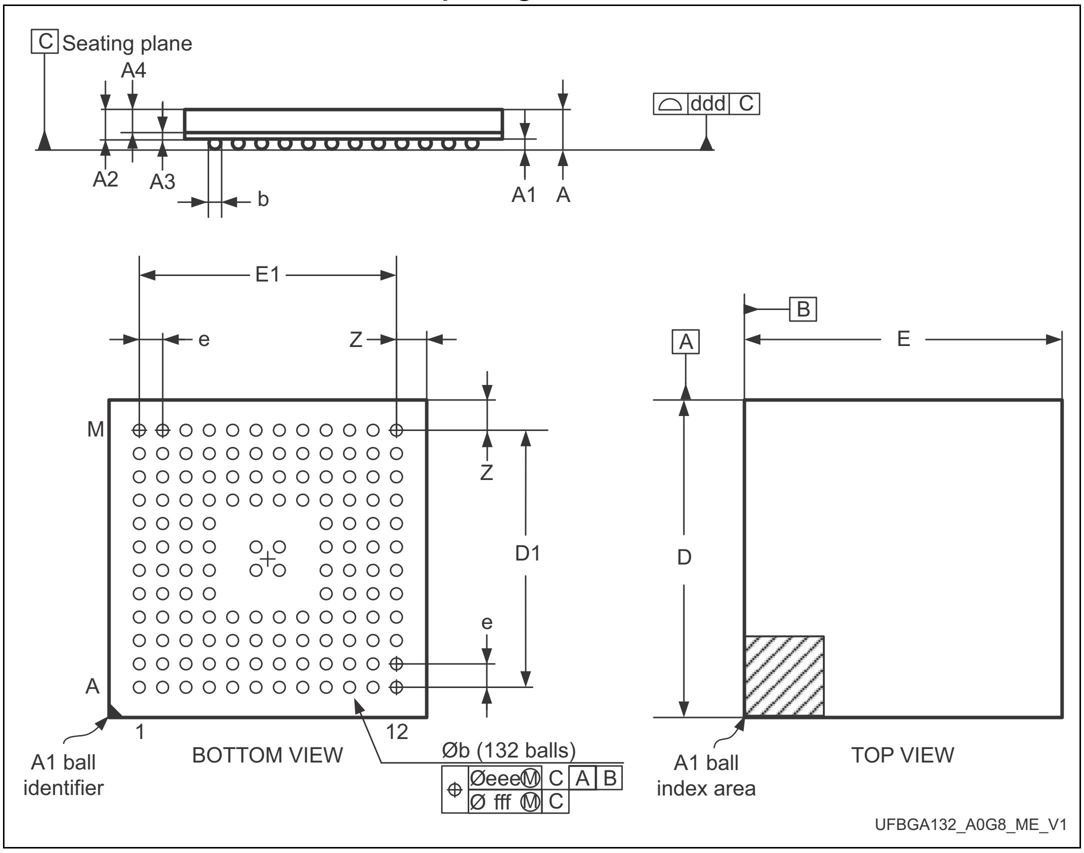
Figure 50. LQFP144 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.2 UFBGA132 package information

Figure 51. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 103. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-

Table 103. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-
ddd	-	0.080	-	-	0.0031	-
eee	-	0.150	-	-	0.0059	-
fff	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package recommended footprint

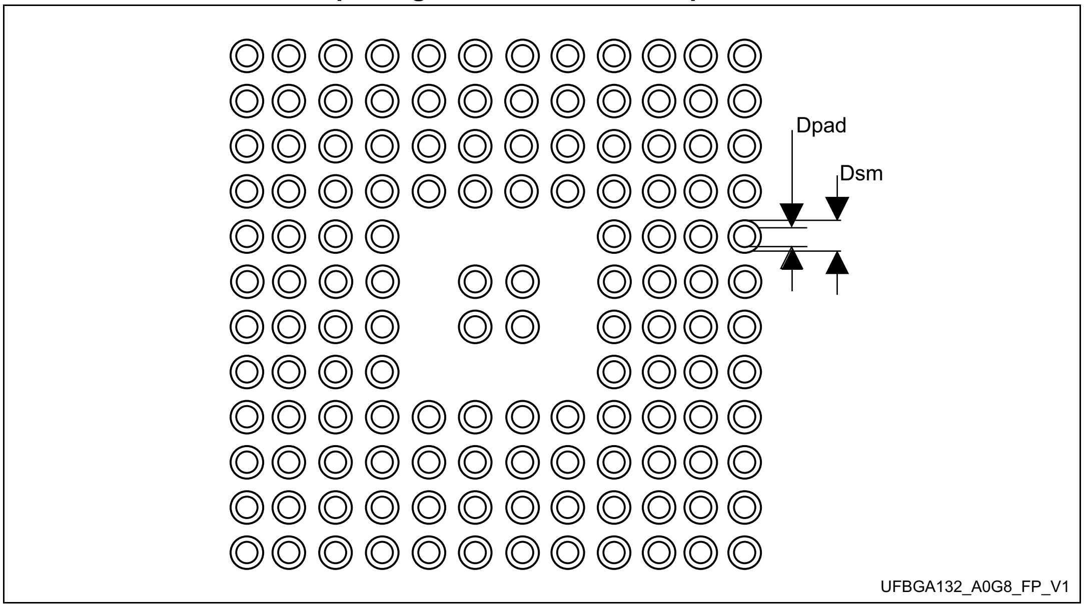


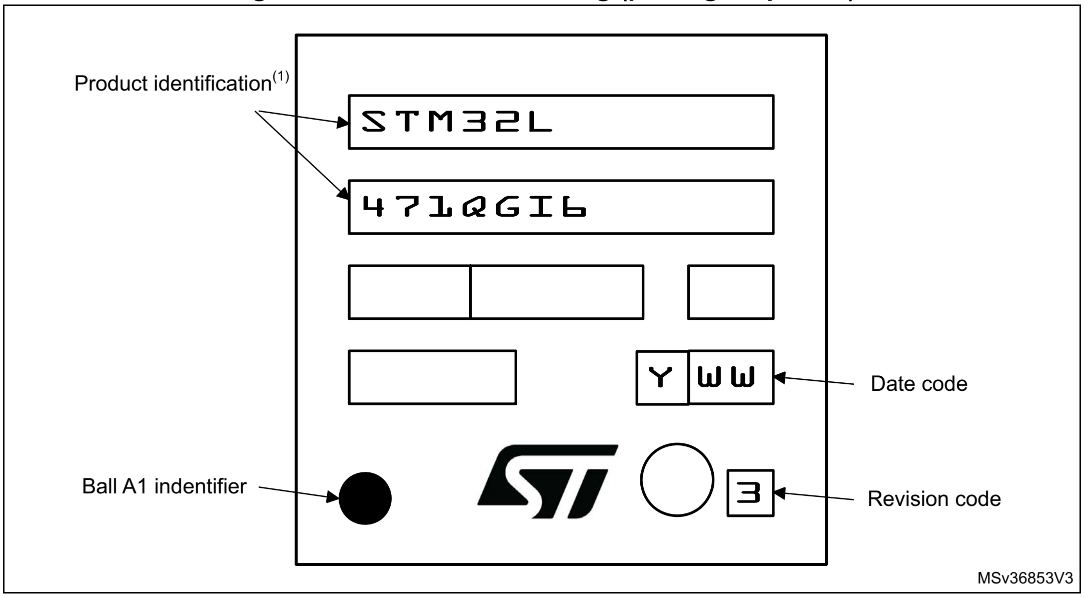
Table 104. UFBGA132 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm
Ball diameter	0.280 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

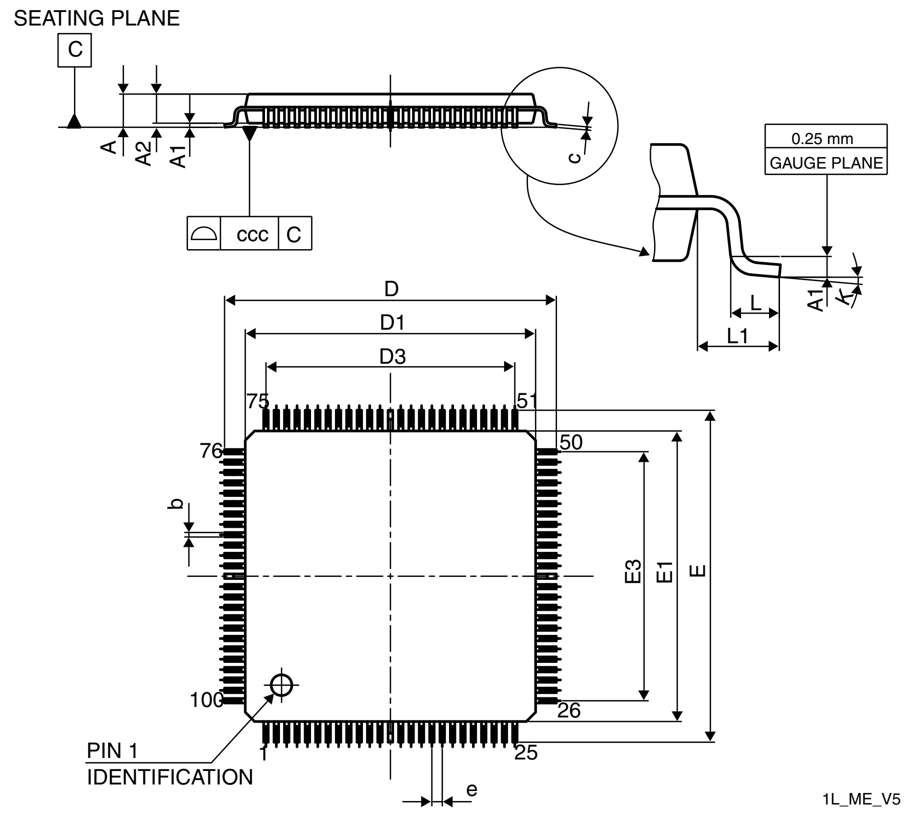
Figure 53. UFBGA132 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.3 LQFP100 package information

Figure 54. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 105. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

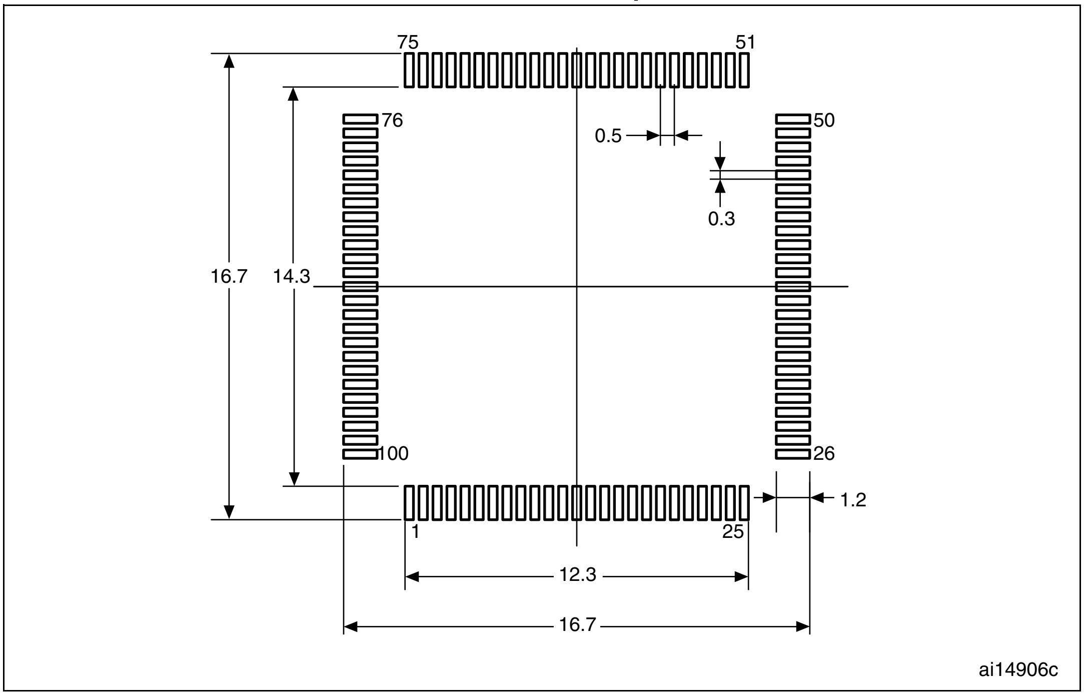
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591

Table 105. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 55. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

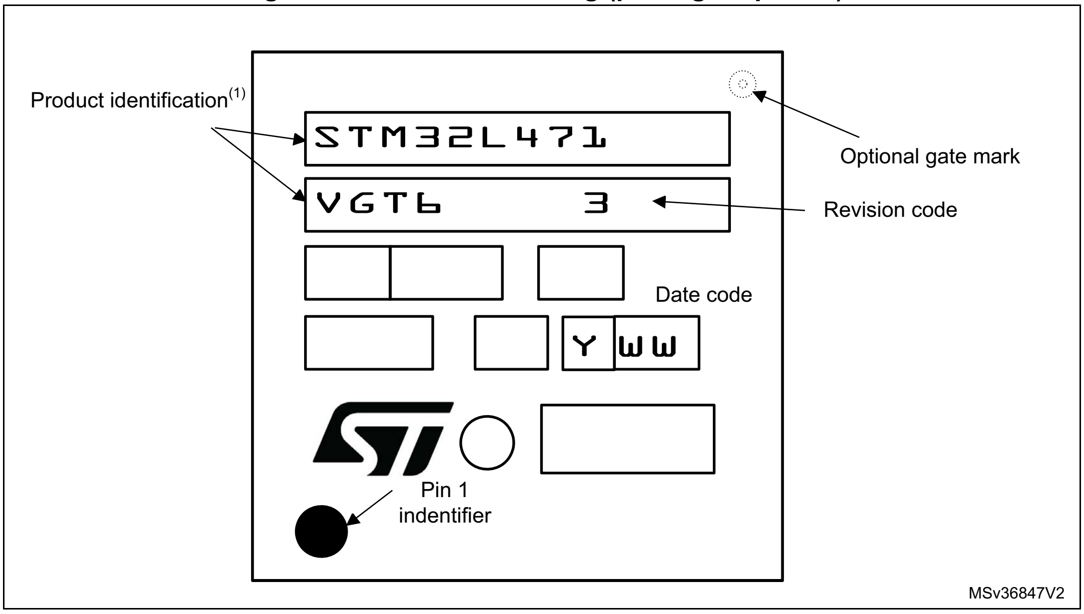


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

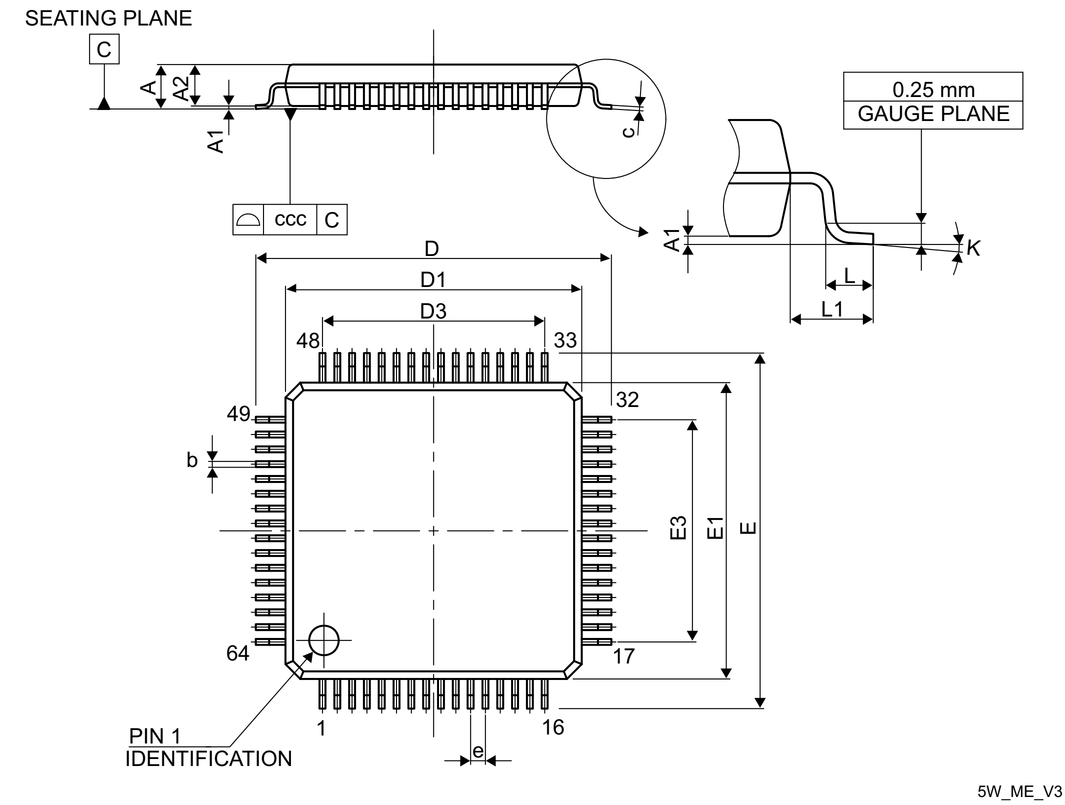
Figure 56. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 LQFP64 package information

Figure 57. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 106. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

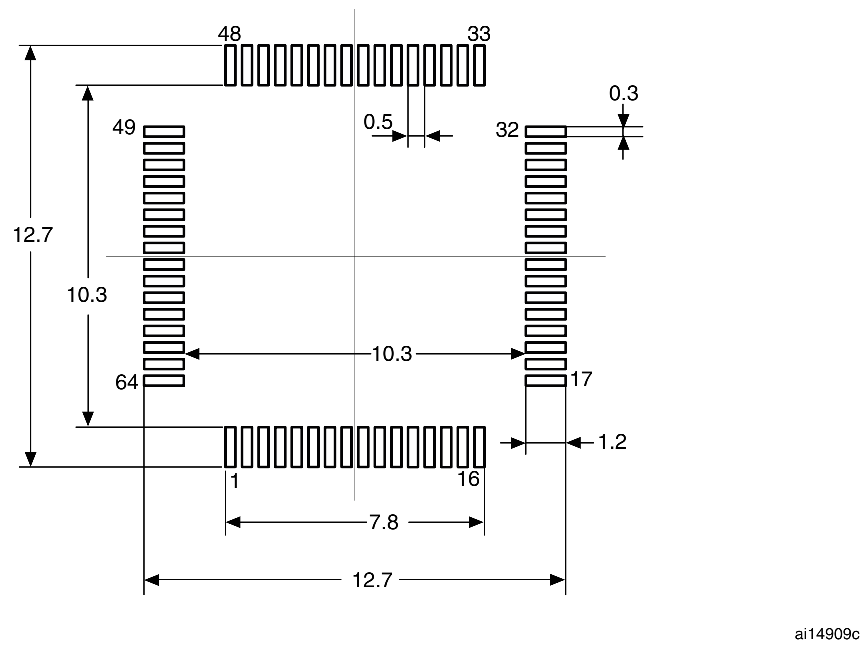
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 106. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 58. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint

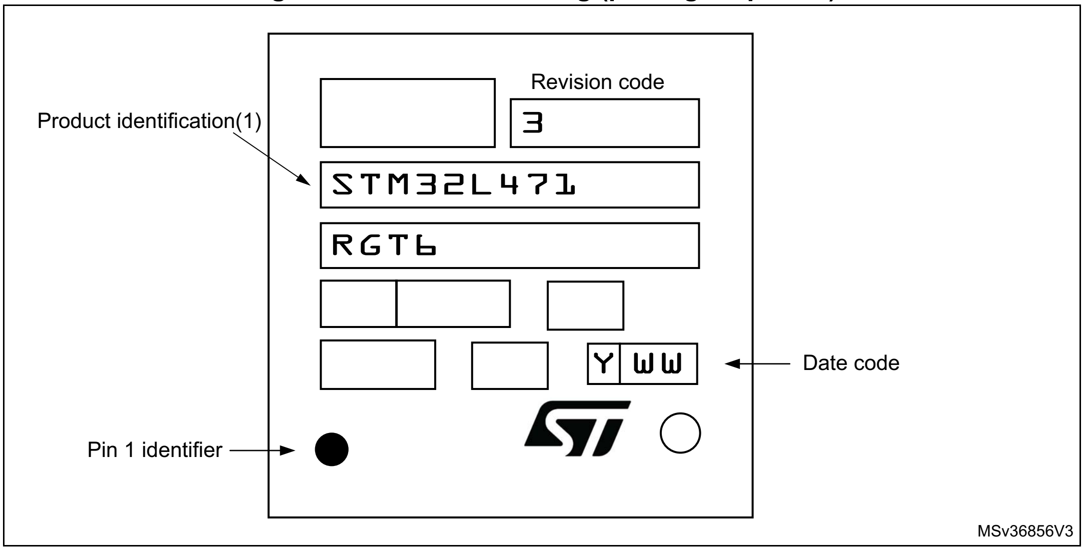


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 59. LQFP64 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 107. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14mm	42	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm	32	
	Thermal resistance junction-ambient UFBGA132 - 7 × 7 mm	55	

7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L471xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in Table 107 T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see Section 8: Part numbering.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (45°C/W × 447 mW) = 105-20.115 = 84.885 °C

Suffix 7: T_{Amax} = T_{Jmax} - (45°C/W × 447 mW) = 125-20.115 = 104.885 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in Table 107 T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

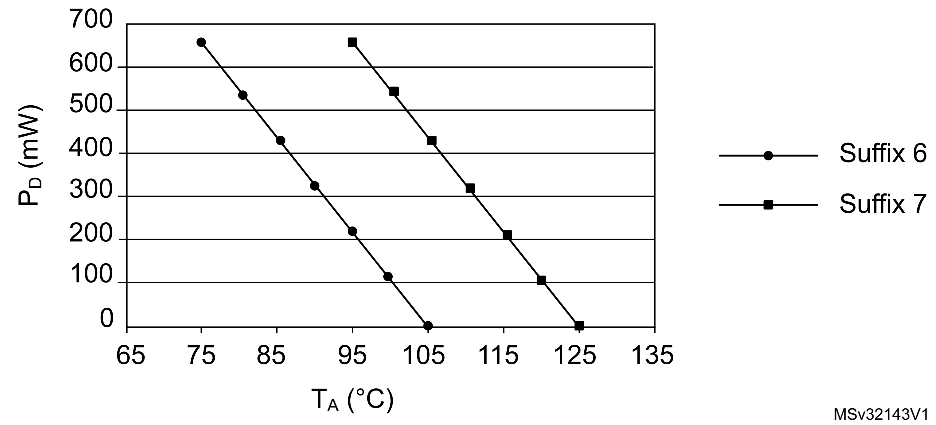
T_{Jmax} = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6.03 °C = 106.03 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 60* to select the required temperature range (suffix 6 or 7) according to your ambient temperature or power requirements.

Figure 60. LQFP64 P_D max vs. T_A



8 Part numbering

Table 108. STM32L471xx ordering information scheme

Example:	STM32	L	471	R	G	T	6	TR

Device family

STM32 = ARM® based 32-bit microcontroller

Product type

L = ultra-low-power

Device subfamily

471: STM32L471xx

Pin count

R = 64 pins

V = 100 pins

Q = 132 pins

Z = 144 pins

Flash memory size

E = 512 KB of Flash memory

G = 1 MB of Flash memory

Package

T = LQFP ECOPACK®2

I = UFBGA ECOPACK®2

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

7 = Industrial temperature range, -40 to 105 °C (125 °C junction)

3 = Industrial temperature range, -40 to 125 °C (130 °C junction)

Packing

TR = tape and reel

xxx = programmed parts

9 Revision history

Table 109. Document revision history

Date	Revision	Changes
04-Fev-2016	1	Initial release.