



SL-5-2128 ✓

SL-7-2128 ✓

021703

Dual 128-Bit Static Shift Registers

FEATURES

- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
No external interfacing components required on data inputs or outputs.
- DC-1MHz Operation
- Full Static Operation—
Data is stored independently of the clock logic level.
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

The SL-5-2128 and SL-7-2128 are dual 128-static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. These devices contain two independent common clock 128-bit DC to 1MHz shift registers, constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. A single phase clock input is provided for both registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition.

*Available only in Europe (14 Lead Plastic DIP)

S-34

ORIG

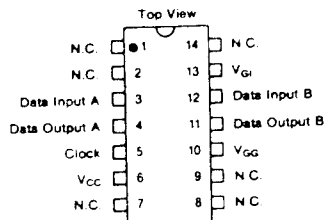
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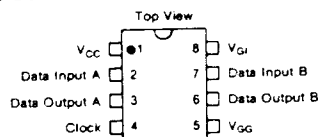
GI

PIN CONFIGURATIONS

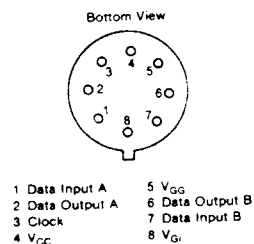
14 LEAD DUAL IN-LINE



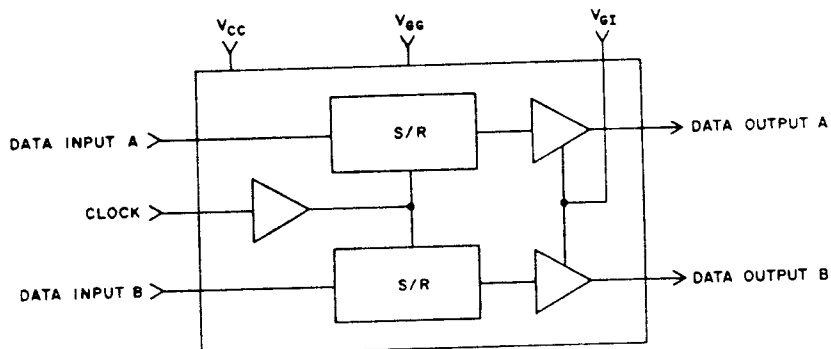
8 LEAD DUAL IN-LINE



8 LEAD TO-78



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GI} with respect to V_{CC} -20V to +0.3V
 Clock and Data Inputs with respect to V_{CC} -15V to +0.3V
 Storage Temperature -65°C to +150°C
 Operating Temperature: 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ± 0.5 Volts (V_{CC} is the substrate voltage)
 V_{GG} = -12 Volts ± 1 Volt
 V_{GI} = GND
 Operating Temperature (T_A) = 0°C to +70°C
 One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	V_{OH}	$V_{CC}-1.5$	—	—	Volts	$V_{in} = V_{CC} - 10V$
Logic 0 Level	V_{OL}	—	—	-0.8	Volts	
Leakage	I_{Le}	—	—	10	μA	
Data Input						
Logic 1 Level	V_{IH}	$V_{CC}-1.5$	—	—	Volts	$V_{in} = V_{CC} - 10V$
Logic 0 Level	V_{IL}	—	—	-0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	
Data Output						
Logic 1 Level	V_{OH}	$V_{CC}-1.0$	—	—	Volts	$I_{OH} = 100 \mu A$ $I_{OL} = 1.6 mA$
Logic 0 Level	V_{OL}	—	—	-0.4	Volts	
Power	—	—	325	425	mW	
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	1.0	MHz	$t_i = t_{pdw} + t_r$ $t_{ed} \geq 1 \mu sec$ 1MHz, $T_A = +25^\circ C$
Pulse Width	t_{pdw}	450	350	—	ns	
Pulse Delay	t_{pd}	450	—	—	ns	
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	30	—	pF	
Data Input						
Set Up Time	t_{DS}	200	150	—	ns	1MHz, $T_A = +25^\circ C$
Hold Time	t_{DH}	100	50	—	ns	
Capacitance	C_i	—	10	—	pF	
Data Output						
Propagation Delay	t_{pd}	—	300	400	ns	

**Typical values are at +25°C and nominal voltages

TIMING DIAGRAM

