SSI 32P4620/4621
Pulse Detector & Data Separator
Advance Information

June, 1990

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DESCRIPTION

The SSI 32P4620 combines pulse detection and data synchronization electronics into a single high-performance bipolar integrated circuit. It provides advanced features like programmable data rate, and write precompensation control. Data synchronization is performed with a fully integrated high-performance PLL. The VCO frequency setting elements are incorporated into the 32P4620 for enhanced performance and reduced board space. Programmable channel filtering supports both constant density recording and pulse slimming applications. These features are programmed by two external DACs such as those provided by the 32D4660. Data rate is programmed by a single external resistor or a DAC in constant-density recording applications. The 32P4620 only requires a +5V power supply and is available in a variety of packages.

FEATURES

- **High performance pulse detector**
  - **Wide bandwidth AGC**
  - **Dual Rate charge pump**
  - **Amplitude pulse qualification**
- **High performance data synchronizer**
  - **Fast aquisition PLL, using zero phase restart**
  - **Programmable write precompensation**
  - **1, 7 ENDEC**
- **Supports Constant-Density Recording applications**
  - **Programmable data rate**
  - **Programmable channel filtering**
- **Variable width pulse slimming**
- **Servo burst output available**
- **Supports external read channel margin testing**
- ***Differential (TTL option) high speed digital data paths and TTL compatible mode control interface***
- **Low power, +5 volt only operation**
- **Available in 68- and 100-pin packages**

CIRCUIT DESCRIPTION

The circuit is intended to be used as a read pulse detector and data/clock recovery circuit for 1, 7 RLL code in hard disk drive systems with a +5V supply. A circuit block diagram is shown in Figure 5.

MODE CONTROL

The circuit mode is controlled by the CHIP_EN, SERVO_EN, WG, RG, $\overline{\text{HOLD}}$, AND SHORT pins. Additionally, the chip can be configured through the PULSE DETECTOR MODE CONTROL register and the DATA/CLOCK RECOVERY MODE CONTROL register, both of which are loaded through the serial digital interface.

When reading or writing data the CHIP_EN pin should be high or open circuited. When the CHIP_EN pin is pulled low and the SERVO_EN pin is pulled high the chip data/clock recovery section is disabled. This mode is intended for monitoring servo data in a low power mode when data is not being read or written. When the CHIP_EN and SERVO_EN pins are pulled low the chip goes into a low power state. Recovering from the low power state can be slow due to the necessity of charging external capacitors.

The input AGC amplifier, pulse detector and write driver sections of the circuit are controlled by the WG pin and are placed in the read mode when the WG pin is low and in write mode when the WG pin is high or open. The write driver is active during write and inactive during read.

The RG pin controls what signal the data/clock recovery PLL locks to. When RG is high the PLL locks to the signal from the pulse detector input. Normally this is the signal from the pulse detector but the signal can be externally supplied from the $\overline{\text{RD}}$ pin for testing by setting the appropriate control register bit. When RG is low the PLL locks to an external reference supplied at the FREF pin.

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT DESCRIPTION (Continued)

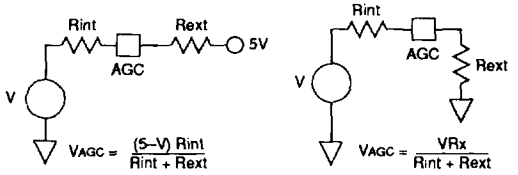
AUTOMATIC GAIN CONTROL CIRCUIT

An amplified head output signal, such as the output of the SSI 32R117, 501, 510 or 32R4610 read/write circuits, is AC coupled to the IN1+ and IN1− inputs. When WG is high or when SHORT is high the pulse detect digital circuitry is disabled and the input impedance of the input AGC stage is reduced to allow more rapid settling of the input coupling capacitors from the read/write circuit upon transition to the read mode. Transition timing to read is controlled to allow settling of the coupling capacitors between the read/write circuit and the 32P4620 before the AGC circuitry is activated when going to the read mode. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling. Also, when SHORT is high the AGC circuit enters the read mode in a maximum gain state and can rapidly attack to the desired level.

The $\overline{\text{HOLD}}$ pin controls the input AGC stage automatic gain circuit. When CHIP_EN or SERVO_EN is high, and $\overline{\text{HOLD}}$ is high and WG and SHORT are low the input AGC amplifier is controlled to keep a constant read data peak level. When the $\overline{\text{HOLD}}$ pin is pulled low the gain of the analog circuit is held at the level determined when the $\overline{\text{HOLD}}$ pin was high (the gain will slowly drift due to leakage).

In the read mode the level at the input to the DIN+, DIN- pins is controlled by full wave rectifying the level at these pins and comparing it to a reference level supplied at the AGC pin. When the input level at the DIN+, DIN- input is greater than about 125% the desired level as set by the AGC pin the circuit is in a fast attack mode and will supply about 1.7 mA of discharge current at the GAIN pin. When the circuit is not in fast attack and the input level is above 100% of the desired level the circuit enters a slower attack mode and will supply about 0.18mA of discharge current. This allows the AGC amplifier to rapidly recover when going from write to read but reduces zero crossing distortion once the AGC amplifier is in range. There is an on-chip fixed slow decay current source. When the slow attack threshold has not been reached for a specified amount of time the circuit assumes the signal is too low and goes into a fast decay mode. The fast attack and fast decay modes can be disabled with the fast attack/decay control bit in the PULSE DETECTOR MODE CONTROL register.

The AGC pin is internally biased so that the target differential voltage input at the DIN+/− pins is 1.0 Vp-p at nominal conditions. The AGC voltage can be modified by tying a resistor between AGC and ground or VPA. A resistor to ground decreases the voltage level while a resistor to VPA increases it. The resultant AGC voltage level is:



where:

V=Voltage at AGC with pin open(TBD, nom.)
Rint = AGC pin input impedance (6.7 kΩ, typ.)
Rx = External resistor

The new DIN+/− input target level is nominally 0.48 Vp-p/V_{AGC}.

Gain of the AGC amplifier is nominally:

Av = Gain of the AGC stage
= K1 x exp[K2 x V(GAIN)]

where:

Av = Gain of AGC stage
V(GAIN) = Voltage on the gain pin

READ MODE DIGITIZING SECTION

In the data path the signal is sent to a hysteresis comparator. The comparator hysteresis level can be set at a fixed level or, with the addition of an external filter network, can be set as a fraction of the signal level as shown in the circuit block diagram. The latter approach allows setting the AGC circuit decay and slow attack times slow enough to minimize distortion of the signal going into the clocking path and setting a shorter time constant for the hysteresis level. Thus when switching to a head with a different output level or when switching from write to read the circuit is properly decoding data before the AGC circuit gain has settled to its final steady state level. In addition, the hysteresis threshold level can be set from the serial data port. The output of the hysteresis comparator is sent to the "D" input of a D flip-flop. The DOUT pin provides the TTL compatible comparator output digital signal for testing purposes and, if required, for use in the servo circuit.

In the clocking path the signal is sent to a differentiator circuit whose characteristics are set by external components. The output of the differentiator circuit is sent to an edge trigger circuit which creates an output pulse on every zero crossing of the output of the differentiator. The output of the edge trigger is the clock input of the D flip flop. The COUT pin provides the edge trigger output signal for testing purposes.

During normal system operation the differentiator circuit clocks the D flip-flop on every positive and negative peak of the signal input to DIN+,DIN-. The data path D input to the flip-flop only changes state when the signal applied to the DIN+, DIN- inputs exceeds the hysteresis comparator threshold in a polarity opposite the polarity of the peak which last exceeded the threshold. Therefore, the clocking path determines signal timing and the data path blocks spurious peaks if they do not exceed the hysteresis comparator threshold. Figure 8 shows circuit operation of the digital section. The two digital signal path delays between the DIN+, DIN- inputs to the flip-flop CK input and the DIN+, DIN- inputs to flip-flop D input are well matched.

SERVO BURST CAPTURE SECTION

The circuit provides a full wave rectified output of the signal appearing at the DIN+/- inputs at the SER_OUT pin and a servo reference level at the SER_REF pin for use in embedded servo recovery.

DATA/CLOCK RECOVERY CIRCUIT

The circuit is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1,7 RLL encoding format. In the read mode the circuit performs data synchronization, sync field search and detect, address mark detect, and data decoding. In the write mode, the circuit converts NRZ data into the 1,7 RLL format described in Table 3, performs write precompensation, generates the preamble field and inserts address marks as requested. The interface electronics and architecture of the circuit have been optimized for use as a companion device to the SSI 32C452, SSI 32C4640 or AIC 010 controllers.

The data rate is established by a single 1% external resistor, RR, connected from the IREF pin to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

RR= (TBD/DR) - TBD kΩ

where: DR = data rate in Mbit/s

In a constant density recording application the IREF pin can be driven by a DAC such as contained in the SSI 32D4660. The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{DRD}$ pulse. In the write and idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, false lock to $\overline{DRD}$ is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. The READ GATE (RG) and WRITE GATE (WG) inputs control the mode of the data/clock recovery section of the chip.

RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output write data pulse. NRZ write data input to encoded write data output latency is 5 NRZ clock periods.

READ OPERATION

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the $\overline{RD}$ (internal) input and a low level selects the external reference clock.

In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of VCO/2. As depicted in Figure 9, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the leading edge of RD. A decode window is developed from the VCO/2 clock.

In the non-read modes, the PLL is locked to the external reference clock. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

SOFT SECTOR OPERATION

Refer to Figure 1.

ADDRESS MARK DETECT

In soft sector read operation the circuit must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark consists of two sets each of seven "0" patterns followed by two sets each of eleven "0" patterns. To begin the read lock sequence the read gate (RG) is asserted high by the controller. The address mark detect (AMD) circuit then initiates a search of the read data (RD) for an address mark. First the address mark detect circuit looks for a set of 6 "0's" within the 7 "0's" patterns. Having detected a 6 "0's" pattern the AMD then looks for a 9 "0's" set within the 11 "0's" patterns. If AMD does not detect 9 "0's" within 5 RD bits after detecting a 6 "0's" pattern it will restart the address mark detect sequence and look for 6 "0's." When the AMD has acquired a 6 "0's," 9 "0's" sequence the $\overline{AMD}$ output transitions low.

PREAMBLE SEARCH

After the address mark (AM) has been detected, an internal counter counts negative transitions of the incoming read data (RD) looking for 3 consecutive "3T" preambles. Once the counter reaches count 3 (i.e. finds 3 consecutive "3T" preambles) the internal read gate enables, switching the phase detector from the external reference clock to the delayed read data input ($\overline{DRD}$); at the same time a zero phase restart (internal) signal restarts the VCO in phase with the read reference clock. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK AND BIT SYNC ENABLE

When the internal counter counts sixteen more "3T" or a total of 19 negative transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the RRC source switches from the external reference clock to VCO clock signal which is phase locked to DRD. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with the data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

HARD SECTOR OPERATION

Refer to Figure 2. In hard sector operation $\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark but starts with a preamble search as with soft sector and sequences identically. In all respects, with the exception of the address mark sequence, hard sector read operation is identical to soft sector.

WRITE MODE

In the write mode the circuit converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. The circuit can operate with a hard or soft sector hard drive.

In soft sector operation the circuit generates a 7"0's," 7"0's," 11"0's," 11"0's" address mark and a preamble ("3T"s) pattern. In hard sector operation the circuit generates a "3T" preamble pattern but no preceeding address mark.

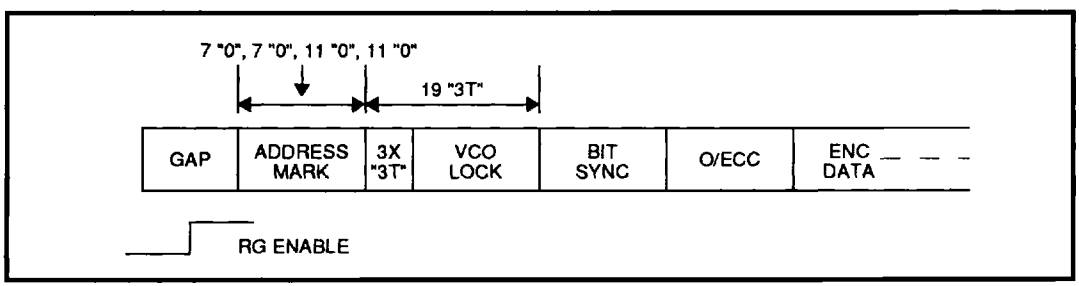


FIGURE 1: Disk Operation Lock Sequence in Read Mode Soft Sector Operation

Serial NRZ data is clocked into the circuit and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the RRC.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The circuit recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back shift. The magnitude of the time shift, TPC, is determined by an external RC network on the PCS pin given by:

TPC =(TBD) (Rps) (Cps + Cs),

and as programmed through the serial data port.

The circuit performs write precompensation according to the algorithm outlined in Table 3.

SOFT SECTOR

In soft sector operation, when read gate (RG) transitions low, VCO source and RRC source switch from RD and VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After a delay of 1 NRZ time period (min) from RG low, the write gate (WG) can be enabled while NRZ is maintained (NRZ write data) low. The address mark enable ($\overline{WAM}$) is made active (high) a minimum of 1 NRZ time period(s) later. The address mark (consisting of 7"0's,"7"0's,"11"0's,"11"0's") and the preamble is then written to $\overline{WD}$. NRZ goes active at this point and after a delay of 5 NRZ time periods begins to toggle out $\overline{WD}$ encoded data. Finally, at the end of the write cycle, 5 NRZ of blank encoded time passes to insure the encoder is flushed of data; WG then goes low.

HARD SECTOR

In hard sector operation, when read gate (RG) transitions low, VCO source and RRC switch references and VCO lock (internal) goes inactive as with soft sector and the $\overline{WAM}$ (address mark enable) is tri-stated. The circuit then sequences from RG disable to WG enable and NRZ active as in soft sector operation.

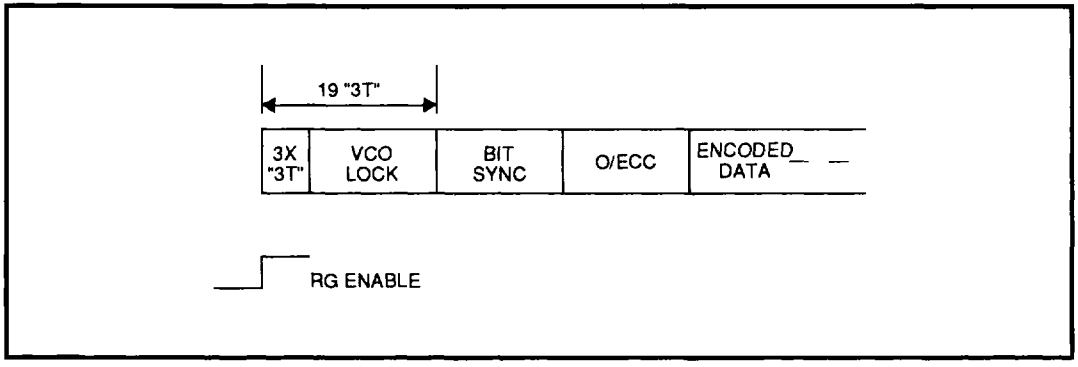


FIGURE 2: Disk Operation Lock Sequence In Read Mode Hard Sector Operation

TABLE 1: 1, 7 RLL Code Set

PREVIOUS CODE WORD LAST BIT	DATA BITS PRESENT	NEXT	CODE BITS
X0	1 0	0 X	1 0 1
X0	1 0	1 X	0 1 0
X0	1 1	0 0	0 1 0
X0	1 1	* *	1 0 0
10	0 0	0 X	0 0 1
10	0 0	1 X	0 0 0
00	0 1	0 X	0 0 1
00	0 1	1 X	0 0 0
X1	0 0	0 X	0 0 1
X1	0 0	1 X	0 1 0
X1	0 1	0 0	0 1 0
X1	0 1	* *	0 0 0
Y2, Y3	D1 D2	D3 D4	Y1 Y2 Y3

X = Don't care

* = Not all zeros

TABLE 3: Write Precompensation Algorithm

BIT n-2	BIT n-1	BIT n	BIT n+1	BIT n+2	COMP. BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its normal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its normal time position towards the bit n-1 time position.

TABLE 2: Clock Frequency

WG	RG	VCO REF	RRC	DECCLK	ENCCLK	MODE
0	0	FREF/2	FREF/3	FREF/2	FREF/2	IDLE
0	1	RD	VCO/3	VCO/2	FREF/2	READ
1	0	FREF/2	FREF/3	FREF/2	FREF/2	WRITE
1	1	EXT. RD	FREF/3	FREF/2	FREF/2	IDLE

Note 1. Until the VCO locks to the new source, the VCO/2 entries will be XTAL/2.

2. Until the VCO locks to the new source, the VCO/3 entries will be XTAL/3.

3. WG=1 and RG=1 implement a test mode where RD is supplied externally at the $\overline{RD}$ pad.

PIN DESCRIPTIONS

POWER SUPPLY

NAME	TYPE	DESCRIPTION
VPA1, VPA2, VPA3	I	5 volt analog power supply pins
VPD1, VPD2	I	5 volt digital power supply pins
AGND1, AGND2, AGND3	I	Analog ground pins
DGND1, DGND2	I	Digital ground pins

CHIP MODE CONTROL

CHIP_EN	I	CHIP ENABLE: TTL compatible input which enables the chip during normal drive operation
SERVO_EN	I	SERVO ENABLE: TTL compatible input which enables only the portions of the chip needed to read the servo burst.
WG	I	WRITE GATE: TTL compatible read/write control pin
SDATA	I	SERIAL DATA: Serial data input
SCLK	I	SERIAL CLOCK: Serial data clock
DATA_EN	I	DATA ENABLE: Serial data enable pin
R/$\overline{W}$	O	READ/WRITE: TTL compatible output pin which is the negative of WG and which is intended to drive the R/$\overline{W}$ input of the read write chip

AGC GAIN STAGE

IN1+, IN1-	I	INPUT1+/-: AGC amplifier signal input pins
OUT1+, OUT1-	O	OUTPUT1+/-: AGC amplifier signal output pins
HP2+, HP2-, LP2+, LP2-	I	HIGH/LOW PASS INPUTS: Inputs into a summer with variable gain coefficients from external high pass and low pass filters. This configuration is intended to implement a pair of real axis variable zeros.
HP3+, HP3-, LP3+, LP3-	O	HIGH/LOW OUTPUTS: Variable gain outputs to an external filter. This configuration is intended to implement a pair of imaginary axis variable zeros.
IN4+, IN4-	I	INPUT4+/-: Fixed gain amplifier signal input pins
OUT4+, OUT4-	O	OUTPUT4+/-: Fixed gain amplifier signal output pins

AGC GAIN STAGE (Continued)

NAME	TYPE	DESCRIPTION
MULT_1, MULT_2	I	MULTIPLIER 1 & 2: Pins whose DC levels control the gain ratios of the 2 multiplier stages setting equalizer & bandwidth response.
$\overline{\text{HOLD}}$	I	HOLD: TTL compatible control pin which, when pulled low, holds the input AGC amplifier gain.
SHORT	I	SHORT: TTL compatible control pin which, when pulled high shorts the AGC input pins.
AGC	I	AUTOMATIC GAIN CONTROL REFERENCE: Reference input voltage level for the AGC circuit.
GAIN	I	GAIN CONTROL VOLTAGE: The AGC timing capacitor is tied between this pin and AGND. Also gain of the AGC amplifier can be controlled by a DC voltage on this pin.
VREF	O	REFERENCE VOLTAGE: A reference voltage for the external D/A which supplies MULT_1 and MULT_2.

PULSE DIGITIZING STAGE

DIN+, DIN-	I	DATA IN+/-: Signal input pins to the hysteresis level detect comparator.
HYS	I	HYSTERESIS: Hysteresis level setting input to the hysteresis level detect comparator.
LEVEL	O	LEVEL: Provides rectified level setting level for input into the hysteresis circuit.
DOUT, $\overline{\text{DOUT}}$	O	DATA OUT+/-: D input into D flip-flop provided as output for testing or servo use. Differential Version (32P4621): Differential Outputs TTL Version (32P4620): DOUT only TTL output, $\overline{\text{DOUT}}$ not provided
CIN+, CIN-	I	CLOCK INPUT+/-: Differential signal input pins to the clocking channel.
COUT	O	CLOCK OUTPUT: Clock input into D flip-flop provided for testing
$\overline{\text{RD}}$	I/O	READ DATA: Bidirectional test pin which provides ECL like read output from the pulse detector section when WG is low and allows a TTL compatible external read data pattern to be sent to the data/clock recovery when WG is high.

SERVO OUTPUT

NAME	TYPE	DESCRIPTION
SERV_OUT	O	SERVO OUTPUT: Servo output signal
SERV_REF	O	SERVO REFERENCE: Servo reference level

DATA/CLOCK RECOVERY SECTION

RG	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the RD input and enables the read mode/address detect sequences. A low level selects the FREF input.
FREF	I	REFERENCE FREQUENCY: The input can be driven by a direct coupled signal or an AC coupled ECL signal. For minimizing pulse jitter during read, FREF should be stopped by gating it externally with $\overline{VCOE}$.
NRZ1	O	NRZ DATA PORT 1: TTL Version (32P4620): When in read mode NRZ1 is a single ended TTL output for NRZ read data. When in write or idle mode NRZ1 is tristated. Differential Version (32P4621): When in read mode NRZ1 is the NRZ read data output (forms differential output with NRZ2). When in write or idle modes NRZ1 is tri stated.
NRZ2	I/O	NRZ DATA PORT 2: TTL Version (32P4620): NRZ2 is a single ended TTL input for NRZ write data. Differential Version (32P4621): When in read mode NRZ2 is the NRZ read data complementary output (forms differential output with NRZ1). When in write mode NRZ2 is a single ended TTL input for NRZ write data. When in idle mode NRZ is tri stated.
$\overline{WAM}$	I/O	WRITE ADDRESS MARK: The pin is the write address mark input when WG is high. In soft sector mode, a one bit wide low level pulse will write a 7"0," 7"0," 11"0," 11"0" address mark.
$\overline{AMD}$	O	ADDRESS MARK DETECT: The pin is the low level address mark detect output when RG is high. In hard sector mode, the pin is in a high impedance state.
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low. The data is automatically re sychronized to one edge of the FREF input clock.

DATA/CLOCK RECOVERY SECTION (Continued)

NAME	TYPE	DESCRIPTION
RRC/$\overline{\text{RRC}}$	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller, see table 2. During a mode change, no glitches are generated and no more than two lost clock pulsed will occur. Differential Version (32P4621): RRC and $\overline{\text{RRC}}$ form a differential output. TTL Version (32P4620): RRC is a single ended TTL output; $\overline{\text{RRC}}$ is not provided.
$\overline{\text{VCOE}}$	O	VCO ENABLE: A low level selects FREF as the PLL input and a high level selects RD as the PLL input. The switching is done sychronously so that the VCO is restarted in phase with the PLL input.
VCO_CLK	O	VCO CLOCK: An open emitter ECL output test point. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. VCO_CLK and DRD can be used with a test chip to window margin test a drive.
$\overline{\text{DRD}}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.

ANALOG PINS

IREF	I	CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase gain are a function of the current sourced into this pin.
FLTR	I	LOOP FILTER INPUT: Input for passive PLL filter.
PCS	I	WRITE PRECOMPENSATION SET: Pin for RC network to program the write precompensation magnitude value.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	NOM	MAX	UNIT
+5V supply voltage - VPA1,VPA2,VPA3,VPD1,VPD2			6	V
Storage Temperature	65		150	°C
Package Temp. PLCC, QFP (20 sec reflow solder)			215	°C
Pin Voltages: DOUT, $\overline{\text{DOUT}}$, RD, $\overline{\text{WD}}$, NRZ1, NRZ2, $\overline{\text{WAM}}$/$\overline{\text{AMD}}$, $\overline{\text{VCOE}}$, RRC, $\overline{\text{RRC}}$, VCO_CLK, $\overline{\text{DRD}}$	–0.3		VPA/VPD+0.3 or +12	V mA
All other pins	–0.3		VPA/VPD+0.3	V

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified: 4.65 ≤ VPA ≤ 5.25, 4.65 ≤ VPD ≤ 5.25, TBD ≤ Tj ≤ TBD.)

POWER SUPPLY

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
+5 V (VPA/VPD) Supply current	Outputs unloaded, CHIP_EN, SERVO_EN=High			260	mA
Power Dissipation	Outputs unloaded, Tj=145 °C,				
	CHIP_EN,SERVO_EN=High		1.0	1.3	W
	CHIP_EN=High, SERVO_EN=Low			1175	mW
	CHIP_EN,SERVO_EN=Low			925	mW

MODE CONTROL

Power Down Modes

CHIP_EN	SERVO_EN	MODE	DESCRIPTION
1	-	Enable	The entire chip is enabled.
0	1	Servo	Only the parts of the chip necessary to generate the SERV_OUT and DOUT/$\overline{\text{DOUT}}$ outputs are active.
0	0	Disable	The entire chip is in a power down mode.

Pulse Detector Mode Control
(CHIP_EN or SERVO_EN = 1)

WG	$\overline{\text{HOLD}}$	SHORT	MODE	DESCRIPTION
0	1	0	Read	Read amp on, AGC active and controlled by data.
0	0	0	Read/Hold	Read amp on, AGC level held at previous active level
1	-	0	Write	(Read amp gain set to zero) AGC level held at previous active level, AGC inputs shorted by low impedance.
-	-	1	Reset AGC	(Read amp gain set to zero) GAIN pin set for AGC maximum AGC gain, AGC inputs shorted by low impedance

Data/Clock Recovery Mode Control
(CHIP_EN = 1)

WG	RG	MODES	DESCRIPTION
0	1	RD lock	Data/clock recovery PLL locked to read data, $\overline{WD}$ is high.
0	0	FREF lock	Data/clock recovery PLL locked to external FREF reference, $\overline{WD}$ high.
1	0	Write	Data/clock recovery PLL locked to external FREF reference, $\overline{WD}$ active.
1	1	-	Undefined state.

PULSE DETECTOR TRANSITION TIMES

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Enable <–> Disable Transition time	Settling time of external capacitors not included			20.0	µs
Read –> Write Transition Time	WG pin Low –> High			1.0	µs
Write –> Read Transition Time	WG pin High –>Low AGC settling not included	1.2		3.0	µs
Read –> Short Transition Time	SHORT pin Low –> High			1.0	µs
Short –> Read Transition Time	SHORT pin High –> Low AGC settling not included	1.2		3.0	µs
Hold On <–> Hold Off Transition time	$\overline{HOLD}$ pin High <–> Low			1.0	µs

SERIAL DIGITAL INTERFACE
(Refer to Figure 3.)

Register Addresses

A0	A1	A2	A3	DESTINATION
0	0	0	0	Pulse detector mode control
1	0	0	0	Data/clock recovery control register
0	1	0	0	Reserved

SERIAL DIGITAL INTERFACE (Continued)

Pulse Detector Mode Control Register Bit Definition

BITS		DESCRIPTION
D0		Fast attack/decay current control
0		Fast attack/decay enabled
1		Fast attack/decay disabled
D1	D2	Hysteresis level control
0	0	Level always controlled by HYS pin level
0	1	Level fixed at maximum percent of input level
1	0	Level fixed at nominal percent of input level
1	1	Level fixed at minimum percent of input level
D3		Test Mode
0		Normal mode: Read mode can be monitored on $\overline{RD}$ pin.
1		Test mode; Read data can be sent to the data/clock recovery section by driving the $\overline{RD}$ pin.

Data/Clock Recovery Mode Control Register Bit Definition

BITS		DESCRIPTION
D0		Phase detector enable control bit
0		Normal mode
1		Disables the phase detector and allows the VCO to coast (test mode only)
D1		Hard/soft sector control bit
1		Hard sector
0		Soft sector activates the 7 "0," 7 "0," 11"0," 11 "0" pattern soft sector address mark circuitry
D2	D3	Write precompensation magnitude control bits
1	1	Maximum shift
0	1	Second highest shift
1	0	Minimum shift
0	0	No shift

SERIAL DIGITAL INTERFACE (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TSLAT	Setup time; see Figure 3	1.5			µs
THLAT	Hold time; see Figure 3	1.0			µs
TSSDAT	Data setup time; see Figure 3	45			ns
THSDAT	Data hold time; see Figure 3	45			ns

DIGITAL INPUTS AND OUTPUTS

Two versions of the chip are supported:

Digital Inputs and Outputs Common to both versions:
WG, CHIP_EN, SERVO_EN, DATA_EN, SDATA, RG, FREF, SHORT, $\overline{HOLD}$, (These are TTL inputs)
$\overline{VCOE}$, R/$\overline{W}$, $\overline{WD}$ are TTL outputs
$\overline{WAM/AMD}$ is a bidirectional TTL pin
$\overline{RD}$ is a bidirectional pin with TTL input and ECL-like output

TTL version: (32P4620)
NRZ2 is a TTL input
DOUT, NRZ1, RRC are TTL outputs

Differential Digital Output Version: (32P4621)
DOUT, $\overline{DOUT}$, RRC, $\overline{RRC}$, NRZ1, NRZ2 are differential outputs; NRZ2 is also bidirectional and acts as a TTL input.

TTL COMPATIBLE INPUTS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Low Voltage	(VIL)	-0.3		0.8	V
Input High Voltage	(VIH)	2.0		VPD+0.3	V
Input Low Current	VIL = 0.4 V	0.0		0.4	mA
Input High Current	VIH = 2.4 V			100	µA

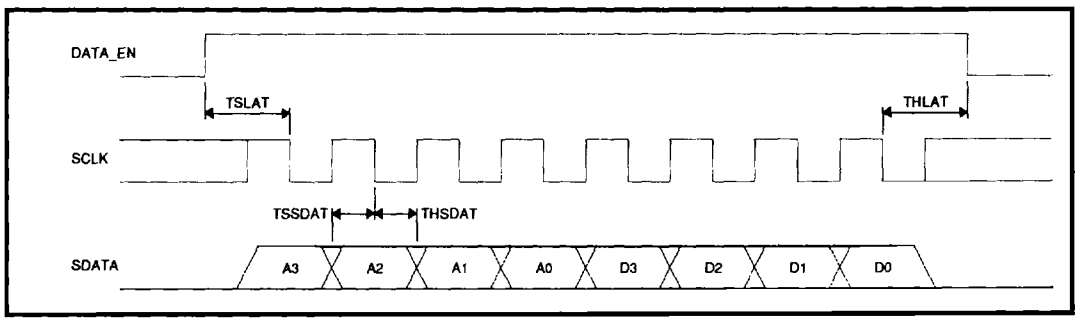


FIGURE 3: Serial Data Interface Timing

TTL COMPATIBLE OUTPUTS

Note: Outputs are loaded with a 4 kΩ resistor to 5V and 15 pF total capacitance (including stray capacitance) to GND for rise/fall time measurements.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output Low voltage	Iol = 4.0 mA			0.4	V
Output High Voltage	Ioh = –400 µA	2.4			V
Output Rise Time	Voh = 2.4 V			9.0	ns
Output Fall Time	Vol = 0.4 V			9.0	ns

DIFFERENTIAL OUTPUTS

Outputs are loaded with a 10 kΩ resistor and 5 pF total capacitance (including stray capacitance) to GND for rise/fall time measurements.

PARAMETER	CONDITION		MIN	MAX	UNIT
Output Low Voltage	–0.5 mA < Iol < 0.5 mA	Tj=25°C	VPD–2.7	VPD–2.5	V
		Tj=145°C	VPD–2.2	VPD–2.0	V
Output High Voltage	–0.5 mA < Ioh < 0.5mA	Tj=25°C	VPD–1.8	VPD–1.7	V
		Tj=145°C	VPD–1.3	VPD–1.2	V
Output Rise Time	Voh = 90% final			6.0	ns
Output Fall time	Vol = 10% final			6.0	ns

ANALOG GAIN SECTION

The circuit is intended to interface with the filter structure shown in Figure 5.
The following measurements are made with the following conditions unless otherwise stated: 1. The circuit is in the read mode (CHIP_EN or SERVO_EN, and $\overline{\text{HOLD}}$ PINS high, WG and SHORT pins low) 2. The circuit is connected as in Figure 5.

Automatic Gain Control Section

The AGC circuit maintains the AC voltage level monitored across the DIN+/- pins at a level defined by the voltage on the AGC pin.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Stage Gain Settings					
K1	K1 = 30 V/V			±17	%
K2	K2 = –2.5 V/V			±5	%
Minimum Gain Range		0.3		20	V/V

Automatic Gain Control Section (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
AGC Loop Level Settings					
DIN+ - DIN- Input Voltage Swing vs. V(AGC)	20mVpp≤V(IN1+–IN1-)≤240mVpp, 0.5Vpp≤V(DIN+ – DIN-)≤1.4Vpp	0.37		0.56	Vpp/V
DIN+ - DIN- Input Voltage Swing When AGC Pin is Open	20 mVpp ≤ V(IN1+ – IN1-) ≤ 240mVpp	0.85	1.0	1.12	%
DIN+ - DIN- Input Voltage Swing Variation	20 mVpp ≤ V(IN1+ – IN1-) ≤ 240mVpp			8.0	%
AGC Pin Input Impedance		4.4		10.8	kΩ
AGC Pin Voltage	V(AGC) = 2.19V, AGC pin open			±11	%
Allowable DIN+ - DIN- Input signal range				1.4	Vpp

AGC Loop Time Constants

Slow AGC Decay Capacitor Charge Current	V(DIN+ - DIN-)=0.0		4.5		µA
Fast AGC Decay Capacitor Charge Current	V(DIN+ - DIN-)=0.0		1.2		mA
Fast Decay Hold Off Time	Slow attack threshold not reached	0.7		0.3	µs
AGC Capacitor Leakage Current	Read/Hold Mode	-0.2		0.2	µA
Slow AGC Attack Capacitor Discharge Current	V(DIN+ - DIN-)=0.8Vdc Vary V(AGC) until slow charge begins.	0.14		0.22	mA
Fast AGC Attack Capacitor Discharge Current	V(DIN+ - DIN-)=0.8Vdc V(AGC)= 3.0V	-1.3		-2.0	mA
Fast –> Slow Attack Switchover Point	V(DIN+ - DIN-) - V(DIN+ - DIN-)Final		0.25		V
Gain Decay Time (Td) (see Figure 7)	Vin = 240 mVpp –> 120 mVpp @ 2.5 Mhz, Vout to 90% of final value		TBD		µs
Gain Attack Time (Ta) (see Figure 7)	WG = high –> low, Vin = 240 mV @ 2.5 Mhz Vout to 110% final value		4		µs

General Amplifier Characteristics

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Input Voltage Range		20		240	mVpp
Differential Input Resistance	V(IN1+ - IN1-) = 100 mVpp @ 2.5 Mhz		5.0		kΩ
Differential Input Capacitance	V(IN1+ - IN1-)=100 mVpp			10.0	pF
Common Mode Input	SHORT pin = low		1.8		kΩ
Impedance (both sides)	SHORT pin = high		250		Ω
Input Noise	Gain set to Maximum			30	$nV/\sqrt{Hz}$
Differential Output Resistance OUT1+/-		16		60	Ω
Output Offset Voltage				±100	mV
Maximum Output Voltage Swing	Set by GAIN pin voltage Z(load diff) = 600Ω	0.56			Vpp
OUT1+ to OUT1- Pin current	No DC path from OUT+/- to GND	±1.1			mA
Bandwidth	Gain set to maximum, ±3 dB bandwidth	30			MHz
Common ModeRejection Ratio (Input Referred)	V(IN1+)=V(IN1-)=100 mVpp, 5 Mhz, Gain set to maximum	40			dB
Power Supply Rejection Ratio (Input Referred)	V(VPA/VPD) = 100 mVpp 5 MHz, Gain set to maximum	30			dB

Adjustable Real and Imaginary Zero Filter Section

See applications section for equations governing generation of real/imaginary axis zeros. All the following measurements are made with LP3+ tied to HP3+ and to a 180Ω resistor to VPA and with LP3- tied to HP3- and to a 180Ω resistor to VPA.

PARAMETER	CONDITION	MIN	MAX	UNITS
Stage Gain Settings				
K4	K4 = 0.0031Ω		±TBD	%
M1	M1 = [7.5 x V(MULT_1)]/V(VREF)		±TBD	%
Minimum M1 Range		0.1	7.0	V/V
M2	M2 = 0.75[V(MULT_2)–0.1]/V(VREF)		±TBD	%
Minimum M2 Range		0.01	0.5	V/V
Allowable Load Resistor Range	180Ω per side to VPA		±5	%

Adjustable Real and Imaginary Zero Filter Section (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
General Amplifier Char.					
Output Offset Voltage				±100	mV
Differential Input Resistance	V(LP2/HP2+ - LP2/HP2-) = 100 mVpp, 2.5 MHz (LP2+ - LP2-) or (HP2+ - HP2-)		10		kΩ
Differential Input Capacitance	V(LP2/HP2+ - LP2/HP2-) = 100 mVpp, 2.5 MHz (LP2+ - LP2-) or (HP2+ - HP2-)			10.0	pF
Common Mode Input Impedance (Both sides)	(LP2+ - LP2-) or (HP2+ - HP2-)		3.3		kΩ
Bandwidth	Gain set to maximum, +3 dB bandwidth	30			MHz
LP3+, LP3, HP3+, HP3 pin current	With LP2+/- and HP3+/- shorted, (LP2+ + HP2+) or (LP2- + HP2-)	1.7			mA
Common Mode Rejection Ratio (Input referred)	V(LP2+)=V(LP2-)=100 mVpp, or V(HP2+)=V(HP2-)=100 mVpp 5 MHz, gain set to maximum	40			dB
Power Supply Rejection Ratio (Input referred)	ΔV(VPA/VPD)=100 mVpp, 5 MHz, Gain set to maximum	30			dB
Differential Output Resistance	(LP3+ - LP3-) or (HP3+ - HP3-)	10			kΩ
MULT_1 Current				±3	mA
MULT_2 Current				±10	mA

Gain Buffer to Differentiator and Matched Delay Section
See applications section for equations development. All of the following measurements are made with a 500Ω resistor tied from OUT4+ to OUT4-.

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Gain	Av = 2.5 V/V			±15	%
Differential Input Resistance	V(IN4+ - IN4-) = 100 mVpp, 2.5 MHz		10		kΩ
Differential Input Capacitance	V(IN4+ - IN4-) = 100 mVpp, 2.5 MHz			10	pF
Common Mode Input Impedance	Both sides		3.0		kΩ

Gain Buffer to Differentiator and Matched Delay Section

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Differential Output Resistance OUT4+/-		10		32	Ω
Maximum Output Voltage Swing	Z(load diff.) = 350 Ω	1.4			Vpp
OUT4+ to OUT4- Pin current	No DC path from OUT+/- to GND	±2.3			mA
Output Offset Voltage				±50	mV
Bandwidth	Gain set to maximum,	30			MHz
Common Mode Rejection Ratio (Input referred)	V(IN4+) = V(IN4-)=100 mVpp, 5 Mhz, Gain set to maximum	40			dB
Power Supply Rejection Ratio (Input referred)	V(VPA/VPD) = 100 mVpp, 5 Mhz, Gain set to maximum	30			dB

Voltage Reference Generator Section

An on-chip reference voltage is generated for use as a reference by the external DACs which supply the MULT_1 and MULT_2 voltages.

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Output Voltage on VREF Pin	0.4 mA < I(VREF) < 1.1 mA	1.9	2.2	2.5	V

READ MODE DIGITIZING SECTION

All of the measurements in the read digital section are made with the following conditions unless otherwise stated:

1. In the read mode, (CHIP_EN high, WG & SHORT pins low)
2. The clock and data input (CIN+ - CIN) and (DIN+ - DIN-), receive AC coupled 2.5 MHz, 1.0 Vpp sine-wave input signals with the DIN+/- input leading CIN+/- by 90 degrees.
3. A 1.8V DC voltage is applied to HYS pin.
4. The $\overline{RD}$ and DOUT pins are loaded with a 10 kΩ resistor and 5 pF total capacitance to GND.

Hysteresis Comparator Circuit

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Input Signal Range				1.4	Vpp
Differential Input Resistance	V(DIN+ - DIN-) = 100 mVpp, 2.5 Mhz	10		16.5	kΩ
Differential Input Capacitance	V(DIN+ - DIN-) = 100 mVpp, 2.5 Mhz			4.0	pF

Hysteresis Comparator Circuit (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Common Mode Input Impedance	Both sides	2.5		4.0	kΩ
LEVEL Pin Output Voltage vs DIN+ - DIN- Input voltage	0.6 < V(DIN+ - DIN-)<1.4 Vpp 10 kΩ between LEVEL & GND	1.3		2.2	V/Vpp
LEVEL Pin Output Impedance	I(LEVEL) = 0.5 mA		140		Ω
LEVEL Pin Maximum Output Current		3.0			mA
Comparator Offset Voltage	HYS pin at GND, ≤1.5 kΩ across DIN+, DIN-			±10	mV
Hysteresis Trip Voltage (at DIN+, DIN-) vs. HYS pin voltage	1V < V(HYS) < 2V	0.44	0.5	0.64	Vpp/V
Hysteresis Threshold Margin as a % of V(DIN+ - DIN-) Peak	V(HYS) = some % of V(AGC)* or V(LEVEL), 1V < V(HYS) < 3V See Figures 18 & 19	-15		+15	% Peak
HYS Pin Input Current	1V < V(HYS) < 3V	0.0		-20	µA

*In an open loop configuration where reference is V(AGC) tolerance may be slightly higher

TABLE 1: Frequency Template of Hysteresis Trip Point as Percent of Peak Input Voltage Across DIN+/– Pins

Frequency	Hysteresis			
	External	High	Medium	Low
0 to TBD MHz	TBD to TBD %	TBD to TBD %	TBD to TBD %	TBD to TBD %
TBD MHz	TBD to TBD %	TBD to TBD %	TBD to TBD %	TBD to TBD %

Note 1: Pulse detector mode control register bits D1, 2 set as follows:

00 = External hysteresis

10 = About 65% hysteresis

01 = About 50% hysteresis

11 = About 35% hysteresis

Note 2: For external hysteresis, LEVEL/HYS pin network is set up with external component values as shown in Figure 5a.

Clocking Circuit

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Input Signal Range				1.4	Vp-p
Differential Input Resistance	V(CIN+ - CIN-) = 100 mVp-p, 2.5 Mhz	10		16.5	kΩ
Differential Input Capacitance	V(CIN+ - CIN-) = 100 mVp-p, 2.5 Mhz			4.0	pF
Common Mode Input Impedance	Both sides	2.7		3.8	kΩ
Input Offset Voltage				6.0	mV
COUT Pin Output Low Voltage	TIE 2 kΩ from COUT to GND		VPA-3.0		V
COUT Pin Output Pulse Voltage V(high) - V(low)	TIE 2 kΩ from COUT to GND		+0.8		V
COUT Pin Output Pulse Width	TIE 2 kΩ from COUT to GND		12		ns

Read Mode Digital Section as System

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Required DFF Set up Time, (Td1 in Figure 8)	Minimum allowable time delay from V(DIN+, DIN) exceeding hysteresis point to V(CIN+,CIN) crossing zero	0			ns
Propagation Delay Td3 in Figure 8				60	ns
Pulse Pairing	|Td3-Td4| in Figure 8			1.0	ns
RD Pin Output Pulse Width	0.0 < Ioh < 0.5 mA		10		ns
RD Pin Output Low Voltage	0.0 < Iol < 0.5 mA		VPA-2.1		V
RD Pin Output Pulse Voltage V(high)-V(low)	0.0 < Ioh < 0.5 mA		+0.8		V

Servo Burst Capture Circuit
All of the measurements for the servo are made with the following conditions unless otherwise stated. The circuit is connected as shown in Figure 5.

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
SERV_REF Pin Level		VPA-2.8		VPA-2.1	V
SERV_OUT to SERV_REF Offset	DIN+ shorted to DIN-			±20	mV
SERV_OUT Level vs AGC Pin Voltage	$\frac{V(SERV\_OUT)}{V(AGC)} = 0.2\ Vp/V$			±TBD	%
Servo Frame vs. V(DIN+/-)	$\frac{V(SERV\_OUT - SERV\_REF)}{V(DIN+/-)}$ = 0.39 Vp/Vpp			TBD	Vp/Vpp
Allowable Load Impedance SERV_OUT or SERV_REF to GND	Equivalent parallel resistance	10			kΩ
	Equivalent parallel capacitance			5	pF

CLOCK/DATA RECOVERY SECTION:
See applications section for loop filter development.

DC Output levels

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Test Point Output High Level (VOHT) $\overline{DRD}$, VCO_CLK, VCO_REF	262Ω to VPD,402Ω to GND VPA = VPD	VPD-1.02			V
Test Point Output Low Level (VOLT) $\overline{DRD}$, VCO_CLK, VCO_REF	262Ω to VPD,402Ω to GND VPA = VPD			VPD-1.625	V

Read Mode

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Read Clock Rise Time (TRRC)	0.8V to 2.0V, C1 ≤ 15 pF			8	ns
Read Clock Fall Time (TFRC)	2.0V to 0.8V, C1 ≤ 15 pF			5	ns
NRZ (out) Set Up and Hold Time (TPNRZ)		.31 TORC			ns
$\overline{AMD}$ Propagation Delay (TPAMD)		10			ns
1/3 Cell Delay	TD = 4.92(RR + 0.53) RR = 2.0 kΩ to 7.0 kΩ	0.8TD		1.2TD	ns

Write Mode

PARAMETER	CONDITION	MIN	MAX	UNIT
Write Data Pulse Width (TWDC)	C1 < 15 pF	$\frac{2TOWC}{3}$ - 2TPC - 5	$\frac{2TOWC}{3}$ +5	ns
Write Data Fall Time (TFWD)	2.0V to 0.8V, C1 ≤ 15 pF		8	ns
Write Data Clock Rise Time (TWRC)	0.8V to 2.0V, C1 < 15 pF		10	ns
Write Data Clock Fall Time (TWFC)	2.0 to 0.8V C1 < 15 pF		8	ns
NRZ Set Up Time (TSNRZ)		5		ns
NRZ Hold Time (THNRZ)		5		ns
Precompensation Time Shift Magnitude Accuracy (TPC)	TPCO = T x A/(B+3A) See note			
	D2 bit=1, D3 bit=1	0	0	ns
	D2 bit=0, D3 bit=1	0.8TPC-0.2	1.2TPC+0.2	ns
	D2 bit=1, D3 bit=0	2(0.8TPC)	2(1.2TPC)	ns
	D2 bit=0, D3 bit=0	3(0.8TPC)	3(1.2TPC)	ns

Note: T = FREF period, A=0.19/(Rpc+0.51)+0.0058, B=0.42/(RR+0.53)+0.0108, Rpc & RR in kΩ

Data Synchronization

PARAMETER	CONDITION	MIN	MAX	UNIT
VCO Center Frequency Period (TVCO)	VCO IN = 2.7V, TO=4.03(RR+1.33), VPA, VPD = 5.0V, RR=2.0 kΩ to 7.0 kΩ	0.8TO	1.2TO	ns
VCO Frequency Dynamic Range	1.0V≤VCO IN≤VPA-0.6V VPA, VPD = 5.0V	±25	±45	%
VCO Control Gain (KVCO)	ωo = 2 x π/TO, 1.0V≤VCO IN≤VPA-0.6V	0.14ωo	0.26ωo	$\frac{rad}{VxS}$
Phase Detector Gain (KD)	For PLL REF=FREF, KD=0.095/(RR+530) For PLL REF=RD, KD=0.19/(RR+530) VPA, VPD = 5.0V	0.83KD	1.17KD	A/rad
KVCOxKD Product Accuracy		-28	+28	%
VCO Phase Restart Error	Referred to RRC	-1	+1	rad
Decode Window Centering Accuracy			±1.0	ns
Decode Window		(2TORC/3) -1.5		ns

APPLICATIONS SECTION

ADJUSTABLE REAL AND IMAGINARY ZERO FILTER SECTION

With external components connected as in Figure 5a, this section generates a pair of symmetric real axis zeros whose position is controlled by the voltage on the MULT_1 pin.

$$Hl(s) = \frac{1}{(L1a + L1b)\,C2 \cdot s^2 + (L1a + L1b/3)s + 1} - \frac{Ml \cdot L5 \dfrac{C4a \cdot C4b}{C4a \cdot C4b} \cdot s^2}{L5 \cdot \dfrac{C4a \cdot C4b}{C4a \cdot C4b} \cdot s^2 + (L5/R6)s + 1}$$

$$= \frac{1 - Ml \cdot L \cdot C \cdot s^2}{LCs^2 + (L/R)s + 1}$$

for: $L = L5 = 2 \cdot L1a = 2 \cdot L1b$
$C = C2 = 0.5 \cdot C4a = 0.5 \cdot C4b$

With the external components connected as in Figure 5a, this section also generates a pair of symmetric imaginary axis zeros whose position is controlled by the voltage on the MULT_2 pin.

$$H2(s) = K4 \cdot \frac{M2(L8a + L8b) \cdot C7 \cdot s^2 + 1}{(E \cdot s^N) + (F \cdot s^{N-1}) + \ldots + 1} \cdot (R12a + R12b)$$

With the external components connected as in Figure 6a, this section can also generate two pairs of symmetric complex zeros whose position is controlled by the voltage on the MULT_2 pin.

$$H2(s) = K4 \cdot \frac{(M2 \cdot A \cdot s^4) + (M2 \cdot B \cdot s^2) + 1}{(E \cdot s^N) + (F \cdot s^{N-1}) + \ldots + 1} \cdot (R12a + R12b)$$

where $A = Cg \cdot C7 \cdot 2L10 \cdot 2L8$
$B = (C7 \cdot 2L8) + (C7 \cdot 2L10) + (Cg \cdot 2L10)$

GAIN BUFFER TO DIFFERENTIATOR AND MATCHED DELAY SECTION

With external components conncected as in Figure 5a, this section generates the differentiated signal applied to CIN+/- and a signal with a matched delay applied to DIN+/-.

$$Hcin(s) = \frac{\dfrac{C16a \cdot C16b}{C16a + C16b} \cdot R17 \cdot s}{(L15a + L15b) \cdot \dfrac{C16a \cdot C16b}{C16a + C16b} \cdot s^2 + \dfrac{C16a \cdot C16b}{C16a + C16b} \cdot R17 \cdot s + 1}$$

$$= \frac{CRs}{LCs^2 + CRs + 1}$$

For: $L = 2 \cdot L15a = 2 \cdot L15b$
$C = 0.5 \cdot C16a = 0.5 \cdot C16b$
$R = R17$

$$Hdin(s) = \frac{1}{(L18a + L18b) \cdot C19 \cdot s^2 + C19 \cdot R20 \cdot s + 1}$$

$$= \frac{1}{LCs^2 + CRs + 1}$$

For: $L = 2 \cdot L18a = 2 \cdot L18b$
$C = C19$
$R = R20$

LOOP FILTER

The low pass filter attenuates high frequency components fo the phase error signal from the phase detector and modifies the dynamics of the PLL. In lock mode, the PLL can be approximated by the linear model shown in Figure 4. The transfer functions of the blocks are as follows:

KD = conversion factor for phase detector in µA/radian
KVCO = VCO gain factor in radians/volt-second
F(s) = low pass filter transfer function

Thus the closed loop transfer function is:

$$H(s) = \frac{\frac{KD \cdot Kvco \cdot F(s)}{N}}{s + \frac{KD \cdot Kvco \cdot F(s)}{N}}$$

where: N = ratio between TBD and FIN
N = 1.0 for preamble
N= 0.5 for external clock

For the low pass filter example:

$$F(s) = \frac{1 + sC1R}{sC1\left(1 + \frac{C2}{C1} + sC2R\right)}$$

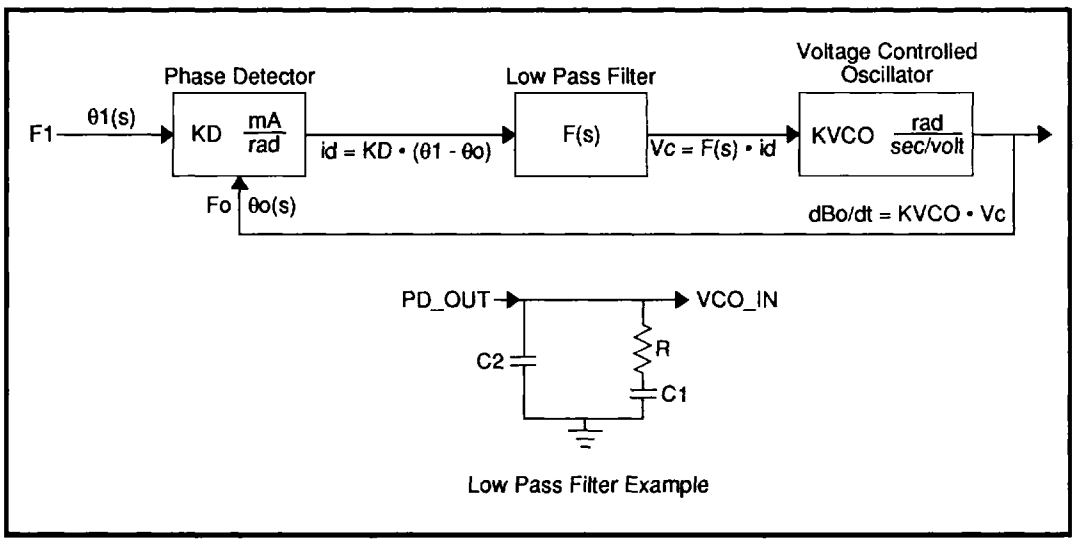


FIGURE 4: Phase Locked Loop

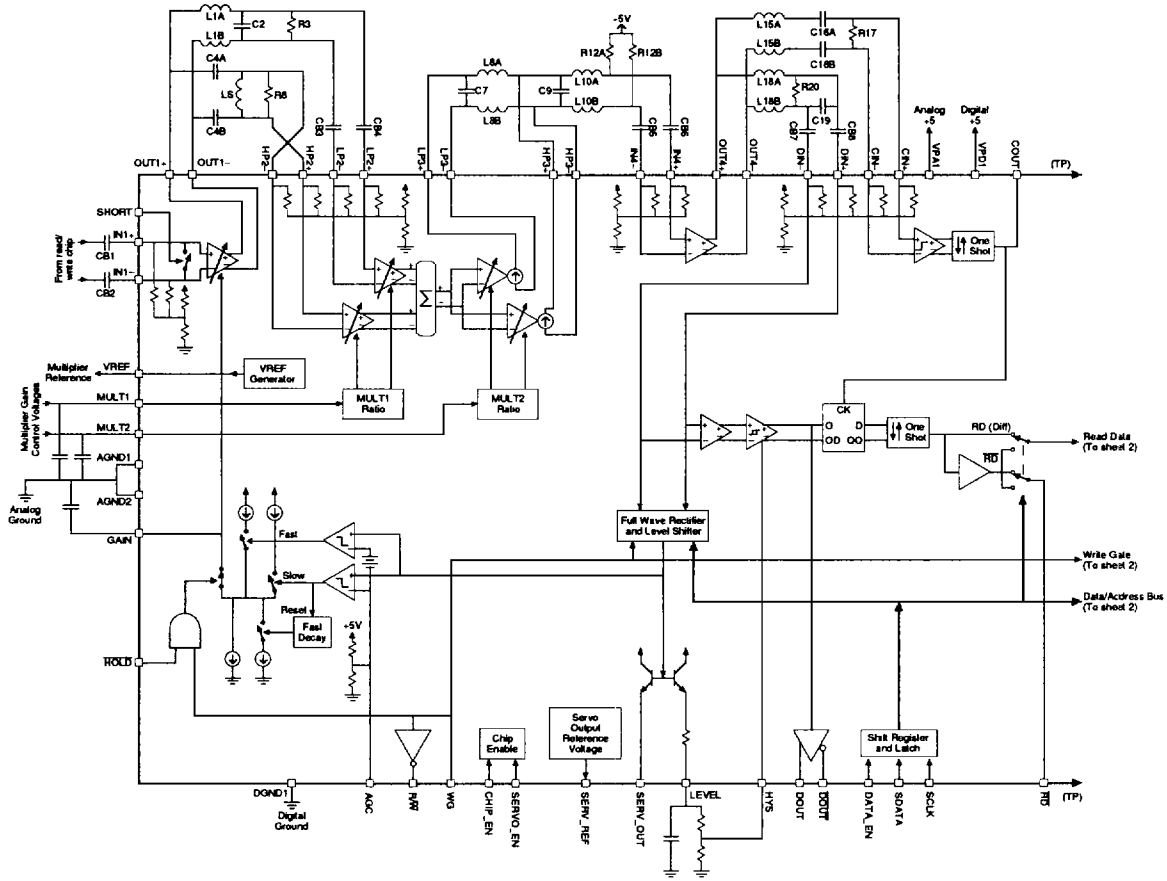


FIGURE 5a: SSI 32P4621 Circuit Block Diagram - Differential Output Data Version - Sheet 1

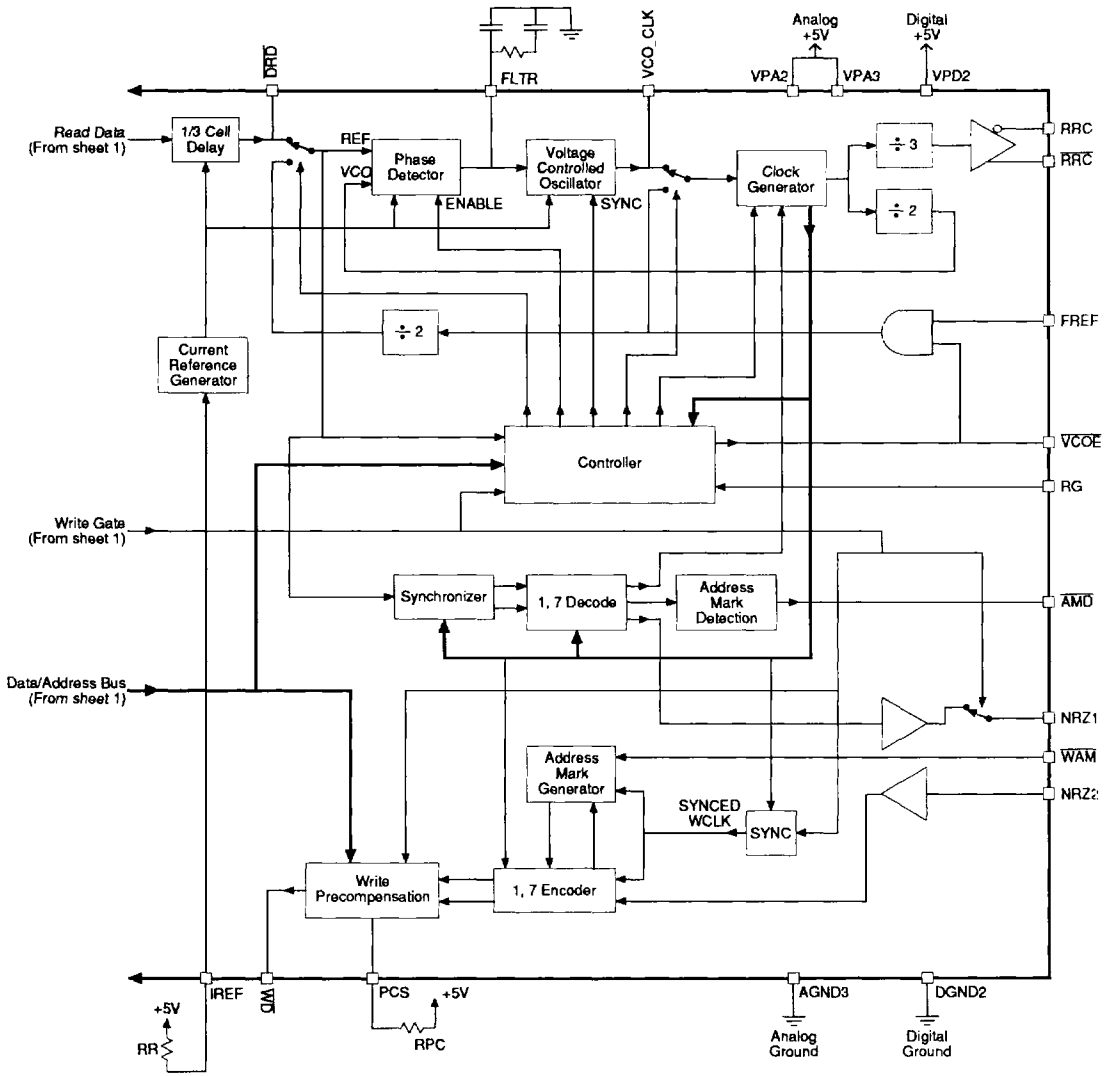


FIGURE 5b: SSI 32P4621 Circuit Block Diagram - Differential Output Data Version - Sheet 2

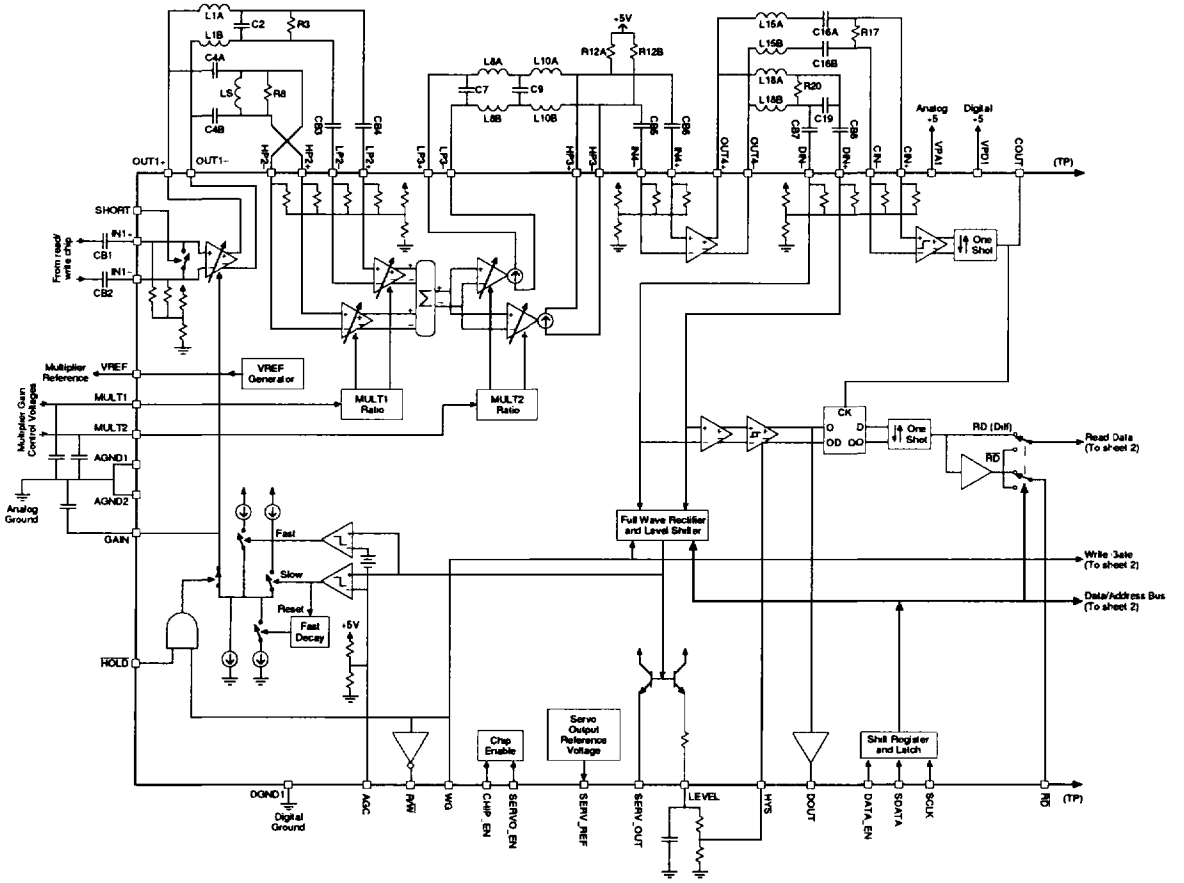


FIGURE 6a: SSI 32P4620 Circuit Block Diagram - Single Ended Output Data Version - Sheet 1

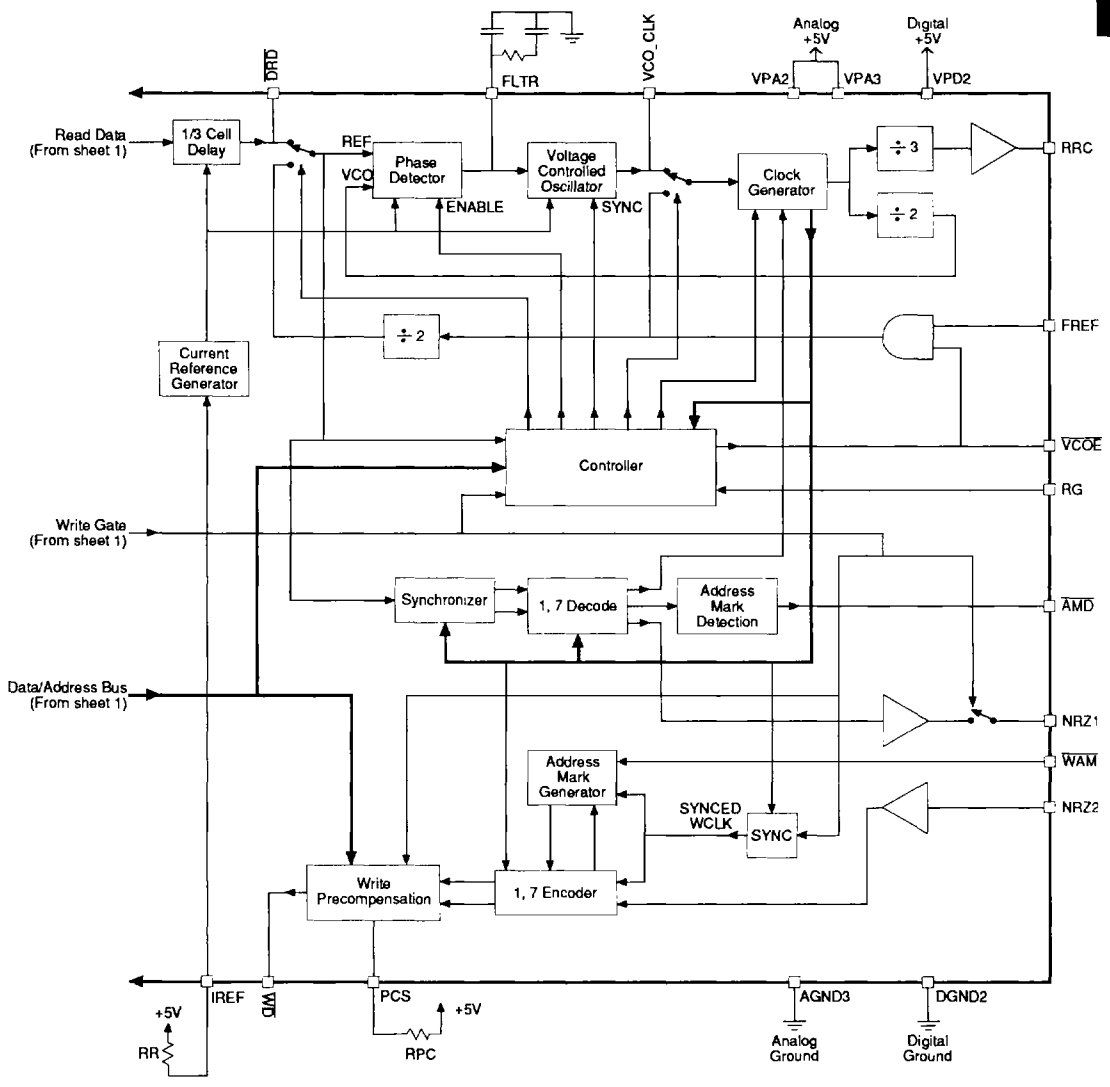


FIGURE 6b: SSI 32P4620 Circuit Block Diagram - Single Ended Output Data Version - Sheet 2

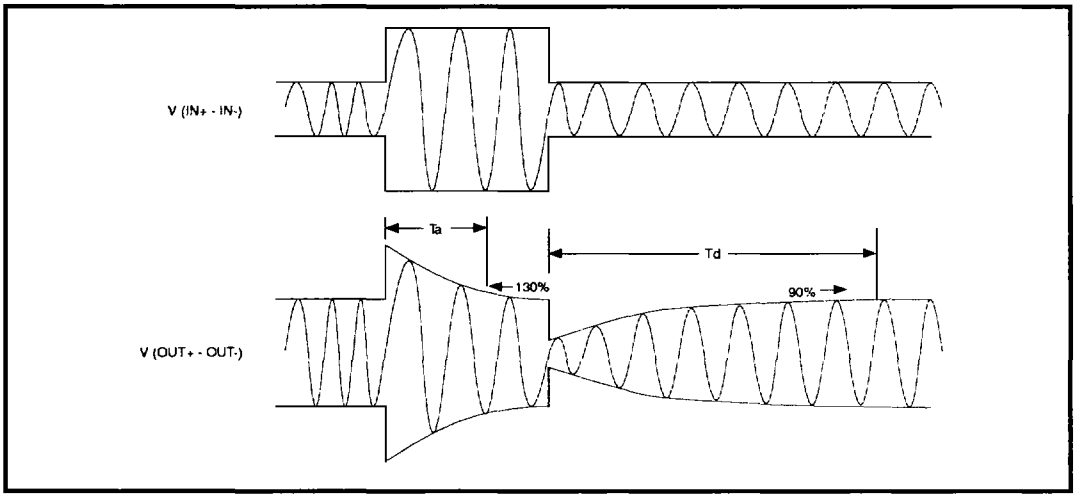


FIGURE 7: AGC Timing Diagram

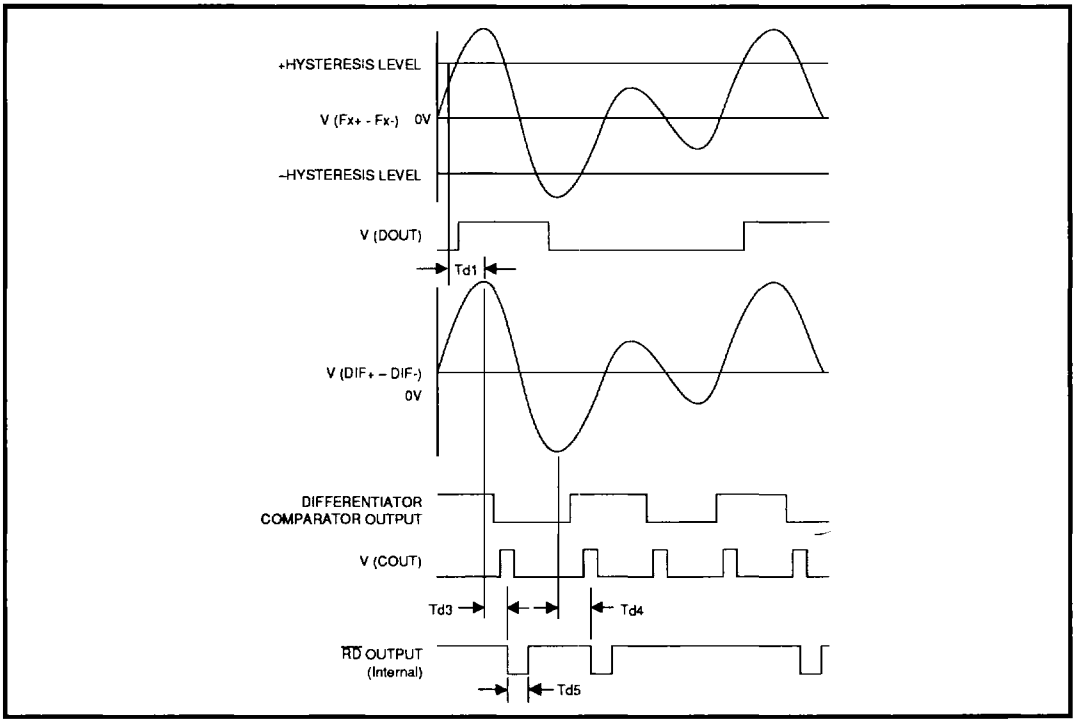


FIGURE 8: Read Mode Digital Section Timing Diagram

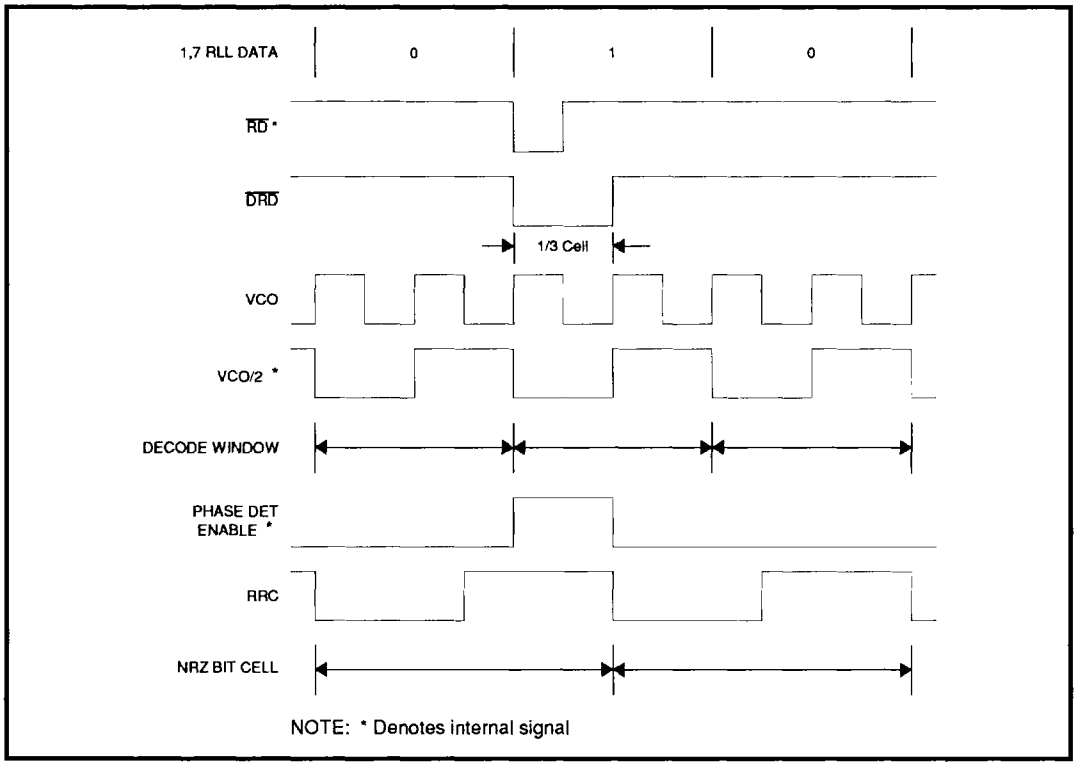


FIGURE 9: Data Synchronization Waveform

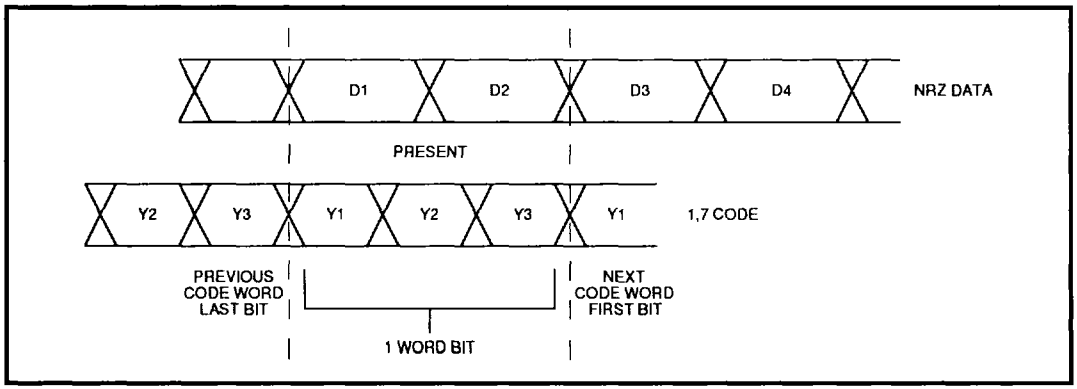


FIGURE 10: NRZ Data Word Comparison to 1, 7 Code Word Bit
(See Table 1 for decode scheme)

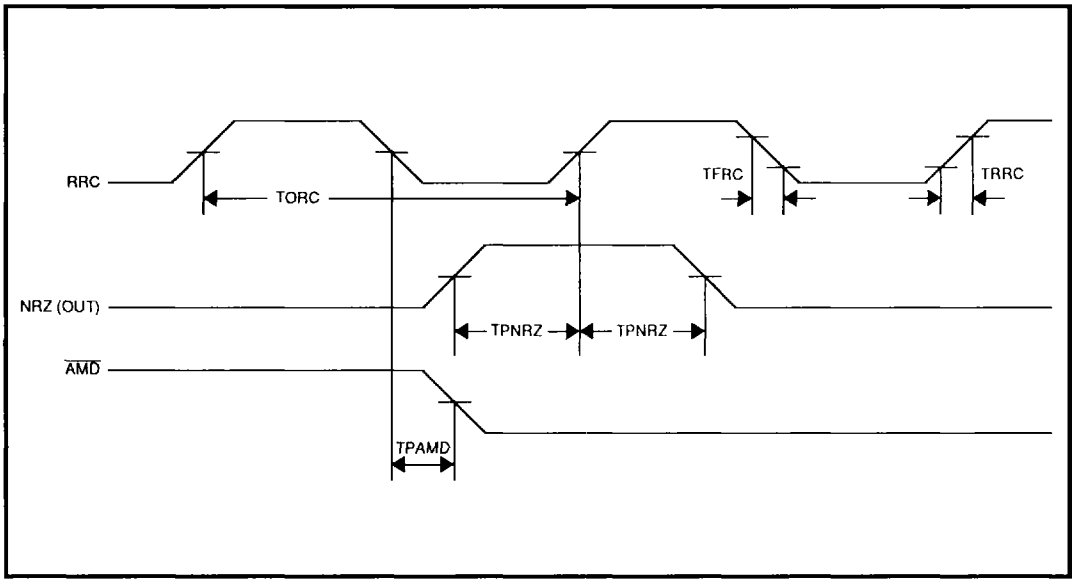


FIGURE 11: Read Timing

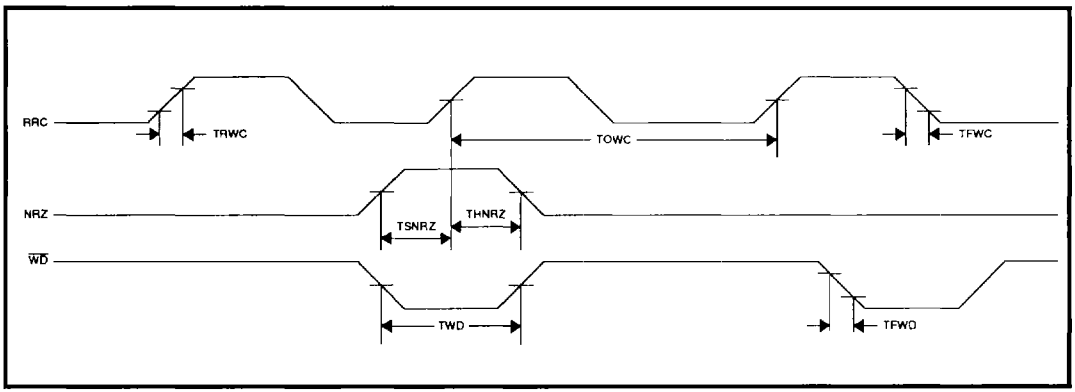
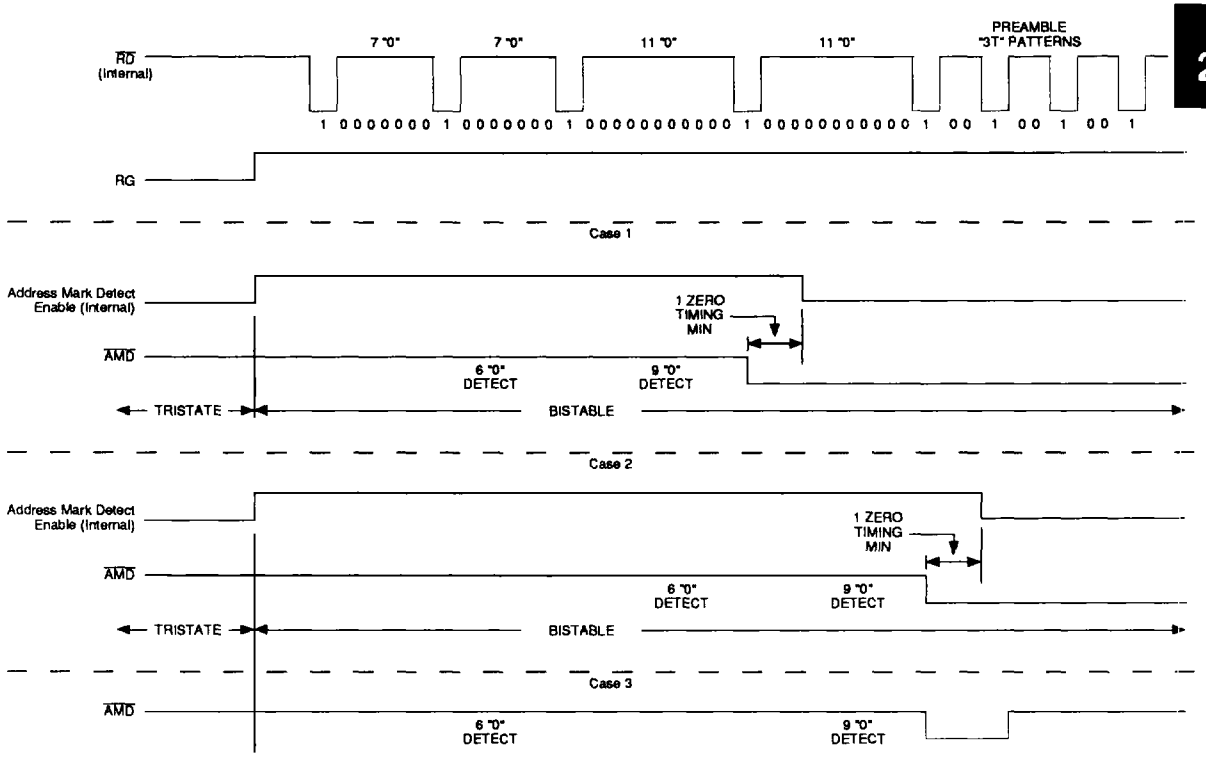


FIGURE 12: Write Timing



If 5 bits of RD are detected after 6 "0" and before 9 "0" are found, then restart and look for 6 "0."

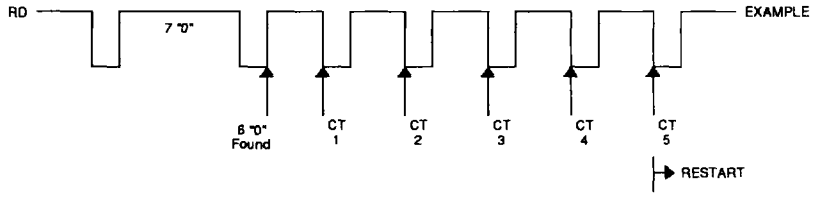
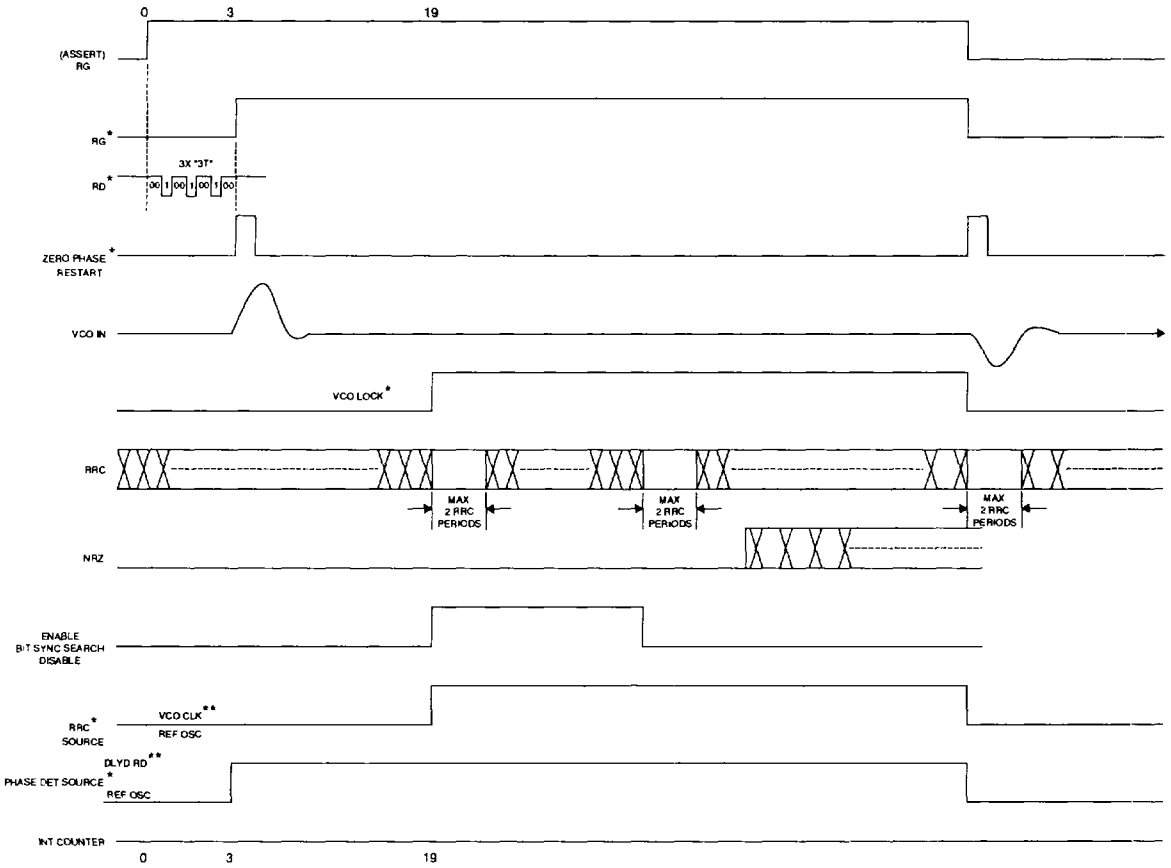


FIGURE 13: Address Mark Search



* = – Internal Source

** = – Test Point

FIGURE 14: Read Mode Locking Sequence (Soft and Hard Sector)

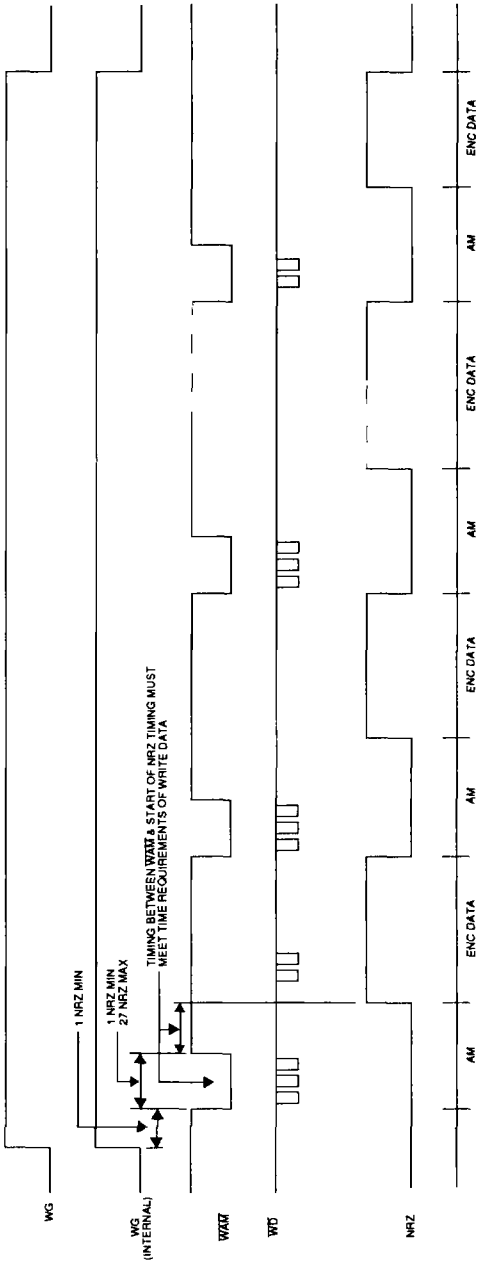


FIGURE 15: Multiple Address Mark Write

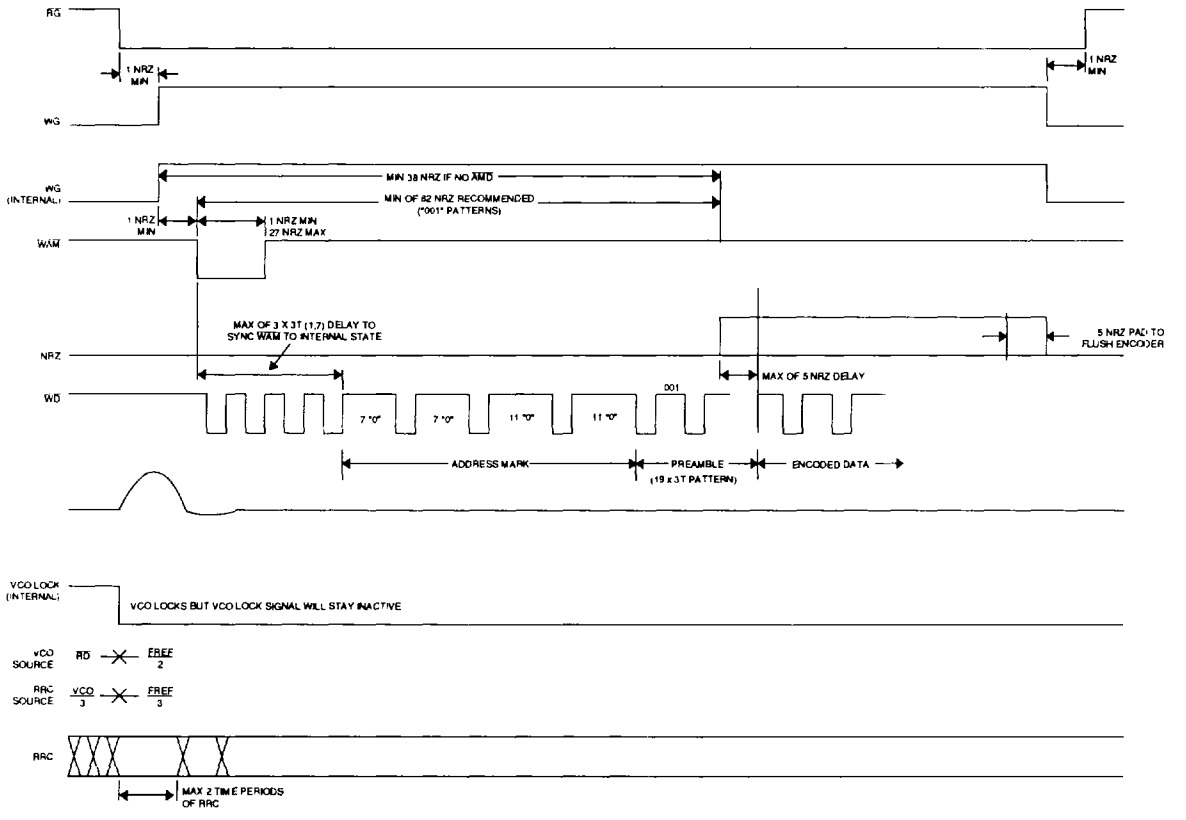


FIGURE 16: Write Data

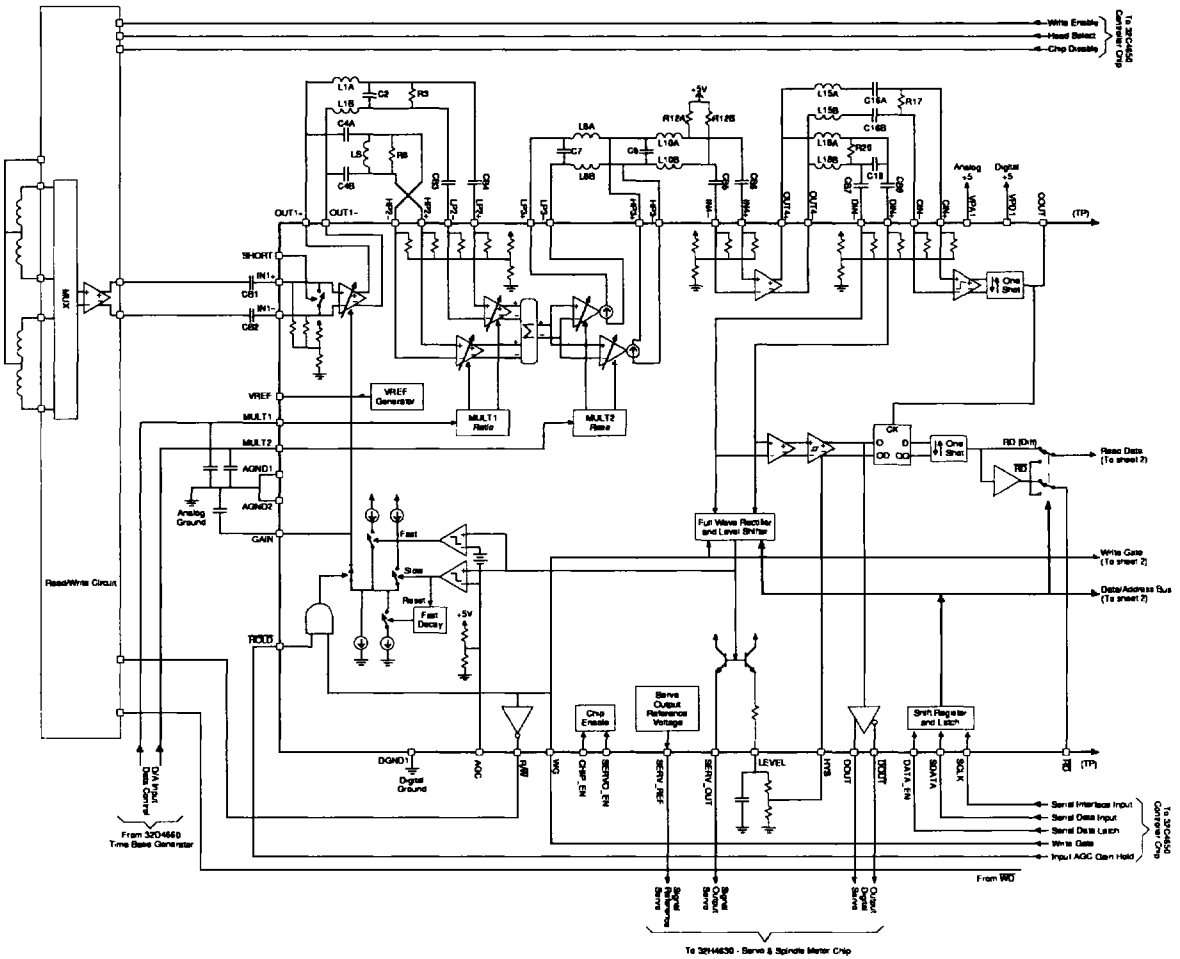


FIGURE 17a: System Configuration - Sheet 1

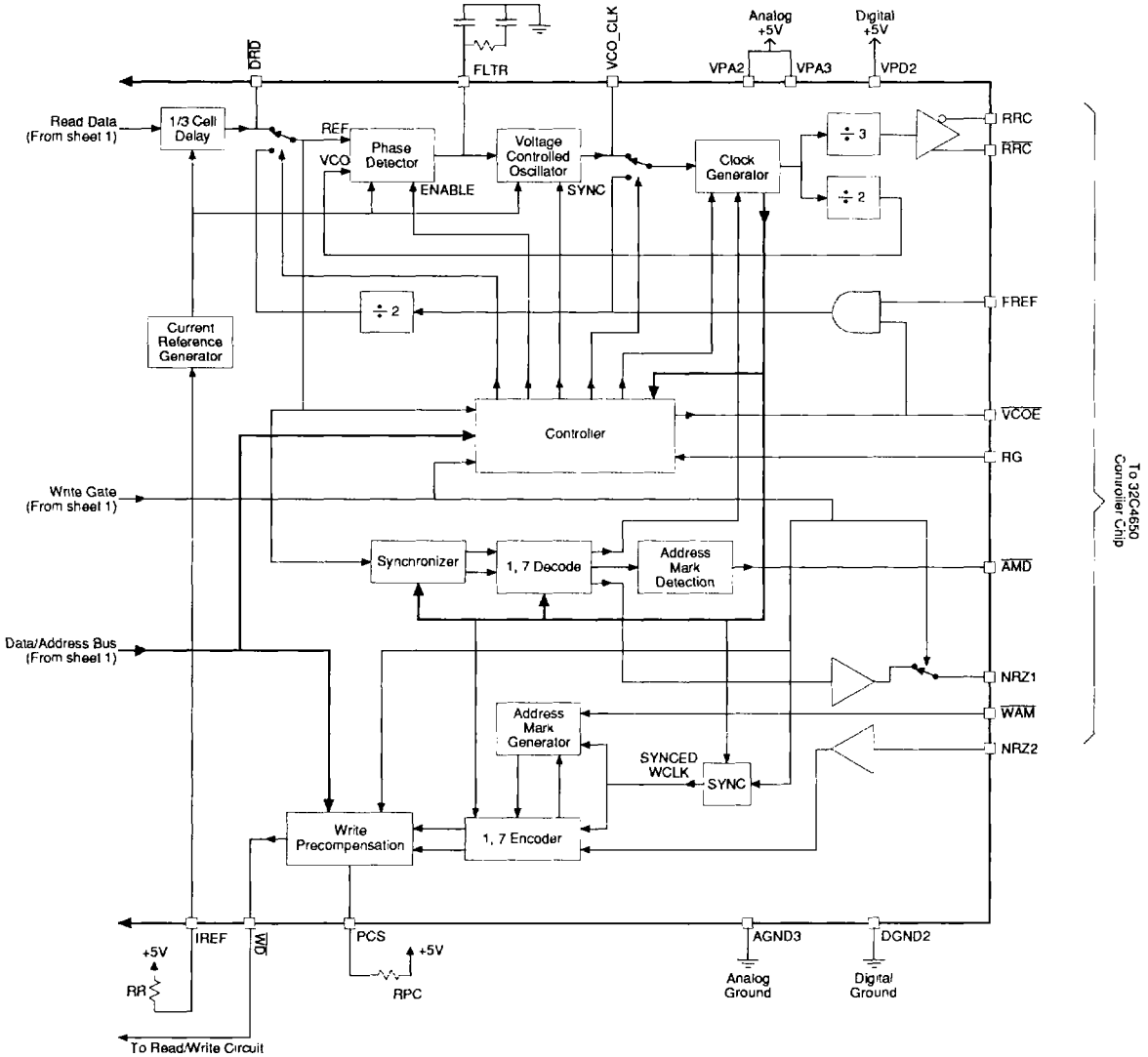


FIGURE 17b: System Configuration - Sheet 2

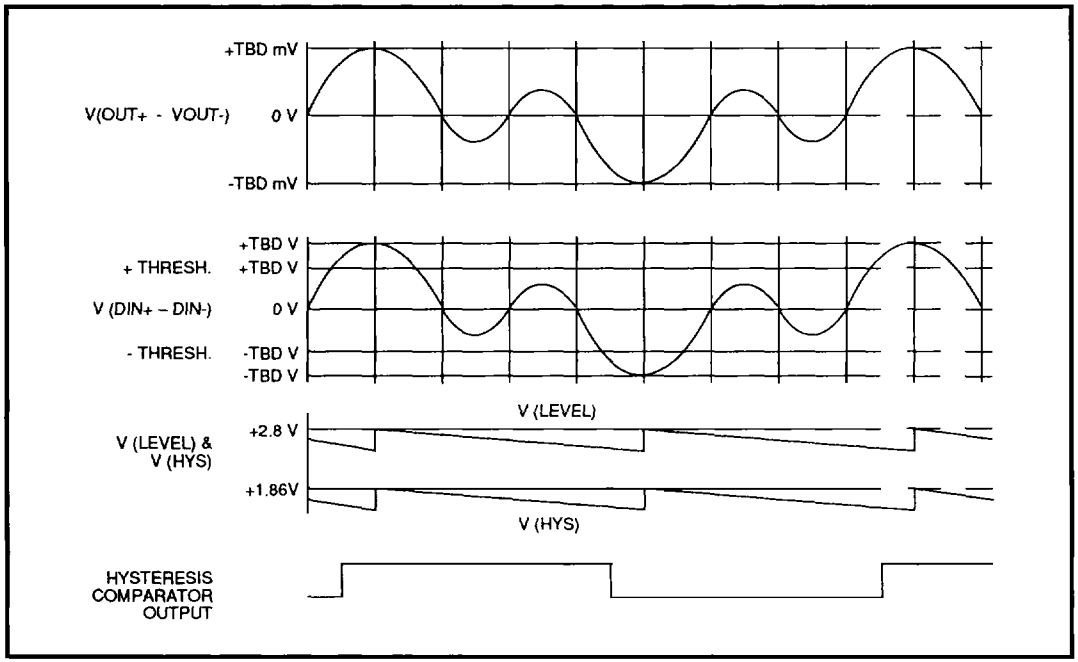


FIGURE 17c: Expected Nominal Voltage Levels

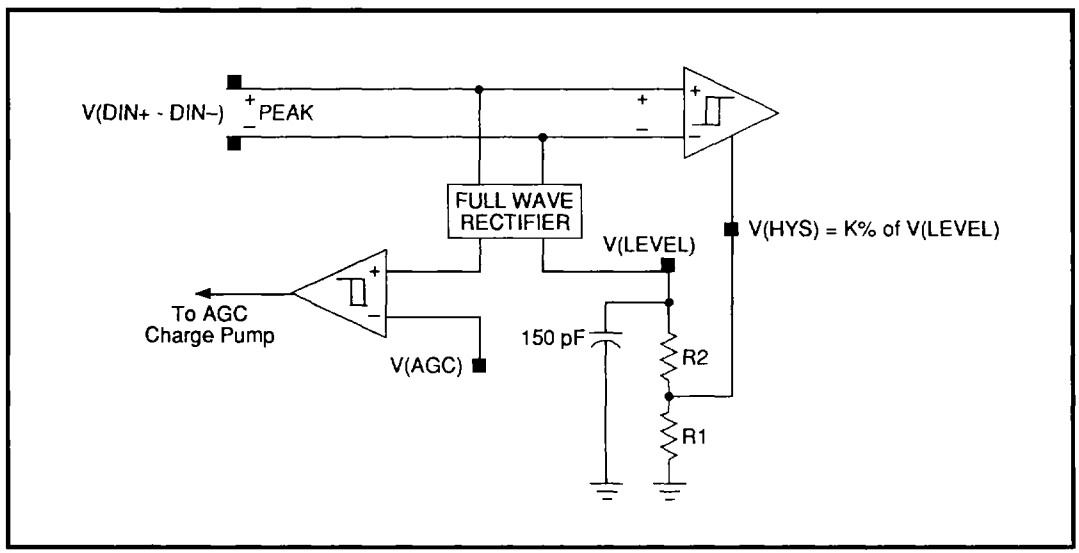


FIGURE 18: Feed forward Mode

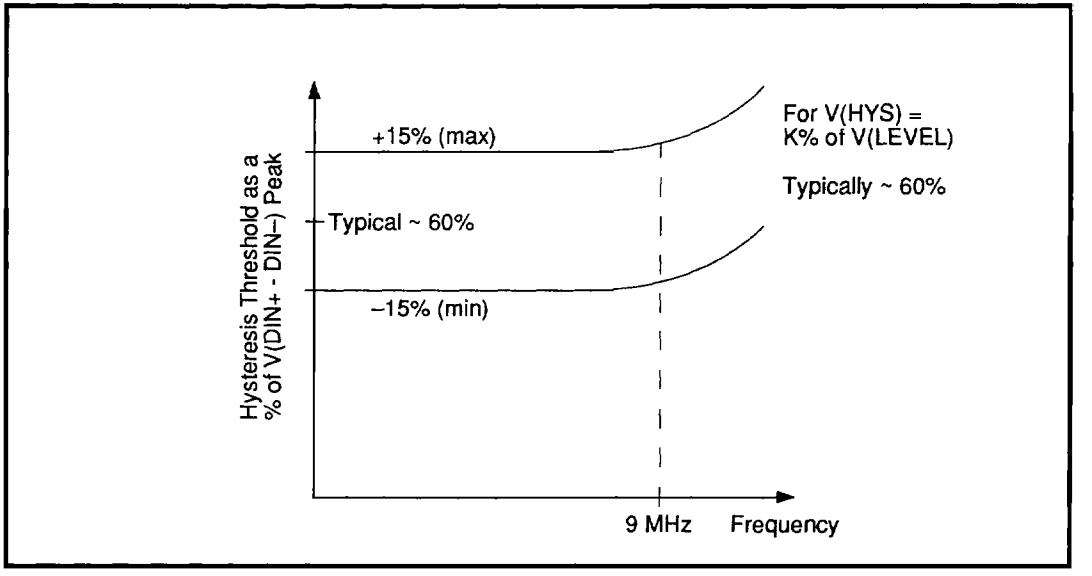


FIGURE 19: Percentage Threshold vs. Frequency

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457