

## MSM511001B

1,048,576-Word × 1-Bit DYNAMIC RAM : NIBBLE MODE TYPE

### DESCRIPTION

The MSM511001B is a new generation dynamic RAM organized as 1,048,576-word × 1-bit. The technology used to fabricate the MSM511001B is OKI's CMOS silicon gate process technology. The device operates at a single 5V power supply. Its I/O pins are TTL compatible.

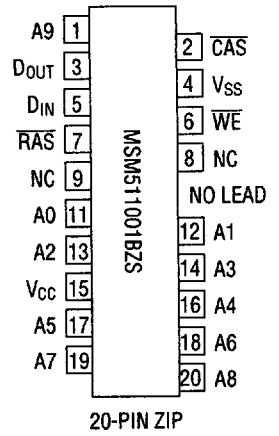
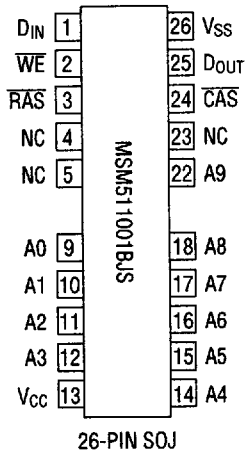
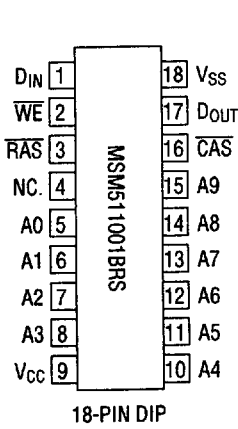
### FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1-transistor memory cell
- 1,048,576-word × 1-bit organization
- Single 5V power supply, ±10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate
- Refresh: 512 cycles/8ms
- Common I/O capability using Early Write operation
- Nibble mode, read modify write capability
- CAS before RAS refresh, Hidden refresh, RAS only refresh capability
- Package:
  - 18-Pin 300mil Plastic DIP (DIP18-P-300-W1)
  - 26-Pin 300mil Plastic SOJ (SOJ26-P-300)
  - 20-Pin 400mil Plastic ZIP (ZIP20-P-400)

### PRODUCT FAMILY

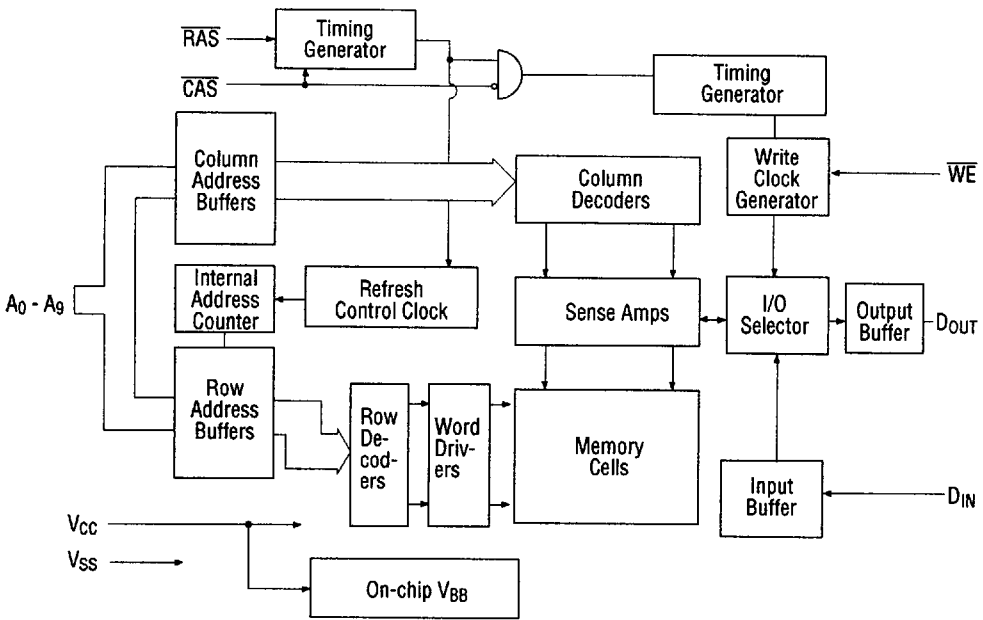
Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>		Operating (Max.)	Standby (Max.)
MSM511001B-60	60ns	30ns	15ns	120ns	495mW	5.5mW
MSM511001B-70	70ns	35ns	20ns	130ns	440mW	
MSM511001B-80	80ns	40ns	20ns	150ns	385mW	
MSM511001B-10	100ns	50ns	25ns	190ns	330mW	

**PIN CONFIGURATION (TOP VIEW)**



Pin Name	Function
A0 - A9	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
D <sub>IN</sub>	Data Input
D <sub>OUT</sub>	Data Output
WE	Write Enable
V <sub>CC</sub>	Power Supply (5V)
V <sub>SS</sub>	Ground (0V)
NC	No Connection

### FUNCTIONAL BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>T</sub>	-1.0 to 7.0	V
Short Circuit Output Current	I <sub>OS</sub>	50	mA
Power Dissipation	P <sub>D</sub> *	1	W
Operating Temperature	T <sub>opr</sub>	0 to 70	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C

\*: Ta = 25°C

## Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	—	6.5	V
Input Low Voltage	V <sub>IL</sub>	-1.0	—	0.8	V

## Capacitance

(V<sub>CC</sub> = 5V ± 10%, Ta = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9, D <sub>IN</sub> )	C <sub>IN1</sub>	—	6	pF
Input Capacitance (RAS, CAS, WE)	C <sub>IN2</sub>	—	7	pF
Output Capacitance (D <sub>OUT</sub> )	C <sub>OUT</sub>	—	7	pF

DC Characteristics

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Condition	MSM 511001B-60		MSM 511001B-70		MSM 511001B-80		MSM 511001B-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
			Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -5.0mA	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4		
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I <sub>LI</sub>	0V ≤ V <sub>I</sub> ≤ 6.5V; All other pins not under test = 0V	-10	10	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I <sub>LO</sub>	D <sub>OUT</sub> disable 0V ≤ V <sub>O</sub> ≤ 5.5V	-10	10	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I <sub>CC1</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling t <sub>RC</sub> = min.	—	90	—	80	—	70	—	60	mA	1, 2
Power Supply Current (Standby)	I <sub>CC2</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$ , $\overline{\text{CAS}} \geq V_{CC} - 0.2V$	—	1	—	1	—	1	—	1	mA	1
Average Power Supply Current (RAS-only Refresh)	I <sub>CC3</sub>	$\overline{\text{RAS}}$ cycling $\overline{\text{CAS}} = V_{IH}$ t <sub>RC</sub> = min.	—	90	—	80	—	70	—	60	mA	1, 2
Average Power Supply Current ( $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	I <sub>CC6</sub>	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	—	90	—	80	—	70	—	60	mA	1
Average Power Supply Current (Nibble Mode)	I <sub>CC8</sub>	$\overline{\text{RAS}} = V_{IL}$ $\overline{\text{CAS}}$ cycling, t <sub>PC</sub> = min.	—	70	—	70	—	50	—	40	mA	1

- Notes : 1. Specified values are obtained with the output open.  
 2. Address can be changed less than three times while  $\overline{\text{RAS}} = V_{IL}$ .

## AC Characteristics (1/2)

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 511001B-60		MSM 511001B-70		MSM 511001B-80		MSM 511001B-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Refresh Period	t <sub>REF</sub>	—	8	—	8	—	8	—	8	ms	
Random Read or Write Cycle Time	t <sub>RC</sub>	120	—	130	—	150	—	190	—	ns	
Read Modify Write Cycle Time	t <sub>RMW</sub>	140	—	155	—	175	—	220	—	ns	
Nibble Mode Cycle Time	t <sub>NC</sub>	40	—	45	—	50	—	55	—	ns	
Nibble Mode Read Modify Write Cycle Time	t <sub>NRMW</sub>	60	—	70	—	75	—	85	—	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	60	—	70	—	80	—	100	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	15	—	20	—	20	—	25	ns	4, 5
Access Time from Column Address	t <sub>AA</sub>	—	30	—	35	—	40	—	50	ns	4, 6
Nibble Mode Access Time	t <sub>NCAC</sub>	—	15	—	20	—	20	—	25	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	—	0	—	0	—	0	—	ns	
Output Buffer Turn-off Delay	t <sub>OFF</sub>	0	20	0	20	0	20	0	20	ns	
Transition Time	t <sub>T</sub>	3	50	3	50	3	50	3	50	ns	3
$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	50	—	50	—	60	—	80	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	15	—	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ Pulse width	t <sub>CAS</sub>	15	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	60	—	70	—	80	—	100	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	20	45	20	50	20	60	25	75	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	15	30	15	35	15	40	20	50	ns	6
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge Time	t <sub>CRP</sub>	5	—	5	—	5	—	5	—	ns	
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	10	—	10	—	10	—	15	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t <sub>CAH</sub>	15	—	15	—	15	—	20	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t <sub>AR</sub>	50	—	55	—	60	—	75	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	30	—	35	—	40	—	50	—	ns	
Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	0	—	0	—	ns	

AC Characteristics (2/2)

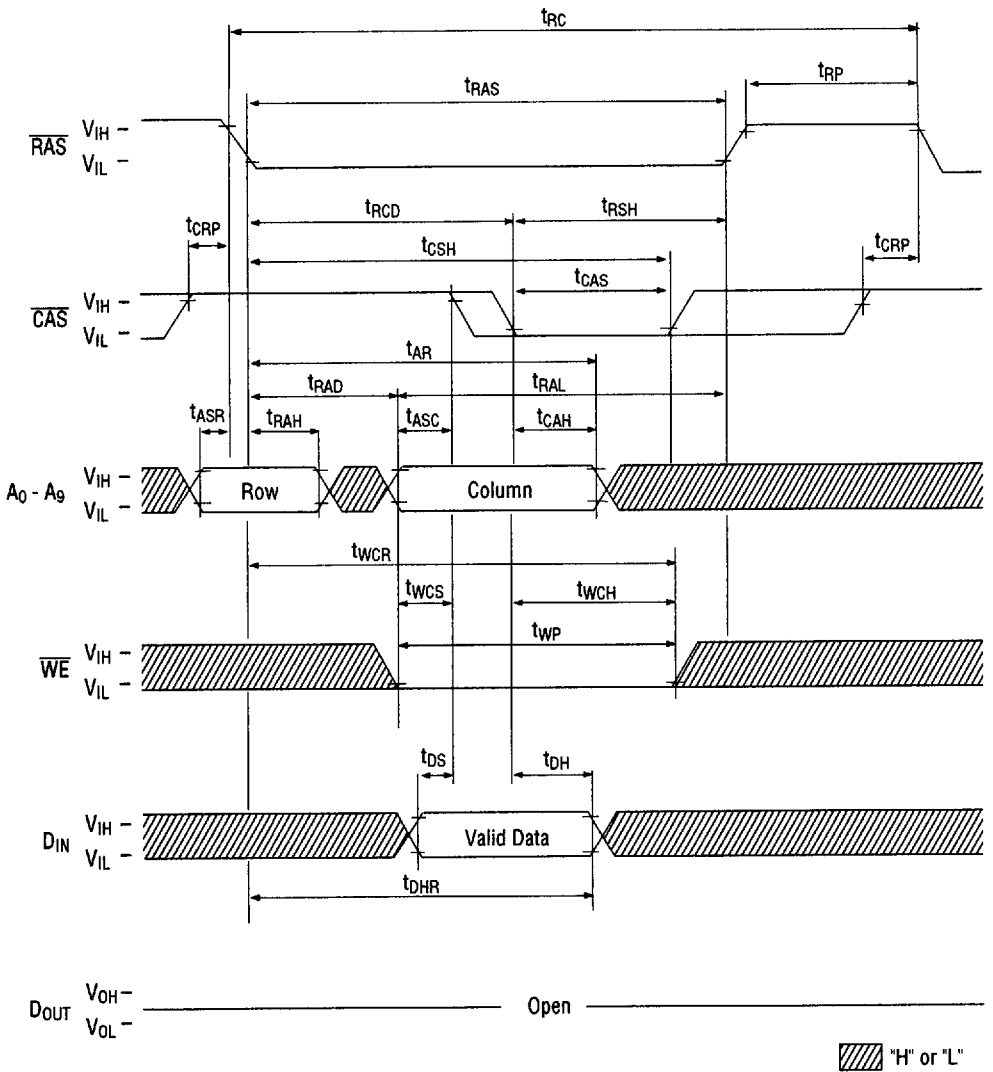
(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 511001B-60		MSM 511001B-70		MSM 511001B-80		MSM 511001B-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	0	—	0	—	ns	8
Write Command Hold Time from $\overline{\text{RAS}}$	t <sub>WCR</sub>	50	—	55	—	60	—	75	—	ns	
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	0	—	0	—	ns	7
Write Command Hold Time	t <sub>WCH</sub>	10	—	15	—	15	—	20	—	ns	
Write Command Pulse width	t <sub>WP</sub>	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	15	—	20	—	20	—	25	—	ns	
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	0	—	0	—	ns	9
Data-in Hold Time	t <sub>DH</sub>	15	—	15	—	15	—	20	—	ns	9
Data-in Hold Time from $\overline{\text{RAS}}$	t <sub>DHR</sub>	50	—	55	—	60	—	75	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	t <sub>CWD</sub>	15	—	20	—	20	—	25	—	ns	7
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay	t <sub>RWD</sub>	60	—	70	—	80	—	100	—	ns	7
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	30	—	35	—	40	—	50	—	ns	7
Read Command Hold Time Reference to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	0	—	0	—	ns	8
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ )	t <sub>CSR</sub>	10	—	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ )	t <sub>CHR</sub>	30	—	30	—	30	—	30	—	ns	
$\overline{\text{CAS}}$ Active Delay from $\overline{\text{RAS}}$ precharge	t <sub>RPC</sub>	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)	t <sub>CPT</sub>	40	—	40	—	40	—	50	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t <sub>CPN</sub>	10	—	10	—	10	—	15	—	ns	
Nibble Mode Pulse Width	t <sub>NCAS</sub>	15	—	20	—	20	—	25	—	ns	
Nibble Mode $\overline{\text{CAS}}$ Precharge Time	t <sub>NCP</sub>	10	—	10	—	10	—	20	—	ns	
Nibble Mode $\overline{\text{RAS}}$ Hold Time	t <sub>NRSH</sub>	15	—	20	—	20	—	25	—	ns	
Nibble Mode $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	t <sub>NCWD</sub>	20	—	20	—	20	—	25	—	ns	
Nibble Mode Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>NRWL</sub>	15	—	20	—	20	—	25	—	ns	
Nibble Mode Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>NCWL</sub>	15	—	20	—	20	—	25	—	ns	

- Notes:
1. An initial pause of 100 $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles (Example:  $\overline{\text{RAS}}$ -only refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 5\text{ns}$ .
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels of input signals for timing measurement. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. Measured with a load circuit equivalent to 2TTL + 100pF.
  5. Operation within the  $t_{\text{RCD}}$  (Max.) limit insures that  $t_{\text{RAC}}$  (Max.) can be met.  $t_{\text{RCD}}$  (Max.) is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}$  (Max.) limit, access time is controlled exclusively by  $t_{\text{CAC}}$ .
  6. Operation within the  $t_{\text{RAD}}$  (Max.) limit insures that  $t_{\text{RAD}}$  (Max.) can be met.  $t_{\text{RAD}}$  (Max.) is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}$  (Max.) limit, access time is controlled exclusively by  $t_{\text{AA}}$ .
  7.  $t_{\text{WCS}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{RWD}}$  and  $t_{\text{AWD}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}}$  (Min.) the cycle is an Early Write and the data out pin remains open circuit (high impedance) throughout the entire cycle; if  $t_{\text{CWD}} \geq t_{\text{CWD}}$  (Min.),  $t_{\text{RWD}} \geq t_{\text{RWD}}$  (Min.) and  $t_{\text{AWD}} \geq t_{\text{AWD}}$  (Min.), the cycle is a read modify write and the data out contains data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
  8. Either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  must be satisfied for a read cycle.
  9. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in an early write cycle and to  $\overline{\text{WE}}$  leading edge in a read modify write cycle.

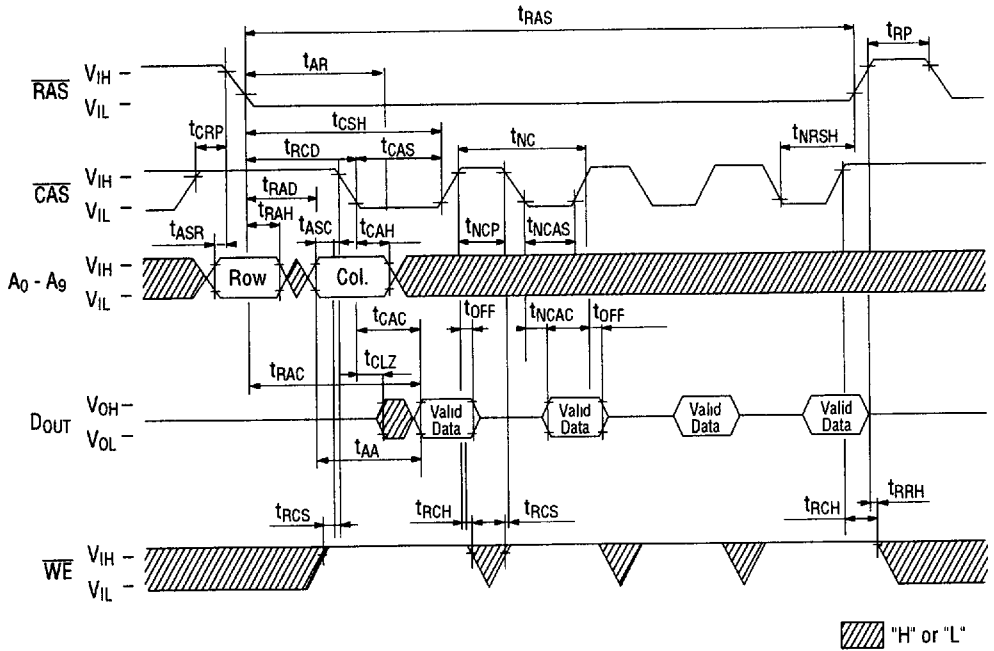


Write Cycle (Early Write)

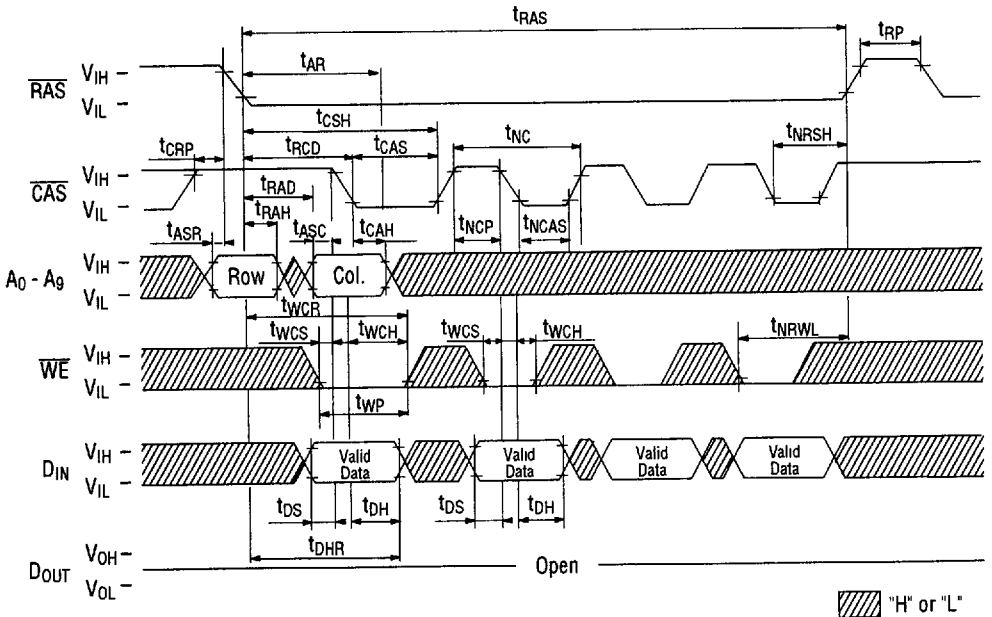




Nibble Mode Read Cycle

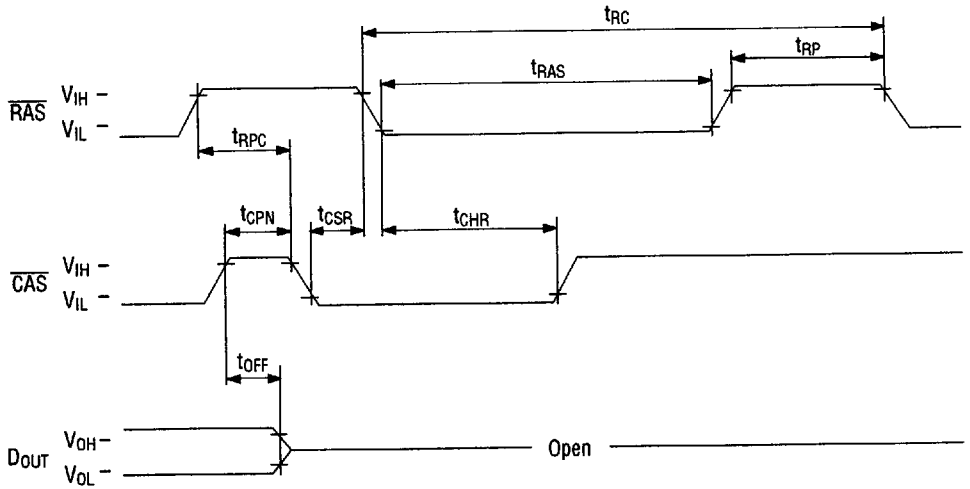


Nibble Mode Write Cycle (Early Write)



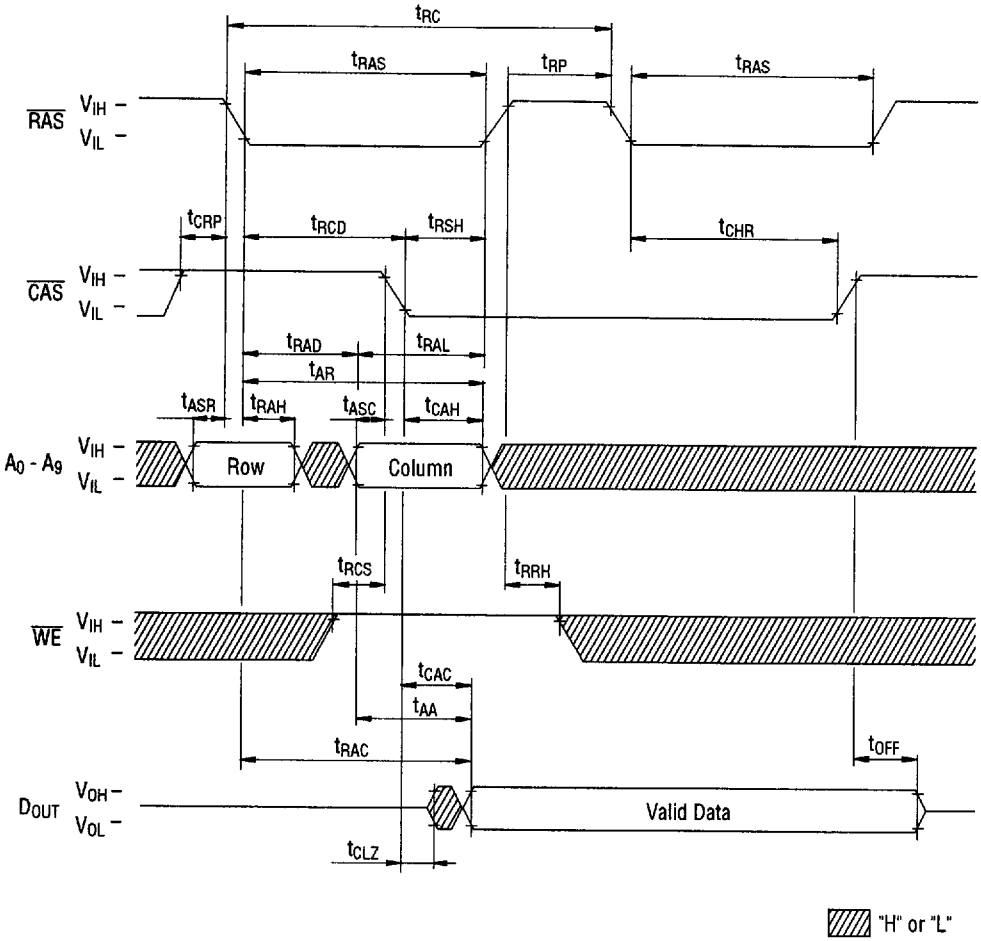


**$\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Auto-refresh Cycle**

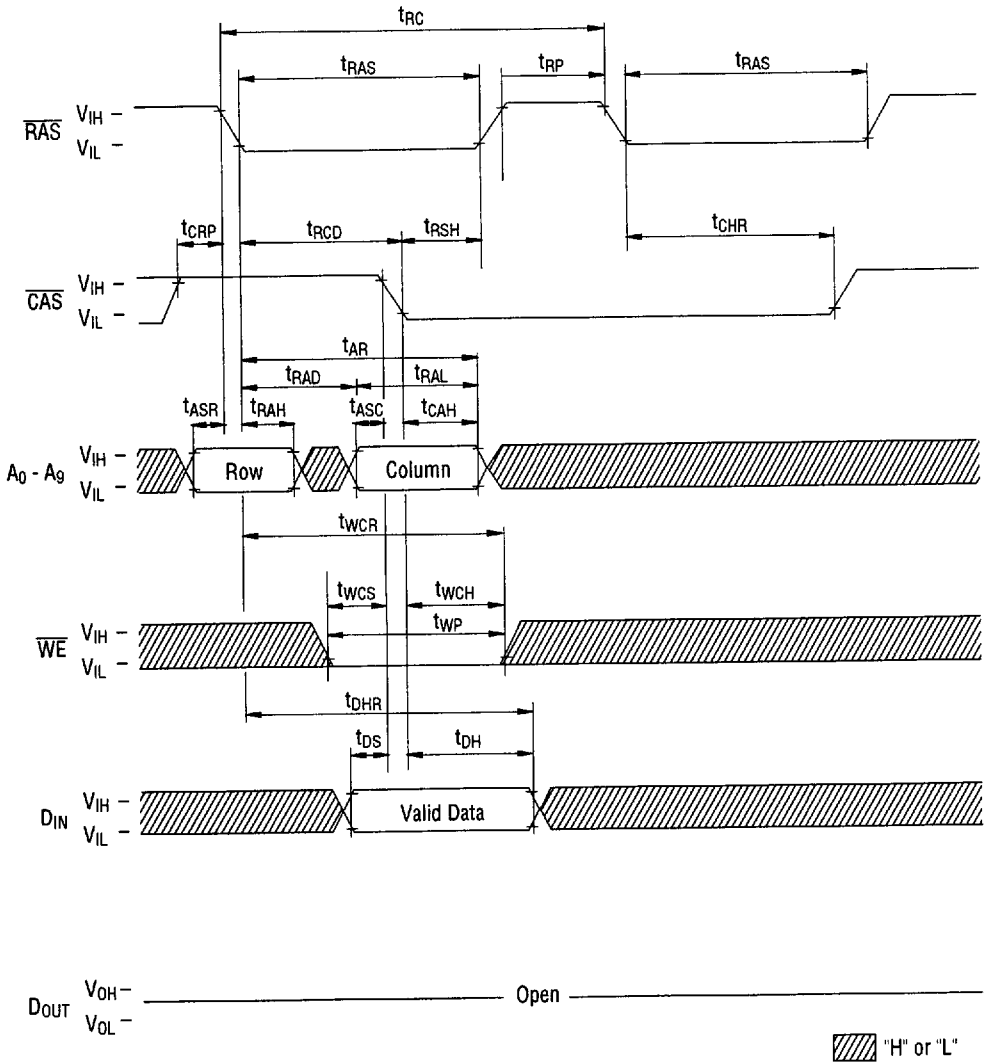


**Note:**  $\overline{\text{WE}}$  = "H" or "L".  $A_0 - A_9$  = "H" or "L"

Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



CAS Before RAS Refresh Counter Test Cycle

