1.1 Scope.

This specification covers the detail requirements for a hybrid, high speed, 16-bit sampling analog-to-digital converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	5962–9171201HX(X)

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-48A.

(X)	Package	Description
A	DH-48A	Tinned Lead Finish
C	DH-48A	Gold Lead Finish

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

$+V_S$ to SGND	+18 V
$-V_S$ to SGND	−18 V
V_{DD} to PGND	+7 V
V_{EE} to PGND	−7 V
Power Dissipation	4.125 W
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	+300°C
Electrostatic Discharge Sensitivity	Class 1
Constant Acceleration	10000 G
Junction Temperature	+175°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 12°C/W
θ_{JA} = 38°C/W

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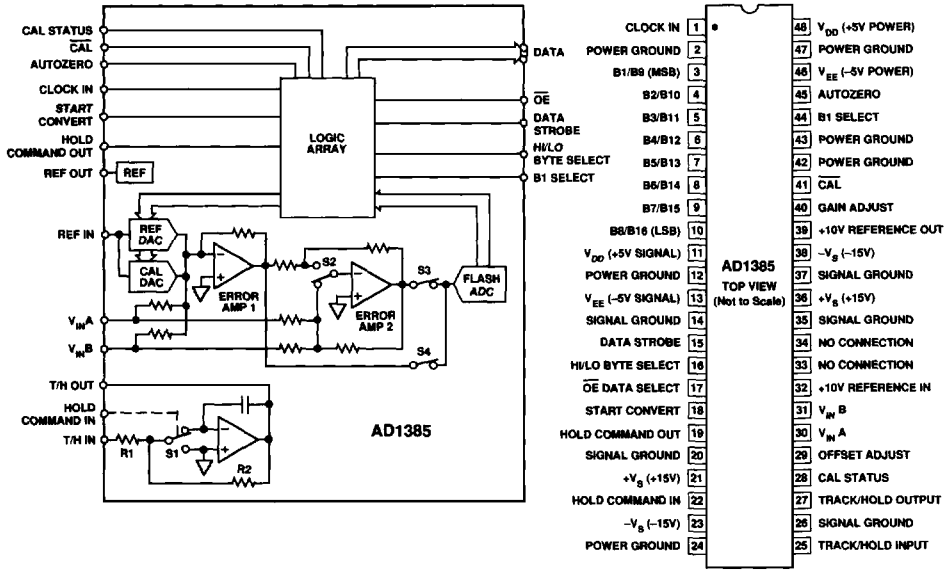
Table 1.

Test	Symbol	Device	Limits Min	Limits Max	Group A Subgroups	Conditions[1] ($-55°C \le T_C \le +125°C$ unless otherwise noted)	Unit
Analog Input Impedance	AIZ	−1	2.45	2.55	7		kΩ
Differential Nonlinearity	DNL	−1	−1.0	+1.0	4, 5, 6	See Note 2	LSB
Gain Error	GE	−1	−0.15	+0.15	1	±5 V dc and ±10 V dc Ranges	% FSR
Gain Drift	ΔGE/ΔT	−1	−15	+15	2, 3	±5 V dc and ±10 V dc Ranges	ppm/°C
Bipolar Zero	BPZ	−1	−0.1	+0.1	1	±5 V dc and ±10 V dc Ranges	% FSR
Bipolar Zero Drift	ΔBPZ/ΔT	−1	−15	+15	2, 3	±5 V dc and ±10 V dc Ranges	ppm/°C
Power Supply Rejection Ratio[3]	PSRR	−1	−0.1	+0.1	1, 2, 3	$+V_S$ = +14.25 V to +15.75 V $-V_S$ = −14.25 V to −15.75 V V_{DD} = +4.75 V to +5.25 V V_{EE} = −4.75 V to −5.25 V	% FSR/V
Signal to Noise Ratio	SNR1	−1	90		4, 5, 6	f = 5.371 kHz, ±5 V FSR, V_{IN} = −0.4 dB	dB
Signal to Noise Ratio	SNR2	−1	90		4, 5, 6	f = 98.389 kHz, ±5 V FSR, V_{IN} = −0.4 dB	dB
Signal to Noise Ratio	SNR3	−1	88		4, 5, 6	f = 197.510 kHz, ±5 V FSR, V_{IN} = −0.4 dB	dB
Peak Distortion	PHD1	−1		−90	4, 5, 6	f = 5.371 kHz, ±5 V FSR, V_{IN} = −0.4 dB	dB
Peak Distortion	PHD2	−1		−88	4, 5, 6	f = 98.389 kHz, ±5 V FSR, V_{IN} = −0.4 dB	dB
Peak Distortion	PHD3	−1		−82	4, 5, 6	f = 197.510 kHz, ±5 V FSR, V_{IN} = −0.4 dB	dB
Total Harmonic Distortion	THD1	−1		−90	4, 5, 6	f = 5.371 kHz, ±5 V FSR, V_{IN} = −0.4 dB	dB
Total Harmonic Distortion	THD2	−1		−88	4, 5, 6	f = 98.389 kHz, ±5 V FSR, V_{IN} = −0.4 dB	dB
Total Harmonic Distortion	THD3	−1		−82	4, 5, 6	f = 197.510 kHz, ±5 V FSR, V_{IN} = −0.4 dB	dB
Signal-to-Noise Ratio	SNR4	−1	90		4, 5, 6	f = 5.371 kHz, ±10 V FSR, V_{IN} = −0.4 dB	dB
Signal-to-Noise Ratio	SNR5	−1	90		4, 5, 6	f = 98.389 kHz, ±10 V FSR, V_{IN} = −0.4 dB	dB
Signal-to-Noise Ratio	SNR6	−1	88		4, 5, 6	f = 197.510 kHz, ±10 V FSR, V_{IN} = −0.4 dB	dB
Peak Distortion	PHD4	−1		−90	4, 5, 6	f = 5.371 kHz, ±10 V FSR, V_{IN} = −0.4 dB	dB
Peak Distortion	PHD5	−1		−80	4, 5, 6	f = 98.389 kHz, ±10 V FSR, V_{IN} = −0.4 dB	dB
Peak Distortion	PHD6	−1		−74	4, 5, 6	f = 197.510 kHz, ±10 V FSR, V_{IN} = −0.4 dB	dB

Test	Symbol	Device	Limits Min	Limits Max	Group A Subgroups	Conditions[1] ($-55°C \le T_C \le +125°C$ unless otherwise noted)	Unit
Total Harmonic Distortion	THD4	−1		−90	4, 5, 6	f = 5.371 kHz, ±10 V FSR, V_{IN} = −0.4 dB	dB
Total Harmonic Distortion	THD5	−1		−80	4, 5, 6	f = 98.389 kHz, ±10 V FSR, V_{IN} = −0.4 dB	dB
Total Harmonic Distortion	THD6	−1		−74	4, 5, 6	f = 197.510 kHz, ±10 V FSR, V_{IN} = −0.4 dB	dB
Digital Input Voltage Logic 1 Logic 0	 V_{IH} V_{IL}	−1	2.25	 0.8	7, 8	Note 3	V
Digital Input Current	I_{IL}	−1	−200	+200	7, 8	V_{IN} = 0 V[3]	μA
	I_{IH}	−1	−200	+200	7, 8	V_{IN} = 5 V[3]	μA
Digital Output Voltage Logic 1 Logic 0	 V_{OH} V_{OL}	−1	2.4	 0.4	7, 8	I_{OH} = −3.2 mA[3] I_{OL} = +3.2 mA[3]	V
Internal Reference Voltage	V_{REF}	−1	9.990	10.010	1	I_L = 2 mA R_L = 5 kΩ Pin 32 Connected to Pin 39	V
	ΔV_{REF}	−1	−15	+15	2, 3		ppm/°C
Supply Currents	$+I_{IS}$ $-I_{IS}$ I_{DD} I_{EE}	−1		80 75 160 200	1, 2, 3	Note 3	mA
Power Dissipation	P_D	−1		4.125		Note 3	W

NOTES
[1]Unless otherwise specified, all tests are performed using a 50 percent duty cycle, 10 MHz clock, ±15 V dc and ±5 V dc power supply voltages, and a 500 kHz conversion rate.
[2]No missing codes; DNL is derived from a histogram test using a full scale sinewave input.
[3]Subgroups 2, 3 and 8 shall be tested for initial device characterization and after design and major changes that affect these parameters. Subgroup 8 shall be guaranteed to the limits specified in Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I)

4.2.1 Burn-In Circuit.

Burn-in is per MIL-STD-883 Method 1015 test condition (B).