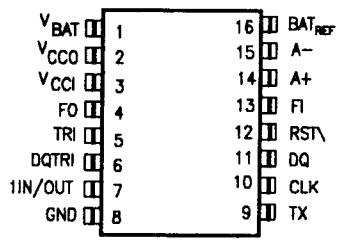
DALLAS SEMICONDUCTOR

DS1209S-B1
Wireless to 3-Wire Converter Chip

FEATURES
- Adapts a wireless device to a 3-wire serial port (DQ, CLK, and RST\ signals)
- Up to 65,536 devices can be uniquely addressed within the same wireless proximity
- Receives IR, RF, or magnetic pulses as small as 25 millivolts peak-to-peak and frequencies up to 250 KHz
- Low-power operation for both battery backup and battery operate modes
- Makes allowances for extra or missing pulses induced by noise in transmission path
- Counts input pulse packets to interpret data and commands
- Internal state machine generates commands and routes data to and from the 3-wire serial port
- Output pin can gate a variety of transmitting devices
- Simplex 1-wire port can override comparator inputs for input/output to 3-wire serial port
- 3-wire serial port connects to large family of products: DS1201 Electronic Tag, DS1204U Electronic Key, DS5000 Soft Microcontroller, DS1280 3-Wire to Bytewide Converter Chip

PIN CONNECTIONS



16-PIN SOIC
(300 MIL)

See Mechanical Drawing
Section 16, pg. 6

PIN NAMES (\ Denotes Condition Low)

BAT_{REF}	Battery Reference
V_{BAT}	Battery Input
V_{CCO}	Switched Output
V_{CCI}	+5V Input
1IN/OUT	1-Wire Input/Output Port
GND	Ground
TRI	Tri-state DQ, CLK, RST\ Input
DQ TRI	Tri-state Only DQ Input
TX	Wireless Transmit
RST\	RESET (3-Wire Port)
CLK	Clock (3-Wire Port)
DQ	Data Input/ Output (3-Wire Port)
FI/FO	Freshness Seal Input/Output
A+	Non-Inverting Comparator Input
A-	Inverting Comparator Input

DESCRIPTION
The DS1209S-B1 Wireless to 3-Wire Converter Chip is a low-power CMOS device designed to implement an addressable, full-duplex wireless to 3-wire communications channel. An internal state machine interprets pulse packets which are received at the comparator input pins and routes data to and from the 3-wire serial port. The TX output pin provides a return transmission link for data received from the 3-wire serial port and can gate a variety of transmitting devices. The low-power input comparator, internal to the DS1209S-B1, is designed to listen for signals with amplitudes as small as 25 millivolts peak-to-peak and frequencies of up to 250 KHz. The DS1209S-B1 also contains a 16-bit chip select value which is stored in the internal command prefix register. This chip select value allows up to 65,536 devices to be uniquely addressed within the same wireless proximity. The 1-wire input/output pin can be used to override the comparator inputs and allow a device to communicate with the DS1209S-B1 in a simplex manner at one-half the frequency of the comparator inputs. Additionally, a sophisticated power switching circuit is provided which allows for both battery backup and battery operate modes.

PIN DESCRIPTIONS

V_{BAT} - This input is designed to be connected to a battery with a voltage range between 2.5 and 4.0 volts. When V_{CCI} is grounded, the DS1209S-B1 acts as a battery-operated device and power is supplied from the V_{BAT} pin at all times. This input should NEVER be grounded. If single supply operation is selected, this pin MUST be the power input for the device.

V_{CCI} - This input is designed to be connected to a power supply with a voltage range of 4.5 to 5.5 volts. This voltage input is switched to the V_{CCO} pin as long as V_{CCI} is greater than V_{BAT}. However, when V_{BAT} is the greater, its voltage will be output. When both V_{CCI} and V_{BAT} inputs are used, the DS1209S-B1 is in the battery backup mode. V_{CCI} should be grounded when not being used.

V_{CCO} - Switched V_{BAT} or V_{CCI} output. V_{CCO} will always be the greater of V_{BAT} or V_{CCI}.

BAT_{REF} - This output pin represents the battery voltage input (V_{BAT}) less 0.6 volts. It is designed to be connected to the battery input pin on the attached 3-wire device.

1IN/OUT - This input/output pin provides an override for the comparator inputs and allows a device to communicate with the DS1209S-B1 in a simplex manner at one-half the frequency of the comparator inputs. The pin acts as an input pin for pulse packets containing both command and data input to the 3-wire serial port. Data is also output on the same pin when memory content is read via the 3-wire serial port.

FI/FO - The FI (Freshness In) and FO (Freshness Out) pins combine to give the DS1209S-B1 a method of conserving battery power until placed in service and determine if the low power consumption mode has been entered. The FI pin is used to start (break freshness seal) or stop (enable freshness seal) the continuous power consumption of the comparator on the DS1209S-B1 that is connected to the comparator input pins A+ and A- (Figure 6).

A+,A- - These are the inputs for the low-power comparator.

TRI - This input is used to tri-state the 3-wire outputs CLK, RST\, and DQ. The TRI pin is active in a high state.

DQ TRI - This input is used to tri-state the 3-wire DQ pin only. The DQ TRI pin is active in a high state.

TX - This output pin contains the data which is output from the 3-wire serial port. In a typical application this pin is used to key the wireless transmitter which will send data back to a wireless receiver.

RST - This output signal is the reset signal for the 3-wire serial port. When RST\ is at high level, the 3-wire port is active and data can be written into or read from the port.

CLK - This output signal is the clock signal for the 3-wire serial port. The clock signal synchronizes data into and out of the DQ line of the 3-wire serial port.

DQ - This input/output is the data input/output for the 3-wire serial port. In a typical application, RST\, CLK, and DQ connect directly to the RST\, CLK, and DQ pins on the DS1204 Electronic Key, DS1201 Electronic Tag, DS1207 TimeKey, or DS1280 3-Wire to Bytewide Converter Chip.

GND - This pin is the ground.

OPERATION

The principle blocks of circuitry contained within the DS1209B-S1 are shown in Figure 1. During normal input conditions, pulse packets present at the comparator input pins pass through the input selector to the pulse counter. The 1-wire port is selected for data input by exception when data is present at the 1-wire port. This data will override the comparator inputs. The 1-wire port pin will be discussed in more detail later in this text. Input pulses arriving at the pulse counter are deciphered into various command codes which affect the command prefix shift register, the state machine, and ultimately the 3-wire serial port. The various command codes are listed in Table 1.

Pulse packets are input to the pulse counter with a 50 *us* dead time after the last pulse in each packet. The DS1209S-B1 uses the dead time to determine how many pulses were sent and the action to be taken. In addition, if input to the pulse counter is low (inactive) for longer than 1.5 mS, the DS1209S-B1 will time out, reset the command prefix shift register, and place the state machine into an inactive state.

As can be seen in the block diagram of Figure 1 and the command codes listed in Table 1, the input pulses are sent in two different directions. If a pulse packet of 100 pulses (greater than 90) arrives at the pulse counter, the next 24 pulse packets are sent to the command prefix shift register and the state machine is set inactive. The 100-pulse packet always sets the state machine to inactive regardless of any action which may have been occurring (aborts current action/conversation).

The 24 pulse packets which go to the command prefix shift register will cause a normal wake-up or mask wake-up, a read of the chip select bits, a write of the chip select bits, or a lock of the chip select bits. The chip select bits make up the first 16 bits of the 24-bit command prefix shift register. The last eight bits comprise the function field. See Figure 2 and Table 2.

NORMAL WAKE-UP AND MASK WAKE-UP

Wake-up refers to the sequence of 24 20- or 40-pulse packets received after a 100-pulse packet is sent to set the DS1209S-B1. The 24 pulse packets contain a 16-bit chip select and 8-bit function code which will cause the device state machine to become active. A normal wake-up requires all 16 chip select bits to be matched to those stored on the device before the device becomes active. A masked wake-up requires only a partial match, starting with the least significant bit pair (bit 0,1) and proceeding to the most significant bit pair left unmasked. For example, if the wake-up command (see Table 2) having function code 00011101 -- "mask CS bits 10-15" -- is issued to the DS1209S-B1, then chip select bits 0 through 9 must be correctly matched before the device will become active. The following step-by-step procedure will illustrate normal and mask wake-up:

1. First, a 100-pulse packet is sent to the comparator input pins, which puts the state machine into an inactive state.

2. Issue wake-up or mask wake-up by sending the 8-bit function code followed by the 16 chip select bits to enable the state machine. The command prefix register is always loaded by sending write zeros (20-pulse packets) or write ones (40-pulse packets). The loaded pulse packets are compared to values stored in the 8-bit Function Code Table and the previously stored 16 chip select bits (storing the chip select values will be covered later).

Pulse packets of 50 to 89 pulses are ignored when loading the command prefix shift register. A pulse packet of greater than 90 pulses always initializes the command prefix shift register back to starting with the LSB and aborts any previous transaction. The state machine is also set inactive. After the first 24 bits are received and a valid wake-up is decoded, the command prefix shift register will no longer allow data bits to be written into it and the enable output will become active and remain active until another 100-pulse packet is received to reinitialize. Subsequent pulse packets which are received will be directed to the state machine with action taken corresponding to the number of pulses received as shown in Table 1.

A pulse packet of 80 pulses, followed by a 20-pulse packet, followed by a 40-pulse packet, enables the beacon mode of the state machine. Beacon mode turns on and off the TX pin at a 5 KHz rate for 1.2 seconds. In a typical application utilizing the DS6065A, this signal can be used to key a transmitter (the DS6065A operates at 303.875 MHz), which allows a base unit to lock onto the transmitted beacon.

3. The DS1209S-B1 is now placed in the active state by issuing a 60-pulse packet which takes RST\ high on the 3-wire serial port. This same 60-pulse packet also turns off the beacon if it has not already timed out. With RST\ high, a conversation can now take place between devices placed on the 3-wire port (DS1201, DS1204U, DS1207, or DS1280) from the comparator inputs, and data is returned to the sending unit via the TX pin. As pulse packets continue to be received, the device attached to the 3-wire port will be written and read using 20- and 40-pulse packets and reset with a 60-pulse packet. The reset pulse packet will take RST\ low until the next pulse packet is detected after the 50 us dead time. When data is read from the 3-wire port, it is always sent to the TX pin for transmission back to the sending unit.

4. If an 80-pulse packet is received, the state machine will go to an inactive state but still remains alert for new pulse packets.

5. If no pulse packets are received for more than 1.5 mS, the DS1209S-B1 will time out, initialize the command prefix shift register, and set the state machine back to the inactive state. The DS1209S-B1 now waits for new inputs to the protocol serial shift register which begin with a 100-pulse packet.

READING THE CHIP SELECT BITS

The 16-bit chip select (CS) value stored in the command prefix shift register can be determined in several ways. In fact, an exhaustive search could be implemented with a trial and error method which would eventually eliminate all but the correct bit pattern. Obviously, this method is painfully slow as 2^{16} possible combinations may need to be tried. In a similar but much more expedient manner, mask bits can be used in a successive approximation manner to determine the value of the CS bits. This procedure is accomplished by gradually increasing the size of the unmasked chip select fields as each set of bits is identified. However, the simplest method of determining the 16-bit CS value is to read the 16-bit value directly. The following step-by-step procedure will illustrate how to read the chip select bits.

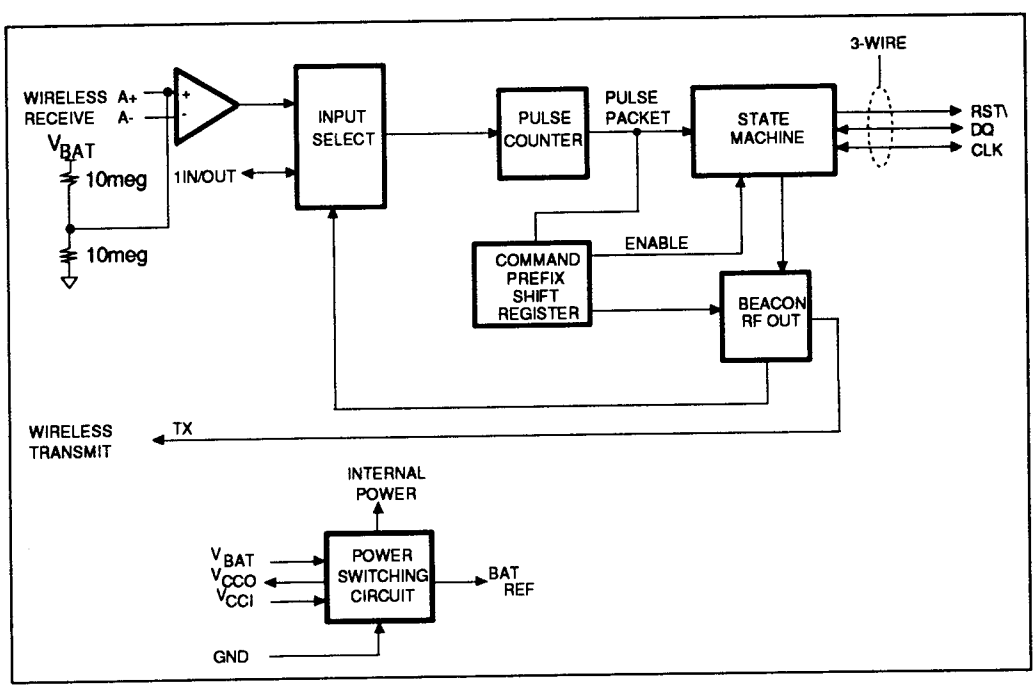
1. Wake up the DS1209S-B1 by using the mask all function code. This is accomplished by sending a 100-pulse packet followed by 24 20-pulse and 40-pulse packets. The first eight pulse packets must match the mask all function code. The last 16 pulse packets can be any combination of 20- and 40-pulse packets as the 16 CS bits are masked. Next, the beacon mode of the state machine is enabled by sending an 80-pulse packet followed by a 20- and then a 40-pulse packet. If the beacon mode has been enabled, it should be disabled after receiver lock-on by sending a 60-pulse packet to the comparator inputs.

B1 COMMAND CODES Table 1

Number of Pulses			Command
Min.	Typ.	Max.	
5	20	29	Write 0 or READ
30	40	49	Write 1
50	60	69	Take RST\ High
70	80	89	Return to Inactive State
90	100	109	Initialize Protocol and Put State Machine Inactive

NOTE: Pulse packets are sent with a minimum of 50 µs quiet time after each pulse packet and a maximum quiet time of approximately 1.5 ms.

DS1209S-B1 BLOCK DIAGRAM Figure 1



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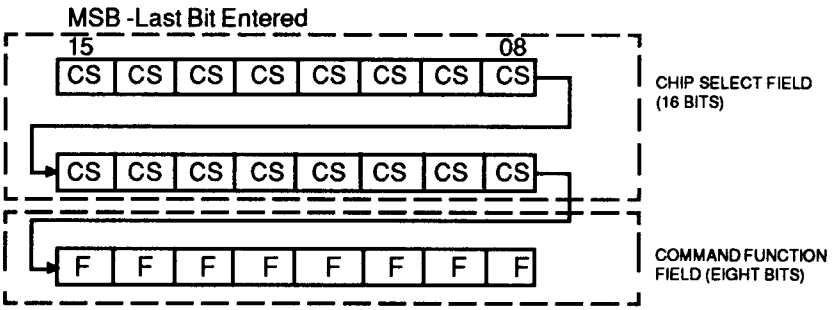
24-BIT COMMAND PREFIX SHIFT REGISTER BIT PATTERN Figure 2



B1 FUNCTION CODES Table 2

FUNCTION	MSB			FUNCTION CODE				LSB	RESULTS
Wakeup	0	0	0	1	1	0	0	0	Mask All Bits
Wakeup	0	0	0	1	0	0	0	1	Mask CS Bits 2-15
Wakeup	0	0	0	1	0	0	1	0	Mask CS Bits 4-15
Wakeup	0	0	0	1	1	0	1	1	Mask CS Bits 6-15
Wakeup	0	0	0	1	0	1	0	0	Mask CS Bits 8-15
Wakeup	0	0	0	1	1	1	0	1	Mask CS Bits 10-15
Wakeup	0	0	0	1	1	1	1	0	Mask CS Bits 12-15
Wakeup	0	0	0	1	0	1	1	1	Mask CS Bits 14-15
Wakeup	0	0	1	0	1	0	0	0	Use all CS Bits
Read CS Bits	0	0	1	0	1	0	1	1	Ignore CS Bits
Store CS Bits	0	0	1	0	1	1	0	1	Use all CS Bits
Lock CS Bits	0	0	1	0	1	1	1	0	Use all CS Bits

2. Now load the DS1209S-B1 command prefix shift register with the read CS bits function code. This is accomplished by sending a 100-pulse packet followed by 24 20- or 40-pulse packets. As before, the first eight pulse packets must match the read CS bits function code. However, the last 16 pulse packets can be any combination of 20- and 40-pulse packets, as the 16 CS bits are ignored. During the 24-bit command prefix shift register load, pulse packets of 60 and 80 are ignored. As usual, pulse packets of 100 will initialize the command prefix shift register and set the state machine inactive.

3. If the 8-bit function code in the command prefix shift register is correctly matched, then for each 20-pulse packet (read command) received at the comparator input pins, one bit of the 16-bit CS field will be read at the TX pin, the LSB of the field appearing first. Thus, it will receive 16 packets of 20 pulses each to read the entire CS field. If more than 16 read pulse packets are sent to the comparator input pins in this mode, the DS1209S-B1 will start over again reading the CS bits, beginning with the first bit. Pulse packets of 40, 60, or 80 pulses are ignored and 100-pulse packets will initialize the command prefix shift register and set the state machine inactive. This is a non-destructive read and can be aborted at any time during the read process.

4. During the entire CS bit read operation, the state machine is disabled. All pulse packets except the 20- and 100-pulse packet are ignored by the state machine. As usual, the 100-pulse packet or a timeout of 1.5 mS will initialize the command prefix shift register and return the state machine to inactive.

STORING THE CHIP SELECT BITS

In order to store a new value into the chip select bits of the protocol shift register, it is necessary to know the existing stored value. In addition, if the lock bit is set, a new value for the chip select bits cannot be stored unless power is removed and reapplied. The lock function is only useful in applications where power is permanently applied or removed by exception. The existing value of the CS bits should be obtained using the procedure described in the "Reading Chip Select Bits" section. After obtaining the existing chip select values, a new value can be entered by using the step-by-step procedure which follows:

1. Load the proper 24-bit pattern into the command prefix shift register for storing the chip select bits. This pattern consists of 24 20-pulse and 40-pulse packets. The first eight packets must match the stored CS bits function code. The last 16 pulse packets must match the existing CS bits. During the 24-bit shift register load, only 20- and 40-pulse packets are accepted while 60- and 80-pulse packets are ignored. As always, 100-pulse packets will initialize the command prefix shift register and set the state machine inactive.

2. If the 8-bit function code and the 16 CS bits are correct, the next 16 pulse packets will store a new CS value, overriding the old CS bits. Only 20-pulse and 40-pulse packets are accepted. Pulse packets of 60 and 80 are ignored and 100-pulse packets cause the stored CS bit command to abort, initializing the command prefix shift register and returning the state machine to inactive. The DS1209S-B1 does not lock up after 16 pulse packets are sent in this mode. If more packets are sent, the new packets will continue to shift in, storing the last 16 packets that are received.

3. During the entire store CS bits operation, the main state machine is disabled. All pulse packets received will have no effect on the state machine except the 100-pulse packet, which will initialize the command prefix shift register and return the state machine to an inactive state. A timeout of 1.5 mS will have the same effect as a 100-pulse packet.

LOCKING THE CHIP SELECT BITS

The design of the DS1209S-B1 allows for both battery backup and battery operation. The device consumes only modest amounts of power. As a result, most applications for this device are permanently powered and memory elements within the device, like the command prefix shift register CS bits, are nonvolatile. A special latch is provided so that upon initial power up (when battery is first connected) the nonvolatile chip select bits can be written with a store CS function code.

The CS bits can be changed as often as desired, using the store function until a lock CS function code is issued. Once sent, the value of the chip select bits cannot be changed until power is removed (battery disconnected) from the DS1209S-B1. The lock CS bit can be accomplished by the following step-by-step procedure.

1. If the CS value is unknown, the procedure for reading the CS bits should be followed so that the value is known.

2. The 8-bit function code for locking the CS bits is transmitted, followed by the 16-bit chip select value. Only 20- and 40-pulse packets are accepted; 60- and 80-pulse packets are ignored. A 100-pulse packet will cause the lock CS bits to abort, initializing the command prefix shift register and returning the state machine to the inactive state.

3. Once the 24-bit command prefix shift register is loaded with an exact match for the CS bits and the lock CS function code, the latch is set automatically and no further action is required.

4. The only way the latch can be reset is to remove power (the battery) from the device. During the lock CS operation the main state machine is disabled so that all pulse

packets have no effect. As usual, a 100-pulse packet or a timeout of 1.5 mS will initialize the command prefix shift register and return the state machine to inactive.

POWER SWITCHING CIRCUIT

As shown in the block diagram of Figure 1, the DS1209S-B1 can receive its power from two different sources: the V_{CCI} input or the V_{BAT} input. The DS1209S-B1 is designed to work off of a battery supply as low as 2.5 volts. However, if an alternate supply is available, it can be connected to the V_{CCI} pin. A voltage level of 3 volts minimum is required on the V_{BAT} pin for proper operation. With both the V_{CCI} pin and the V_{BAT} pin attached to appropriate power sources, the DS1209S-B1 will automatically select the supply input which is the higher level. If only one power source is connected, it **MUST** be connected to the V_{BAT} input. The V_{REF} output is designed specifically to supply power to a connected 3-wire device such as a DS1204U, DS1201, DS1207, or DS1280. The V_{REF} output is equal to the V_{BAT} input less a voltage drop of about 0.5 volts. This pin is capable of sourcing a current of 2 mA.

PULSE PACKETS

The minimum time between pulse packets is 50 *us* and the idle time of 1.5 mS will always cause the protocol shift register to initialize and the state machine to go inactive.

Pulse packets range from 20 pulses to 100 pulses, depending on the action to be taken (see command codes in Table 1). If a read pulse packet is detected, data is to be read from a device connected on the 3-wire serial port and the TX pin will become active high for a logic 1 or remain low for a 0. Time is allotted beyond the 50 *us* between pulse packets for the DS1209S-B1 to send out a 1 or a 0. This time is specified as a 375 *us* window. If a logic 0 is being sent, the TX pin will remain low for the entire window. If a logic 1 is being sent, the TX pin will be driven to high level within a maximum of 75 *us* and will remain high for a minimum of an additional 150 *us*.

However, if a minimum of four pulses is received at the comparator inputs, the TX pin activity is terminated on the assumption that a logic 1 has been received and the sending unit has started the next pulse packet. The timing diagram of Figure 3 illustrates the comparator output and the TX pin timing relationship.

COMPARATOR OPERATION

The low-power comparator inputs are brought out to the user on the A+ and A- pins. The low- power input comparator is designed to listen for signals with amplitudes as small as 25 millivolts peak-to-peak and frequencies of up to 250 KHz.

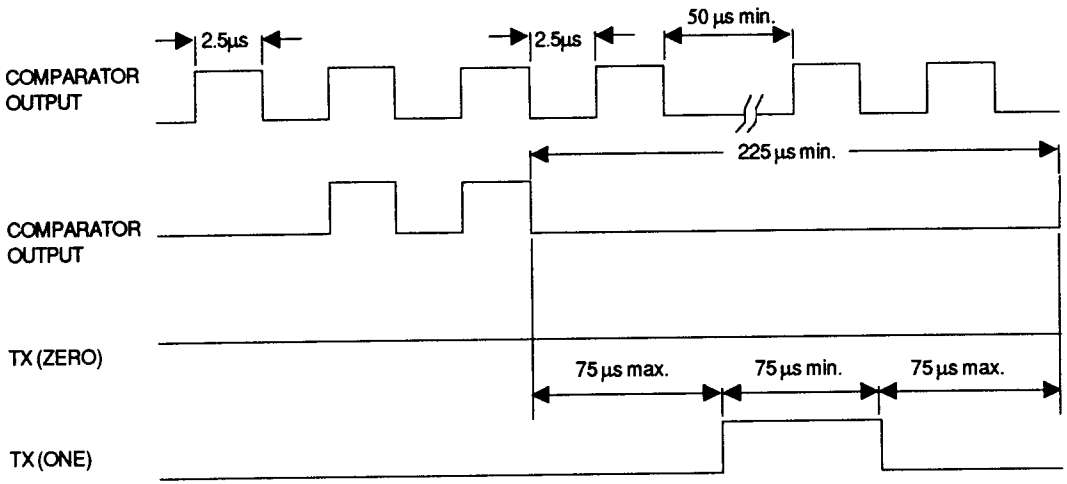
1IN/OUT

This pin is an input/output one-wire signal port designed to override the comparator input pins and multiplex the TX pin on a single connection. Data is input on the port pin using a frequency of one-half the comparator input frequency with a symmetrical high and low time of 5 *us* ± 20%. Therefore, the time between pulse packets is 2X the time allotted between pulse packets when 250 KHz is used. If a read pulse packet is detected, time is allotted beyond the 100 *us* between pulse packets for the DS1209S-B1 to send out a 1 or a 0. This time is specified as a 450 *us* window. If a logic 1 is being sent, the 1IN/OUT pin will remain low for the entire window. If a logic 0 is being sent, the 1IN/OUT pin will be tri-stated to a high impedance state by the DS1209B and should be pulled high using a pullup resistor. This high impedance state will occur within a maximum of 150 *us* and remain for a maximum of 150 *us*. The 1IN/OUT pin is guaranteed to be inactive after a third 150 *us* time period. The timing diagram of Figure 4 illustrates the 1IN/OUT timing.

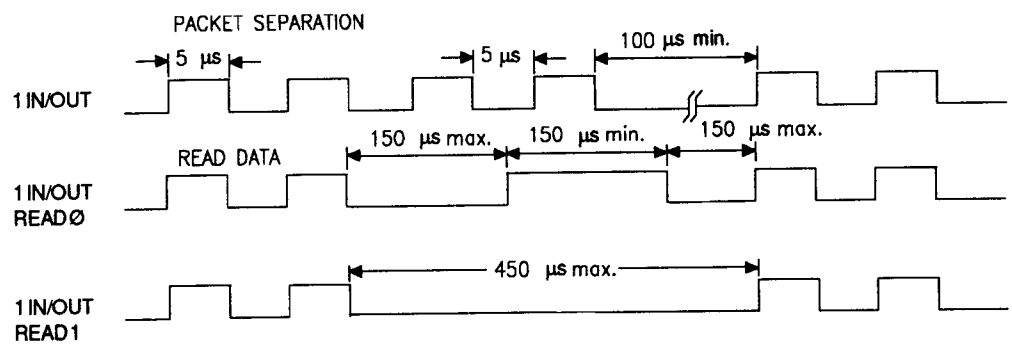
RST\, CLK, AND DQ

The 3-wire serial port on the DS1209S-B1 consists of the RST\, CLK, and DQ signals. These signals are designed to connect directly to the CLK, RST\, and DQ lines of various 3-wire devices, such as the DS1204U, DS1207, DS1201, or DS1280. The RST\ pin on the DS1209S-B1 is driven to a high level whenever a 60-pulse packet is received by the state machine. The RST\ signal remains high until a 80- or 100-pulse packet is received or until 1.5 mS has elapsed without activity at the comparator inputs. The CLK pin on the DS1209S-B1 is normally high until the RST\ signal is high. When RST\ is high and a 20- or 40-pulse packet is received by the state machine (indicating a "read from" or "write to" the 3-wire port), the CLK pin is driven low for a period of 500 ns minimum to 1.0*us* maximum. If data is being read from a device on the 3-wire serial port, it will become valid within 200 ns of the falling edge of the clock returned to the sending unit. The output will be a high level for a logic 1 or remain at low level for a logic 0. If data is being written to a device on the 3-wire serial port, then data will be sent from the state machine to the DQ line prior to the falling edge of the clock. This data will remain valid until the clock transitions back to a high level. The TX pin remains low while data is being written to the 3-wire serial port. A timing diagram for the 3-wire serial port is shown in Figure 5. For more detailed information on the 3-wire serial port, see the data sheets on the DS1201, DS1207, or DS1280.

COMPARATOR INPUT TIMING Figure 3



1IN/OUT TIMING Figure 4



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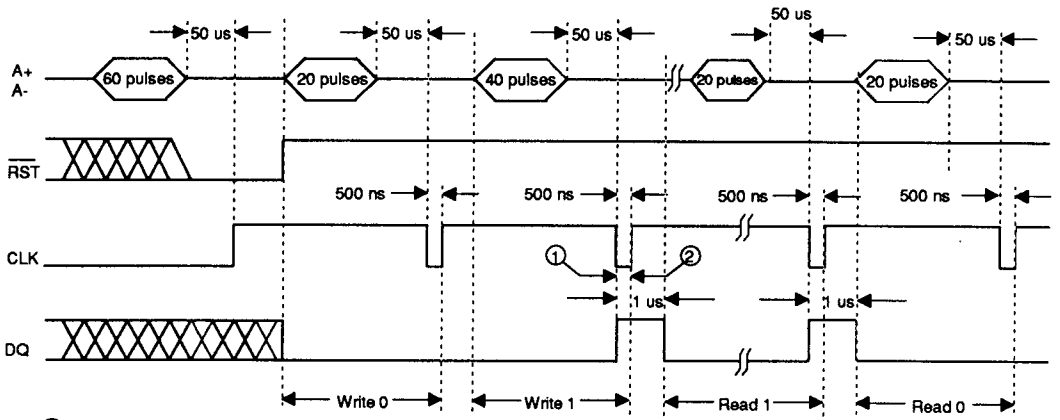
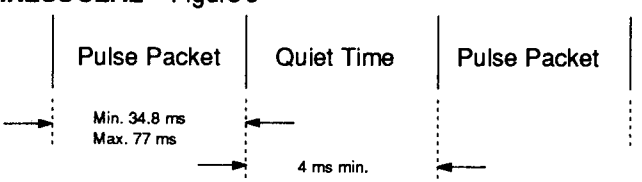
RST\, CLK, AND DQ TIMING Figure 5



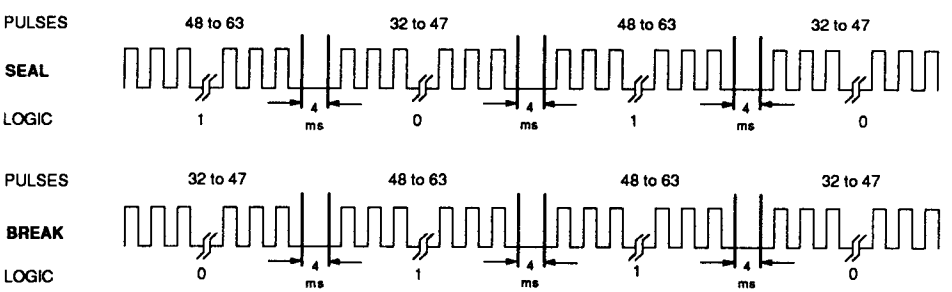
① Data setup time:100 ns min.

② Data hold time: 100 ns max.

FRESHNESS SEAL Figure 6



SEAL AND BREAK COMMAND



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative to Ground	0.5V to +7V
Storage Temperature	-55° to +125°C
Operating Temperature	0° to 70° C
Soldering Temperature	260° for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Input	V_{CCI}	3.0	5.0	5.5	Volts	1,2
Battery input	V_{BAT}	2.5		4.0	Volts	1,2
Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	Volts	1,3
Input Logic 0	V_{IL}	-0.3		0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, V_{BAT} =3 V, 0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Battery Reference	V_{REF}	V_{BAT} -0.7		V_{BAT}	Volts	1
Switched Voltage Out	V_{CCO}	V_{CCI} -0.3			Volts	1,4
Switched Current Out	I_{CCO}	3	4		mA	5
Operating Current	I_{CC}		2	75	uA	6
Standby Current	I_{cc1}			2	uA	7
Output Logic 1	V_{OH}	V_{CC} -10%			Volts	1,3
Output Logic 0	V_{OL}			0.4	Volts	1
Output Current Logic 1	I_{OH}			250	uA	
Output Current Logic 0	I_{OL}			500	uA	
Comparator Leakage Current	I_L	-1.0		1.0	uA	8
Comparator Sensivity	V_{SINE}	25	20		mV	9
Comparator Frequency	C_{FREQ}	40		250	KHz	
Comparator Input Resistance	R_{IMP}	1			M ohm	
Input Capacitance	C_{IO}			5	pF	

NOTES:

1. All voltages are referenced to ground.
2. When both the battery and supply pins are being used, V_{CCI} should be at least 500 mV higher than V_{BAT} when V_{CCI} is supplying power.
3. V_{CC} applies to the greater of V_{CCI} or V_{BAT} depending on which input is supplying power.
4. V_{CCO} is either V_{CCI} -0.3 V or V_{BAT} -0.3 V.
5. I_{CCO} is current coming from V_{BAT} or V_{CCI} depending on which input is supplying power.
6. Operating current comes from V_{CCI} or V_{BAT} depending on which is supplying power and if power is consumed by the DS1209S-B1 when comparator or 1-wire is active.
7. With freshness seal not broken, receiver standby current is 50 nA.
8. Leakage current applies to all inputs except V_{CCI} and V_{BAT}. 1 IN/OUT, TRI, and DQTRI have 150 µA max. leakage to ground.
9. Input signal is a sine wave, measured in peak-to-peak millivolts at a frequency of 133.3 KHz.

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