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Rev 0, 07/2002

Preliminary Information

Single-Wire CAN Transceiver

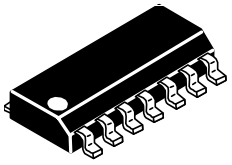
33897

SINGLE-WIRE CAN TRANSCEIVER

The 33897 is intended to be used as the physical interface in an SWCAN (Single-Wire Controller Area Network) application. It supports both the standard 33.333 kbps communications rate and the high-speed service rate of 83.333 kbps. The modes (speed, high-voltage wakeup [HVWU], and sleep) are controlled by the state of two input pins for easy MCU interfacing.

Features

- 33.33 kbps Data Rate with Loading per J2411
- Waveshaping for Low EMI
- High-Speed Mode up to 83.33 kbps
- Responds to High-Voltage Wakeup
- CNTL Output to External Regulator for Bus-Controlled Module Wakeup
- Built-In Delay Timers to Allow MCU-Required Wakeup Timing
- Detects and Automatically Handles Loss of Ground
- Extended Frame Tolerance
- Worst-Case Sleep Mode Current of Only 80 μA
- Current Limit Prevents Damage Due to Bus Shorts
- Built-In Thermal Shutdown on Bus Output
- Protected Against Vehicular Electrical Transients
- Undervoltage Lockout Prevents False Data with Low Battery
- Designed to Meet GMW3089 V2.1 Requirements

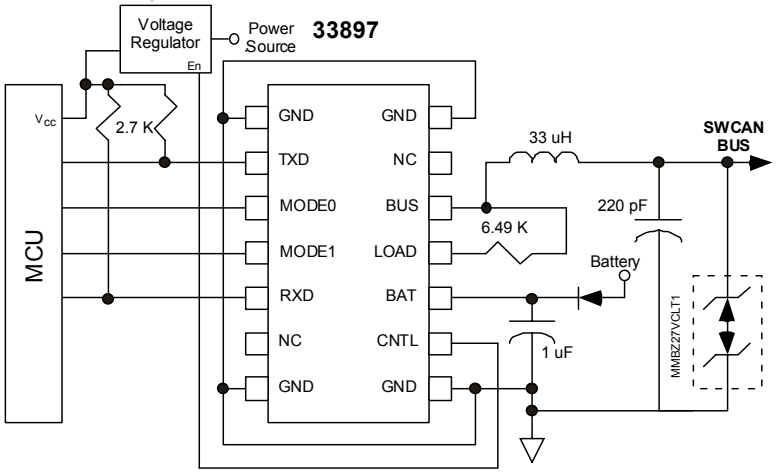


D SUFFIX
14-LEAD NARROW SOIC
CASE 751A

PIN CONNECTIONS

1	GND
2	TXD
3	MODE0
4	MODE1
5	RXD
6	NC
7	GND
8	GND
9	CNTL
10	BAT
11	LOAD
12	BUS
13	NC
14	GND

33897 Simplified Application Diagram



ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PC33897D	-40 to 125°C	14 SOIC

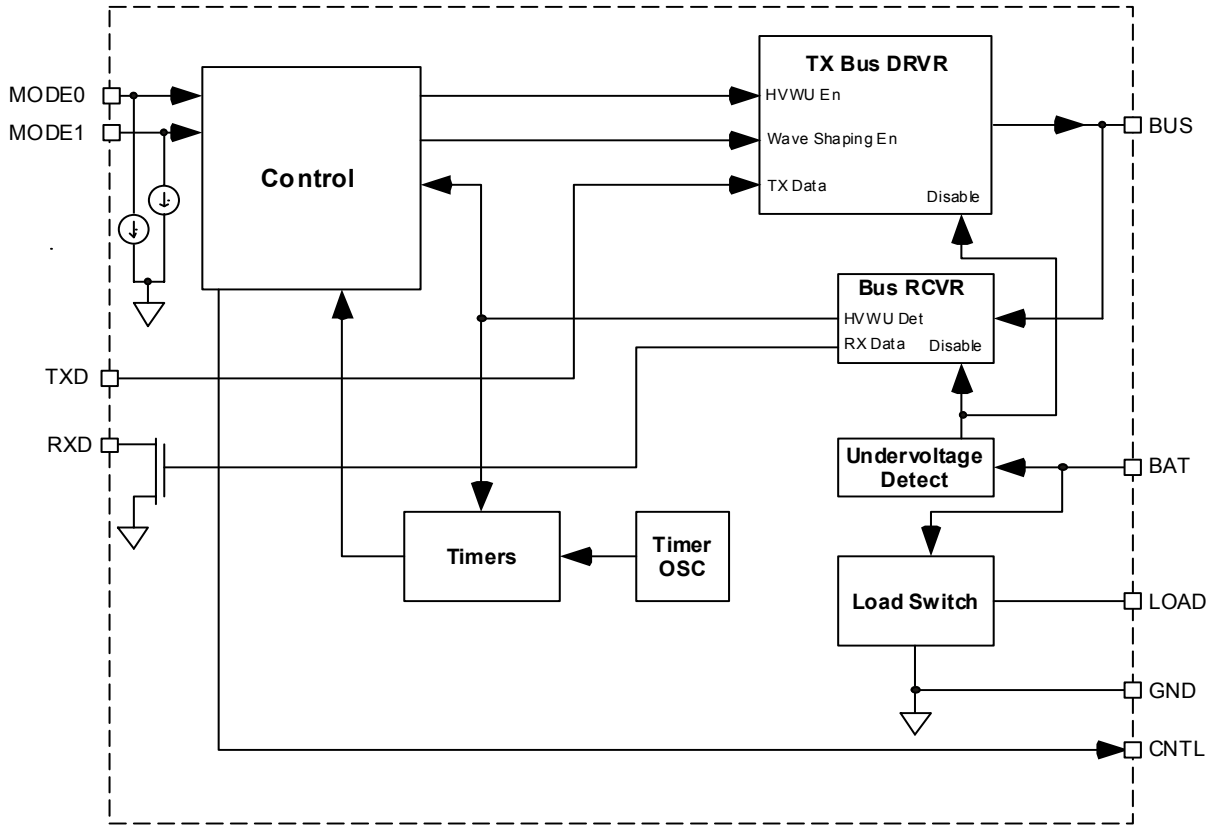


Figure 1. 33897 Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1, 7, 8, 14	GND	Electrical Common Ground and Heat removal. A good thermal path will also reduce the die temperature.
2	TXD	Data input here will appear on the BUS pin. A logic “0” will assert the bus, a “1” will go to the recessive state.
3, 4	MODEn	These control Sleep Mode, Transmit Level, and Speed. They have weak pull-downs.
5	RXD	Open drain output of the data on BUS. A recessive bus = “1”, dominant = “0”. An external pull-up is required.
6, 13	NC	No internal connection to this pin.
9	CNTL	Enables an external regulator when not in Sleep mode. The regulator should be activated by a logic high level.
10	BAT	Power input. An external diode is needed for reverse battery protection.
11	LOAD	The external bus load resistor connects here to prevent bus pull-up in the case of loss of module ground.
12	BUS	This pin connects to the bus through external components.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Supply Voltage	V_{BATT}	40	V
Input Logic Voltage	V_{IN}	-0.3 to 7.0	V
RXD	V_{RXD}	-0.3 to 7.0	V
CNTL	V_{CNTL}	-0.3 to 40	V
ESD1 Voltage (All Pins) (Note 1)	V_{ESD1}	2000	V
ESD2 Voltage (All Pins) (Note 2)	V_{ESD2}	200	V
Storage Temperature	T_{STG}	-55 to +150	°C
Operating Ambient Temperature	T_A	-40 to +125	°C
Operating Junction Temperature	T_J	-40 to +150	°C
Junction-to-Ambient Thermal Resistance	$R_{\theta J-A}$	150	°C/W
Soldering Temperature (for 10 seconds)	T_{SOLDER}	260	°C

Notes:

1. ESD1 performed in accordance with Human Body Model (C_{ZAP} = 100 pF, R_{ZAP}= 1500 Ω).
2. ESD2 performed in accordance with Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).

STATIC DC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions -40°C ≤ T_A ≤ 125°C unless otherwise noted. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
Logic I/O					
Logic Input Low Threshold (MODE0, MODE1, and TXD) 5.0 V ≤ V_{BATT} ≤ 27.0 V	V_{IL}	–	–	0.8	V
Logic Input High Threshold (MODE0, MODE1, and TXD) 5.0 V ≤ V_{BATT} ≤ 27 V	V_{IH}	2.0	–	–	V
Mode Pin Pull Down Current Pin Voltage = 0.8 V, 5.0 V ≤ V_{BATT} ≤ 27 V	I_{PD}	10	–	50	μA
Receiver Output Low I_{IN} = 2.0 mA, 5.0 V ≤V_{BATT} ≤ 27 V	V_{OL}	–	–	0.45	V
CNTL Output Low I_{in} = 5.0 μA, 5.0 V ≤V_{BATT} ≤ 27 V	V_{OLCNTL}	0	–	0.8	V
CNTL Output High I_{out} = 180 μA, 5.0 V ≤ V_{BATT} ≤ 27 V	V_{OHCNTL}	V_{BATT} -0.8	–	V_{BATT}	V
General					
Passive Out Bus Leakage No Loss of Ground 0 ≤V_{BATT} ≤ 27 V, V_{BUS} = -1.5 V Loss of Ground V_{BATT} = 0, V_{BUS} = -18 V, V_{LOAD} = -18 V Passive Out Active In 0 ≤ V_{BATT} ≤ 27 V, V_{BUS} = 10 V	 I_{LEAK} I_{LKLOG} I_{LKAI}	 0 0 0	 – – –	 -10 -50 100	μA
Sleep Mode Current V_{BATT} = 13 V	I_{QSLP}	–	35	80	μA
Undervoltage Shutdown	V_{BATTUV}	2.5	4.8	5.0	V
Undervoltage Hysteresis	V_{UVHYS}	0		0.5	V
Load Pin Voltage Rise Normal I = 1.0 mA, 5.0 V ≤ V_{BATT} ≤ 27 V Loss of Ground I = 7.0 mA	V_{LDRISE}	 – –	 – –	 0.1 1.0	V

STATIC DC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions -40°C ≤ T_A ≤ 125°C unless otherwise noted. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
Transmitter					
Offset Wakeup Output High Voltage V_{BATT} = 5.0 V, 200 ≤ R_L ≤ 4596	V_{OHWUO}	V_{BATT} -1.6	–	V_{BATT}	V
Fixed Wakeup Output High Voltage 12 V ≤ V_{BATT} ≤ 27 V, 200 ≤ R_L ≤ 4596	V_{OHWUF}	9.9	–	12.5	V
High Speed Mode Output High Voltage 6.0 V ≤ V_{BATT} ≤ 18 V, R_L = 92	V_{OHHS}	4.2	–	5.1	V
Normal Mode Output High Voltage 6.0 V ≤ V_{BATT} ≤ 27 V, 200 ≤ R_L ≤ 4596	V_{OH}	4.4	4.75	5.1	V
Normal Mode Low Battery Output High Voltage V_{BATT} = 5.0 V, 200 ≤ R_L ≤ 4596	$V_{OHLOBATT}$	V_{BATT} -1.6	–	V_{BATT}	V
Bus Low Voltage V_{BATT} = 5.0 V, 200 ≤ R_L ≤ 4596	V_{OL}	-0.2	–	0.2	V
Short Circuit Bus Output Current Dominant State, 6.0 V ≤ V_{BATT} ≤ 27 V	I_{BSC}	-50	–	-350	mA
Thermal Shutdown Bus driver disabled.	T_{SD}	150	–	190	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	10	–	20	°C
Receiver					
Offset Wakeup Input High-Voltage Threshold V_{BATT} = 5.0 V	V_{BIHWUO}	V_{BATT} -4.3	–	V_{BATT} -3.25	V
Fixed Wakeup Input High-Voltage Threshold 12 V ≤ V_{BATT} ≤ 27 V	V_{BIHWUF}	6.6	–	7.9	V
High Speed and Normal Mode Input High-Voltage Input Threshold 5.0 V ≤ V_{BATT} ≤ 27 V	V_{BIH}	2.0	2.1	2.2	V

DYNAMIC AC TIMING

Characteristics noted under conditions -40°C ≤ T_A ≤ 125°C unless otherwise noted. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
Transmitter					
Normal Speed Delay 200 ≤R_L ≤ 4596 Rising Output – Measured from TXD = V_{IL} to V_{BUS} as follows: Max Time to V_{BUS} = 3.7 V, Load time constant = 4.0 µS, 6.0 V ≤ V_{BATT} ≤27 V Min Time to V_{BUS} = 1.0 V, Load time constant = 1.0 µS, 6.0 V ≤ V_{BATT} ≤27 V Max Time to V_{BUS} = 2.7 V, Load time constant = 4.0 µS, V_{BATT} = 5.0 V Min Time to V_{BUS} = 2.7 V, Load time constant = 1.0 µS, V_{BATT} = 5.0 V Falling Output – Measured from TXD = V_{IH} to V_{BUS} as follows: Max Time to V_{BUS} = 1.0 V, Load time constant = 4.0 µS, 6.0 V ≤ V_{BATT} ≤ 27 V Min Time to V_{BUS} = 3.7 V, Load time constant = 1.0 µS, 6.0 V ≤ V_{BATT} ≤ 27V Max Time to V_{BUS} = 1.0 V, Load time constant = 4.0 µS, V_{BATT} = 5.0 V Min Time to V_{BUS} = 1.0 V, Load time constant = 1.0 µS, V_{BATT} = 5.0 V	$T_{DLYNORM}$	3.0	–	6.3	µSec
High Speed Delay Time R_L = 92 Rising Output – Measured from TXD = V_{IL} to V_{BUS} as follows: Max Time to V_{BUS} = 3.7 V, Load time constant = 1.5 µS, 8.0 V ≤ V_{BATT} ≤ 27 V Min Time to V_{BUS} = 1.0 V, Load time constant = 0 µS, 8.0 V ≤ V_{BATT} ≤ 27 V Falling Output – Measured from TXD = V_{IH} to V_{BUS} as follows: Max Time to V_{BUS} = 1.0 V, Load time constant = 1.5 µS, 8.0 V ≤ V_{BATT} ≤ 27V Min Time to V_{BUS} = 3.7 V , Load time constant = 0 µS, 8.0 V ≤ V_{BATT} ≤ 27 V	T_{DLYHS}	0.1	–	1.5	µSec

DYNAMIC AC TIMING

Characteristics noted under conditions -40°C ≤ T_A ≤ 125°C unless otherwise noted. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
Transmitter					
High Voltage Delay Time	T_{DLYHV}				
200 ≤RL ≤ 4596					µSec
Rising Output – Measured from V_{IL} to V_{BUS} as follows:					
Max Time to V_{BUS} = 3.7 V, Load time constant = 4.0 µS, 6.0 V ≤ V_{BATT} ≤ 27 V		3.0	–	6.3	
Min Time to V_{BUS} = 1.0 V, Load time constant = 1.0 µS, 6.0 V ≤ V_{BATT} ≤ 27 V		3.0	–	6.3	
Max Time to V_{BUS} = 9.4 V, Load time constant = 4.0 µS, 12.0 V ≤ V_{BATT} ≤ 27 V		3.0	–	18	
Falling Output – Measured from V_{IH} to V_{BUS} as follows:					
Max Time to V_{BUS} = 1.0 V, Load time constant = 4.0 µS, 12.0 V ≤ V_{BATT} ≤27 V		3.0	–	TBD	
Min Time to V_{BUS} = 9.4 V, Load time constant = 1.0 µS, 12.0 V ≤ V_{BATT} ≤ 27V		3.0	–	TBD	
Bus Disable Delay	T_{DLYDIS}		1.0		mSec
From passive to bus disabled					
Receiver					
Receive Delay Time (6.0 V ≤ V_{BATT} ≤ 27 V, Bus Rising to RXD falling)	T_{RDLY}				µSec
Awake		0.2	–	TBD	
Sleep		10	–	70	
CNTL Transition to Sleep Hold Time	$T_{CNTLHLD}$				mSec
From low voltage to high voltage on bus, MODE0, and MODE1 must be ≤ V_{IL} at end of T_{CNTHLD}.		0.75	–	10	
CNTL Power-Up Hold Time	T_{CNTLPU}				mSec
From rising edge of V_{BATT} ≥ 5.5 V		100	–	1000	

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33897 is intended for use as a physical layer device in a single-wire CAN communications bus. The communications takes place from a single pin over a single wire using a common ground for a current return path. Two data rates are available, with the high rate used for factory or assembly line communications and the lower for actual system communications where the radiated EMI of the higher rate could be an issue.

Two pins control of the mode of operation (sleep, low-speed, high-speed, and high voltage wakeup).

BLOCK DIAGRAM COMPONENTS

Timer OSC

This circuit generates a 500 kHz signal to be used for internal logic. It is the reference for some of the required delays.

Timer

This circuit contains the timing logic used to hold the CNTL active for the required time after the conditions for sleep mode have been met. It is also used to keep the TXD driver active for a period of time after the it has generated a passive level on the bus.

Control

This circuit contains the control logic for the various operating modes and conditions required for the IC.

Bus RCVR

This circuit translates the levels on the BUS pin to a CMOS level indicating the presence of a data 0 or 1. It also determines the presence of a High-Voltage Wakeup Signal that is passed to CONTROL and TIMERS. An analog filter is used to “de-glitch” the high-voltage wakeup signal and prevent false exits from the sleep mode.

TX Bus DRVR

This circuit drives the bus. It can drive it with the higher voltage wakeup signals when enabled by the MODE CONTROL. It can also provide waveshaping for reduced EMI or not provide it for the higher data rate mode. The actual data is received on TXD at CMOS logic levels, then translated by this circuit to the necessary operating voltages.

Undervoltage Detect

This circuit monitors internal operating voltage to assure proper operation of the part. If a low-voltage condition is detected, it sends a signal to disable the Bus RCVR and Tx Bus DRVR. This prevents incorrect data from being put on the Bus or sent to the MCU.

Load Switch

The load switch provides a path for an external resistor connected to the bus to be connected to ground. When a loss of ground is detected, this switch is opened to prevent the current that would normally be flowing to the ground from the module from going back through the load resistor and raising the bus level. The circuit is opened when the voltage between GND and BAT becomes too low as would be the case if module ground were lost.

OPERATION

The 33897 is intended to be used with an MCU to control its operation and to process and generate the data for the bus.

Ground Pins

The four ground pins are not only for electrical conduction, their number and locations at each of the four corners serve also to remove heat from the IC. The biggest benefit of this is obtained by putting a lot of copper on the PCB in this area and, if ground is an internal layer, by adding numerous plated through connections to it with the largest diameter holes the layout can use.

TX Data

The data driven onto the SWCAN Bus is inverted from the TXD pin. A “1” driven on TXD will result in an undriven (recessive) state (bus at near zero volts). When the TXD pin is low, the output goes to a driven state. The voltage and waveshaping in the driven state is determined by the levels on the MODE0 and MODE1 pins (see Table 1).

Table 1. Mode Control

MODE0	MODE1	Operation
0	0	Sleep Mode
0	1	Transmit High Voltage (Wakeup)
1	0	Transmit High Speed
1	1	Normal Speed and Voltage

Mode Control

The Mode pins control the transmitter filtering and bus voltage and the IC sleep mode operation. Table 1 shows the mode versus the logic levels on MODE0 and MODE1.

The MODE0 and MODE1 pins have a weak pull-down in the IC so that in case the pins are not driven, the device will enter the sleep mode. This is usually the situation as the MCU comes out of reset, before the driving signals have been configured as outputs.

RX Data

The data received on the Bus is translated to logic levels on this pin. This pin is a logic high when the bus is in the recessive state (near zero volts) and is low when in the bus is in either the normal or high voltage dominant state.

This is an open-drain type of output that requires an external resistor to pull it up. When the device is in sleep mode, the output will be off unless a high-voltage wakeup level is detected on the bus. If the wakeup level is detected, the output will be driven by the data on the bus. If the level of the data returns to normal level, the output will return to off after a short delay unless a non-sleep mode condition is set by the MCU.

Load Switch

This switch is on in all operating modes unless a loss of ground is detected. If this happens, the switch is opened and the resistor normally attached to its pin will be no longer pass current to or from the bus.

CNTL Output

This logic level signal is used to control a V_{CC} regulator. When the output is low, the V_{CC} regulator is expected to shutdown. This is normally used to shut down the MCU and all the devices powered by V_{CC} when the IC is in sleep mode. This is done to save power. When the part is taken out of the sleep mode by the higher than normal bus voltage, this pin is asserted high and the Vcc regulator brings its output up to the regulated level. This starts the MCU, which controls the mode of the IC. The MCU must change the mode signals to non-sleep mode levels in order to keep this pin from going low. There is a delay to allow the MCU to fully wake up and take control after the high-voltage signaling is removed before the level on this output returns low. After a delay time, even if the bus is at high voltage, the IC will return to sleep mode if both mode pins are low.

BAT Input

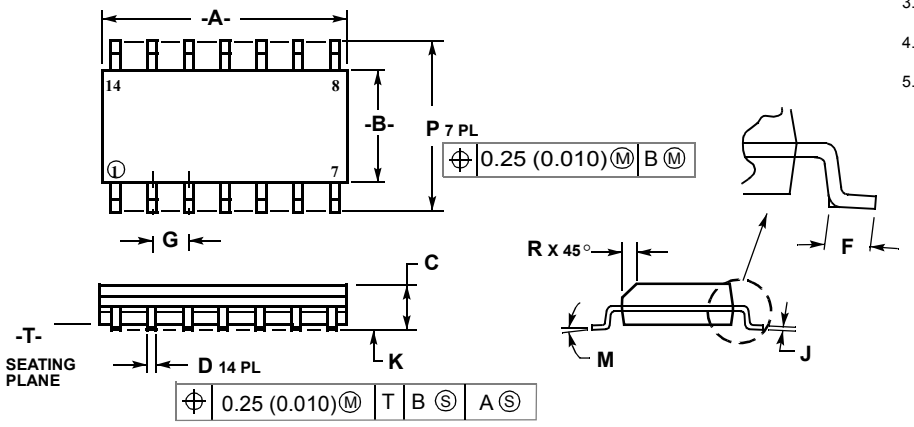
This power input is not reverse battery protected and should use an external diode to protect it from damage due to reverse battery if this protection is desired. The voltage drop of the diode must be taken into consideration when the operating range of the system is being determined. This diode is generally used to protect the entire module from reverse battery and should be selected accordingly.

BUS I/O

This Input/Output may require ESD and/or EMI external circuitry. A set of components is shown in the Simplified Application Diagram on the front of this data sheet. The value of the capacitor should be adjusted downward in direct proportion to the added capacitance of the ESD or EMI circuits. The series resistance of the inductor should be kept below 3.5 Ω to prevent its voltage drop from significantly degrading system noise margins.

PACKAGE DIMENSIONS

D SUFFIX
(14-LEAD SOIC)
CASE 751A-03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

NOTES

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