Integrated Device Technology, Inc.

Quad PHY (Physical Layer) for 25.6 and 51.2 Mbps ATM Networks

ADVANCE INFORMATION
IDT77V1254

FEATURES

- Performs the PHY-Transmission Convergence (TC) and Physical Media Dependent (PMD) Sublayer functions for four 25.6 Mpbs ATM channels
- Compliant to ATM Forum specification for 25.6 Mbps physical interface (af-phy-040.000)
- UTOPIA Level 1, UTOPIA Level 2, or DPI-4 Interface
- 2-Cell Transmit & Receive FIFOs
- Supports Multi PHY Connections
- LED Interface for status signalling
- Supports UTP Category 3 (CAT 3) physical media
- Interfaces to standard magnetics
- Low-Power CMOS
- 3.3V operation with 5V tolerant inpouts
- 144-pin PQFP Package (28 x 28mm)

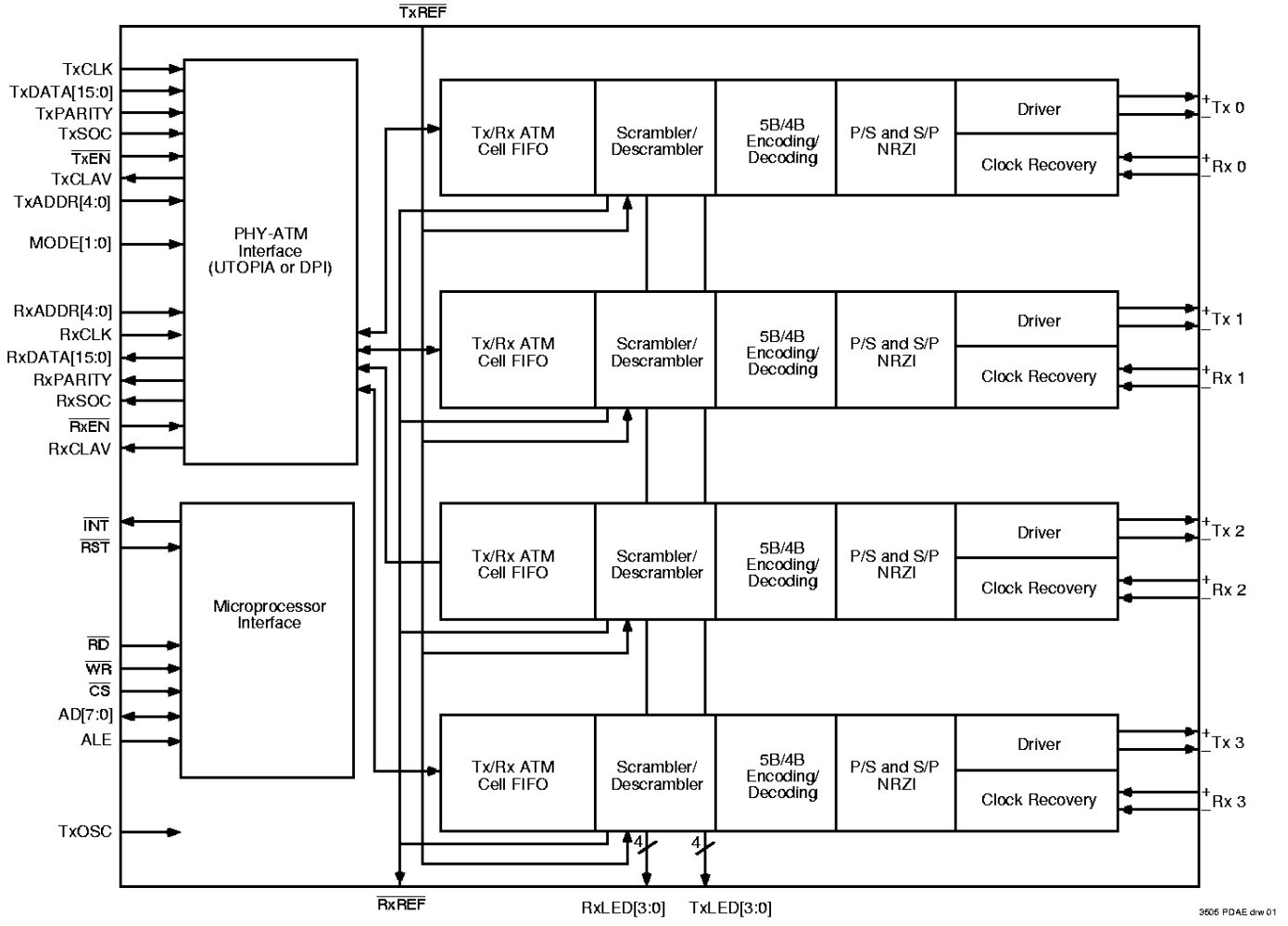
DESCRIPTION

The IDT77V1254 is a member of IDT's family of products developed to support Asynchronous Transfer Mode (ATM) data communications and networking. The IDT77V1254 implements the physical layer layer for 25.6 Mbps ATM, connecting four serial copper links (UTP Category 3) to one ATM layer device (such as a SAR or a switch ASIC). The 77V1254-to-ATM layer interface is selectable as one of three options: 16-bit UTOPIA Level 2, 8-bit UTOPIA Level 1, or quadruple 4-bit DPI (Data Path Interface).

The IDT77V1254 supports a simple interface to magnetics modules.

The IDT77V1254 is fabricated using IDT's state-of-the-art CMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	VDD	37	TXADDR3	73	RXDATA3	109	TX2-
2	GND	38	VDD	74	RXDATA2	110	TX2+
3	TX0-	39	TXADDR2	75	RXDATA1	111	GND
4	TX0+	40	TXADDR1	76	RXDATA0	112	AGND
5	VDD	41	TXADDR0	77	GND	113	AVDD
6	MM	42	TXCLAV	78	VDD	114	RX3-
7	MODE1	43	TXCLK	79	RXLED0	115	RX3+
8	MODE0	44	GND	80	RXLED1	116	AVDD
9	$\overline{\text{RXREF}}$	45	VDD	81	RXLED2	117	AGND
10	$\overline{\text{TXREF}}$	46	RXCLK	82	RXLED3	118	AGND
11	GND	47	$\overline{\text{RXEN}}$	83	GND	119	AVDD
12	TXLED3	48	RXADDR0	84	VDD	120	RX2-
13	TXLED2	49	RXADDR1	85	$\overline{\text{INT}}$	121	RX2+
14	TXLED1	50	GND	86	GND	122	AVDD
15	TXLED0	51	RXADDR2	87	$\overline{\text{RST}}$	123	AGND
16	VDD	52	RXADDR3	88	$\overline{\text{WR}}$	124	AGND
17	TXDATA0	53	RXADDR4	89	$\overline{\text{RD}}$	125	AVDD
18	TXDATA1	54	RXCLAV	90	$\overline{\text{CS}}$	126	TXOSC
19	TXDATA2	55	RXSOC	91	ALE	127	AGND
20	TXDATA3	56	GND	92	VDD	128	AVDD
21	TXDATA4	57	VDD	93	AD0	129	AGND
22	TXDATA5	58	RXPARITY	94	AD1	130	AGND
23	TXDATA6	59	RXDATA15	95	AD2	131	AVDD
24	TXDATA7	60	RXDATA14	96	AD3	132	RX1-
25	TXDATA8	61	RXDATA13	97	GND	133	RX1+
26	TXDATA9	62	RXDATA12	98	AD4	134	AVDD
27	TXDATA10	63	RXDATA11	99	AD5	135	AGND
28	TXDATA11	64	RXDATA10	100	AD6	136	AGND
29	TXDATA12	65	RXDATA9	101	AD7	137	AVDD
30	TXDATA13	66	RXDATA8	102	SE	138	RX0-
31	TXDATA14	67	GND	103	DA	139	RX0+
32	TXDATA15	68	VDD	104	VDD	140	AVDD
33	TXPARITY	69	RXDATA7	105	TX3-	141	AGND
34	$\overline{\text{TXEN}}$	70	RXDATA6	106	TX3+	142	GND
35	TXSOC	71	RXDATA5	107	GND	143	TX1-
36	TXADDR4	72	RXDATA4	108	VDD	144	TX1+

SIGNAL DESCRIPTIONS

SIGNAL NAME	PIN NUMBER	I/O	SIGNAL DESCRIPTION
AD[7:0]	101, 100, 99, 98 96, 95, 94, 93	In/Out	Utility bus address/data bus. The address input is sampled on the falling edge of ALE. Data is output on this bus when a read is performed. Input data is sampled at the completion of a write operation.
AGND	112, 117, 118, 123,124,127, 129,130,135, 136, 141	-	Analog ground. This grounds the noise sensitive analog portion of the circuit which need isolation from the noisier digital portion. The analog load is constant, with minimal current switching.
ALE	91	In	Utility bus address latch enable. Asynchronous input. An address on the AD bus is sampled on the falling edge of ALE. ALE may be either high low when the AD bus is being used for data.
AVDD	113, 116, 119, 122, 125, 128, 131, 134, 137, 140	-	Analog power supply. 3.3 ± 0.3V This powers the noise sensitive analog portion of the circuit which need isolation from the noisier digital portion. The analog load is constant, with minimal current switching.
$\overline{CS}$	90	In	Utility bus asynchronous chip select. $\overline{CS}$ must be asserted to read or write an internal register. It may remain asserted at all times if desired.
DA	103	In	Reserved signal. This input must be connected to logic low.
GND	2, 11, 44, 50, 56 67, 77, 83, 86, 97, 107, 111, 142	-	Digital Ground
$\overline{INT}$	85	Out	Interrupt. $\overline{INT}$ is driven low to indicate an interrupt. Once low, $\overline{INT}$ remains low until the interrupt status in the appropriate register (01, 11, 21 or 31) is read. Interrupt sources are programmable via registers 07, 17, 27 and 37.
MM	6	In	Reserved signal. This input must be connected to logic low.
MODE[1:0]	7, 8	In	Mode Selects. They determine the configuration of the PHY/ATM interface. 00 = UTOPIA Level 2. 01 = UTOPIA Level 1. 10 = DPI. 11 is reserved.
$\overline{RD}$	89	In	Utility bus read enable. Active low asynchronous input. After latching an address, a read is performed by deasserting $\overline{WR}$ and asserting $\overline{RD}$ and $\overline{CS}$.
$\overline{RST}$	87	In	Reset. Active low asynchronous input resets all control logic, counters and FIFOs. A reset must be performed after power up prior to normal operation of the part.
RX0+, -	139, 138	Out	Port 0 positive and negative receive differential input pair
RX1+, -	133, 132	Out	Port 1 positive and negative receive differential input pair
RX2+, -	121, 120	Out	Port 2 positive and negative receive differential input pair
RX3+, -	115, 114	Out	Port 3 positive and negative receive differential input pair
RXADDR[4:0]	53, 52, 51, 49, 48	Mode Dependent	Function depends on PHY/ATM interface mode. Please see appropriate section.
RXCLAV	54	Out	Function depends on PHY/ATM interface mode. Please see appropriate section.
RXCLK	46	In	Function depends on PHY/ATM interface mode. Please see appropriate section.
RXDATA[15:0]	59, 60, 61, 62, 63, 64, 65, 66, 69, 70, 71, 72, 73, 74, 75, 76	Out	Function depends on PHY/ATM interface mode. Please see appropriate section.
$\overline{RXEN}$	47	In	Function depends on PHY/ATM interface mode. Please see appropriate section.

SIGNAL DESCRIPTIONS (continued)

SIGNAL NAME	PIN NUMBER	I/O	SIGNAL DESCRIPTION
RXLED[3:0]	82, 81, 80, 79	Out	Receive LED drivers. Driven low for 262ms beginning with RXSOC when that port receives a good cell. Drives 8mA both high and low. One per port.
RXPARITY	58	Out	Function depends on PHY/ATM interface mode. Please see appropriate section.
$\overline{\text{RXREF}}$	9	Out	Receive Reference. Active low, synchronous to TXOSC. $\overline{\text{RXREF}}$ pulses low for a programmable number of clock cycles when an X-8 command byte is received. Register 40 is programmed to indicate which port is referenced.
RXSOC	55	Out	Function depends on PHY/ATM interface mode. Please see appropriate section.
SE	102	In	Reserved signal. This input must be connected to logic low.
TX0+, -	4, 3	Out	Port 0 positive and negative transmit differential output pair
TX1+, -	144, 143	Out	Port 1 positive and negative transmit differential output pair
TX2+, -	110, 109	Out	Port 2 positive and negative transmit differential output pair
TX3+, -	106, 105	Out	Port 3 positive and negative transmit differential output pair
TXADDR[4:0]	36, 37, 39, 40, 41	Mode Dependent	Function depends on PHY/ATM interface mode. Please see appropriate section.
TXCLAV	42	Out	Function depends on PHY/ATM interface mode. Please see appropriate section.
TXCLK	43	In	Function depends on PHY/ATM interface mode. Please see appropriate section.
TXDATA[15:0]	32, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17	In	Function depends on PHY/ATM interface mode. Please see appropriate section.
$\overline{\text{TXEN}}$	34	In	Function depends on PHY/ATM interface mode. Please see appropriate section.
TXLED[3:0]	12, 13, 14, 15	Out	Ports 3 thru 0 Transmit LED driver. Driven low for 262ms beginning with TXSOC when this port receives a cell for transmission. 8mA drive current both high and low. One per port.
TXOSC	126	In	32MHz line rate clock input used for transmision. Typically driven by an oscillator.
TXPARITY	33	In	Function depends on PHY/ATM interface mode. Please see appropriate section.
$\overline{\text{TXREF}}$	10	In	Transmit Reference. Synchronous to TXOSC. When this pin is asserted, an X_8 command byte is inserted into the transmit data stream. Logic for this signal is programmed in register 40. Typical application is WAN timing.
TXSOC	35	In	Function depends on PHY/ATM interface mode. Please see appropriate section.
VDD	1, 5, 16, 38, 45 57, 68, 78, 84, 92, 104, 108	-	Digital power supply. 3.3 ±0.3V
$\overline{\text{WR}}$	88	In	Utility bus write enable. Active low asynchronous input. After latching an address, a write is performed by deasserting $\overline{\text{RD}}$, placing data on the AD bus, and asserting $\overline{\text{WR}}$ and $\overline{\text{CS}}$. Data is sampled when $\overline{\text{WR}}$ or $\overline{\text{CS}}$ is deasserted.

UTOPIA 2 MODE SIGNAL DESCRIPTIONS

SIGNAL NAME	PIN MUMBER	I/O	UTOPIA 2 MODE SIGNAL DESCRIPTION
AD[7:0]		In/Out	please see note 1
AGND		-	please see note 1
ALE		In	please see note 1
AVDD		-	please see note 1
$\overline{CS}$		In	please see note 1
DA		In	please see note 1
GND		-	please see note 1
$\overline{INT}$		Out	please see note 1
MM		In	please see note 1
MODE[2:0]		In	please see note 1
$\overline{RD}$		In	please see note 1
$\overline{RST}$		In	please see note 1
RX[3:0]+, -		Out	please see note 1
RXADDR048		In	UTOPIA Receive Address bit 0
RXADDR1	49	In	UTOPIA Receive Address bit 1
RXADDR2	51	In	UTOPIA Receive Address bit 2
RXADDR3	52	In	UTOPIA Receive Address bit 3
RXADDR4	53	In	UTOPIA Receive Address bit 4
RXCLAV	54	Out	UTOPIA Receive FIFO Empty / Cell Available. Bit 1 of rbus operates in cell mode or byte mode.egisters 00, 10, 20, and 30 determines whether the UTOPIA
RXCLK	46	In	UTOPIA Receive Clock
RXDATA0	76	Out	UTOPIA Receive Data bit 0
RXDATA1	75	Out	UTOPIA Receive Data bit 1
RXDATA2	74	Out	UTOPIA Receive Data bit 2
RXDATA3	73	Out	UTOPIA Receive Data bit 3
RXDATA4	72	Out	UTOPIA Receive Data bit 4
RXDATA5	71	Out	UTOPIA Receive Data bit 5
RXDATA6	70	Out	UTOPIA Receive Data bit 6
RXDATA7	69	Out	UTOPIA Receive Data bit 7
RXDATA8	66	Out	UTOPIA Receive Data bit 8
RXDATA9	65	Out	UTOPIA Receive Data bit 9
RXDATA10	64	Out	UTOPIA Receive Data bit 10
RXDATA11	63	Out	UTOPIA Receive Data bit 11
RXDATA12	62	Out	UTOPIA Receive Data bit 12
RXDATA13	61	Out	UTOPIA Receive Data bit 13
RXDATA14	60	Out	UTOPIA Receive Data bit 14
RXDATA15	59	Out	UTOPIA Receive Data bit 15
$\overline{RXEN}$	47	In	UTOPIA Receive Enable
RXLED[3:0]		Out	please see note 1
RXPARITY	58	Out	UTOPIA Receive Data Parity bit. Parity is generated to match the 16-bit receive word.
$\overline{RXREF}$		Out	please see note 1
RXSOC	55	Out	UTOPIA Receive Start of Cell
SE		In	please see note 1
TX[3:0]+, -		Out	please see note 1
TXADDR0	41	In	UTOPIA Transmit Address bit 0

UTOPIA 2 MODE SIGNAL DESCRIPTIONS (continued)

SIGNAL NAME	PIN MUMBER	I/O	UTOPIA 2 MODE SIGNAL DESCRIPTION
TXADDR1	40	In	UTOPIA Transmit Address bit 1
TXADDR2	39	In	UTOPIA Transmit Address bit 2
TXADDR3	37	In	UTOPIA Transmit Address bit 3
TXADDR4	36	In	UTOPIA Transmit Address bit 4
TXCLAV	42	Out	UTOPIA Transmit FIFO Full / Cell Available. Bit 1 of registers 00, 10, 20, and 30 determines whether the UTOPIA bus operates in cell mode or byte mode.
TXCLK	43	In	UTOPIA Transmit Clock
TXDATA0	17	In	UTOPIA Transmit Data bit 0
TXDATA1	18	In	UTOPIA Transmit Data bit 1
TXDATA2	19	In	UTOPIA Transmit Data bit 2
TXDATA3	20	In	UTOPIA Transmit Data bit 3
TXDATA4	21	In	UTOPIA Transmit Data bit 4
TXDATA5	22	In	UTOPIA Transmit Data bit 5
TXDATA6	23	In	UTOPIA Transmit Data bit 6
TXDATA7	24	In	UTOPIA Transmit Data bit 7
TXDATA8	25	In	UTOPIA Transmit Data bit 8
TXDATA9	26	In	UTOPIA Transmit Data bit 9
TXDATA10	27	In	UTOPIA Transmit Data bit 10
TXDATA11	28	In	UTOPIA Transmit Data bit 11
TXDATA12	29	In	UTOPIA Transmit Data bit 12
TXDATA13	30	In	UTOPIA Transmit Data bit 13
TXDATA14	31	In	UTOPIA Transmit Data bit 14
TXDATA15	32	In	UTOPIA Transmit Data bit 15
$\overline{\text{TXEN}}$	34	In	UTOPIA Transmit Enable
TXLED[3:0]		Out	please see note 1
TXOSC		In	please see note 1
TXPARITY	33	In	UTOPIA Transmit Data Parity bit. Bit 4 of registers 00, 10, 20 and 30 determines if a parity check is performed on the transmit data.
$\overline{\text{TXREF}}$		In	please see note 1
TXSOC	35	In	UTOPIA Transmit Start of Cell
VDD	-		please see note 1
$\overline{\text{WR}}$		In	please see note 1

Note 1: This signal is common to all modes and is described in another table.

UTOPIA 1 MODE SIGNAL DESCRIPTIONS

SIGNAL NAME	PIN NUMBER	I/O	ALTERNATE SIGNAL NAME	UTOPIA 1 MODE SIGNAL DESCRIPTION
AD[7:0]		In/Out		please see Note 1
AGND		-		please see Note 1
ALE		In		please see Note 1
AVDD		-		please see Note 1
$\overline{CS}$		In		please see Note 1
DA		In		please see Note 1
GND		-		please see Note 1
$\overline{INT}$		Out		please see Note 1
MM		In		please see Note 1
MODE[2:0]		In		please see Note 1
$\overline{RD}$		In		please see Note 1
$\overline{RST}$		In		please see Note 1
RX[3:0]+, -		Out		please see Note 1
RXADDR0	48	In	$\overline{RXEN}$[1]	Port 1 UTOPIA Receive Enable
RXADDR1	49	In	$\overline{RXEN}$[2]	Port 2 UTOPIA Receive Enable
RXADDR2	51	In	$\overline{RXEN}$[3]	Port 3 UTOPIA Receive Enable
RXADDR3	52	In		please see Note 2
RXADDR4	53	In		please see Note 2
RXCLAV	54	Out	RXCLAV[0]	Port 0 UTOPIA Receive FIFO Empty / Cell Available. Bit 1 of register 00h determines whether the UTOPIA bus operates in cell mode or byte mode.
RXCLK	46	In		UTOPIA Receive CLock
RXDATA0	76	Out		UTOPIA Receive Data bit 0
RXDATA1	75	Out		UTOPIA Receive Data bit 1
RXDATA2	74	Out		UTOPIA Receive Data bit 2
RXDATA3	73	Out		UTOPIA Receive Data bit 3
RXDATA4	72	Out		UTOPIA Receive Data bit 4
RXDATA5	71	Out		UTOPIA Receive Data bit 5
RXDATA6	70	Out		UTOPIA Receive Data bit 6
RXDATA7	69	Out		UTOPIA Receive Data bit 7
RXDATA8	66	Out	RXCLAV[1]	Port 1 UTOPIA Receive FIFO Empty / Cell Available. Bit 1 of register 10 determines whether the UTOPIA bus operates in cell mode or byte mode.
RXDATA9	65	Out	RXCLAV[2]	Port 2 UTOPIA Receive FIFO Empty / Cell Available. Bit 1 of register 20 determines whether the UTOPIA bus operates in cell mode or byte mode.
RXDATA10	64	Out	RXCLAV[3]	Port 3 UTOPIA Receive FIFO Empty / Cell Available. Bit 1 of register 30 determines whether the UTOPIA bus operates in cell mode or byte mode.
RXDATA11	63	Out		please see Note 3
RXDATA12	62	Out		please see Note 3
RXDATA13	61	Out		please see Note 3
RXDATA14	60	Out		please see Note 3
RXDATA15	59	Out		please see Note 3
$\overline{RXEN}$	47	In	$\overline{RXEN}$[0]	Port 0 UTOPIA Receive Enable
RXLED[3:0]		Out		please see Note 1
RXPARITY	58	Out		UTOPIA Receive Data Parity bit. Parity is gener ated to match the 8-bit receive data word.
$\overline{RXREF}$	Out			please see Note 1
RXSOC	55	Out		UTOPIA Receive Start of Cell
SE	In			please see Note 1

UTOPIA 1 MODE SIGNAL DESCRIPTIONS (continued)

SIGNAL NAME	PIN NUMBER	I/O	ALTERNATE SIGNAL NAME	UTOPIA 1 MODE SIGNAL DESCRIPTION
TX[3:0]+, -	Out			please see Note 1
TXADDR0	41	Out	TXCLAV[1]	Port 1 UTOPIA Transmit FIFO Full / Cell Available
TXADDR1	40	Out	TXCLAV[2]	Port 2 UTOPIA Transmit FIFO Full / Cell Available
TXADDR2	39	Out	TXCLAV[3]	Port 3 UTOPIA Transmit FIFO Full / Cell Available
TXADDR3	37	In		please see Note 2
TXADDR4	36	In		please see Note 2
TXCLAV	42	Out	TXCLAV[0]	Port 0 UTOPIA Transmit FIFO Full / Cell Available
TXCLK	43	In		UTOPIA Transmit Clock
TXDATA0	17	In		UTOPIA Transmit Data bit 0
TXDATA1	18	In		UTOPIA Transmit Data bit 1
TXDATA2	19	In		UTOPIA Transmit Data bit 2
TXDATA3	20	In		UTOPIA Transmit Data bit 3
TXDATA4	21	In		UTOPIA Transmit Data bit 4
TXDATA5	22	In		UTOPIA Transmit Data bit 5
TXDATA6	23	In		UTOPIA Transmit Data bit 6
TXDATA7	24	In		UTOPIA Transmit Data bit 7
TXDATA8	25	In	$\overline{\text{TXEN}}$[1]	Port 1 UTOPIA Transmit Enable
TXDATA9	26	In	$\overline{\text{TXEN}}$[2]	Port 2 UTOPIA Transmit Enable
TXDATA10	27	In	$\overline{\text{TXEN}}$[3]	Port 3 UTOPIA Transmit Enable
TXDATA11	28	In		please see Note 2
TXDATA12	29	In		please see Note 2
TXDATA13	30	In		please see Note 2
TXDATA14	31	In		please see Note 2
TXDATA15	32	In		please see Note 2
$\overline{\text{TXEN}}$	34	In	$\overline{\text{TXEN}}$[0]	Port 0 UTOPIA Transmit Enable
TXLED[3:0]		Out		please see Note 1
TXOSC		In		please see Note 1
TXPARITY	33	In		UTOPIA Transmit Data Parity bit
$\overline{\text{TXREF}}$	In			please see Note 1
TXSOC	35	In		UTOPIA Transmit Start of Cell
VDD	-			please see Note 1
$\overline{\text{WR}}$		In		please see Note 1

Note 1: This signal is common to all modes and is described in another table.
Note 2: This signal is an unused input in this mode. It must be connected to either logic high or logic low.
Note 3: This signal is an unused output in this mode. It must be left unconnected.

DPI MODE SIGNAL DESCRIPTIONS

SIGNAL NAME	PIN NUMBER	I/O	ALTERNATE SIGNAL NAME	DPI MODE SIGNAL DESCRIPTION
AD[7:0]		In/Out		please see Note 1
AGND		-		please see Note 1
ALE		In		please see Note 1
AVDD		-		please see Note 1
$\overline{CS}$		In		please see Note 1
DA		In		please see Note 1
GND		-		please see Note 1
$\overline{INT}$		Out		please see Note 1
MM		In		please see Note 1
MODE[2:0]		In		please see Note 1
$\overline{RD}$		In		please see Note 1
RST		In		please see Note 1
RX[3:0]+, -		Out		please see Note 1
RXADDR0	48	In	P0_RCLK	Port 0 DPI Receive Clock
RXADDR1	49	In	P1_RCLK	Port 1 DPI Receive Clock
RXADDR2	51	In	P2_RCLK	Port 2 DPI Receive Clock
RXADDR3	52	In	P3_RCLK	Port 3 DPI Receive Clock
RXADDR4	53	Out	P3_RFRM	Port 3 DPI Receive Start of Cell
RXCLAV	54	Out	P1_RFRM	Port 1 DPI Receive Start of Cell
RXCLK	46	In		please see Note 2
RXDATA0	76	Out	P0_RD[0]	Port 0 DPI Receive Data bit 0
RXDATA1	75	Out	P0_RD[1]	Port 0 DPI Receive Data bit 1
RXDATA2	74	Out	P0_RD[2]	Port 0 DPI Receive Data bit 2
RXDATA3	73	Out	P0_RD[3]	Port 0 DPI Receive Data bit 3
RXDATA4	72	Out	P1_RD[0]	Port 1 DPI Receive Data bit 0
RXDATA5	71	Out	P1_RD[1]	Port 1 DPI Receive Data bit 1
RXDATA6	70	Out	P1_RD[2]	Port 1 DPI Receive Data bit 2
RXDATA7	69	Out	P1_RD[3]	Port 1 DPI Receive Data bit 3
RXDATA8	66	Out	P2_RD[0]	Port 2 DPI Receive Data bit 0
RXDATA9	65	Out	P2_RD[1]	Port 2 DPI Receive Data bit 1
RXDATA10	64	Out	P2_RD[2]	Port 2 DPI Receive Data bit 2
RXDATA11	63	Out	P2_RD[3]	Port 2 DPI Receive Data bit 3
RXDATA12	62	Out	P3_RD[0]	Port 3 DPI Receive Data bit 0
RXDATA13	61	Out	P3_RD[1]	Port 3 DPI Receive Data bit 1
RXDATA14	60	Out	P3_RD[2]	Port 3 DPI Receive Data bit 2
RXDATA15	59	Out	P3_RD[3]	Port 3 DPI Receive Data bit 3
RXEN	47	In		please see Note 2
RXLED[3:0]		Out		please see Note 1
RXPARITY	58	Out	P2_RFRM	Port 2 DPI Receive Start of Cell
RXREF		Out		please see Note 1
RXSOC	55	Out	P0_RFRM	Port 0 DPI Receive Start of Cell
SE		In		please see Note 1
TX[3:0]+, -		Out		please see Note 1
TXADDR0	41	Out	P0_TCLK	Port 0 DPI Transmit Clock
TXADDR1	40	Out	P1_TCLK	Port 1 DPI Transmit Clock

DPI MODE SIGNAL DESCRIPTIONS (continued)

SIGNAL NAME	PIN NUMBER	I/O	ALTERNATE SIGNAL NAME	DPI MODE SIGNAL DESCRIPTION
TXADDR2	39	Out	P2_TCLK	Port 2 DPI Transmit Clock
TXADDR3	37	Out	P3_TCLK	Port 3 DPI Transmit Clock
TXADDR4	36	In	P3_TFRM	Port 3 DPI Transmit Start of Cell
TXCLAV	42	Out		please see Note 3
TXCLK	43	In	DPICLK	DPI Clock. This free-running input clock is used as the source for the generation of the DPI receive clocks RCLK[3:0].
TXDATA0	17	In	P0_TD[0]	Port 0 DPI Transmit Data bit 0
TXDATA1	18	In	P0_TD[1]	Port 0 DPI Transmit Data bit 1
TXDATA2	19	In	P0_TD[2]	Port 0 DPI Transmit Data bit 2
TXDATA3	20	In	P0_TD[3]	Port 0 DPI Transmit Data bit 3
TXDATA4	21	In	P1_TD[0]	Port 1 DPI Transmit Data bit 0
TXDATA5	22	In	P1_TD[1]	Port 1 DPI Transmit Data bit 1
TXDATA6	23	In	P1_TD[2]	Port 1 DPI Transmit Data bit 2
TXDATA7	24	In	P1_TD[3]	Port 1 DPI Transmit Data bit 3
TXDATA8	25	In	P2_TD[0]	Port 2 DPI Transmit Data bit 0
TXDATA9	26	In	P2_TD[1]	Port 2 DPI Transmit Data bit 1
TXDATA10	27	In	P2_TD[2]	Port 2 DPI Transmit Data bit 2
TXDATA11	28	In	P2_TD[3]	Port 2 DPI Transmit Data bit 3
TXDATA12	29	In	P3_TD[0]	Port 3 DPI Transmit Data bit 0
TXDATA13	30	In	P3_TD[1]	Port 3 DPI Transmit Data bit 1
TXDATA14	31	In	P3_TD[2]	Port 3 DPI Transmit Data bit 2
TXDATA15	32	In	P3_TD[3]	Port 3 DPI Transmit Data bit 3
$\overline{\text{TXEN}}$	34	In	P1_TFRM	Port 1 DPI Transmit Start of Cell
TXLED[3:0]		Out		please see Note 1
TXOSC		In		please see Note 1
TXPARITY	33	In	P2_TFRM	Port 2 DPI Transmit Start of Cell
$\overline{\text{TXREF}}$		In		please see Note 1
TXSOC	35	In	P0_TFRM	Port 0 DPI Transmit Start of Cell
VDD		-		please see Note 1
$\overline{\text{WR}}$		In		please see Note 1

Note 1: This signal is common to all modes and is described in another table.
Note 2: This input signal is an unused in this mode. It must be connected to either logic high or logic low.
Note 3: This output signal is an unused in this mode. It must be left unconnected.

FUNCTIONAL DESCRIPTION

25MbpsATM COMMUNICATIONS STANDARD

The IDT77V1254 implements the physical layer standard for 25.6Mbps ATM network communications. The physical layer is divided into a Physical Media Dependent sub layer (PMD) and Transmission Convergence (TC) sub layer. The PMD sub layer includes the functions for the transmitter, receiver, and timing recovery that allow connection to transmission media conforming to TIA/EIA 568 (UTP Category 3). The TC sub layer defines the line coding, scrambling, data framing and synchronization, and is described below.

• TRANSMISSION CONVERGENCE (TC) SUB LAYER

Introduction

Under control of a switch interface or Segmentation and Reassembly (SAR) unit, the 25.6Mbps ATM PHY accepts a 53-byte ATM cell, scrambles the data, appends a command byte to the beginning of the cell, and encodes the entire 53 bytes before transmission. These data transformations ensure that the signal is evenly distributed across the frequency spectrum. In addition, the serialized bit stream is NRZI coded. An 8kHz timing sync pulse may be used for isochronous communications.

Data Structure and Framing

Each 53-byte ATM cell is preceded with a command byte. This byte is distinguished by an escape symbol followed by one of 17 encoded symbols. Together, this byte forms one of seventeen possible command bytes. Three command bytes are defined:

1. **X_X** (read: 'escape' symbol followed by another 'escape'): Start-of-cell with scrambler/descrambler reset.
2. **X_4** ('escape' followed by '4'): Start-of-cell without scrambler/descrambler reset.
3. **X_8** ('escape' followed by '8'): 8kHz timing marker. This command byte is generated when the 8kHz sync pulse is detected, and has priority over all line activity (data or command bytes). It is transmitted immediately when the sync pulse is detected. When this occurs during a cell transmission, the data transfer is temporarily interrupted on an octet boundary, and the X_8 command byte is inserted. This condition is the only allowed interrupt in an otherwise contiguous transfer.

FUNCTIONAL BLOCK DIAGRAM (Continued)

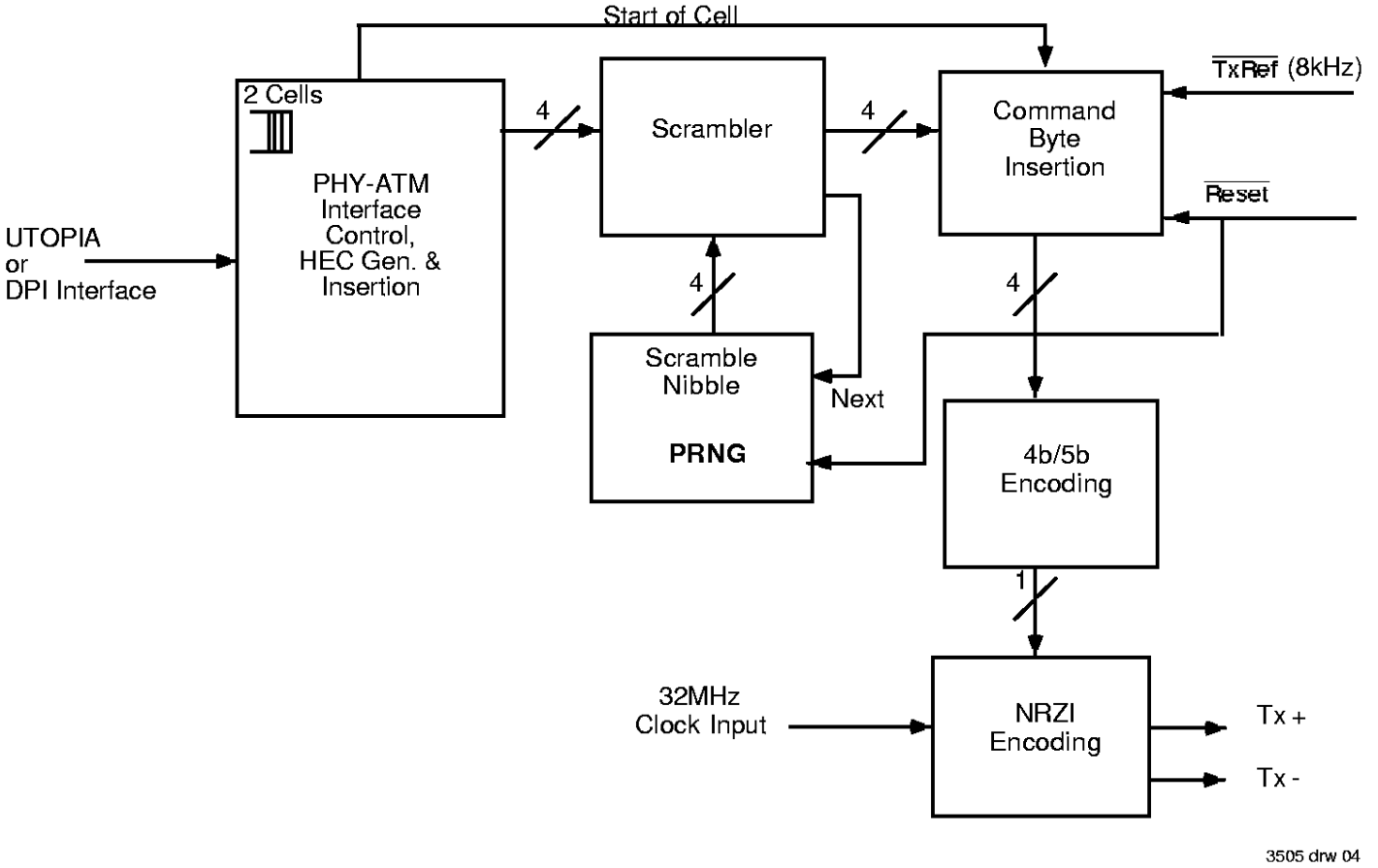


Figure 1. TC Transmit Block Diagram

Below is an illustration of the cell structure and command byte usage:

{X_X} {53-byte ATM cell} {X_4} {53-byte ATM {X_8} cell} ...

In the above example, the first ATM cell is preceded by the X_X start-of-cell command byte which resets both the transmitter-scrambler and receiver-descrambler pseudo-random nibble generators (PRNG) to their initial states. The following cell illustrates the insertion of a start-of-cell command without scrambler/descrambler reset. During this cell's transmission, an 8kHz timing sync pulse triggers insertion of the X_8 8kHz timing marker command byte.

Transmission Description

Refer to the "25Mbps PHY transmit Block Diagram" on the previous page. Cell transmission begins with the Octet Interface Control:

- The SAR (or other upstream system) confirms that the PHY may accept transmit data by polling the $\overline{\text{TxFull}}$ flag. If this signal is 'high' (PHY xmit buffer not full), the SAR then asserts $\overline{\text{TxEnb}}$.
- The SAR then asserts TxSOC for one cycle of TxCLK, while putting the first byte on the TxData bus. TxSOC is then deasserted.
- Following bytes are transmitted by putting them onto the TxData bus while $\overline{\text{TxEnb}}$ is asserted.
- 4-bit data (MSB first) is asynchronously (to TxClk) sent to the 'Scrambler'.

The 'Scrambler' takes each nibble of data and exclusive-ORs them against the 4 high order bits (X(t), X(t-1), X(t-2), X(t-3)) of a 10 bit pseudo-random nibble generator (PRNG). Its function is to provide the appropriate frequency distribution for the signal across the line.

The PRNG is clocked every time a nibble is processed, regardless of whether the processed nibble is part of a data or command byte. Note however that only data nibbles are scrambled. The entire command byte (X_C) is NOT scrambled before it's encoded (see diagram for illustration). The PRNG is based upon the following polynomial:

$$X^{10} + X^7 + 1$$

With this polynomial, the four output data bits (D3, D2, D1, D0) will be generated from the following equations:

D3 = d3 xor X(t-3)
D2 = d2 xor X(t-2)
D1 = d1 xor X(t-1)
D0 = d0 xor X(t)

The following nibble is scrambled with X(t+4), X(t+3), X(t+2), and X(t+1).

A scrambler lock between the transmitter and receiver occurs each time an X_X command is sent. An X_X command is initiated only at the beginning of a cell transfer after the PRNG has cycled through all of its states (2^{10} - 1 = 1023 states). The first valid ATM data cell transmitted after power on will also be accompanied with an X_X command byte. Each time an X_X command byte is sent, the first nibble after the last escape (X) nibble is XOR'd with 1111b (PRNG = 3FFx).

Because a timing marker command (X_8) may occur at any time, the possibility of a reset PRNG start-of-cell command and a timing marker command occurring consecutively does exist (e.g. X_X_X_8). In this case, the detection of the last two consecutive escape (X) nibbles will cause the PRNG to reset to its initial 3FFx state. Therefore, the PRNG is clocked only after the first nibble of the second consecutive escape pair.

Once the data nibbles have been scrambled using the PRNG, the nibbles are further encoded using a 4b/5b process. The 4b/5b scheme ensures that an appropriate number of signal transitions occur on the line. A total of seventeen 5-bit symbols are used to represent the sixteen 4-bit data nibbles and the one escape (X) nibble. The table below lists the 4-bit data with their corresponding 5-bit symbols:

Data	Symbol
0000	10101
0100	00111
1000	10010
1100	10111

Data	Symbol
0001	01001
0101	01101
1001	11001
1101	11101

Data	Symbol
0010	01010
0110	01110
1010	11010
1110	11110

Data	Symbol
0011	01011
0111	01111
1011	11011
1111	11111

ESC(X) = 00010

3217 tbl 01

This encode/decode implementation has several very desirable properties. Among them is the fact that the output symbol bits can be represented by a set of relatively simple logic equations. The other main advantage is that it contains transmission properties that are desirable, which include:

- Transition averages over 3 per 5 signal elements;
- Encode/Decode is not affected by the incorporation of the scrambler;
- Run length is limited to <= 5;
- Disparity never exceeds +/- 1.

On the receiver, the decoder determines from the received symbols whether a timing marker command (X_8) or a start-of-cell command was sent (X_X or X_4). If a start-of-cell command is detected, the next 53 bytes received are decoded and forwarded to the descrambler. (See Recv Block Diagram, Figure 2).

The output of the 4b/5b encoder provides serial data to the NRZI encoder. The NRZI code transitions the wire voltage each time a '1' bit is sent. This, together with the previous encoding schemes guarantees that long run lengths of either '0' or '1's are prevented. Each symbol is shifted out with its most significant bit sent first.

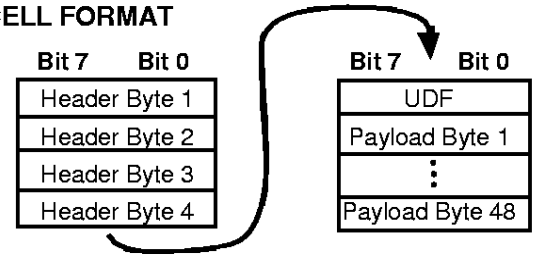
When it has no cells to transmit, the 77V1254 keeps the line active by continuing to transmit valid symbols. But it

does not transmit another start-of-cell command until it has another cell for transmission.

TRANSMIT HEC BYTE CALCULATION/INSERTION

Byte #5 of each ATM cell, the HEC (Header Error Control) is calculated automatically across the first 4 bytes of the cell header, depending upon the setting of bit 5 of registers 0x03, 0x13, 0x23 and 0x33. This byte is then either inserted as a replacement of the fifth byte transferred to the PHY by the external system, or the cell is transmitted as received. A second operating mode provides for insertion of "Bad" HEC codes which may aid in communication diagnostics.

ATM CELL FORMAT



UDF = User Defined Field (or HEC)

RECEIVER DESCRIPTION

On the receiving end, the inverse occurs. The data is NRZI decoded before each symbol is reassembled. The symbols are then sent to the 5b/4b decoder, followed by the Command Byte Interpreter, De-Scrambler, and finally the UTOPIA or DPI interface to the outside world.

Note that although the IDT77V1254 can detect symbol and HEC errors, it does not attempt to correct them.

Upon reset or the re-connect, the IDT77V1254 receiver is typically not symbol-synchronized. Synchronization is established when it receives a command byte, usually the start-of-cell command preceding the first received cell.

The IDT77V1254 monitors line conditions and can provide an interrupt if the line is deemed 'bad'. The interrupt status registers (registers 0x01, 0x11, 0x21 and 0x31) contain a Good Signal Bit (bit 6, set to 0 = Bad signal initially) which shows the status of the line per the following algorithm:

To declare 'Good Signal" (from "Bad" to "Good"):

There is an up-down counter that counts from 7 to 0 and is initially set to 7. When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and no "bad symbol" has been received, the counter decreases by one. However, if at least one "bad symbol" is de-

FUNCTIONAL BLOCK DIAGRAM (Continued)

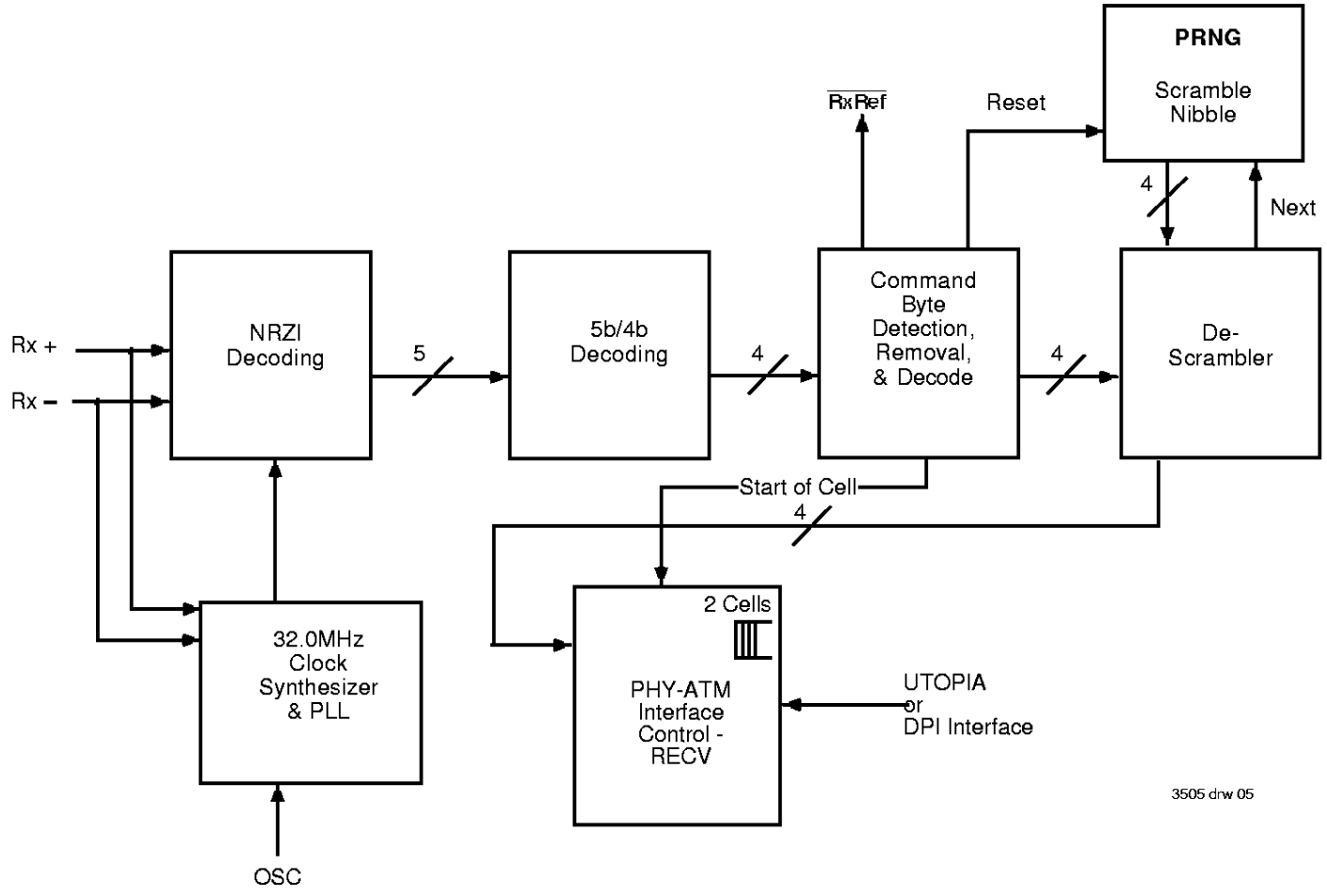


Figure 2. TC Receive Block Diagram

tected during these 1,024 clocks, the counter is increased by one, to a maximum of 7. The Good Signal Bit is set to 1 when this counter reaches 0. The Good Signal Bit could be set to 1 as quickly as 1,433 symbols (204.8 x 7) if no bad symbols have been received.

To declare 'Bad Signal' (from "Good" to "Bad"):

The same up-down counter counts from 0 to 7 (being at 0 to provide a "Good" status). When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and there is at least one "bad symbol", the counter increases by one. If it detects all "good symbols" and no "bad symbols" in the next time period, the counter decreases by one. The "Bad Signal" is declared when the counter reaches 7. The Good Signal Bit could be set to 0 as quickly as 1,433 symbols (204.8 x 7) if at least one "bad symbol" is detected in each 204.8 symbols of seven consecutive groups of 204.8 symbols.

PHY-ATM INTERFACE

The 77V1254 PHY offers great flexibility in interfacing to ATM layer devices such as segmentation and reassembly (SAR) and switching chips. MODE[1:0] are used to select the configuration of this interface, as shown in the table below.

MODE[1:0]	PHY-ATM Interface configuration
00	one 16-bit UTOPIA Level 2 port
01	one 8-bit UTOPIA Level 1 port
10	four 4-bit Data Path Interface (DPI) ports

UTOPIA is a Physical Layer to ATM Layer interface standardized by the ATM Forum. It has separate transmit and receive channels and specific handshaking protocols. UTOPIA Level 2 has dedicated address signals for both the transmit and receive directions that allow the ATM layer device to specify which of the four PHY channels it is communicating with. UTOPIA Level 1 does not have address signals. Instead, key handshaking signals are duplicated so that each channel has its own signals. In both versions of UTOPIA, all channels share a single transmit data bus and a single receive data bus for data transfer.

Bit 1 of registers 0x00, 0x10, 0x20 and 0x30 is used to program whether the UTOPIA bus is in cell mode or byte mode.

DPI is a low-pincount Physical Layer to ATM Layer interface. The low-pincount characteristic allows the 77V1254 to incorporate four separate DPI 4-bit ports, one for each of the four serial ports. As with the UTOPIA interfaces, the transmit and receive directions have their own data paths and handshaking.

UTOPIA Level 2 DETAILS

In each direction it has a 16-bit data path with a parity bit. There is optional checking of parity in the transmit direction, as determined by bit 4 in registers 0x00, 0x10, 0x20 and 0x30. The UTOPIA address of each channel is determined by bits 4 to 0 in registers 0x08, 0x18, 0x28 and 0x38. In the receive direction, parity is generated on the 16 bits.

UTOPIA Level 1 DETAILS

UTOPIA Level 1 doesn't use addressing. Instead, it has TxCLAV, $\overline{\text{TxEN}}$, RxCLAV and $\overline{\text{RxEN}}$ signals for each channel. There are just one each of the TxSOC and RxSOC signals, which are shared across all four channels.

DPI DETAILS

The DPI interface is relatively new and worth additional description. The biggest difference between the DPI configurations and the UTOPIA configurations is that each channel has its own DPI interface. Each interface has a 4-bit data path, a clock and a start-of-cell signal, for both the transmit direction and the receive directions. Additionally, there is one master DPI clock input (DPICLK) into the 77V1254 which is used as a source for the DPI clock outputs. DPI is a cell-based transfer scheme, whereas UTOPIA transfers can be either byte- or cell-based.

In the DPI transmit direction (ATM to PHY), the start-of-cell signal is asserted for one clock cycle, one clock prior to the first nibble of the cell. Once the ATM side has begun sending a cell, it is prepared to send the entire cell without interruption. The 77V1254 drives the transmit DPI clock to the ATM device, based on the DPICLK source. It can modulate the clock to modulate the cell transfer as necessary. Specifically, if it cannot accept another nibble, it disables the output clock and does not generate another rising edge until it has room for the nibble.

The DPI protocol is exactly symmetrical in the receive direction, with the 77V1254 driving the data and start-of-cell signals while receiving the DPI clock as an input.

CONTROL AND STATUS INTERFACE

The Control and Status Interface provides the data and control pins needed to set and reset registers within the IDT77V1254 . Registers are used to set desired operating characteristics and functions, and to communicate status to external systems.

The Control and Status Interface is implemented using a multiplexed address and data bus (AD[7:0]) where the register address is latched via the use of an Address Latch Enable.

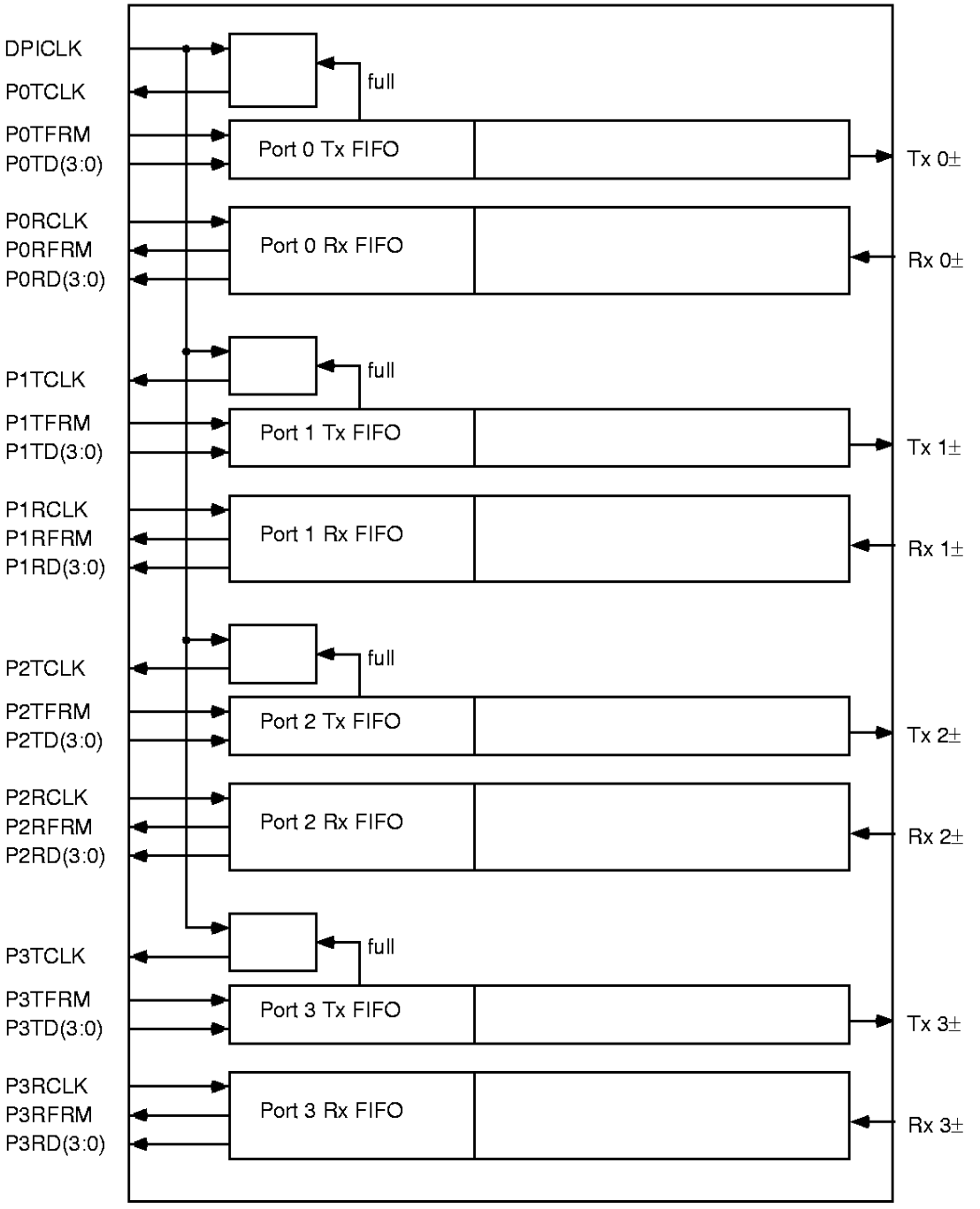
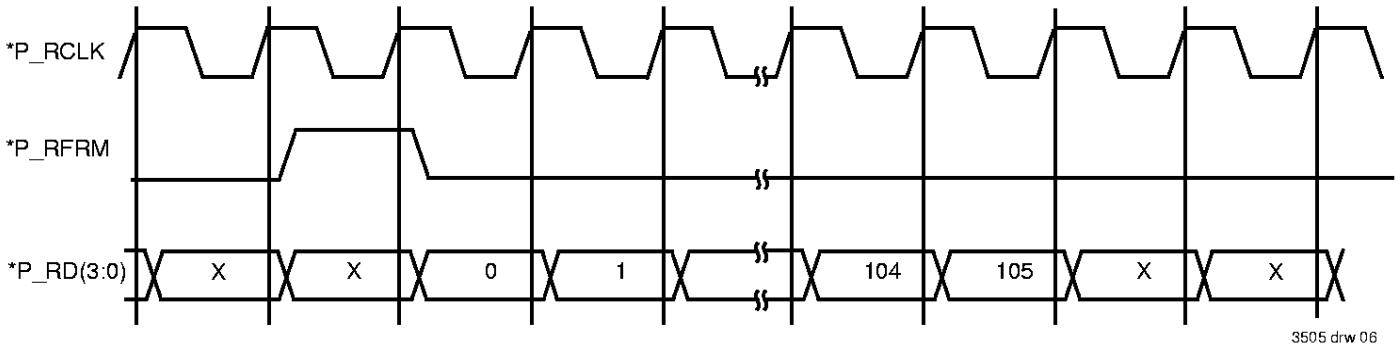
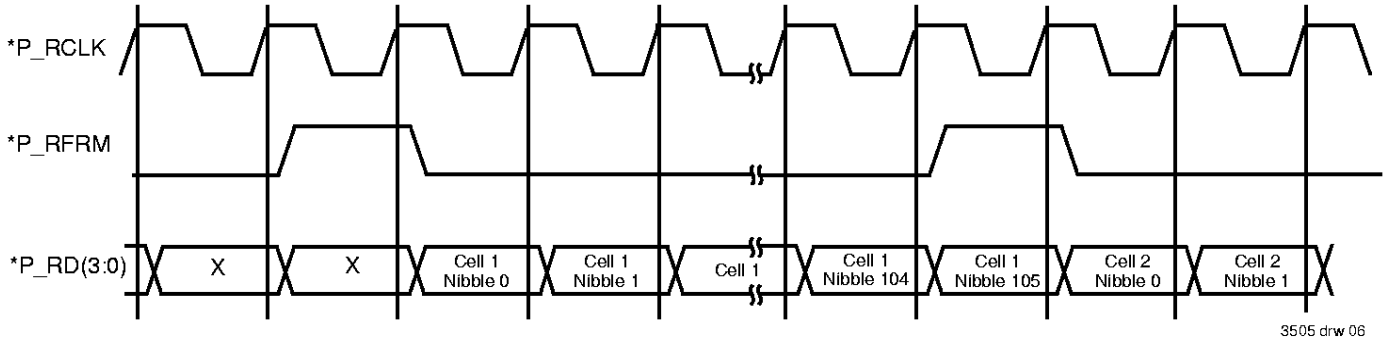


Figure 3. PHY-ATM Interface in DPI Mode



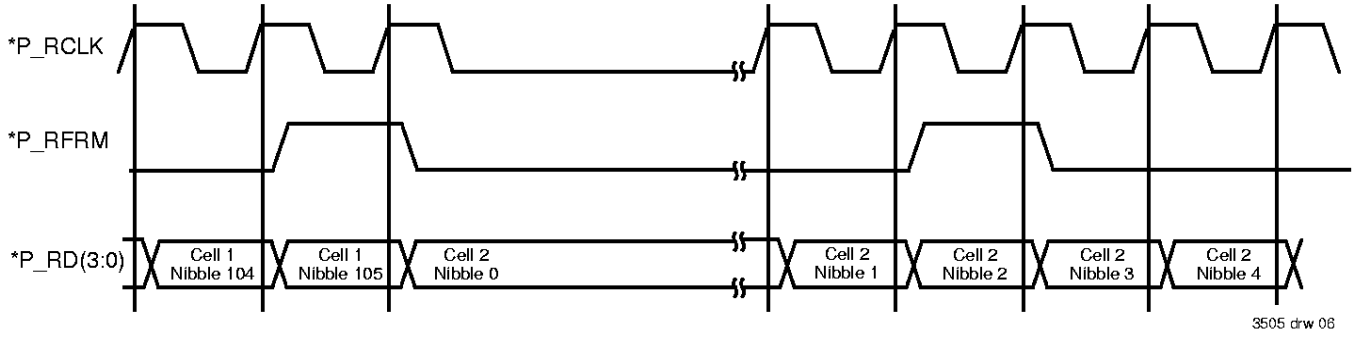
* Note that these signal names are "alternate signal names" rather than the formal pin names.

Figure 4. DPI Receive Handshake - One Cell Received



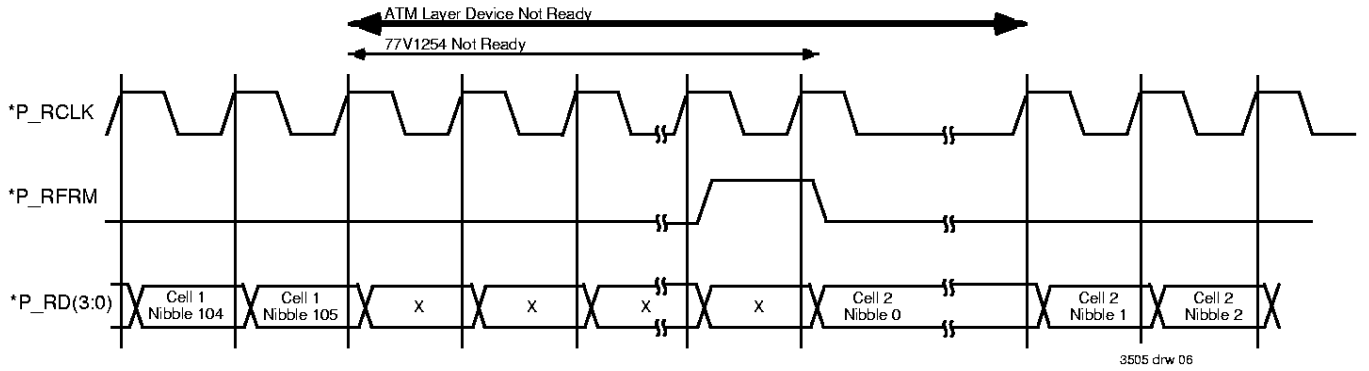
* Note that these signal names are "alternate signal names" rather than the formal pin names.

Figure 5. DPI Receive Handshake - Back-to-Back Cells



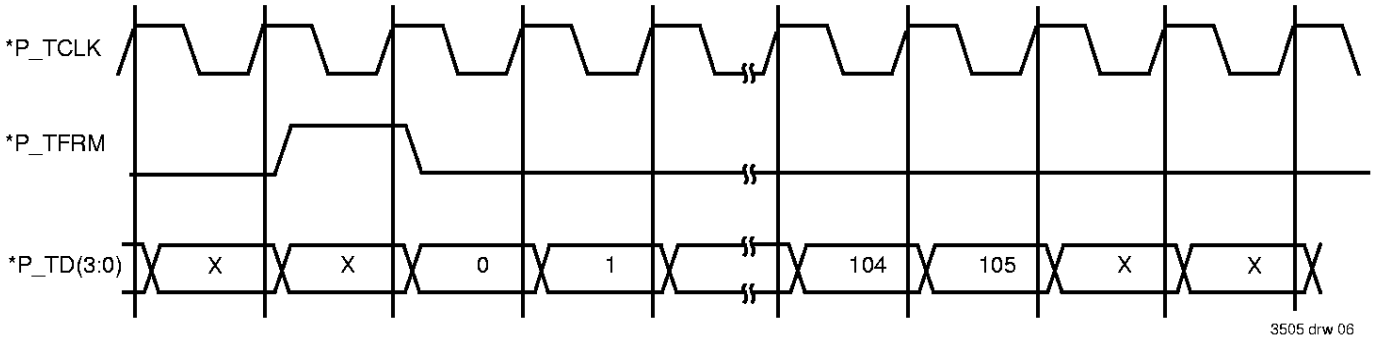
* Note that these signal names are "alternate signal names" rather than the formal pin names.

Figure 6. DPI Receive Handshake - ATM Layer Device Suspends Transfer



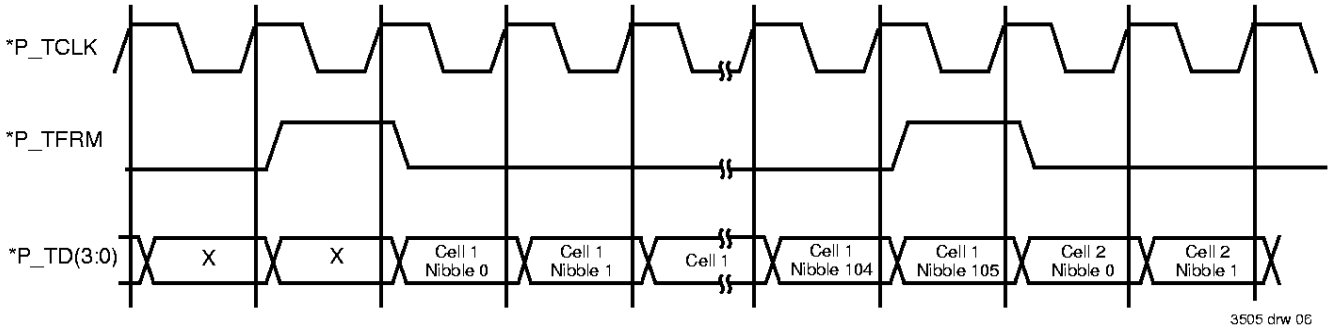
* Note that these signal names are "alternate signal names" rather than the formal pin names.

Figure 7. DPI Receive Handshake - Neither Device Ready



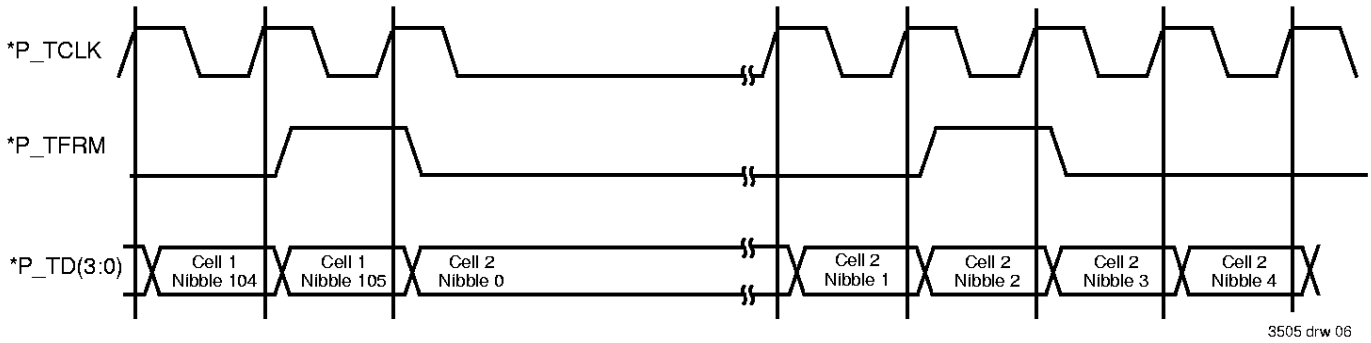
* Note that these signal names are "alternate signal names" rather than the formal pin names.

Figure 8. DPI Transmit Handshake - One Cell for Transmission



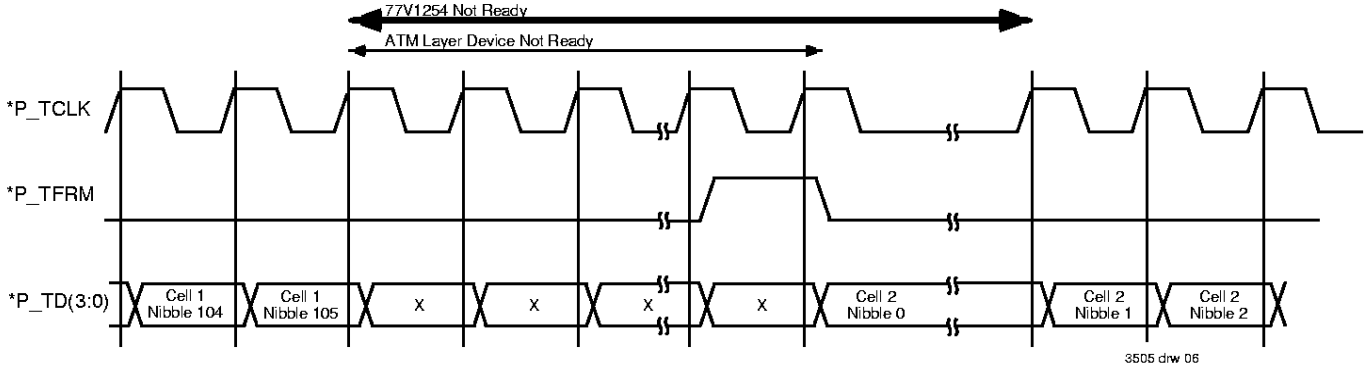
* Note that these signal names are "alternate signal names" rather than the formal pin names.

Figure 9. DPI Tramsnit Handshake - Back-to-Back Cells for Trnsmission



* Note that these signal names are "alternate signal names" rather than the formal pin names.

Figure 10. DPI Transmit Handshake - 77V1254 Transmit FIFO Full



* Note that these signal names are "alternate signal names" rather than the formal pin names.

Figure 11. DPI Transmit Handshake - Neither Device Ready

FUNCTIONAL DESCRIPTION (Continued)

UTILITY BUS

The Utility Bus is a byte-wide interface that provides access to the registers within the IDT77105. These registers are used to select desired operating characteristics and functions, and to communicate status to external systems.

The Utility Bus is implemented using a multiplexed address and data bus (AD[7:0]) where the register address is latched via the Address Latch Enable (ALE) signal.

The Utility Bus interface is comprised of the following pins:

AD[7:0]
ALE
$\overline{CS}$
$\overline{RD}$
$\overline{WR}$

Read Operation

Refer to the Utility Bus waveforms on Figures 19 - 20. A register read is performed as follows:

1. Initial condition:
   - $\overline{RD}$, $\overline{WR}$, $\overline{CS}$ not asserted (logic 1)
   - ALE not asserted (logic 0)
2. Set up register address:
   - place desired register address on AD[7:0]
   - set ALE to logic 1;
   - latch this address by setting ALE to logic 0.
3. Read register data:
   - Remove register address data from AD[7:0]
   - assert $\overline{CS}$ by setting to logic 0;
   - assert $\overline{RD}$ by setting to logic 0
   - wait minimum pulse width time (see AC specifications)

Write Operation

A register write is performed as described below:

1. Initial condition:
   - $\overline{RD}$, $\overline{WR}$, $\overline{CS}$ not asserted (logic 1)
   - ALE not asserted (logic 0)
2. Set up register address:
   - place desired register address on AD[7:0]
   - set ALE to logic 1;
   - latch this address by setting ALE to logic 0.
3. Write data:
   - place data on AD[7:0]
   - assert $\overline{CS}$ by setting to logic 0;
   - assert $\overline{WR}$ (logic 0) for minimum time (according to timing specification); reset $\overline{WR}$ to logic 1 to complete register write cycle.

INTERRUPT OPERATIONS

The IDT77V1254 provides a variety of selectable interrupt and signalling conditions which are useful both during 'normal' operation, and as diagnostic aids. Refer to the Status and Control Register List section.

Overall interrupt control is provided via bit 0 of registers 0x00, 0x10, 0x20 and 0x30. When this bit is cleared (set to 0), interrupt signalling is prevented. Registers 0x07, 0x17, 0x27 and 0x37 allow individual masking of different interrupt sources. Additional interrupt signal control is provided by bit 5 of registers 0x00, 0x10, 0x20 and 0x30. When this bit is set (=1), receive cell errors will be flagged via interrupt signalling and all other interrupt conditions are masked. These errors include:

- Bad receive HEC
- Short (fewer than 53 bytes) cells
- Received cell symbol error

Normal interrupt operations are performed by setting registers 0x00, 0x10, 0x20 and 0x30 bit-0 = 1, and bit-5 = 0. $\overline{INT}$ (pin 85) will go to a low state when an interrupt condition is detected. The external system should then interrogate the 77V1254 to determine which one (or more) conditions caused this flag, and reset the interrupt for further occurrences. This is accomplished by reading registers 0x01, 0x11, 0x21 and 0x31. Decoding the bits in this byte will tell which error condition caused the interrupt. Reading these registers also:

- clears all interrupt status bits
- resets $\overline{INT}$

This leaves the interrupt system ready to signal an alarm for further problems.

LED CONTROL AND SIGNALLING

The LED outputs provide bi-directional LED drive capability of 10mA. As an example, the RxLED outputs aredescribed in the truth table:

STATE	PIN VOLTAGE
Cells being received	Low
Cells not being received	High

As illustrated in the following drawing (Figure 12), this could be connected to provide for a two-LED condition indicator. These could also be different colors to provide simple status indication at a glance. (The value of R is determined to limit LED current to 10mA or less as specified by the LED manufacturer. Minimum value for R should be 270Ω).

TxLED Truth Table

STATE	PIN VOLTAGE
Cells being transmitted	Low
Cells not being transmitted	High

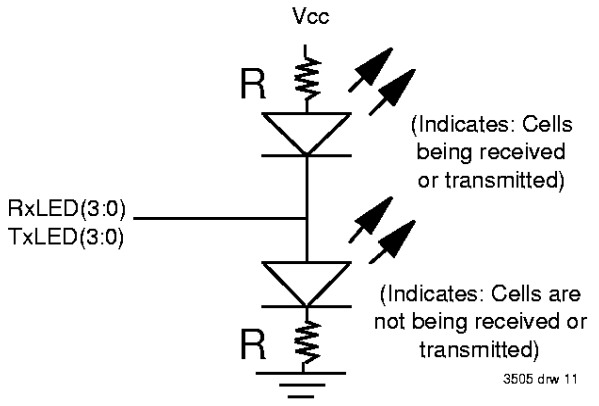


Figure 12.

DIAGNOSTIC FUNCTIONS

1. LOOPBACK

There are two loopback modes supported by the 77V1254. The loopback mode is controlled via bits 1 and 0 of Registers 0x02, 0x12, 0x22 and 0x32:

Bit 1	Bit 0	
0	0	Normal operating mode
1	0	PHY Loopback
1	1	Line Loopback

Normal Mode

This mode, Figure 13, supports normal operating conditions: data to be transmitted is transferred to the TC, where it is queued and formatted for transmission by the PMD. Receive data from the PMD is decoded along with its clock for transfer to the receiving "upstream system".

PHY Loopback

As Figure 14 illustrates below, this loopback mode provides a connection within the PHY between transmit and receive data. Note that while this mode is operating, no data is forwarded to or received from the line interface.

Line Loopback

Figure 15 might also be called “remote loopback” since it provides for a means to test the overall system, including the line. Since this mode will probably be entered under direction from another system (at a remote location), receive data is also decoded and transferred to the upstream system to allow it to listen for commands. A common example would be a command asking the upstream system to direct the TC to leave this loopback state, and resume normal operations.

2. COUNTERS

Several condition counters are provided to assist external systems (e.g. software drivers) in evaluating communications

- 16 bit counter
- counts all received cells

• Receive HEC Error Counter

- 5 bit counter
- counts all received HEC errors

The TxCell and RxCell counters are sized (16 bits) to provide a full cell count (without roll over) if the counter is read once/second. The Symbol Error counter and HEC Error counter were given sufficient size to indicate exact counts for low error-rate conditions. If these counters overflow, a gross condition is occurring, where additional counter resolution does not provide additional diagnostic benefit.

Reading Counters

1. Decide which counter value is desired. Write to registers 0x06, 0x16, 0x26 and 0x36 to the bit location corresponding to the desired counter. This loads the Counter Read registers with the selected counter’s value, and resets this counter to zero.

NOTE: Only one counter (Selected bit in 0x06) may be enabled at any time.

2. Read registers 0x04, 0x14, 0x24 or 0x34 (low byte) and 0x05, 0x15, 0x25 or 0x35 (high byte) to get the value.

Further reads may be accomplished in the same manner by writing to register 0x06.

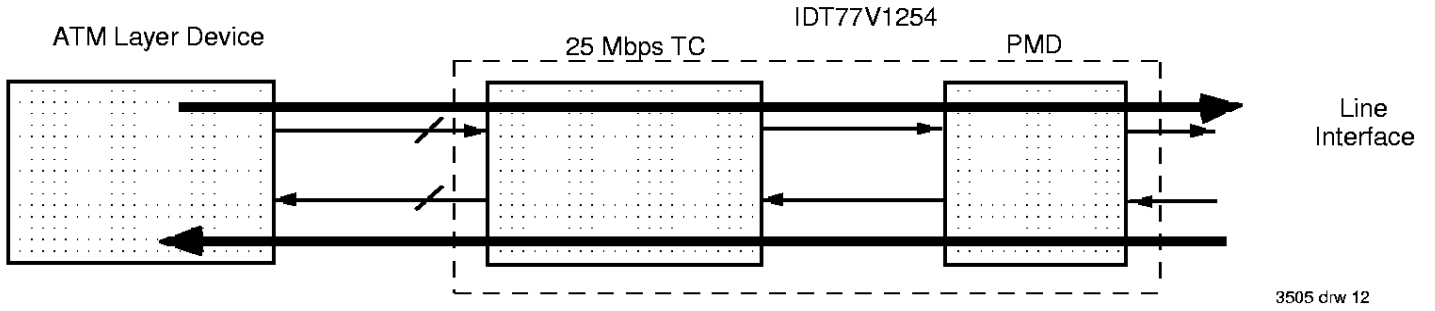


Figure 13. Normal Mode

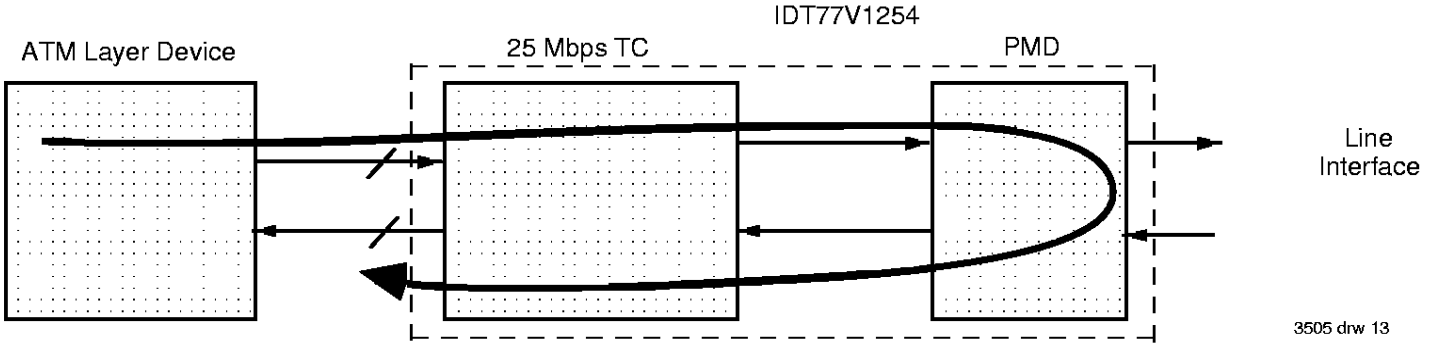


Figure 14. PHY Loopback

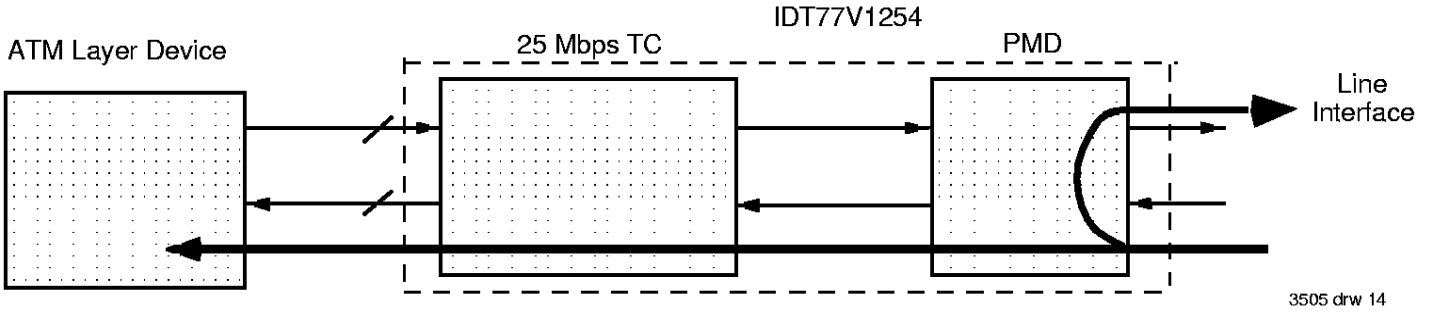


Figure 15. Line Loopback

STATUS AND CONTROL REGISTER LIST

The 77V1254 has 37 registers that are accessible through the microprocessor interface. Each of the four ports has 9 registers dedicated to that port. There is only one register which is not port specific.

Register Name	Register Address				
	Port 0	Port 1	Port 2	Port 3	All Ports
Master Control Registers	0x00	0x10	0x20	0x30	
Interrupt Status Registers	0x01	0x11	0x21	0x31	
Diagnostic Control Registers	0x02	0x12	0x22	0x32	
LED Driver and HEC Status/Control	0x03	0x13	0x23	0x33	
Low Byte Counter Register [7:0]	0x04	0x14	0x24	0x34	
High Byte Counter Register [15:8]	0x05	0x15	0x25	0x35	
Counter Registers Read Select	0x06	0x16	0x26	0x36	
Interrupt Mask Registers	0x07	0x17	0x27	0x37	
Enhanced Control Registers	0x08	0x18	0x28	0x38	
$\overline{\text{RxREF}}$ and $\overline{\text{TxREF}}$ Control Register					0x40

Nomenclature
R/W = register may be read and written via the utility bus;
R-only or W-only = register may be read-only or write-only via the utility bus;
sticky = register bit is cleared after the register containing it is read.
"0" = 'cleared' or 'not set'
"1" = 'set'

MASTER CONTROL REGISTERS

Addresses: 0x00, 0x10, 0x20, 0x30

Master	Type	Initial State	Function
Bit 7	R/W	0 = 25.6 Mbps	**Line Rate Selection** 25.6 Mbps is selected by setting this bit low. 51.2 Mbps is selected by setting this bit high. TxOSC is a 32MHz input for both 25.6 and 51.2 Mbps.
Bit 6	R/W	1 = discard	**Discard Receive Error Cells** On receipt of any cells with an error (e.g. short cell, invalid command mnemonic, receive HEC error (if enabled), the receive FIFO queue will be cleared of this cell, and cell discarded without further intervention from outside the PHY.
Bit 5	R/W	0 = disabled	**Enable Cell Error Interrupts Only** If Bit 0 in this register is set (Interrupts Enabled), setting of this bit enables only "Received Cell Error" to trigger interrupt line.
Bit 4	R/W	0 = disabled	**Transmit Data Parity Check** Directs TC to check parity of TxData[0:7] against parity bit located in TxParity.
Bit 3	R/W	1 = enabled	**Discard Received Idle Cells** Directs TC to discard received idle (VPI/VCI = 0) cells from PMD without signaling external systems.
Bit 2	R/W	0 = disabled	**Halt Tx** Halts transmission of data from TC to PMD and forces both TxD signals low.
Bit 1	R/W	0 = cell mode	**UTOPIA mode select:** 0 = cell mode, 1 = byte mode. Not applicable for DPI mode.
Bit 0	R/W	1 = enabled	**Enable Interrupt Pin (Interrupt Mask Bit)** Enables interrupt output pin. If cleared, pin is always high, and interrupt is masked. If set, an interrupt will be signaled on the interrupt pin (pin 53), by setting its output to "0".

INTERRUPT STATUS REGISTERS

addresses: 0x01, 0x11, 0x21, 0x31

Bit	Type	Initial State	Function
Bit 7		Reserved	
Bit 6	R	0 = Bad Signal	**Good Signal Bit** 1 = Good Signal 0 = Bad Signal
Bit 5	sticky	0	**HEC error cell received**
Bit 4	sticky	0	**"Short Cell" Received** Interrupt signal which flags received cells with fewer than 53 bytes. This condition is detected by the TC receiving Start-of-Cell command bytes with fewer than 53 bytes between them.
Bit 3	sticky	0	**Transmit Parity Error** If Bit 4 of Register 0x00 is set (Transmit Data Parity Check), this interrupt flags a transmit data parity error condition.
Bit 2	sticky	0	**Receive Signal Condition change** This interrupt is set when the received 'signal' changes either from 'bad to good' or from 'good to bad'.
Bit 1	sticky	0	**Received Cell Symbol Error** Set on receiving a cell with an undefined symbol.
Bit 0	sticky	0	**Receive FIFO Overrun** Interrupt which flags condition where receive FIFO has reached full condition and cannot accept additional data.

DIAGNOSTIC CONTROL REGISTERS

Addresses: 0x02, 0x12, 0x22, 0x32

Bit	Type	Initial State	Function
Bit 7	R/W	0=normal	**Force TxClav deassert.** Used during line loopback mode to prevent upstream system from continuing to send data to 77V1254 .
Bit 6	R/W	0=UTOPIA	**RxClav operation select.** The UTOPIA standard dictates that during cell mode operation, if the receive FIFO no longer has a complete cell available for transfer from PHY, RxClav is deasserted following transfer of the last byte out of the PHY to the upsteam system. With this bit set, early deassertion of this signal will occur at the end of Payload byte 44 (as in octet mode for TxFull). This provides early indication to the upstream system of this impending condition. "Standard UTOPIA RxClav" = 0 "Cell mode = Byte mode" = 1
Bit 5	R/W	1 = tri-state	**Single/Multi-PHY configuration select** 0 = single; 1 = multi. Multi-PHY mode: $\overline{\text{RxEnb}}$ = 1 then tristate RxData, RxPrty, RxSOC
Bit 4	R/W	0=normal	**RFLUSH = clear receive FIFO** This signal is used to tell the TC to flush (clear) all data in the receive FIFO. The TC signals this completion by clearing this bit.
Bit 3	R/W	0=normal	**Insert Transmit payload error** Tells TC to insert cell payload errors in transmitted cells. This can be used to test error detection and recovery systems at destination station, or , under loopback control, the local receiving station. This payoad error is accomplished by flipping bit 0 of the last cell payload byte.
Bit 2	R/W	0=normal	**Insert Transmit HEC Error** Tells TC to insert HEC error in Byte 5 of cell. This can be used to test error detection and recovery systems in down-stream switches, or, under loopback control, the local receiving station. This HEC error is accomplilshed by flipping bit 0 of the HEC byte.
Bit 1,0	R/W	00=normal	**Loopback control** **bit# 1 0** 0 0 Normal mode (receive from network) 1 0 PHY Loopback 1 1 Line Loopback

LED DRIVER AND HEC STATUS/CONTROL REGISTERS

Addresses: 0x03, 0x13, 0x23, 0x33

Bit	Type	Initial State	Function
7		0	Reserved
6	R/W	0 = enabled	**Disable Receive HEC Checking (HEC Enable)** When not set, TC calculates HEC byte on first 4 bytes of received cell, and compares value against 5th byte. When set (= 1), TC does not check HEC byte
5	R/W	0 = enabled	**Disable Xmit HEC Calculate & Replace** Directs TC not to calculate HEC on first 4 bytes of cell queued for transmit and replace the 5th byte with this HEC calculation result.
4,3	R/W	00 = 1 cycle	**$\overline{\text{RxRef}}$ pulse width select** bit # 4 3 0 0 RxRef active for 1 TxOsc cycle 0 1 RxRef active for 2 TxOsc cycles 1 0 RxRef active for 4 TxOsc cycles 1 1 RxRef active for 8 TxOsc cycles
2	R	1 = empty	FIFO Status 1=TxFIFO empty 0=TxFIFO not empty
1	R	0	TxLED Status 1=Cell Received 0=Cell NOT Received
0	R	0	RxLED Status 1=Cell Received 0=Cell NOT Received

LOW BYTE COUNTER REGISTERS [7:0]

Addresses: 0x04, 0x14, 0x24, 0x34

Bit	Type	Initial State	Function
[7:0]	R	0x00	Provides low-byte of counter value selected via registers 0x06, 0x16, 0x26 and 0x36.

HIGH BYTE COUNTER REGISTERS [15:8]

Addresses: 0x05, 0x15, 0x25, 0x35

Bit	Type	Initial State	Function
[7:0]	R	0x00	Provides high-byte of counter value selected via register 0x06, 0x16, 0x26 and 0x36.

COUNTER REGISTERS READ SELECT

NOTE: Only one bit may set at any time for proper operation

Addresses: 0x06, 0x16, 0x26, 0x36

Bit	Type	Initial State	Function
Bit 7	—	—	Reserved
Bit 6	—	—	Reserved
Bit 5	—	—	Reserved
Bit 4	—	—	Reserved
Bit 3	W	0	Symbol Error Counter
Bit 2	W	0	TxCell Counter
Bit 1	W	0	RxCell Counter
Bit 0	W	0	Receive HEC Error Counter

INTERRUPT MASK REGISTERS

Addresses: 0x07, 0x17, 0x27, 0x37

Bit	Type	Initial State	Function
7		0	Reserved
6		0	Reserved
5	R/W	0 = interrupt enabled	HEC Error Cell
4	R/W	0 = interrupt enabled	Short Cell Error
3	R/W	0 = interrupt enabled	Transmit Parity Error
2	R	0 = interrupt enabled	Receive Signal Condition Change
1	R	0 = interrupt enabled	Received Cell Symbol Error
0	R	0 = interrupt enabled	Receive FIFO Overflow

ENHANCED CONTROL REGISTERS

Addresses: 0x08, 0x18, 0x28, 0x38

Bit	Type	Initial State	Function
7	R/W	0 = not reset	Individual Port Software Reset 1 = Reset. This bit is not self clearing; must write 0 to exit reset.
6	R/W	0 = TxOSC	Transmit Line Clock When set to 0, the TxOSC input is used as the transmit line clock. When set to 1, the recovered receive clock is used as the transmit line clock.
5		0	Reserved
4-0	R/W	Port 0 (Reg 0x08): 00000 Port 1 (Reg 0x18): 00001 Port 2 (Reg 0x28): 00010 Port 3 (Reg 0x38): 00011	Port Address When operating in Utopia 2 Mode, these register bits determine the Utopia 2 port addresses.

$\overline{\text{RXREF}}$ AND $\overline{\text{TXREF}}$ CONTROL REGISTER

Address: 0x40

Bit	Type	Initial State	Function
7, 6	R/W	00 = RxREF0 (Port 0)	RxREF Source Select Selects which of the four ports (0 to 3) is the source of RxREF.
5	R/W	0 = not reset	Master Software Reset 1 = Reset. This bit is not self clearing; must write 0 to exit reset.
4		0	Reserved
3-0	R/W	0000 = not looped	$\overline{\text{RxREF}}$ to $\overline{\text{TxREF}}$ Loop Select When set to 0, TxREF is used to generate X_8 timing marker commands. When set to 1, TxREF input is ignored, and received X_8 timing commands are looped back and added to the transmit stream of that same port. See Figure xx. bit 3: port 3 bit 2: port 2 bit 1: port 1 bit 0: port 0

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with respect to GND	–0.5 to +7.0	V
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 3139 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Type	Max.	Unit
VDD	Digital Supply Voltage	3.0	3.3	3.6	V
GND	Digital Ground Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	5.25	V
VIL	Input Low Voltage	—	—	0.8	V
AVDD	Analog Supply Voltage	3.0	3.3	3.6	V
AGND	Analog Ground Voltage	0	0	0	V

NOTES:
(1) Relative to AGND.
(2) Relative to Vcc. This condidtion must be met at all times, including the power-on phase.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND, AGND	VDD, AVDD
Commercial	0°C to 70°C	0V	3.3V± 0.3V
Industrial	-40°C to +85°C	0V	3.3V± 0.3V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Max	Unit
ILI(1)	Input Leakage Current (any input)	–1	1	µA
ILO(2)	I/O and Output Leakage Current	–10	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	0.4	V
IDD1(3)	Active Power Supply Current	—	300	mA

NOTES:

1. Measurements with 0.4 ≤ VIN ≤ VDD.
2. $\overline{OE}$ ≥ VIH, 0.4 ≤ VOUT ≤ VDD.
3. Tested at f = 32MHz with outputs unloaded.

Output Parameters for Transmit Line Signal

Symbol	Parameter	Min.	Typ.	Max	Unit
Voh	Output High Voltage for Transmit Line Signal, Ioh = –2 mA	VDD - 0.8V	—	—	V
Vol	Output Low Voltage for Transmit Line Signal, Iol = 8 mA	—	—	0.5	V
Ioh	Output High Current for Transmit Line Signal	—	80	—	mA
Iol	Output Low Current for Transmit Line Signal	—	75	—	mA
ZOUT	Output Impedance	—	20	—	Ohm

Input Parameters for Receive Line Signal

Symbol	Parameter	Min.	Typ.	Max	Unit
ILI	Input Leakage Current(1)	–1	—	1	µA
CIN	Input Capacitance(2)	—	—	10	pF

NOTES:
1. Input Voltage = 2.5V (typ) ± 600mV
2. Measued with f=1MHz.

CAPACITANCE (TA = +25°C, f = 1MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}[1]	Input Capacitance	VIN = 0V	10	pF
C_{OUT}[1]	Output Capacitance	VOUT = 0V	10	pF

NOTES:
1. Characterized values, not currently tested.

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LED OUTPUT

LED outputs are able to source and sink current, to enable driving two-color LEDs. The Tx and Rx LEDs are driven according to the following table:

	State	Pin Voltage
RxLED	Cells being received Cells not being received	Low High
TxLED	Cells being transmitted Cells not being transmitted	Low High

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 15

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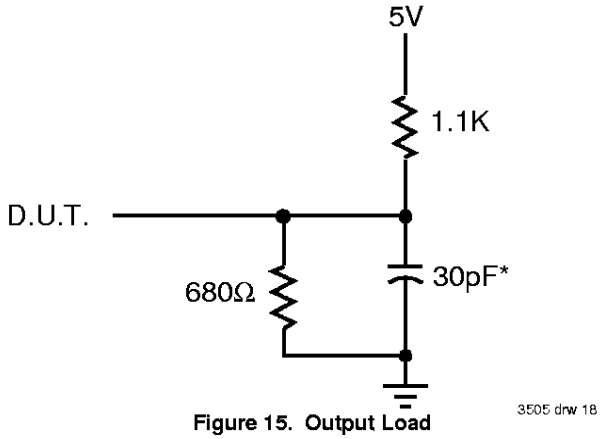


Figure 15. Output Load

* Includes jig and scope capacitances.

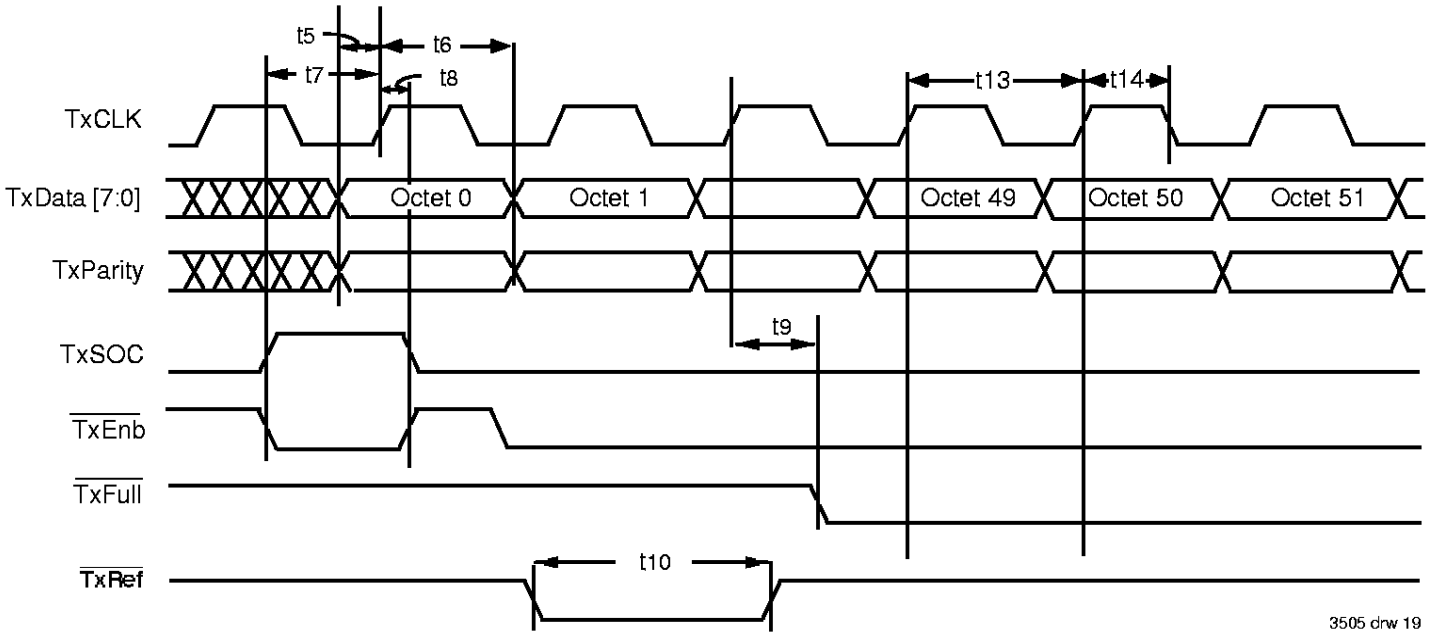


Figure 16. UTOPIA Transmit

UTOPIA Bus Timing Parameters

Symbol	Parameter	Min.	Max.	Units
t1	$\overline{\text{RxEnb}}$ set up time to RxCLK	10	—	ns
t2	$\overline{\text{RxEnb}}$ hold time from RxCLK	2	—	ns
t3	tPD from RxCLK to RxSOC, RxData, and $\overline{\text{RxRef}}$	3	10	ns
t4	$\overline{\text{RxEmpty}}$ delay from RxCLK	1	20	ns
t5	TxData[7:0], TxParity setup time to TxCLK	10	—	ns
t6	TxData[7:0], TxParity hold time from TXCLK	2	—	ns
t7	TxSOC, $\overline{\text{TxEnb}}$ setup time to TxCLK	10	—	ns
t8	TxSOC, $\overline{\text{TxEnb}}$ hold time from TxCLK	2	—	ns
t9	$\overline{\text{TxFull}}$ delay from TxCLK	1	20	ns
t10	$\overline{\text{TxRef}}$ pulse width	TxCLK Period + 5 ns	—	ns
t11	RxCLK period	30	400	ns
$\overline{\text{t12}}$	RxCLK duty cycle (% of t11)	40	60	%
t13	TxCLK period	30	400	ns
t14	TxCLK duty cycle (% of t13)	40	60	%
t15	RxCLK to RxData [7:0], RxParity, and RxSOC high impedance	2	12	ns

NOTES:
The speed rate for the UTOPIA bus ranges from 10MHz to 32MHz based on a 32MHz line clock.

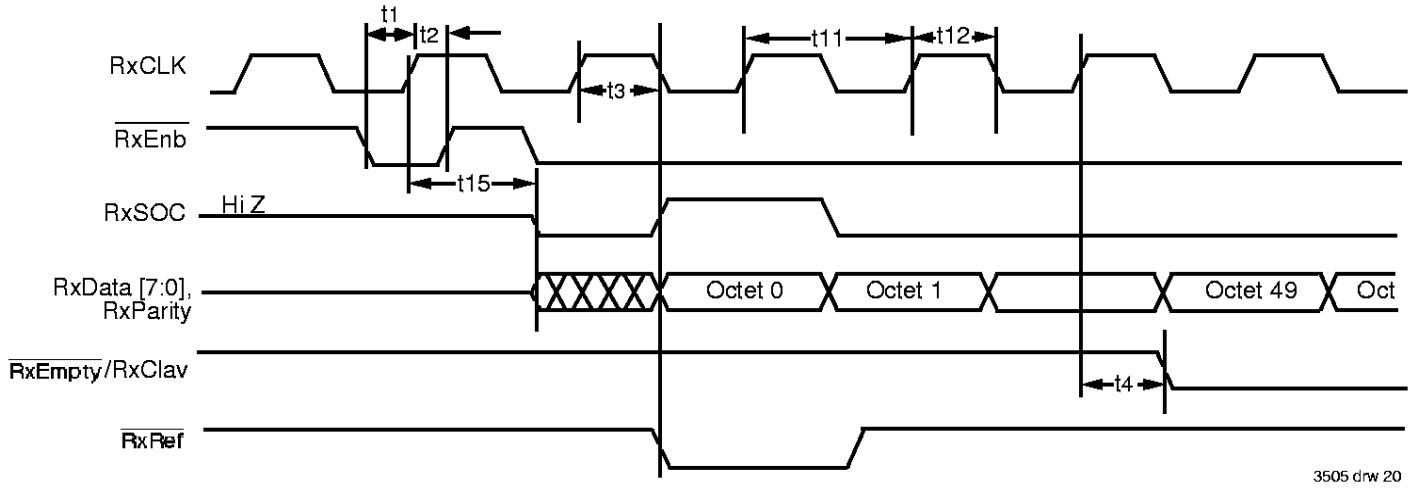


Figure 17. UTOPIA Receive

Reset Timing

Symbol	Parameter	Min.	Max.
Trpw(1)	Minimum $\overline{\text{Reset}}$ pulse width	2 * TxCLK period 2 8 RxCLK period	— —

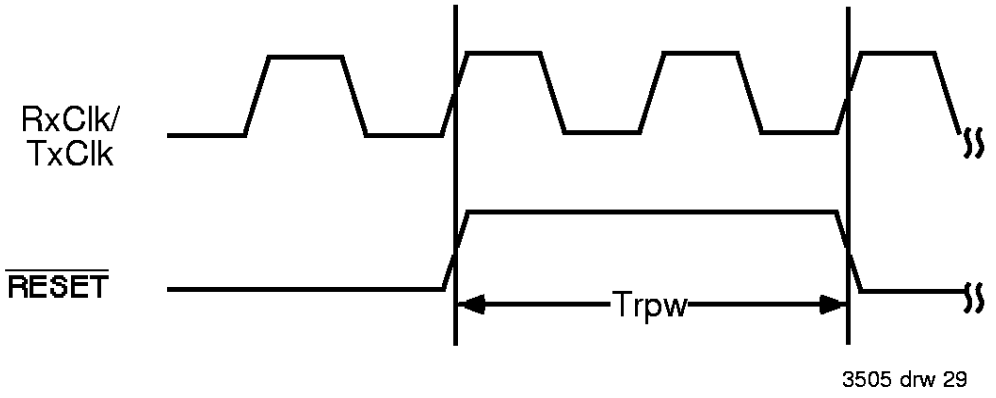


Figure 18. Reset Timing

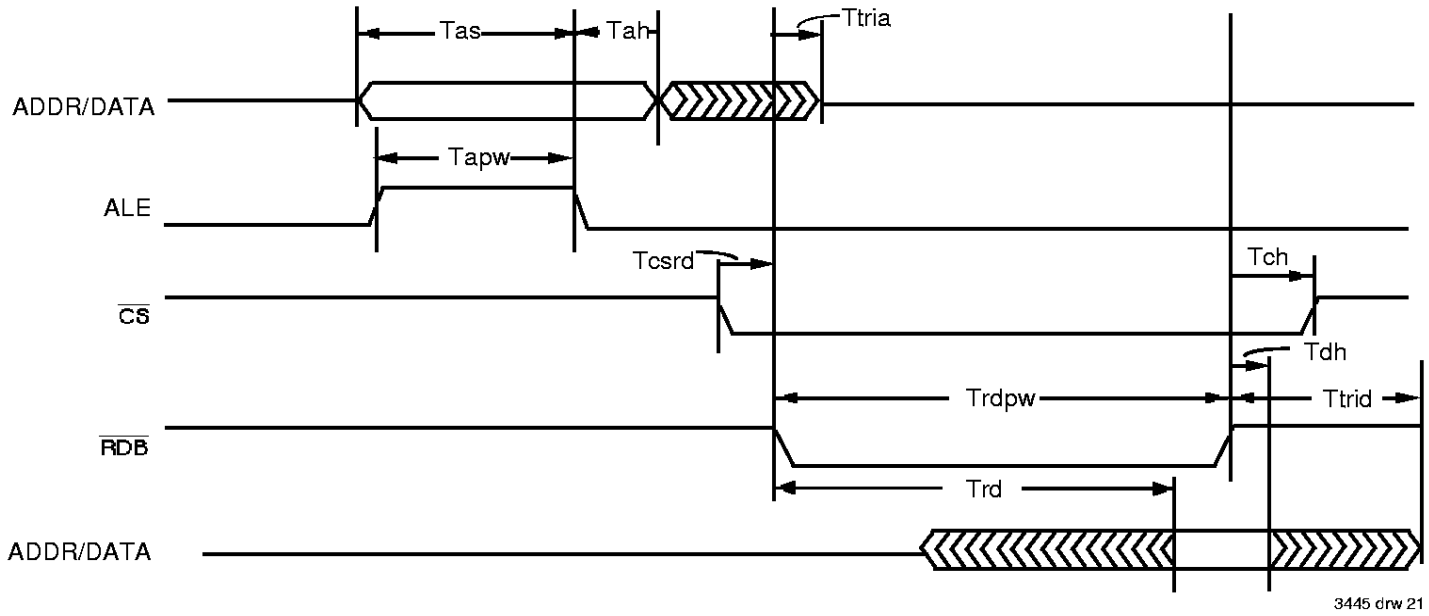


Figure 19. Utility Bus Read Cycle

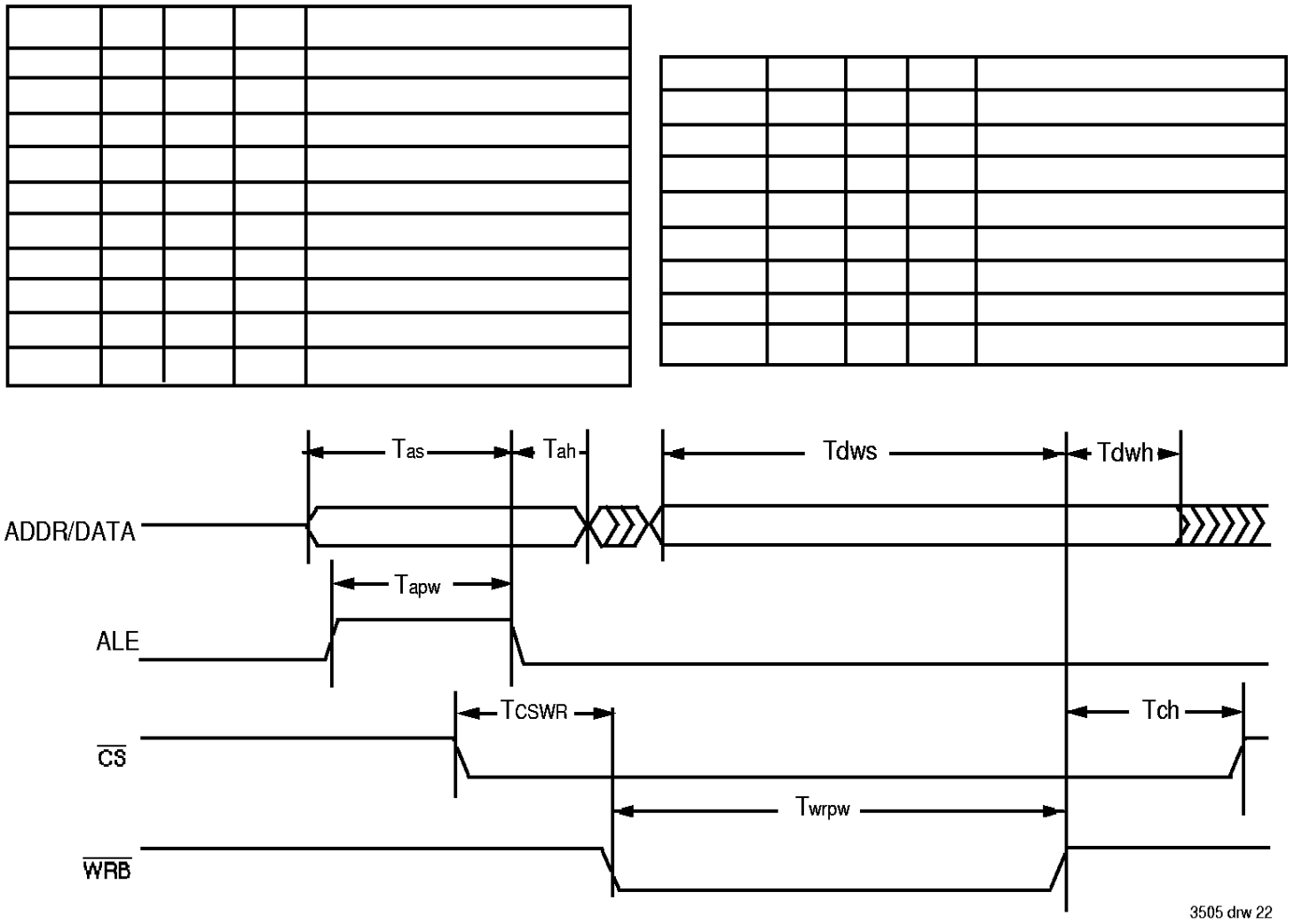
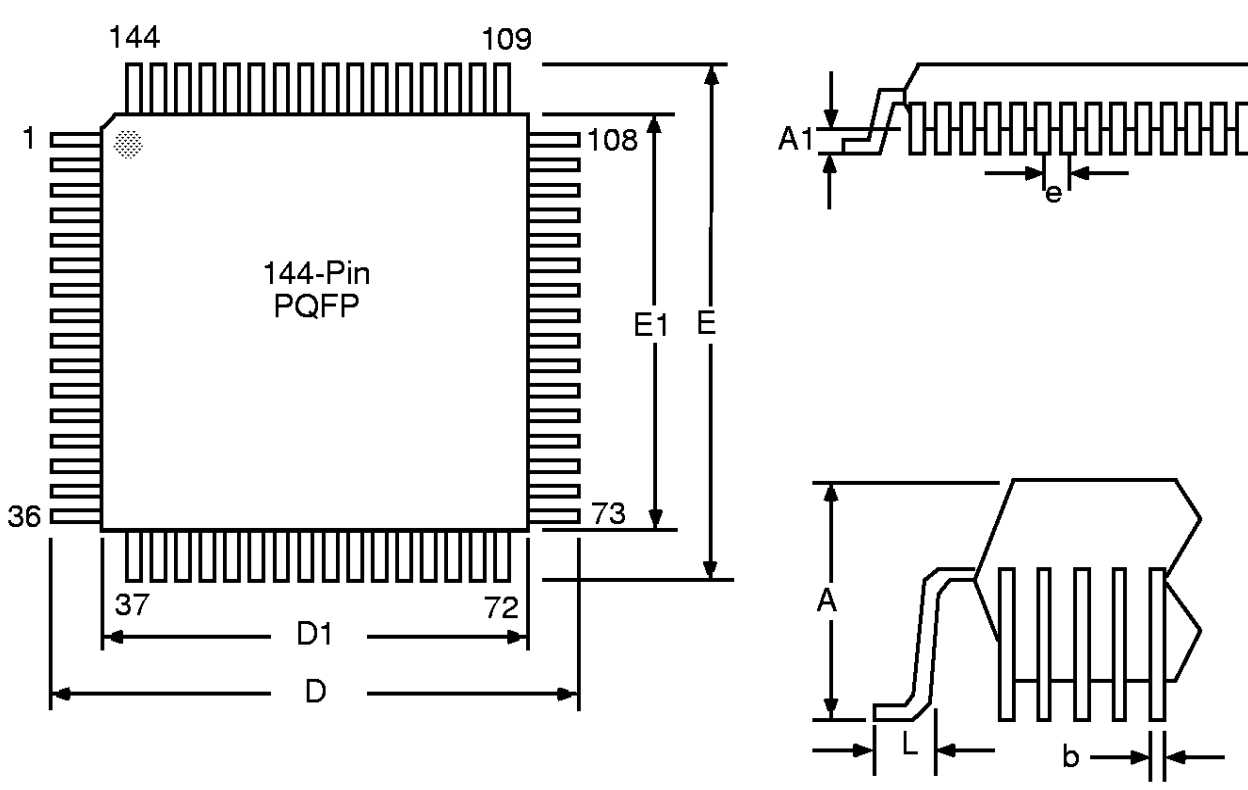


Figure 20. Utility Bus Write Cycle

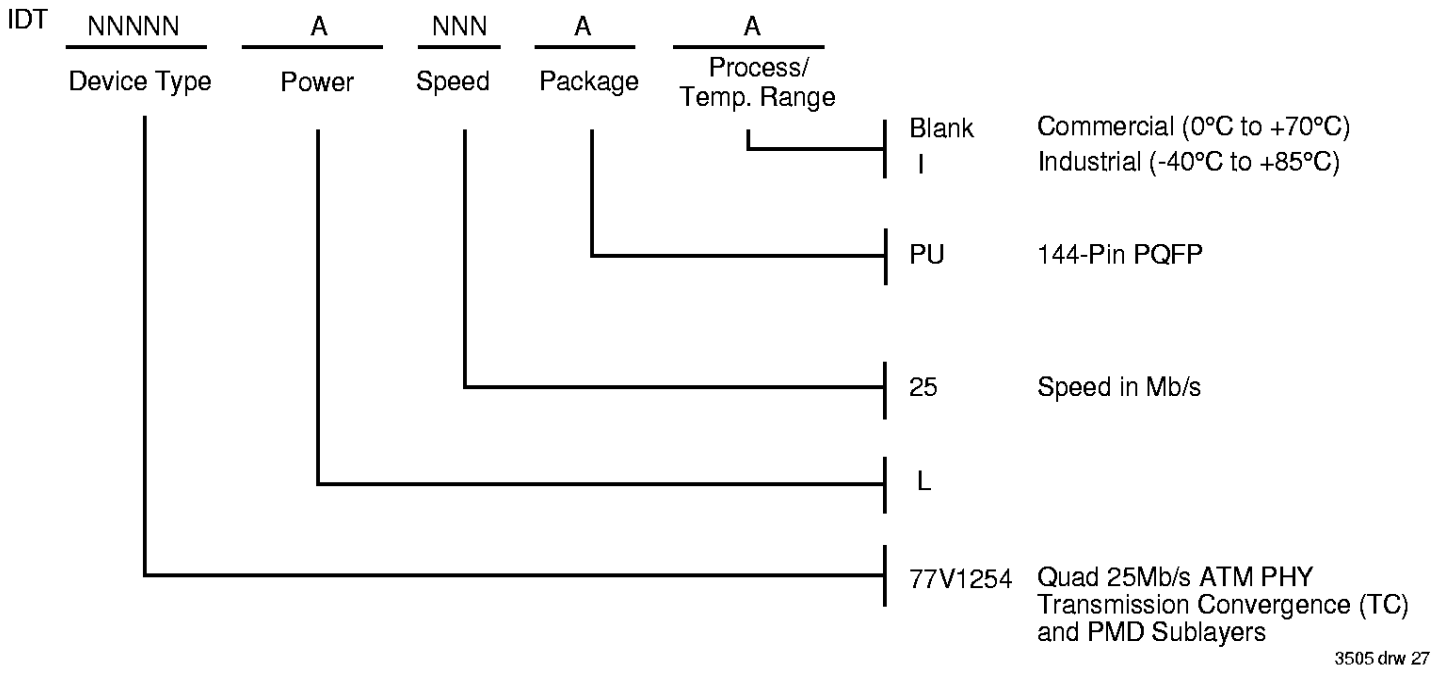
PACKAGE DIMENSIONS



SYMBOL	MIN.	NOM.	MAX.
A	-	3.70	4.07
A1	0.25	0.33	-
A2	3.20	3.37	3.60
D	-	31.20	-
D1	-	28.00	-
E	-	31.20	-
E1	-	28.00	-
L	0.73	0.88	1.03
e	-	0.65	-
b	0.22	-	0.38

Dimensions are in millimeters

ORDERING INFORMATION



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ADVANCE INFORMATION DATASHEET: DEFINITION

"ADVANCE INFORMATION" datasheets contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

Datasheet Document History

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