

74LS266 Gate

Quad 2-Input Exclusive-NOR Gate (Open Collector)
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS266	18ns	8mA

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level.
L = LOW voltage level

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS266N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

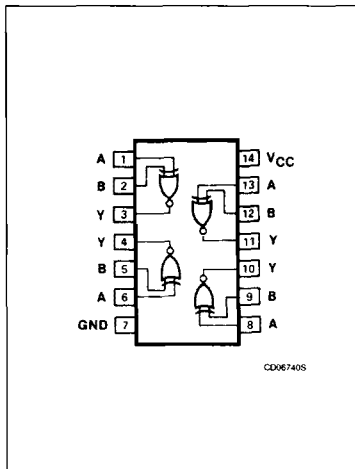
PINS	DESCRIPTION	74LS
A, B	Inputs	2LSul
Y	Output	10LSul

NOTE:

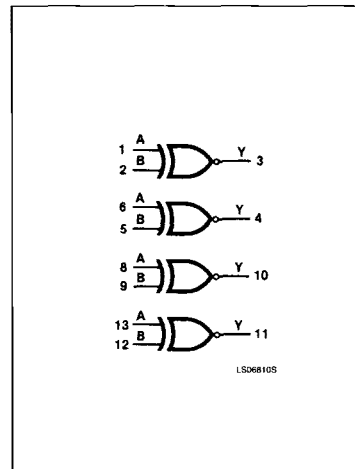
A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

5

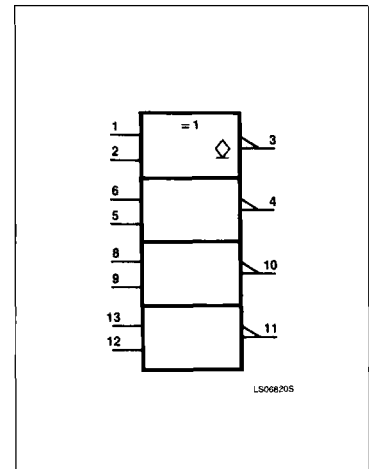
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Gate

74LS266

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	HIGH-level output voltage			5.5	V
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹		74LS266			UNIT
				Min	Typ ²	Max	
I_{OH}	HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5V$				100	μA
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$		0.35	0.5	V
			$I_{OL} = 4mA$		0.25	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-1.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$				0.2	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$				40	μA
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4V$				-0.8	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$			8	13	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_A = 25^\circ C$.
- I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with one input of each gate at 4.5V, the other inputs grounded and the outputs open.

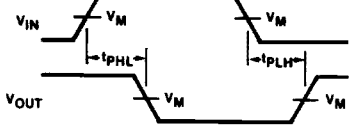
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS		74LS		UNIT
				$C_L = 15pF, R_L = 2k\Omega$		
				Min	Max	
t_{PLH}	Propagation delay	Waveform 1, other input LOW	30	30	ns	
t_{PHL}	A or B to output					
t_{PLH}	Propagation delay	Waveform 2, other input HIGH	30	30	ns	
t_{PHL}	A or B to output					

Gate

74LS266

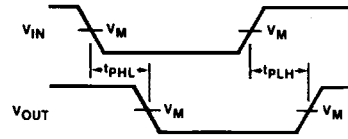
AC WAVEFORMS



WF07570S

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 1. Waveform For Inverting Outputs

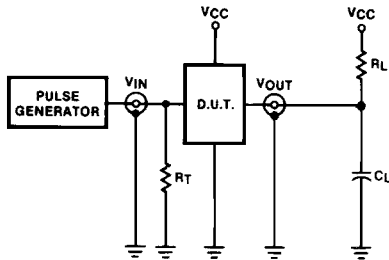


WF07580S

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

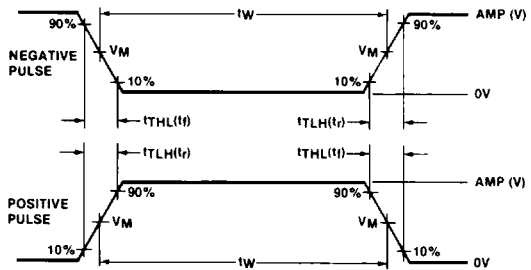
Waveform 2. Waveform For Non-Inverting Outputs

TEST CIRCUITS AND WAVEFORMS



TC02830S

Test Circuit For 74 Open Collector Outputs



WF06450S

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns