M-88L70
3V DTMF Receiver

Features
- Operates between 2.7 and 3.6 volts
- Low power consumption
- Power-down mode
- Inhibit mode
- Central office quality and performance
- Inexpensive 3.58 MHz time base
- Adjustable acquisition and release times
- Dial tone suppression
- Functionally compatible with Clare's M-8870

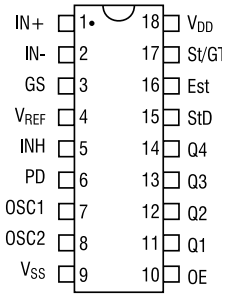
Applications
- Telephone switch equipment
- Mobile radio
- Remote control
- Paging systems
- PCMCIA
- Portable TAD
- Remote data entry

Description
The M-88L70 monolithic DTMF receiver offers small size, low power consumption and high performance, with 3 volt operation. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Ordering Information

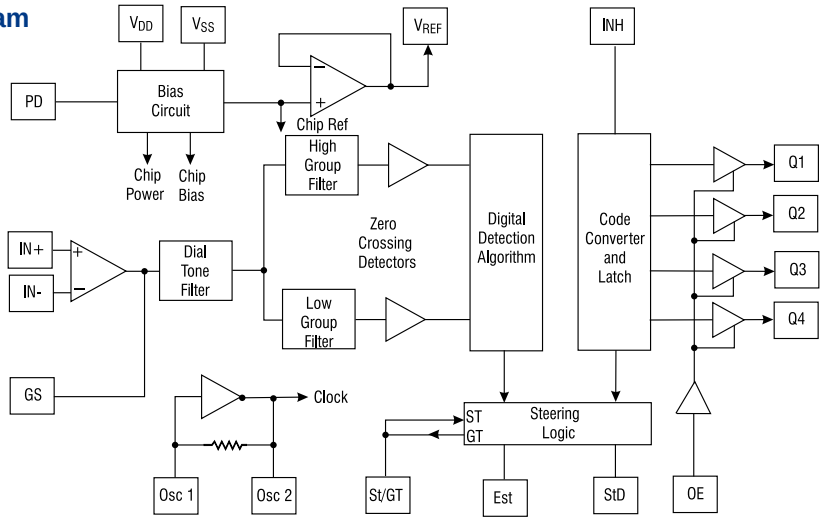
Part #	Description
M-88L70-01P	18-pin plastic DIP
M-88L70-01S	18-pin SOIC
M-88L70-01T	18-pin SOIC, Tape and Reel

Figure 1 Pin Connections



The M-88L70 is a full DTMF Receiver that integrates both bandsplit filter and decoder functions into a single 18-pin DIP or SOIC package. Manufactured using CMOS process technology, the M-88L70 offers low power consumption (18 mW max), precise data handling and 3V operation. Its filter section uses switched capacitor technology for both the high and low group filters and for dial tone rejection. Its decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by provision of an on-chip differential input amplifier, clock generator, and latched tri-state interface bus. Minimal external components required include a low-cost 3.579545 MHz color burst crystal, a timing resistor, and a timing capacitor.

Figure 2 Block Diagram



Filter

The low and high group tones are separated by applying the dual-tone signal to the inputs of two 9th order switched capacitor bandpass filters with bandwidths that correspond to the bands enclosing the low and high group tones. The filter also incorporates notches at 350 and 440 Hz, providing excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section that smoothes the signals prior to limiting. Signal limiting is performed by high-gain comparators provided with hysteresis to prevent detection of unwanted low-level signals and noise. The comparator outputs provide full-rail logic swings at the frequencies of the incoming tones.

Decoder

The M-88L70 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while tolerating small frequency variations. The algorithm ensures an optimum combination of immunity to talkoff and tolerance to interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the Early Steering flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before a decoded tone pair is registered, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (see Figure 3) to rise as the capacitor discharges. Provided that signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), VC reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (see Table 2) into the output latch. At this point, the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropouts) too short to be consid-

Table 1 Pin Functions

Pin	Name	Description	
1	IN+	Non-inverting input	Connections to the front-end differential amplifier
2	IN	-Inverting input	
3	GS	Gain select. Gives access to output of front-end amplifier for connection of feedback resistor.	
4	V_{REF}	Reference voltage output (nominally $V_{DD}/2$). May be used to bias the inputs at mid-rail.	
5	INH	Inhibits detection of tones representing keys A, B, C, and D. This input is internally pulled down.	
6	PD	Power down. Logic high powers down the device and inhibits the oscillator. This input is internally pulled down.	
7	OSC1	Clock input	3.579545 MHz crystal connected between these pins completes internal oscillator.
8	OSC2	Clock output	
9	V_{SS}	Negative power supply (normally connected to 0 V).	
10	OE	Tri-state output enable (input). Logic high enables the outputs Q1 - Q4. Internal pullup.	
11-14	Q1, Q2, Q3, Q4	Tri-state outputs. When enabled by OE, provides the code corresponding to the last valid tone pair received (see Table 5.)	
15	StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below V_{TSt}	
16	ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
17	St/GT	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St. (See Figure 5).	
18	V_{DD}	Positive power supply	

ered a valid pause. This capability, together with the ability to select the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

Where independent selection of receive and pause are not required, the simple steering circuit of Figure 3 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{GTP} @ 0.67\ RC$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 ms would be 300 K ohm. A typical circuit using this steering configuration is shown in Figure 4. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications that place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talkoff and noise immunity. Increasing t_{REC} improves talkoff performance, since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to dropouts would be required. Design information for guard time adjustment is shown in Figure 5.

Input Configuration

The input arrangement of the M-88L70 provides a differential input operational amplifier as well as a bias source (V_{REF}) to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for gain adjustment.

In a single-ended configuration, the input pins are connected as shown in Figure 4 with the op-amp connected for unity gain and V_{REF} biasing the input at $1/2V_{DD}$. Figure 7 shows the differential configuration, which permits gain adjustment with the feedback resistor R5.

Figure 3 Basic Steering Circuit

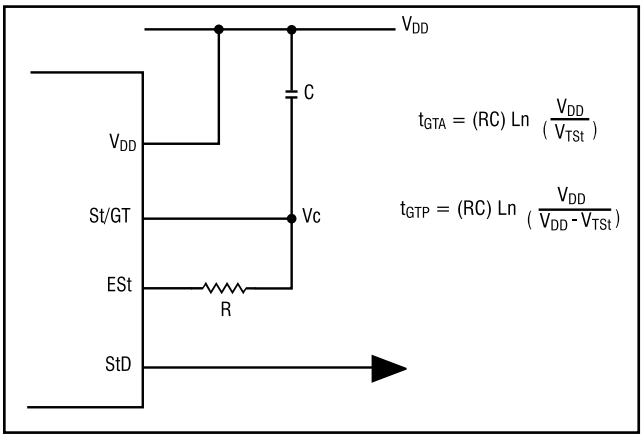


Table 2 Tone Decoding

F_{LOW}	F_{HIGH}	Key (ref.)	OE	INH	ESt	Q4	Q3	Q2	Q1
ANY	ANY	ANY	L	X	H	Z	Z	Z	Z
697	1209	1	H	X	H	0	0	0	1
697	1336	2	H	X	H	0	0	1	0
697	1477	3	H	X	H	0	0	1	1
770	1209	4	H	X	H	0	1	0	0
770	1336	5	H	X	H	0	1	0	1
770	1477	6	H	X	H	0	1	1	0
852	1209	7	H	X	H	0	1	1	1
852	1336	8	H	X	H	1	0	0	0
852	1477	9	H	X	H	1	0	0	1
941	1336	0	H	X	H	1	0	1	0
941	1209	*	H	X	H	1	0	1	1
941	1477	#	H	X	H	1	1	0	0
697	1633	A	H	L	H	1	1	0	1
770	1633	B	H	L	H	1	1	1	0
852	1633	C	H	L	H	1	1	1	1
941	1633	D	H	L	H	0	0	0	0
697	1633	A	H	H	L	Undetected, the output code will remain the same as the previous detected code.			
770	1633	B	H	H	L				
852	1633	C	H	H	L				
941	1633	D	D	H	L				

L = logic low, H = logic high, Z = high impedance, X = don't care

Absolute Maximum Ratings

Parameter	Symbol	Value
Power supply voltage (V_{DD} - V_{SS})	V_{DD}	6.0 V max
Voltage on any pin	V_{dc}	V_{SS} -0.3 Min, V_{DD} +0.3 Max
Current on any pin	I_{DD}	10 mA max
Operating temperature	T_A	-40˚C to + 85˚C
Storage temperature	T_S	-65˚C to + 150˚C

Note:

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and effect its reliability.

Table 4 DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Operating supply voltage	V_{DD}	2.7	3.0	3.6	V	
Operating supply current	I_{DD}	-	3.0	5.0	mA	
Standby supply current	I_{DDS}	-	5.0	10	µA	PD=V_{DD}
Power consumption	P_O	-	9	18	mW	
Low level input voltage	V_{IL}	-v	-	1.0	V	V_{DD} = 3.0 V
High level input voltage	V_{IH}	2	-	-	V	V_{DD} = 3.0 V
Input leakage current	I_{IH}/I_{IL}	-	0.1	-	µA	V_{IN} = V_{SS} or V_{DD} (see Note 2)
Pullup (source) current on OE	I_{SO}	-12	-	-	µA	OE = 0 V
Pull down (sink) Curent PD	I_{PD}	-	1.0	45	µA	PD = 3.0 V
Pull down (sink) Current INH	I_{INH}	-	1.0	45	µA	INH = 3.0 V
Input impedance, signal inputs 1, 2	R_{IN}	-	10	-	MΩ	@ 1 kHz
Steering threshold voltage	V_{TSt}	-	1.5	-	V	
Low level output voltage	V_{OL}	-	0.1	0.4	V	I_{OL} = 1.0 mA
High level output voltage	V_{OH}	2.4	2.6	-	V	I_{OH} = -400 mA
Output high (source) current	I_{OH}	1.0		-	mA	V_{OUT} = 2.5 V @ V_{DD} = 2.7 V
Output voltage V_{REF}	V_{REF}	-	1.5	-	V	No load
Output resistance V_{REF}	R_{OR}	-	10	-	kΩ	

Notes:

1. All voltages referenced to V_{SS} unless otherwise noted. For typical values, V_{DD} = 3.0 V + 20%/-10%, V_{SS} = 0 V, T_A = 25˚C
2. Input pins defined as IN+, IN-, and OE.

Table 5 Operating Characteristics - Gain Setting Amplifier

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Input leakage current	I_N	-	100	-	nA	$V_{SS} < V_{IN} < V_{DD}$
Input resistance	R_{IN}	-	10	-	MΩ	
Input offset voltage	V_{OS}	-	15	25	mV	
Power supply rejection	PSRR	50	60	-	dB	1 kHz
Common mode rejection	CMRR	40	60	-	dB	$-3.0V < V_{IN} < 3.0V$
DC open loop voltage gain	A_{VOL}	32	65	-	dB	
Open loop unity gain bandwidth	f_C	0.3	1.0	-	MHz	
Output voltage swing	V_O	-	2.2	-	V_{P-P}	RL 3 100 kΩ to V_{SS}
Tolerable capacitive load (GS)	C_L	-	-	100	pF	
Tolerable resistive load (GS)	R_L	50	-	-	kΩ	
Common mode range	V_{CM}	-	1.5	-	V_{P-P}	No load

All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 3.0 V +20%/-10%, V_{SS} = 0 V, TA = -40°C to + +85°C

Table 6 AC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Valid input signal levels	-	-36	-	-6.4	dBm	1,2,3,4,5,8
(each tone of composite signal)	-	12.3	-	370	mVRMS	
Positive twist accept	-	-	-	6	dB	
Negative twist accept	-	-	-	6	dB	
Frequency deviation accept limit	-	-	-	1.5% ±2 Hz	Nom.	2,3,5,8,10
Frequency deviation reject limit	-	±3.5%	-	-	Nom.	2,3,5
Third tone tolerance	-	-	-16	-	dB	2,3,4,5,8,9,13,14
Noise tolerance	-	-	-12	-	dB	2,3,4,5,6,8,9
Dial tone tolerance	-	-	+22	-	dB	2,3,4,5,7,8,9
Tone present detection time	t_{DP}	5	8	14	ms	See Figure 8
Tone absent detection time	t_{DA}	0.5	3	8.5	ms	
Minimum tone duration accept	t_{REC}		-	40	ms	User adjustable (see Figures 3 and Figure 5)
Maximum tone duration reject	$t_{\overline{REC}}$	20	-	-	ms	
Minimum interdigit pause accept	t_{ID}	-	-	40	ms	
Maximum interdigit pause reject	t_{DO}	20	-	-	ms	
Propagation delay (St to Q)	t_{PQ}	-	13	-	µs	OE = V_{DD}
Propagation delay (St to StD)	t_{PStD}	-	8	-	µs	
Output data setup (Q to StD)	t_{QStD}	-	3.4	-	µs	
Propagation delay (OE to Q), enable	t_{PTE}	-	200	-	ns	R_L = 10kΩ, CL = 50 pF
Propagation delay (OE to Q), disable	t_{PTD}	-	500	-	ns	
Crystal clock frequency	f_{CLK}	3.5759	3.5795	3.5831	MHz	
Clock output (OSC2), capacitive load	C_{LO}	-	-	30	pF	

All voltages referenced to VSS unless otherwise noted. For typical values V_{DD} = 3.0 V, V_{SS} = 0 V, T_A = -40°C to +85°C, f_{CLK} = 3.579545 MHz. Notes:

1. dBm = decibels above or below a reference power of 1 mW into a 600 Ω load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms. Tone pause = 40 ms.
4. Nominal DTMF frequencies are used, measured at GS.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 kHz) Gaussian noise.
7. The precise dial tone frequencies are (350 and 440 Hz) ± 2%.
8. For an error rate of better than 1 in 10,000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and OE.
12. External voltage source used to bias VREF.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 4. Input DTMF tone level at -28 dBm.

Figure 4 Single-Ended Input Configuration

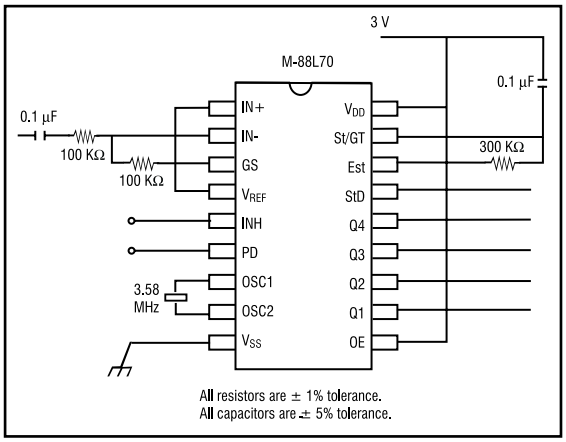


Figure 5 Guard Time Adjustment

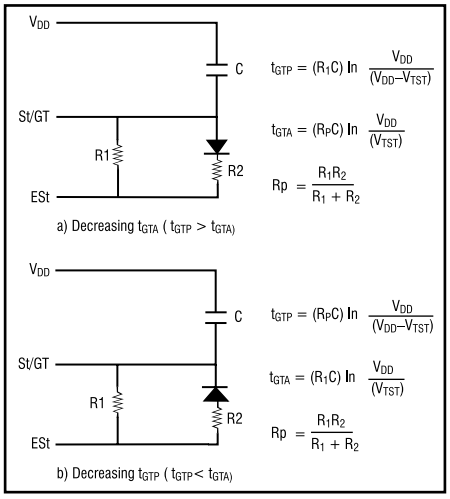
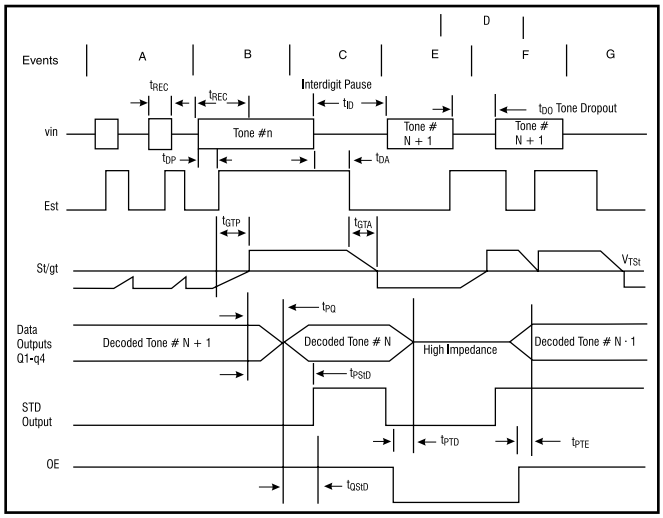


Figure 6 Timing Diagram



Explanation of Events

(A) Tone bursts detected, tone duration invalid, outputs not updated.

(B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.

(C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.

(D) Outputs switched to high impedance state.

(E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).

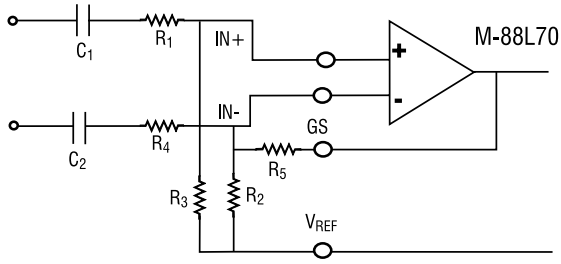
(F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.

(G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

V_{IN}	DTMF composite input signal.
ESt	Early steering output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
Q1 - Q4	4-bit decoded tone output.
StD	Delayed steering output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
OE	Output enable (input). A low level shifts Q1 - Q4 to its high impedance state.
$t_{\overline{REC}}$	Maximum DTMF signal duration not detected as valid.
$t_{\overline{REC}}$	Minimum DTMF signal duration required for valid recognition.
t_{ID}	Minimum time between valid DTMF signals.
t_{DO}	Maximum allowable dropout during valid DTMF signal.
t_{DP}	Time to detect the presence of valid DTMF signals.
t_{DA}	Time to detect the absence of valid DTMF signals.
t_{GTP}	Guard time, tone present.
t_{GTA}	Guard time, tone absent.

Figure 7 Differential Input Configuration



Differential Input Amplifier
$C_1 = C_2 = 10$ nF
$R_1 = R_4 = R_5 = 100$ KΩ
$R_2 = 60$ kΩ, $R_3 = 37.5$ KΩ

$$R_3 = \frac{R_2 R_5}{R_2 + R_5}$$

$$\text{Voltage Gain (Av diff)} = \frac{R_5}{R_1}$$

All resistors are ± 1% tolerance.
All capacitors are ± 5% tolerance.

Input Impedance

$$(Z_{INDIFF}) = 2\sqrt{R_1^2 + \left(\frac{1}{\omega C}\right)^2}$$

Figure 8 Common Crystal Connection

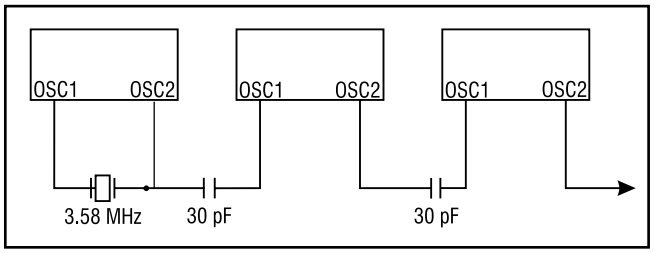
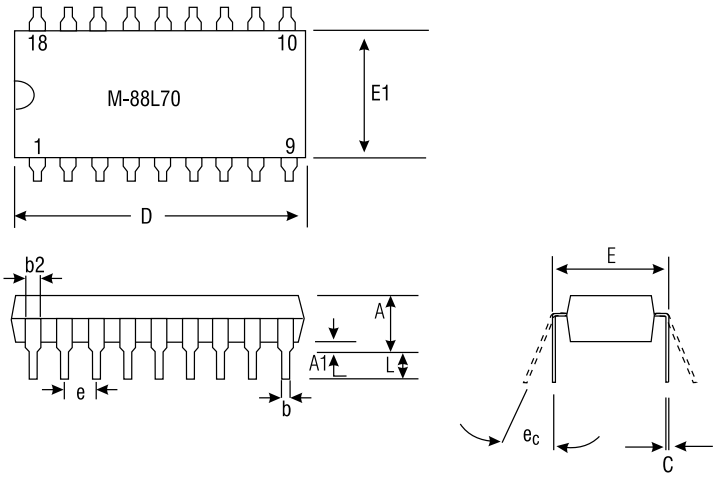


Figure 9 Package Dimensions

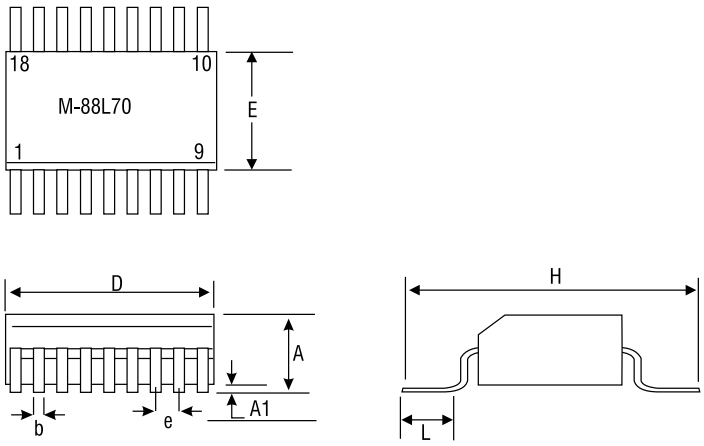
Drawing not to scale.
Does not reflect actual part marking.

18-Pin DIP



Tolerances				
	Inches		Metric (mm)	
	Min	Max	Min	Max
A		.210		5.33
A1	.015		.38	
b	.014	.022	36	.56
b2	.045	.070	1.1	1.7
C	.008	.014	.20	.36
D	.880	.920	23.35	23.37
E	.300	.325	7.62	8.26
E1	.240	.280	6.10	7.11
e	.100 BSC		2.54 BSC	
ec	0°	15°	0°	15°
L	.115	.150	2.92	3.81

18-Pin SOIC



Tolerances				
	Inches		Metric (mm)	
	Min	Max	Min	Max
A	.0926	.1043	2.35	2.65
A1	.0040	.0118	.10	.30
b	.013	.020	.33	.51
D	.4469	.4625	11.35	11.75
E	.2914	.2992	7.4	7.6
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	.40	1.27

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