ICS1532

Document Type: Data Sheet

Product Stage: Preliminary

205 MSPS Triple 8-bit ADCs with Clock Generator for LCD Monitors

General Description

The ICS1532-140,-165 and -205 chips are high-performance, cost-effective, 3-channel, 8-bit analog-to-digital converters with an integrated line-locked clock generator. They are part of a family of chips for high-resolution video applications that use analog inputs, such as LCD monitors, projectors, plasma displays, and HDTVs. Using low-voltage CMOS mixed-signal technology, they are an effective data-capture solution for VGA to UXGA.

The ICS1532 chips offer analog-to-digital data conversion and synchronized pixel-clock generation up to 205 Mega samples per second, (MSPS) or 205 MHz. The Dynamic Phase Adjust (DPA) circuitry allows end-user control over the pixel clock phase, relative to the recovered sync signal and analog pixel data. The ICS1532 provides two 24-bit pixels per clock. An ADCSYNC output pin provides recovered HSYNC in phase with the ADCRCLK output to be used to synchronize horizontal timing.

A clamp signal can be generated internally or provided through the CLAMP pin. An adjustable-gain video amplifier fine tunes the analog signal. The PLL uses an internal programmable feedback divider. Two additional, independent programmable PLLs, each with spread-spectrum functionality, support memory and panel clock requirements.

Features

- 500 ps Maximum pk-pk Jitter @ 205 MHz
- 3-channel 8-bit AtoD conversion up to 205 MHz
- Uses 2.5 and 3.3 VDC
- External Digital Inputs are 5-V tolerant
- Direct Connection to Analog Inputs
- Integrated Video Amplifier with adjustable gain
- Dynamic Phase Adjust (DPA) for software-adjustable analog sample points
- Internal Clamp Circuit and External Clamp Input
- Low-voltage TTL clock outputs, synchronized with digital pixel data outputs
- Two additional PLLs with spread spectrum for memory and panel clock
- Automatic Power-On Reset (POR) detection
- I2C serial interface speeds:100 to 800 kHz
- Lock Detection in both Hardware and Software
- 144-pin LQFP package

Application

- LCD Monitors

Block Diagram

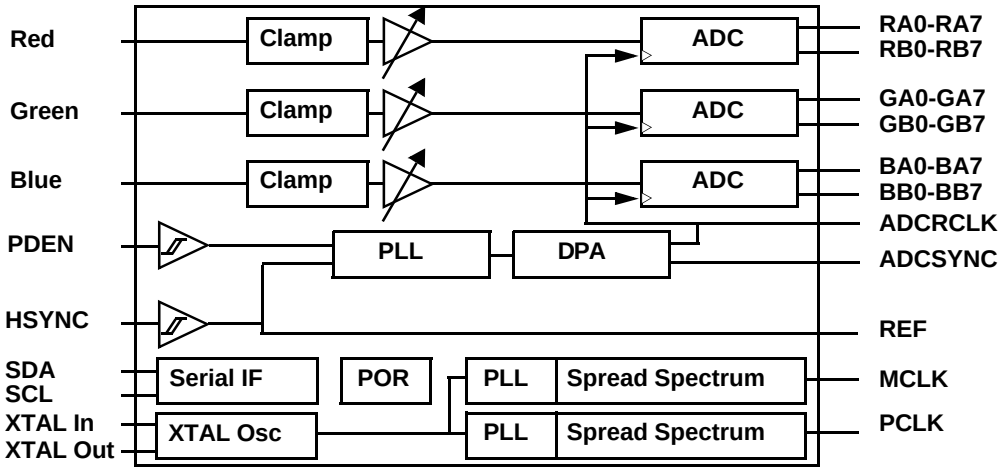


Table of Contents

Related Documents

The following related documents are available on the ICS web site http://www.icst.com

- None at this time

Chapter 1 Summary

1.1 Dynamic Phase Adjust (Positions Pixel Clock on Sub-Pixel Basis)

Table 1-1 lists the number of possible delay element units that can be used to program to add a delay of up to one pixel clock period, in increments of either 16, 32, or 64 (Reg 04, Bits 5:0 and Reg 05, Bits 1:0)

Table 1-1. Increments for Delay Element Units

Number of Delay Element Units	Pixel Clock Range, MHz
16	55 ▬ 260
Reserved	-
32	27 ▬ 130
64	14 ▬ 64

1.2 Automatic Power-On Reset Detection (Automatically Resets ICS1532)

The ICS1532 automatically detects power-on resets. As a result, the ICS1532 resets itself if the supply voltage drops below threshold values. No external connection to a reset signal is required.

1.3 I2C Serial Interface

For registers access, the ICS1532 uses an I2C serial interface operateing between 100 and 400 kHz

The ICS1532 has 5 V-tolerant I2C inputs and can use either of two unique, alternative sets of addresses depending on the input SBADR pin. See Table 1-2. Since I2C is a 7 bit address yet has a Read/Write bit, this can be thought of as either a single 7 bit address, or 2 addresses; an 8 bit read and a different 8 bit write address.,

Table 1-2. ICS1532 Address Sets

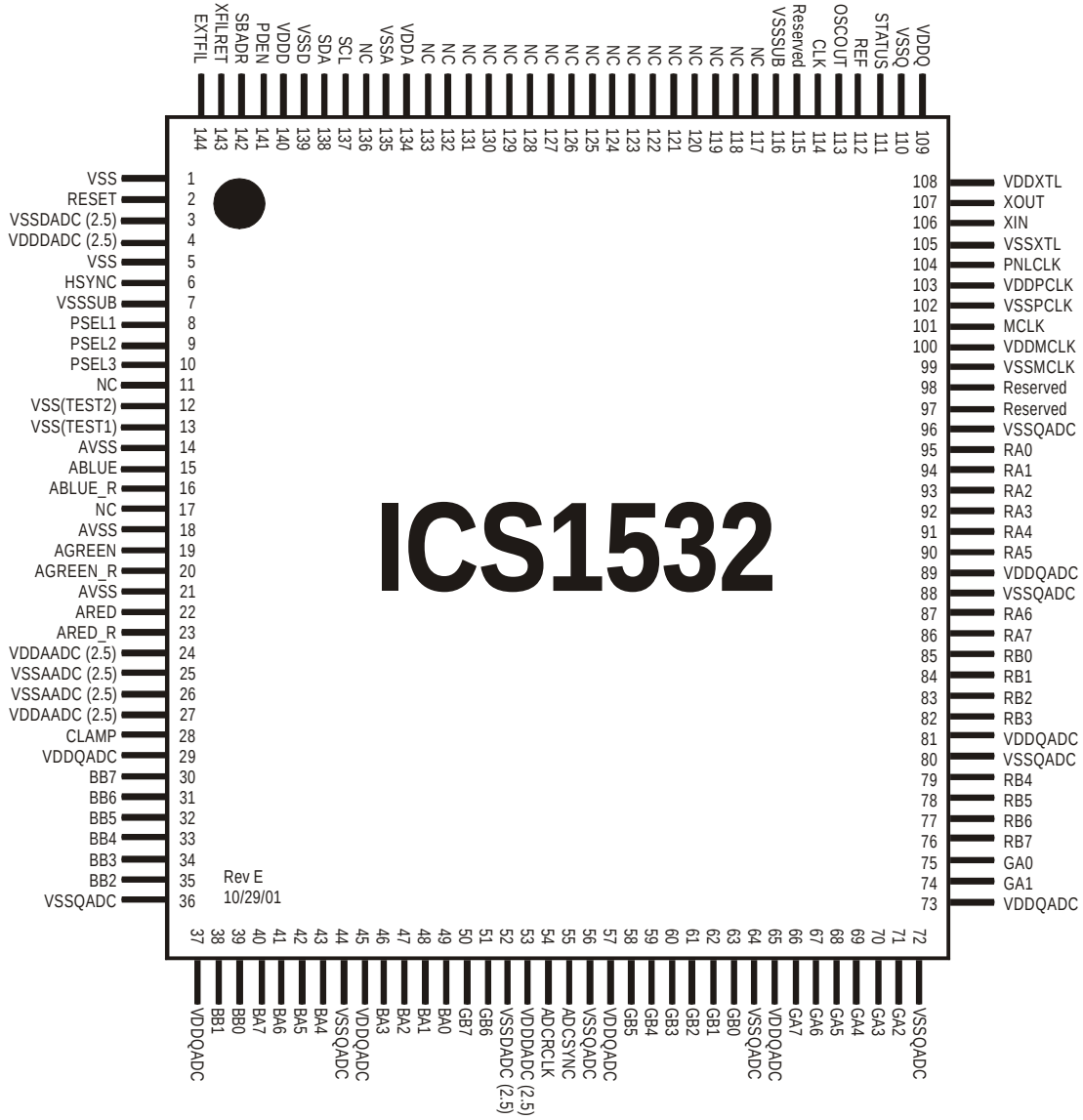
Addresses in Address Set	Address Set 1. (SBADR Pin Is Low)	Address Set 2. (SBADR Pin Is High)
7-bit device address	24h	25h
8-bit read address	49h	4Bh
8-bit write address	48h	4Ah

1.4 Programmable Outputs

For general-purpose outputs, the ICS1532 provides programmable pins PSEL3, PSEL2, and PSEL1 (Reg 37:2-0).

Chapter 2 Pin Diagram and Listings

Figure 2-1. Pin Diagram



2.0.1 Pin Listing by Functional Grouping

2.0.1.1 Clock Pins

For more information on the clock pins, see Figure 3-2 and Figure 3-3.)

Table 2-1. Clock Pins

Pin Name	Pin Type	Pin Description
ADCRCLK	Input or Output	**Analog-to-Digital Converter Reference Clock.** • This pin outputs a half-rate pixel clock for latching digital output pixel data. • Typically, this pin connects to an LCD panel controller/scaler. • In this table, see also CLK.
ADCSYNC	Input or Output	**Analog-to-Digital Converter Sync.** • This pin provides a recovered HSYNC signal (that is, an HSYNC signal conditioned by a Schmitt trigger) that aligns to ADCRCLK. • For some previous ICS chips, the ADCSYNC pin is called FUNC.
CLK	Output	**Clock.** • This pin outputs the full-rate pixel clock for latching digital output pixel data. • In this table, see also ADCRCLK.
HSYNC	Input	**Horizontal Sync.** (See Table 2-4.)
MCLK	Output	**Memory Clock.** • This pin provides an independent user-programmable clock source. • Typically, this pin is used by LCD panel controller/scaler chips or microcontrollers.
OSCOUT	Output	**Oscillator Output.** • The output from this pin is from a crystal oscillator. • The output frequency is one of the following: – The same frequency as the input frequency to the crystal oscillator – The frequency that results when the input frequency is divided by a programmable value
PNLCLK	Output	**Panel Clock.** • This pin provides an independent user-programmable clock source. • Typically, this pin is used by LCD panel controller/scaler chips or microcontrollers.
REF	Output	**Reference.** This pin provides various reference line clock sync signals.
SCL	Input	**Serial Clock.** (See Table 2-5.)
XIN	Input	**Crystal Input.** This pin accepts input from one of the following: • A 14.31818-MHz crystal • An external clock source
XOUT	Output	**Crystal Output.** Do one of the following with this pin: • Connect it to a 14.31818-MHz crystal. • Leave it open for an external clock source.

2.0.1.2 Control Pins

Table 2-2. Control Pins

Pin Name	Pin Type	Pin Description
CLAMP	Input	**Clamp.** This pin accepts an external signal that is provided as an alternative to the ICS1532's internally generated clamp signal.
PSEL1, PSEL2, PSEL3	Output	**Programmable Select 1, 2, 3.** These pins are used as general-purpose programmable output pins.
RESET#	Input	**Reset.** This active low pin is 5-V tolerant. and resets the ICS1532 to an initial known state.
VSS(Test2) VSS(Test1)	Input/ Output	**Ground or Test Outputs** • Normal Mode. These pins must be connected to Ground. • Test Mode. (Reserved)

2.0.1.3 Pixel Data Pins

Table 2-3. Pixel Data Pins

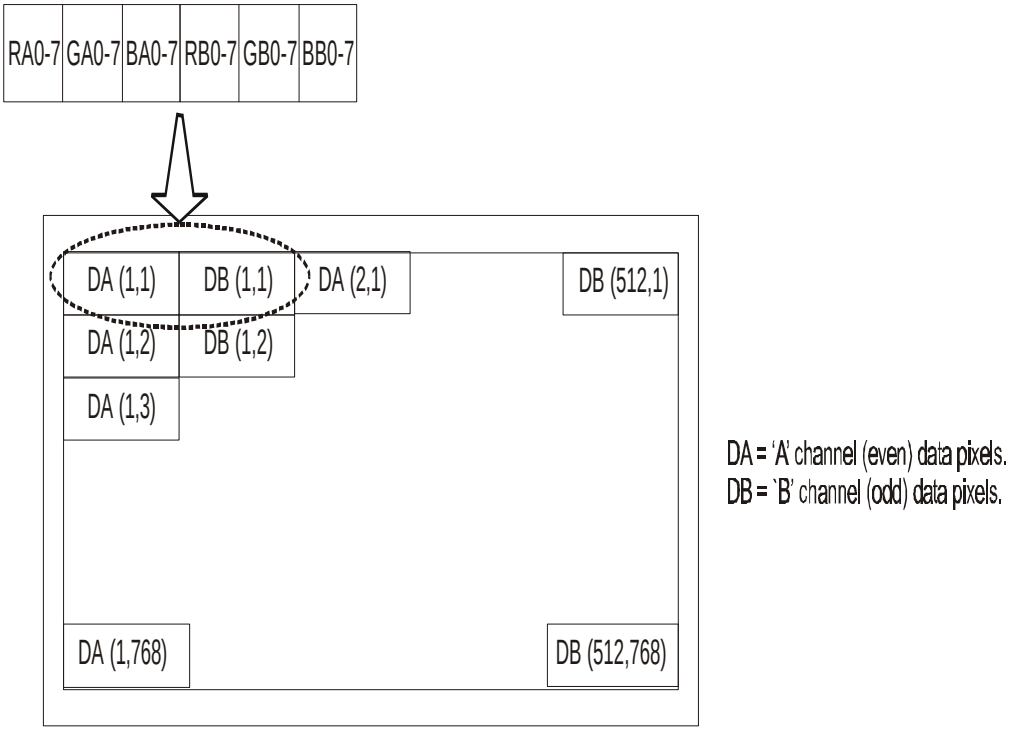
Pin Name	Pin Type	Pin Description
ABLUE, AGREEN, ARED	Input	**Analog Blue, Analog Green, Analog Red.** • These pins accept analog data for the ADC blue, green, and red channels. • Typically, the data for these pins comes from a PC display controller.
ABLUE_R, AGREEN_R, ARED_R	Output	**Analog Blue Return, Analog Green Return, Analog Red Return.** • These pins provide a return path for the input analog data • Typically, these pins are connected to the respective analog signal return pins from a PC display controller.
BA7 – BA0, GA7 – GA0, RA7 – RA0	Output	**Blue ('A channel') A7 – A0, Green ('A channel') A7 – A0, Red ('A channel') A7 – A0.** • These pins output first blue, green, and red pixel data, respectively. • A7 pins reflect most-significant data bits. A0 pins reflect least-significant data bits.
BB7 – BB0, GB7 – GB0, RB7 – RB0	Output	**Blue ('B channel') B7 – B0, Green ('B channel') B7 – B0, Red ('B channel') B7 – B0.** • These pins output second blue, green, and red pixel data, respectively. • B7 pins reflect most-significant data bits. B0 pins reflect least-significant data bits.

Figure 2-2 shows the relationship of outputs from the ICS1532 ADC to inputs of a 1024 × 768 LCD panel that samples 2 pixels of data with up to 48-bit data signal.

- DA indicates 'A channel' pixels, and DB indicates 'B channel' pixels.)

For timing information, see Chapter 7, "Timing Diagrams".

Figure 2-2. Relationship of Outputs from an ICS1532's ADC to Inputs of 1024 × 768 LCD Panel



2.0.1.4 Phase-Locked Loop Pins

Table 2-4 lists the pins for the phase-locked loop circuitry. For a block diagram that shows the function of these pins, see Figure 3-1.

Table 2-4. Phase-Locked Loop Pins

Pin Name	Pin Type	Pin Description
EXTFIL	Input	**External Filter.** This pin works with XFILRET (in this table, see XFILRET) and other components as part of an optional external filter for the pixel phase-locked loop.
HSYNC	Input	**Horizontal Sync.** • This 5-V tolerant pin is the clock input for the pixel PLL. • Typically this pin connects to the HSYNC from a PC display controller. • In this data sheet, this HSYNC signal is also called 'input HSYNC'.
LOCK#	Output	In this table, see the 'STATUS' pin name.
PDEN	Input	**Phase-Detector Enable.** This pin is the input for the Phase/Frequency Detector enable that can suspend the charge pump activity. It is 5-V tolerant. (For more information, see Reg 00:1-0 in Section 4.5.1, "Register 00h: Input Control Register".)
STATUS#	Output	**Status (Formerly called 'Lock').** This active-low pin works with Reg 2C:1-0. • Low - When a lock condition occurs for the PLL selected by Reg 2C:1-0. • High -When no lock condition occurs for the PLL selected by Reg 2C:1-0.
XFILRET	Input	**External Filter Return.** This pin works with EXTFIL (in this table, see EXTFIL) and other components as part of an optional external filter for the pixel phase-locked loop.

2.0.1.5 I2C Serial Bus Pins

Table 2-5. I2C Serial Bus Pins

Pin Name	Pin Type	Pin Description
SBADR	Input	**Serial Bus Address.** This pin determines the address for the ICS1532 I2C serial bus. • When the signal on this pin is: – Low, the pixel bit address is 49h for read operations and 48h for write operations. – High, the pixel bit address is 4Bh for read operations and 4Ah for write operations. • For more information on this pin, see Section 1.3, "I2C Serial Interface".
SCL	Input	**Serial Clock.** This 5-V tolerant pin is the clock for the interface to an I2C serial bus.
SDA	Input/ Output	**Serial Data.** This 5-V tolerant pin connects to the data pin for an I2C serial bus.

2.0.1.6 Ground Pins

Table 2-6. Ground Pins

Pin Name	Pin Description
VSS	**Ground for (Analog Inputs for Digital Pixel PLL Circuitry).** • These pins are used to ground digital portions of the pixel PLL circuitry that receive analog inputs. • The VSSD pin must also connect to these pins.
VSSA	**Ground for Analog (Pixel PLL Circuitry).** This pin is used to ground the analog portions of the pixel PLL circuitry.
VSSAADC (2.5)	**Ground for 2.5 Volt Analog ADC (Circuitry).** These pins are used to ground the 2.5 volt analog portions of the ADC
VSSD	**Ground for Digital (Pixel PLL and Circuitry for I2C Serial Interface).** This pin is used to ground the digital portions of the pixel PLL circuitry and the circuitry for an I2C serial interface.
VSSDADC (2.5)	**Ground for 2.5 Volt Digital ADC (Circuitry).** This pin is used to ground 2.5 volt digital portions of the ADC.
VSSMCLK	**Ground for Memory Clock (Circuitry).** This pin is used to ground circuitry for the memory clock PPL (that is, MCLK).
VSSPCLK	**Ground for Panel Clock (Circuitry).** This pin is used to ground circuitry for the panel clock PLL (that is, PNLCLK).
VSSQ	**Ground for Output Drivers.** This pin is used to ground output drivers for the pixel PLL circuitry.
VSSQADC	**Ground for Output Drivers for ADC.** These pins are used to ground the pixel data output drivers for the analog-to-digital converter.
VSSSUB	**Ground for Substrate.** These pins are used to provide ground for the chip substrate.
VSS(Test2) VSS(Test1)	**Ground (Normal Mode) or Test Outputs.** This pin must be connected to ground. Test mode is Reserved.
VSSXTL	**Ground for Crystal Oscillator.** This pin is used to ground the internal crystal oscillator circuitry.

2.0.1.7 Power Pins

Table 2-7. Power Pins

Pin Name	Pin Description
VDDA	**(3.3 V) Supply for Analog (Pixel PLL Circuitry).** This pin supplies 3.3 V to the analog portions of the pixel PLL circuitry.
VDDAADC (2.5)	**(2.5 V) Supply for Analog ADC (Circuitry).** These pins supply 2.5 volts to the analog portions of the ADC.
VDDD	**(3.3 V) Supply for Digital (Pixel PLL and I2C Serial Bus) Circuitry.** This pin supplies 3.3 V to the digital pixel PLL and circuitry for an I2C serial bus interface.
VDDDADC (2.5)	**(2.5 V) Supply for Digital ADC (Circuitry).** This pin supplies 2.5V to digital portions of the ADC.
VDDMCLK	**(3.3 V) Supply for Memory Clock.** This pin supplies 3.3 V to the memory clock PLL circuitry.
VDDPCLK	**(3.3 V) Supply for Panel Clock.** This pin supplies 3.3 V to the panel clock PLL circuitry.
VDDQ	**(3.3 V) Supply for Output Drivers.** This pin supplies 3.3 V to the output driver circuitry for the pixel PLL.
VDDQADC	**(3.3 V) Supply for Output Drivers for Analog-to-Digital Converter.** These pins supply 3.3 V to the pixel data output drivers of the ADC.
VDDXTL	**(3.3V) Supply for Crystal Oscillator.** This pin supplies 3.3 V to the internal crystal oscillator circuitry.

2.0.1.8 No-Connect and Reserved Pins

Table 2-8. No-Connect and Reserved Pins

Pin Name	Pin Description
NC	**No Connect.** Do not connect these pins.
Reserved	**Reserved.** These pins are always reserved for use by ICS.

Chapter 3 Functional Blocks

Figure 3-1. Pixel PLL Block Diagram

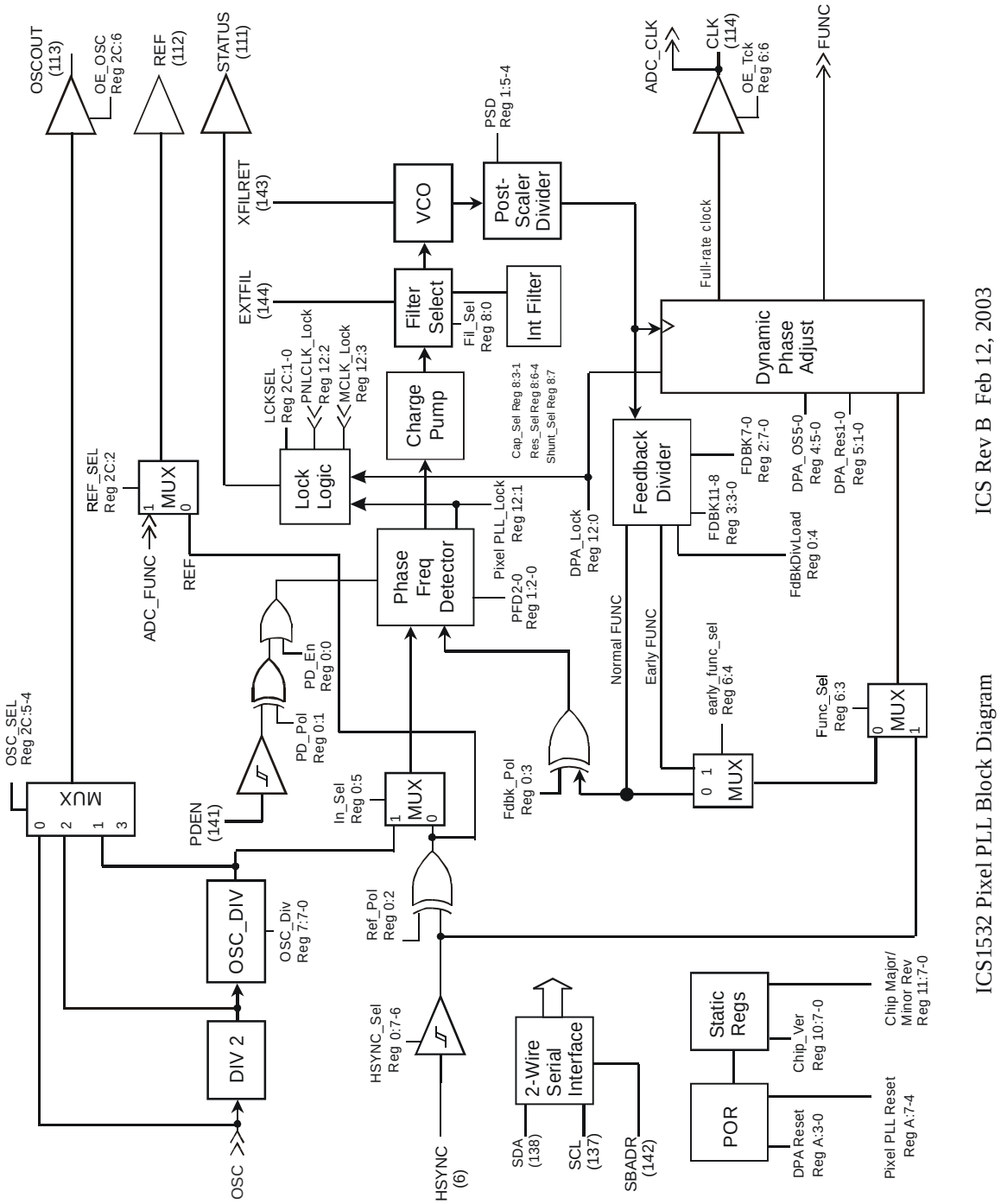


Figure 3-2. CLK Block Diagram

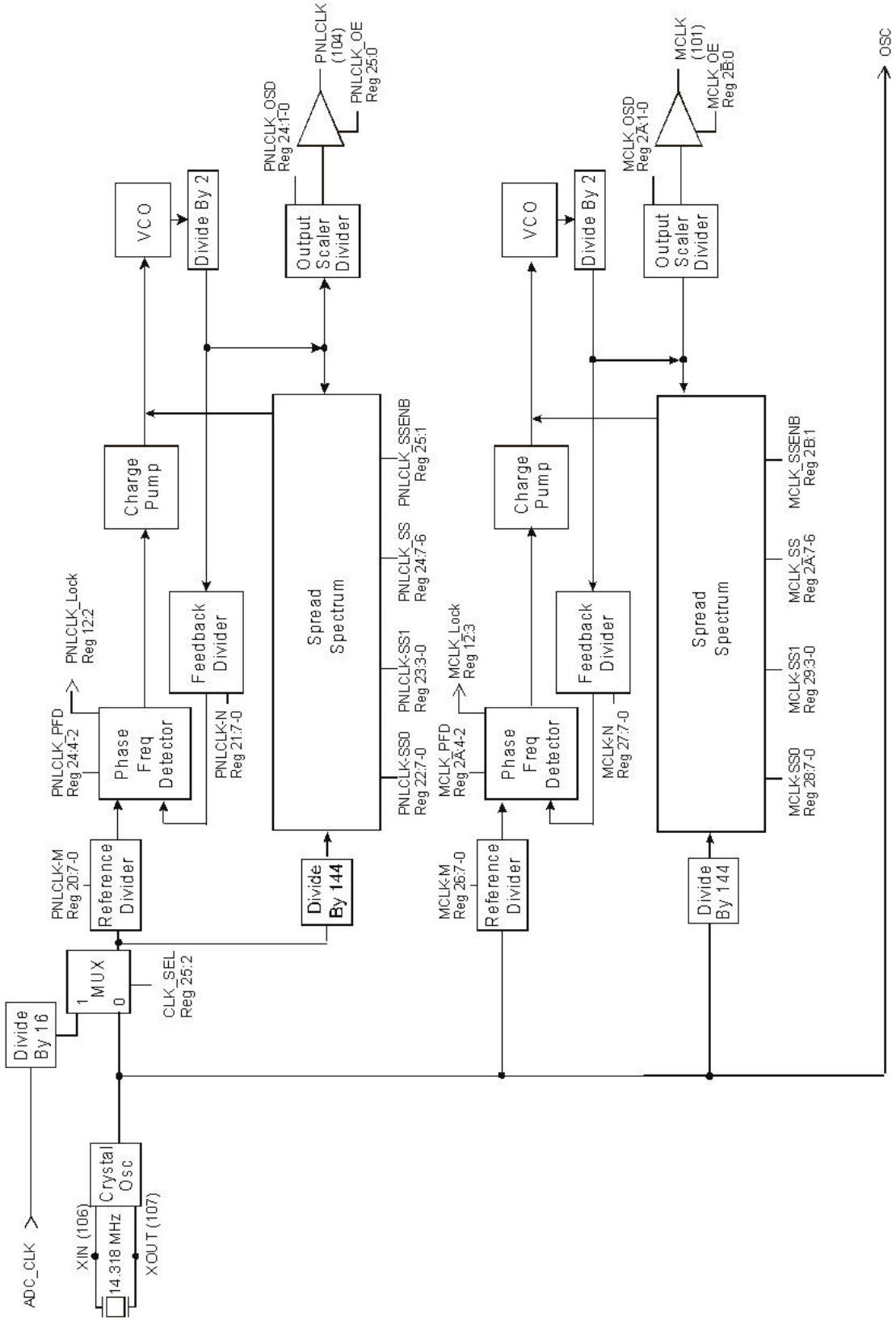
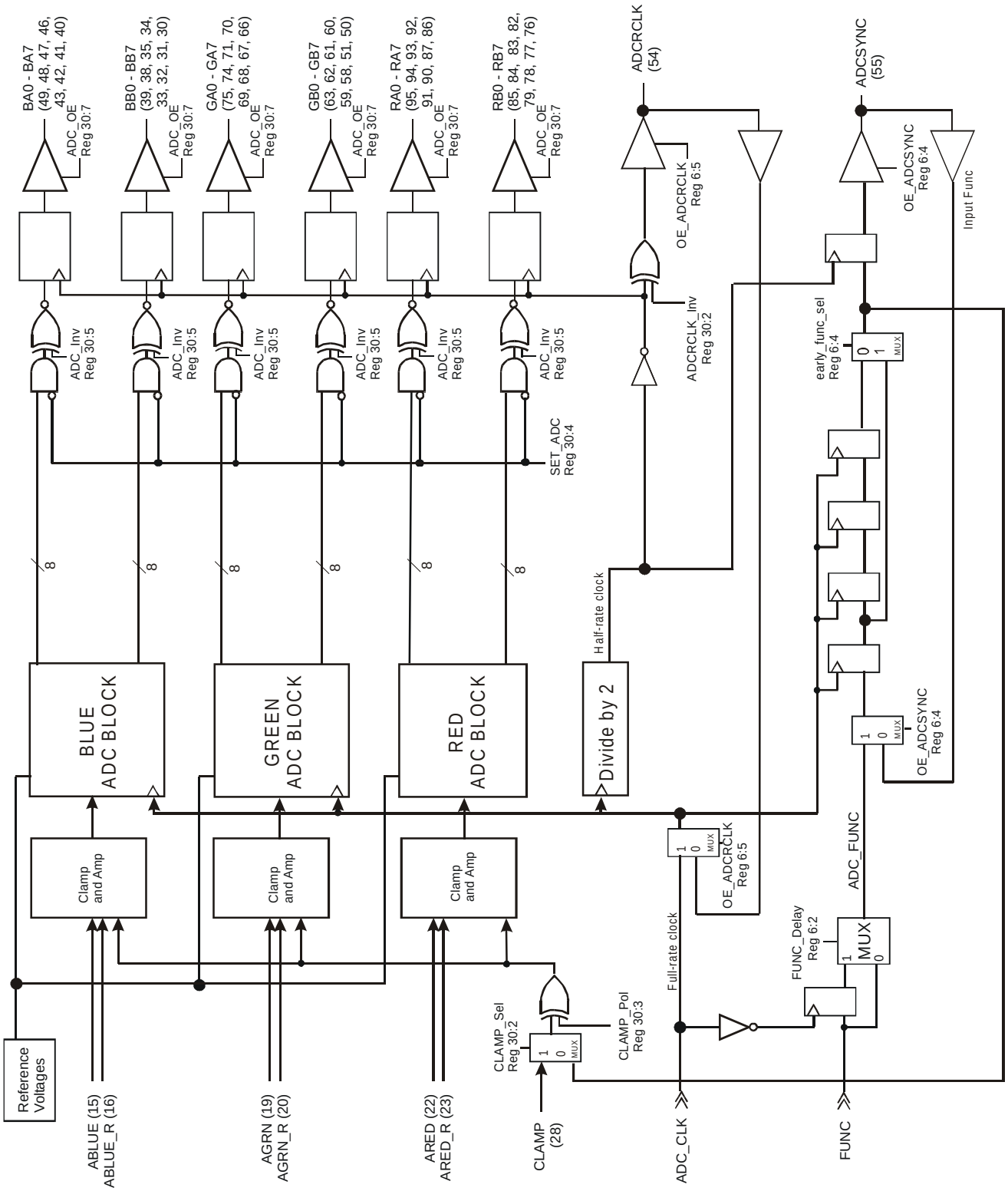


Figure 3-3. ADC Block Diagram



ICS1532 ADC Block Diagram ICS Rev D Feb 12, 2003

Chapter 4 Register Set

The tables in this chapter detail the functionality of the ICS1532 Register Set bits. The tables include the register locations, the bit positions, names, and definitions, along with their read/write access, reset values, and any special functions or capabilities.

4.1 Reserved Bits

The ICS1532 has a number of reserved bits throughout the Register Set. These bits provide enhanced test functions (intended for use only by ICS manufacturing) and calibration functions (intended for use in production environments).

Important: The customer must not change the value of reserved bits. If the customer changes the default values of these reserved bits, normal operation of the ICS1532 can be affected.

4.2 Register Set Conventions

Register Set conventions include the following:

- Bits are listed in the order of most-significant bit (MSB) to least-significant bit (LSB).
- Unless otherwise indicated, bit settings are listed in terms of digital (and not hexadecimal) values.
- When a bit definition includes word(s) in parentheses, the word in parenthesis is not part of the bit name, but is given to explain the origin of the bit's name.

4.3 Register Set Abbreviations and Acronyms

Table 4-1 lists and defines abbreviations and acronyms used specifically in this chapter.

Table 4-1. Register Set Abbreviations and Acronyms

Abbreviation or Acronym	Definition
DB-DPA	**Double-Buffered / Dynamic Phase Adjust.** Indicates double-buffered registers for which working registers load during a software Dynamic Phase Adjust reset.
DB-MK	**Double-Buffered / Memory Clock.** Indicates double-buffered registers for which working registers load during a software MCLK reset.
DB-PK	**Double-Buffered / Panel Clock.** Indicates double-buffered registers for which working registers load during a software PNLCLK reset.
DB-PLL	**Double-Buffered / Phase-Locked Loop.** Indicates double-buffered registers for which working registers load during a software pixel PLL reset.
IN-A	**Increment All.** Indicates a value that increments with each all-layer revision of the ICS1532.
Reg	**Register**
R/W	**Read/Write**

4.4 Register Set Outline.

Table 4-2. Register Set Outline

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
00h	Input Control	R/W	7-6	HSYNC_Sel	Select a Schmitt trigger	0
			5	In_Sel	Select Phase Detector Input	1
			4	Fdbk Div Load	Select load for Feedback Divider	0
			3	Fdbk_Pol	Select feedback polarity for Phase/Frequency Detector	0
			2	Ref_Pol	Select polarity of external reference	0
			1	PD_Pol	Select polarity of PDEN to Phase/Frequency Detector	0
			0	PD_En	Enable Phase/Frequency Detector	1
01h	Loop Control	R/W. D-PLL.	7-6	Reserved	Reserved	0
			5-4	PSD	Select value for Post-Scaler Divider	0
			3	Reserved	Reserved	0
			2-0	PFD	Select Phase/Frequency Detector gain	0
02h	Fdbk Div 0	R/W. D-PLL.	7-0	FDBK [7-0]	Select value for Feedback Divider LSBs bits 7-0	FF
03h	Fdbk Div 1	R/W. D-PLL.	7-4	Reserved	Reserved	–
			3-0	FDBK [11-8]	Select value for Feedback Divider MSBs bits 11-8	0
04h	DPA Offset	R/W	7-6	Reserved	Reserved	0
			5-0	DPA_OS	Select offset for Dynamic Phase Adjust	0
05h	DPA Control	R/W. D-DPA.	7-2	Reserved	Reserved	–
			1-0	DPA_Res	Select resolution for Dynamic Phase Adjust	0
06h	Output Enables	R/W	7	Reserved	Reserved	0
			6	OE_TCLK	Enable clock output to ADC and CLK pin	0
			5	OE_ADCRCLK	Enable ADCRCLK clock output	0
			4	OE_ADCSYNC	Enable output for ADCSYNC	0
			3	FUNC_Sel	Select signal source for ADC_FUNC signal	0
			2	FUNC_Delay	Select one CLK delay for ADC_FUNC signal	0
			1	Reserved	Reserved	0
			0	Early_FUNC	Enable 12 CLK earlier FUNC	0
07h	OSC Divider	R/W	7-0	OSC_Div	Oscillator divider value	0
08h	Internal Filter	R/W	7	Shunt_Sel	Select internal filter shunt capacitor size	1
			6-4	Res_Sel	Select internal filter resistor size	7
			3-1	Cap_Sel	Select internal filter capacitor size	7
			0	Fil_Sel	Select type of loop filter	1
09h	Reserved					N/A
0Ah	Pixel PLL/ DPA Resets	Write	7-4	Pixel PLL Reset	Writing 5xh resets pixel PLL and loads working Regs 1h through 3h	N/A
			3-0	DPA Reset	Writing xAh resets DPA and loads working Reg 5h	N/A
0Bh-0Fh	Reserved					N/A
10h	Chip Ver	Read	7-0	Chip Ver	Read chip version 32 decimal (20 hex) as in 1532	20
11h	Chip Rev	Read. IN-A.	7-4	Chip Major Rev	Read initial value 00h. +Value increments with chip revision.	00+
			3-0	Chip Minor Rev	Read initial value 01h. +Value increments with chip revision.	01+

Table 4-2. Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
12h	Rd_Reg	Read	7-4	Reserved	Reserved	N/A
			3	PLL_Lock	Read Pixel PLL lock status	N/A
			2	MCLK_Lock	Read Memory MCLK lock status	N/A
			1	PCLK_Lock	Read Panel PLL lock status	N/A
			0	DPA_Lock	Read DPA lock status	N/A
13h	r_ou_range_B	Read	7-4	Reserved	Reserved	N/A
	r_ou_range_A	Read	3-0	Reserved	Reserved	N/A
14h	r_high	Read	7-0	Reserved	Reserved	N/A
15h	r_low	Read	7-0	Reserved	Reserved	N/A
16h	g_ou_range_B	Read	7-4	Reserved	Reserved	N/A
	g_ou_range_A	Read	3-0	Reserved	Reserved	N/A
17h	g_high	Read	7-0	Reserved	Reserved	N/A
18h	g_low	Read	7-0	Reserved	Reserved	N/A
19h	b_ou_range_B	Read	7-4	Reserved	Reserved	N/A
	b_ou_range_A	Read	3-0	Reserved	Reserved	N/A
1Ah	b_high	Read	7-0	Reserved	Reserved	N/A
1Bh	b_low	Read	7-0	Reserved	Reserved	N/A
1Ch-1Fh	Reserved					N/A
20h	PNLCLK-M	R/W. D-PK.	7-0	PNLCLK_M	Select value for PNLCLK M Reference Divider	0
21h	PNLCLK-N	R/W. D-PK.	7-0	PNLCLK_N	Select value for PNLCLK N Feedback Divider	0
22h	PNLCLK-SS0	R/W. D-PK.	7-0	PNLCLK_SS0	Select value for PNLCLK spread-spectrum counter LSBs bits 7-0	0
23h	PNLCLK-SS1	R/W. D-PK.	7-4	Reserved	Reserved	0
			3-0	PNLCLK_SS1	Select value for PNLCLK spread-spectrum counter MSBs bits 11-8	0
24h	PNLCLK-SSOE	R/W. D-PK.	7-6	PNLCLK_SS	Select PNLCLK spread-spectrum gain	0
			5	Reserved	Reserved	0
			4-2	PNLCLK_PFD	Select PNLCLK Phase/Frequency Detector gain	0
			1-0	PNLCLK_OSD	Select value for PNLCLK Output Scaler Divider	0
25h	PNLCLK-OE	R/W	7-3	Reserved	Reserved	0
			2	CLK_SEL	Select input for PNLCLK PLL	0
			1	PNLCLK_SSENB	Enable PNLCLK spread-spectrum	0
			0	PNLCLK_OE	Enable PNLCLK output	0
26h	MCLK-M	R/W. D-MK.	7-0	MCLK_M	Value for MCLK M Feedback Divider	0
27h	MCLK-N	R/W. D-MK.	7-0	MCLK_N	Value for MCLK N (Numerator)Feedback Divider	0
28h	MCLK-SS0	R/W. D-MK.	7-0	MCLK_SS0	Select MCLK spread-spectrum counter LSBs bits 7-0	0

Table 4-2. Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
29h	MCLK-SS1	R/W. D-MK.	7-4	Reserved	Reserved	0
			3-0	MCLK_SS1	Select MCLK spread-spectrum counter MSBs bits 11-8	0
2Ah	MCLK-SSOE	R/W. D-MK.	7-6	MCLK_SS	Select MCLK spread-spectrum gain	0
			5	Reserved	Reserved	0
			4-2	MCLK_PFD	Select MCLK Phase/Frequency Detector gain	0
			1-0	MCLK_OSD	Select value for MCLK Output Scaler Divider	0
2Bh	MCLK-OE	R/W	7-2	Reserved	Reserved	0
			1	MCLK_SSENB	Enable MCLK spread-spectrum	0
			0	MCLK_OE	Enable MCLK output	0
2Ch	OUTPUT MUX	R/W	7	High_Drive#	Select drive strength for ADC Data output pins	0
			6	OE_OSC	Enable OSCOUT output pin	1
			5-4	OSC_Sel	Select output from 4-way MUX to OSCOUT	0
			3	Reserved	Reserved	0
			2	REFSEL	Select REF status	0
			1-0	LCKSEL	Select PLL lock status	1
2Dh	PLL Reset	Write	7-4	MCLK_Reset	Writing 5xh resets MCLK PLL & loads Regs 26h~2Bh	N/A
			3-0	PNLCLK_Reset	Writing xAh resets PNLCLK PLL & loads Regs 20~25h	N/A
2Eh-2Fh	Reserved					N/A
30h	ADC CTRL	R/W	7	ADC_OE	Enable ADC output	0
			6	ADC_Inv	Invert ADCRCLK signal	0
			5	Force_ADC	Force ADC Outputs to off state	0
			4	ADC_Clock_D	ADC clock state delay	0
			3	ADC_Inv	Invert ADC Outputs	0
			2-1	CLAMP_Sel	Select source to clamp control	0
			0	CLAMP_Pol	Select polarity of signal to clamp control	0
31h	R_Control	R/W	7	R_VIN_Range	Red Input Voltage Range (0=700mv, 1=1V)	1
			6	Reserved	Reserved	0
			5	R_CLAMP_T3	Red Clamp Time Constant (0= Nom., 1=0.3 Nom.)	0
			4	R_CLAMP_Type	Soft/Xhard Clamp Function	1
			3	R_CLAMP_T5	Red Clamp Time Constant (0= Nom., 1=0.5 Nom.)	0
			2-1	Reserved	Reserved	1
			0	XPD_R	Power Down Red Channel (0=Powered Down)	1
32h	G_Control	R/W	7	G_Fixed_Gain	Green Gain Adjust. (0=100%, 1=140%)	1
			6	Reserved	Reserved	0
			5	G_CLAMP_T3	Green Clamp Time Constant (0= Nominal, 1=0.3 Nom.)	0
			4	G_CLAMP_Type	Green Soft/Xhard Clamp Function	1
			3	G_CLAMP_T5	Green Clamp Time Constant (0= Nominal,1=0.5 Nom.)	0
			2	Reserved	Reserved	1
			1	SOG	Sync On Green	0
			0	XPD_G	Power Down Green Channel (0=Powered Down)	1
33h	B_Control	R/W	7	B_Fixed_Gain	Blue Gain Adjust. (0=100%, 1=140%)	1
			6	Reserved	Reserved	0
			5	B_CLAMP_T3	Blue Clamp Time Constant (0= Nominal, 1=0.3 Nom.)	0
			4	B_CLAMP_Type	Blue Soft/Xhard Clamp Function	1
			3	B_CLAMP_T5	Blue Clamp Time Constant (0= Nominal,1=0.5 Nom.)	0
			2-1	Reserved	Reserved	0
			0	XPD_B	Power Down Blue Channel	1

Table 4-2. Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
34h	R_Gain	R/W	7-3	R_PGA_Gain	Fine adjust red channel ADC ladder voltage	tbd
			2-0	R_ADC_Gain	Adjust Video Amp Gain for red channel of ADC	tbd
35h	G_Gain	R/W	7-3	G_PGA_Gain	Fine adjust green channel ADC ladder voltage	tbd
			2-0	G_ADC_Gain	Adjust Video Amp Gain for green channel of ADC	tbd
36h	B_Gain	R/W	7-3	B_PGA_Gain	Fine adjust blue channel ADC ladder voltage	tbd
			2-0	B_ADC_Gain	Adjust Video Amp Gain for blue channel of ADC	tbd
37h	PSEL	R/W	7-4	BG_CAL	Band Gap Calibration	8
			3	XBG_PD	Band Gap Power Down (0=Powered Down)	1
			2	PSEL3	Select general-purpose programmable output 3	0
			1	PSEL2	Select general-purpose programmable output 2	0
			0	PSEL1	Select general-purpose programmable output 1	0
38h	R_Offset		7-0	R_Offset	Red channel offset	80
39h	G_Offset		7-0	G_Offset	Green channel offset	80
3Ah	B_Offset		7-0	B_Offset	Blue channel offset	80
3Bh	IBias		7-6	IBias_Buf	ADC Buffer Bias Adjustment	2
			5-4	IBias_VA	Video Amp Bias Adjustment	2
			3-0	IBias_ADC	ADC Bias Adjustment	A
3Ch	Test_Mux		7-3		Channel Test Mux	0
			2-0		Band Gap Test Mux	0

4.5 Register Definitions

The tables in this section specify for each register bit the reset value, if one exists. After a reset, the ICS1532 sets all register bits to their default values.

4.5.1 Register 00h: Input Control Register

The Input Control Register is used to select inputs that control the pixel PLL Phase/Frequency Detector.

Table 4-3. Input Control Register

Bit	Bit Name	Bit Definition	Access	Reset
00:7-00:6	HSYNC_Sel [1-0]	**HSYNC Select (Schmitt Level) [1-0].** • 00, 01, 10, 11 = Schmitt trigger levels 0, 1, 2 & 3 respectively	R/W	0
00:5	In_Sel	**Input Select (Phase/Frequency Detector)** • 0 = Input is the HSYNC pin. • 1 = Input is the OSC pin	R/W	1
00:4	Fdbk Div Load	**(Internal) Feedback Divider Load Control.** • 0 = New values are loaded on a pixel PLL reset. • 1 = New values are loaded on the next scan line without a PLL reset.	R/W	0
00:3	Fdbk_Pol	**Invert Feedback Polarity (Phase/Frequency Detector)** • 0 = The polarity is positive edge. • 1 = The polarity is negative edge.	R/W	0
00:2	Ref_Pol	**Invert REF Polarity.** REF is the HSYNC input signal, post Schmitt trigger • 0 = Polarity is non-inverted. • 1 = Polarity is inverted.	R/W	0
00:1	PD_Pol	**Phase/(Frequency) Detector Polarity.** • See Table 4-4	R/W	0
00:0	PD_En	**Phase/(Frequency) Detector Enable.** This bit is used to globally enable the Phase/Frequency Detector. • See Table 4-4	R/W	1

Table 4-4. Main PLL Phase Detector Controls

PD_Pol (Reg 00:1)	PD_En (Reg 00:0)	Pixel PLL Phase Detector Enabled?
X	1	Enabled
0	0	PDEN (pin 144) Active HIGH
1	0	PDEN (pin 144) Active LOW

4.5.2 Register 01h: Loop Control Register

The Loop Control Register is used to control the pixel PLL.

Table 4-5. Loop Control Register

Bit	Bit Name	Bit Definition	Access	Reset
01:7-01:6	Reserved	**Reserved**	–	0
01:5-01:4	PSD [1-0]	**Post-Scaler Divider [1-0]** • These bits sets the ratio of the VCO (loop) frequency output to the pixel clock frequency. – 0 = 2:1 – 1 = 4:1 – 2 = 8:1 – 3 = 16:1 • DB-PLL. These bits take effect after 5x is written to Reg 0Ah, bits 7:4.	R/W	0
01:3	Reserved	**Reserved**	–	0
01:2-01:0	PFD [2-0]	**Phase/Frequency Detector (Gain) [2-0]** – 0 = PFD gain = 1μA/2πrad. – 1 = PFD gain = 2μA/2πrad. – 2 = PFD gain = 4μA/2πrad. – 3 = PFD gain = 8μA/2πrad. – 4 = PFD gain = 16μA/2πrad. – 5 = PFD gain = 32μA/2πrad. – 6 = PFD gain = 64μA/2πrad. – 7 = PFD gain = 128μA/2πrad. • DB-PLL. These bits take effect after 5x is written to Reg 0Ah, bits 7:4.	R/W	0

4.5.3 Register 02h: Fdbk Div 0 Register

The Fdbk Div 0 (Feedback Divider 0) Register, in combination with Fdbk Div 1 Register, sets the value of the internal feedback divider for the pixel PLL. It adjusts the number of pixel clocks by using the horizontal total, where:

Horizontal Total = [(Number of displayed pixels) + (Horizontal blanking interval)] per HSYNC

Table 4-6. Fdbk Div 0 Register

Bit	Bit Name	Bit Definition	Access	Reset
02:7-02:0	FDBK [7–1]	**(Pixel PLL) Feedback Divider [7-1].** • These bits are the least-significant bits [7-1] for the internal pixel PLL Feedback Divider. (See Table 4-7 and Figure 4-1) • DB-PLL. These bits take effect after 5x is written to Reg 0Ah, bits 7:4.	R/W	7F
02:0	FDBK [0]	**(Pixel PLL) Feedback Divider [0].** • MUST be 0, meaning the total number of pixels must be even.	R/W	1

4.5.4 Register 03h: Fdbk Div 1 Register

The Fdbk Div 1 (Feedback Divider 1) Register is used in combination with Fdbk Div 0 Register.

Table 4-7. Fdbk Div 1 Register

Bit	Bit Name	Bit Definition	Access	Reset
03:7-03:4	Reserved	**Reserved.** • These bits can be programmed to ‘0’.	–	–
03:3-03:0	FDBK [11-8]	**(Pixel PLL) Feedback Divider [11-8].** • These bits are the most-significant bits [11-8] for the internal pixel PLL Feedback Divider. (See Table 4-6.) • Controls the total number of clock periods that the ICS1532 generates between successive HSYNCs – The ICS1532 generates 8 more clocks than what is programmed in these bits. See Figure 4-1. • DB-PLL. These bits take effect after 5x is written to Reg 0Ah, bits 7:4.	R/W	0

Figure 4-1. Feedback Divider Modulus

Feedback Divider Modulus =

Fdbk Div 1 (Reg 3)				Fdbk Div 0 (Reg 2)							
3	2	1	0	7	6	5	4	3	2	1	0

+ 8

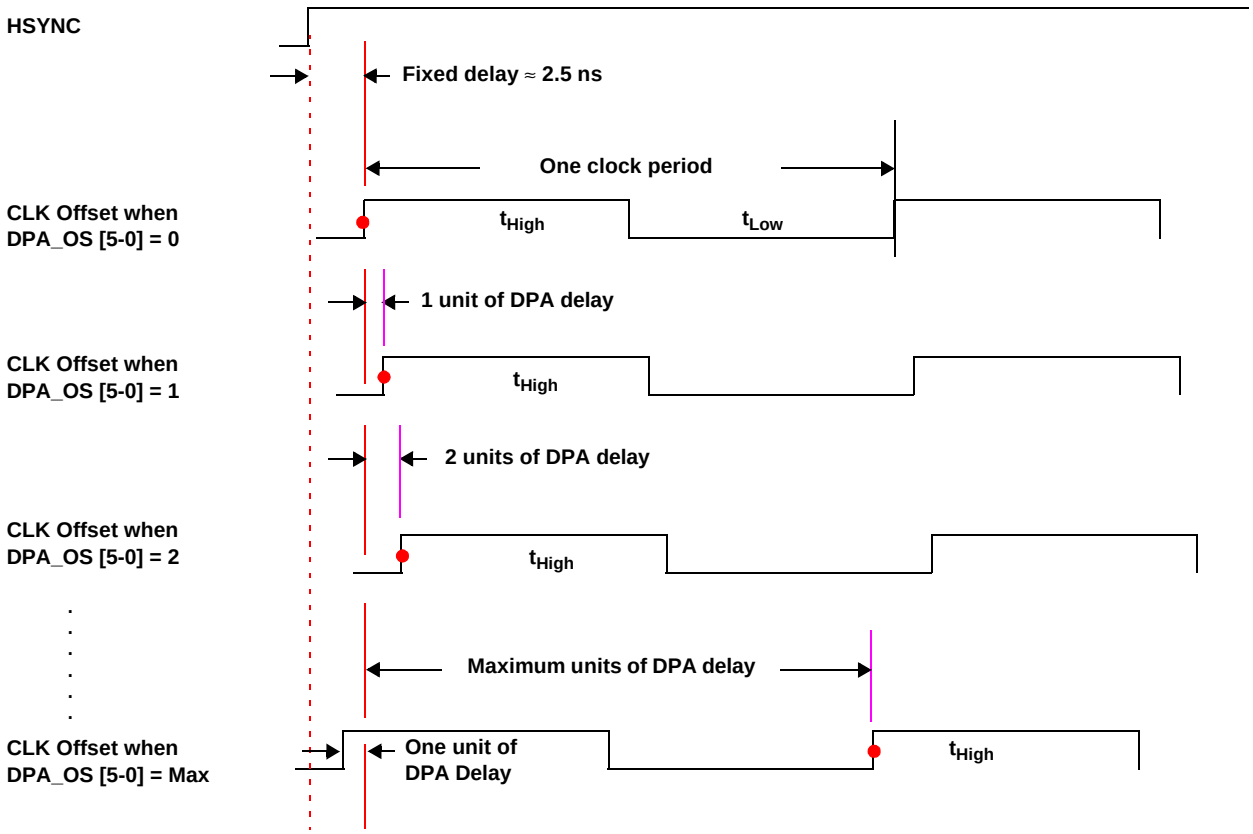
4.5.5 Register 04h: DPA Offset

The DPA Offset (Dynamic Phase Adjust Offset) Register is used to select the clock edge offset.

Table 4-8. DPA Offset Register

Bit	Bit Name	Bit Definition	Access	Reset
04:7-04:6	Reserved	**Reserved**	–	0
04:5-04:0	DPA_OS [5-0]	**Dynamic Phase Adjust Offset [5-0]** As Figure 4-2 shows, these bits control the amount of offset between the rising edge of the recovered HSYNC and the rising edge of CLK. • The offset is in discrete steps from 0 clock periods up to 1 clock period, minus one unit of a DPA delay element. • The unit of the DPA delay depends on both the pixel clock output frequency and the number of delay element units (as selected by Reg 05:1-0).	R/W	0

Figure 4-2. DPA Offset (As Determined by Regs 04 and 05)



4.5.6 Register 05h: DPA Control

The DPA (Dynamic Phase Adjust) Control Register is used to select the resolution of the Dynamic Phase Adjust circuitry, used to adjust the pixel clock on a sub-pixel basis.

Table 4-9. DPA Control Register

Bit	Bit Name	Bit Definition	Access	Reset
05:7-05:2	Reserved	**Reserved**	–	–
05:1-05:0	DPA_Res [1-0]	**Dynamic Phase Adjust Resolution [1-0].** Selects the number of delay elements used by the Dynamic Phase Adjuster. • See Table 4-10 • DB-DPA. These bits take effect after xA is written to Reg 0Ah, bits 3:0.	R/W	0

Table 4-10. DPA Control

Reg 05:1-0		1. Number of Delay Element Units (Decimal)	2. Reg 04:5-0 Max. Value (Hex)	3. Pixel Clock Range (MHz)
Bit 1	Bit 0			
0	0	16	0F	55 – 260
0	1	32	1F	27 – 130
1	0	Reserved	Reserved	
1	1	64	3F	14 – 64

4.5.7 Register 06h: Output Enables

The Output Enables Register is used to select and enable various outputs.

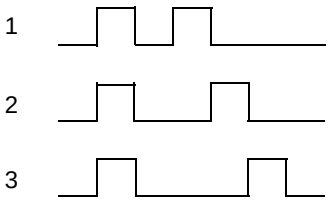
Note: Table 4-11 refers to ADC_FUNC, an internally generated signal that is delayed so it is in the same domain as the internal ADC_CLK signal (that is, the pixel clock). Functionally, depending on the setting of Reg 06:3, ADC_FUNC is equivalent to either ADCSYNC (which provides recovered HSYNC) or the input HSYNC.

Table 4-11. Output Enables Register

Bit	Bit Name	Bit Definition	Access	Reset
06:7	Reserved	**Reserved**	–	0
06:6	OE_Tck	**Output Enable Clock.** This bit enables the pixel clock output on the CLK pin. • 0 = The pixel clock output is disabled (high-impedance). • 1 = The pixel clock output is enabled.	R/W	0
06:5	OE_ADCRCLK	**Output Enable for ADCRCLK.** • 0 – The clock output for the ADC is disabled (high-impedance). – An external clock can be provided to the ADC via the ADCRCLK pin. • 1 – The clock output for the ADC is enabled. – The input multiplexer selects the internal pixel clock.	R/W	0
06:4	OE_ADCSYNC	**Output Enable for ADCSYNC.** • 0 – The output for the ADCSYNC signal is disabled (high-impedance) – An external ADC sync signal is accepted from the ADCSYNC pin • 1 – The ADCSYNC output is enabled and internally selected.	R/W	0
06:3	FUNC_Sel	**FUNC (Source) Select.** This bit selects the source of the signal to ADC_FUNC. • 0 = ADC_FUNC source is the output of the Feedback Divider • 1 = ADC_FUNC source is REF: the post-Schmitt input HSYNC	R/W	0
06:2	FUNC_Delay	**FUNC Delay.** • 0 = The ADC_FUNC signal is unaltered. • 1 = The ADC_FUNC signal is delayed by 1 pixel clock, which has the effect of transposing the channel ‘A” data to the ‘B’ channel output pins and the reverse.	R/W	0
06:1	Reserved	**Reserved**	–	0
06:0	EARLY_FUNC	**EARLY FUNC Select** • 0 = ADC_FUNC output signal is unaltered. • 1 = ADC_FUNC output signal is generated 12 pixel clocks earlier than normal. This is generally used to guarantee internal black level clamping completes before the active HSYNC edge transitions.	R/W	0

4.5.8 Register 07h: OSC Divider

Table 4-12. OSC Divider Register

Bit	Bit Name	Bit Definition	Access	Reset
07:7-07:0	OSC_Div [7-0]	**Oscillator Divider [7-0].** After the signal from the internal crystal oscillator is divided by 2 (see Figure 3-1), these bits select the value by which the resulting signal is divided. • 0 = Reserved. • 1 = Divide by 1 • 2 = Divide by 2 • 3 = Divide by 3, and so forth. 	R/W	0

4.5.9 Register 08h: Internal Filter

The Internal Filter Register is used to select values for the internal loop filter.

Table 4-13. Internal Filter Register

Bit	Bit Name	Bit Definition	Access	Reset
08:7	Shunt_Sel	**Shunt (Capacitor) Select** • 0 = Selects an alternate-size shunt capacitor • 1 = Select the default-size shunt capacitor	R/W	1
08:6-08:4	Res_Sel [2-0]	**Resistor Select [2-0]** These bits are used to select the size of the internal filter's resistor. Resistor value $\approx$ {(Value of Res_Sel [2-0] bits) $\times$ 4kΩ} + 3kΩ	R/W	7
08:3-08:1	Cap_Sel [2-0]	**Capacitor Select [2-0]** These bits are used to select the size of the internal filter's capacitor. Capacitor value: $\approx$ {(Value of Cap_Sel [2-0] bits) + 1} $\times$ 236 pF	R/W	7
08:0	Fil_Sel	**Internal (Loop) Filter Select** • 0 = Loop filter is external • 1 = Loop filter is internal	R/W	1

4.5.10 Register 09h: Reserved

This register is reserved. (See Section 4.1, "Reserved Bits".)

4.5.11 Register 0Ah: Pixel PLL/DPA Reset

The Pixel PLL/DPA Reset Register is used to reset the pixel PLL and DPA circuits.

Table 4-14. Register

Bit	Bit Name	Bit Definition	Access	Reset
0A:7-0A:4	Pixel PLL Reset [3-0]	**Pixel Phase-Locked Loop Reset [3-0].** Writing 5xh to these bits does the following: • Resets the pixel phase-locked loop. • Loads working Regs 01 to 03.	Write	N/A
0A:3-0A:0	DPA Reset [3-0]	**Dynamic Phase Adjust Reset [3-0].** Writing xAh to these bits does the following: • Resets the Dynamic Phase Adjust. • Loads working Reg 05.	Write	N/A

4.5.12 Register 0Bh-0Fh: Reserved

These registers are reserved.

4.5.13 Register 10h: Chip Ver

The Chip Ver (Chip Version) Register is used to read the version number of the ICS1532.

Table 4-15. Chip Ver Register

Bit	Bit Name	Bit Definition	Access	Reset
10:7-10:0	Chip Ver [7-0]	**Chip Version [7-0].** • This register indicates the version number of the ICS chip. • For the ICS1532, these bits have a value of 32 decimal (that is, 20 hex), as in 1532.	Read	20

4.5.14 Register 11h: Chip Rev

The Chip Rev (Chip Revision) Register is used to read the revision level of the ICS1532 chip.

Table 4-16. Chip Rev Register

Bit	Bit Name	Bit Definition	Access	Reset
11:7-11:4	Chip Major Rev [3-0]	**Chip Major Revision [3-0].** • Indicate a ICS1532 major revision. • Increment (+) with each all-layer revision. • Have an initial (reset) value of 00h.	Read	00+
11:3-11:0	Chip Minor Rev [3-0]	**Chip Minor Revision [3-0].** • Indicate a ICS1532 minor revision. • Increment (+) with each all-layer revision. • Have an initial (reset) value of 01h.	Read	01+

4.5.15 Register 12h: Rd_Reg

The Rd_Reg (Read Register) is used to read the lock status of the four PLLs on the ICS1532.

Table 4-17. Rd_Reg Register

Bit	Bit Name	Bit Definition	Access	Reset
12:7-12:4	Reserved	**Reserved.**	Read	N/A
12:3	Pixel PLL_Lock	**Pixel Phase-Locked Loop Lock (Status)** • 0 = The pixel PLL is 'unlocked'. • 1 = The pixel PLL is 'locked'.	Read	N/A
12:2	MCLK_Lock	**MCLK Lock (Status)** • 0 = The MCLK is 'unlocked'. • 1 = The MCLK is 'locked'.	Read	N/A
12:1	PNLCLK_Lock	**PNLCLK Lock (Status)** • 0 = The PNLCLK is 'unlocked'. • 1 = The PNLCLK is 'locked'.	Read	N/A
12:0	DPA_Lock	**Dynamic Phase Adjust Lock (Status)** • 0 = The DPA is 'unlocked'. • 1 = The DPA is 'locked'.	Read	N/A

4.5.16 Registers 13h-1Fh: Reserved

These registers are reserved.

4.5.17 Register 20h: PNLCLK-M

The PNLCLK-M Register is used to divide the reference frequency provided to the PNLCLK PLL. The 'M' value is used to determine the output frequency of the PLL as specified in the equation given in Section 4.5.18, "Register 21h: PNLCLK-N".

Table 4-18. PNLCLK-M Register

Bit	Bit Name	Bit Definition	Access	Reset
20:7-20:0	PNLCLK_M [7-0]	**PNLCLK_M (Reference Divider) [7-0]** • Used as the variable 'M' in the frequency equation given in Section 4.5.18, "Register 21h: PNLCLK-N". • DB-PK. These bits take effect after writing xA to Reg 2Dh, bits 3:0	R/W	0

4.5.18 Register 21h: PNLCLK-N

The PNLCLK-N Register is used to determine the output frequency of the PNLCLK.

Table 4-19. PNLCLK-N Register

Bit	Bit Name	Bit Definition	Access	Reset
21:7-21:0	PNLCLK_N [7-0]	**PNLCLK_N (Feedback Divider) [7-0]** • Used as the variable 'N' in the frequency equation for the PNLCLK. • DB-PK. These bits take effect after writing xA to Reg 2Dh, bits 3:0	R/W	0

To determine the PNLCLK frequency (which is in units of MHz), use the following equation:

$$F_{PNLCLK} = \frac{OSC \times (N + 8)}{(M + 2)}$$

4.5.19 Register 22h: PNLCLK-SS0

The PNLCLK-SS0 (PNLCLK Spread-Spectrum Counter 0) Register is used in combination with the PNLCLK-SS1 Register to specify the amount of clock spread.

Table 4-20. PNLCLK-SS0 Register

Bit	Bit Name	Bit Definition	Access	Reset
22:7-22:0	PNLCLK_SS0 [7-0]	**PNLCLK Spread-Spectrum (Counter) 0 [7-0]** • These bits are the least-significant bits [7-0] for the PNLCLK spread-spectrum counter • DB-PK. These bits take effect after writing xA to Reg 2Dh, bits 3:0	R/W	0

4.5.20 Register 23h: PNLCLK-SS1

The PNLCLK-SS1 (PNLCLK Spread-Spectrum Counter 1) Register is used in combination with the PNLCLK-SS0 Register.

Table 4-21. PNLCLK-SS1 Register

Bit	Bit Name	Bit Definition	Access	Reset
23:7-23:4	Reserved	**Reserved**	–	0
23:3-23:0	PNLCLK_SS1 [3-0]	**PNLCLK Spread-Spectrum (Counter) 1 [3-0].** • These bits are the most-significant bits [11-8] for the PNLCLK spread-spectrum counter. • DB-PK. These bits take effect after writing xA to Reg 2Dh, bits 3:0.	R/W	0

4.5.21 Register 24h: PNLCLK-SSOE

The PNLCLK-SSOE (PNLCLK Spread-Spectrum Output Enable) Register is used to control the gain of the PNLCLK PFD and spread spectrum.

Table 4-22. PNLCLK-SSOE Register

Bit	Bit Name	Bit Definition	Access	Reset
24:7-24:6	PNLCLK_SS [1-0]	**PNLCLK Spread-Spectrum (Gain Select) [1-0]** – 0 = The gain is 1 – 1 = The gain is 2 – 2 = The gain is 4 – 3 = The gain is 8 • DB-PK. These bits take effect after writing xA to Reg 2Dh, bits 3:0	R/W	0
24:5	Reserved	**Reserved**	–	0
24:4-24:2	PNLCLK_PFD [2-0]	**PNLCLK Phase/Frequency Detector (Gain Select) [2-0]** – 0 = Gain is 1 – 1 = Gain is 2 – 2 = Gain is 4 – 3 = Gain is 8 – 4 = Gain is 16, and so forth. • DB-PK. These bits take effect after xA is written to Reg 2Dh, bits 3:0.	R/W	0
24:1-24:0	PNLCLK_OSD [1-0]	**PNLCLK Output Scaler Divider (Value) [1-0].** – 0 = Division is by 1 – 1 = Division is by 2 – 2 = Division is by 4 – 3 = Division is by 8 • DB-PK. These bits take effect after xA is written to Reg 2Dh, bits 3:0.	R/W	0

4.5.22 Register 25h: PNLCLK-OE

The PNLCLK-OE (PNLCLK Output Enable) Register is used to enable the PNLCLK output and spread-spectrum functionality.

Table 4-23. PNLCLK-OE Register

Bit	Bit Name	Bit Definition	Access	Reset
25:7-25:3	Reserved	**Reserved**	–	0
25:2	CLK_SEL	**Clock Selection.** This bit selects the input to the PNLCLK phase-lock loop • 0 = Frequency input is from the crystal input • 1 = Frequency input is from ADC_CLK, divided by 16	R/W	0
25:1	PNLCLK_SSENB	**PNLCLK Spread-Spectrum Enable.** • 0 = Disable PNLCLK spread-spectrum functionality • 1 = Enable PNLCLK spread-spectrum functionality	R/W	0
25:0	PNLCLK_OE	**PNLCLK Output Enable.** • 0 = Disable PNLCLK output • 1 = Enable PNLCLK output	R/W	0

4.5.23 Register 26h: MCLK-M

The MCLK-M Register is used to divide the reference frequency provided to the MCLK PLL. The 'M' value is used to determine the output frequency of the PLL as specified in the equation given in Section 4.5.24, "Register 27h: MCLK-N".

Table 4-24. MCLK-M Register

Bit	Bit Name	Bit Definition	Access	Reset
26:7-26:0	MCLK_M [7-0]	**MCLK M (Reference Divider) [7-0].** • The value in this register is used as the variable 'M' in the frequency equation given in Section 4.5.24, "Register 27h: MCLK-N". • DB-MK. Takes effect after 5x is written to Reg 2Dh, bits 7:4.	R/W	0

4.5.24 Register 27h: MCLK-N

The MCLK-N Register is used to determine the output frequency of the MCLK.

Table 4-25. MCLK-N Register

Bit	Bit Name	Bit Definition	Access	Reset
27:7-27:0	MCLK_N [7-0]	**MCLK N (Feedback Divider) [7-0].** • The value in this register is used as the variable 'N' in the frequency equation for the MCLK. • DB-MK. Takes effect after 5x is written to Reg 2Dh, bits 7:4.	R/W	0

To determine the MCLK frequency (which is in units of MHz), use the following equation:

$$F_{MCLK} = \frac{OSC \times (N + 8)}{(M + 2)}$$

4.5.25 Register 28h: MCLK-SS0

The MCLK-SS0 (MCLK Spread-Spectrum Counter 0) Register is used in combination with the MCLK-SS1 Register to specify the amount of clock spread.

Table 4-26. MCLK-SS0 Register

Bit	Bit Name	Bit Definition	Access	Reset
28:7-28:0	MCLK_SS0 [7-0]	**MCLK Spread-Spectrum (Counter) 0 [7-0]** • These bits are the least-significant bits [7-0] for the MCLK spread-spectrum counter • DB-MK. These bits take effect after writing 5x to Reg 2Dh, bits 7:4	R/W	0

4.5.26 Register 29h: MCLK-SS1

The MCLK-SS1 (MCLK Spread-Spectrum Counter 1) Register is used in combination with the MCLK-SS0 Register.

Table 4-27. MCLK-SS1 Register

Bit	Bit Name	Bit Definition	Access	Reset
29:7-29:4	Reserved	**Reserved**	–	0
29:3-29:0	MCLK_SS1 [3-0]	**MCLK Spread-Spectrum (Counter) 1 [3-0]** • These bits are the most-significant bits [11-8] for the MCLK spread-spectrum counter • DB-MK. These bits take effect after writing 5x to Reg 2Dh, bits 7:4	R/W	0

4.5.27 Register 2Ah: MCLK-SSOE

The MCLK-SSOE (MCLK Spread Spectrum Output Enable) Register is used to control the gain of the MCLK PFD and spread spectrum.

Table 4-28. MCLK-SSOE Register

Bit	Bit Name	Bit Definition	Access	Reset
2A:7-2A:6	MCLK_SS [1-0]	**MCLK Spread-Spectrum (Gain Select) [1-0]** – 0 = The gain is 1 – 1 = The gain is 2 – 2 = The gain is 4 – 3 = The gain is 8 • DB-MK. These bits take effect after writing 5x to Reg 2Dh, bits 7:4	R/W	0
2A:5	Reserved	**Reserved**	–	0
2A:4-2A:2	MCLK_PFD [2-0]	**MCLK Phase/Frequency Detector (Gain Select) [2-0]** – 0 = The gain is 1 – 1 = The gain is 2 – 2 = The gain is 4 – 3 = The gain is 8 – 4 = The gain is 16, and so forth. • DB-MK. These bits take effect after writing 5x to Reg 2Dh, bits 7:4	R/W	0
2A:1-2A:0	MCLK_OSD [1-0]	**MCLK Output Scaler Divider [1-0].** – 0 = Division is by 1 – 1 = Division is by 2 – 2 = Division is by 4 – 3 = Division is by 8 • DB-MK. These bits take effect after writing 5x to Reg 2Dh, bits 7:4	R/W	0

4.5.28 Register 2Bh: MCLK-OE

The MCLK-OE (MCLK Output Enable) Register is used to enable the MCLK output and spread-spectrum functionality.

Table 4-29. MCLK-OE Register

Bit	Bit Name	Bit Definition	Access	Reset
2B:7-2B:2	Reserved	**Reserved**	–	0
2B:1	MCLK_SSENB	**MCLK Spread-Spectrum Enable.** • 0 = Disable MCLK spread-spectrum functionality. • 1 = Enable MCLK spread-spectrum functionality.	R/W	0
2B:0	MCLK_OE	**MCLK Output Enable.** • 0 = Disable MCLK output. • 1 = Enable MCLK output.	R/W	0

4.5.29 Register 2Ch: OUTPUT MUX

The OUTPUT MUX Register is used to select the source for the REF pin and STATUS pin (an active-low pin formerly called ‘LOCK’).

Table 4-30 refers to ADC_FUNC, an internally generated signal that is delayed so it is in the same domain as the internal ADC_CLK signal. Functionally, depending on the setting of Reg 06:3, ADC_FUNC is equivalent to either ADCSYNC (which provides recovered HSYNC) or the input HSYNC.

Table 4-30. OUTPUT MUX Register

Bit	Bit Name	Bit Definition	Access	Reset
2C:7	High_Drive	**High Drive (ADC Digital Outputs) Disable** • 0 = Drive strength is normal. • 1 = Drive strength is half of normal	R/W	0
2C:6	OE_OSC	**Output Enable for OSCOUT** • 0 = Disable OSCOUT output • 1 = Enable OSCOUT output	R/W	1
2C:5-2C:4	OSC_Sel [1-0]	**OSCOUT (Multiplexer) Select [1-0]** • 0 = The OSCOUT source is OSC. • 1 = The OSCOUT source is OSCDIVIDER. • 2 = The OSCOUT source is OSC/2. • 3 = Reserved	R/W	0

Table 4-30. OUTPUT MUX Register

Bit	Bit Name	Bit Definition	Access	Reset
2C:3	Reserved	**Reserved**	–	0
2C:2	REF_Sel	**REF (Status) Select.** This bit selects the REF pin reference output. • 0 = The REF output source is from the input to the pixel PLL PDINPUT (the Phase/Frequency Detector Input). • 1 = The REF output source is from ADC_FUNC. (For more information on ADC_FUNC, see Section 4.5.7, "Register 06h: Output Enables".)	R/W	0
2C:1-2C:0	LCKSEL [1-0]	**(PLL) Lock (Status) Select [1-0].** These bits select the lock status output for the active-low STATUS pin • 0 = Status pin output is for the Pixel PLL • 1 = Status pin output is for the MCLK: Memory Clock • 2 = Status pin output is for the DPA: Dynamic Phase Adjust • 3 = Status pin output is for the PNLCLK: Panel Clock	R/W	1

4.5.30 Register 2Dh: PLL Reset

The PLL Reset (Phase-Locked Loop Reset) Register is used to reset the MCLK and PNLCLK PLLs.

Table 4-31. PLL Reset Register

Bit	Bit Name	Bit Definition	Access	Reset
2D:7-2D:4	MCLK_Reset [3-0]	**MCLK Reset [3-0]** Writing 5xh to these bits resets MCLK PLL • Loads working Regs 26h to 2Bh	Write	N/A
2D:3-2D:0	PNLCLK_Reset [3-0]	**PNLCLK Reset [3-0]** Writing xAh to these bits resets PNLCLK PLL • Loads working Regs 20h to 25h	Write	N/A

4.5.31 Register 2Eh-2Fh: Reserved

These registers are reserved.

4.5.32 Register 30h: ADC CTRL

The ADC CTRL (Analog-to-Digital Converter Control) Register is used to control the ADC.

Table 4-32. ADC CTRL Register

Bit	Bit Name	Bit Definition	Access	Reset
30:7	ADC_OE	**Analog-to-Digital Converter (Digital) Outputs Enable** • 0 = The ADC digital outputs are disabled and are high-impedance • 1 = The ADC digital outputs are enabled	R/W	0
30:6	ADCRCLK_Inv	**Invert ADCRCLK** • 0 = Non-inverted – ADC Data is to be latched on the rising edge of ADCRCLK • 1= Inverted – ADC Data is to be latched on the falling edge of ADCRCLK	R/W	0
30:5	Force_ADC	**Force Analog-to-Digital Converter (Outputs).** • 0 = Normal operation • 1 = Force all ADC output buffers low or high. – Reg 30:5 = 0 to force buffers low – Reg 30:5 = 1 to force buffers high	R/W	0
30:4	ADC_CLK_D	**ADCRCLK Delay** Delay the ADCRCLK signal relative to start of data by one pixel clock. • This has the effect of swapping data between the A and B channels	R/W	2
30:3	ADC_Inv	**Analog-to-Digital Converter (Output) Invert (Disable)** • 0 = The ADC outputs are inverted • 1 = The ADC outputs are not inverted	R/W	1
30:2~1	CLAMP_Sel	**Clamp (Source) Select** This bit selects the source of the signal to a clamp • 0 =External CLAMP pin • 1 =Reserved • 2 =Internal (ADC_SYNC) • 3 =Reserved	R/W	0
30:0	CLAMP_Pol	**Clamp Polarity** • 0 = The polarity of the signal to a clamp is positive • 1 = The polarity of the signal to a clamp is negative	R/W	0

4.5.33 Register 31h: R_Control

Table 4-33. R_CONTROL Register

Bit	Bit Name	Bit Definition	Access	Reset
31:7	R_VIN_Range	**Red Input Voltage Range** (0 = 700mV 1 = 1 Volt	R/W	0
31:6	Reserved	Reserved	R/W	0
31:5	R_CLAMP_T3	**Red Clamp T3 Time Constant** 0 = Nominal 1 = 0.3 Nominal	R/W	1
31:4	R_CLAMP_Type	**Soft/Xhard Clamp Function**	R/W	0
31:3	R_CLAMP_T5	**Red Clamp T5 Time Constant** 0 = Nominal 1 = 0.5 Nominal	R/W	0
31:2-31:1	Reserved	Reserved	-	0
31:0	XPD_R	**Red Channel Power Down** 0 = Red ADC Channel Disabled 1 = Red ADC Channel Enabled	R/W	0

4.5.34 Register 32h: G_Control

Table 4-34. G_CONTROL Register

Bit	Bit Name	Bit Definition	Access	Reset
32:7	G_VIN_Range	**Green Input Voltage Range** (0 = 700mV 1 = 1 Volt	R/W	0
32:6	Reserved	Reserved	R/W	0
32:5	G_CLAMP_T3	**Green Clamp T3 Time Constant** 0 = Nominal 1 = 0.3 Nominal	R/W	1
32:4	G_CLAMP_Type	**Soft/Xhard Clamp Function**	R/W	0
32:3	G_CLAMP_T5	**Green Clamp T5 Time Constant** 0 = Nominal 1 = 0.5 Nominal	R/W	0
32:2	Reserved	Reserved	-	0
32:1	SOG_EN	**Enable Sync on Green Compensation** This will compensate the Green channel for ~300 mv level shift seen on Sync on Green signals 0 = No level Shift 1 = Enable -300mv shift on the Analog Green input	R/W	0
32:0	XPD_G	**Green Channel Power Down** 0 = Green ADC Channel Disabled 1 = Green ADC Channel Enabled	R/W	0

4.5.35 Register 33h: B_Control.

Table 4-35. B_CONTROL Register

Bit	Bit Name	Bit Definition	Access	Reset
33:7	B_VIN_Range	**Blue Input Voltage Range** (0 = 700mV 1 = 1 Volt	R/W	0
33:6	Reserved	Reserved	R/W	0
33:5	B_CLAMP_T3	**Blue Clamp T3 Time Constant** 0 = Nominal 1 = 0.3 Nominal	R/W	1
33:4	B_CLAMP_Type	**Soft/Xhard Clamp Function**	R/W	0
33:3	B_CLAMP_T5	**Blue Clamp T5 Time Constant** 0 = Nominal 1 = 0.5 Nominal	R/W	0
33:2-33:1	Reserved	Reserved	-	0
33:0	XPD_B	**Blue Channel Power Down** 0 = Blue ADC Channel Disabled 1 = Blue ADC Channel Enabled	R/W	0

4.5.36 Register 34h: R_Gain

Table 4-36. R_GAIN Register

Bit	Bit Name	Bit Definition	Access	Reset
33:7-33:5	R_PGA_Gain	**Adjust Video Amp Gain for red channel of ADC**	R/W	0
33:4-33:0	R_ADC_Gain	**Fine adjust red channel ADC ladder voltage**	R/W	0

4.5.37 Register 35h: G_Gain

Table 4-37. G_GAIN Register

Bit	Bit Name	Bit Definition	Access	Reset
35:7-35:5	G_PGA_Gain	**Adjust Video Amp Gain for green channel of ADC**	R/W	0
35:4-35:0	G_ADC_Gain	**Fine adjust green channel ADC ladder voltage**	R/W	0

4.5.38 Register 36h: B_Gain

Table 4-38. B_GAIN Register

Bit	Bit Name	Bit Definition	Access	Reset
36:7-36:5	B_PGA_Gain	**Adjust Video Amp Gain for blue channel of ADC**	R/W	0
36:4-36:0	B_ADC_Gain	**Fine adjust blue channel ADC ladder voltage**	R/W	0

4.5.39 Register 37h: PSEL.

Table 4-39. PSEL Register

Bit	Bit Name	Bit Definition	Access	Reset
37:7-37:4	BG_CAL	**Bandgap Calibration** **NOTE:** MSB = Bit 4, LSB = Bit 7 1111=Maximum value, 0000=Minimum Value	R/W	0
37:3	XBG_PD	**Bandgap Power Down Enable** • 1 = The Bandgap voltage generator functions normally • 0 = The Bandgap voltage generator is powered down	R/W	1
37:2	PSEL3	**Programmable Select 3** This bit controls general-purpose pin PSEL3	R/W	0
37:1	PSEL2	**Programmable Select 2** This bit controls general-purpose pin PSEL2	R/W	0
37:0	PSEL1	**Programmable Select 1** This bit controls general-purpose pin PSEL1	R/W	0

4.5.40 Register 38h: R_OFFSET

Table 4-40. R_OFFSET Register

Bit	Bit Name	Bit Definition	Access	Reset
38:7-38:0	R_Offset[7-0]	**Red Offset Adjust [7-0].** These bits adjust the amount of code offset on the red channel • 80 = Zero Offset • Values greater than 80h result in a positive offset • Values less than 80h result in a negative offset	R/W	80

Register 39h: G_OFFSET

Table 4-41. G_OFFSET Register

Bit	Bit Name	Bit Definition	Access	Reset
39:7-39:0	G_Offset[7-0]	**Green Offset Adjust [7-0].** These bits adjust the amount of code offset on the green channel • 80 = Zero Offset • Values greater than 80h result in a positive offset • Values less than 80h result in a negative offset	R/W	80

Register 3Ah: B_OFFSET

Table 4-42. B_OFFSET Register

Bit	Bit Name	Bit Definition	Access	Reset
3A:7-3A:0	R_Offset[7-0]	**Blue Offset Adjust [7-0].** These bits adjust the amount of code offset on the blue channel • 80 = Zero Offset • Values greater than 80h result in a positive offset • Values less than 80h result in a negative offset	R/W	80

Register 3Bh: IBIAS

Table 4-43. IBIAS Register

Bit	Bit Name	Bit Definition	Access	Reset
3B:7-3B:6	IBias_Buf[1-0]	**ADC BUFFER BIAS Adjustment [1-0]**	R/W	2
3B:5-3B:4	IBias VA[1-0]	**Video Amplifier BIAS Adjustment [1-0]**	R/W	2
3B:3-3B:0	IBias ADC[3-0]	**ADC BIAS Adjustment [3-0]**	R/W	Ah

Register 3Ch: TEST_MUX

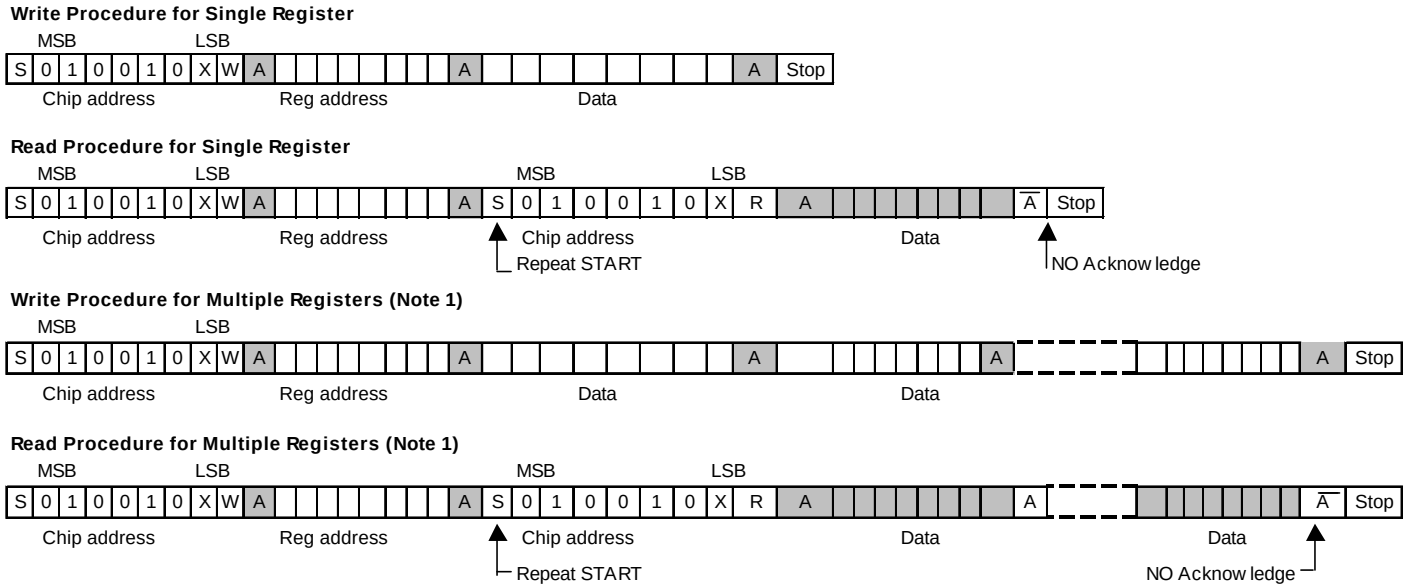
Table 4-44. TEST_MUX Register

Bit	Bit Name	Bit Definition	Access	Reset
3B:7-3B:3	CH_TEST[4-0]	**Channel Test Mux**	R/W	2
3B:2-3B:0	BG_TEST[2-0]	**Bandgap Test Mux**	R/W	Ah

Chapter 5 Programming

5.1 I2C Serial Bus: Data Format

Figure 5-1. ICS1532 Data Format for I2C Serial Bus



Legend

All values are transmitted with the most-significant bit (MSB) first and least-significant bit (LSB) last.

A = ACK = Acknowledge = 0	$\overline{A}$ = NAK = No Acknowlege = 1
R = Read = 1	W = Write = 0
S = Start	X = Bit value that equals logic state of SBADR pin.

= (Dashed Line) Multiple transactions

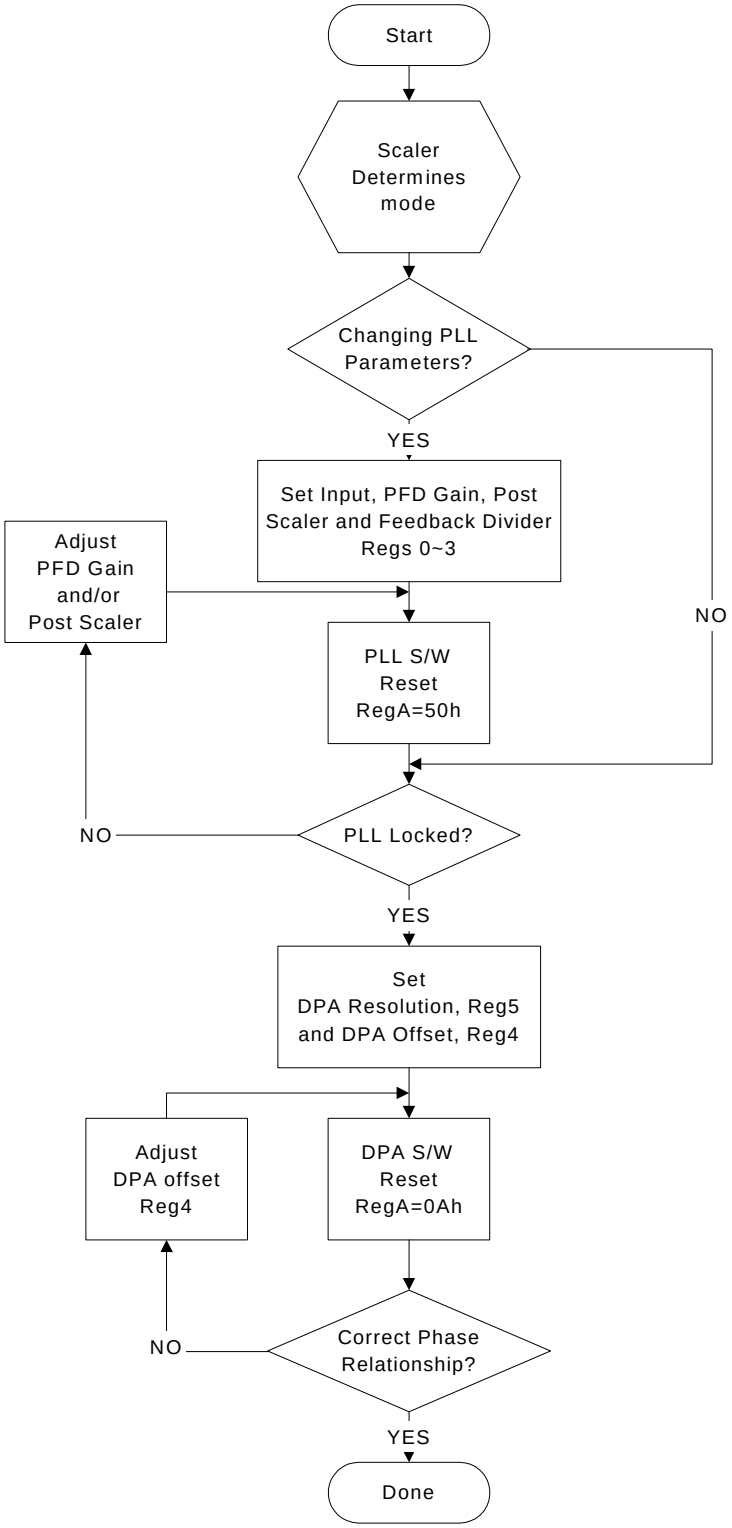
Master device drives signal to ICS153x ICS153x drives signal to master device

Note: In general, the:

- Lower nibble of the I2C register automatically increments after each successive data byte is written to or read from the ICS1532.
- Upper nibble of the I2C register does not automatically increment, and the software must explicitly re-address the ICS1532. As a result, to write or read all the ICS1532 registers, the software:
  - Must NOT index 0 and then do 64 one-byte transactions.
  - Must break the transactions into at least four separate bus transactions:
    (1) 00 to 0F (2) 10 to 1F (3) 20 to 2F (4) 30 to 3F

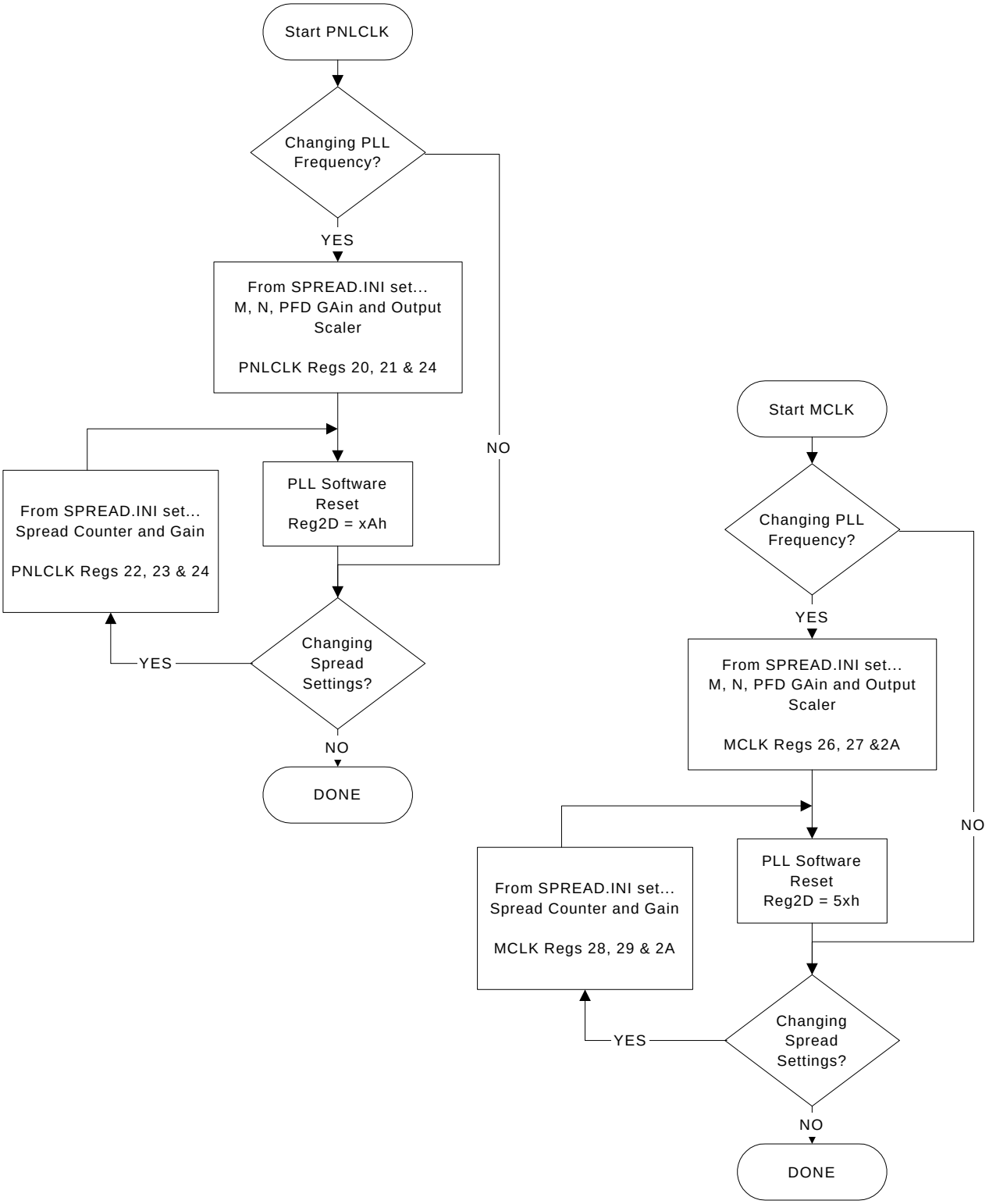
5.2 Programming Flow for Modifying PLL and DPA Settings

Figure 5-2. ICS1532 Flow for Capture/Input Clock PLL



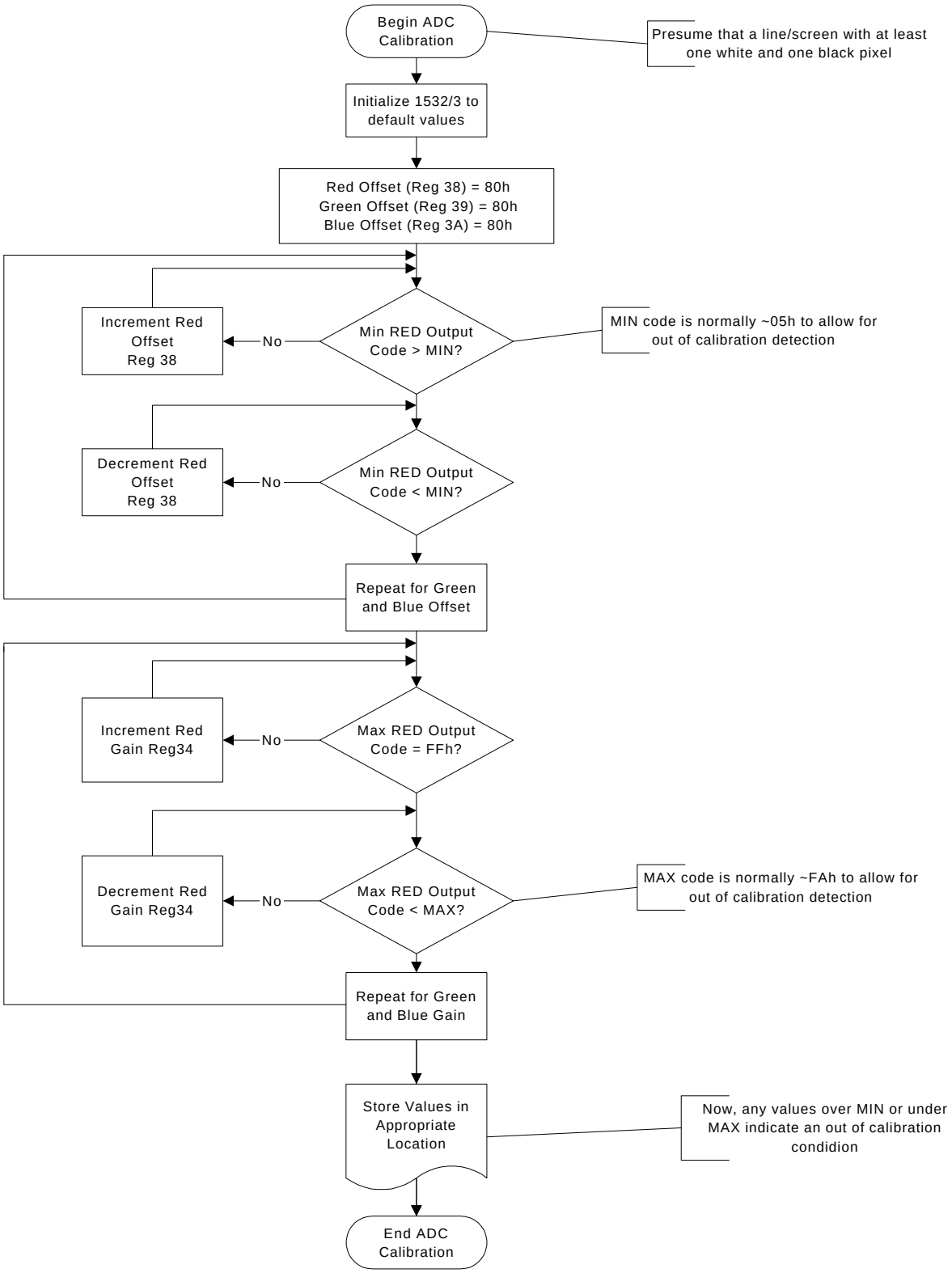
5.2.1 Programming Flow for Modifying Settings for Spread Spectrum

Figure 5-3. ICS1532 Flow for PNLCLK and MCLK PLL Spread-Spectrum Settings



5.2.2 Programming Flow for Calibrating

Figure 5-4. ICS1532 Flow for ADC Calibration



Chapter 6 AC/DC Operating Conditions

Values in this chapter are preliminary and subject to change.

6.1 Absolute Maximum Ratings

Table 6-1 lists absolute maximum ratings for the ICS1532. Stresses above these ratings can cause permanent damage to the ICS1532. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the ICS1532 at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 6-1. ICS1532 Absolute Maximum Ratings

Item	Rating
VDD, VDDQ (See Note)	4.3 V
VDDxADC (See Note)	3.6 V
Digital Inputs	VSS -0.3 V to +5.5 V
Digital Outputs	VSSQ -0.3 V to VDDQ +0.3 V
Analog Inputs	VSS -0.3 V to +5.5 V
Analog Outputs	VSSA -0.3 V to VDDA +0.3 V
Storage Temperature	-65 to +150° C
Junction Temperature	175° C
Soldering Temperature	260° C

Note: Measured with respect to VSS. During normal operations, the VDD supply voltage for the ICS1532 must remain within the recommended operating conditions.

6.2 Recommended Operating Conditions

Table 6-2. ICS1532 Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Units
Ambient Operating Temperature	0	–	+70	° C
3.3 Power Supply Voltage	+3.15	+3.3	+3.45	V
2.5 Volt Power Supply Voltage	+2.35	+2.5	+2.65	V

6.3 Power Dissipation Values

Table 6-3. ICS1532 Power Dissipation Values

Item	Conditions	Typical	
Power Dissipation, Active	Nominal	ICS1532 (140 MHz):	800 mW
		ICS1532 (165 MHz):	850 mW
		ICS1532 (205 MHz):	900 mW
Power Dissipation, Standby	Nominal	<250 mW	

6.4 AC Operating Characteristics

Table 6-4. AC Operating Characteristics for ICS1532 Inputs

Parameter	Symbol	Min.	Max.	Units
Input HSYNC: Input Frequency	f_{HSYNC}	12	120	kHz
PDEN: Input Frequency	f_{PDEN}	30	120	Hz

6.5 DC Operating Characteristics

Table 6-5. DC Operating Characteristics

Parameter	Symbol	Conditions	Notes	Min.	Typ.	Max.	Units
Operating Characteristics for Supply Current							
Supply Current, Digital	IDDD	VDDD = 3.3 V, 140 MHz	1	–	135	tbd	mA
3.3V Supply Current, Analog	IDDA	VDDA = 3.3 V, 140 MHz	1	–	125	tbd	mA
2.5V Supply Current, Analog	IDDA2.5	VDDA = 2.5 V, 140 MHz	1	–	125	tbd	mA
Operating Characteristics for Digital TTL Inputs							
Input High Voltage	V_{IH}	–	2	2.4	–	–	V
Input Low Voltage	V_{IL}	–	2	–	–	0.8	V
Input High Current	I_{IH}	V_{IH} = VDD	1, 2	–	–	±10	µA
Input Low Current	I_{IL}	V_{IL} = 0	2	±10	–	–	µA
Input Capacitance	C_{in}	–	3	–	10	–	pF
Operating Characteristics for Digital TTL Outputs							
Output Low Voltage	V_{OL}	I_{OUT} = 3 mA	4	–	–	0.4	V

Note:

1. All VDD measurements are taken with respect to VSS (which equals 0 V).
   a. IDDD is the current through VDDD
   b. IDDA is the current through VDDA
   c. IDDA is the current through VDDAADC (2.5)
2. These DC operating characteristics apply to the following ICS1532 TTL input pins: HSYNC, PDEN, SCL, SDA.
3. Typically guaranteed by design.
4. This DC operating characteristic applies only to the SDA pin when it is in output mode.

Chapter 7 Timing Diagrams

7.1 AC Timing Diagrams

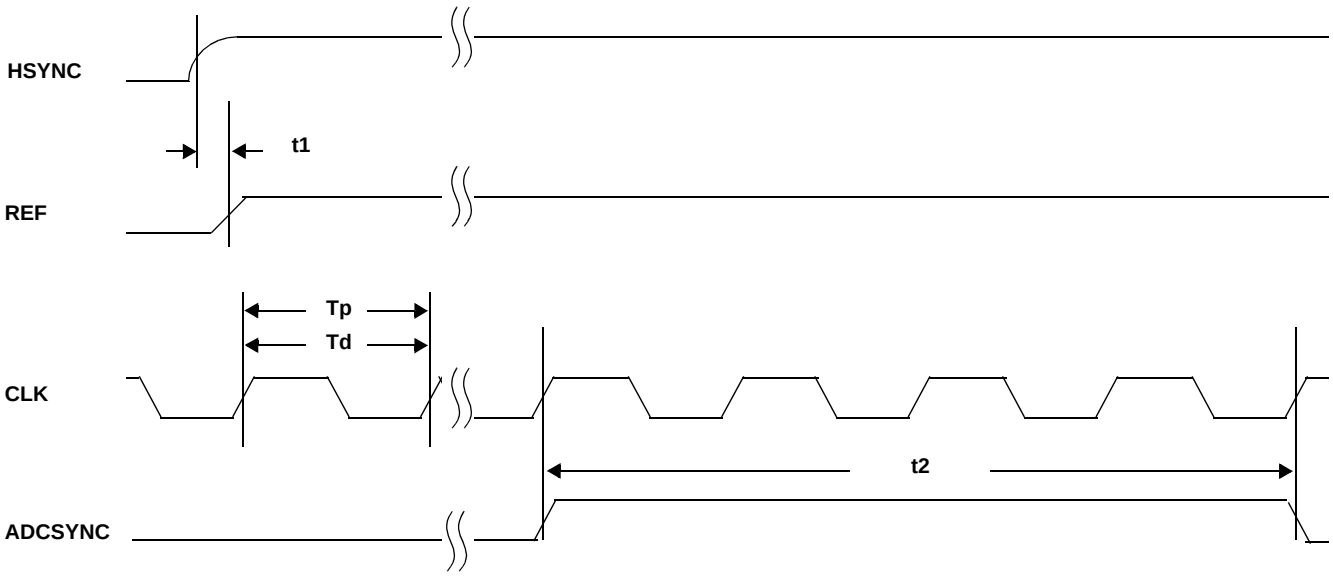
7.1.1 Phase-Locked-Loop Timing for Digital Setup and Hold

The input HSYNC signal is used to generate the REF output signal. In the Phase/Frequency Detector, the REF signal is compared with ADCSYNC (which provides the recovered HSYNC signal). Table 7-1 gives the timing for these signals, and Figure 7-1 shows timing characteristics.

Table 7-1. Phase-Locked-Loop Timing

Time Period	Timing Description	Min	Typ	Max	Units
t1	Input HSYNC Rise Time to REF Rise Time	TBD	7	TBD	ns
Tp	Clock Period		$Tp = \frac{\text{Input HSYNC Frequency}}{\text{Result from Reg 02 and 03}}$		ns
Td	Clock Duty Cycle	45-55	50-50	55-45	%
t2	ADCSYNC Active Time		4 × Tp		ns

Figure 7-1. Timing for Phase-Locked Loop



7.1.2 Two-Pixels-per-Clock Mode Timing

For 2-pixels-per-clock mode, Reg 30:6 must be cleared to '0'. Table 7-2 lists pixel characteristics for this mode, as determined by Reg 2:0. (The 'A' channel pixels are pipelined and align with an ADCRCLK rising edge, whereas 'B' channel pixels are pipelined and align with an ADCRCLK falling edge.) Table 7-3 lists time measures for this mode, and Figure 7-2 shows timing characteristics.

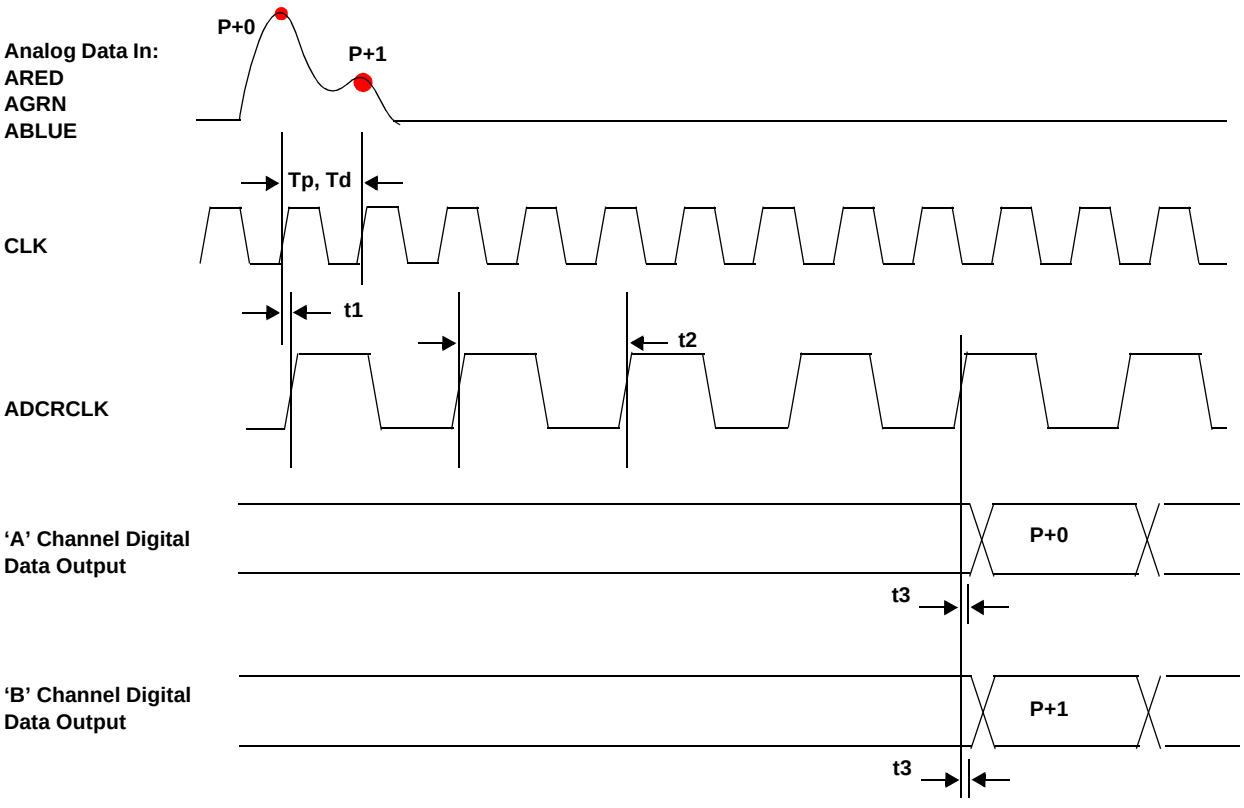
Table 7-2. Pixel Characteristics for 2-Pixels-per-Clock Mode

Reg 2:0 Setting	Pixel Characteristics When Reg 30:6 is Cleared to '0'		
	Total Number of Pixels	**Pixel Output (P + *x*)**	**What the Pixels Represent**
0	Total number is even.	Output is on Channel 'A'.	Samples on half-rate ADCRCLK's rising edge.
1	Total number is odd.	Output is on Channel 'B'.	Samples on half-rate ADCRCLK's falling edge.

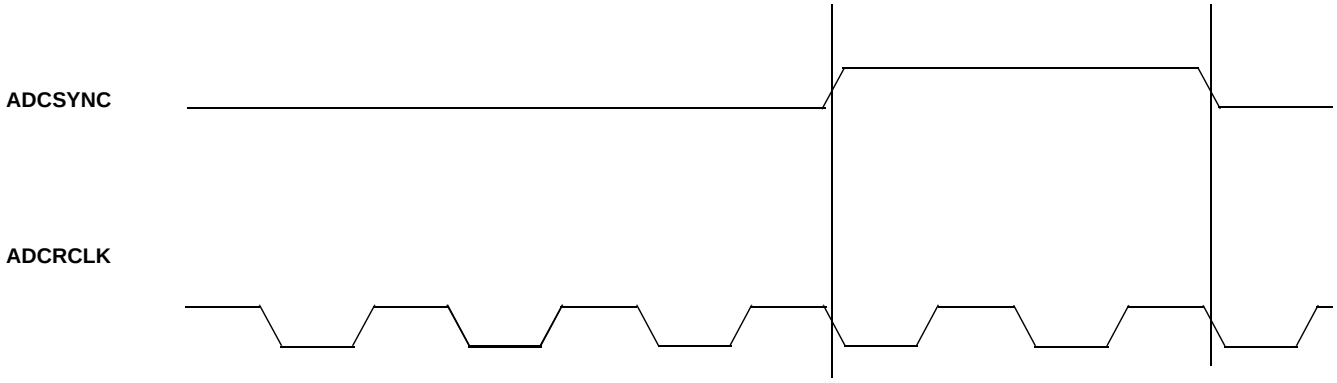
Table 7-3. Timing for 2-Pixels-per-Clock Mode

Time Period	Timing Description	Min	Typ	Max	Units
Tp, Td	CLK Period, CLK Duty Cycle	–	See Table 7-1.	–	ns
t1	CLK Rise Time to ADCRCLK Rise Time	–	2.6	–	ns
t2	ACDRCLK Period	–	t2 = 2 × Tp	–	ns
t3	Digital Data Transition, A Channel	TBD	3.5	TBD	ns

Figure 7-2. AC Timing for 2-Pixels-per-Clock Mode



7.1.3 ADCRCLK v.s. ADCSYNC Timing ADCRCLK v.s. ADCSYNC Edge Relationship



7.2 Resetting the 1532 to a known state

Below is shown the two ways to reset the 1532 to a known state.

7.2.1 Reset Pin Input

Momentarily bring the active high RESET# input pin low to cause the part to reset to a known state.

7.2.2 Power-On Reset (POR) Timing

The ICS1532 incorporates special internal power-on reset circuitry that requires no external reset signal.

To use the POR circuitry:

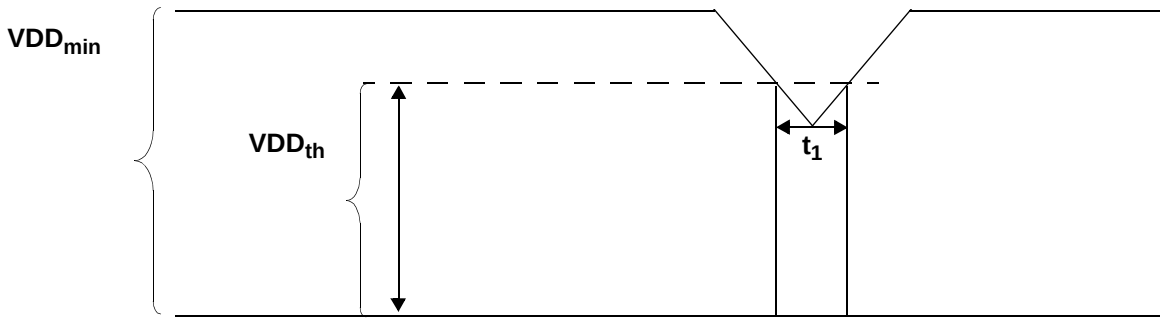
- Reduce the level of the all supply voltages to the ICS1532 (and the voltage seen on all ICS1532 pins) so that it is below the threshold voltage (VDD_{th}) of the POR circuit for the period t1 shown below
- Keep the supply voltage below that threshold voltage for time t1, such that power-conditioning capacitors for the printed circuit board are drained and the proper reset state is latched.

- A successful power-on reset results in all the ICS1532 registers having the appropriate reset values as stated in the tables in Chapter 4, “Register Set”.)

Table 7-4. ICS1532 POR Transition Times

Symbol	Timing Description	Min	Typ	Max	Units
VDD	Supply Voltage (‘On’ State)	3.15	3.3	3.45	V
VDD_{th}	Threshold Supply Voltage	–	1.8	–	V
t_1	Hold Time for Reset State	–	10	–	ms

Figure 7-3. Power-On Reset Condition for ICS1532



Chapter 8 Package Dimensions

This section gives the physical dimensions for the package for the ICS1532, which is a 144-pin LQFP.

- The lead count (N) for the package is 144 leads.
- The nominal footprint (that is the body) for the package is 20 mm × 20 mm × 1.4 mm.

Note:

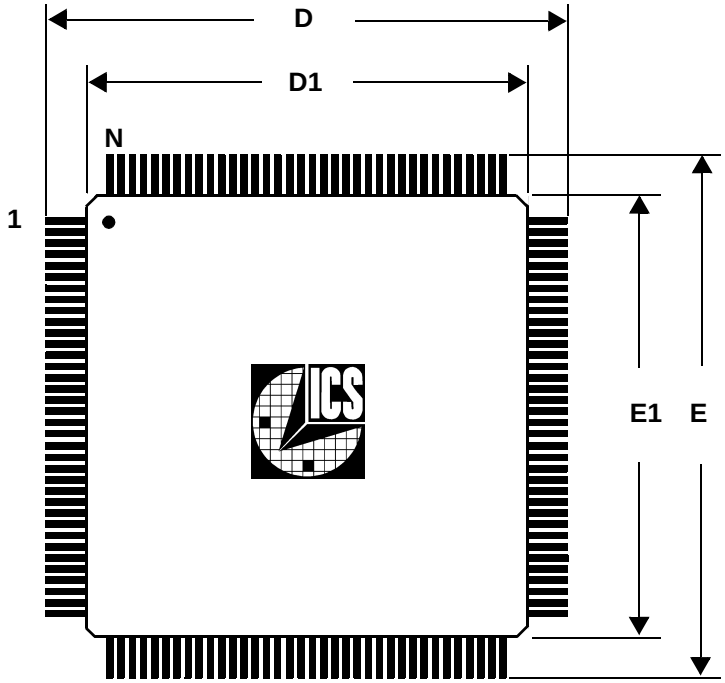
1. For full mechanical specifications, see JEDEC drawing number MS-026 Rev A.
2. Table 8-1 lists the ICS1532 physical dimensions. These dimensions are:
   a. For planning purposes only.
   b. Subject to change.
   c. Shown in Figure 8-1.

Table 8-1. Physical Dimensions for ICS1532

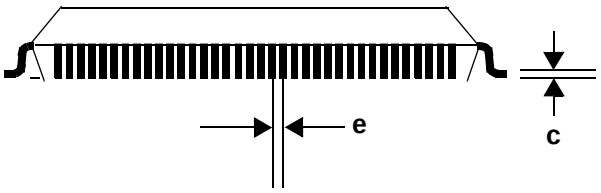
Symbol	Description	Min.	Nominal	Max.	Unit
A	Full Package Height	–	–	1.60	mm
A1	Package Body Standoff (the distance from the seating plane to the base plane of the package body)	0.05	–	0.15	mm
A2	Package Body Thickness	1.35	1.40	1.45	mm
b	Lead Width	0.17	0.22	0.27	mm
c	Lead Thickness	0.09	–	0.20	mm
D	Tip-to-Tip Dimension	–	22.0	–	mm
D1	Package Body Dimension	–	20.0	–	mm
e	Lead Pitch	–	0.50	–	mm
E	Tip-to-Tip Dimension	–	22.0	–	mm
E1	Package Body Dimension	–	20.0	–	mm
L	Lead Tip Length	0.45	0.60	0.75	mm
L1	Lead Length, Entire Length	–	1.0	–	mm
Θ	Lead Tip Angle	0	3.5	7	degrees

Figure 8-1. Physical Dimensions for ICS1532

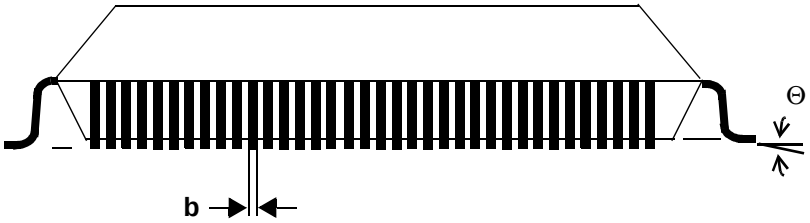
Top View



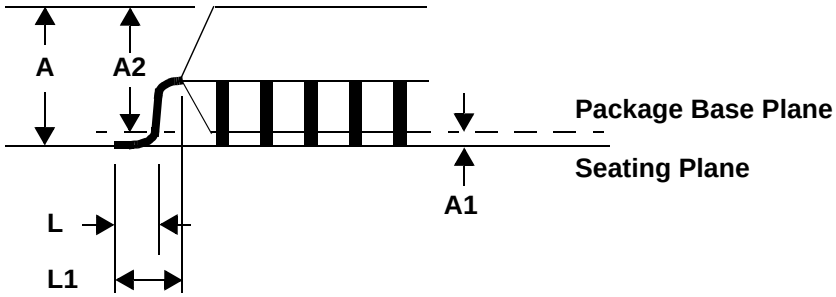
Side View



Detail View 1

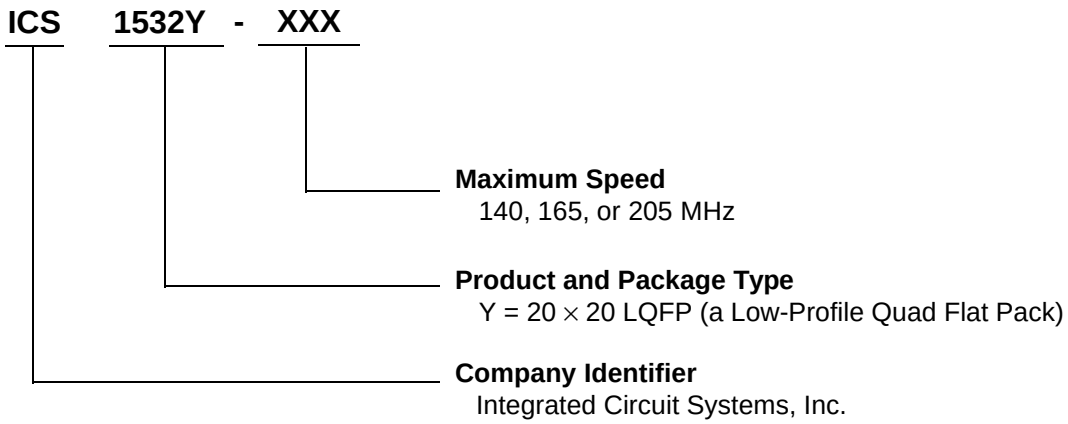


Detail View 2



Chapter 9 Ordering Information

Figure 9-1. ICS1532 Ordering Information



Revision

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