Crystal Oscillator

Series CPW

- *Factory Programmable*
- *Standard Package Options*
- *Also available in 1.8 V*

RoHS COMPLIANT 2002 / 95 / EC

Part Numbering Example: CPW C 1 L Z – A3 B6 - XX.XXXX TS

CPW	C	1	L	Z	A3	B6	XX.XXXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP	STABILITY	FREQUENCY	TRI-STATE
CPW	C=CMOS	3=3.2x2.5 Ceramic 5=3.2x5 Ceramic 7=5x7 Ceramic	L=3.3V R=2.5V Q=1.8V	Blank=Bulk T=Tube Z=Tape and Reel	A3=-40°C+85°C	B6=±100ppm BP=±50ppm	1.000~166.000 MHz	TS=Tri-State PD=PowrDwn

Specifications:

Description	Min	Typ	Max	Unit
Frequency Range: Programmable to Any Discrete Frequency	1.0		166.0	MHz
Available Stability Options:	-100 -50 -25		100 50 25	ppm ppm ppm
Programmable Supply Voltage: (1–133 MHz) (1–100 MHz)	3.0 2.2 1.6	3.3 2.5 1.8	3.6 2.8 2.0	V V V
Operating Temperature Range:	-40		+85	°C
Storage Temperature:	-55		+125	°C
Aging (PPM/Year) Ta=25C, Vdd=3.3V			±5	

Operating Conditions:

Description		Min	Max	Unit
Vdd	Supply Voltage	1.6	3.6	V
C_{CMOS}	Max Capacitive Load on outputs for CMOS levels		15	pF

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ELECTRICAL CHARACTERISTICS

Description	Test Conditions	Min	Typ	Max	Unit
Input Characteristics (Pin 1): V_{IL}, Low–Level Input Voltage TO DISABLE OUTPUT				0.2Vdd	V
V_{IH}, High–Level Input Voltage TO ENABLE OUTPUT OPEN		0.8VddV			V
I_{IL}, Input Low Current I_{IH}, Input High Current	V_{IN} = 0V V_{IN} =Vdd			10 10	µA µA
Output Characteristics: V_{OL}, Low–Level Output Voltage	1.8V-2.5V Vdd, 4mA I_{OL} 3.0V–3.6V Vdd, 8 mA I_{OL}			0.1Vdd 0.4	V
V_{OHCMOS}, High-level CMOS Voltage	1.8V-2.5V Vdd , 4mA I_{OL} 3.0V–3.6V Vdd, -8 mA I_{OL}	0.9 Vdd-0.4			V
Power Supply Current: (unloaded)	1 MHz ≤ f0 ≤ 25 MHz	3.5		4.0	mA
	25 MHz < f0 ≤ 50 MHz	5.0		6.5	mA
	50 MHz < f0 ≤ 75 MHz	6.0		8.5	mA
	75 MHz < f0 ≤ 100 MHz	7.0		10.5	mA
	100 MHz < f0 ≤ 125 MHz	8.5		12.5	mA
	125 MHz < f0 ≤ 166 MHz	10.0		15.0	mA
Standby Current:			10	50	pA
Pull-Up (Pin 1)	3.0 – 3.6 Vdd, VIN = 0V 3.0 – 3.6 Vdd, VIN = 0.7V	1.1 50	3.0 100	8.0 200	MΩ KΩ
Tri-State Leakage Current	3.3 Vdd			50	µA
Output Enable Mode:	Output is Tri-Stated				
Power Down Mode:	Output is Tri-Stated.				

OUTPUT CLOCK SWITCHING CHARACTERISTICS

Description	Test Conditions	Min	Typ	Max	Unit
Duty Cycle:		45		55	%
Output Clock Rise/Fall	15pF			1.5	ns
Start Up Time	From power on		5	10	ms
Power Down Delay Time					
Synchronous	PWR_DWN pin LOW to output Hi-Z			1.5T+100	ns
Asynchronous				100	ns
Output Disable Time					
Synchronous	OE pin LOW to output Hi-Z			1.5T+100	ns
Asynchronous	T = Frequency oscillator period			100	ns
Output Enable Time					
Synchronous	OE pin LOW to output Hi-Z			1.5T+100	ns
Asynchronous	T = Frequency oscillator period			100	ns
	< 33.000 MHz		6		ps
RMS Period Jitter:	> 33.000, MHz		7		ps
Peak to Peak *	< 33.000 MHz		80		ps
	> 33.000 MHz		60		ps

* Jitter tested at > 1,000,000 samples, exceeding JEDEC std JESD65.

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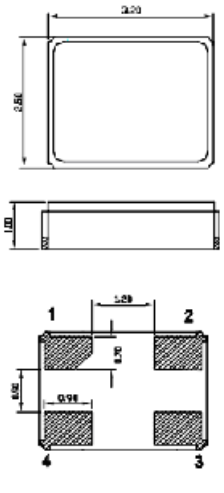
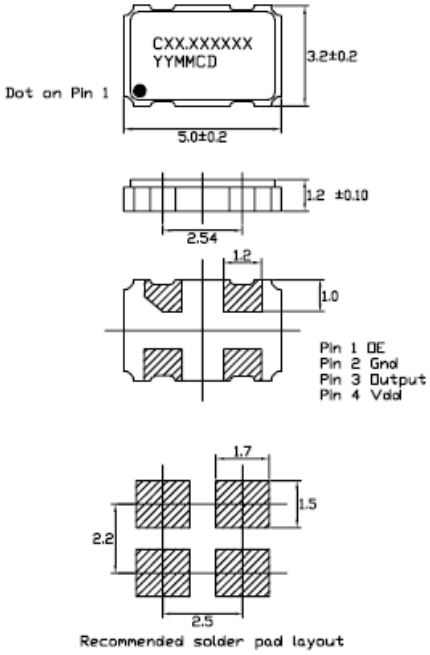
Note: Bypass Vdd to GND with a 0.01 µF capacitor

Style 3 3.2x2.5 Ceramic SMD

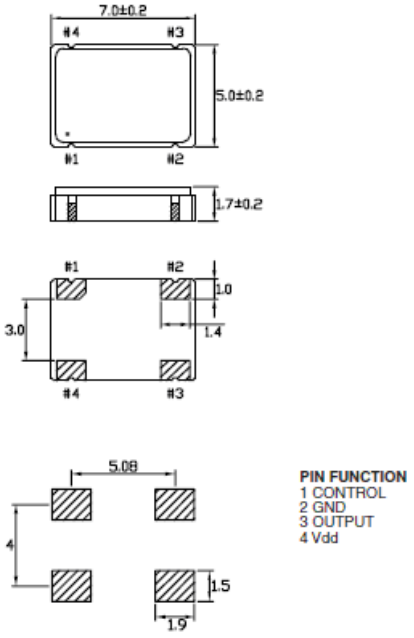


PIN FUNCTION
1 CONTROL
2 GND
3 OUTPUT
4 Vdd

Style 5 3.2x5 Ceramic SMD



Style 7 5x7 Ceramic SMD



PIN FUNCTION
1 CONTROL
2 GND
3 OUTPUT
4 Vdd