ADE-207-189 (Z)

HD153036TF

64-Mbps Single Chip Read Channel

HITACHI

Preliminary
1st. Edition
December 1995

Description

The HD153036TF is fully integrated single-chip Data Channel LSI for high performance magnetic disk drives. Function blocks include the automatic gain control (AGC) circuit, pulse detector, programmable filter, 4-burst servo demodulator, write clock synthesizer, data synchronizer, and 1,7RLL ENDEC with programmable write precompensation circuit. This LSI supports from 24 Mbit/s to 64 Mbit/s data rate, and can be ultilized for either single or multiple zone recording.

The HD153036TF is fabricated in HITACHI 1-3 µm Hi-BiCMOS process technology which yields a high performance device at low power consumption. In power down mode, power consumption is reduced to 5 mW.

General Features :

- 24 to 64 Mbit/s data transfer rate.
- A serial port for register access.
- User-selectable single zone recording or multiple zone recording options. The following are programmable for multiple zone recording : VCO center frequency (64 settings), Read-PLL loop filter dumping factor, charge pump current levels (16 settings), active filter cut-off frequency for servo and data modes (128 settings).
- Power Management system
  (Servo = 400mW, Idle = 50mW, Sleep = 5mW)
- Selectable 1 bit serial or 2 bits parallel NRZ bus.
- Power consumption is at 770 mW typical.
- A single 5 V supply is required.
- This type 64 pin TQFP package (1.2 mm height)

Read Pulse Detector & Servo Functions :

- Built-in AGC amplifier for stable operation in spite of varying media and head characteristics.
- AGC amplifier gain can be set to zero during writing.
- Fast AGC attack can be accomplished with RX function.
- AGC input's short time can be controlled by internal time and register.
- 4-burst servo circuit (peak-hold) with buffer amps.
- Servo reference voltage output.
- Servo charging speed can be controlled by register.

Programmable Filter :

- Programmable cut-off frequency of 6 to 24 MHz.
- Cut-off frequency and boost level can be set independently for servo and data mode.
- 7th order Bessel filter.
- ±10 % cut-off (fc) accuracy.
- ±3 % group delay variation. (0.2 fc to fc)

Write Clock Synthesizer :

- On-chip frequency synthesizer generates write clock. (fmax./fmin. = 2.67)
- Independent M and N divide by registers.
- Unlock detect function.
- VCO center frequency matched to data synchronizer.
- VCO center frequency accuracy is within ±10 %.

Synchronizer :

- High-speed acquisition can be accomplished with highly stable reproduction by switching between normal-gain and high-gain modes, and by switching loop filter constants.(6 NRZ bytes typ. acquisition time)
- Dual-mode phase detector compares both phase and frequency to ensure a wide capture range.
- VCO center frequency accuracy is within ±10 %.

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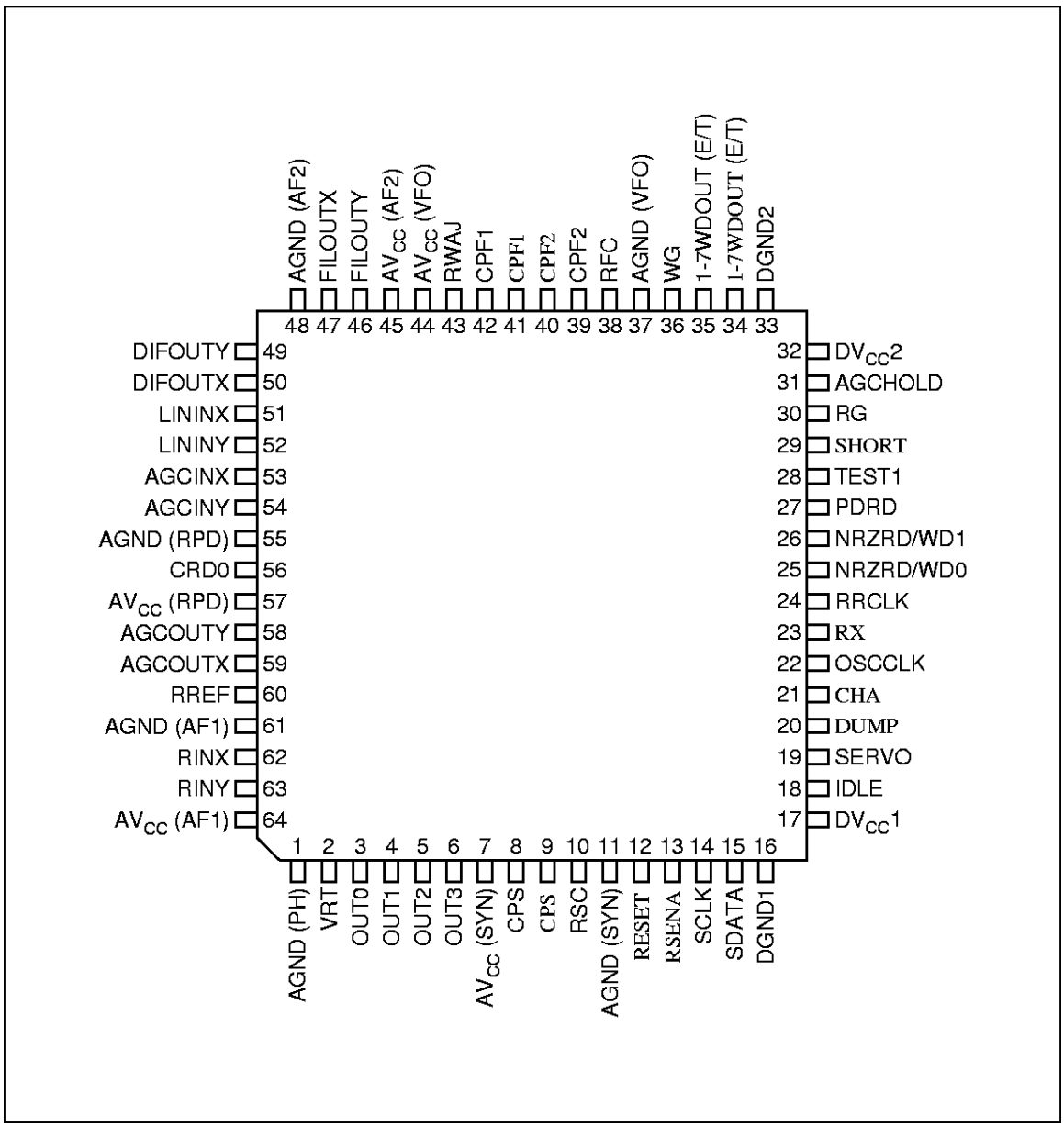
Data Separator :

- Window center accuracy is 0 ± 1.5 ns.
- Programmable window shift control.
- Window monitoring functions.

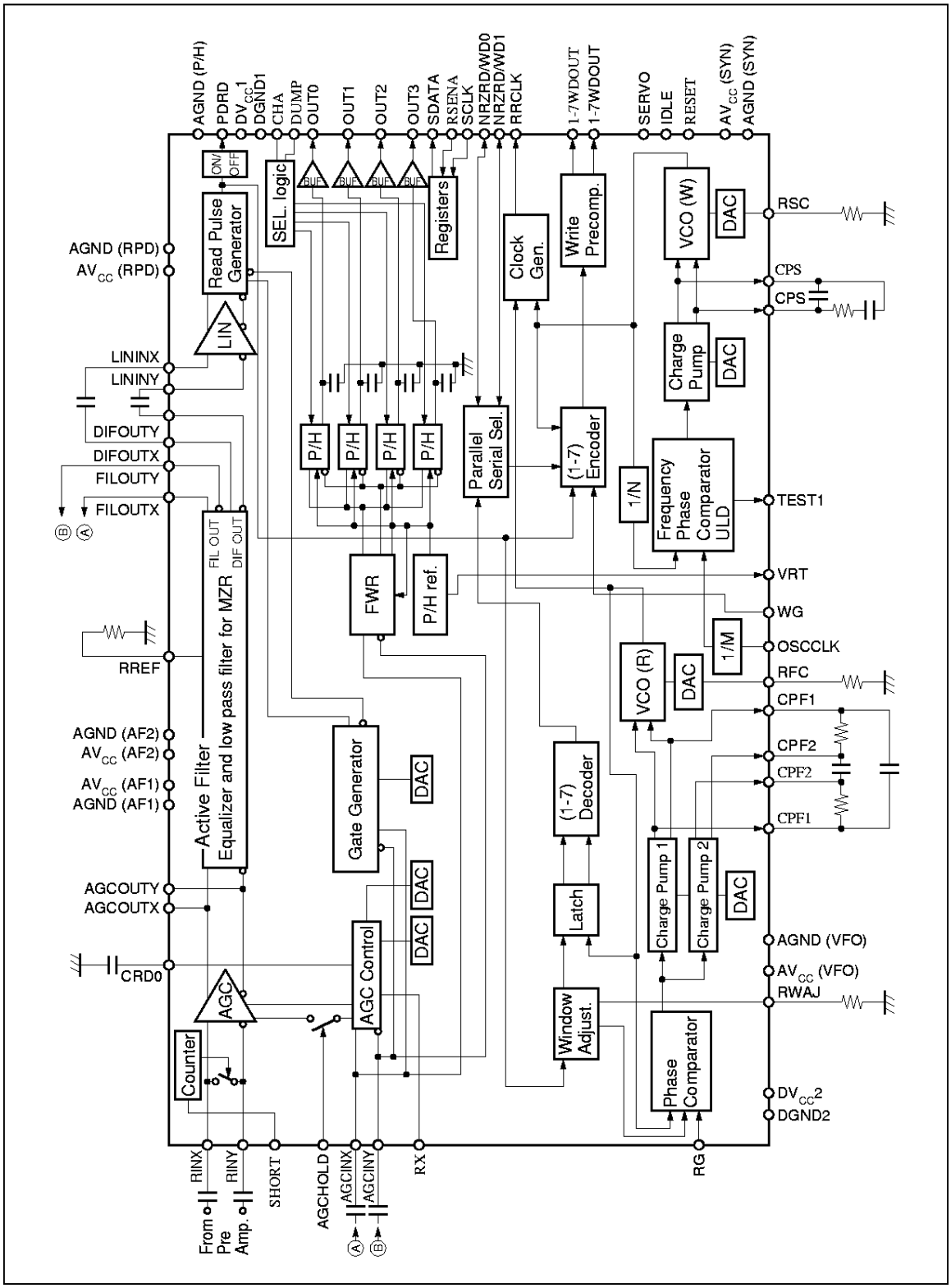
Encoder/Decoder :

- IBM 1,7RLL code.
- 1 bit serial or 2 bits parallel NRZ bus.
- 1,7 data to be written to disk can be programmed to be differential pseudo-ECL or TTL pair for high speed transfer without timing error.
- On chip write precompensation function with programmable delay line.

Pin Arrangement



Block Diagram



Pin Functions

Pin Name	Pin No.	Type	Function
RINX RINY	62 63	Differential input	Differential input lines for the read signal from the recording medium.
AGCOUTX AGCOUTY	59 58	Differential output	Differential output lines for monitor from the AGC amplifier. The outputs are open-emitter type and would need external 3.9 kΩ pull down resistors.
CRD0	56	External component required	The charge/discharge current output line for the AGC control circuit.
FILOUTX FILOUTY	47 46	Differential output	Differential output line from Active Filter. Connect to AGCINX, Y through bypass capacitors.
DIFOUTX DIFOUTY	50 49	Differential output	Differential output line from Active Filter. Connect to LININX, Y through bypass capacitors.
AGCINX AGCINY	53 54	Differential input	Differential input lines to the AGC output amplitude detector. Connect to FILOUTX/Y outputs of the Active Filter with bypass capacitors.
LININX LININY	51 52	Differential input	Differential input lines for the zero-crossing comparator. Normally connect to DIFOUTX/Y of the Active Filter with bypass capacitors.
RREF	60	External component required	Connect to a resistor to set the reference current for the Active Filter's DAC.
CPF1 CPF1 CPF2 CPF2	42 41 39 40	External component required	Current output to the external loop filter for read PLL.
RWAJ	43	External component required	Connect to a resistor to set the half window delay.
RFC	38	External component required	Connect to a resistor to set the center frequency of the VCO in the decode clock generator's VFO.
RSC	10	External component required	Connect to a resistor to set the center frequency of the VCO in the encode clock generator's frequency synthesizer.
CPS CPS	8 9	External component required	Current output to an external loop filter for write clock synthesizer.
OSCCLK (Oscillator clock)	22	In (TTL)	Clock synthesizer's reference clock input. The frequency synthesizer generates encode clock frequencies from the input on this line. Data writing is synchronized with the encode clock. When not reading data, the decode clock generator's VFO is also synchronized to this frequency (1.5 times the data transfer rate).

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
SHORT	29	In (TTL)	When this terminal is "L", RINX and RINY are shorted together. This short timing can be generated both by the internal short pulse generate circuit or direct input by this pin.
RX	23	In (TTL)	TTL-level input that switches the AGC loop on or off. When RX signal turn Low to High, AGC gain starts from maximum gain. HD153039TF has internal automatic RX pulse generate circuit.
AGCHOLD	31	In (TTL)	TTL-level input that locks the AGC amplifier gain. When AGCHOLD goes High, the gain is locked at its immediately preceding value.
SERVO	19	In (TTL)	"H" : Servo mode, "L" : Read mode. In the servo mode, "FCS" register set the A/F's cut-off frequency and GSH/GSLS register set the gate slice level. In the read mode, "FCR" register set the A/F's cut-off frequency and GSH/GSLR register set the gate slice level.
OUT0, OUT1, OUT2, OUT3	3, 4, 5, 6	Analog outputs	Servo burst's peak and hold outputs. Connect to A/D converter. Holding capacitors resides inside the chip with buffered outputs.
VRT	2	Analog outputs	Servo reference (maximum) voltage output.
CHA	21	In (TTL)	The sampling control signal for Servo Peak/Hold circuit (TTL level). Position signal is sampled by CHA = "L".
DUMP	20	In (TTL)	The discharge control signal of Servo Peak/Hold circuit (TTL level). DUMP = "L" is for discharge.
PDRD	27	Out (TTL)	Output line for the data read from disk as reshaped into digital data by the read pulse detector. When SERVO (pin19) goes high, PDRD outputs read data pulse. When SERVO goes low, PDRD is disable.
WG	36	In (TTL)	Write gate input signal. Set this pin high during writing.
RG (Read Gate)	30	In (TTL)	High level at this input selects read mode. This signal switches the clock for counters and internal circuits, and begins phase synchronization of the decode clock generator's VFO with the 1-7 decode data.
NRZRD/WD1	26	In/Out (TTL)	The parallel data I/O pin of NRZ signal.
NRZRD/WD0	25	In/Out (TTL)	The parallel data I/O pin of NRZ signal. When the bypass encoder mode, provide the 1-7 write into this pin. Write data will be directory output from 1-7WDOUT and 1-7WDOUT.

RX input	AGC loop
High	AGC loop closed
Low	AGC loop open

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
RRCLK	24	Out (TTL)	Read reference clock output (TTL level). At read time, this pin provides a clock which is synchronized with the converted NRZRD signal. This controller should read NRZRD by this clock. Other than read mode, reference clock is provided to disk controller.
1-7WDOUT 1-7WDOUT (Write data outputs)	35 34	Out (TTL/ECL)	1-7 RLL Write Data Differential Output. Pseudo ECL/TTL are available by bit 0 of register "$h14". When this bit is "H", these outputs are ECL. When this bit is "L", these outputs are TTL. These pin provide the 1-7 write data that goes to the Read/Write amplifier after the write pre-compensation. When WG goes high, 1-7WDOUT and 1-7WDOUT pin are in the output mode.
RESET	12	In (TTL)	Low input initializes internal logic circuits and registers.
RSENA	13	In (TTL)	This active low input selects the device and enables the serial port.
SCLK	14	In (TTL)	This is the serial clock sent in by the hard disk controller or other ASIC device. For either read or write transfer, a 16 clock burst is required for proper operation. Data is latched in during write or sent out during read at the rising edge of the SCLK.
SDATA	15	In/Out (TTL)	Data is transmitted in 16-bit packet MSB first. The first 2 bits is used to determine the read or write mode, the next 5 bits are for the register address, followed by 1 "Don't Care" bit, then the last 8 bits are for the Write or Read Data.
IDLE	18	In (TTL)	The input is used in combination with the two mode bits in the PCN register to reduce power consumption in the Idle mode. When PCN = 00, device is in the R/W normal mode, all circuits are ON. When PCN = 11, device is in the Sleep mode, all circuits are OFF except the I/O and register. When PCN = 10, then depending on the logic level of the IDLE pin; if it is High, then chip is in the Idle mode and all circuits are OFF except for the I/O, register, and the bias circuit's; if it is Low, then the device is in the Servo mode and the I/O, logic, bias circuit's, AGC, Active Filter, Read Pulse Detector, and Servo circuit will be ON with only the RD VFO and the WR synthesizer being OFF.
TEST1	28	Test pin	Output pin of the test signal.
$DV_{CC}1$ $DV_{CC}2$	17 32	Power	Digital V_{CC} power supply.
DGND1 DGND2	16 33	Ground	Digital ground.
AV_{CC}(AF1) AV_{CC}(AF2)	64 45	Power	Analog V_{CC} power supplies for active filter.
AGND(AF1) AGND(AF2)	61 48	Ground	Analog ground for active filter.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
AV_{CC}(RPD)	57	Power	Analog V_{CC} power supply for read pulse detector.
AGND(RPD)	55	Ground	Analog ground for read pulse detector.
AGND(P/H)	1	Ground	Analog ground for peak hold.
AV_{CC}(VFO)	44	Power	Analog V_{CC} power supply for synchronizer.
AGND(VFO)	37	Ground	Analog ground for synchronizer.
AV_{CC}(SYN)	7	Power	Analog V_{CC} power supply for synthesizer.
AGND(SYN)	11	Ground	Analog ground for synthesizer.

Registers

Address	Name	Abbreviation	Note
00h	VCO center frequency control register	VFC register	fmax/fmin = 2.67
01h	Read PLL (Synchronizer) charge pump gain control register	NCR register	Normal gain mode
	Write precompensation delay control register (Value S)	WPS register	
02h	Read PLL (Synchronizer) damping factor control register	NDR register	Normal gain mode
	Write precompensation delay control register (Value L)	WPL register	
03h	Read PLL (Synchronizer) charge pump gain control register	HCR register	High gain mode
	Write precompensation delay control register (Value N)	WPN register	
04h	Read PLL (Synchronizer) damping factor control register	HDR register	High gain mode
	Write precompensation delay control register (Value E)	WPE register	
05h	Read PLL (Synchronizer) charge pump gain control register	NCW register	Write clock Ref. mode
	AGC super discharge time control register.	SLT register	
06h	Read PLL (Synchronizer) damping factor control register	NDW register	Write clock Ref. mode
	AGC amp. internal short time control register.	SHT register	
07h	Write PLL charge pump gain control register	NCS register	
	Internal RX time control register	RXT register	
08h	Pre-Scaler of write clock synthesizer control register (Value M)	PSM register	
09h	Divider of write clock synthesizer control register (Value N)	PSN register	
0Ah	Decode window adjustment register	WAJ register	
0Bh	Half window delay adjustment register	WTS register	
	Unlock detect sensitivity control register	ULD register	
0Ch	AGC amplitude setting register	ADSL register	
	AGC Det. charge/discharge ratio setting register	DSL register	
	AGC Det. charge/discharge current control register	ASL register	
0Dh	Filter cut-off frequency control register (Read mode)	FCR register	fc = 6 to 24 MHz
0Eh	Filter cut-off frequency control register (Servo mode)	FCS register	fc = 6 to 24 MHz
0Fh	Filter boost level control register (Read mode)	BLR register	0 to 10 dB
10h	Filter boost level control register (Servo mode)	BLS register	0 to 10 dB
11h	High pass filter cut-off frequency control register	HPF register	
	High pass filter pre-amp gain control register	PAG register	
12h	Gate slice low-level setting register (Read mode)	GSLR register	
	Gate slice low-level setting register (Servo mode)	GSLS register	
13h	PDRD pulse width control register	PW register	
	PDRD output mode select register	PDS register	

Registers (cont)

Address	Name	Abbreviation	Note
14h	1-7 write data output type control bit (ECL/TTL)	WDSEL bit	Pseudo ECL or TTL
	1-7 write data 1/2 divide mode select bit	WDDIV bit	
	Servo circuit's charge rate control bit	PHSEL bit	× 1.0, × 0.8
15h	Negate counter control register	RGN register	
16h	Power management control register	PCN register	
	Gate slice high level setting register	GSH register	
17h	Test mode control register	TEST register	

Mode Control Register Map

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Resister Functions
0 0 0 0 0	" 0"	" 0"	VFC5*	VFC4	VFC3	VFC2	VFC1	VFC0	VFC: Read and Write center frequency PLL
0 0 0 0 1	WPS2	WPS1	WPS0	" 0"	NCR3*	NCR2	NCR1	NCR0*	NCR: Normal pump current for read mode WPS: Write precomp. delay (S) gain
0 0 0 1 0	WPL2	WPL1	WPL0	" 0"	NDR3*	NDR2	NDR1	NDR0	NDR: Normal damping factor for read mode WPL: Write precomp. delay (L) gain
0 0 0 1 1	WPN2	WPN1	WPN0	" 0"	HCR3*	HCR2*	HCR1*	HCR0*	HCR: High pump current for read mode WPN: Write precomp. delay (N) gain
0 0 1 0 0	WPE2	WPE1	WPE0	" 0"	HDR3	HDR2	HDR1*	HDR0*	HDR: High damping factor for read mode WPE: Write precomp. delay (E) gain
0 0 1 0 1	SLT2	SLT1	SLT0	" 0"	NCW3*	NCW2	NCW1	NCW0*	NCW: Normal pump current for Ref. mode SLT: AGC Super discharge time setting
0 0 1 1 0	SHT2	SHT1	SHT0	" 0"	NDW3*	NDW2	NDW1	NDW0	NDW: Normal damping factor for Ref. mode SHT: AGC amp. short time setting gain
0 0 1 1 1	RXT2	RXT1	RXT0	" 0"	NCS3	NCS2*	NCS1	NCS0	NCS: Write charge pump current RXT: Internal RX pulse time setting synthesizer's
0 1 0 0 0	PSM7	PSM6	PSM5	PSM4	PSM3	PSM2	PSM1	PSM0	PSM: Write M synthesizer's clock

									divide value
0 1 0 0 1 clock	PSN7	PSN6	PSN5	PSN4	PSN3	PSN2	PSN1	PSN0	PSN: Write N synthesizer's divide value
0 1 0 1 0 window adjustment	" 0"	" 0"	WAJ5*	WAJ4	WAJ3	WAJ2*	WAJ1	WAJ0	WAJ: Decode
0 1 0 1 1 window delay adjustment	ULD1	ULD0	WTS5	WTS4	WTS3	WTS2	WTS1*	WTS0	WTS: Half ULD: Unlock detector sensitivity
0 1 1 0 0 AGC Loop amplitude setting	" 0"	" 0"	ASL	DSL	ADSL3*		ADSL2	ADSL1	ADSL0 ADSL: DSL: AGC CHG/ DISCHG ratio ASL: AGC CHG/ DISCHG current
0 1 1 0 1 cut-off	" 0"	FCR6	FCR5*	FCR4*	FCR3	FCR2	FCR1	FCR0	FCR: Active filter frequency for read mode
0 1 1 1 0 cut-off	ACE	FCS6	FCS5*	FCS4*	FCS3	FCS2	FCS1	FCS0	FCS: Active filter frequency for servo mode
0 1 1 1 1 boost	" 0"	" 0"	" 0"	BLR4	BLR3 level	BLR2	BLR1	BLR0	BLR: Active filter for read mode
1 0 0 0 0 boost	" 0"	" 0"	" 0"	BLS4	BLS3 level	BLS2	BLS1	BLS0	BLS: Active filter for servo mode

Note: * These bits are set "1" when RESET pin is assented.

Register Descriptions

VCO Center Frequency Control Register (VFC)

Address : $00 (at write="C0" hex, at read="80" hex)

MSB							LSB
0	0	D5	D4	D3	D2	D1	D0

VFC register

This register is used in multiple-zone recording to set the center frequency of the decode clock generator's VCO and the oscillation frequency of the encode clock generator's frequency synthesizer.
Resistors connected to the RFC and RSC lines set these values for the maximum data transfer rate.
(0.375 times maximum transfer rate)

VFC [5:0]

0 1 1 0 0 0 Minimum transfer rate
•
1 0 0 0 0 0 Default transfer rate
•
1 1 1 1 1 1 Maximum transfer rate

Unused bits, must be 0 when written.

Read PLL's Charge Pump Output Current Control Register for Normal Gain Mode (NCR), Write Precompensation Delay Control Register (WPS)

Address : $01 (at write="C2" hex, at read="82" hex)

MSB							LSB
D7	D6	D5	0	D3	D2	D1	D0

NCR register

Select the output current of the R-PLL's charge pump for normal gain mode to vary the gain.

NCR [3:0]

0 0 0 0
•
1 0 0 1 (Default)
•
1 1 1 1

Unused bit, must be 0 when written.

WPS register

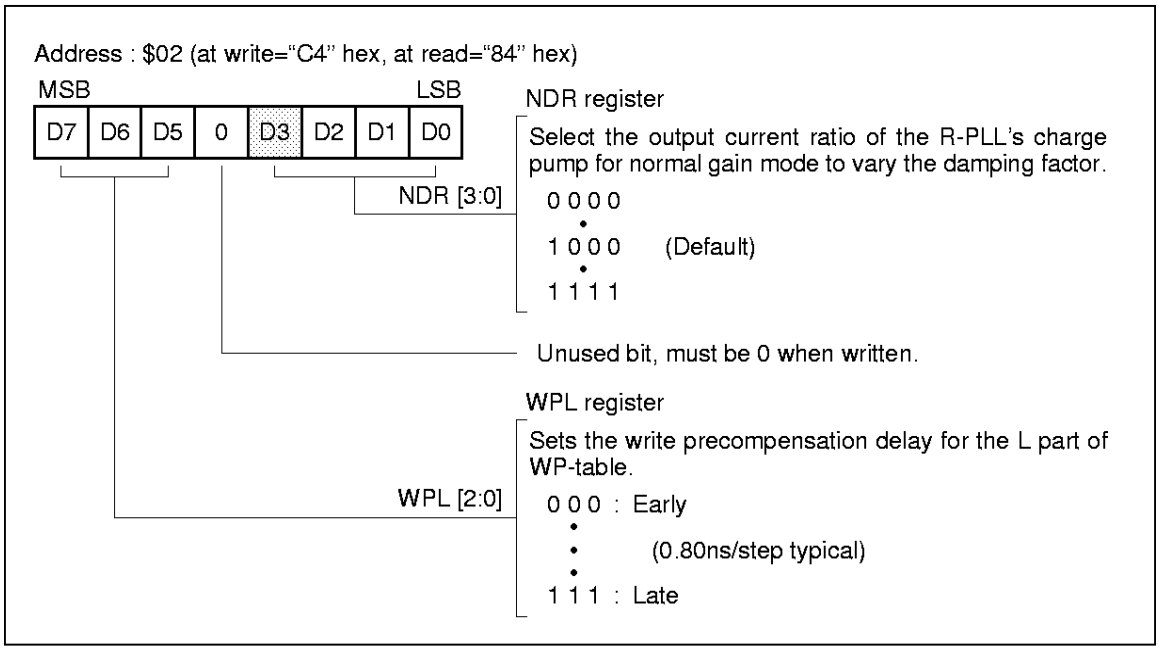
Sets the write precompensation delay for the S part of WP-table.

WPS [2:0]

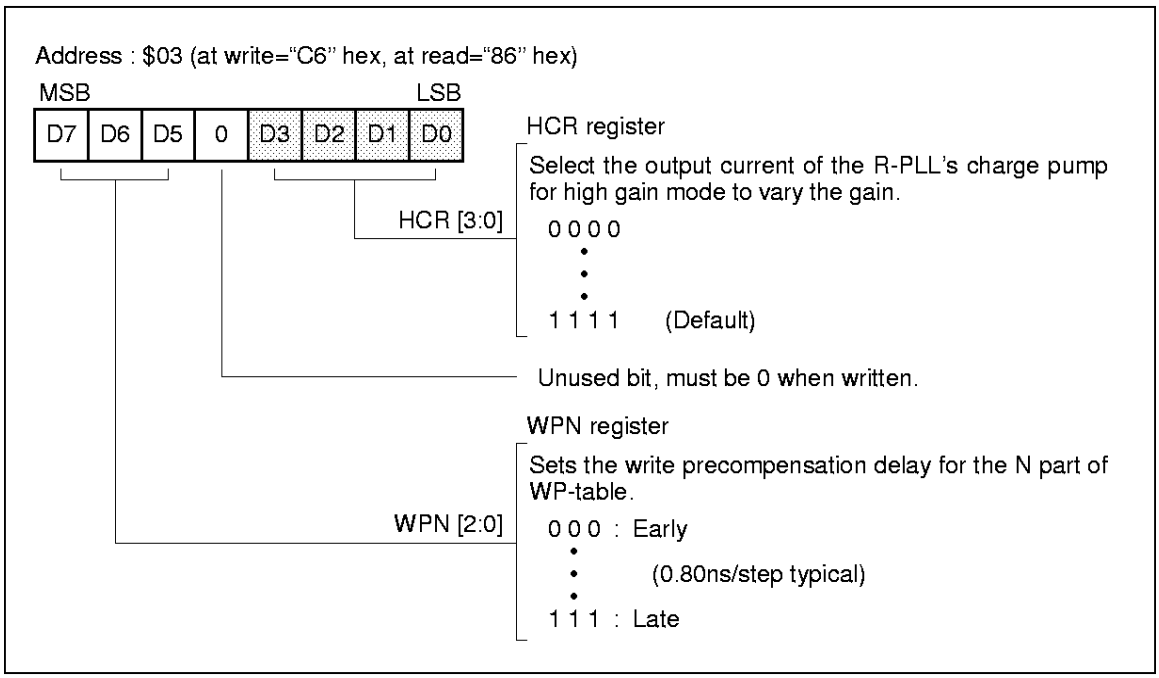
0 0 0 : Early
•
•
•
1 1 1 : Late

(0.80ns/step typical)

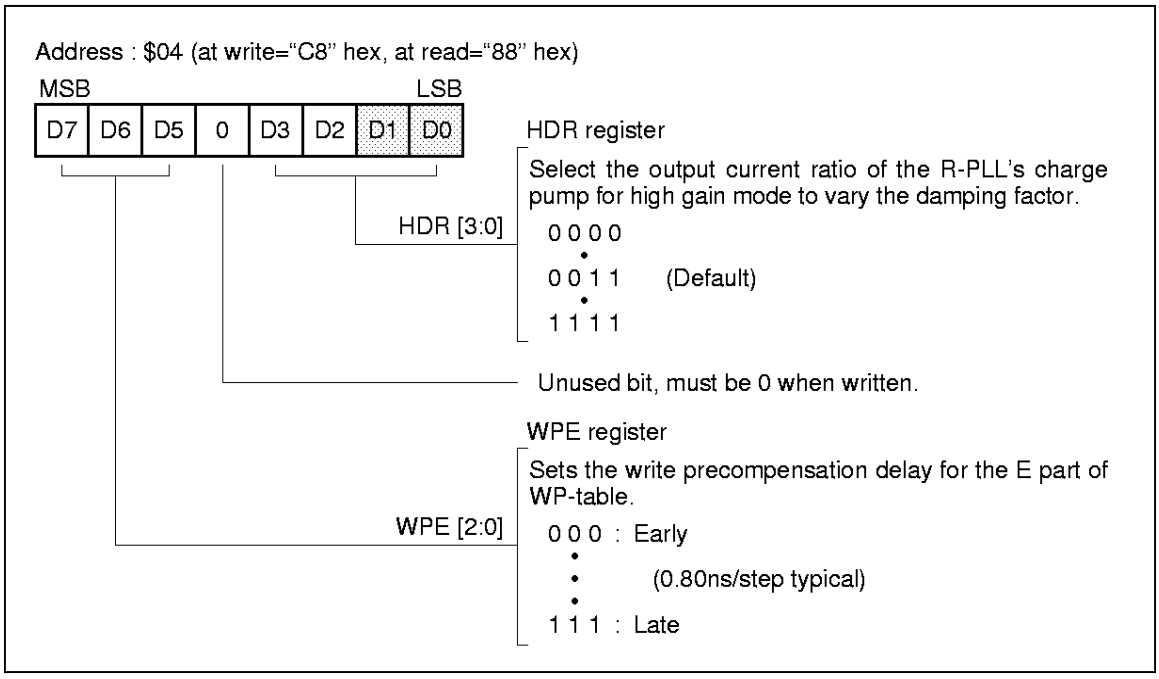
Read PLL's Damping Factor Control Register for Normal Gain Mode (NDR), Write Precompensation Delay Control Register (WPL)



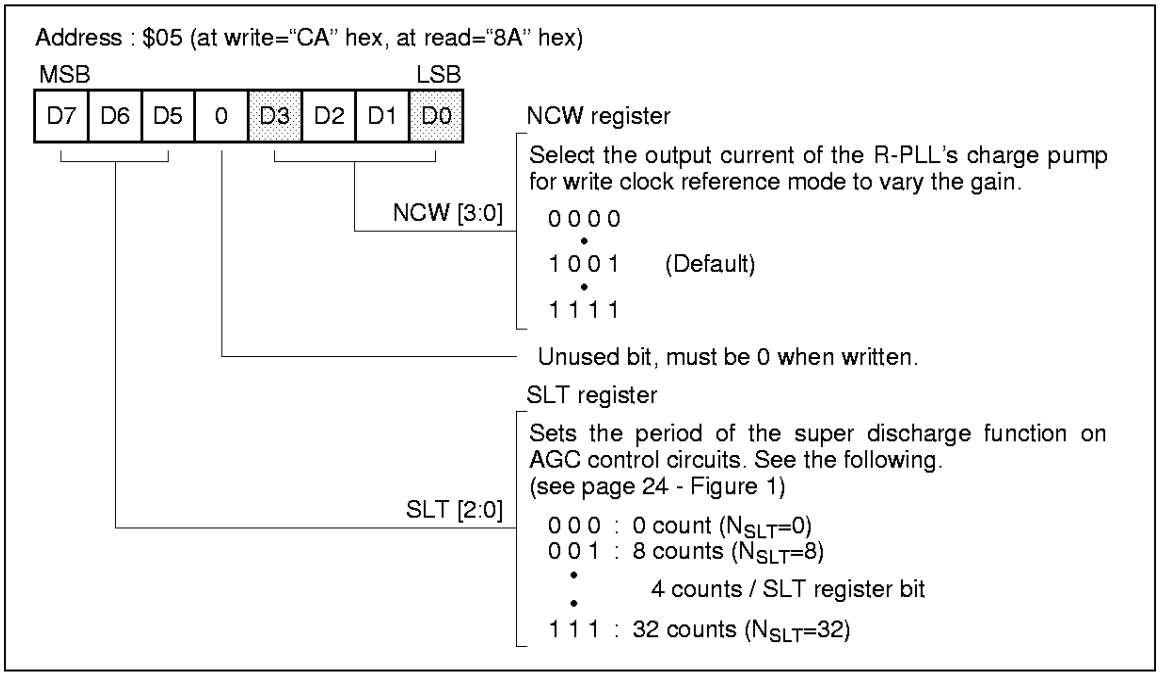
Read PLL's Charge Pump Output Current Control Register for High Gain Mode (HCR), Write Precompensation Delay Control Register (WPN)



Read PLL's Damping Factor Control Register for High Gain Mode (HDR), Write Precompensation Delay Control Register (WPE)

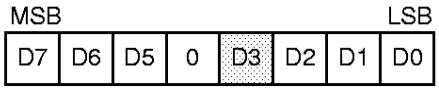


Read PLL's Charge Pump Output Current Control Register for Write Clock Reference Mode (NCW), AGC Super Discharge Time Control Register (SLT)



Read PLL's Damping Factor Control Register for Write Clock Reference Mode (NDW), AGC Amp. Input's Short Time Control Register (SHT)

Address : $06 (at write="CC" hex, at read="8C" hex)



NDW register

Select the output current ratio of the R-PLL's charge pump for normal gain mode to vary the damping factor.

NDW [3:0]

0 0 0 0
•
1 0 0 0 (Default)
•
1 1 1 1

Unused bit, must be 0 when written.

SHT register

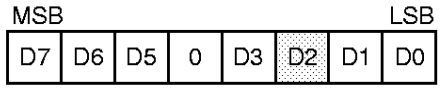
Sets the internal SHORT pulse ganerator. SHORT(Pin 29) pin and internal SHORT pulse gen. are connected OR logic. See the following. (see page 24 - Figure 2)

SHT [2:0]

0 0 0 : 0 count (N_{SHT}=0)
0 0 1 : 8 counts (N_{SHT}=8)
•
•
4 counts / SHT register bit
1 1 1 : 32 counts (N_{SHT}=32)

Write Synthesizer's Charge Pump Current Control Register (NCS), Internal RX Time Control Register (RXT)

Address : $07 (at write="CE" hex, at read="8E" hex)



NCS register

Select the output current of the write synthesizer's charge pump to vary the gain.

NCS [3:0]

0 0 0 0
•
0 1 0 0 (Default)
•
1 1 1 1

Unused bit, must be 0 when written.

RXT register

Sets the internal RX pulse generator. RX(Pin 23) pin and internal RX pulse gen. are connected OR logic. See the following. (see page 25 - Figure 3)

RXT [2:0]

0 0 0 : 0 count (N_{RXT}=0)
0 0 1 : 8 counts (N_{RXT}=8)
•
•
4 counts / RXT register bit
1 1 1 : 32 counts (N_{RXT}=32)

Pre-scaler of the Synthesizer Control Register (PSM) [M value]

Address : $08 (at write="D0" hex, at read="90" hex)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

PSM [7:0]

PSM register

This register controls the M pre-scale counter's value of the synthesizer. The OSCCLK signal is divided by 4 to 255.

0 0 0 0 0 1 0 0 divided by 4 (Minimum)

•

1 1 1 1 1 1 1 1 divided by 255

Divide of the Synthesizer Control Register (PSN) [N value]

Address : $09 (at write="D2" hex, at read="92" hex)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

PSN [7:0]

PSN register

This register controls the N divide counter's value of the synthesizer. The write VCO clock signal is divided by 4 to 255.

0 0 0 0 0 1 0 0 divided by 4 (Minimum)

•

1 1 1 1 1 1 1 1 divided by 255

Decode Window Adjust Register (WAJ)

Address : $0A (at write="D4" hex, at read="94" hex)

MSB							LSB
0	0	D5	D4	D3	D2	D1	D0

WAJ [5:0]

WAJ register

This register adjusts the setting of the window. Window centering can be adjusted by an on-chip delay line.

0 1 0 0 1 0 (Minimum)

•

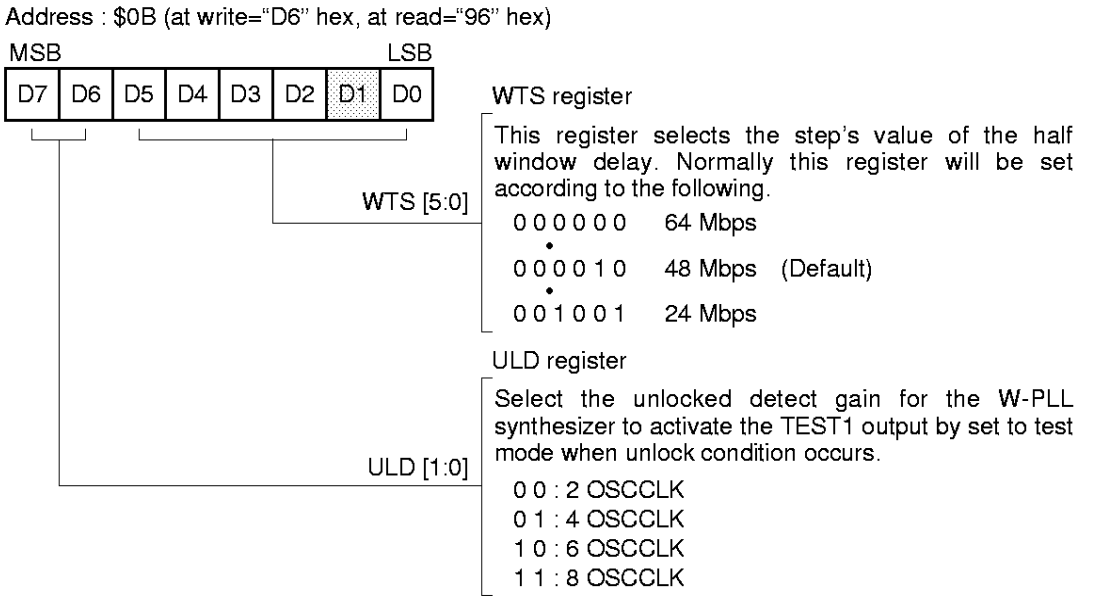
1 0 0 1 0 0 (Default)

•

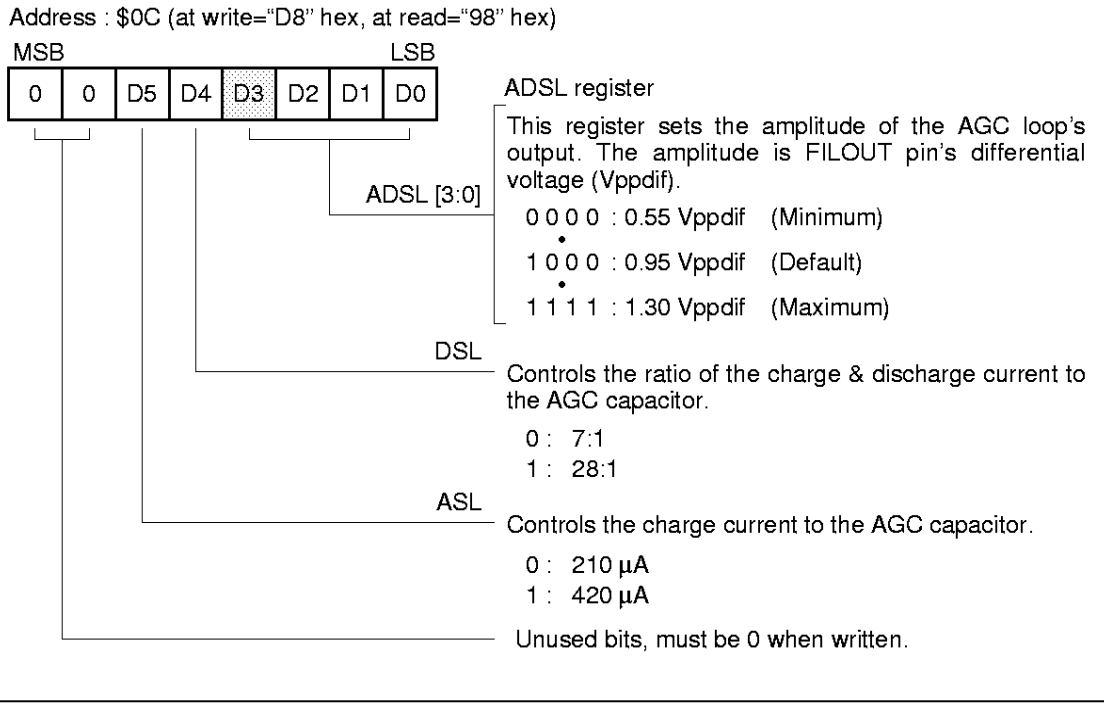
1 1 1 1 1 1 (Maximum)

Unused bits, must be 0 when written.

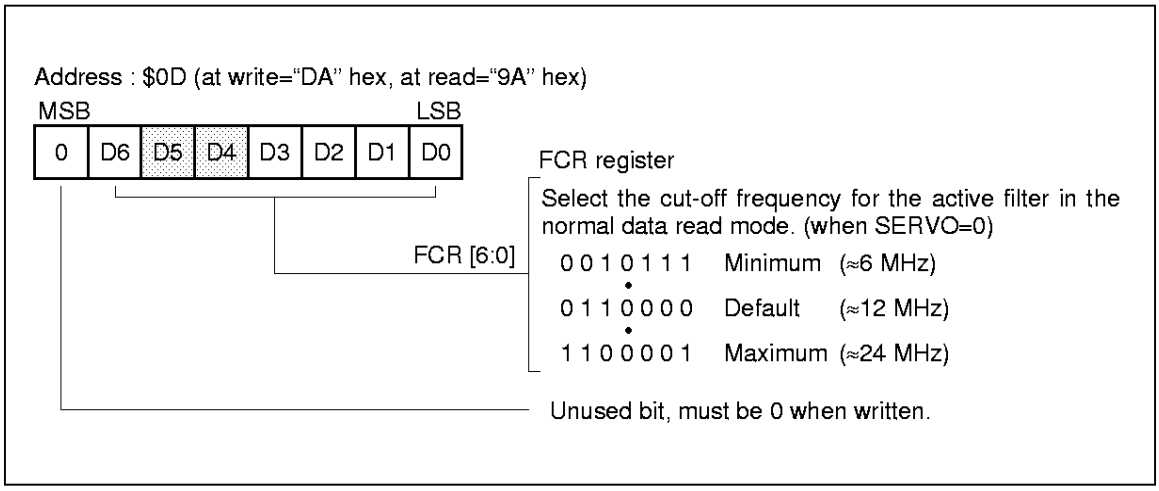
Half Window Delay Adjust Register (WTS),
Unlock Detector Sensitivity Control Register (ULD)



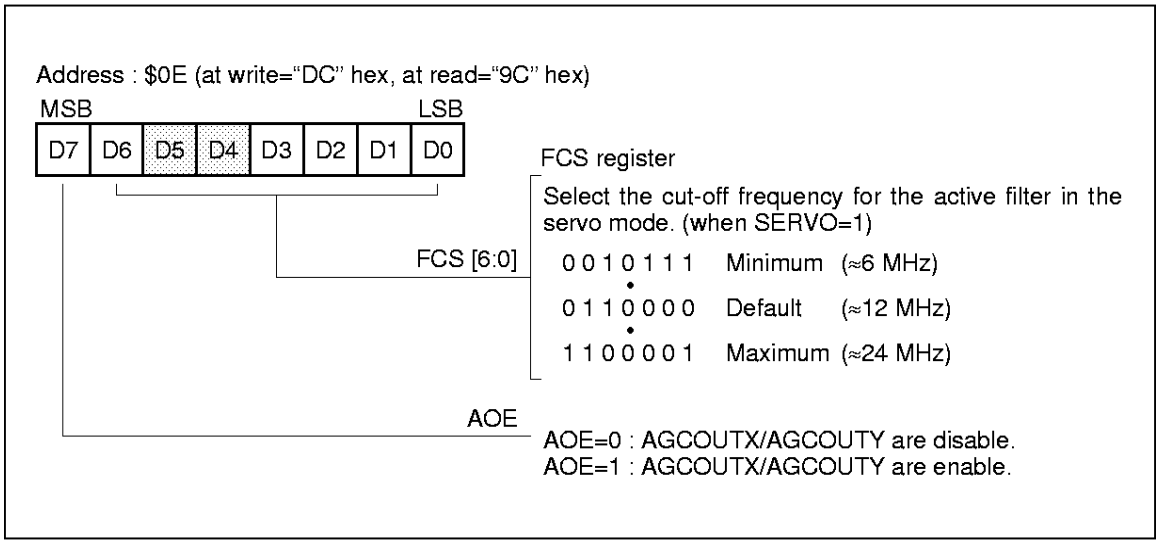
AGC Loop Amplitude Setting Register (ADSL),
AGC DET. Circuit's Charge Discharge Ratio Setting Register (DSL),
AGC DET. Circuit's Charge Current Setting Register (ASL)



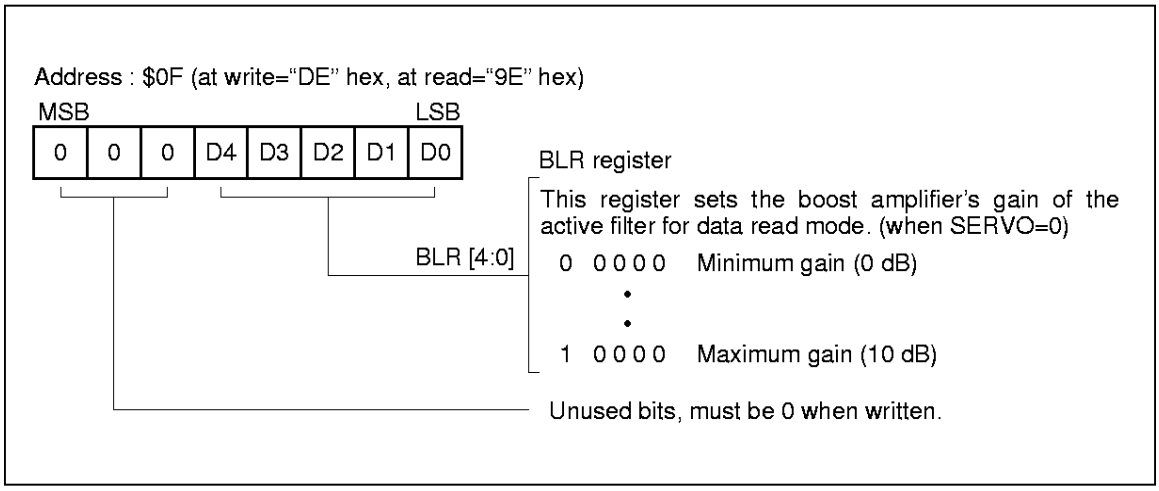
Read Mode AF Cut-off Frequency Register (FCR)



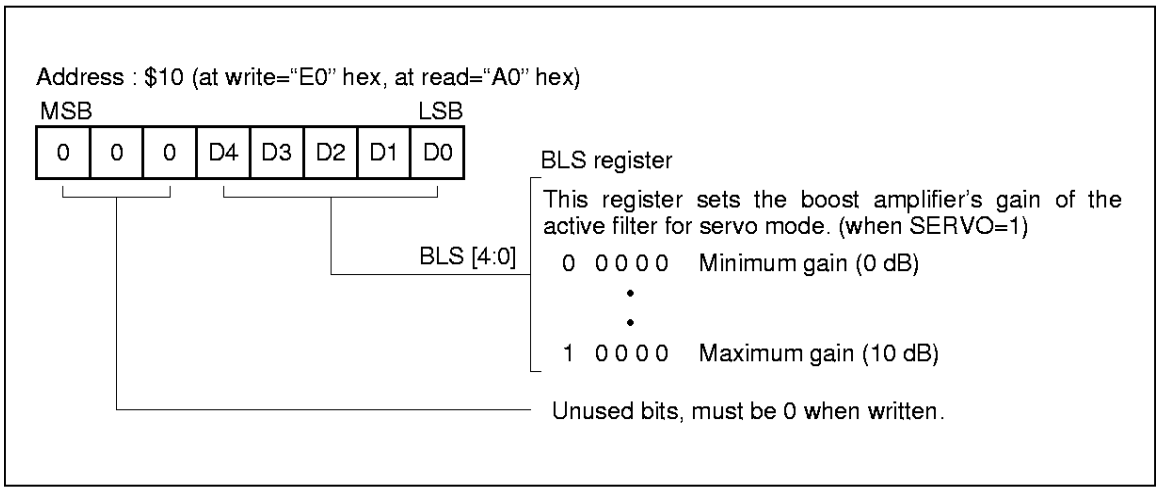
Servo Mode AF Cut-off Frequency Register (FCS)



Read Mode AF Boost Level Control Register (BLR)

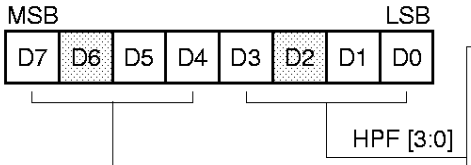


Servo Mode AF Boost Level Control Register (BLS)



High-Pass Filter Cut-off Frequency Control Register (HPF),
High-Pass Filter Pre-amp Gain Control Register (PAG)

Address : $11 (at write="E2" hex, at read="A2" hex)



HPF register

This register controls the cut-off frequency of the high-pass filter in the active filter circuit during read and servo mode.

0 0 0 0 Minimum 50 %
•
0 1 0 0 Default 100 % (FCR register)
•
1 1 1 1 Maximum 237.5 % (12.5 %/step typical)

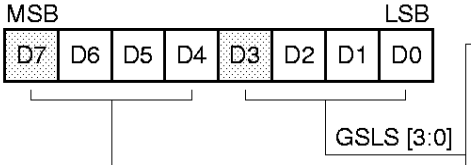
PAG register

This register controls the pre-amp gain of the high-pass filter in the active filter circuit during read and servo mode.

0 0 0 0 Minimum gain (–6 dB)
•
0 1 0 0 Default gain (0 dB)
•
1 1 1 1 Maximum gain (6 dB)

Read Mode Low-Slice Level Register (GSLR),
Servo Mode Low-Slice Level Register (GSLS)

Address : $12 (at write="E4" hex, at read="A4" hex)



GSLS register

These are input to the internal DAC using to generate the low-slice level for the pulse detection circuit in the servo mode. (when SERVO=1)

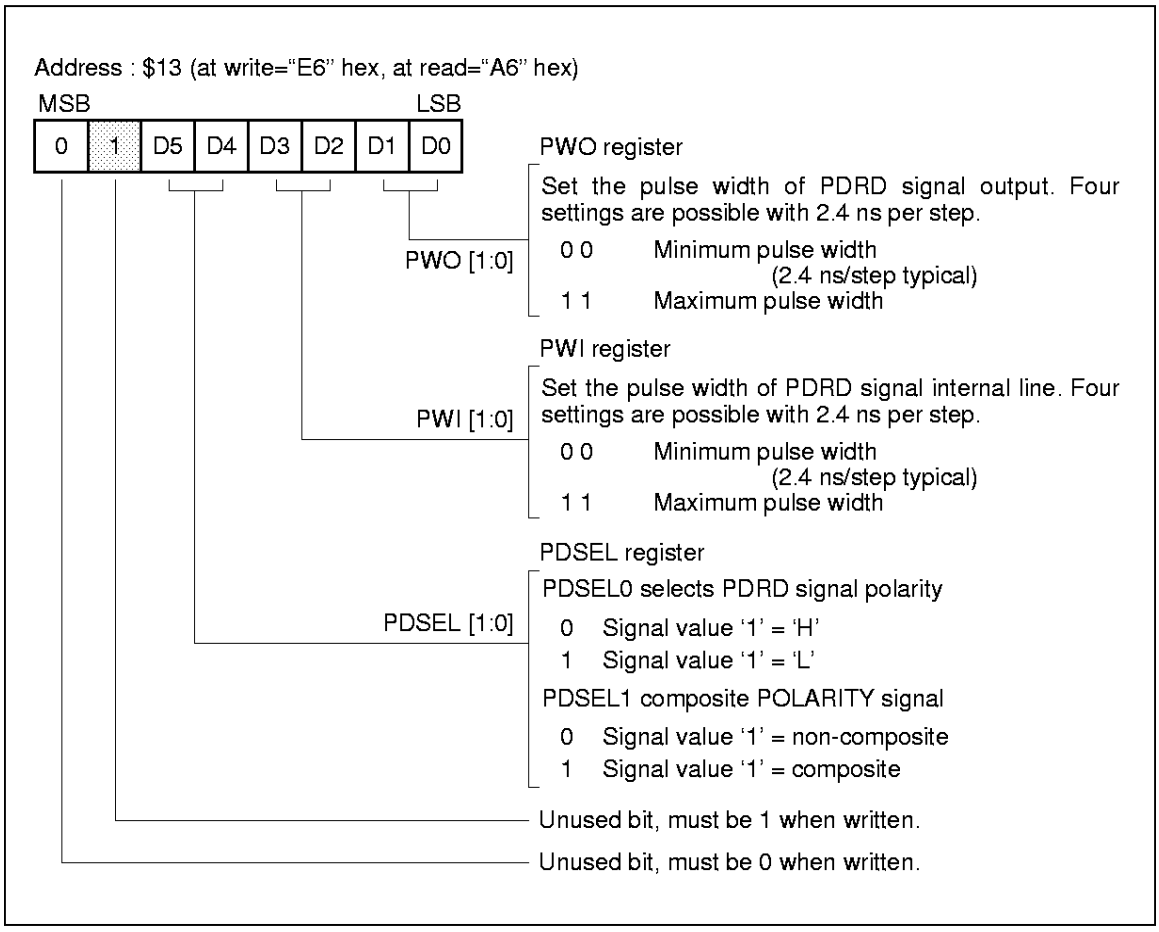
0 0 0 0 Minimum low-slice level 0.0 V
•
1 0 0 0 Default low-slice level 0.50 V
•
1 1 1 1 Maximum low-slice level 0.95 V

GSLR register

These are input to the internal DAC using to generate the low-slice level for the pulse detection circuit in the read mode. (when SERVO=0)

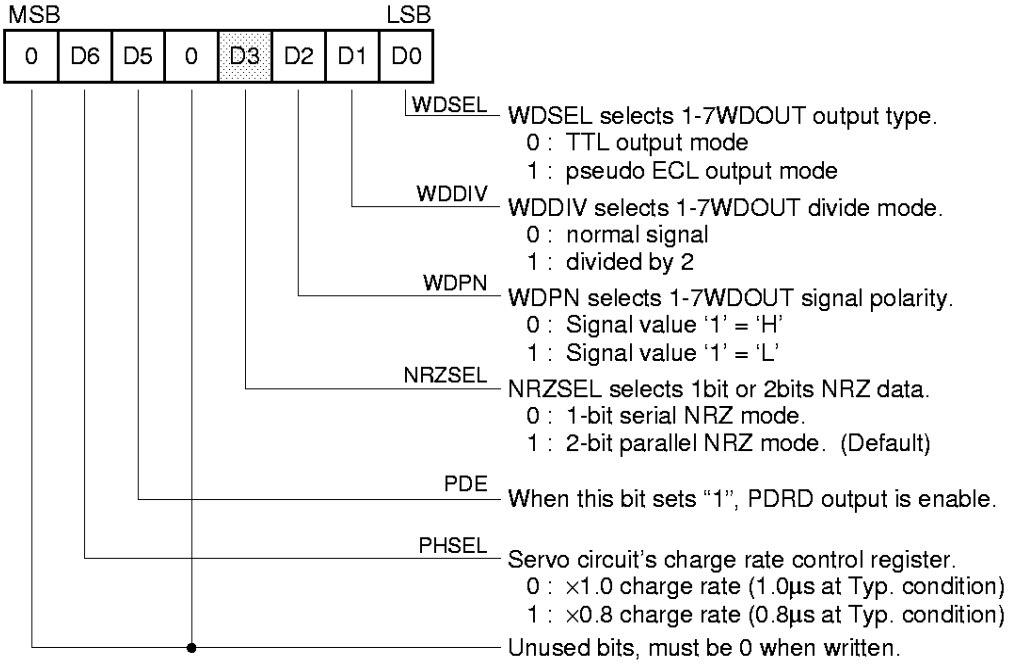
0 0 0 0 Minimum low-slice level 0.0 V
•
1 0 0 0 Default low-slice level 0.50 V
•
1 1 1 1 Maximum low-slice level 0.95 V

Read Data Pulse Width Control Register (PWO),
Internal Read Data Pulse Width Control Register (PWI),
Read Data Polarity Control Register (PDSEL)



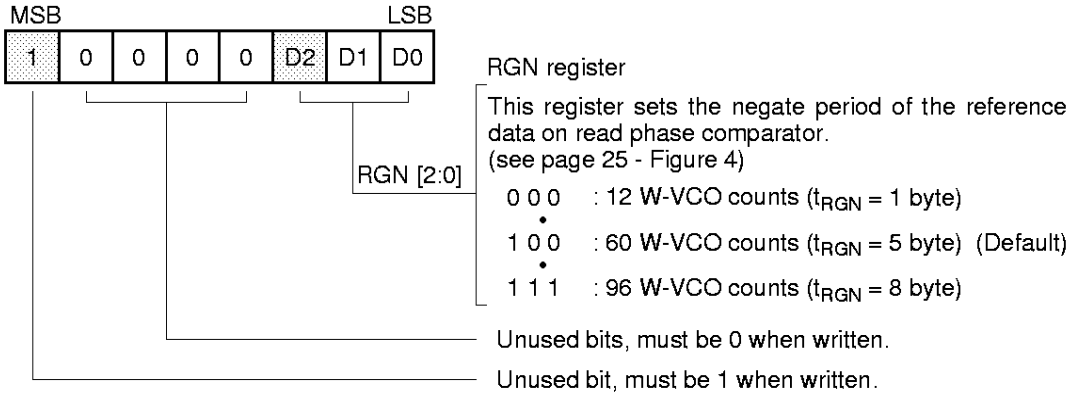
1-7WDOUT Output Type Select Bit (WDSEL), 1-7WDOUT Polarity Select Bit (WDPN), 1-7WDOUT Divide Mode Select Bit (WDDIV), NRZ Data Mode Select Bit (NRZSEL), PDRD Output Enable Control Bit (PDE), Servo Circuit's Charge Rate Select Bit (PHSEL)

Address : $14 (at write="E8" hex, at read="A8" hex)



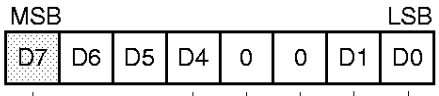
Negate Counter Setting Register (RGN)

Address : $15 (at write="EA" hex, at read="AA" hex)



Read and Servo Mode High-Slice Level Register (GSH)
Power Control Register (PCN)

Address : $16 (at write="EC" hex, at read="AC" hex)



PCN0 : Power control register (see page 26)

PCN1 : Power control register (see page 26)

PCN1, 0 = 00 : Normal mode. All circuits are powered.

PCN1, 0 = 11 : Sleep mode. Everything powered down except the I/O and the logic section of the chip.

PCN1, 0 = 10 : Power Save mode. In this mode, the IDLE pin will select which of the two power save modes to be used. If IDLE = 1 then Idle mode is selected and all modules will be powered down except for the I/O, logic, and the bias circuits. If IDLE = 0 then Servo mode will be selected and all blocks will be kept on except the clock synthesizer (WR PLL) and the synchronizer (RD PLL).

Unused bits, must be 0 when written.

GSH register

There are input to the internal DAC using to generate the programmable High-Slice level for the Pulse detection circuit in the read and servo mode.

GSH [3:0]

0 0 0 0 : Minimum high-slice level 0.0 V

•

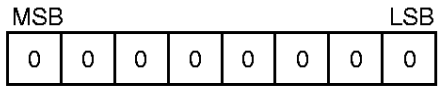
1 0 0 0 : Default high-slice level 0.50 V

•

1 1 1 1 : Maximum high-slice level 0.95 V

Test Mode Control Register

Address : $17 (at write="EE" hex, at read="AE" hex)



Unused bits, must be 0 when written.

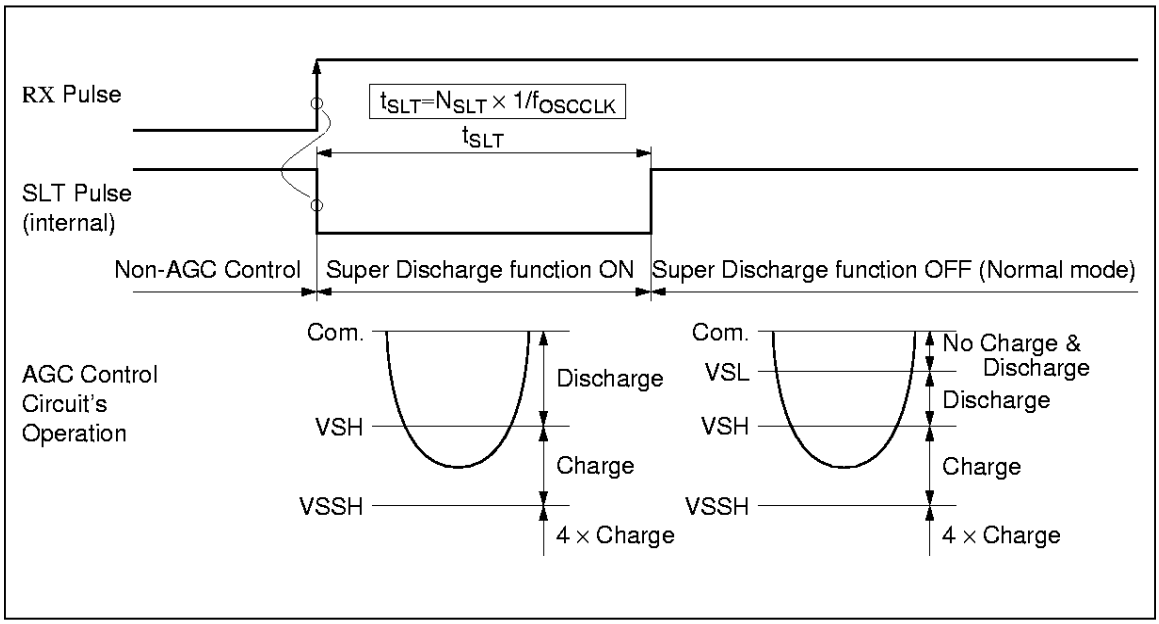


Figure 1 Super Discharge Function of the AGC Control Circuits

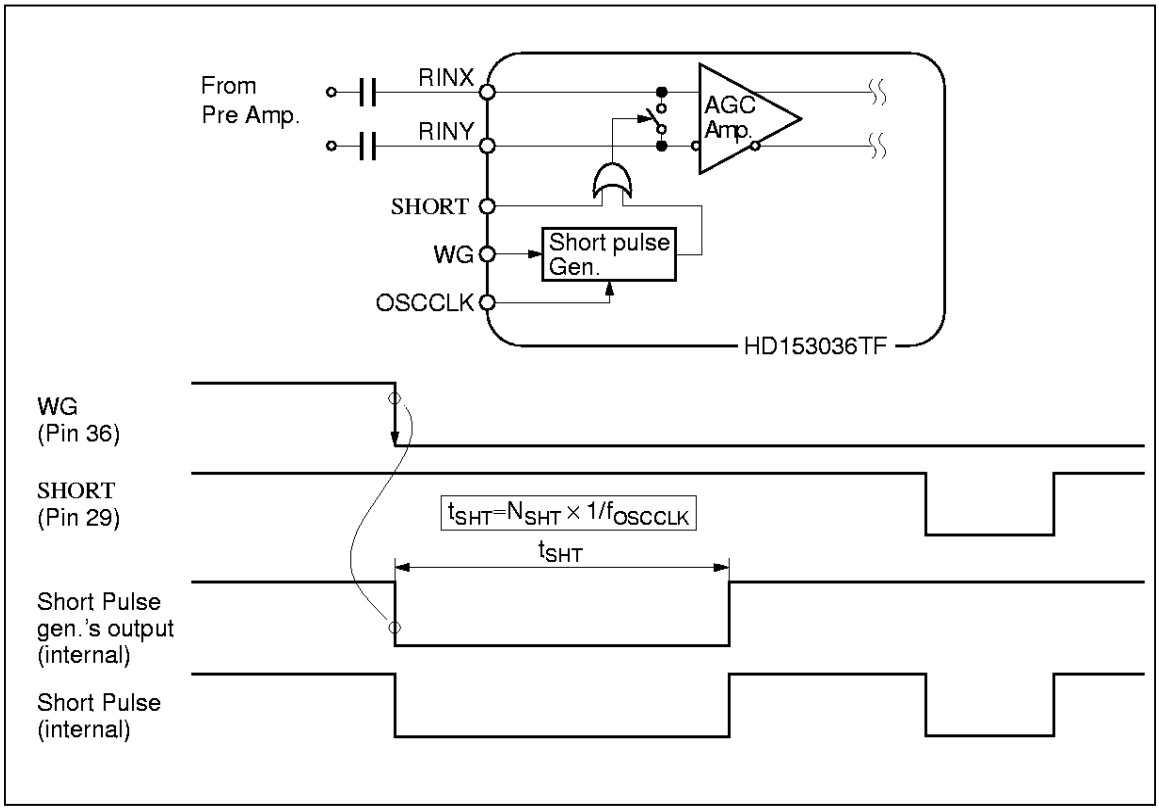


Figure 2 Short Timing Generate Function

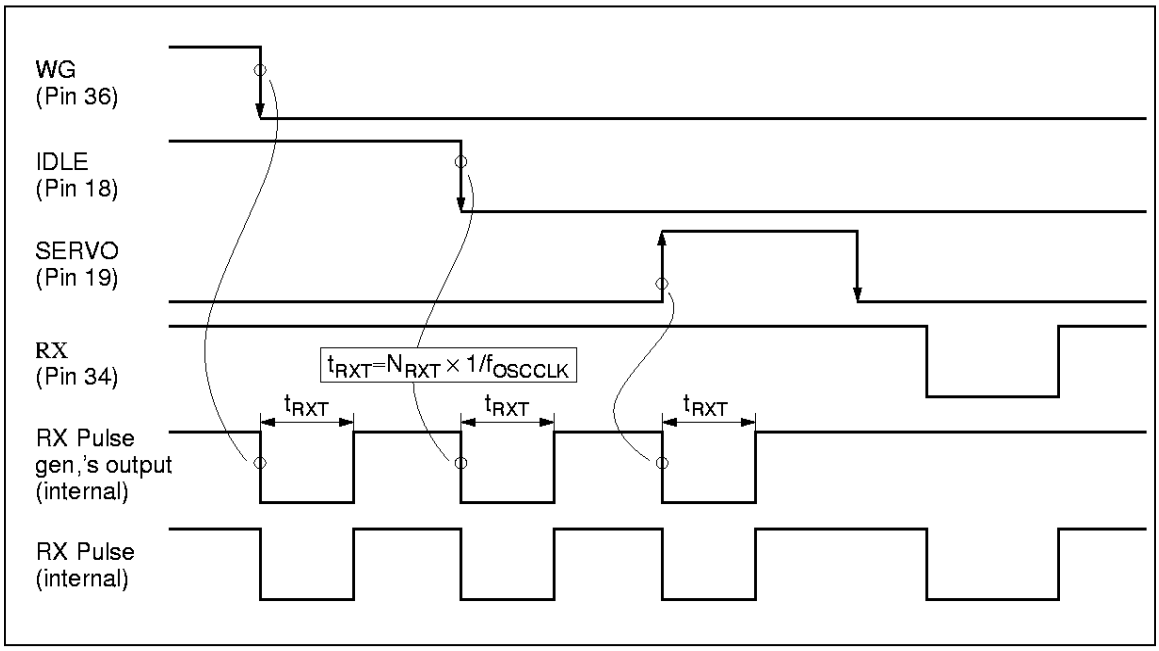


Figure 3 RX Pulse Generate Function

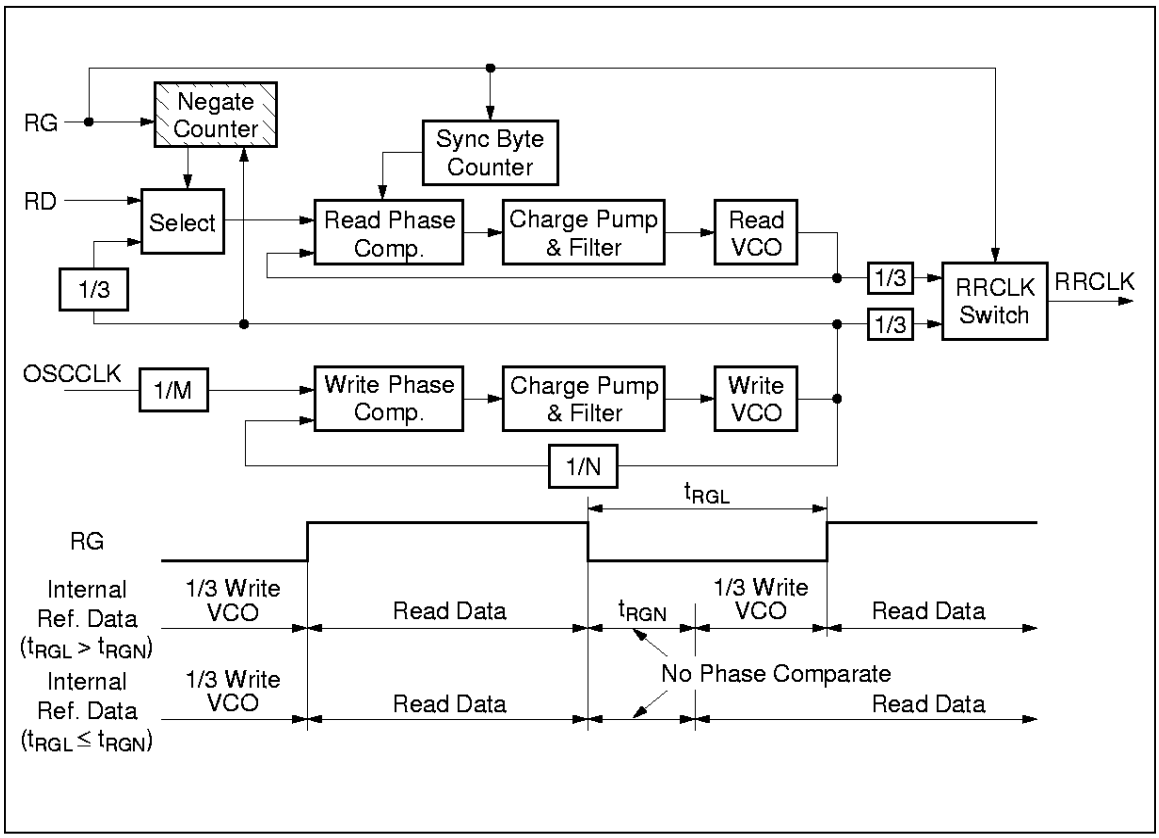
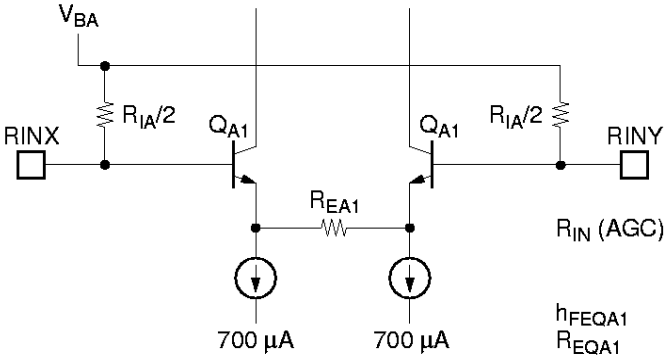


Figure 4 Read / Write PLL's Block Diagram & Negate Count Function

Input / Output Impedance of the Read Pulse Detector's Amplifiers

• AGC amplifier

Input impedance



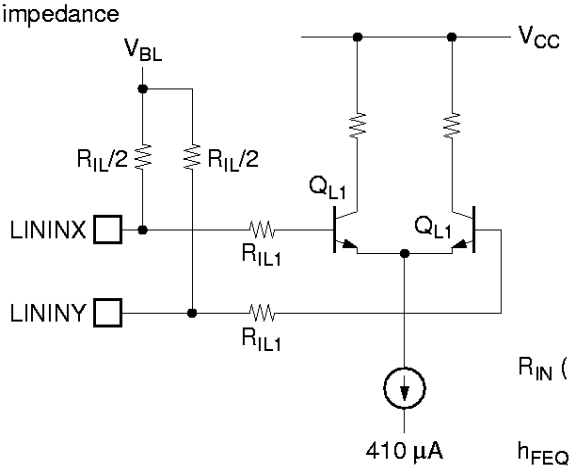
$R_{IA}/2$	1.5 kΩ
R_{EA1}	300 Ω
R_{EQA1}	37.143 Ω
h_{FEQA1}	80

R_{IN} (AGC) $\cong R_{IA}/2 \,//\, h_{FEQA1} \times (R_{EA1}/2 + R_{EQA1})$
$\cong 1.5\ k\Omega \,//\, 14.971\ k\Omega$
$\cong 1.363\ k\Omega$

h_{FEQA1} : h_{FE} of Q_{A1}
R_{EQA1} : Emitter resistance of Q_{A1}

• LIN amplifier

Input impedance



$R_{IL}/2$	1.5 kΩ
R_{IL1}	100 Ω
R_{EQL1}	63.415 Ω
h_{FEQL1}	80

R_{IN} (LIN) $\cong R_{IL}/2 \,//\, (R_{IL1} + h_{FEQL1} \times R_{EQL1})$
$\cong 1.5\ k\Omega \,//\, 5.173\ k\Omega$
$\cong 1.163\ k\Omega$

h_{FEQL1} : h_{FE} of Q_{L1}
R_{EQL1} : Emitter resistance of Q_{L1}

P/H Circuit for Servo

The P/H circuits consists of a full-wave rectifier, sample and hold, followed by a gain stage that drives internal capacitors through switches. Four outputs are made available to enable detection for four channel servo. When, the DUMP signal goes low, all holding capacitors are discharged. Then, the CHA signal is activated producing a succession of four negative pulses.

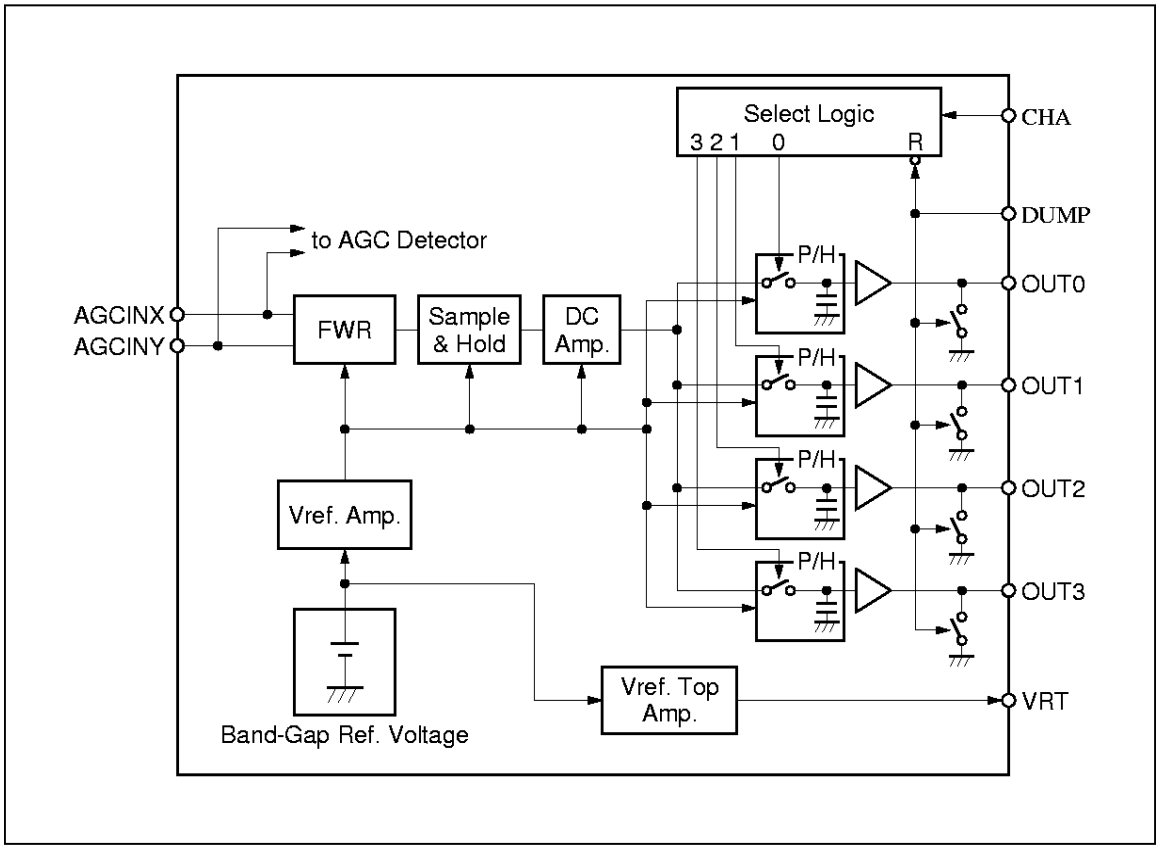


Figure 5 Servo Peak & Hold Circuit Block Diagram

AGC (Automatic Gain Control) Amplifier Circuit

The AGC amplifier is a two-stage differential amplifier. The first stage has variable gain and the second stage has fixed gain. The AGC block consists of the first stages. The output of the active filter (FILOUT and DIFOUT) stage is the second gain stage of the AGC block.

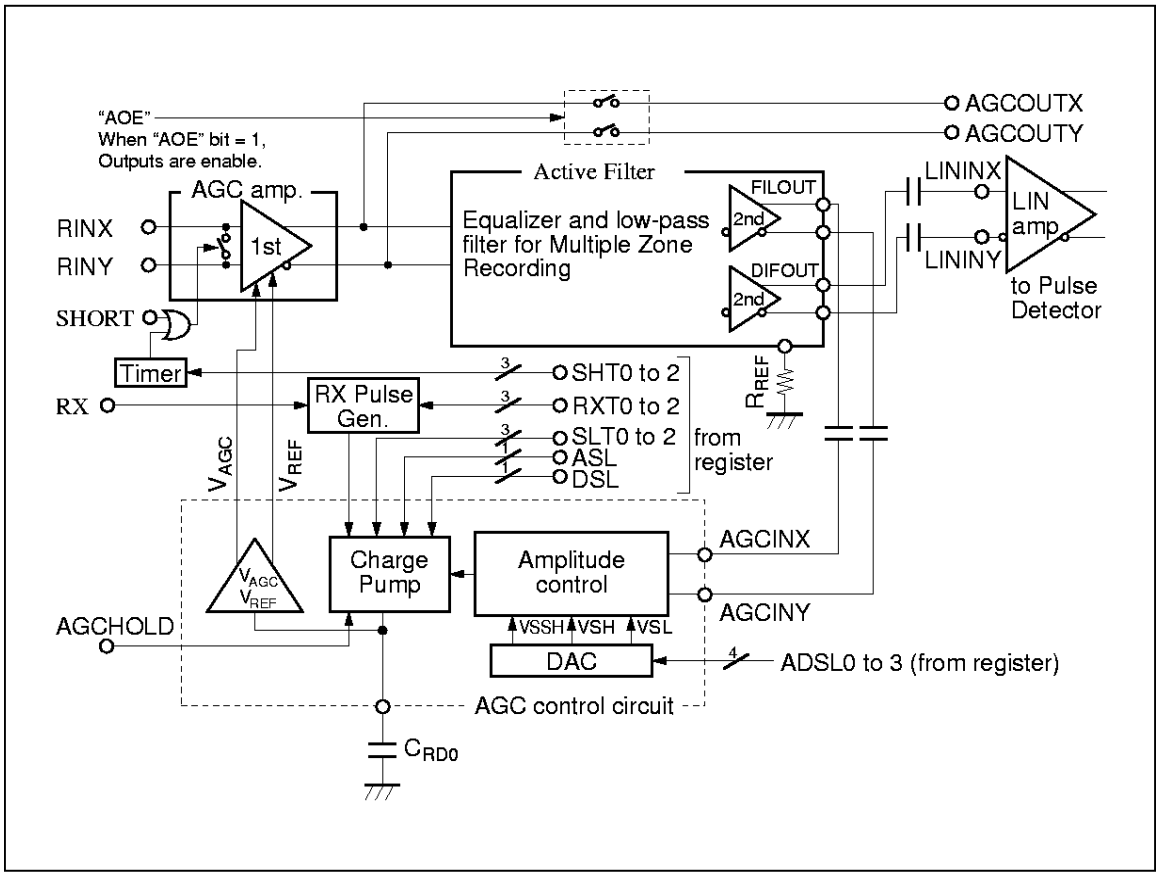


Figure 6 AGC Block Diagram

The first-stage gain can be controlled in the range from – ∞ to approximately 17 dB by an amplitude control signal (VAGC) from the AGC control circuit. The first-stage gain is given by the following formula.

$$A_V = K_1 \cdot \left(\frac{1}{1 + \exp\ (qV_C / kT)} \right)$$

$K_1 = 7.08$

$V_C = V_{AGC} - V_{REF}$

q: Unit electrical charge

k: Bolzmann constant

T: Absolute temperature

The second-stage amplifier within the active filter has fixed gains of 21 dB (at the outputs of FILOUT).

The AGC full gain is 79.4 V/V (=38 dB).

When bit 7 of register address "01110" (AOE bit) is set to "1", AGCOUTX and AGCOUTY pins can be used to monitor the output of the AGC amplifier. These pins are open emitter type. When monitor them, please terminate to ground by 3.9 kΩ resistor.

Bit 4 of register address "01100" (DSL register) determines the AGC control current ratio. When DSL will be set to "0", Charge: Discharge ratio will be 7 : 1. When DSL will be set to "1", Charge: Discharge ratio will be 28 : 1.

Bit 5 of register address "01100" (ASL register) determines charge current of AGC. When ASL will be set to "0", the charge current will be 210 µA. When ASL will be set to "1", the charge current will be 420 µA.

Table 1 Charge, Discharge Current of AGC Amp. vs. ASL, DSL Register

Register "01100"			
ASL	**DSL**	**Charge Current**	**Discharge Current**
"0"	"0"	210 µA	30 µA
"0"	"1"	210 µA	7.5 µA
"1"	"0"	420 µA	60 µA
"1"	"1"	420 µA	15 µA

The AGC amplifier gain control system is shown in figure 6. The AGC amplifier output is amplified by the post-amplifier then passed through a low-pass filter. The low-pass filter output is connected to the differentiating amplifier, and is also feedback to the AGC control circuit. Here it is compared with reference voltages V_{SH} and V_{SL} that are set internally (V_{SL} is 50 % of V_{SH}), then the external capacitor (CRD) are charged or discharged. The charging and discharging of the external capacitor varies the control signal V_{AGC} which directly affects the gain of the AGC amplifier. The final amplitude V_P (of the AGCINX and AGCINY waveforms) in this control system can be calculated from the following equations, assuming sine waveforms:

$$T_1 \times Ich = T_2 \times Idis \quad (1)$$

$$T_1 = \left(1 - \frac{2}{\pi} \sin^{-1} \frac{V_{COM} - V_{SH}}{V_P}\right) \times T \quad (2)$$

$$T_2 = \left(1 - \frac{2}{\pi} \sin^{-1} \frac{V_{COM} - V_{SL}}{V_P}\right) \times T \quad (3)$$

From equations (1), (2) and (3):

$$\sin^{-1} \frac{V_{COM} - V_{SH}}{V_P} - \frac{Idis}{Ich} \sin^{-1} \frac{V_{COM} - V_{SL}}{V_P} = \frac{\pi}{2}\left(1 - \frac{Idis}{Ich}\right) \quad (4)$$

The final amplitude of the AGC amplifier loop is determined mainly by V_{SH} bias level. If appropriate values are set for V_{SL}, Ich and Idis, then from the preceding equations the final differential peak voltage V_{PDF} is:

$$V_{PDF} = 4\,(V_{COM} - V_{SH}) \times m \quad (5)$$

where m = 1.00 to 1.05

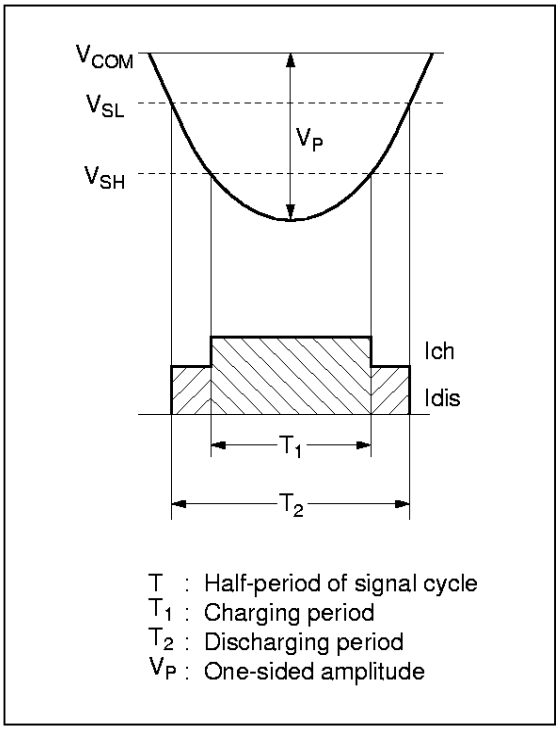


Figure 7 Charge / Discharge Timing

Programmable Active Filter Circuit

Active filter consists of equalizer and electronic filter. Electronic filter is 7-pole, Bessel-type, low-pass filter and can be used in multiple zone recording (MZR) design. Cut-off frequency of filter is set by writing to register FCR and FCS. Writing to the HPF register will set the high-pass cut-off frequency of the differential amplifier. Writing of the PAG register will set the pre-amp gain of the high-pass filter. The equalizer is double differentiation pulse sliming equalization. The boost level is set by writing to register BLR and BLS.

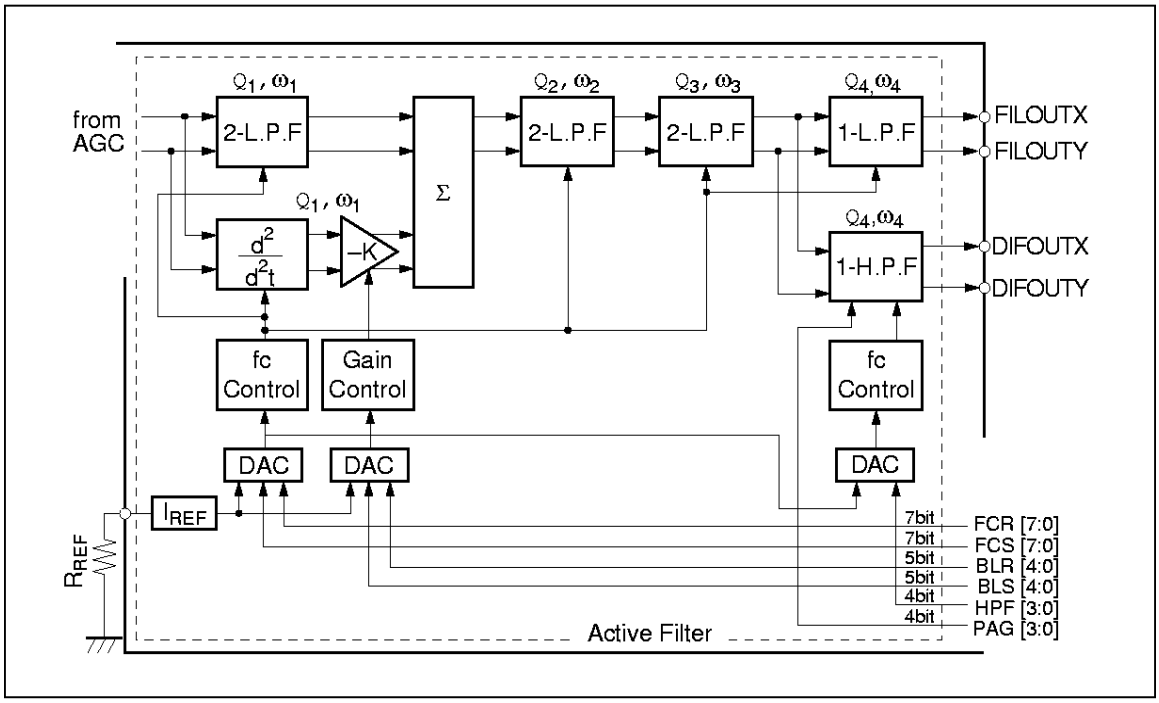
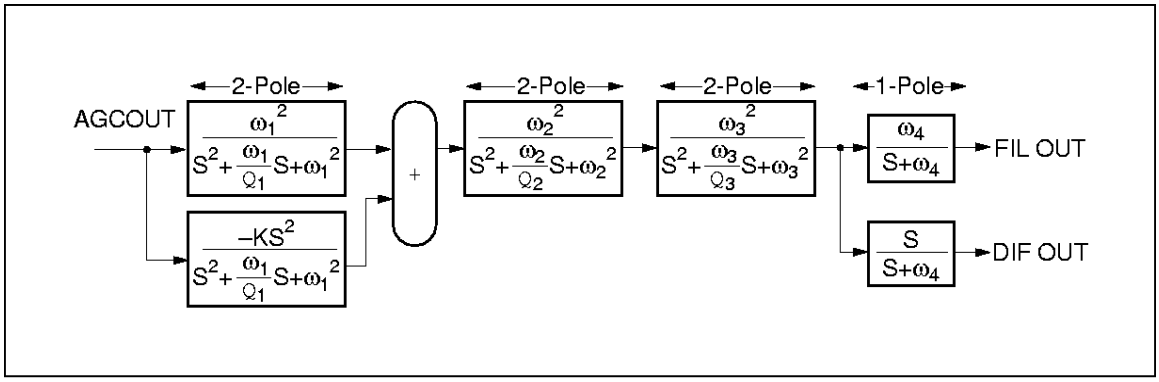
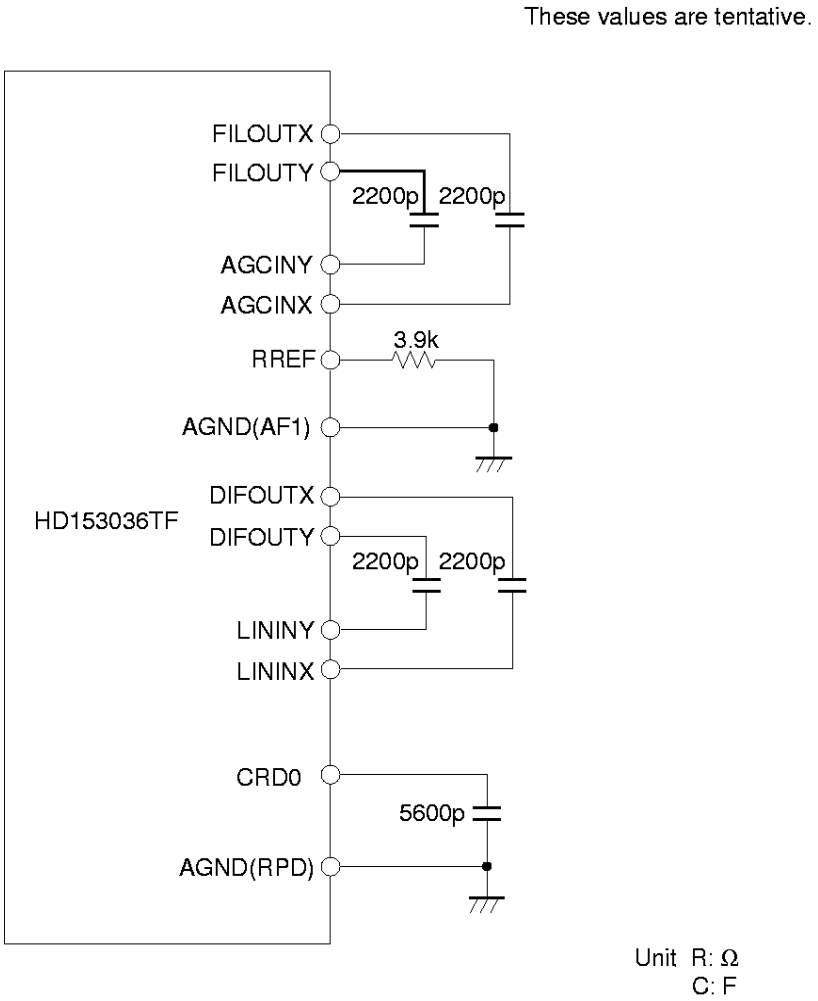


Figure 8 Active Filter Block Diagram

Transfer Function



Example of External Components Connected to the RPD



The AGC full gain is 79.4 V/V (=38 dB).
When bit 7 of register address "01110" (AOE bit) is set to "1", AGCOUTX and AGCOUTY pins can be used to monitor the output of the AGC amplifier. These pins are open emitter type. When monitor them, please terminate to ground by 3.9 kΩ resistor.
Bit 4 of register address "01100" (DSL register) determines the AGC control current ratio. When DSL will be set to "0", Charge: Discharge ratio will be 7 : 1. When DSL will be set to "1", Charge: Discharge ratio will be 28 : 1.
Bit 5 of register address "01100" (ASL register) determines charge current of AGC. When ASL will be set to "0", the charge current will be 210 µA. When ASL will be set to "1", the charge current will be 420 µA.

Table 1 Charge, Discharge Current of AGC Amp. vs. ASL, DSL Register

Register "01100"

ASL	DSL	Charge Current	Discharge Current
"0"	"0"	210 µA	30 µA
"0"	"1"	210 µA	7.5 µA
"1"	"0"	420 µA	60 µA
"1"	"1"	420 µA	15 µA

The AGC amplifier gain control system is shown in figure 6. The AGC amplifier output is amplified by the post-amplifier then passed through a low-pass filter. The low-pass filter output is connected to the differentiating amplifier, and is also feedback to the AGC control circuit. Here it is compared with reference voltages V_{SH} and V_{SL} that are set internally (V_{SL} is 50 % of V_{SH}), then the external capacitor (CRD) are charged or discharged. The charging and discharging of the external capacitor varies the control signal V_{AGC} which directly affects the gain of the AGC amplifier. The final amplitude V_P (of the AGCINX and AGCINY waveforms) in this control system can be calculated from the following equations, assuming sine waveforms:

$$T_1 \times Ich = T_2 \times Idis \quad (1)$$

(2)

(3)

From equations (1), (2) and (3):

(4)

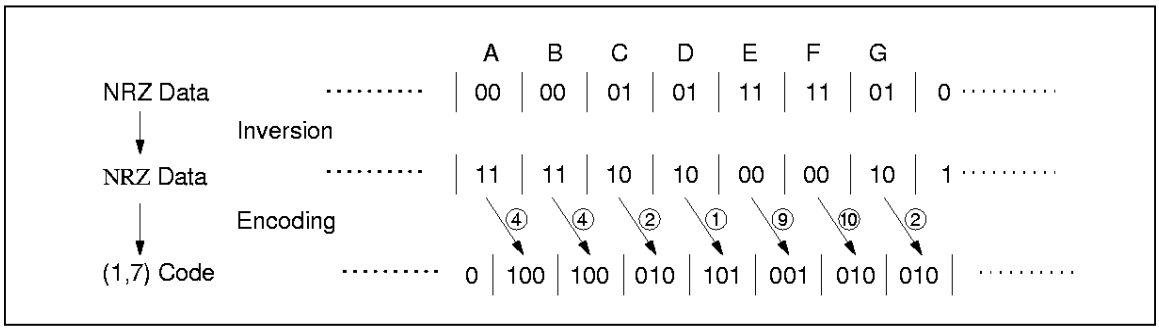


Figure 9 Shows an Example of NRZ to (1, 7) Code Conversion

Table 3 Decoding Table ((1, 7) Code to NRZ)

	(1, 7) Code Bits										
No.	**Previous**			**Current**			**Next**			**NRZ Data Bit**	
1	X	1	0	0	0	0	X	X	X	0	0
2	X	0	0	0	0	0	X	X	X	0	1
3	X	X	X	1	0	0	X	X	X	1	1
4	X	X	0	0	1	0	$\overline{0}$	$\overline{0}$	X	1	0
5	X	X	0	0	1	0	0	0	X	1	1
6	X	X	X	1	0	1	X	X	X	1	0
7	X	0	0	0	0	1	X	X	X	0	1
8	X	1	0	0	0	1	X	X	X	0	0
9	X	X	1	0	0	1	X	X	X	0	0
10	X	X	1	0	1	0	$\overline{0}$	$\overline{0}$	X	0	0
11	X	X	1	0	1	0	0	0	X	0	1
12	X	X	1	0	0	0	X	X	X	0	1

00 : Anything other than 00
X: Don't care

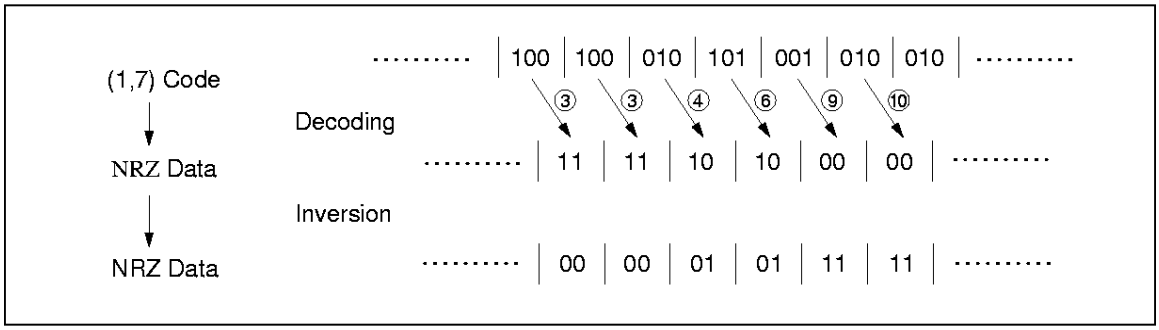
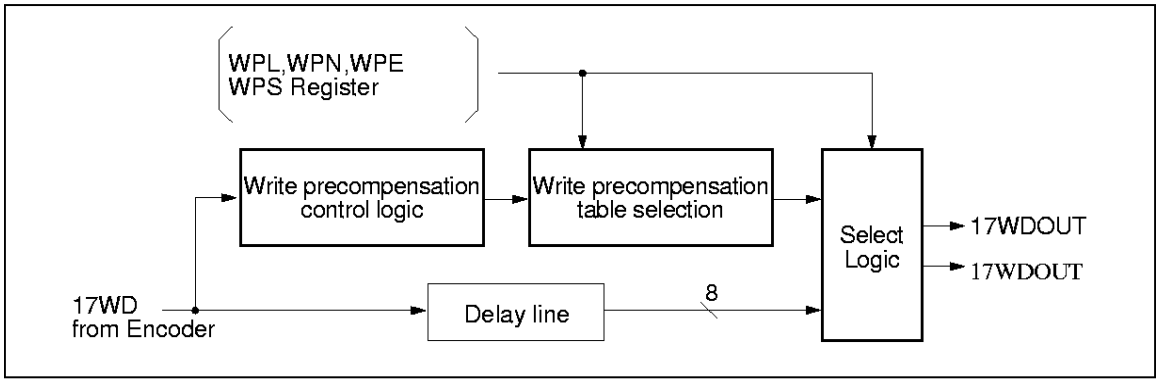


Figure 10 (1, 7) Code to NRZ Decoding Example

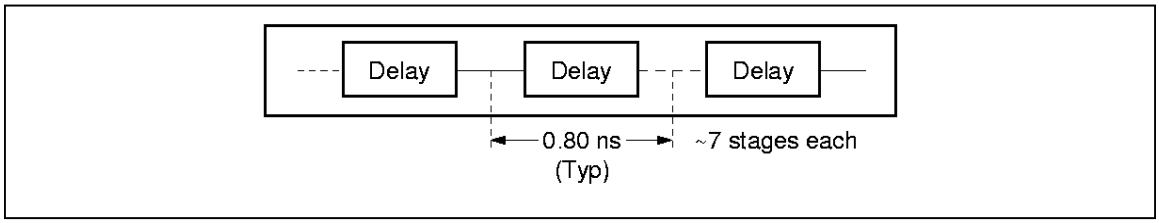
Write Precompensation Circuit

The HD153036TF has a built-in synchronous write precompensation circuit, and the 4 matrix delay levels from the write precompensation table shown below can be selected independently for the NORMAL (N), EARLY (E) and LATE (L) sides. Each delay group of the table can select delay value independently.

(1) Circuit Configuration

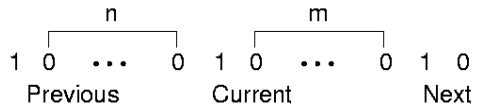


(2) Programmable Delay Line



(3) Table

n \ m	1	2	3	4	5	6	7
1	N	E					
2	L	S					
3							
4							
5							
6							
7							



n : The number of zero's between the current 1 bit and the previous 1 bit

m : The number of zero's between the current 1 bit and the next 1 bit

The precompensation delay time for each the 4 matrix entries in the precompensation table (see Table) can be set independently.
The delay time (8 levels) is selected by the each part of register.

Decode Window Adjustment Circuits

The half window delay circuits select T/2 delay value each transfer rate. The delay value will be controlled by WTS register. When window center adjustment mode, the latch input data's delay will be controlled by WAJ and WTS register. The width of the window adjustment is ±1.8 ns (typ.).

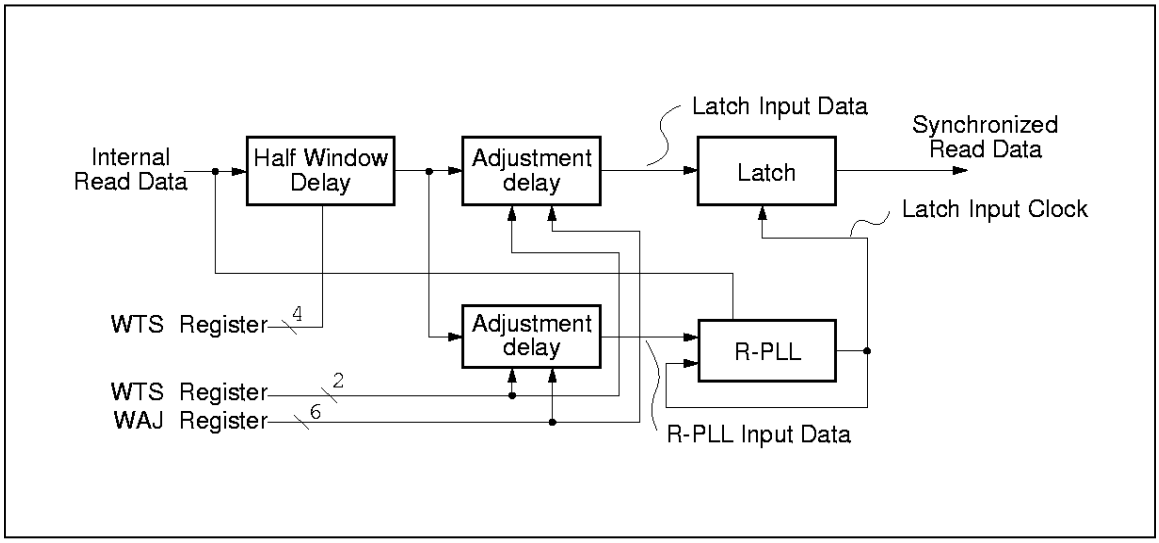


Figure 11 Window Adjustment Circuit Block Diagram

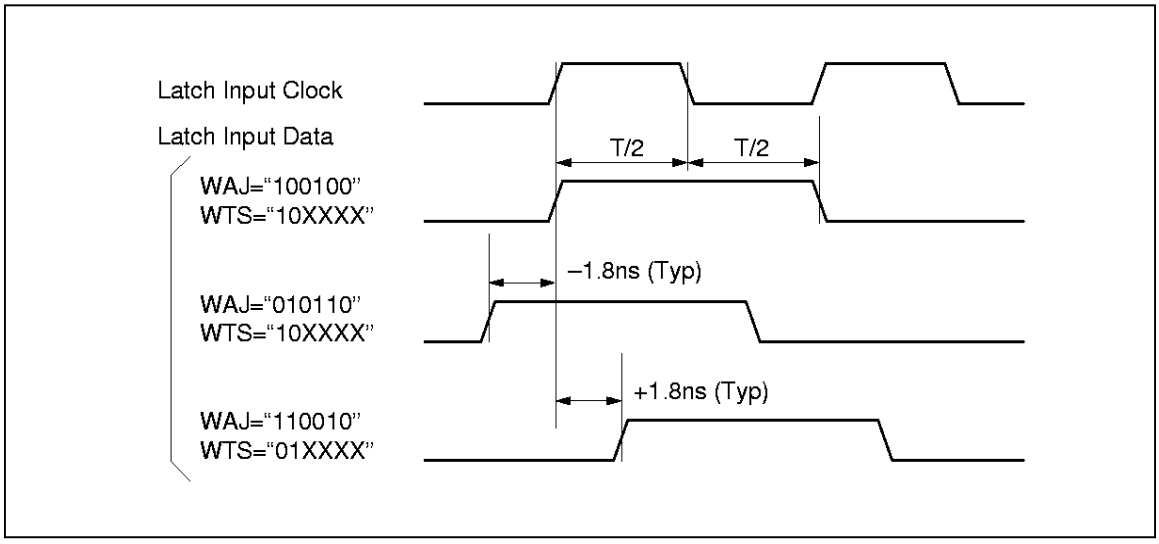


Figure 12 Window Adjustment Timing Waveform

For example, if the NRZ data 00 is to be (1, 7) encoded, it is first inverted to 11.

Next, since the last bit of the previous conversion result A (100) was 0, and the next state of the NRZ data C is 01 (C = 10), the NRZ data B (00) is converted to the (1, 7) code 100.

In decoding the (1, 7) code I (= 100) to NRZ data (see figure 12), since the previous data H was 100 and the next data J is 010, the decoding table gives 11 as the NRZ data. Inverting this gives the NRZ data 00, which is then output.

Sync Field Detection

By using an internal counter to the transitions (24 pulses), the HD153036TF RD-PLL can operate in the high-gain mode immediately after RG is asserted, then automatically switched over to the normal-gain mode after the counter counts 24 transitions (4×6).

It is recommended that the sync field should be of 3T pattern, and that a minimum of "6-NRZ-byte" period is allowed for proper RD-PLL phase locking.

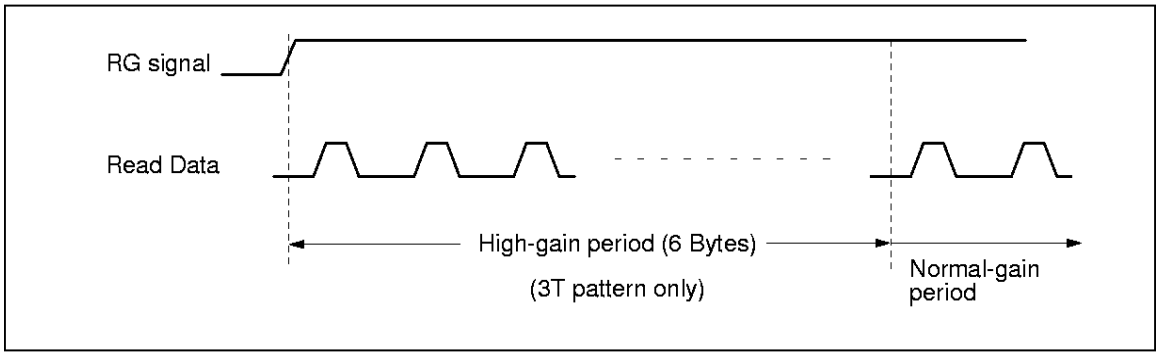


Figure 13 Sync Field Detection Timing

Read and Write Mode

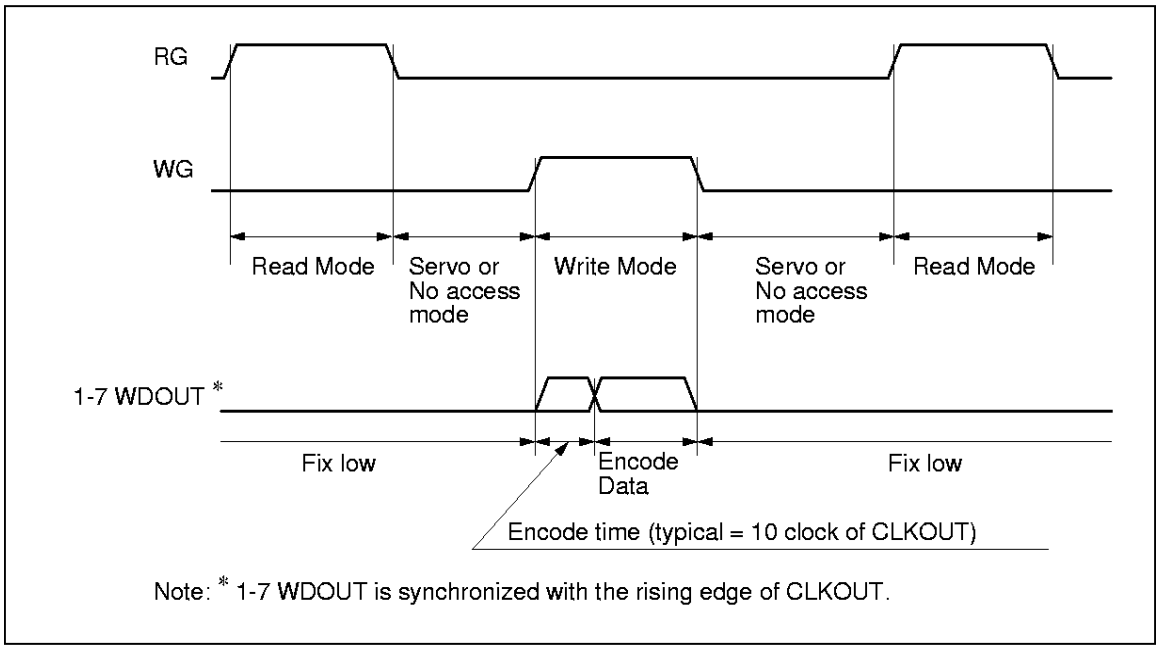
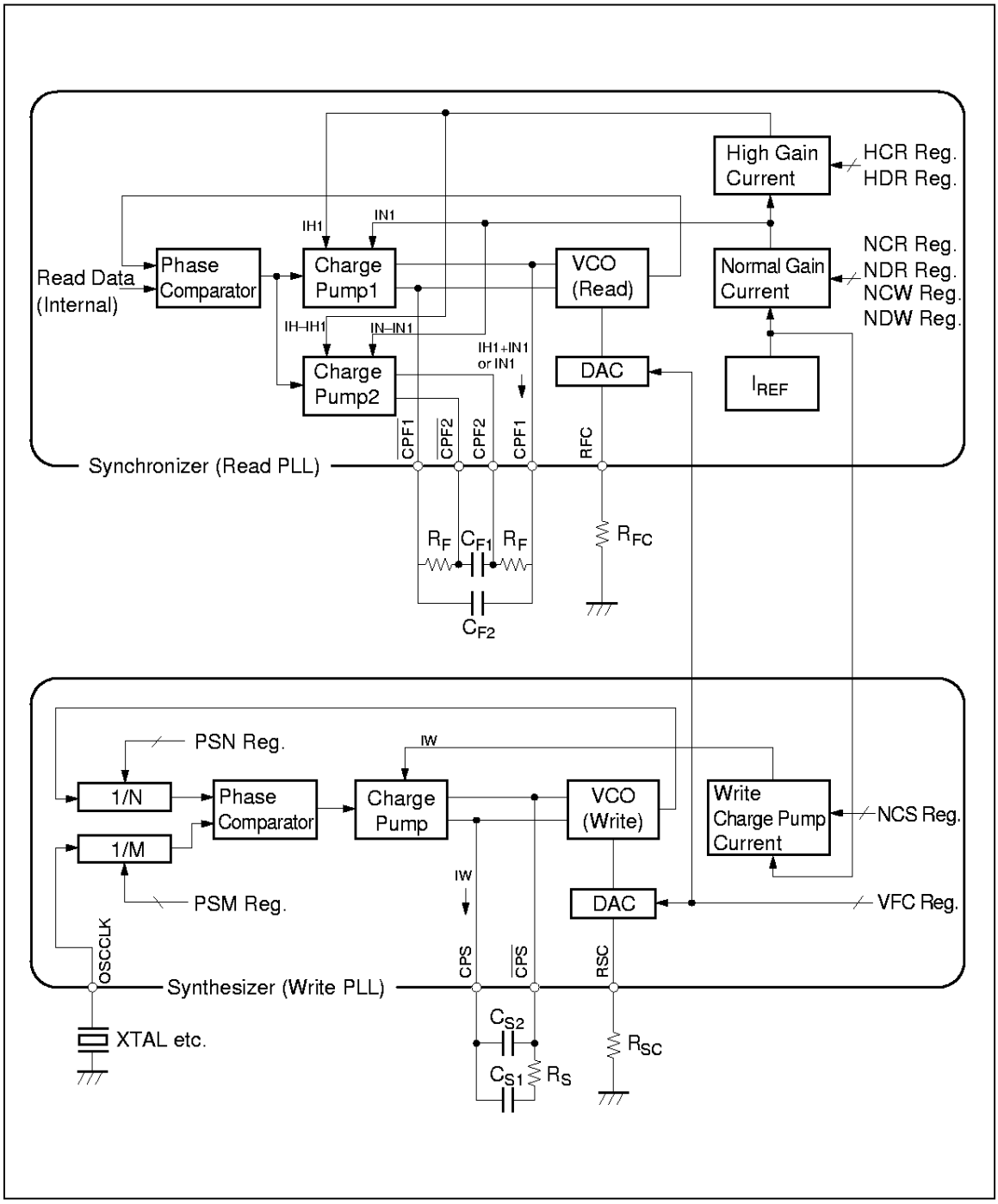


Figure 14 Read and Write Mode Timing

Read and Write PLL Block Diagram



Calculation of PLL Constants

1. Encode Clock Generator's Frequency Synthesizer (W-PLL)

1. VCO center frequency f_{CW}

$$f_{CW} = \frac{(9.90 \times 10^9) \cdot L}{(R_{SC} + 400)} \text{ (Hz)} \quad (1\text{-}1)$$

where $24 \le L \le 63$ (L : VFC register value)

2. VCO oscillation frequency f_{OW}

$$f_{OW} = \frac{N}{M} \cdot f_{OSC} \text{ (Hz)} \quad (1\text{-}2)$$

where $4 \le M \le 255$ (M : PSM register value)
where $4 \le N \le 255$ (N : PSN register value)
fosc : Osc clock's input frequency

3. VCO gain K_{OW}

$$K_{OW} = (2.15 \times 10^9) \cdot \sqrt{\frac{L}{(R_{SC} + 400)}} \left(\frac{\text{rad}}{\text{sec} \cdot \text{V}}\right) \quad (1\text{-}3)$$

where $24 \le L \le 63$ (L : VFC register value)

4. Charge pump current I_W

$$I_W = (2.05 \times 10^{-5}) \cdot (NCS + 1) \text{ (A)} \quad (1.4)$$

where $0 \le NCS \le 15$ (NCS : NCS register value)

5. Characteristic frequency ω_{nW}

$$\omega_{nW} = \sqrt{\frac{K_{OW} \cdot I_W}{2\pi \cdot N \cdot (C_{S1} + C_{S2})}} \left(\frac{\text{rad}}{\text{sec}}\right) \quad (1\text{-}5)$$

where $4 \le N \le 255$ (N : PSN register value)

6. Attenuation ζ_W

$$\zeta_W = \frac{1}{2} \cdot C_{S1} \cdot R_S \cdot \omega_{nW} \quad (1\text{-}6)$$

2. Decode Clock Generator's VFO

1. VCO center frequency f_{CR}

$$f_{CR} = \frac{(9.90 \times 10^9) \cdot L}{(R_{FC} + 400)} \text{ (Hz)} \quad (2\text{-}1)$$

where $24 \le L \le 63$ (L : VFC register value)

2. VCO gain K_{OR}

$$K_{OR} = (7.42 \times 10^9) \cdot \sqrt{\frac{L}{(R_{FC} + 400)}} \left(\frac{\text{rad}}{\text{sec} \cdot \text{V}}\right) \quad (2\text{-}2)$$

where $24 \le L \le 63$ (L : VFC register value)

3. Charge pump normal gain current I_N, I_{N1}

$$I_N = (3.25 \times 10^{-5}) \cdot (NCR + 1) \text{ (A)} \quad (2.3)$$

where $0 \le NCR \le 15$ (NCR : NCR register value)

$$I_{N1} = \frac{NDR + 1}{16} \cdot I_N \text{ (A)} \quad (2\text{-}4)$$

where $0 \le NDR \le 15$ (NDR : NDR register value)

4. Charge pump high gain current I_H, I_{H1}

$$I_H = \frac{HCR + 3}{2} \cdot I_N \text{ (A)} \quad (2\text{-}5)$$

where $0 \le HCR \le 15$ (HCR : HCR register value)

$$I_{H1} = \frac{HDR}{32} (I_H - I_N) + I_{N1} \text{ (A)} \quad (2\text{-}6)$$

where $0 \le HDR \le 15$ (HDR : HDR register value)

5. Charge pump reference gain current I_R, I_{R1}

$$I_N = (3.25 \times 10^{-5}) \cdot (NCW + 1) \text{ (A)} \quad (2.7)$$

where $0 \le NCW \le 15$ (NCW : NCW register value)

$$I_{R1} = \frac{NDW + 1}{16} \cdot I_R \text{ (A)} \quad (2\text{-}8)$$

where $0 \le NDW \le 15$ (NDW : NDW register value)

6. Characteristic frequency (high gain) ω_{nRH}

$$\omega_{nRH} = \sqrt{\frac{K_{OR} \cdot I_H}{2\pi \cdot 3 \cdot (C_{F1} + C_{F2})}} \left(\frac{rad}{sec}\right) \quad (2\text{-}9)$$

7. Characteristic frequency (normal gain) ω_{nRN}

$$\omega_{nRN} = \sqrt{\frac{K_{OR} \cdot I_N}{2\pi \cdot 4 \cdot (C_{F1} + C_{F2})}} \left(\frac{rad}{sec}\right) \quad (2\text{-}10)$$

8. Characteristic frequency (reference gain) ω_{nRR}

$$\omega_{nRR} = \sqrt{\frac{K_{OR} \cdot I_R}{2\pi \cdot 3 \cdot (C_{F1} + C_{F2})}} \left(\frac{rad}{sec}\right) \quad (2\text{-}11)$$

9. Attenuation (high gain) ζ_{RH}

$$\zeta_{RH} = C_{F1} \cdot R_F \cdot \omega_{nRH} \cdot \frac{I_{H1}}{I_H} \quad (2\text{-}12)$$

10. Attenuation (normal gain) ζ_{RN}

$$\zeta_{RN} = C_{F1} \cdot R_F \cdot \omega_{nRN} \cdot \frac{I_{N1}}{I_N} \quad (2\text{-}13)$$

11. Attenuation (reference gain) ζ_{RR}

$$\zeta_{RR} = C_{F1} \cdot R_F \cdot \omega_{nRR} \cdot \frac{I_{R1}}{I_R} \quad (2\text{-}14)$$

Calculation Example of HD153036TF W-PLL Constants

Transfer rate ; 64 Mbps, 32 Mbps, 24 Mbps 3 zones

(1) R_{SC} = 6.2 kΩ
VCO center frequency = 96 MHz (L = 63)

(2) PSM register, PSN register (M, N)

where Transfer rate $= \frac{2}{3} \times f_{OW}$ $f_{OW} = \frac{N}{M} \cdot fosc$

$\therefore$ Transfer rate $= \frac{2}{3} \times \frac{N}{M} \cdot fosc$

where fosc = 12 MHz,
Transfer rate resolution = 500 kbps

$\therefore M = \frac{2}{3} \times \frac{fosc}{500 \times 10^3} = 16$

$\therefore$ Transfer rate $= \frac{2}{3} \times \frac{N}{16} \times 12 \times 10^6$ bps

$\therefore$ 64Mbps $N_{64} = \frac{64 \times 10^6}{12 \times 10^6} \times \frac{3}{2} \times 16 = 128$

32Mbps $N_{32} = \frac{32 \times 10^6}{12 \times 10^6} \times \frac{3}{2} \times 16 = 64$

24Mbps $N_{24} = \frac{24 \times 10^6}{12 \times 10^6} \times \frac{3}{2} \times 16 = 48$

(3) C_{S1}, C_{S2} (calculate from max. transfer rate)

where, $\omega_n \leq \frac{1}{30} \times 2\pi \times \frac{fosc}{M}$

$\omega_n = \frac{1}{40} \times 2\pi \times \frac{12 \times 10^6}{16} = 117.8$krad / s

Max. transfer rate $= \frac{2}{3} \times \frac{128}{16} \times 12 \times 10^6$
$= 64$Mbps

where I_W = max. (NCS = 15)
$I_W = 2.05 \times 10^{-5} \times (15 + 1) = 328.0$ μA
where calculate VCO gain from L

$64 \times 10^6 \times \frac{3}{2} = \frac{9.90 \times 10^9}{6.6 \times 10^3} \times L$

$\therefore L = 63$

$\therefore K_{OW64} = 2.15 \times 10^9 \sqrt{\frac{63}{6.6 \times 10^3}}$
$= 210.1$Mrad / s · V

where $C_{S2} = \frac{C_{S1}}{40}$

$117.8 \times 10^3 = \sqrt{\frac{328.0 \times 10^{-6} \times 210.1 \times 10^6}{2\pi \times 128 \times 41 / 40\, C_{S1}}}$

$\therefore C_{S1} = 6000$pF $C_{S2} = 150$pF
$\omega_{nW64} = 118.0$krad / s

(4) R_S (calculate from max. transfer rate)
where $\zeta_{W64} = 1.0$

$1.0 = \frac{1}{2} \times 6000 \times 10^{-12} \times R_S \times 118.0 \times 10^3$

$\therefore R_S = 2.7$kΩ $\zeta_{W64} = 0.9558$

(5) 32 Mbps

Transfer rate $= \frac{2}{3} \times \frac{64}{16} \times 12 \times 10^6 = 32$Mbps

where calculate VCO gain from L

$32 \times 10^6 \times \frac{3}{2} = \frac{9.90 \times 10^9}{6.6 \times 10^3} \times L$

$\therefore L = 32$

$\therefore K_{OW32} = 2.15 \times 10^9 \sqrt{\frac{32}{6.6 \times 10^3}}$
$= 149.7$Mrad / s · V

where $\omega_{nW64} = \omega_{nW32}$

$118.0 \times 10^3 = \sqrt{\frac{I_W \times 149.7 \times 10^6}{2\pi \times 64 \times 6150 \times 10^{-12}}}$

$\therefore I_W = 230.0$μA

$230.0 \times 10^{-6} = 2.05 \times 10^{-5} \times (NCS + 1)$

$\therefore NCS = 10$ $I_W = 230.0$μA
$\omega_{nRN32} = 118.0$krad / s

$\therefore \zeta_{W32} = \frac{1}{2} \times 6000 \times 10^{-12} \times 2.7 \times 10^3$
$\times 118.0 \times 10^3 = 0.9558$

(6) 24 Mbps

$$\text{Transfer rate} = \frac{2}{3} \times \frac{48}{16} \times 12 \times 10^6 = 24\text{Mbps}$$

where calculate VCO gain from L

$$24 \times 10^6 \times \frac{3}{2} = \frac{9.90 \times 10^9}{6.6 \times 10^3} \times L$$

$$\therefore L = 24$$

$$\therefore K_{OW24} = 2.15 \times 10^9 \sqrt{\frac{24}{6.6 \times 10^3}}$$

$$= 129.6\text{Mrad / s} \cdot \text{V}$$

where $\omega_{nW64} = \omega_{nW24}$

$$118.0 \times 10^3 = \sqrt{\frac{I_W \times 129.6 \times 10^6}{2\pi \times 48 \times 6150 \times 10^{-12}}}$$

$$\therefore I_W = 199.3\mu\text{A}$$

$$199.3 \times 10^{-6} = 2.05 \times 10^{-5} \times (\text{NCS} + 1)$$

$$\therefore \text{NCS} = 9 \quad \text{Ɪ}_W = 205.0\mu\text{A},$$

$$\omega_{nRN24} = 119.7\text{krad / s}$$

$$\therefore \zeta_{W24} = \frac{1}{2} \times 6000 \times 10^{-12} \times 2.7 \times 10^3$$

$$\times 119.7 \times 10^3 = 0.9696$$

Calculation Example of HD153036TF R-PLL Constants

Transfer rate ; 64 Mbps, 32 Mbps, 24 Mbps 3 zones

(1) $R_{FVCO} = 6.2\ k\Omega$
VCO center frequency = 96 MHz(L = 63)

(2) VCO gain K_{OR}

$$K_{OR64} = 7.42 \times 10^9 \sqrt{\frac{63}{6.6 \times 10^3}}$$
$$= 724.9 Mrad / s \cdot V$$

$$K_{OR32} = 7.42 \times 10^9 \sqrt{\frac{32}{6.6 \times 10^3}}$$
$$= 516.7 Mrad / s \cdot V$$

$$K_{OR24} = 7.42 \times 10^9 \sqrt{\frac{24}{6.6 \times 10^3}}$$
$$= 447.4 Mrad / s \cdot V$$

(3) C_{F1}, C_{F2} (calculate from max. transfer rate's high gain)
where $\omega_n \cdot T_{aq64} = 6.0$

$$T_{aq64} = \frac{8}{64 \times 10^6} \cdot 4\ bytes = 500ns$$

$\omega_{nRH64} = 12.0$ Mrad/s

where $C_{F2} = \frac{C_{F1}}{130}$ C_{F1} (min.) = 910pF C
3T sync pattern

$\therefore C_{F1} = 910pF$ $C_{F2} = 7pF$

$$12.0 \times 10^6 = \sqrt{\frac{I_H \times 724.9 \times 10^6}{2\pi \times 3 \times (C_{F1} + C_{F2})}}$$

$\therefore I_H = 3.434mA$

(4) R_F (calculate from min. transfer rate's normal gain)
where $\omega_n \cdot T_{aq24} = 6.0$

$$T_{aq24} = \frac{8}{24 \times 10^6} \cdot 4\ bytes = 1333ns$$

$\omega_{nRH24} = 4.50$ Mrad/s
where $\omega_H = 3.0 \cdot \omega_N$
$\omega_{nRN24} = 1.50$ Mrad/s

$$1.50 \times 10^6 = \sqrt{\frac{I_H \times 447.4 \times 10^6}{2\pi \times 4 \times 917 \times 10^{-12}}}$$

$\therefore I_N = 115.9\mu A$

$115.9 \times 10^{-6} = 3.25 \times 10^{-5} \times (NCR + 1)$

$\therefore NCR = 3$ $I_N = 130.0\mu A$

where NDR = 14 (max. –1)

$$I_{N1} = \frac{14 + 1}{16} \times 130.0 \times 10^{-6} = 121.9\mu A$$

$$\omega_{nRN24} = \sqrt{\frac{130.0 \times 10^{-6} \times 447.4 \times 10^6}{2\pi \times 4 \times 917 \times 10^{-12}}}$$
$$= 1.589 Mrad / s$$

$$\zeta_{RN24} = 910 \times 10^{-12} \times R_F \times 1.589 \times 10^6 \times \frac{121.9 \times 10^{-6}}{130.0 \times 10^{-6}}$$

where $\zeta_{RN24} = 1.0$

$$1.0 = 910 \times 10^{-12} \times R_F \times 1.589 \times 10^6 \times \frac{121.9 \times 10^{-6}}{130.0 \times 10^{-6}}$$

$\therefore R_F = 750\Omega$ $\zeta_{RN24} = 1.0169$

(5) 64 Mbps normal gain
where $\omega_H = 3.0 \cdot \omega_N$
$\omega_{nRN64} = 4.0$ Mrad/s

$$4.0 \times 10^6 = \sqrt{\frac{I_N \times 724.9 \times 10^6}{2\pi \times 4 \times 917 \times 10^{-12}}}$$

$\therefore I_N = 508.7\mu A$

$508.7 \times 10^{-6} = 3.25 \times 10^{-5} \times (NCR + 1)$

$\therefore NCR = 14$ $I_N = 487.5\mu A$ C

$\omega_{nRN64} = 3.916$Mrad / s

where $\zeta_{RN64} = 1.0$

$$1.0 = 910 \times 10^{-12} \times 750 \times 3.916 \times 10^6 \times \frac{I_{N1}}{487.5 \times 10^{-6}}$$

$\therefore I_{N1} = 182.4\mu A$

$$182.4 \times 10^{-6} = \frac{NDR + 1}{16} \times 487.5 \times 10^{-6}$$

$\therefore NDR = 5$ $I_{N1} = 182.8\mu A$

$$\zeta_{RN64} = 910 \times 10^{-12} \times 750 \times 3.916 \times 10^6 \times \frac{5 + 1}{16}$$

$\therefore \zeta_{RN64} = 1.0023$

(6) 64 Mbps high gain

ω_{nRH64} = 12.0 Mrad/s

$$12.0 \times 10^6 = \sqrt{\frac{I_H \times 724.9 \times 10^6}{2\pi \times 3 \times 917 \times 10^{-12}}}$$

$$\therefore I_H = 3.434\text{mA}$$

$$3.434 \times 10^{-3} = \frac{HCR + 3}{2} \times 487.5 \times 10^{-6}$$

$$\therefore HCR = 11 \quad \text{Ø} I_H = 3.413\text{mA} \quad \text{C}$$

$$\omega_{nRH64} = 11.964\text{Mrad / s}$$

where $\zeta_{RH64} = 0.7$

$$0.7 = 910 \times 10^{-12} \times 750 \times 11.964 \times 10^6 \times \frac{I_{H1}}{3.413 \times 10^{-3}}$$

$$\therefore I_{H1} = 292.6\mu\text{A}$$

$$292.6 \times 10^{-6} = \frac{HDR}{32} \times \left\{(3.413 \times 10^{-3}) - (487.5 \times 10^{-6})\right\} + 182.8 \times 10^{-6}$$

$$\therefore HDR = 1 \quad \text{Ø} I_{H1} = 274.2\mu\text{A}$$

$$\zeta_{RH64} = 910 \times 10^{-12} \times 750 \times 11.964 \times 10^6 \times \frac{274.2 \times 10^{-6}}{3.413 \times 10^{-3}}$$

$$\therefore \zeta_{RH64} = 0.656$$

(7) 64 Mbps reference gain

where $\omega_{nRR64} = \omega_{nRN64}$

$$4.0 \times 10^6 = \sqrt{\frac{I_R \times 724.9 \times 10^6}{2\pi \times 3 \times 917 \times 10^{-12}}}$$

$$\therefore I_R = 381.5\mu\text{A}$$

$$381.5 \times 10^{-6} = 3.25 \times 10^{-5} \times (NCW + 1)$$

$$\therefore NCW = 11 \quad \text{Ø} I_R = 390.0\mu\text{A} \quad \text{C}$$

$$\omega_{nRR64} = 4.044\text{Mrad / s}$$

where $\zeta_{RR64} = 1.0$

$$1.0 = 910 \times 10^{-12} \times 750 \times 4.044 \times 10^6 \times \frac{I_{R1}}{390.0 \times 10^{-6}}$$

$$\therefore I_{R1} = 141.3\mu\text{A}$$

$$141.3 \times 10^{-6} = \frac{NDW + 1}{16} \times 390.0 \times 10^{-6}$$

$$\therefore NDW = 5 \quad \text{Ø} I_{R1} = 146.3\mu\text{A}$$

$$\zeta_{RR64} = 910 \times 10^{-12} \times 750 \times 4.044 \times 10^6 \times \frac{5 + 1}{16}$$

$$\therefore \zeta_{RR64} = 1.0350$$

(8) 32 Mbps normal gain

from the above ω_{nRN24}

$$\zeta_{nRN32} = 1.5 \times 10^6 \times \frac{32 \times 10^6}{24 \times 10^6} = 2.0\text{Mrad / s}$$

$$2.0 \times 10^6 = \sqrt{\frac{I_N \times 516.7 \times 10^6}{2\pi \times 4 \times 917 \times 10^{-12}}}$$

$$\therefore I_N = 178.4\mu\text{A}$$

$$178.4 \times 10^{-6} = 3.25 \times 10^{-5} \times (NCR + 1)$$

$$\therefore NCR = 4 \quad \text{Ø} I_N = 162.5\mu\text{A} \quad \text{C}$$

$$\omega_{nRN32} = 1.909\text{Mrad / s}$$

where $\zeta_{RN32} = 1.0$

$$1.0 = 910 \times 10^{-12} \times 750 \times 1.909 \times 10^6 \times \frac{I_{N1}}{162.5 \times 10^{-6}}$$

$$\therefore I_{N1} = 124.7\mu\text{A}$$

$$124.7 \times 10^{-6} = \frac{NDR + 1}{16} \times 162.5 \times 10^{-6}$$

$$\therefore NDR = 11 \quad \text{Ø} I_{N1} = 121.9\mu\text{A}$$

$$\zeta_{RN32} = 910 \times 10^{-12} \times 750 \times 1.909 \times 10^6 \times \frac{11 + 1}{16}$$

$$\therefore \zeta_{RN32} = 0.9772$$

(9) 32 Mbps high gain

where $\omega_n \cdot T_{aq32} = 6.0$

$$T_{aq32} = \frac{8}{32 \times 10^6} \cdot 4 \text{ bytes} = 1000\text{ns}$$

$$\omega_{nRH32} = 6.0\text{Mrad/s}$$

$$6.0 \times 10^6 = \sqrt{\frac{I_H \times 516.7 \times 10^6}{2\pi \times 3 \times 917 \times 10^{-12}}}$$

$$\therefore I_H = 1.204\text{mA}$$

$$1.204 \times 10^{-3} = \frac{HCR + 3}{2} \times 162.5 \times 10^{-6}$$

$$\therefore HCR = 12 \quad \text{Ó}_H = 1.219\text{mA} \quad \text{C}$$

$$\omega_{nRH32} = 6.037\text{Mrad/s}$$

where $\zeta_{RH32} = 0.7$

$$0.7 = 910 \times 10^{-12} \times 750 \times 6.037 \times 10^6 \times \frac{I_{H1}}{1.219 \times 10^{-3}}$$

$$\therefore I_{H1} = 207.1\mu\text{A}$$

$$207.1 \times 10^{-6} = \frac{HDR}{32} \times \left\{(1.219 \times 10^{-3}) - (162.5 \times 10^{-6})\right\} + 121.9 \times 10^{-6}$$

$$\therefore HDR = 3 \quad \text{Ó}_{N1} = 220.9\mu\text{A}$$

$$\zeta_{RH32} = 910 \times 10^{-12} \times 750 \times 6.037 \times 10^6 \times \frac{220.9 \times 10^{-6}}{1.219 \times 10^{-3}}$$

$$\therefore \zeta_{RH32} = 0.7466$$

(10) 32 Mbps reference gain

where $\omega_{nRR32} = \omega_{nRN32}$

$$2.0 \times 10^6 = \sqrt{\frac{I_R \times 516.7 \times 10^6}{2\pi \times 3 \times 917 \times 10^{-12}}}$$

$$\therefore I_R = 133.8\mu\text{A}$$

$$133.8 \times 10^{-6} = 3.25 \times 10^{-5} \times (NCW + 1)$$

$$\therefore NCW = 3 \quad \text{Ó}_R = 130.0\mu\text{A} \quad \text{C}$$

$$\omega_{nRR32} = 1.971\text{Mrad/s}$$

where $\zeta_{RR32} = 1.0$

$$1.0 = 910 \times 10^{-12} \times 750 \times 1.971 \times 10^6 \times \frac{I_{R1}}{130.0 \times 10^{-6}}$$

$$\therefore I_{R1} = 96.6\mu\text{A}$$

$$96.6 \times 10^{-6} = \frac{NDW + 1}{16} \times 130.0 \times 10^{-6}$$

$$\therefore NDW = 11 \quad \text{Ó}_{R1} = 97.5\mu\text{A}$$

$$\zeta_{RR32} = 910 \times 10^{-12} \times 750 \times 1.971 \times 10^6 \times \frac{11 + 1}{16}$$

$$\therefore \zeta_{RR32} = 1.0089$$

(11) 24 Mbps normal gain

$\omega_{nRN24} = 1.376$ Mrad/s

NCR = 3, $I_N = 130.0\ \mu\text{A}$

NDR = 14, $I_{N1} = 121.9\ \mu\text{A}$

$\zeta_{RN32} = 1.0169$

(12) 24 Mbps high gain

$\omega_{nRH24} = 4.5$ Mrad/s

$$\therefore I_H = 782.3\mu\text{A}$$

$$782.3 \times 10^{-6} = \frac{HCR + 3}{2} \times 130.0 \times 10^{-6}$$

$$\therefore HCR = 9 \quad \text{Ó}_H = 780.0\mu\text{A} \quad \text{C}$$

$$\omega_{nRH24} = 4.493\text{Mrad/s}$$

where $\zeta_{RH24} = 0.7$

$$0.7 = 910 \times 10^{-12} \times 750 \times 4.493 \times 10^6 \times \frac{I_{H1}}{780.0 \times 10^{-6}}$$

$$\therefore I_{H1} = 178.1\mu\text{A}$$

$$178.1 \times 10^{-6} = \frac{HDR}{32} \times \left\{(780.0 \times 10^{-6}) - (130.0 \times 10^{-6})\right\} + 121.9 \times 10^{-6}$$

$$\therefore HDR = 3 \quad \text{Ó}_{N1} = 182.8\mu\text{A}$$

$$\zeta_{RH24} = 910 \times 10^{-12} \times 750 \times 4.493 \times 10^6 \times \frac{182.8 \times 10^{-6}}{780.0 \times 10^{-6}}$$

$$\therefore \zeta_{RH24} = 0.7187$$

(13) 24 Mbps reference gain

where $\omega_{nRR24} = \omega_{nRN24}$

$$1.5 \times 10^6 = \sqrt{\frac{I_R \times 447.4 \times 10^6}{2\pi \times 3 \times 917 \times 10^{-12}}}$$

$$\therefore I_R = 86.9\mu A$$

$$86.9 \times 10^{-6} = 3.25 \times 10^{-5} \times (NCW + 1)$$

$$\therefore NCW = 2 \quad \text{C}_R = 97.5\mu A \quad \text{C}$$

$$\omega_{nRR24} = 1.589 Mrad/s$$

where $\zeta_{RR24} = 1.0$

$$1.0 = 910 \times 10^{-12} \times 750 \times 1.589 \times 10^6 \times \frac{I_{R1}}{97.5 \times 10^{-6}}$$

$$\therefore I_{R1} = 89.9\mu A$$

$$89.9 \times 10^{-6} = \frac{NDW + 1}{16} \times 97.5 \times 10^{-6}$$

$$\therefore NDW = 14 \quad \text{C}_{R1} = 91.4\mu A$$

$$\zeta_{RR24} = 910 \times 10^{-12} \times 750 \times 1.589 \times 10^6 \times \frac{14 + 1}{16}$$

$$\therefore \zeta_{RR24} = 1.0167$$

Calculation of PLL Constants

1. Encode Clock Generator's Frequency Synthesizer (W-PLL)

1. VCO center frequency f_{CW}

(1-1)

where $24 \leq L \leq 63$ (L : VFC register value)

2. VCO oscillation frequency f_{OW}

(1-2)

where $4 \leq M \leq 255$ (M : PSM register value)
where $4 \leq N \leq 255$ (N : PSN register value)
fosc : Osc clock's input frequency

3. VCO gain K_{OW}

(1-3)

where $24 \leq L \leq 63$ (L : VFC register value)

4. Charge pump current I_W

$I_W = (2.05 \times 10^{-5}) \cdot (NCS + 1)$ (A) (1.4)

where $0 \leq NCS \leq 15$ (NCS : NCS register value)

5. Characteristic frequency ω_{nW}

(1-5)

where $4 \leq N \leq 255$ (N : PSN register value)

6. Attenuation ζ_W

(1-6)

2. Decode Clock Generator's VFO

1. VCO center frequency f_{CR}

(2-1)

where $24 \leq L \leq 63$ (L : VFC register value)

2. VCO gain K_{OR}

(2-2)

where $24 \leq L \leq 63$ (L : VFC register value)

3. Charge pump normal gain current I_N, I_{N1}

$I_N = (3.25 \times 10^{-5}) \cdot (NCR + 1)$ (A) (2.3)

where $0 \leq NCR \leq 15$ (NCR : NCR register value)

(2-4)

where $0 \leq NDR \leq 15$ (NDR : NDR register value)

4. Charge pump high gain current I_H, I_{H1}

(2-5)

where $0 \leq HCR \leq 15$ (HCR : HCR register value)

(2-6)

where $0 \leq HDR \leq 15$ (HDR : HDR register value)

5. Charge pump reference gain current I_R, I_{R1}

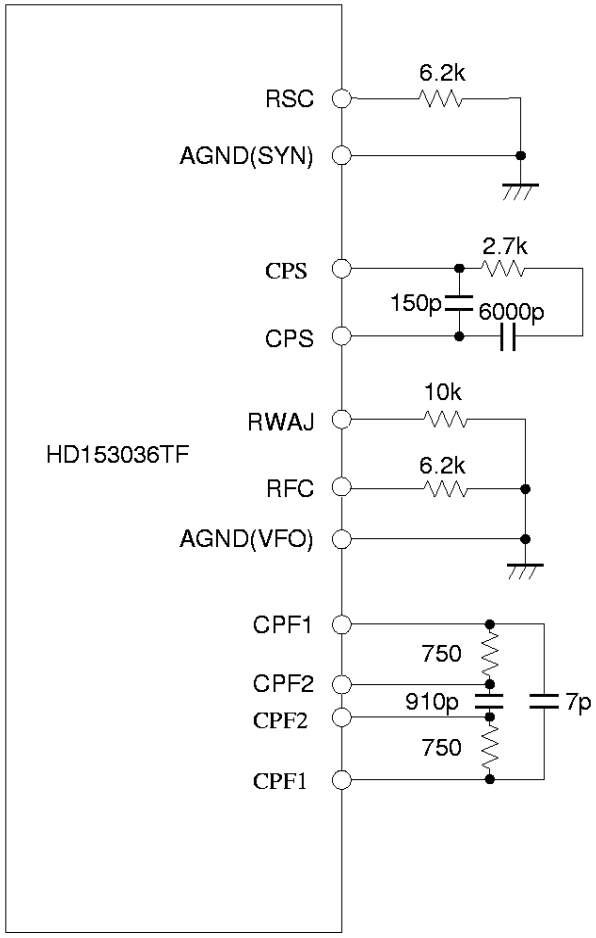
$I_N = (3.25 \times 10^{-5}) \cdot (NCW + 1)$ (A) (2.7)

where $0 \leq NCW \leq 15$ (NCW : NCW register value)

(2-8)

where $0 \leq NDW \leq 15$ (NDW : NDW register value)

Example of External Components Connected to the R-PLL & W-PLL



Unit R: Ω
C: F

10. Attenuation (normal gain) ζ_{RN}

(2-13)

11. Attenuation (reference gain) ζ_{RR}

(2-14)

Calculation Example of HD153036TF W-PLL Constants

Transfer rate ; 64 Mbps, 32 Mbps, 24 Mbps 3 zones

(1) R_{SC} = 6.2 kΩ
VCO center frequency = 96 MHz (L = 63)

(2) PSM register, PSN register (M, N)

—

where fosc = 12 MHz,
Transfer rate resolution = 500 kbps

(3) C_{S1}, C_{S2} (calculate from max. transfer rate)

where I_W = max. (NCS = 15)
$I_W = 2.05 \times 10^{-5} \times (15 + 1) = 328.0$ μA
where calculate VCO gain from L

(4) R_S (calculate from max. transfer rate)
where $\zeta_{W64} = 1.0$

(5) 32 Mbps

where calculate VCO gain from L

where $\omega_{nW64} = \omega_{nW32}$

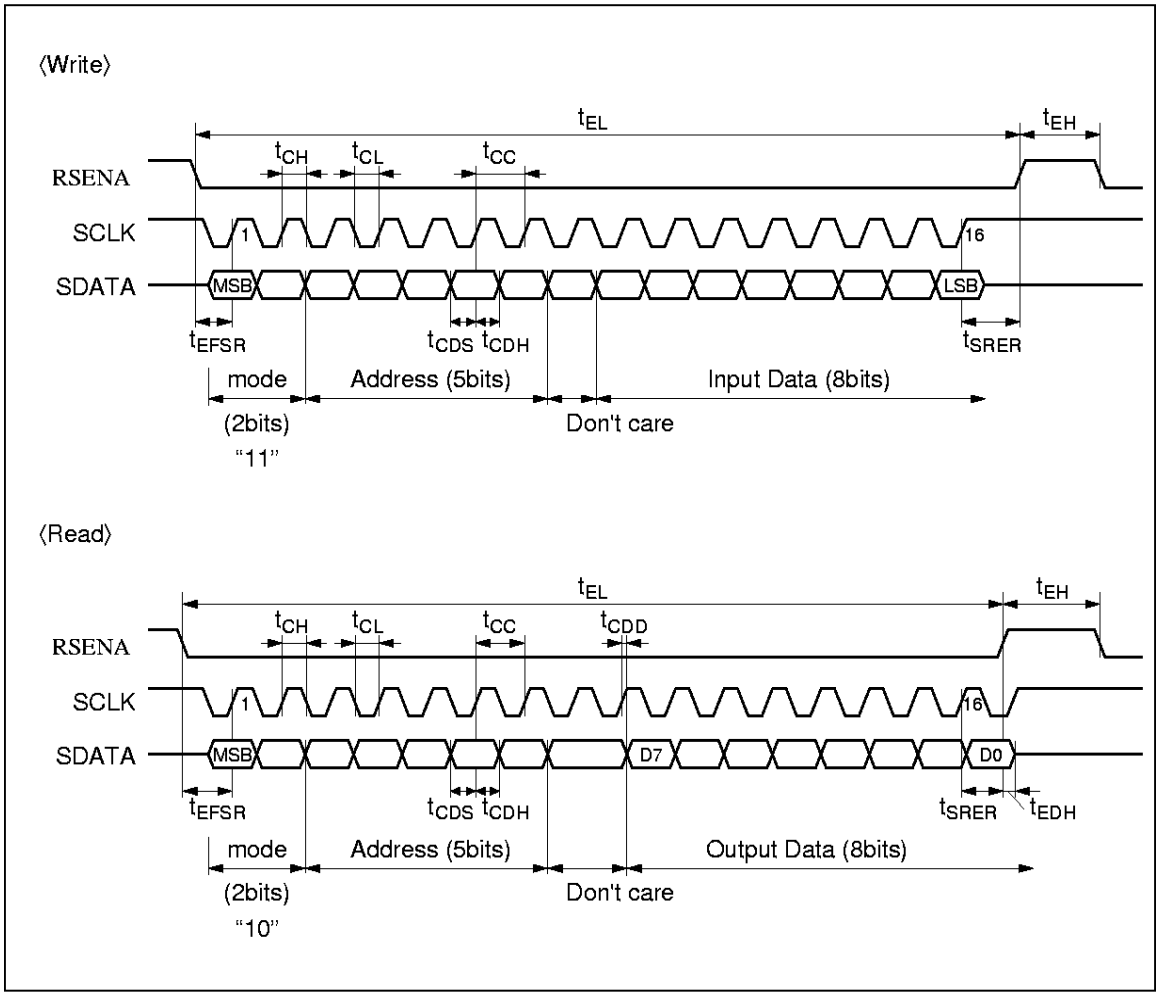
(6) 24 Mbps

where calculate VCO gain from L

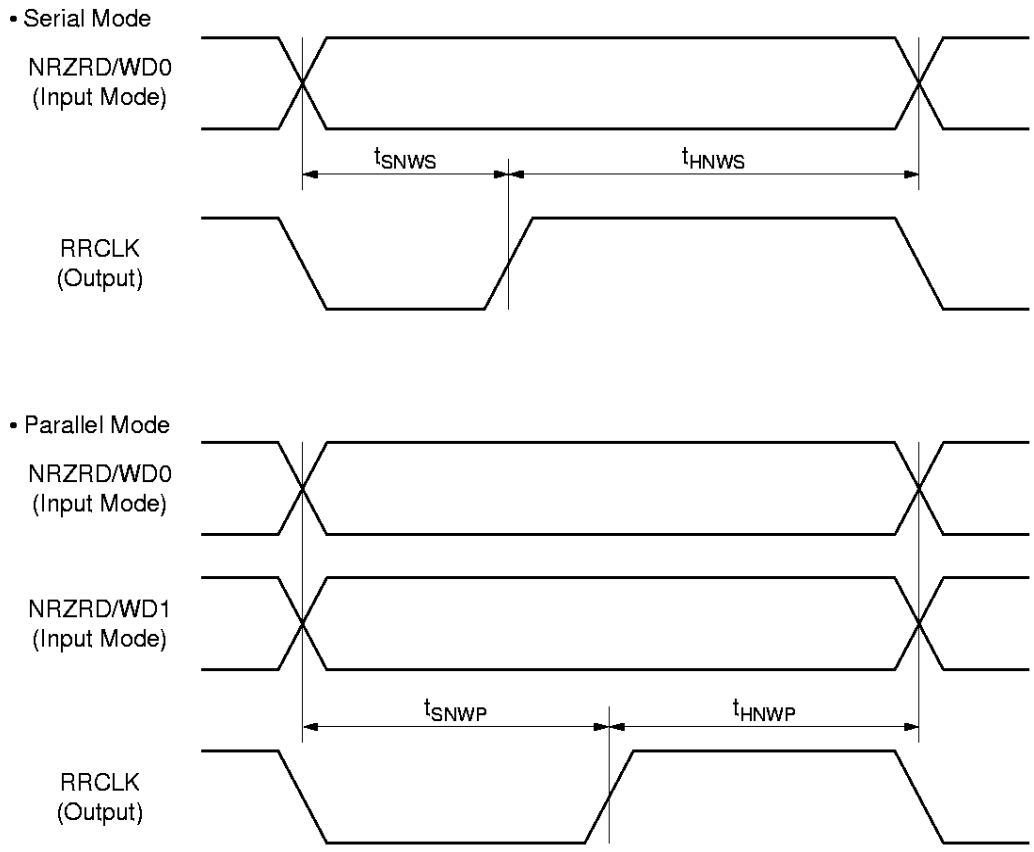
where $\omega_{nW64} = \omega_{nW24}$

AC Timing Chart

(1) Register Read / Write

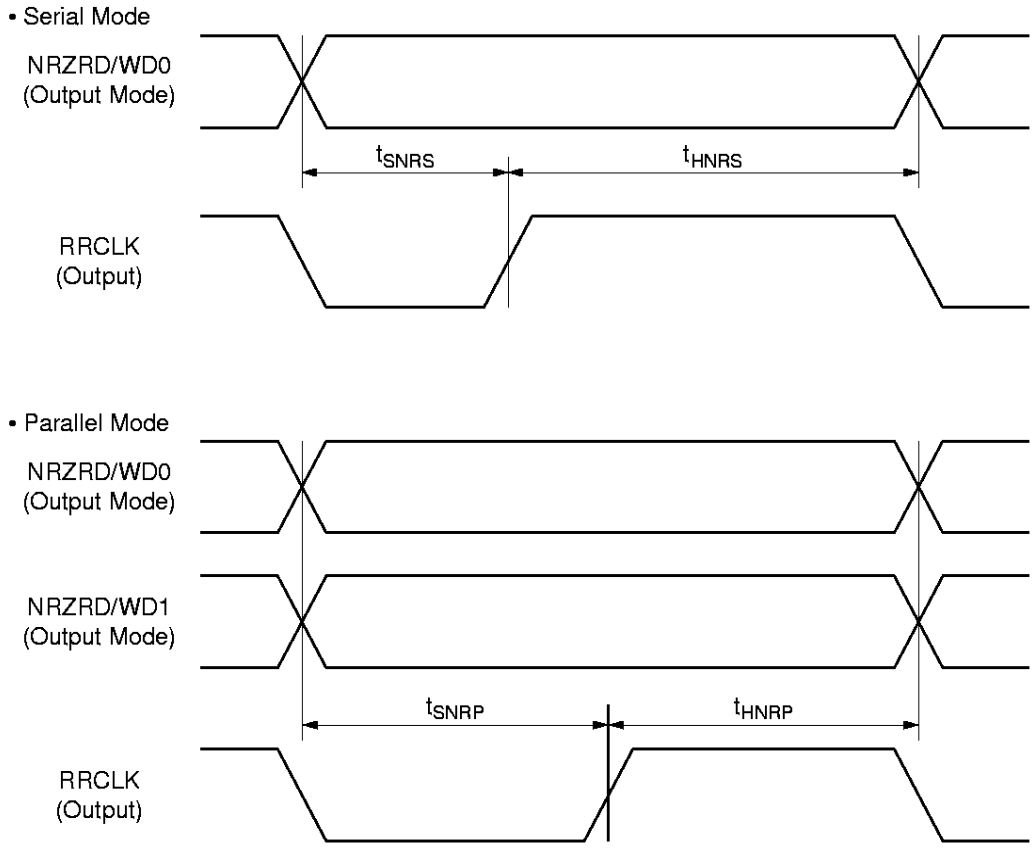


(2) Write for NRZ Data



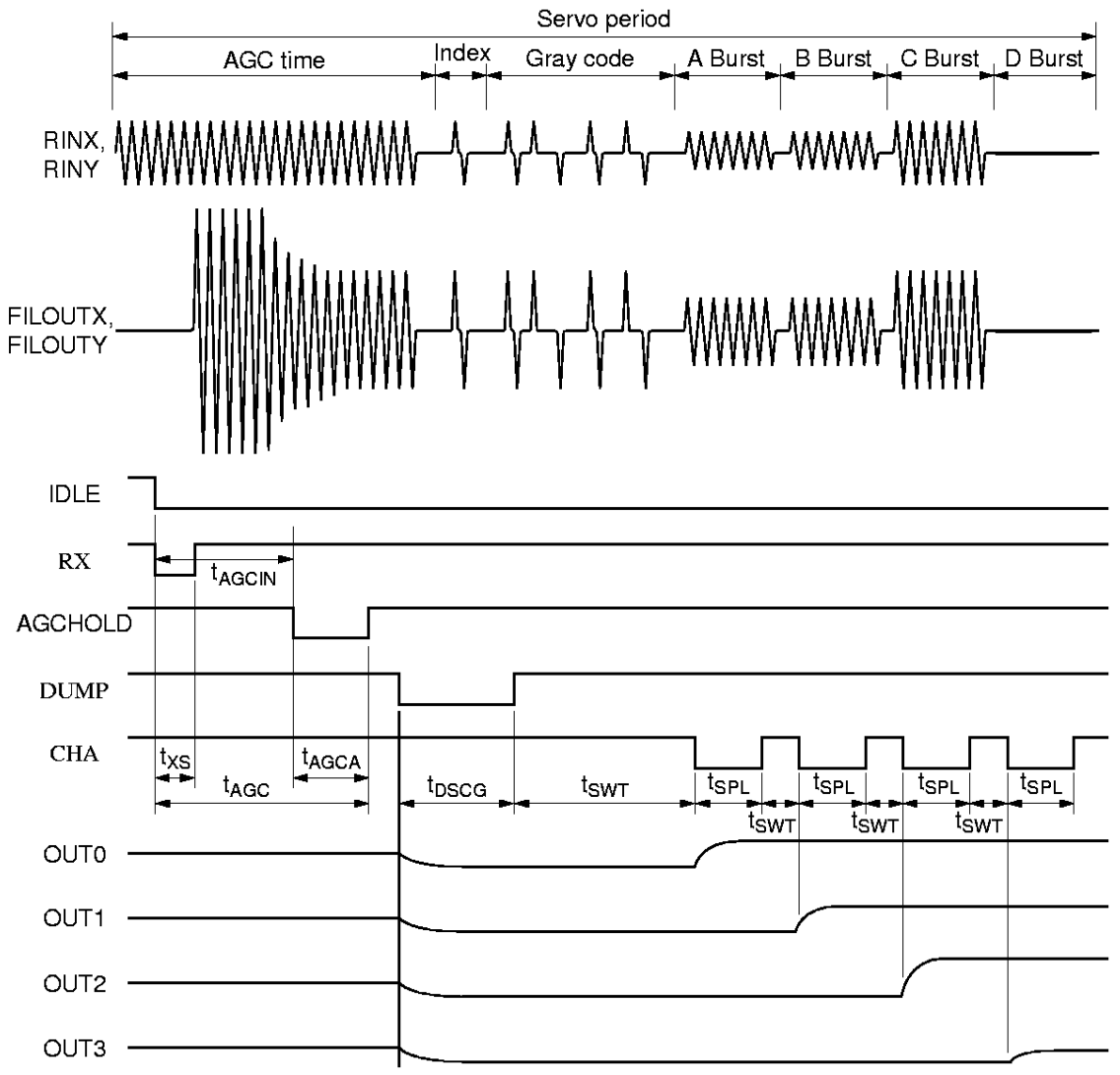
Note: When data transfer rate is 40Mbps (Serial Mode), RRCLK output is 40MHz.
RRCLK clock duty "L" : "H" = 1 : 2.
When data transfer rate is 40Mbps (Parallel Mode), RRCLK output is 20MHz.
RRCLK clock duty "L" : "H" = 1 : 1.
We recommend that more than 40Mbps, please select the "Parallel" mode.

(3) Read for NRZ Data



Note: When data transfer rate is 40Mbps (Serial Mode), NRZ and RRCLK output is 40MHz.
RRCLK clock duty "L" : "H" = 1 : 2.
When data transfer rate is 40Mbps (Parallel Mode), NRZ and RRCLK output is 20MHz.
RRCLK clock duty "L" : "H" = 1 : 1.
We recommend that more than 40Mbps, please select the "Parallel" mode.

Example of The Idle to Servo Mode Waveform

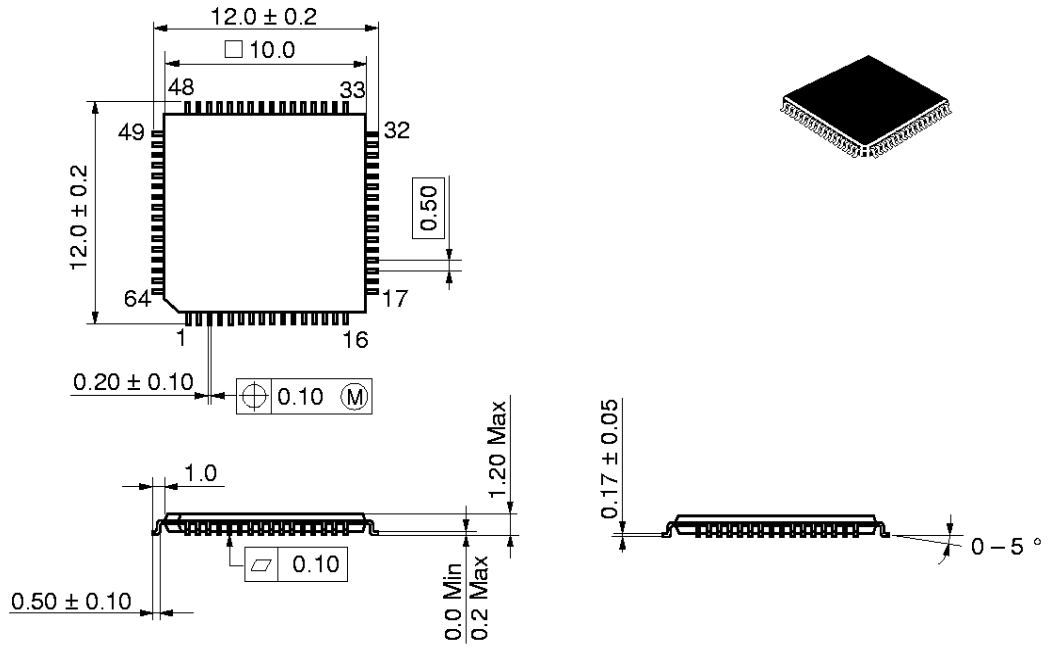


During D Burst, no signal coming out.

Symbol	Min	Typ	Max	Unit	Conditions
t_{XS}	6.0	—	—	µs	C_{AGCIN}=2200 pF A0C=28 Hex
t_{AGCA}	—	3.0	6.0	µs	CRD=5600 pF A0C=28 Hex
t_{DSCG}	—	—	1.0	µs	
t_{SWT}	100	200	—	µs	
t_{SPL}	—	1.0	1.7	µs	Register A14=08 Hex
t_{AGCIN}	10.0	—	—	µs	C_{AGCIN}=2200 pF A0C=28 Hex

Package Dimensions

Unit: mm



Hitachi Code	TFP-64B
EIAJ	—
JEDEC	—

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ADE-207-189 (Z) Printed in Japan