



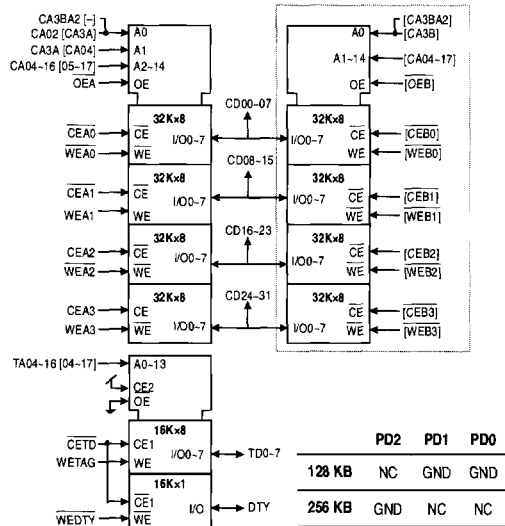
Features

- ◆ Cache + tag + dirty module
- ◆ High performance
 - 15 / 20 ns cache address access time
 - 50 / 33 MHz i486™ bus frequency
 - CPU speeds to 100 MHz
- ◆ Industry's lowest power consumption
- ◆ Multiple chipset support

Pin Configuration

PD0	1	65	PD1	WEA2	33	97	WEB2
PD2	2	66	GND	WEA3	34	98	WEB3
CD00	3	67	CD01	WETAG	35	99	WEDTY
CD02	4	68	CD03	CETD	36	100	Vcc
CD04	5	69	Vcc	NC	37	101	NC
CD06	6	70	CD05	NC	38	102	NC
CD08	7	71	CD07	CA3A	39	103	CA3BA2
GND	8	72	CD09	CA02	40	104	CA3B
CD10	9	73	CD11	GND	41	105	GND
CD12	10	74	CD13	CA04	42	106	CA05
CD14	11	75	CD15	CA06	43	107	CA07
CD16	12	76	CD17	CA08	44	108	CA09
CD18	13	77	CD19	CA10	45	109	CA11
CD20	14	78	CD21	CA12	46	110	CA13
GND	15	79	GND	CA14	47	111	CA15
CD22	16	80	CD23	CA16	48	112	CA17
CD24	17	81	CD25	NC	49	113	NC
Vcc	18	82	Vcc	GND	50	114	GND
CD26	19	83	CD27	TA04	51	115	TA05
CD28	20	84	CD29	TA06	52	116	TA07
CD30	21	85	CD31	TA08	53	117	TA09
NC	22	86	NC	TA10	54	118	TA11
NC	23	87	NC	TA12	55	119	TA13
GND	24	88	GND	TA14	56	120	TA15
CEA0	25	89	CEB0	TA16	57	121	TA17
CEA1	26	90	CEB1	NC	58	122	NC
CEA2	27	91	Vcc	GND	59	123	GND
CEA3	28	92	CEB2	TD0	60	124	TD1
GND	29	93	CEB3	TD2	61	125	TD3
OEA	30	94	OEB	TD4	62	126	TD5
WEA0	31	95	WEB0	TD6	63	127	TD7
WEA1	32	96	WEB1	DTY	64	128	Vcc

Logic Block Diagram



Overview

The AS7M32D128 and AS7M32D256 are members of Alliance's cache module family for 486 processors. The modules feature one or two 128KByte 32-bit-wide banks of cache data storage, plus 8-bit-wide tag and 1-bit-wide 'dirty' storage for a complete cache subsystem in a DIMM2x64 package. Speeds are optimized for 50 and 33 MHz system bus frequency.

Selection Guide

	7M32D128		7M32D256		Unit	
	D128-15	D128-20	D256-15	D256-20		
Cache size	128K	128K	256K	128K	byte	
Tag+dirty size	8Kx9	8Kx9	16Kx9	8Kx9	bits	
Maximum access time (cache/tag)	t_{AA}	15/12	15/12	20/15	ns	
Recommended system bus frequency	f_{max}	50	33	50	33	MHz
Maximum operating current	I_{CC}	700	650	1150	1050	mA
Maximum CMOS standby current	I_{SB}	15	15	25	25	mA