Rad-Hard
32-bit SPARC
Embedded Processor

Data Sheet

Preliminary

Data Sheet Information

Foreword

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Preview	This Data Sheet contains the targeted specifications, all electrical parameters correspond to either targeted or simulated values. Specifications may change in any manner without notice.
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1. Overview

The TSC695E (ERC32 Single-Chip) is a highly integrated, high-performance 32-bit RISC embedded processor implementing the SPARC architecture V7 specification. It has been developed with the support of the ESA (European Space Agency), and is offering a full development environment for embedded space applications.

The processor is manufactured using the TEMIC 0.5 µm radiation tolerant (≥ 300 KRADs (Si)) CMOS enhanced process (RTP). It can operate at a low voltage for optimized power consumption. It has been especially designed for space, as it has on-chip concurrent transient and permanent error detection.

The TSC695E includes on chip an Integer Unit (IU), a Floating Point Unit (FPU), a Memory Controller and a DMA Arbiter. For Real Time applications, the TSC695E offers a high security Watch Dog, two Timer's, an Interrupt Controller, Parallel and Serial interfaces. Fault tolerance is supported using parity on internal/external buses and an EDAC on the external data bus. The design is highly testable with the support of an On-Chip Debugger (OCD), an internal and boundary scan through JTAG interface.

2. Features

- Integer Unit based on SPARC V7 high performance RISC architecture
- Optimized integrated 32/64-bit floating-point unit
- On-chip peripherals:
  - EDAC and parity generator and checker
  - Memory interface:
    - chip select generator
    - waitstate generation
    - memory protection
  - DMA arbiter
  - Timers:
    - General purpose timer (GPT)
    - Real time clock timer (RTCT)
    - Watch dog timer (WDT)
  - Interrupt controller with 5 external inputs
  - General purpose interface (GPI)
  - Dual UART
- Speed optimized code RAM interface
  8 or 32-bit boot-PROM (Flash) interface
- IEEE 1149.1 test access port (TAP) for debugging and test purposes
- Fully static design
- Performance: 25 MIPs / 5 MFlops (double precision) @ SYSCLK = 35 MHz - 5 V
  14 MIPs / 3 MFlops (double precision) @ SYSCLK = 20 MHz - 3 V
- Core consumption: 1.5 W typ. @ 25 MIPs / 0.7 W typ. @ 10 MIPs - Vcc = 5 V
  0.4 W typ. @ 14 MIPs / 0.2 W typ. @ 6 MIPs - Vcc = 3 V
- Operating range: 2.7 V to 5.5 V (2.5 V capability) -55 °C to +125 °C
- Total dose radiation capability (parametric & functional): 300 KRADs (Si)
- SEU event rate better than $1E^{-8}$ error/component/day (worst case)
- Latch up immunity better than (LET) 100 MeV-cm^2/mg
- Quality grades: ESA SCC, QML Q or V
- Package: 256 MQFPF; KGD

3. Product Organization

3.1 Block Diagram

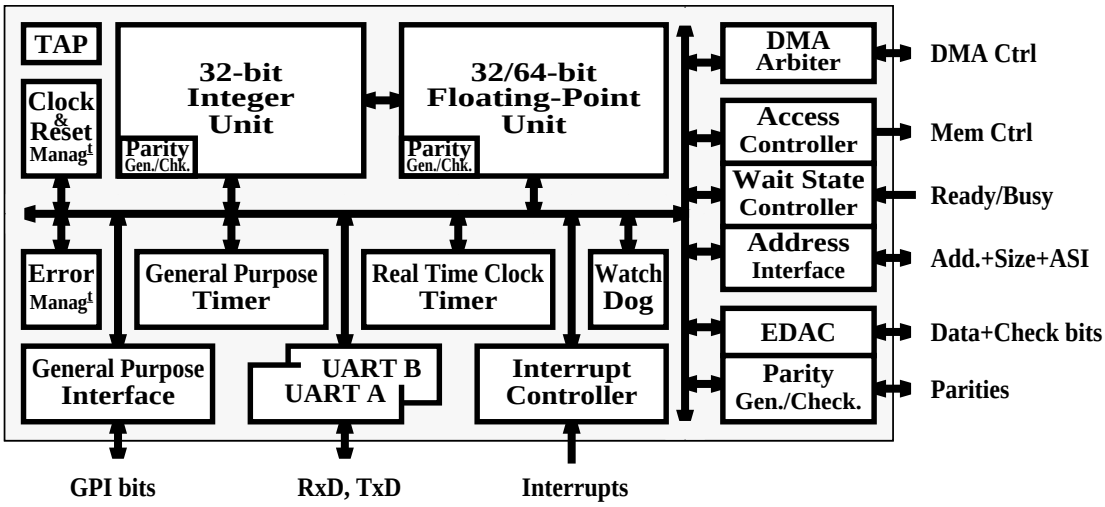


Figure 1. TSC695E Block Diagram

3.2 Signals Descriptions

Table 1. TSC695E External Signals Summary

Signal	Type	Active	Description	
RA[31:0]	I/O		32-bit registered address bus	Output buffer: 400pF
RAPAR	I/O	High	Registered address bus parity	Output buffer: 100pF
RASI[3:0]	I/O		4-bit registered address space identifier	
RSIZE[1:0]	I/O		2-bit registered bus transaction size	
RASPAR	I/O	High	Registered ASI and SIZE parity	
CPAR (IMPAR)	I/O	High	Control bus parity	
D[31:0]	I/O		32-bit data bus	Output buffer: 150pF
CB[6:0]	I/O		7-bit check-bit bus	
DPAR	I/O	High	Data bus parity	
RLDSTO	I/O	High	Registered atomic load-store	
$\overline{ALE}$	O	Low	Address latch enable	
DXFER	I/O	High	Data transfer	
LOCK	I/O	High	Bus lock	
RD	I/O	High	Read access	
$\overline{WE}$	I/O	Low	Write enable	
WRT	I/O	High	Advanced write	
$\overline{MHOLD}$	O	Low	Memory bus hold	MHOLD+FHOLD+BHOLD+FCCV
$\overline{MDS}$	O	Low	Memory data strobe	
$\overline{MEXC}$	O	Low	Memory exception	
$\overline{PROM8}$	I	Low	Select 8-bit wide PROM	
BA[1:0]	O		Latched address used for 8-bit wide boot PROM	
$\overline{ROMCS}$	O	Low	PROM chip select	
$\overline{ROMWRT}$	I	Low	ROM write enable	
$\overline{MEMCS[9:0]}$	O	Low	Memory chip select	
$\overline{MEMWR}$	O	Low	Memory write strobe	Output buffer: 400pF
$\overline{OE}$	O	Low	Memory output enable	
$\overline{BUFFEN}$	O	Low	Data buffer enable	
DDIR	O	High	Data buffer direction	

Table 1. TSC695E External Signals Summary

Signal	Type	Active	Description	
$\overline{\text{DDIR}}$	O	Low	Data buffer direction	
$\overline{\text{IOSEL}}$[3:0]	O	Low	I/O chip select	
$\overline{\text{IOWR}}$	O	Low	I/O and exchange memory write strobe	
$\overline{\text{EXMCS}}$	O	Low	Exchange memory chip select	
$\overline{\text{BUSRDY}}$	I	Low	Bus ready	
$\overline{\text{BUSERR}}$	I	Low	Bus error	
$\overline{\text{DMAREQ}}$	I	Low	DMA request	
$\overline{\text{DMAGNT}}$	O	Low	DMA grant	
DMAAS	I	High	DMA address strobe	
$\overline{\text{DRDY}}$	O	Low	Data ready during DMA access	
$\overline{\text{IUERR}}$	O	Low	IU error	
$\overline{\text{CPUHALT}}$	O	Low	Processor (IU & FPU) halt	
$\overline{\text{SYSERR}}$	O	Low	System error	
$\overline{\text{SYSHALT}}$	I	Low	System halt	
SYSAV	O	High	System availability	
$\overline{\text{NOPAR}}$	I	Low	No parity	
INULL	O	High	Integer unit nullify cycle	
INST	O	High	Instruction fetch	Used to check the execute stage of IU instruction pipeline
FLUSH	O	High	FPU instruction flush	
DIA	O	High	Delay instruction annulled	
RTC	O	High	Real Time Clock Counter output	
RxA/RxB	I		Receive data UART "A" and "B"	Input trigger
TxA/TxB	O		Transmit data UART "A" and "B"	
GPI[7:0]	I/O		GPI input/output	Input trigger
GPIINT	O	High	GPI interrupt	
EXTINT[4:0]	I		External interrupt	Input trigger
EXTINTACK	O	High	External interrupt acknowledge	
IWDE	I	High	Internal watch dog enable	
EWDINT	I	High	External watch dog input interrupt	Input trigger
WDCLK	I		Watch dog clock	
CLK2	I		Double frequency clock	
SYSCLK	O		System clock	Output buffer: 150 pF
$\overline{\text{RESET}}$	O	Low	Output reset	
$\overline{\text{SYSRESET}}$	I	Low	System input reset	Input trigger
TMODE[1:0]	I		Factory test mode	Functionnal mode = 00
DEBUG	I	High	Software debug mode	
TCK	I		Test (JTAG) clock	
$\overline{\text{TRST}}$	I	Low	Test (JTAG) reset	
TMS	I		Test (JTAG) mode select	
TDI	I		Test (JTAG) data input	
TDO	O		Test (JTAG) data output	
VCCI/VSSI			Main internal power	
VCCO/VSSO			Output driver power	

3.3 System Architecture

The TSC695E is to be used as an embedded processor requiring only memory and application specific peripherals to be added to form a complete on-board computer. All other system support functions are provided by the core.

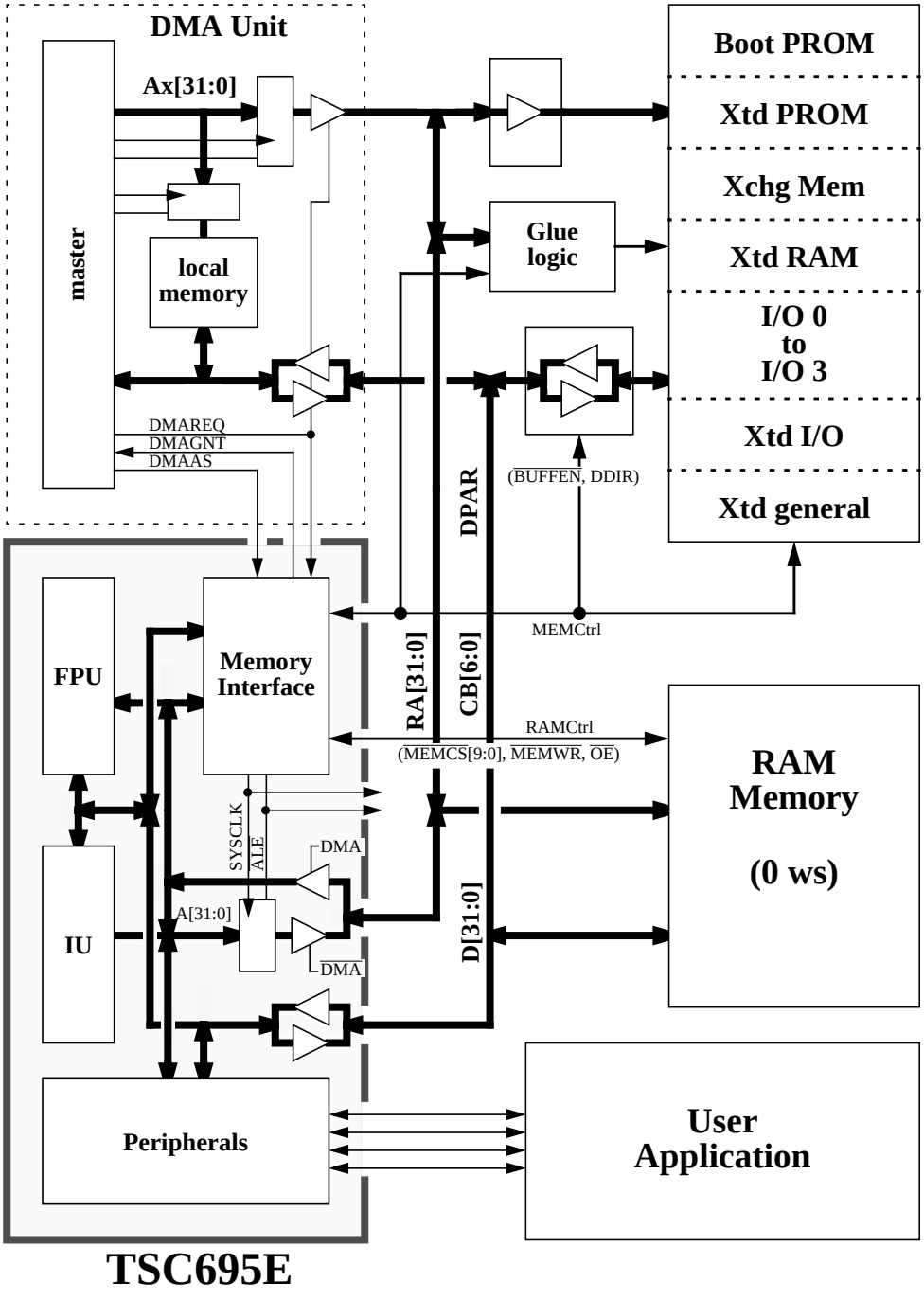


Figure 2. TSC695E System Architecture

4. Product Description

4.1 Integer Unit

The IU is designed for highly dependable space and military applications, and includes support for error detection. The RISC architecture makes possible the creation of a processor that can execute instructions at a rate approaching one instruction per processor clock.

To achieve that rate of execution, the IU employs a four-stage instruction pipeline that permits parallel execution of multiple instructions.

- **Fetch-** The processor outputs the instruction address to fetch the instruction.
- **Decode-** The instruction is placed in the instruction register and is decoded. The processor reads the operands from the register file and computes the next instruction address.
- **Execute-** The processor executes the instruction and saves the results in temporary registers. Pending traps are prioritized and internal traps are taken during this stage.
- **Write-** If no trap is taken, the processor writes the result to the destination register.

All four stages operate in parallel, working on up to four different instructions at a time. A basic "single-cycle" instruction enters the pipeline and completes in four cycles.

By the time it reaches the write stage, three more instructions have entered and are moving through the pipeline behind it. So, after the first four cycles, a single-cycle instruction exits the pipeline and a single-cycle instruction enters the pipeline on every cycle. Of course, a "single-cycle" instruction actually takes four cycles to complete, but they are called single cycle because with this type of instruction the processor can complete one instruction per cycle after the initial four-cycle delay.

4.2 Floating-Point Unit

The FPU is designed to provide execution of single and double-precision floating-point instructions concurrently with execution of integer instructions by the IU. The FPU is compliant to the ANSI/IEEE-754 (1985) floating-point standard.

The FPU is designed for highly dependable space and military applications, and includes support for concurrent error detection and testability.

The FPU uses a four stage instruction pipeline consisting of fetch, decode, execute and write stages (F, D, E and W). The fetch unit captures instructions and their addresses from the data and address busses. The decode unit contains logic to decode the floating-point instruction opcodes. The execution unit handles all instruction execution. The execution unit includes a floating-point queue (FP queue), which contains stored floating-point operate (FPop) instructions under execution and their addresses. The execution unit controls the load unit, the store unit, and the datapath unit. The FPU depends upon the IU to access all addresses and control signals for memory access. Floating-point loads and stores are executed in conjunction with the IU, which provides addresses and control signals while the FPU supplies or stores the data. Instruction fetch for integer and floating-point instructions is provided by the IU.

The FPU provides three types of registers: f registers, FSR, and the FP queue. The FSR is a 32-bit status and control register. It keeps track of rounding modes, floating-point trap types, queue status, condition codes, and various IEEE exception information. The floating-point queue contains the floating-point instruction currently under execution, along with its corresponding address.

4.3 Instruction Set

TSC695E instructions fall into six functional categories: load/store, arithmetic/logical/shift, control transfer, read/write control register, floating-point-operate-operate, and miscellaneous.

❑ Note: The execution of IFLUSH will cause an illegal instruction trap.

4.4 On-Chip Peripherals

4.4.1 Memory Interface

4.4.1.1 Memory Mapping

The TSC695E is design to allow an easy interfacing to internal/external memory resources.

Table 2. Memory Mapping

Memory contents	Start Address	Size (bytes)	Data size and parity options	
Boot PROM	0x0000 0000	128K → 16M	8-bit mode	-No parity / -Only byte write
			40-bit mode	-Parity + EDAC mandatory / -Only word write
Extended PROM	0x0100 0000	Max: 15M	8-bit mode	-No parity / -Only byte write
			40-bit mode	-Parity + EDAC mandatory / -Only word write
Exchange Memory	0x01F0 0000	4k → 512k	-Parity + EDAC option / -Only word write	
System Registers	0x01F8 0000	512K (124 used)	-Parity / -Only word read/write access	
RAM (8 blocks)	0x0200 0000	8*32K → 8*4M	-Parity + EDAC option / -All data sizes allowed	
Extended RAM	0x0400 0000	Max: 192M		
I/O Area 0	0x1000 0000	0 → 16M	-Parity option / -All data sizes allowed	
I/O Area 1	0x1100 0000	0 → 16M		
I/O Area 2	0x1200 0000	0 → 16M		
I/O Area 3	0x1300 0000	0 → 16M		
Extended I/O Area	0x1400 0000	Max: 1728M		
Extended General	0x8000 0000	Max: 2G	-No parity / -All data sizes allowed	

4.4.1.2 System Registers

The system registers are only writeable by IU in the supervisor mode or by DMA during $\overline{\text{CPUHALT}}$. Byte or halfword access is not allowed in any mode and will generate Memory Exception.

Table 3. System Registers Address Map

System Register Name		Address
System Control Register	SYSCTR	0x 01F8 0000
Software Reset	SWRST	0x 01F8 0004
Power Down	PDOWN	0x 01F8 0008
System Fault Status Register	SYSFSR	0x 01F8 00A0
Failing Address Register	FAILAR	0x 01F8 00A4
Error & Reset Status Register	ERRRSR	0x 01F8 00B0
Test Control Register	TESCTR	0x 01F8 00D0
Memory Configuration Register	MCNFR	0x 01F8 0010
I/O Configuration Register	IOCNFR	0x 01F8 0014
Waitstate Configuration Register	WSCNFR	0x 01F8 0018
Access Protection Segment 1 Base Register	APS1BR	0x 01F8 0020
Access Protection Segment 1 End Register	APS1ER	0x 01F8 0024
Access Protection Segment 2 Base Register	APS2BR	0x 01F8 0028
Access Protection Segment 2 End Register	APS2ER	0x 01F8 002C
Interrupt Shape Register	INTSHR	0x 01F8 0044
Interrupt Pending Register	INTPDR	0x 01F8 0048
Interrupt Mask Register	INTMKR	0x 01F8 004C
Interrupt Clear Register	INTCLR	0x 01F8 0050
Interrupt Force Register	INTFCR	0x 01F8 0054
Watchdog Timer Register	WDOGTR	0x 01F8 0060
Watchdog Timer Trap Door Set	WDOGST	0x 01F8 0064
Real Time Clock Timer <Counter> Register	RTCCR	0x 01F8 0080

Table 3. System Registers Address Map

System Register Name		Address
Real Time Clock Timer <Scaler> Register	RTCSR	0x 01F8 0084
General Purpose Timer <Counter> Register	GPTCR	0x 01F8 0088
General Purpose Timer <Scaler> Register	GPTSR	0x 01F8 008C
Timers Control Register	TIMCTR	0x 01F8 0098
General Purpose Interface Configuration Register	GPICNFR	0x 01F8 00A8
General Purpose Interface Data Register	GPIDATR	0x 01F8 00AC
UART "A" Rx & Tx Register	UARTAR	0x 01F8 00E0
UART "B" Rx & Tx Register	UARTBR	0x 01F8 00E4
UART Status Register	UARTSR	0x 01F8 00E8

4.4.1.3 Wait-State and Time-out Generator

It is possible to control the wait state generation by programming a Waitstate Configuration Register. The maximum programmable number of wait-states is applied by default at reset.

It is possible to program the number of wait states for the following combinations:

- RAM read and write
- PROM read and write (i.e. EEPROM or FLASH write)
- Exchange Memory read/write
- Four individual I/O peripherals read/write

A bus time-out function of 256 or 1024 system clock cycles is provided for the bus ready controlled memory areas, 256 system clock cycles in the Extended RAM, Extended General and Extended I/O areas and 1024 system clock cycles in the Extended PROM area.

4.4.1.4 EDAC

The TSC695E includes a 32-bit EDAC (Error Detection And Correction). Seven bits (CB[6:0]) are used as check bits over the data bus. The Data Bus Parity signal (DPAR) is used to check and generate the odd parity over the 32-bit data bus. This means that altogether 40 bits are used when the EDAC is enabled. The EDAC corrects any single bit data error on the 40-bit bus.

4.4.1.5 Memory and I/O Parity

The TSC695E handles parity towards memory and I/O in a special way. The processor can be programmed to use no parity, only parity or parity and EDAC protection towards memory and to use parity or no towards I/O. The signal used for the parity bit is DPAR.

4.4.1.6 Memory Redundancy

Programming the Memory Configuration Register, the TSC695E provides chip selects for two redundant memory banks for replacement of faulty banks.

4.4.1.7 Memory Access Protection

- **Unimplemented Areas -** Accesses to all unimplemented memory areas are handled by the TSC695E and detected as illegal.
- **RAM Write Access Protection -** The TSC695E can be programmed to detect and mask write accesses in any part of the RAM. The protection scheme is enabled only for data area, not for the instruction area. The programmable write access protection is based on two segments.
- **Boot PROM Write Protection -** The TSC695E supports a qualified PROM write for an 8-bit wide PROM and/or for a 40-bit wide PROM.

4.4.2 DMA

4.4.2.1 DMA Interface

The TSC695E supports Direct Memory Access (DMA). The DMA unit requests access to the processor bus by asserting the DMA request signal ($\overline{\text{DMAREQ}}$). When the DMA unit receives the $\overline{\text{DMAGNT}}$ signal in response, the processor bus is granted. In case the processor is in the power down mode the processor is permanent tri-stated, and a $\overline{\text{DMAREQ}}$ will directly give a $\overline{\text{DMAGNT}}$. The TSC695E includes a DMA session time-out function.

4.4.2.2 Bus Arbiter

The TSC695E always has the lowest priority on the system bus.

4.4.3 Traps

A trap is a vectored transfer of control to the supervisor through a special trap table that contains the first four instructions of each trap handler. The base address of the table is established by supervisor and the displacement, within the table, is determined by the trap type. Two categories of traps can appear.

4.4.3.1 Synchronous Traps

Table 4. Synchronous Traps

Trap		Priority		Trap Type (tt)	Comments
Reset		1		-	Sources: - SYSRESET* pin - software reset - watch dog reset - IU, FPU or System error reset
Hardware Error	Non-restartable, imprecise error	2	2.1	64h	Severe error requiring a re-boot TSC695E enters (if not masked) in halt or reset mode.
	Non-restartable, precise error		2.2	62h	Error not removable, PC & nPC OK TSC695E enters (if not masked) in halt or reset mode.
	Register file error		2.3	65h	Special case of non -restartable, precise error. TSC695E enters (if not masked) in halt or reset mode.
	Restartable, late error		2.4	63h	Retrying instruction but PC & nPC have to be re-adjusted TSC695E enters (if not masked) in halt or reset mode.
	Restartable, precise error		2.5	61h	Retrying instruction TSC695E enters (if not masked) in halt or reset mode.
Instruction access (*Error on instruction fetch*)		3		01h	- Parity error on control bus - Parity error on data bus - Parity error on address bus - Access to protected or unimplemented area - Uncorrectable error in memory - Bus time out - Bus error
Illegal Instruction		4		02h	
Privileged instruction		5		03h	
FPU disabled		6		04h	
Window	Overflow	7		05h	During SAVE instruction or trap taken
	Underflow			06h	During RESTORE instruction or RETT instruction
Memory address not aligned		8		07h	

Trap		Priority		Trap Type (tt)	Comments
FPU exception	Non-restartable error	9	9.1	08h	Severe error, cannot restarting the instruction. TSC695E enters (if not masked) in halt or reset mode.
	Data bus error		9.2		Parity error on FPU data bus. TSC695E enters (if not masked) in halt or reset mode.
	Restartable error		9.3		Can be removed restarting the instruction. TSC695E enters (if not masked) in halt or reset mode.
	Sequence error		9.4		
	Unimplemented FPop		9.5		
	IEEE exceptions:		9.6		- Invalid operation - Division by zero - Overflow - Underflow - Inexact
Data access exception (*Error on data load*)		10		09h	- Idem “instruction access” - System register access violation
Tag overflow		11		0Ah	TADDccTV and TSUBccTV instructions
Trap instructions		12		80h to FFh	Trap on integer condition codes (Ticc)

4.4.3.2 Interrupts or Asynchronous Traps

Table 5. Interrupts or Asynchronous Traps

Trap		Priority	Trap Type (tt)	Comments
Watch dog time-out		13	1Fh	Internal or external (EWDINT pin)
External INT 4		14	1Eh	EXTINTAK on only one of EXTINT[4:0]
Real time clock timer		15	1Dh	
General purpose timer		16	1Ch	
External INT 3		17	1Bh	EXTINTAK on only one of EXTINT[4:0]
External INT 2		18	1Ah	EXTINTAK on only one of EXTINT[4:0]
DMA time-out		19	19h	
DMA access error		20	18h	
UART Error		21	17h	
Correctable error in memory		22	16h	Data read OK but source not updated
UART B	- Data ready - Transmitter ready	23	15h	
UART A	- Data ready - Transmitter ready	24	14h	
External INT 1		25	13h	EXTINTAK on only one of EXTINT[4:0]
External INT 0		26	12h	EXTINTAK on only one of EXTINT[4:0]
Masked hardware errors		27	11h	Logical OR of: - IU hardware error masked - FPU hardware error masked - System hardware error masked

It is possible to mask each individual interrupt (except interrupt 15). The interrupts in the Interrupt Pending Register are cleared automatically when the interrupt is acknowledged.
By programming the Interrupt Shape Register, it is possible to define the external interrupts to be either active low or active high and to define the external interrupts to be either edge or level sensitive.

4.4.4 Timers

In software debug mode the timers are controlled by a system register bit and the external pin DEBUG.

4.4.4.1 General Purpose Timer

The General Purpose Timer (GPT) provides, in addition to a generalized counter function, a mechanism for setting the step size in which actual time counts are performed.
GPT is clocked by the internal system clock. They are possible to program to be either of single-shot type or periodical type and in both cases generate an interrupt when the delay time has elapsed. The current value of the scaler and counter of the GPT can be read.

4.4.4.2 Real Time Clock Timer

The only functional differences between the two timers are that the Real Time Clock Timer (RTCT) has an 8-bit scaler (16-bit scaler for GPT) and that the RTCT interrupt has higher priority than the GPT interrupt.
RTCT information is available on RTCT output pin.

4.4.4.3 Watchdog Timer

Setting the external pin IWDE to Vcc enables the internal watchdog timer. Otherwise the watchdog function must be externally provided.
The watchdog is supplied from a separate external input (WDCLK). After reset, the timer is enabled and starts running with the maximum range. If the timer is not refreshed (reprogrammed) before the counter reaches zero value, an interrupt is sent. Simultaneously, the timer starts counting a reset time-out period. If the timer is not acknowledged before the reset time-out period elapses, a reset is applied to TSC695E.

4.4.5 UART's

Two full duplex asynchronous receiver transmitters (UART) are included. In software debug mode the UART's are controlled by system register bits.
The data format of the UART's is eight bits. It is possible to choose between even or odd parity, or no parity, and between one and two stop bits. The UART's provide double buffering, i.e. each UART consists of a transmitter holding register, a receiver holding register, a transmitter shift register, and a receiver shift register. Each of these registers are 8-bit wide. For each UART a RX and TX Register is provided. The UART's generate an interrupt each time a byte has been received or a byte has been sent. There is another interrupt to indicate errors.
The baud rate of both the UART's is programmable. The clock is derived either from the system clock or can use the watchdog clock.

4.4.6 General Purpose Interface

The General Purpose Interface (GPI) is an 8-bit parallel I/O port. Each pin can be configured as an input or an output. A falling or rising edge detection is made on each selected GPI inputs. Every input transition on GPI generates an external positive pulse on GPIINT pin of two SYSCLK width.

4.4.7 Execution Modes

4.4.7.1 Reset Mode

Reset mode is entered when:

- The $\overline{\text{SYSRES}}$ input is asserted,
- Software reset which is caused by the software writing to a Software Reset Register,
- Watchdog reset which is caused by a Watchdog counter time-out,
- Error reset which is caused by a hardware parity error, EDAC uncorrectable error.

This $\overline{\text{RESET}}$ output have a minimum of 1024 SYSCLK width to allow the usage of flash memories.
Error and Reset Status Register contains the source of the last processor reset.

4.4.7.2 Run Mode

In this mode the IU/FPU is executing, all peripherals are running (if software enabled).

4.4.7.3 System Halt Mode

System Halt mode is entered when the $\overline{\text{SYSHALT}}$ input is asserted. In this mode, the IU and FPU are frozen, the timers and UART's are stopped.

4.4.7.4 Power Down Mode

This mode is entered by writing to the Power Down Register. In this mode, the IU and FPU are frozen. The TSC695E leaves the power-down mode if an external interrupt is asserted.

4.4.7.5 Error Halt Mode

Error Halt mode is entered under the following circumstances:

- A hardware parity error or an EDAC uncorrectable error has occurred.
- The IU enters error mode.

The only way to exit Error Halt Mode is through Cold Reset by asserting $\overline{\text{SYSRES}}$.

4.4.8 Error Handler

The TSC695E has one error output signal ($\overline{\text{SYSERR}}$) which indicates that an unmasked error has occurred. Any error signalled on the error inputs from the IU and the FPU is latched and reflected in the Error and Reset Status Register. As default, an error leads to a processor halt.

4.4.9 Parity Checking

The TSC695E includes:

- Parity checking and generation (if required) on the external data bus,
- Parity checking on the external address bus,
- Parity checking on ASI and SIZE,
- Parity checking and generation on all system registers,
- Parity generation and checking on the internal control bus to the IU,

All external parity checking can be disabled using the $\overline{\text{NOPAR}}$ signal.

4.4.10 System Clock

The TSC695E uses CLK2 clock input directly and creates a system clock signal by dividing CLK2 by two. It drives SYSCLK pin with a nominal 50% duty cycle for the application. It is highly recommended that only SYSCLK rising edge is used as reference as far as possible.

4.4.11 System Availability

The SYSAV bit in the Error and Reset Status Register can be used by software to indicate system availability.

4.4.12 Test Mode

The TSC695E includes a number of software test facilities such as EDAC test, Parity test, Interrupt test, Error test and a simple Test Access Port. These test functions are controlled using the Test Control Register.

5. Test and Diagnostic Hardware Functions

A variety of TSC695E test and diagnostic hardware functions, including boundary scan, internal scan, clock control and On-Chip Debugger, are controlled through an IEEE 1149.1 (JTAG) standard Test Access Port (TAP).

5.1 Test Access Port

The TAP interfaces to the JTAG bus via 5 dedicated pins on the TSC695E chip. These pins are:

- TCK (input): Test Clock,
- TMS (input): Test Mode Select,
- TDI (input): Test Data Input,
- TDO (output): Test Data Output,
- $\overline{\text{TRST}}$ (input): Test Reset

5.2 The Instruction Register

Eleven instructions are supported by the TSC695E TAP.

Table 6. JTAG Instructions

Binary Value	Name of Instruction	Data Register	Scan Chain Accessed
01 . 1000	CCTEST	Checkers Scan Register	IU parity checkers scan chain
01 . 1100	IUTEST	IU Scan Register	UI registers scan chain
01 . 1101	FPUTEST	FPU Scan Register	FPU registers scan chain
01 . 1110	SYSTEST	System Scan Register	System registers scan chain
01 . 1010	OCDTEST	OCD Scan Register	OCD registers scan chain
01 . 1001	CTSTEST	OCD Ctrl/Stat Register	OCD control/status scan chain
00 . 0000	EXTEST	Boundary Scan Register	Boundary scan chain
00 . 0001	SAMPLE/PRELOAD	Boundary Scan Register	Boundary scan chain
00 . 0011	INTEST	Boundary Scan Register	Boundary scan chain
11 . 1111	BYPASS	Bypass Register	Bypass register
10 . 0000	IDCODE	Device ID Register	ID register scan chain

5.3 Test Data Registers

Nine data registers are supported in the TSC695E TAP:

- Bypass register,
- ID. register (value: 0x 0b64 40b1),
- Boundary Scan register (input, output and in/out pins excepted TAP interface),
- Checkers scan register (only used for factory test),
- IU Scan register (%psr, %tbr, %wim, %y, windowed registers *(# 128)*, %g0 up to %g7, %fpc, %dpc, %epc, %wpc),
- FPU Scan register (%fsr, %fqr, %f0 up to %f31),
- System Scan register,
- OCD Scan register (4 breakpoints for program execution, 1 breakpoint for data memory, 1 cycle counter, step-by step),
- OCD control & status register (reset request & status, halt request & status, run).

6. Electrical ans Mechanical Specification

6.1 Maximum Rating and DC Characteristics

6.1.1 Maximum Ratings

- Storage Temperature. . . . . -65 ˚C to +150 ˚C
- Ambiante Temperature with Power Applied . . . . . -55 ˚C to +125 ˚C
- Supply Voltqge. . . . . -0.5 V to +7.0 V
- Input Voltqge . . . . . -0.5 V to +7.0 V

6.1.2 Operating Range

Range	Ambient Temperature	Vcc
Military	-55 ˚C to +125 ˚C	+5 V ± 10%
		+3 V ± 10%

6.1.3 DC Characteristics *Over the Operating Range*

Symbol		Parameter	min	Typ	MAX	Unit	Test Conditions
$VIL_{trigger}$		Input Low Voltage for trigger input			0.8	V	Vcc = 4.5 to 5.5 V
					0.6		Vcc = 2.7 to 3.3 V
$VIH_{trigger}$		Input High Voltage for trigger input	3.0			V	Vcc = 4.5 to 5.5 V
			2.2				Vcc = 2.7 to 3.3 V
ΔVT		Input Hysteresis for trigger input		0.9		V	Vcc = 4.5 to 5.5 V
				0.4			Vcc = 2.7 to 3.3 V
VIL_{TTL}		Input Low Voltage for TTL input			0.8	V	Vcc = 4.5 to 5.5 V
							Vcc = 2.7 to 3.3 V
VIH_{TTL}		Input High Voltage for TTL input	2.2			V	Vcc = 4.5 to 5.5 V
							Vcc = 2.7 to 3.3 V
$VOL_{3/3}$	**5 V**	Output Low Voltage for 400pf buffer		0.3	0.4	V	IOL = 12 mA
	3V						IOL = 9 mA
$VOH_{3/3}$	**5 V**	Output High Voltage for 400pf buffer	2.4	4.3		V	IOH = - 48 mA
	3V			3.0			IOH = - 6 mA
$VOL_{1/3}$	**5 V**	Output Low Voltage for 150pf buffer		0.3	0.4	V	IOL = 4 mA
	3V						IOL = 3 mA
$VOH_{1/3}$	**5 V**	Output High Voltage for 150pf buffer	2.4	4.3		V	IOH = - 16 mA
	3V			3.0			IOH = - 2 mA
Icc_{OP}		Operating Supply Current for core and input buffers	**(to be defined)**				Vcc = 5 V, f = 35 MHz
							Vcc = 3 V, f = 20 MHz
Icc_{PD}		Power Down Supply Current for core and input buffers					Vcc = 5 V, f = 35 MHz
							Vcc = 3 V, f = 20 MHz

6.1.4 Capacitance Ratings

Parameter	Description	MAX
C_{IN}	Input Capacitance	7 pF
C_{OUT}	Output Capacitance	8 pF
C_{IO}	Input/Output Capacitance	8 pF

6.2 AC Characteristics

6.2.1 AC Characteristics (SYSCLK Freq. = 30MHz - 5V)

Param	Min	Max	Comment	Reference edge
t1	17		CLK2 period	
t2	34		SYSCLK period	
t3	7.65	9.35	CLK2 high and low pulse width	
t4		4.5	RA(31:0) RAPAR RSIZE output delay	SYSCLK+
t5		7.5	MEMCS*(9:0) ROMCS* EXMCS* output delay	SYSCLK+
t6		20	DDIR DDIR* output delay	SYSCLK+
t7		18	MEMWR* output delay	SYSCLK-
t8		15.5	OE* HL output delay	SYSCLK+
t9	10		Data setup time during load	SYSCLK+
t10	2		Data hold time during load	SYSCLK+
t11		15	Data output delay	MEMWR*-
t12	4		Data output valid	MEMWR*+
t13		16	CB output delay	SYSCLK+
t14		15	ALE* output delay	SYSCLK-
t15		15.5	BUFFEN* HL output delay	SYSCLK+
t17		15	MDS* DRDY* output delay	SYSCLK+
t19		15.5	Data and DPAR valid to high-Z delay	SYSCLK+
t20		15	MEXC* output delay	SYSCLK-
t21	10		RASI(3:0) RSIZE(1:0) RASPAR setup time	SYSCLK+
t22	2		RASI(3:0) RSIZE(1:0) RASPAR hold time	SYSCLK+
t23		15	BOOT PROM address output delay	SYSCLK+
t24	13		BUSRDY* setup time	SYSCLK+
t25	0		BUSRDY* hold time	SYSCLK+
t27		15	IOSEL output delay	SYSCLK+ HL / SYSCLK- LH
t28	12		DMAAS setup time	SYSCLK+
t29	0		DMAAS hold time	SYSCLK-
t30	10		DMAREQ* setup time	SYSCLK+
t31		15	DMAGNT* output delay	SYSCLK+
t32	10		RA(31:0) RAPAR CPAR setup time	SYSCLK+
t33	4		RA(31:0) RAPAR CPAR hold time	SYSCLK+
t36	100		TCK period	
t37	10		TMS setup time	TCK+
t38	4		TMS hold time	TCK+
t39	10		TDI setup time	TCK+
t40	10		TDI hold time	TCK+
t41		20	TDO output delay	TCK-
t46		15	INULL output delay	SYSCLK+
t48		20	RESET* CPUHALT* output delay	SYSCLK+
t49		15	SYSERR* SYSAV output delay	SYSCLK+

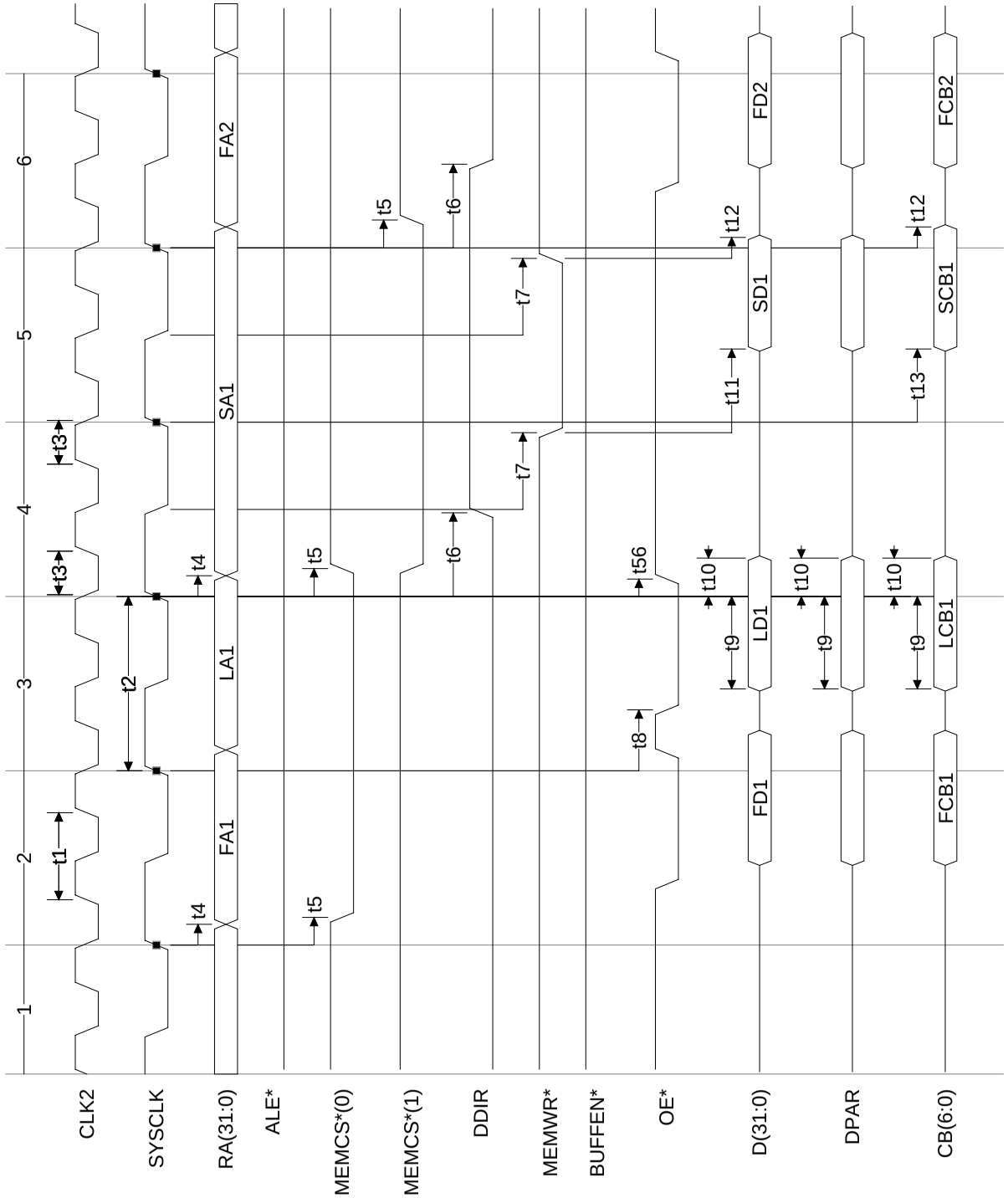
Param	Min	Max	Comment	Reference edge
t50		15	IUERR* output delay	SYSCLK+
t52	12		EXTINT(4:0) setup time	SYSCLK-
t53	0		EXTINT(4:0) hold time	SYSCLK+
t54		15	EXTINTACK output delay	SYSCLK+
t56		7	OE* LH output delay	SYSCLK+
t57		5	BUFFEN* LH output delay	SYSCLK+

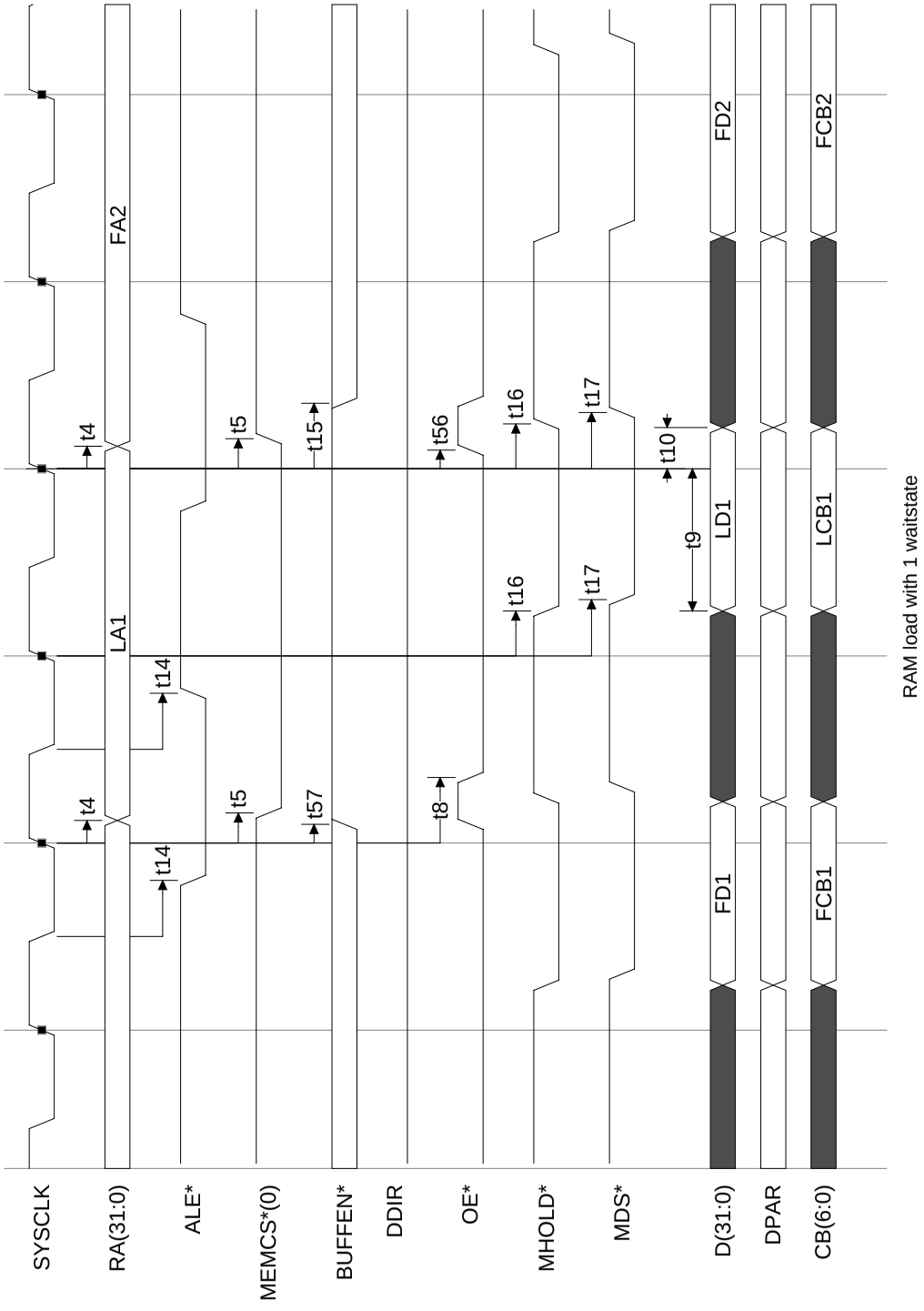
6.2.2 AC Characteristics (SYSCLK Freq. = 20MHz - 5V)

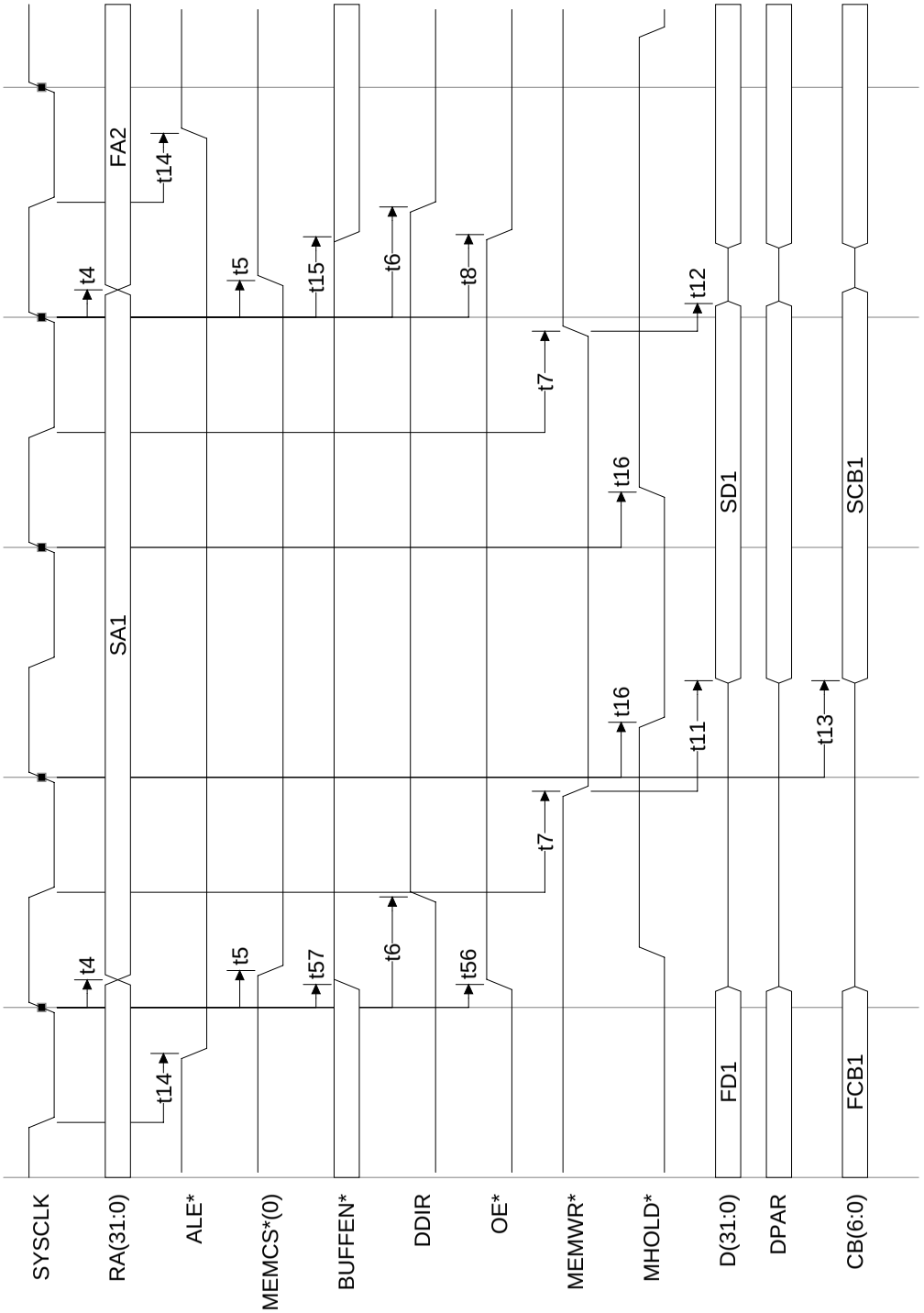
Param	Min	Max	Comment	Reference edge
t1	25		CLK2 period	
t2	50		SYSCLK period	
t3	11.25	13.75	CLK2 high and low pulse width	
t4		6.5	RA(31:0) RAPAR RSIZE output delay	SYSCLK+
t5		8.5	MEMCS*(9:0) ROMCS* EXMCS* output delay	SYSCLK+
t6		24	DDIR DDIR* output delay	SYSCLK+
t7		22	MEMWR* output delay	SYSCLK-
t8		17.5	OE* HL output delay	SYSCLK+
t9	15		Data setup time during load	SYSCLK+
t10	3		Data hold time during load	SYSCLK+
t11		23	Data output delay	MEMWR*-
t12	6		Data output valid	MEMWR*+
t13		20	CB output delay	SYSCLK+
t14		15	ALE* output delay	SYSCLK-
t15		17.5	BUFFEN* HL output delay	SYSCLK+
t17		15	MDS* DRDY* output delay	SYSCLK+
t19		17.5	Data and DPAR valid to high-Z delay	SYSCLK+
t20		15	MEXC* output delay	SYSCLK-
t21	12		RASI(3:0) RSIZE(1:0) RASPAR setup time	SYSCLK+
t22	3		RASI(3:0) RSIZE(1:0) RASPAR hold time	SYSCLK+
t23		15	BOOT PROM address output delay	SYSCLK+
t24	13		BUSRDY* setup time	SYSCLK+
t25	0		BUSRDY* hold time	SYSCLK+
t27		18	IOSEL output delay	SYSCLK+ HL / SYSCLK- LH
t28	12		DMAAS setup time	SYSCLK+
t29	0		DMAAS hold time	SYSCLK-
t30	10		DMAREQ* setup time	SYSCLK+
t31		15	DMAGNT* output delay	SYSCLK+
t32	10		RA(31:0) RAPAR CPAR setup time	SYSCLK+
t33	4		RA(31:0) RAPAR CPAR hold time	SYSCLK+
t36	100		TCK period	
t37	10		TMS setup time	TCK+
t38	4		TMS hold time	TCK+
t39	10		TDI setup time	TCK+
t40	10		TDI hold time	TCK+
t41		20	TDO output delay	TCK-
t46		15	INULL output delay	SYSCLK+
t48		20	RESET* CPUHALT* output delay	SYSCLK+
t49		15	SYSERR* SYSAV output delay	SYSCLK+
t50		15	IUERR* output delay	SYSCLK+

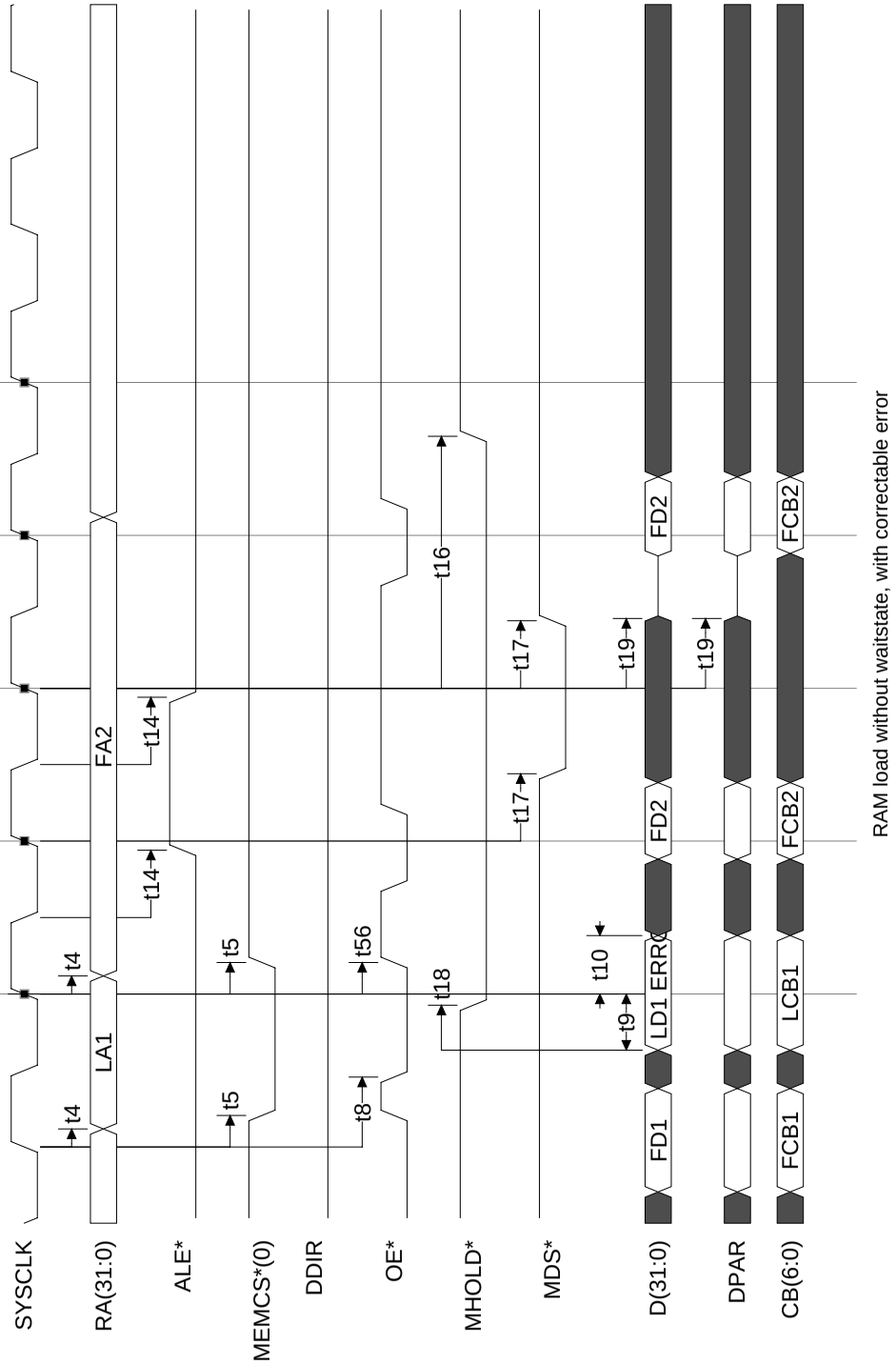
Param	Min	Max	Comment	Reference edge
t52	12		EXTINT(4:0) setup time	SYSCLK-
t53	0		EXTINT(4:0) hold time	SYSCLK+
t54		15	EXTINTACK output delay	SYSCLK+
t56		5	OE* LH output delay	SYSCLK+
t57		5	BUFFEN* LH output delay	SYSCLK+

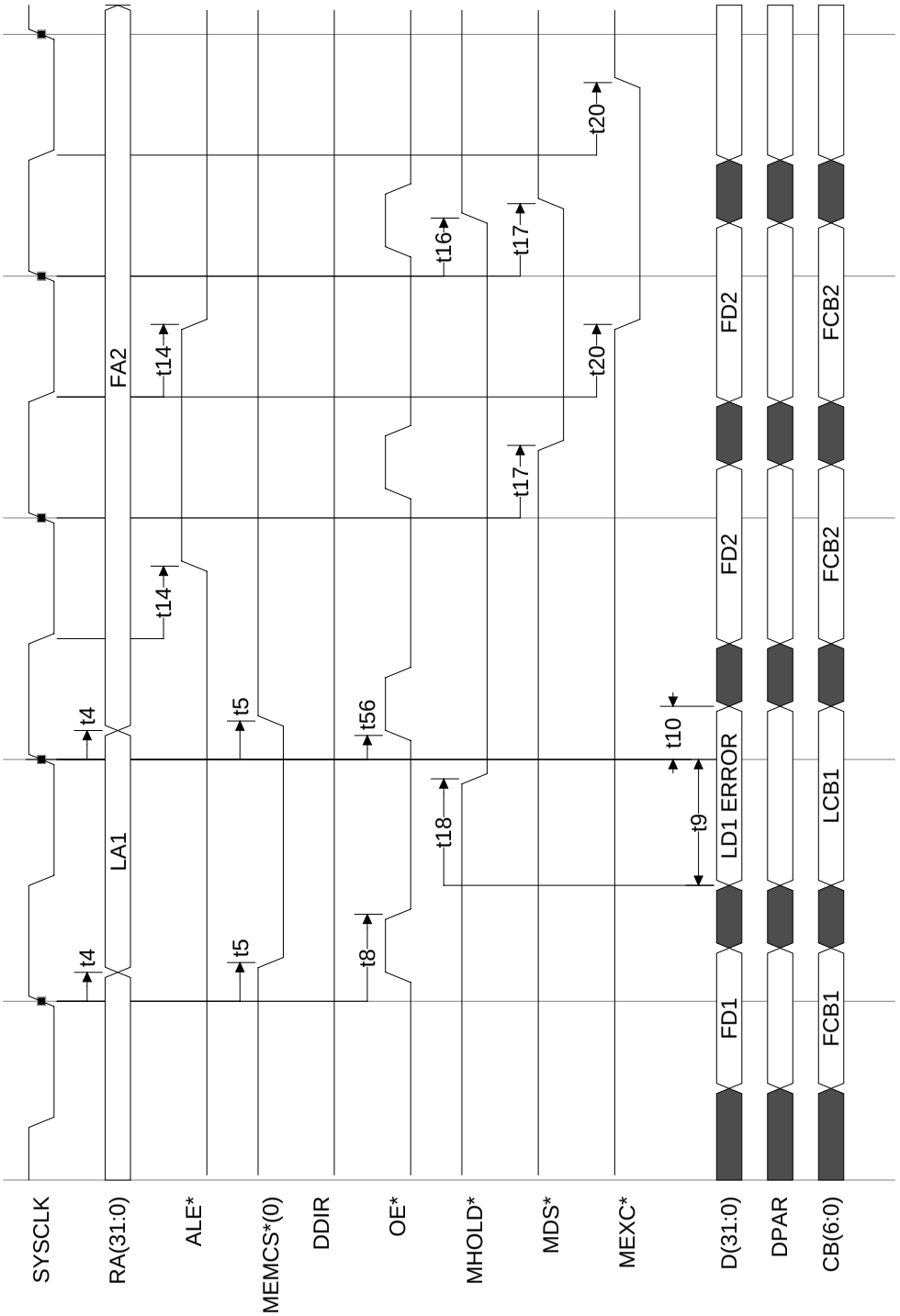
6.2.3 Timing Diagrams

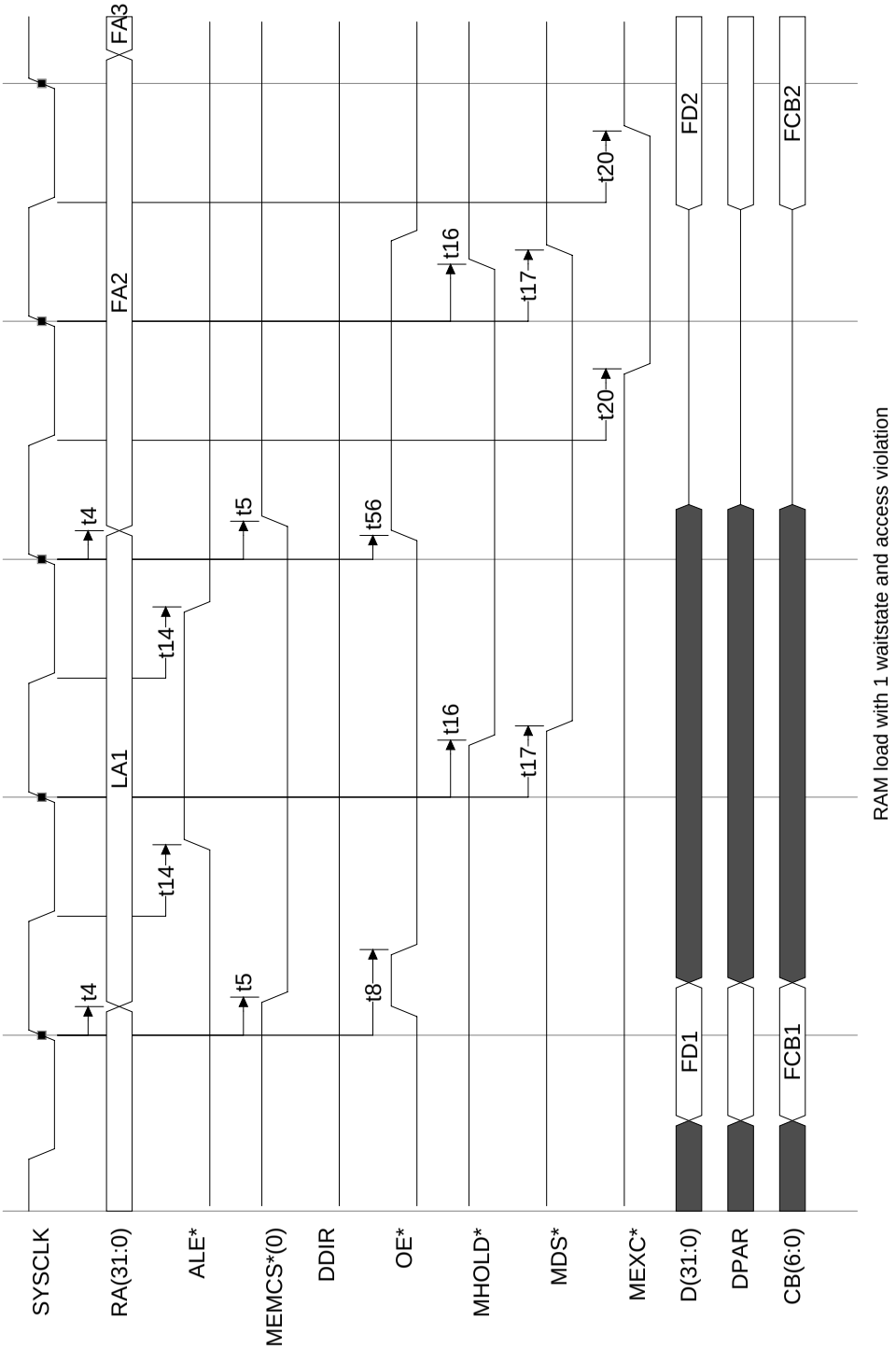


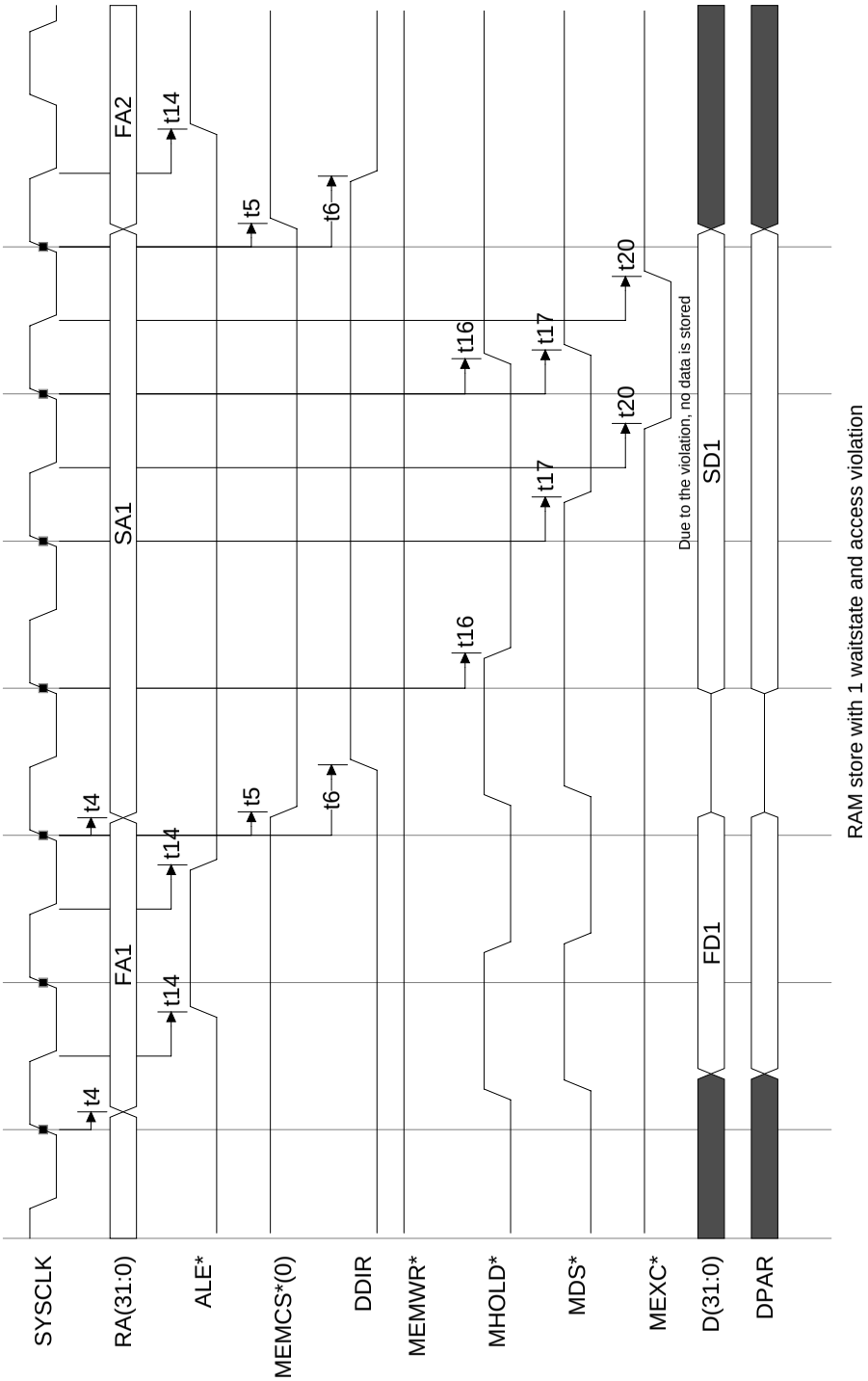

SYSCLK
RA(31:0)
ALE*
MEMCS*(0)
BUFFEN*
DDIR
OE*
MHOLD*
MDS*
D(31:0)
DPAR
CB(6:0)
FA2
LA1
FD1
FD2
LD1
FCB1
FCB2
LCB1
t4
t5
t14
t15
t56
t16
t17
t10
t9
t57
t8
RAM load with 1 waitstate

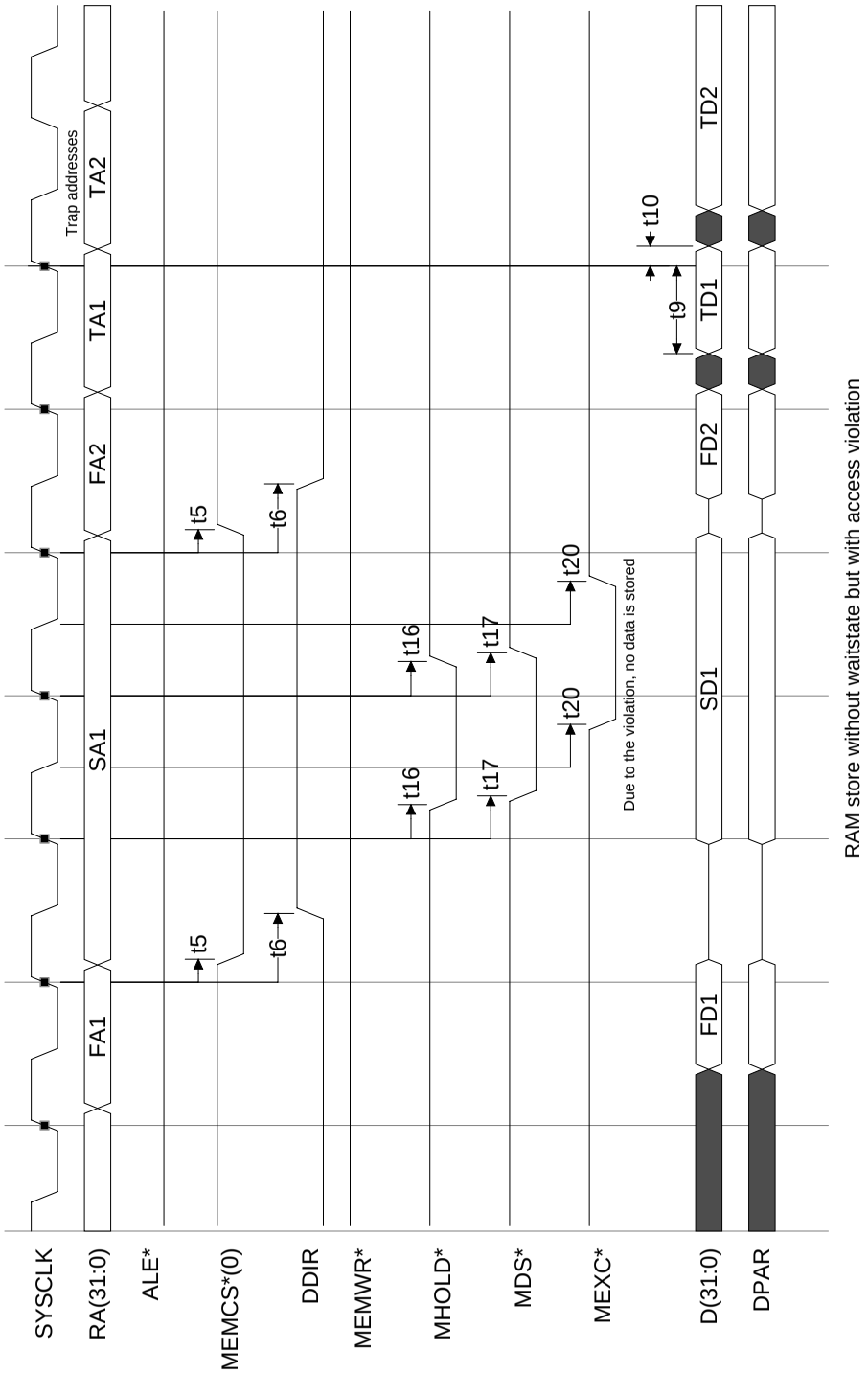

SYSCLK
RA(31:0)
ALE*
MEMCS*(0)
BUFFEN*
DDIR
OE*
MEMWR*
MHOLD*
D(31:0)
DPAR
CB(6:0)
SA1
FA2
SD1
SCB1
FD1
FCB1
t4
t5
t6
t7
t8
t11
t12
t13
t14
t15
t16
t57
t56
RAM store with 1 waitstate

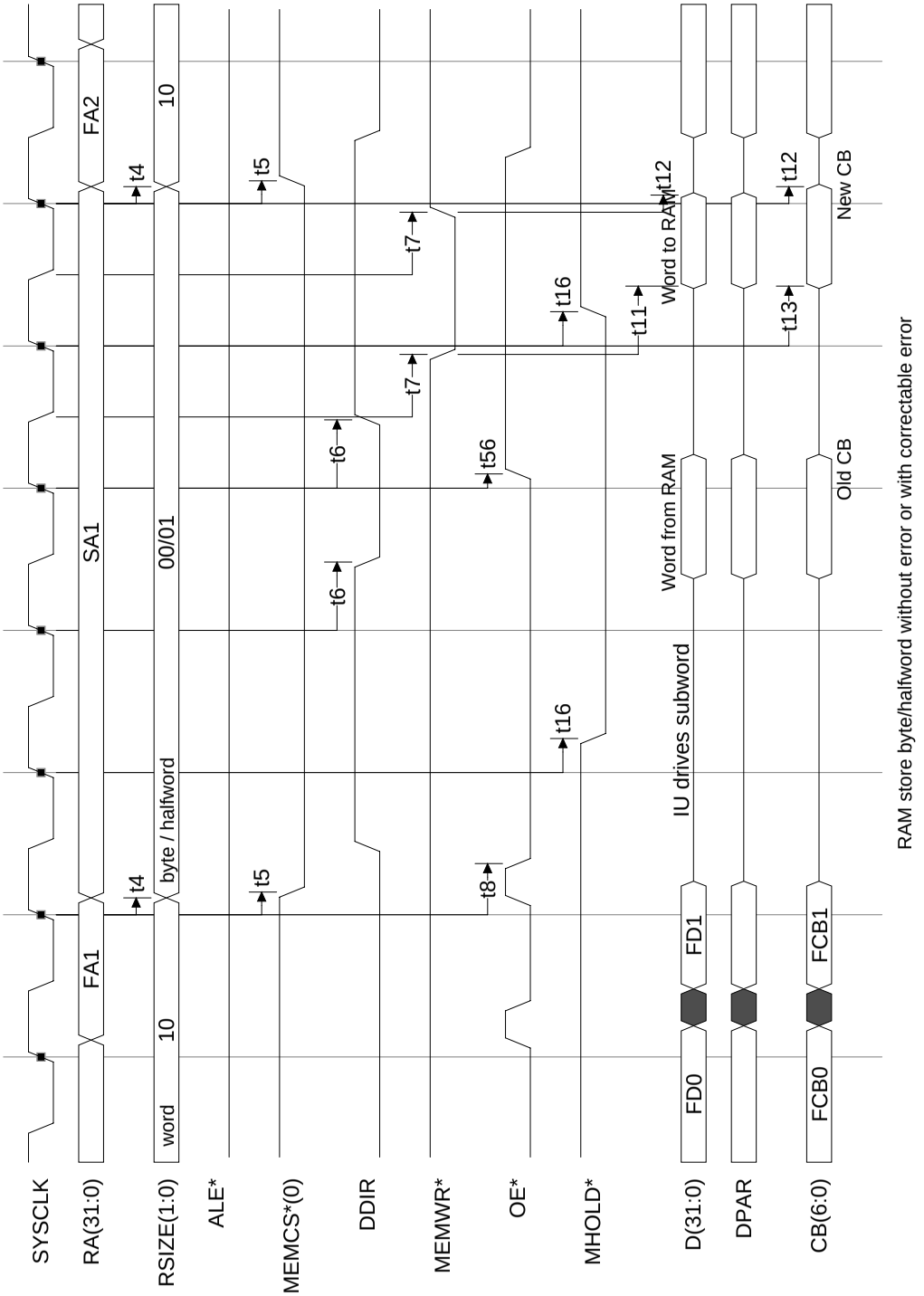

SYSCLK
RA(31:0)
ALE*
MEMCS*(0)
DDIR
OE*
MHOLD*
MDS*
D(31:0)
DPAR
CB(6:0)
t4
t4
t5
t5
t8
t14
t14
t56
t16
t18
t17
t17
t10
t9
t19
t19
LA1
FA2
FD1
LD1 ERR
FD2
FD2
FCB1
LCB1
FCB2
FCB2
RAM load without waitstate, with correctable error

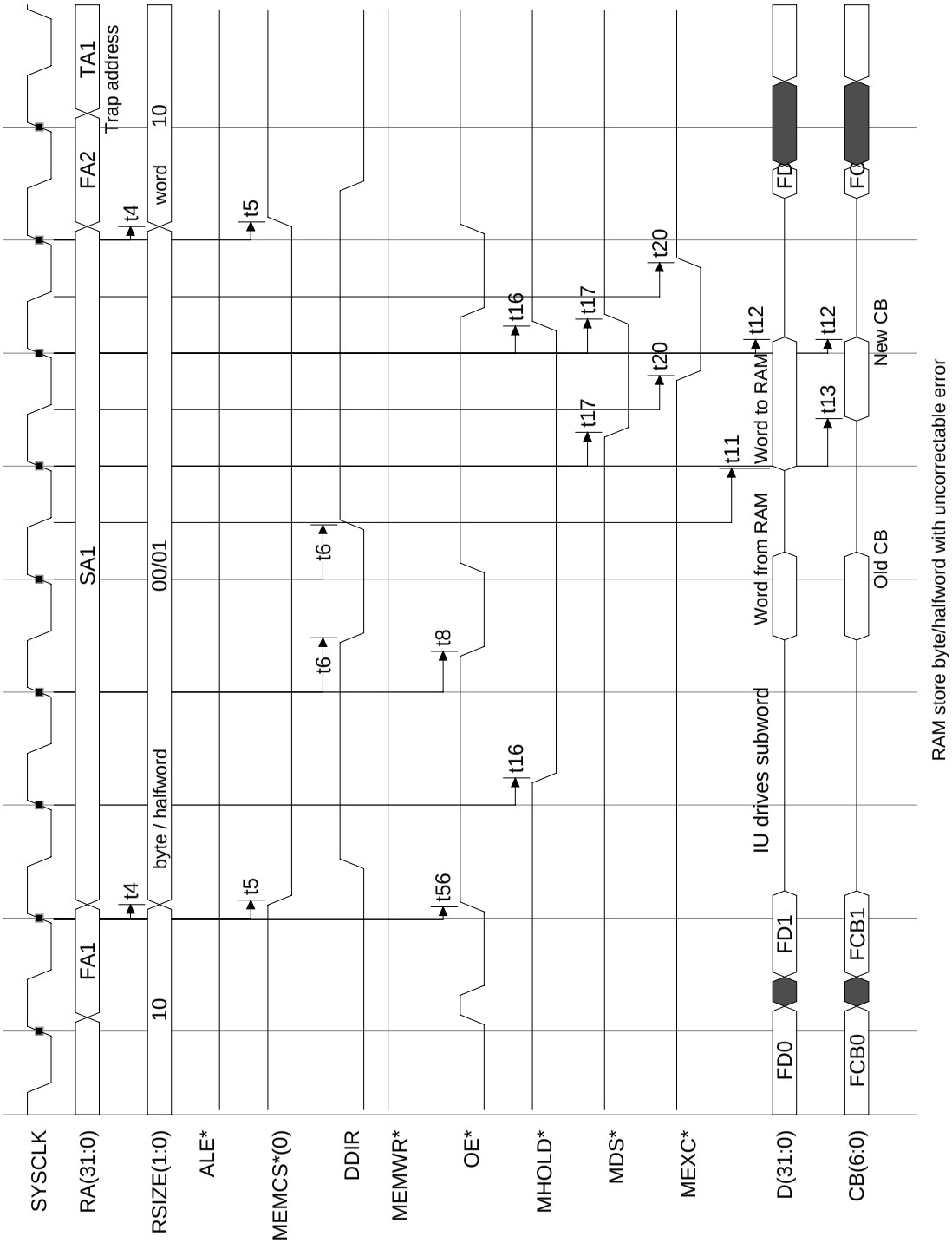

SYSCLK
RA(31:0)
ALE*
MEMCS*(0)
DDIR
OE*
MHOLD*
MDS*
MEXC*
D(31:0)
DPAR
CB(6:0)
FA2
LA1
t4
t5
t8
t14
t56
t18
t16
t17
t20
t10
t9
FD1
LD1 ERROR
FD2
FCB1
LCB1
FCB2
RAM load with uncorrectable error, no waitstate

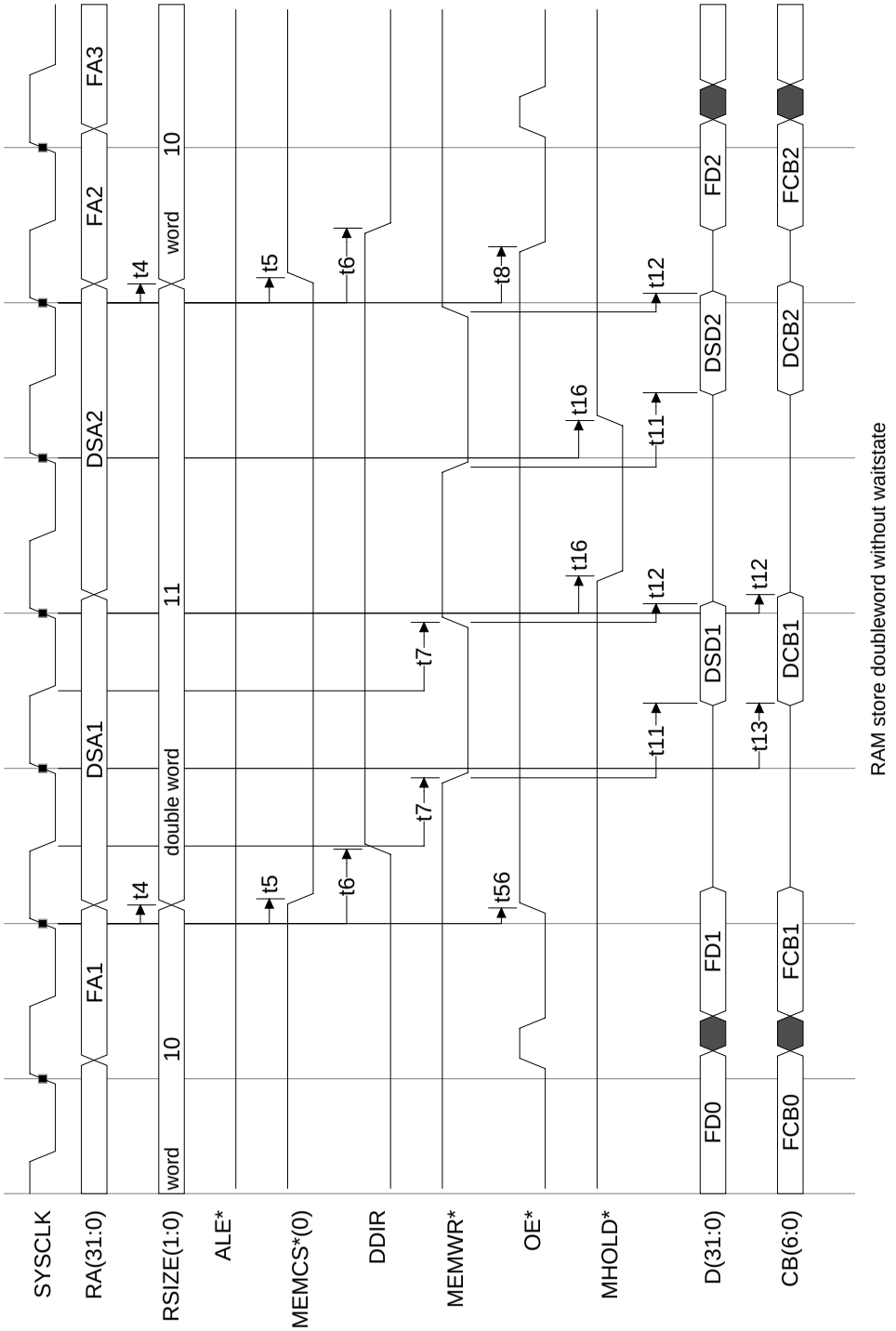

SYSCLK
RA(31:0)
ALE*
MEMCS*(0)
DDIR
OE*
MHOLD*
MDS*
MEXC*
D(31:0)
DPAR
CB(6:0)
FA3
FA2
LA1
FD2
FD1
FCB2
FCB1
t4
t5
t14
t56
t8
t16
t17
t20
RAM load with 1 waitstate and access violation

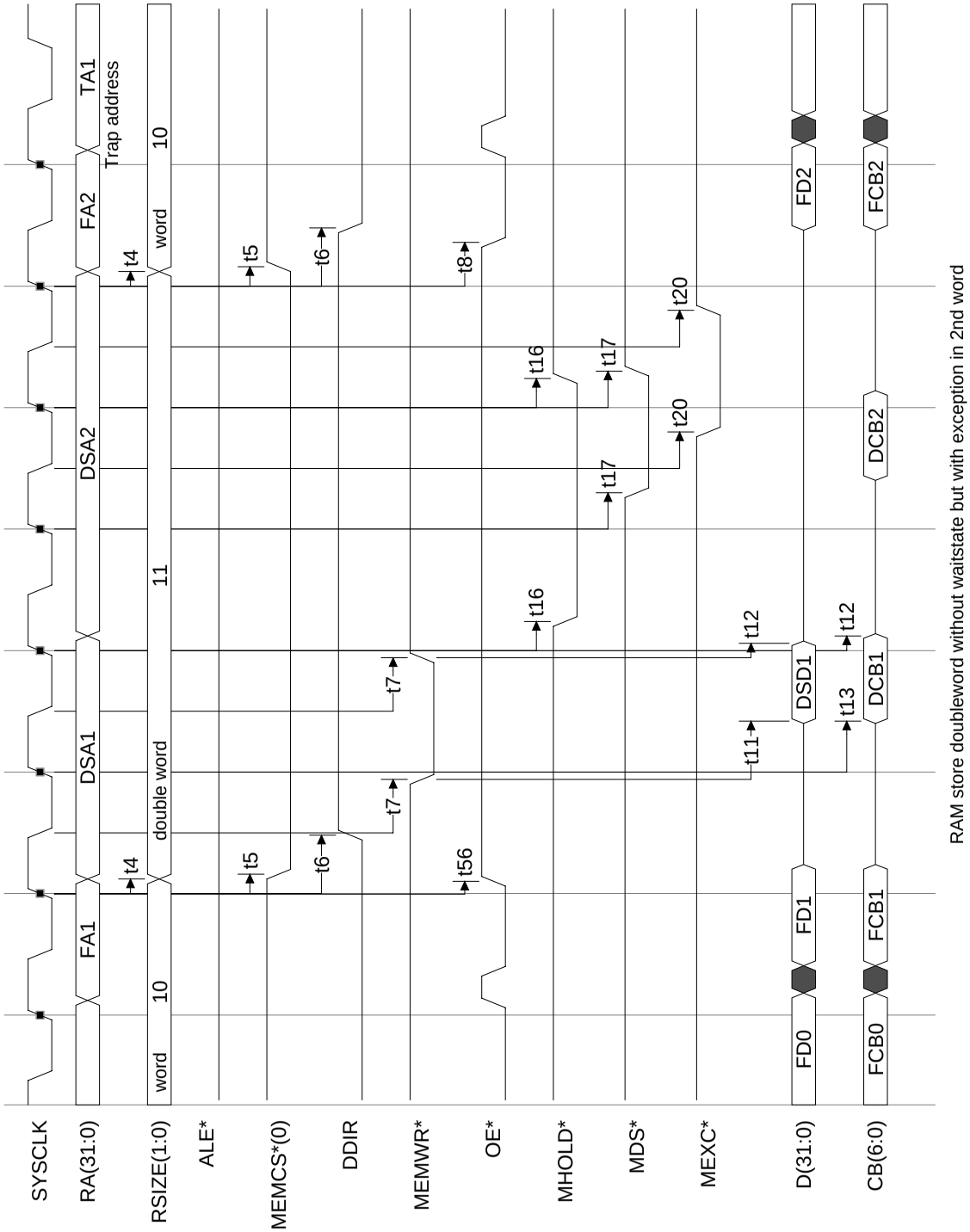

SYSCLK
RA(31:0)
ALE*
MEMCS*(0)
DDIR
MEMWR*
MHOLD*
MDS*
MEXC*
D(31:0)
DPAR
FA1
FA2
SA1
FD1
SD1
t4
t5
t6
t14
t16
t17
t20
Due to the violation, nd data is stored
RAM store with 1 waitstate and access violation

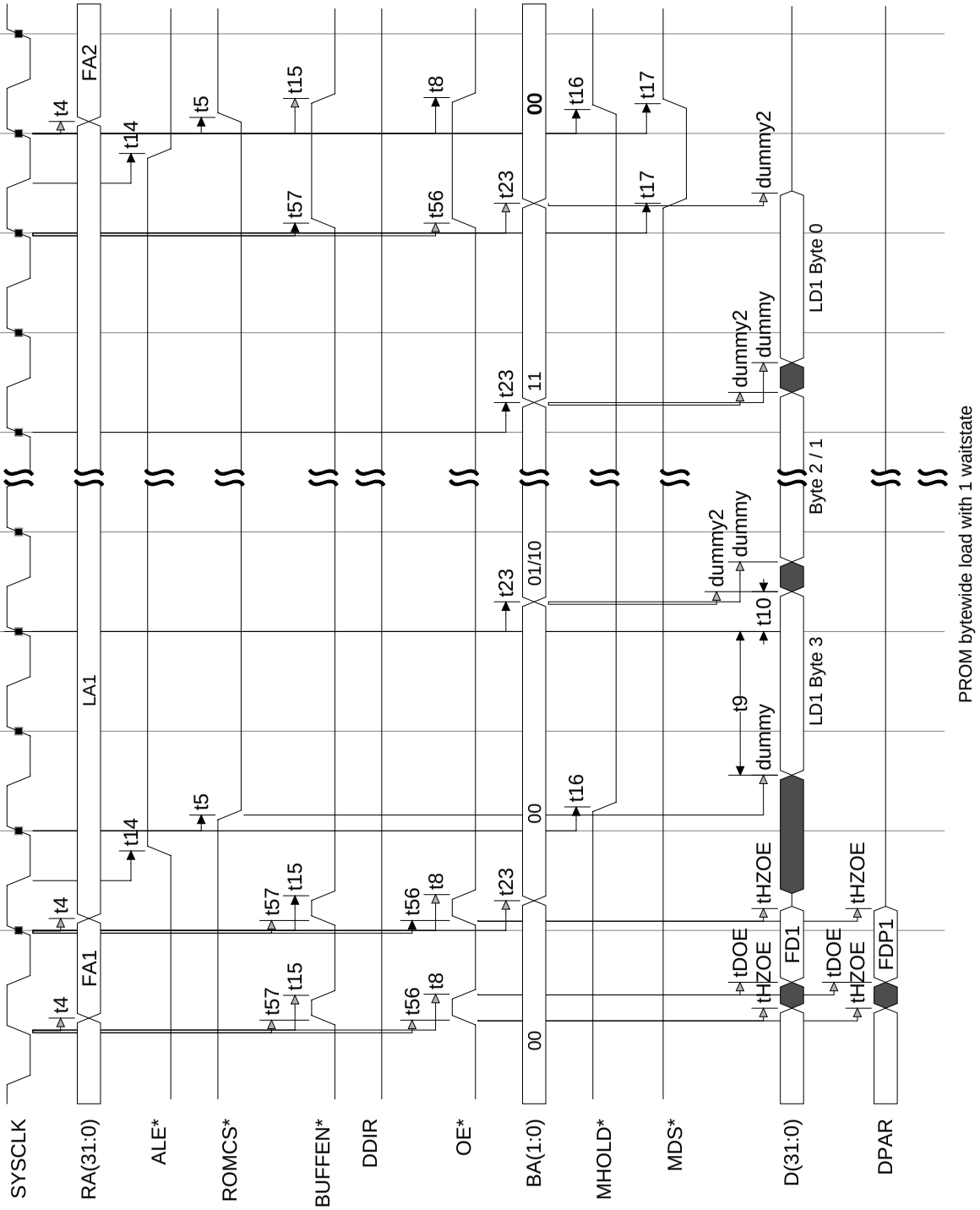

SYSCLK
RA(31:0)
ALE*
MEMCS*(0)
DDIR
MEMWR*
MHOLD*
MDS*
MEXC*
D(31:0)
DPAR
Trap addresses
TA2
TA1
FA2
FA1
SA1
FD2
FD1
SD1
TD2
TD1
t5
t6
t16
t17
t20
t9
t10
Due to the violation, no data is stored
RAM store without waitstate but with access violation

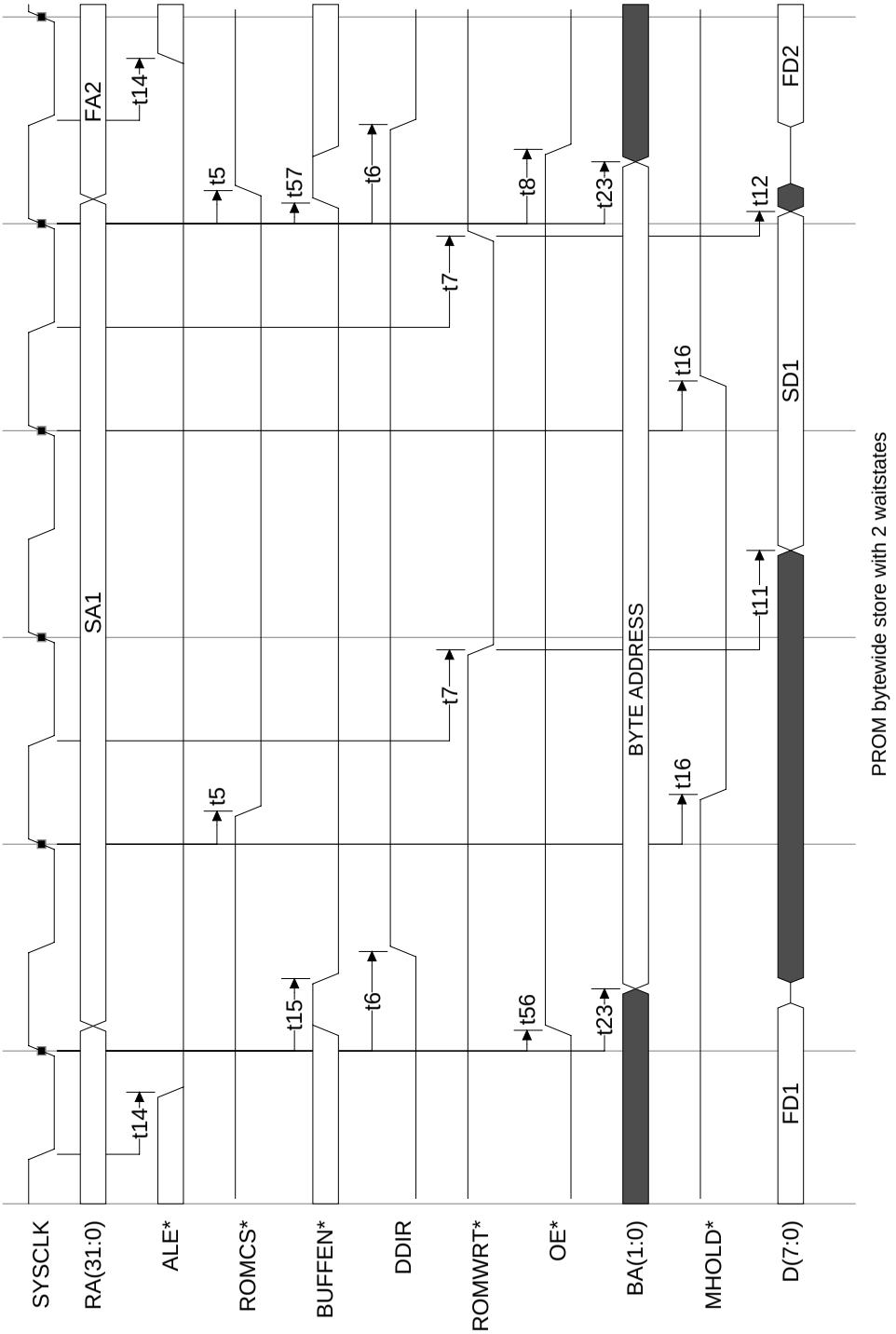

SYSCLK
RA(31:0)
RSIZE(1:0)
ALE*
MEMCS*(0)
DDIR
MEMWR*
OE*
MHOLD*
D(31:0)
DPAR
CB(6:0)
FA1
SA1
FA2
word
10
byte / halfword
00/01
10
FD0
FD1
FCB0
FCB1
t4
t5
t6
t7
t8
t56
t16
t11
t12
t13
IU drives subword
Word from RAM
Word to RAM
Old CB
New CB
RAM store byte/halfword without error or with correctable error

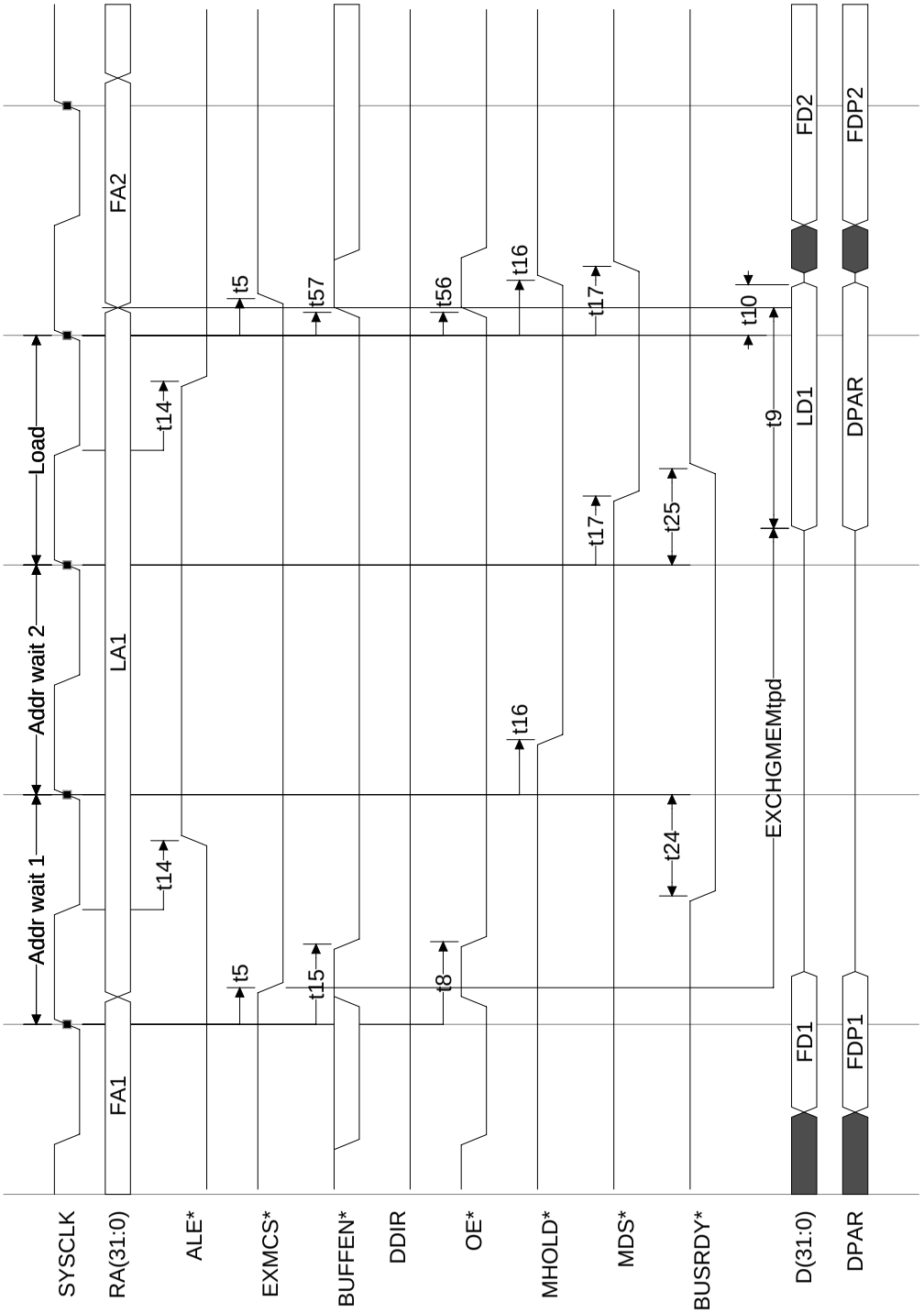

SYSCLK
RA(31:0)
RSIZE(1:0)
ALE*
MEMCS*(0)
DDIR
MEMWR*
OE*
MHOLD*
MDS*
MEXC*
D(31:0)
CB(6:0)
FA1
SA1
FA2
TA1
Trap address
10
00/01
word
byte / halfword
t4
t5
t6
t8
t56
t16
t17
t20
t11
t12
t13
FD0
FD1
FCB0
FCB1
IU drives subword
Word from RAM
Word to RAM
Old CB
New CB
RAM store byte/halfword with uncorrectable error

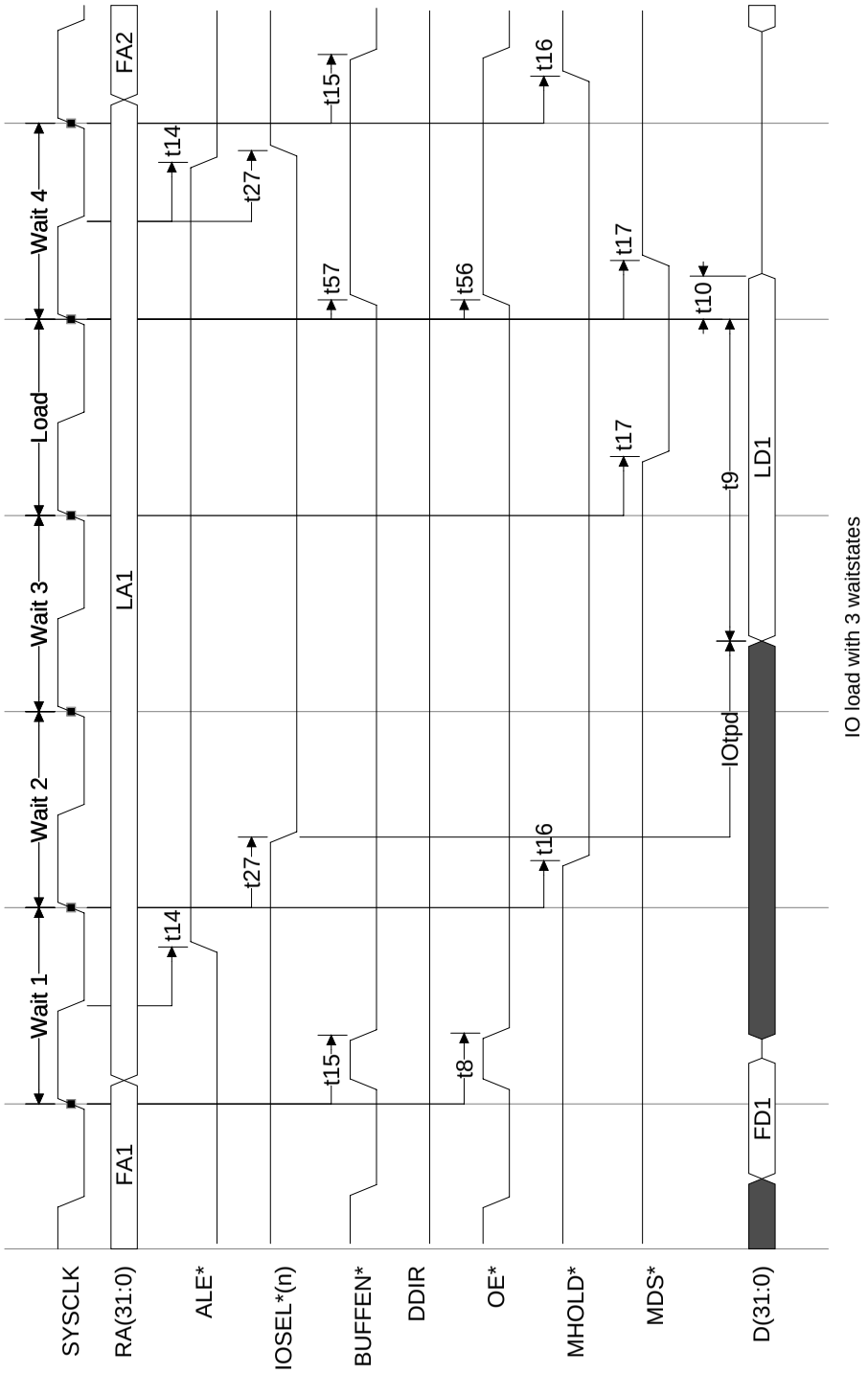

SYSCLK
RA(31:0)
RSIZE(1:0)
ALE*
MEMCS*(0)
DDIR
MEMWR*
OE*
MHOLD*
D(31:0)
CB(6:0)
FA1
FA2
FA3
DSA1
DSA2
word
double word
10
11
FD0
FD1
FD2
DSD1
DSD2
FCB0
FCB1
FCB2
DCB1
DCB2
t4
t5
t6
t7
t8
t11
t12
t13
t16
t56
RAM store doubleword without waitstate

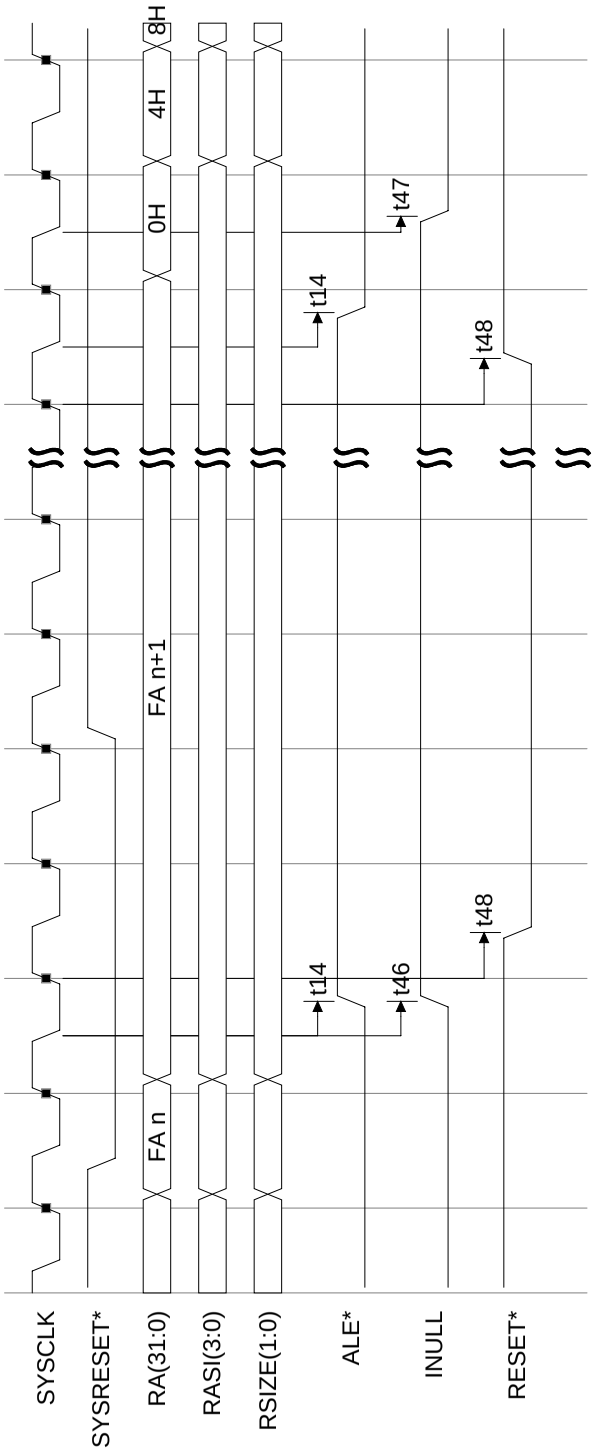

SYSCLK
RA(31:0)
RSIZE(1:0)
ALE*
MEMCS*(0)
DDIR
MEMWR*
OE*
MHOLD*
MDS*
MEXC*
D(31:0)
CB(6:0)
FA1
DSA1
DSA2
FA2
TA1
Trap address
word
10
double word
11
t4
t5
t6
t7
t56
t8
t16
t17
t20
t11
t12
t13
FD0
FD1
FD2
FCB0
FCB1
FCB2
DSD1
DCB1
DCB2
RAM store doubleword without waitstate but with exception in 2nd word


SYSCLK
RA(31:0)
ALE*
ROMCS*
BUFFEN*
DDIR
OE*
BA(1:0)
MHOLD*
MDS*
D(31:0)
DPAR
FA1
FA2
LA1
t4
t5
t8
t9
t10
t14
t15
t16
t17
t23
t56
t57
tDOE
tHZOE
FD1
FDP1
00
01/10
11
dummy
dummy2
LD1 Byte 0
Byte 2 / 1
LD1 Byte 3
PROM bytewide load with 1 waitstate

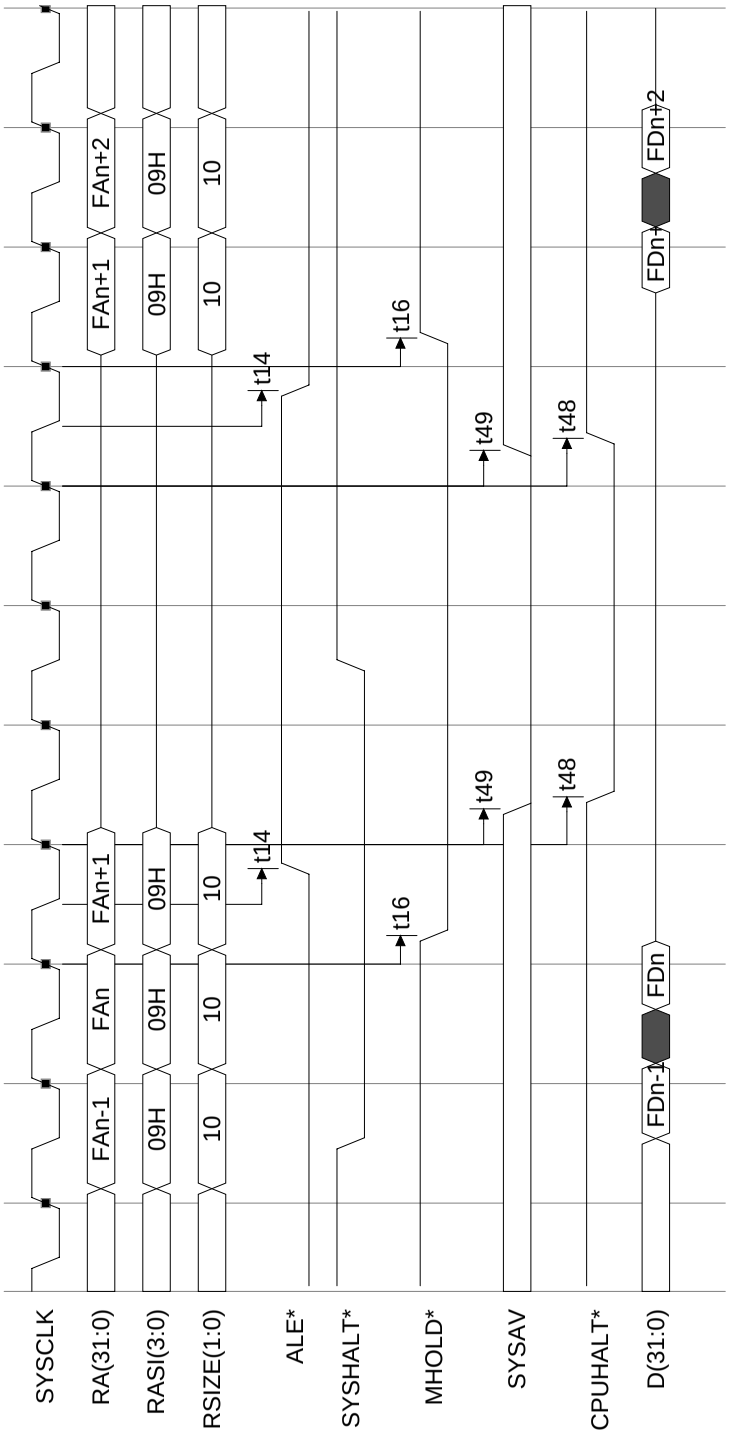

SYSCLK
RA(31:0)
ALE*
ROMCS*
BUFFEN*
DDIR
ROMWRT*
OE*
BA(1:0)
MHOLD*
D(7:0)
FA2
SA1
FD1
FD2
SD1
BYTE ADDRESS
t14
t5
t57
t6
t8
t23
t12
t7
t16
t11
t15
t56
PROM bytewide store with 2 waitstates


SYSCLK
RA(31:0)
ALE*
EXMCS*
BUFFEN*
DDIR
OE*
MHOLD*
MDS*
BUSRDY*
D(31:0)
DPAR
FA1
LA1
FA2
FD1
FDP1
LD1
DPAR
FD2
FDP2
Addr wait 1
Addr wait 2
Load
t5
t14
t15
t8
t16
t24
t25
t17
t56
t57
t10
t9
EXCHGMEMtpd
Exchange memory load with parity but without EDAC protection

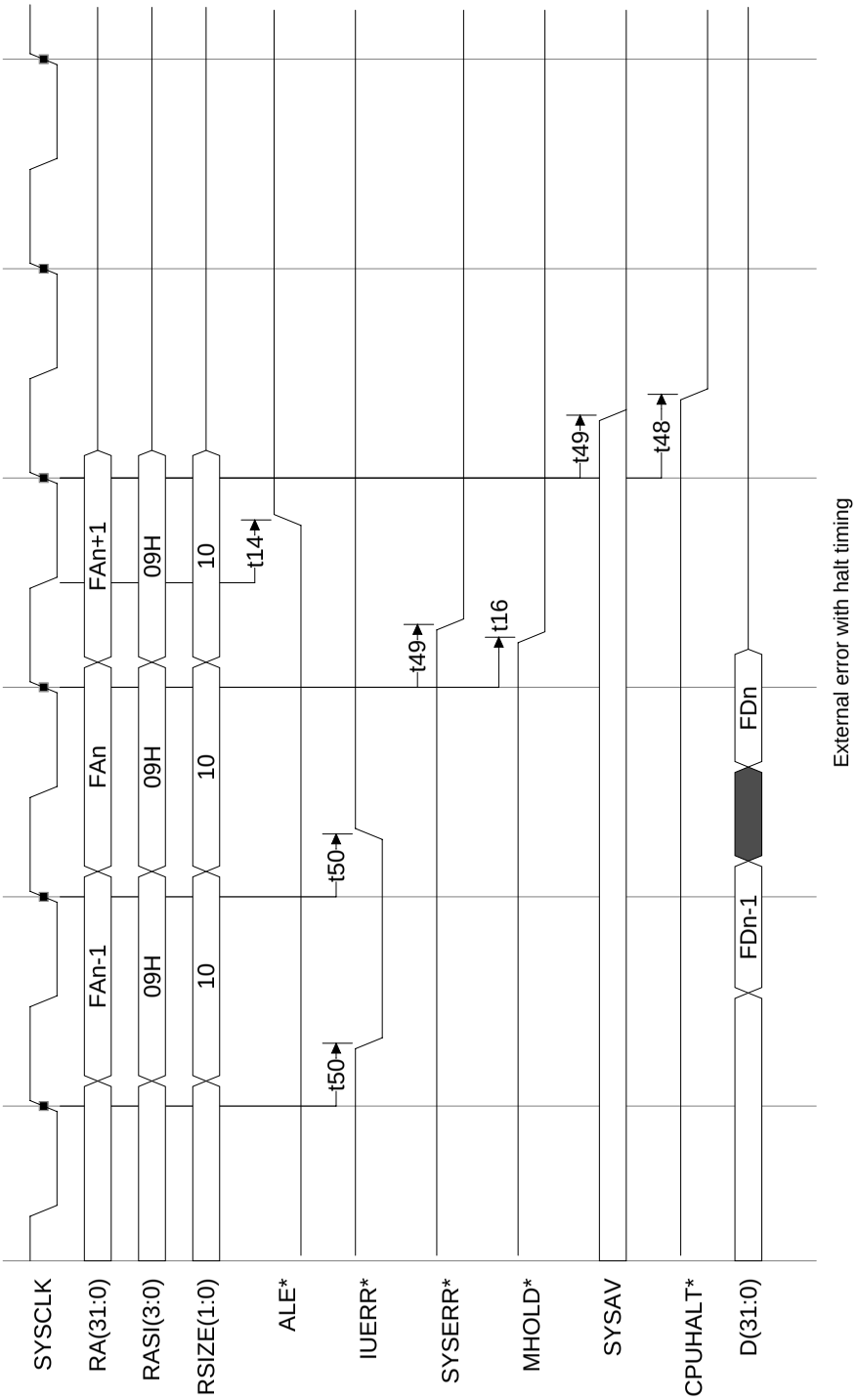

SYSCLK
RA(31:0)
ALE*
IOSEL*(n)
BUFFEN*
DDIR
OE*
MHOLD*
MDS*
D(31:0)
FA1
FA2
LA1
FD1
LD1
Wait 1
Wait 2
Wait 3
Load
Wait 4
t14
t27
t15
t57
t8
t56
t16
t17
t9
t10
IOtpd
IO load with 3 waitstates

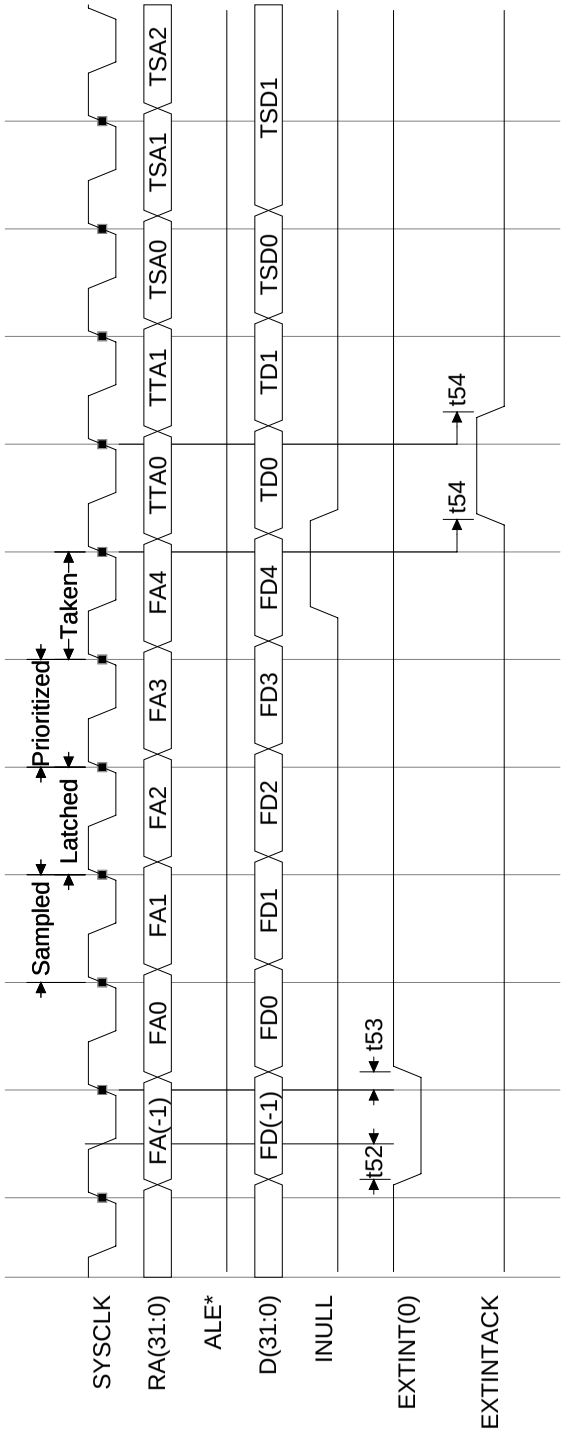


Reset timing


SYSCLK
RA(31:0)
RASI(3:0)
RSIZE(1:0)
ALE*
SYSHALT*
MHOLD*
SYSAV
CPUHALT*
D(31:0)
FAn-1
FAn
FAn+1
FAn+2
09H
10
FDn-1
FDn
FDn+1
FDn+2
t14
t16
t49
t48

Halt timing


SYSCLK
RA(31:0)
RASI(3:0)
RSIZE(1:0)
ALE*
IUERR*
SYSERR*
MHOLD*
SYSAV
CPUHALT*
D(31:0)
FAn-1
FAn
FAn+1
09H
10
t14
t50
t49
t16
t48
FDn-1
FDn
External error with halt timing

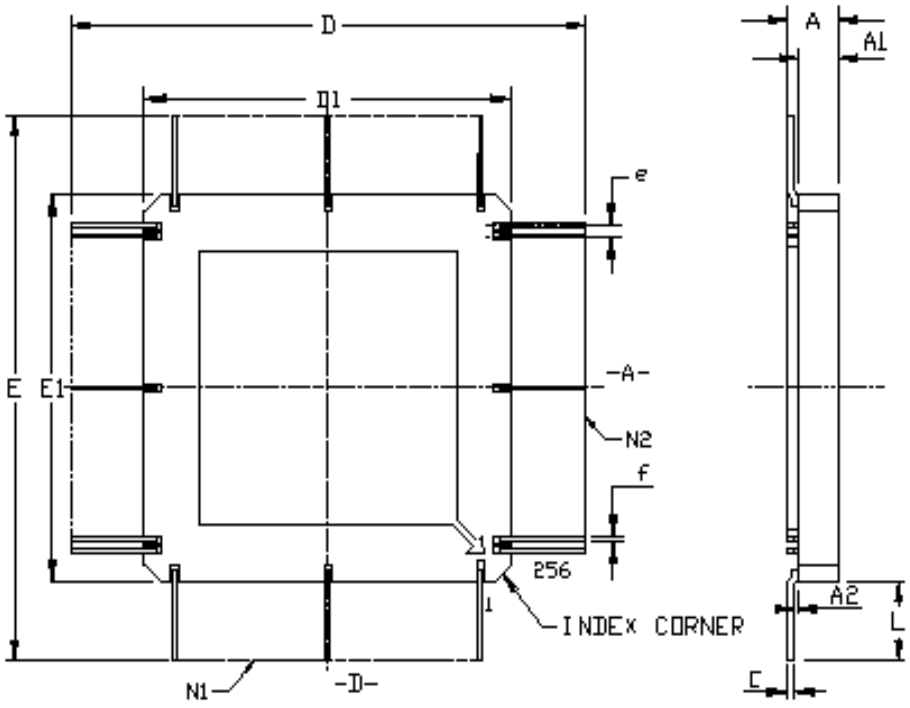


Edge triggered interrupt timing

6.3 Package Description

6.3.1 256-pin MQFP-F Package

256 LEAD MQFP_F



	mm		mils	
	Min	Max	Min	Max
A	2.41	3.18	.095	.125
C	0.10	0.20	.004	.008
D	53.23	55.74	2.095	2.195
D1	36.83	37.34	1.450	1.470
E	53.23	55.74	2.095	2.195
E1	36.83	37.34	1.450	1.470
e	0.508 BSC		.020 BSC	
f	0.15	0.25	.006	.010
A1	2.06	2.56	.081	.101
A2	0.05	0.36	.002	.014
L	8.20	9.20	.323	.362
N1	64		64	
N2	64		64	

6.3.2 256-pin MQFP-F Pin Assiggnments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GPIINT	65	D[0]	129	RA[0]	193	DXFER
2	GPI[7]	66	RSIZE[1]	130	VCCO	194	MEXC ✻
3	VCCO	67	RSIZE[0]	131	VSSO	195	VCCO
4	VSSO	68	RASI[3]	132	RAPAR	196	VSSO
5	GPI[6]	69	VCCO	133	RASPAR	197	RESET ✻
6	GPI[5]	70	VSSO	134	DPAR	198	SYSRESET ✻
7	GPI[4]	71	RASI[2]	135	VCCO	199	BA[1]
8	GPI[3]	72	RASI[1]	136	VSSO	200	BA[0]
9	VCCO	73	RASI[0]	137	SYSCLK	201	CB[6]
10	VSSO	74	RA[31]	138	TDO	202	CB[5]
11	GPI[2]	75	RA[30]	139	TRST ✻	203	VCCO
12	GPI[1]	76	VCCO	140	TMS	204	VSSO
13	GPI[0]	77	VSSO	141	TDI	205	CB[4]
14	D[31]	78	RA[29]	142	TCK	206	CB[3]
15	D[30]	79	RA[28]	143	CLK2	207	CB[2]
16	VCCO	80	RA[27]	144	DRDY ✻	208	CB[1]
17	VSSO	81	VCCO	145	DMAAS	209	VCCO
18	D[29]	82	VSSO	146	VCCO	210	VSSO
19	D[28]	83	RA[26]	147	VSSO	211	CB[0]
20	VCCI	84	RA[25]	148	DMAGNT ✻	212	ALE ✻
21	VSSI	85	RA[24]	149	EXMCS ✻	213	VCCI
22	D[27]	86	VCCI	150	VCCI	214	VSSI
23	D[26]	87	VSSI	151	VSSI	215	PROM8 ✻
24	VCCO	88	VCCO	152	DMAREQ ✻	216	ROMCS ✻
25	VSSO	89	VSSO	153	BUSERR ✻	217	MEMCS[9] ✻
26	D[25]	90	RA[23]	154	BUSRDY ✻	218	VCCO
27	D[24]	91	RA[22]	155	ROMWRT ✻	219	VSSO
28	D[23]	92	RA[21]	156	NOPAR ✻	220	MEMCS[8] ✻
29	D[22]	93	VCCO	157	SYSHALT ✻	221	MEMCS[7] ✻
30	VCCO	94	VSSO	158	CPUHALT ✻	222	MEMCS[6] ✻
31	VSSO	95	RA[20]	159	VCCO	223	MEMCS[5] ✻
32	D[21]	96	RA[19]	160	VSSO	224	MEMCS[4] ✻
33	D[20]	97	RA[18]	161	SYSERR ✻	225	MEMCS[3] ✻
34	D[19]	98	VCCO	162	SYSAV	226	VCCO
35	D[18]	99	VSSO	163	EXTINT[4]	227	VSSO
36	VCCO	100	RA[17]	164	EXTINT[3]	228	MEMCS[2] ✻
37	VSSO	101	RA[16]	165	EXTINT[2]	229	MEMCS[1] ✻
38	D[17]	102	RA[15]	166	EXTINT[1]	230	MEMCS[0] ✻
39	D[16]	103	VCCO	167	EXTINT[0]	231	VCCI
40	VCCI	104	VSSO	168	VCCI	232	VSSI
41	VSSI	105	RA[14]	169	VSSI	233	OE ✻
42	D[15]	106	VCCI	170	EXTINTACK	234	VCCO
43	D[14]	107	VSSI	171	IUERR ✻	235	VSSO
44	VCCO	108	RA[13]	172	VCCO	236	MEMWR ✻
45	VSSO	109	RA[12]	173	VSSO	237	BUFFEN ✻
46	D[13]	110	VCCO	174	CPAR	238	DDIR
47	D[12]	111	VSSO	175	TXA	239	VCCO
48	D[11]	112	RA[11]	176	RXA	240	VSSO
49	D[10]	113	RA[10]	177	RXB	241	DDIR ✻
50	VCCO	114	RA[9]	178	TXB	242	MHOLD ✻
51	VSSO	115	VCCO	179	IOWR ✻	243	MDS ✻
52	D[9]	116	VSSO	180	IOSEL[3] ✻	244	WDCLK
53	D[8]	117	RA[8]	181	VCCO	245	IWDE
54	D[7]	118	RA[7]	182	VSSO	246	EWDINT
55	D[6]	119	RA[6]	183	IOSEL[2] ✻	247	TMODE[1]
56	VCCO	120	VCCO	184	IOSEL[1] ✻	248	TMODE[0]
57	VSSO	121	VSSO	185	IOSEL[0] ✻	249	DEBUG
58	D[5]	122	RA[5]	186	WRT	250	INULL
59	D[4]	123	RA[4]	187	WE ✻	251	DIA
60	D[3]	124	RA[3]	188	VCCO	252	VCCO
61	D[2]	125	VCCO	189	VSSO	253	VSSO
62	VCCO	126	VSSO	190	RD	254	FLUSH
63	VSSO	127	RA[2]	191	RLDSTO	255	INST
64	D[1]	128	RA[1]	192	LOCK	256	RTC

❑ Note: XYZ✻ ≡ $\overline{XYZ}$, signal active low