Features

- **Programmable 4,194,304 x 1 and 8,388,608 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)**
- **3.3V Output Capability**
- **5V Tolerant I/O Pins**
- **In-System Programmable (ISP) via 2-wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Compatible with Atmel AT40K and AT94K Devices, Altera FLEX®, APEX™ Devices, Lucent ORCA® FPGAs, Xilinx XC3000™, XC4000™, XC5200™, Spartan®, Virtex® FPGAs, Motorola MPA1000 FPGAs**
- **Cascadable Read-back to Support Additional Configurations or Higher-density Arrays**
- **Low-power CMOS FLASH Process**
- **Available in 6 mm x 6 mm x 1 mm 8-lead LAP (Pin-compatible with 8-lead SOIC/VOIC Packages), 20-lead PLCC, 44-lead PLCC and 44-lead TQFP Packages**
- **Emulation of Atmel's AT24CXXX Serial EEPROMs**
- **Low-power Standby Mode**
- **Single Device Capable of Holding 4 Bitstream Files Allowing Simple System Reconfiguration**
- **Fast Serial Download Speeds up to 33 MHz**

Description

The AT17F Series of In-System Programmable Configuration PROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17F Series device is packaged in the 8-lead LAP, 20-lead PLCC, 44-lead PLCC and 44-lead TQFP, see Table 1. The AT17F Series Configurator uses a simple serial-access procedure to configure one or more FPGA devices.

The AT17F Series Configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable.

Table 1. AT17F Series Packages

Package	AT17F040	AT17F080
8-lead LAP	Yes	Yes
20-lead PLCC	Yes	Yes
44-lead PLCC	–	Yes
44-lead TQFP	–	Yes

In-System Programmable Configuration PROM

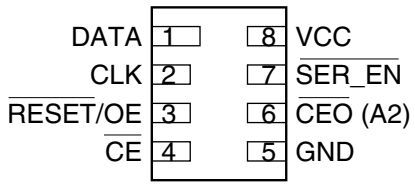
AT17F040
AT17F080

Advance Information

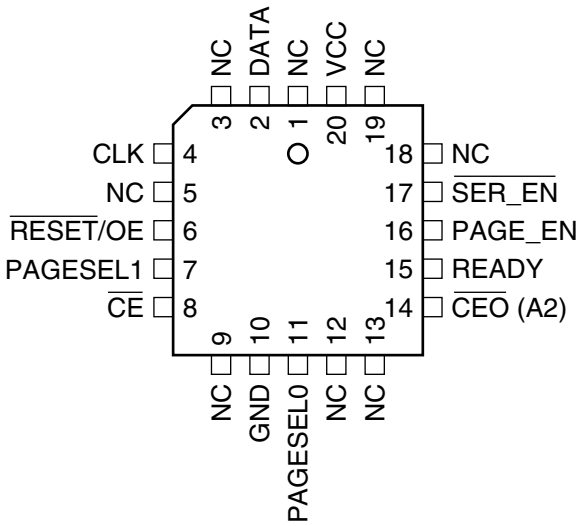
Rev. 3039A–CNFG–06/02

Pin Configuration

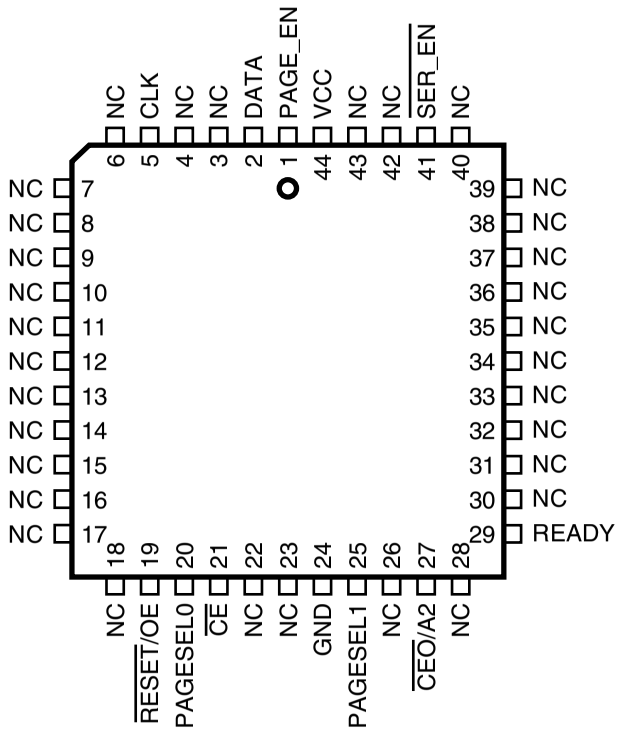
8-lead LAP



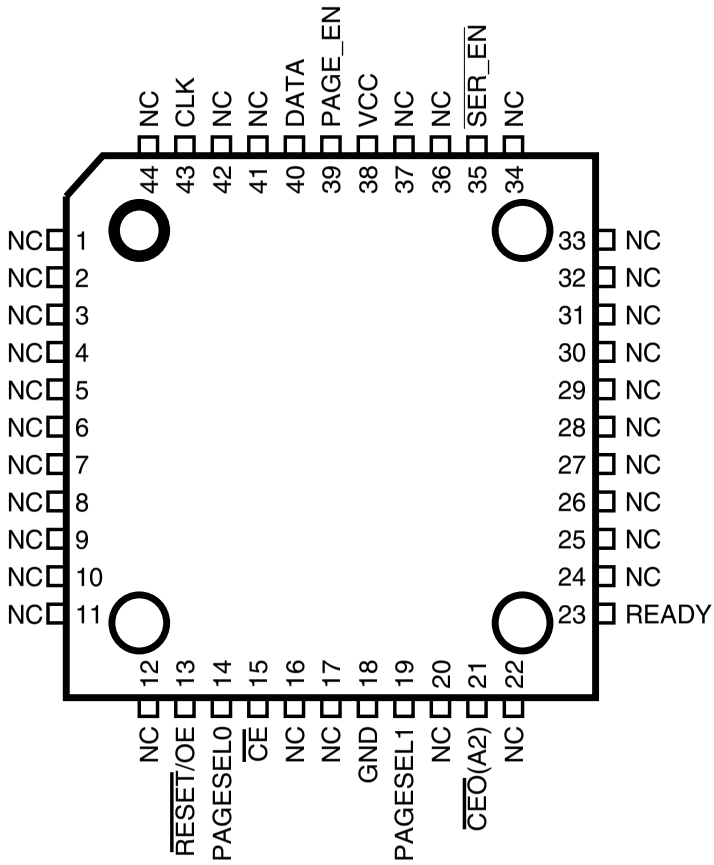
20-lead PLCC



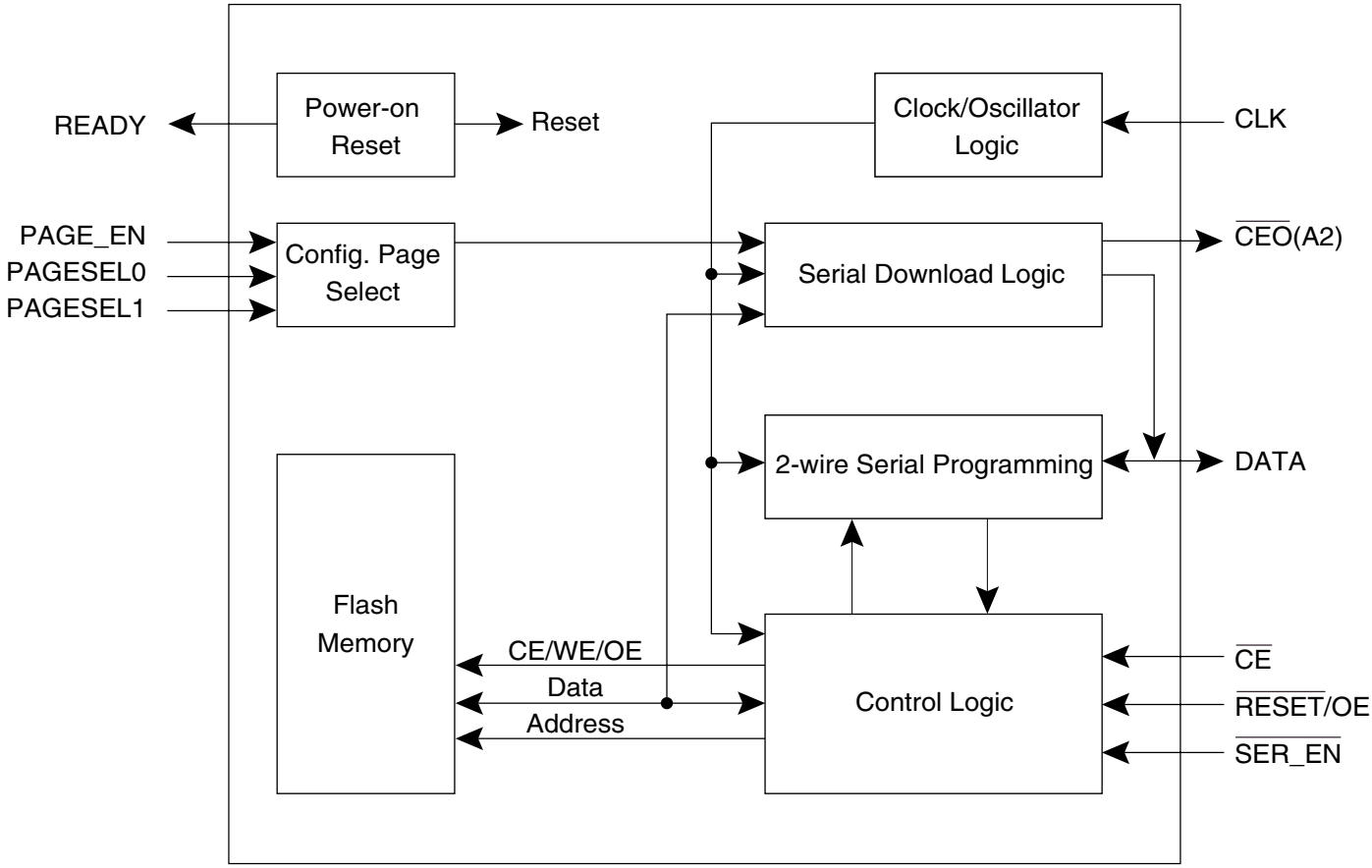
44 PLCC



44 TQFP



Block Diagram



Device Description

The control signals for the configuration memory device ($\overline{CE}$, $\overline{RESET}$/OE and CLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration device without requiring an external intelligent controller.

The $\overline{RESET}$/OE and $\overline{CE}$ pins control the tri-state buffer on the DATA output pin and enable the address counter. When $\overline{RESET}$/OE is driven Low, the configuration device resets its address counter and tri-states its DATA pin. The $\overline{CE}$ pin also controls the output of the AT17F Series Configurator. If $\overline{CE}$ is held High after the $\overline{RESET}$/OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When OE is subsequently driven High, the counter and the DATA output pin are enabled. When $\overline{RESET}$/OE is driven Low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of $\overline{CE}$.

When the configurator has driven out all of its data and $\overline{CEO}$ is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

Pin Description

Name	I/O	AT17F040		AT17F080			
		8 LAP	20 PLCC	8 LAP	20 PLCC	44 PLCC	44 TQFP
DATA	I/O	1	2	1	2	2	40
CLK	I	2	4	2	4	5	43
PAGE_EN	I	–	16	–	16	1	39
PAGESEL0	I	–	11	–	5	20	14
PAGESEL1	I	–	7	–	7	25	19
$\overline{\text{RESET}}$/OE	I	3	6	3	6	19	13
$\overline{\text{CE}}$	I	4	8	4	8	21	15
GND	–	5	10	5	10	24	18
$\overline{\text{CEO}}$	O	6	14	6	14	27	21
A2	I						
READY	O	–	15	–	15	29	23
$\overline{\text{SER\_EN}}$	I	7	17	7	17	41	35
V_{CC}	–	8	20	8	20	44	38

DATA

Three-state DATA output for configuration. Open-collector bi-directional pin for programming.

CLK

Clock input. Used to increment the internal address and bit counter for reading and programming.

PAGE_EN

Input used to enable page download mode. When PAGE_EN is high the configuration download address space is partitioned into 4 equal pages. This gives users the ability to easily store and retrieve multiple configuration bitstreams from a single configuration device. This input works in conjunction with the PAGESEL inputs. PAGE_EN must be held low if paging is not desired. When SER_EN is Low (ISP mode) this pin has no effect.

PAGESEL[1:0]

Page select inputs. Used to determine which of the 4 memory pages are targeted during a serial configuration download. The address space for each of the pages is shown in Table 2. When SER_EN is Low (ISP mode) these pins have no effect.

Table 2. Address Space

Paging Decodes	AT17F040 (4 Mbits)	AT17F080 (8 Mbits)
PAGESEL = 00, PAGE_EN = 1	00000 – 0FFFFh	00000 – 1FFFFh
PAGESEL = 01, PAGE_EN = 1	10000 – 1FFFFh	20000 – 3FFFFh
PAGESEL = 10, PAGE_EN = 1	20000 – 2FFFFh	40000 – 5FFFFh
PAGESEL = 11, PAGE_EN = 1	30000 – 3FFFFh	60000 – 7FFFFh
PAGESEL = XX, PAGE_EN = 0	00000 – 3FFFFh	00000 – 7FFFFh

$\overline{\text{RESET}}$/OE — Output Enable (active High) and RESET (active Low) when $\overline{\text{SER\_EN}}$ is High. A Low level on $\overline{\text{RESET}}$/OE resets both the address and bit counters. A High level (with $\overline{\text{CE}}$ Low) enables the data output driver.

$\overline{\text{CE}}$ — Chip Enable input (active Low). A Low level (with OE High) allows CLK to increment the address counter and enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will *not* enable/disable the device in the 2-wire Serial Programming mode ($\overline{\text{SER\_EN}}$ Low).

GND — Ground pin. A 0.2 µF decoupling capacitor between V_{CC} and GND is recommended.

$\overline{\text{CEO}}$ — Chip Enable Output (active Low). This output goes Low when the address counter has reached its maximum value. If the PAGE_EN input is set High, the maxvalue is the highest address in the selected partition. The PAGESEL[1:0] inputs are used to make the 4 partition selections. If the PAGE_EN input is set Low, the device is not partitioned and the address maxvalue is the highest address in the device, see Table 2 on page 5. In a daisy chain of AT17F Series devices, the $\overline{\text{CEO}}$ pin of one device must be connected to the $\overline{\text{CE}}$ input of the next device in the chain. It will stay Low as long as $\overline{\text{CE}}$ is Low and OE is High. It will then follow CE until OE goes Low; thereafter, $\overline{\text{CEO}}$ will stay High until the entire EEPROM is read again.

A2 — Device selection input, A2. This is used to enable (or select) the device during programming (i.e., when $\overline{\text{SER\_EN}}$ is Low). A2 has an internal pull-down resistor.

READY — Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. (recommended 4.7 kΩ pull-up on this pin if used).

$\overline{\text{SER\_EN}}$ — Serial enable must be held High during FPGA loading operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the 2-Wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER\_EN}}$ should be tied to V_{CC}.

V_{CC} — +3.3V (±10%).

FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17F Serial Configuration PROM has been designed for compatibility with the Master Serial mode.

This document discusses the Atmel AT40K, AT40KAL and AT94KAL applications as well as Xilinx applications.

Control of Configuration

Most connections between the FPGA device and the AT17F Serial Configurator PROM are simple and self-explanatory.

- The DATA output of the AT17F Series Configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17F Series Configurator.
- The $\overline{CEO}$ output of any AT17F Series Configurator drives the $\overline{CE}$ input of the next Configurator in a cascade chain of configurator devices.
- $\overline{SER\_EN}$ must be connected to V_{CC} (except during ISP).
- The READY pin is available as an open-collector indicator of the device's reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.
- PAGE_EN must be held Low if download paging is not desired. The PAGESEL[1:0] inputs must be tied off High or Low. If paging is desired, PAGE_EN must be High and the PAGESEL pins must be set to High or Low such that the desired page is selected, see Table 2 on page 5.

Cascading Serial Configuration Devices

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded configurators provide additional memory.

After the last bit from the first configurator is read, the clock signal to the configurator asserts its $\overline{CEO}$ output Low and disables its DATA line driver. The second configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the $\overline{RESET}$/OE on each configurator is driven to its active (Low) level.

If the address counters are not to be reset upon completion, then the $\overline{RESET}$/OE input can be tied to its inactive (High) level.

Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip. The AT17F parts are read/write at 3.3V nominal. Refer to the AT17F Configuration application note available on the Atmel web site (www.atmel.com) for more programming details.

Standby Mode

The AT17F Series Configurators enter a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the AT17F Configurator consumes less than 50 µA of current at 3.3V. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

Absolute Maximum Ratings*

Operating Temperature	-4°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} +0.5V
Supply Voltage (V_{CC})	-0.5V to +4.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

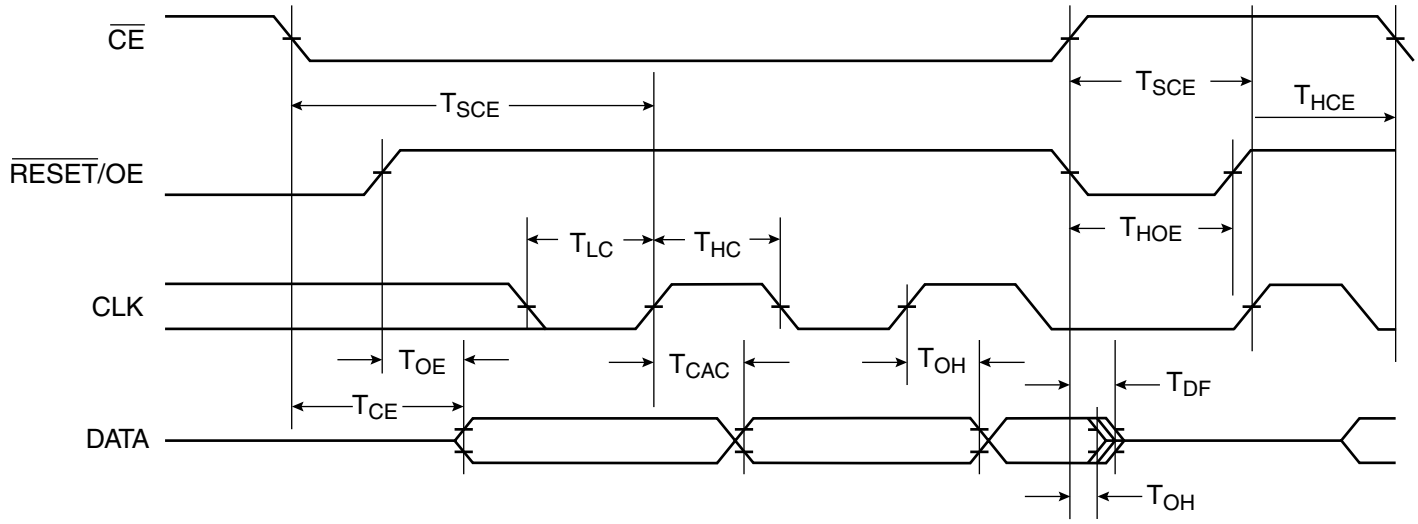
Operating Conditions

Symbol	Description		AT17F Series Configurator Min	AT17F Series Configurator Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	2.97	3.63	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	2.97	3.63	V

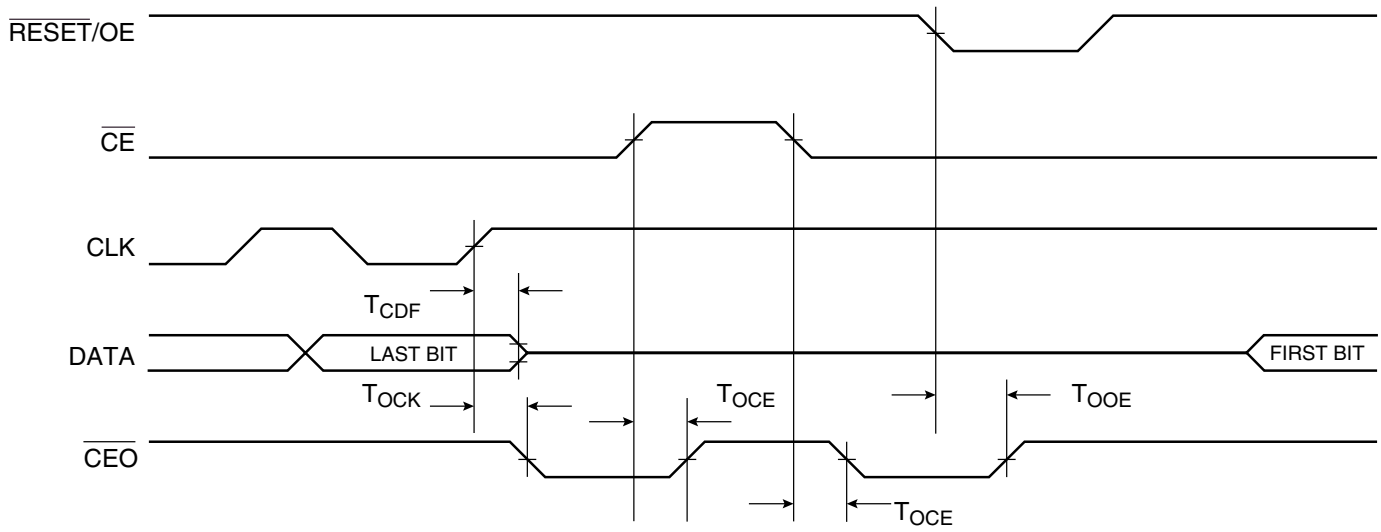
DC Characteristics

Symbol	Description		AT17F040 Min	AT17F040 Max	AT17F080 Min	AT17F080 Max	Units
V_{IH}	High-level Input Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0	0.8	0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)	Commercial		0.4		0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	2.4		2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)	Industrial		0.4		0.4	V
I_{CCA}	Supply Current, Active Mode			5		5	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	-10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		100		200	µA
		Industrial		100		200	µA

AC Characteristics



AC Characteristics when Cascading



AC Characteristics

Symbol	Description		AT17F040		AT17F080		Units
			Min	Max	Min	Max	
T_{OE}[2]	OE to Data Delay	Commercial		50		50	ns
		Industrial[1]		55		55	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay	Commercial		60		55	ns
		Industrial[1]		60		60	ns
T_{CAC}[2]	CLK to Data Delay	Commercial		75		55	ns
		Industrial[1]		80		60	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	Commercial	0		0		ns
		Industrial[1]	0		0		ns
T_{DF}[3]	$\overline{CE}$ or OE to Data Float Delay	Commercial		55		50	ns
		Industrial[1]		55		50	ns
T_{LC}	CLK Low Time	Commercial	20		20		ns
		Industrial[1]	20		20		ns
T_{HC}	CLK High Time	Commercial	20		20		ns
		Industrial[1]	20		20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	Commercial	35		20		ns
		Industrial[1]	40		25		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	Commercial	0		0		ns
		Industrial[1]	0		0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	Commercial	20		20		ns
		Industrial[1]	20		20		ns
F_{MAX}	Maximum Input Clock Frequency SEREN = 0	Commercial		10		10	MHz
		Industrial[1]		10		10	MHz
F_{MAX}	Maximum Input Clock Frequency SEREN = 1	Commercial		33		33	MHz
		Industrial[1]		33		33	MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test lead = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

AC Characteristics When Cascading

Symbol	Description		AT17F040 Min	AT17F040 Max	AT17F080 Min	AT17F080 Max	Units
T_{CDF}[3]	CLK to Data Float Delay	Commercial		60		50	ns
		Industrial[1]		60		50	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay	Commercial		55		50	ns
		Industrial[1]		60		55	ns
T_{OCE}[2]	$\overline{CE}$ to $\overline{CEO}$ Delay	Commercial		55		35	ns
		Industrial[1]		60		40	ns
T_{OOE}[2]	$\overline{RESET}$/OE to $\overline{CEO}$ Delay	Commercial		40		35	ns
		Industrial[1]		45		35	ns
F_{MAX}	Maximum Input Clock Frequency	Commercial		33		33	MHz
		Industrial[1]		33		33	MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test lead = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

Thermal Resistance Coefficients[1]

Package Type			AT17F040	AT17F080
8CN4	Leadless Array Package (LAP)	θ_{JC} [°C/W]	–	–
		θ_{JA} [°C/W][2]	–	–
20J	Plastic Leaded Chip Carrier (PLCC)	θ_{JC} [°C/W]	–	–
		θ_{JA} [°C/W][2]	–	–
44A	Thin Plastic Quad Flat Package (TQFP)	θ_{JC} [°C/W]	17	17
		θ_{JA} [°C/W][2]	62	62
44J	Plastic Leaded Chip Carrier (PLCC)	θ_{JC} [°C/W]	15	15
		θ_{JA} [°C/W][2]	50	50

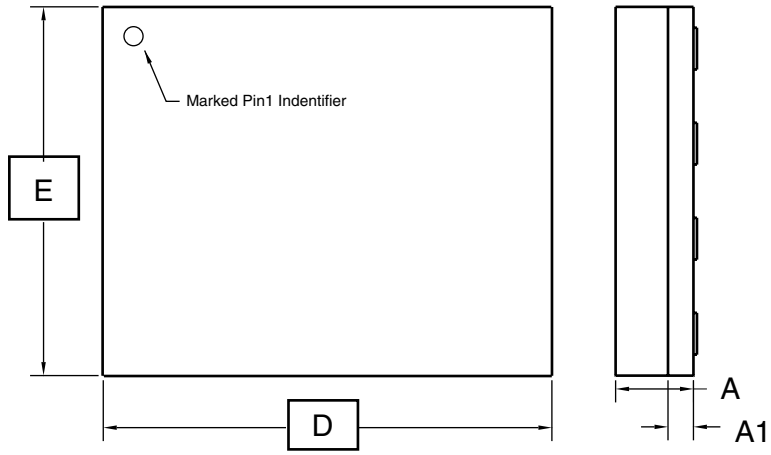
Notes: 1. For more information refer to the “Thermal Characteristics of Atmel’s Packages”, available on the Atmel web site, at http://www.atmel.com/atmel/acrobat/doc0636.pdf.
2. Airflow = 0 ft/min.

Ordering Information

Memory Size	Ordering Code	Package	Operation Range
4-Mbit	AT17F040-10TQC AT17F040-10BJC	8CN4 - 8 LAP 20J - 20 PLCC	Commercial (0°C to 70°C)
	AT17F040-10TQI AT17F040-10BJI	8CN4 - 8 LAP 20J - 20 PLCC	Industrial (-40°C to 85°C)
8-Mbit	AT17F080-10CC AT17F080-10JC AT17F080-10TQC AT17F080-10BJC	8CN4 - 8 LAP 20J - 20 PLCC 44A - 44 TQFP 44J - 44 PLCC	Commercial (0°C to 70°C)
	AT17F080-10CI AT17F080-10JI AT17F080-10TQI AT17F080-10BJI	8CN4 - 8 LAP 20J - 20 PLCC 44A - 44 TQFP 44J - 44 PLCC	Industrial (-40°C to 85°C)

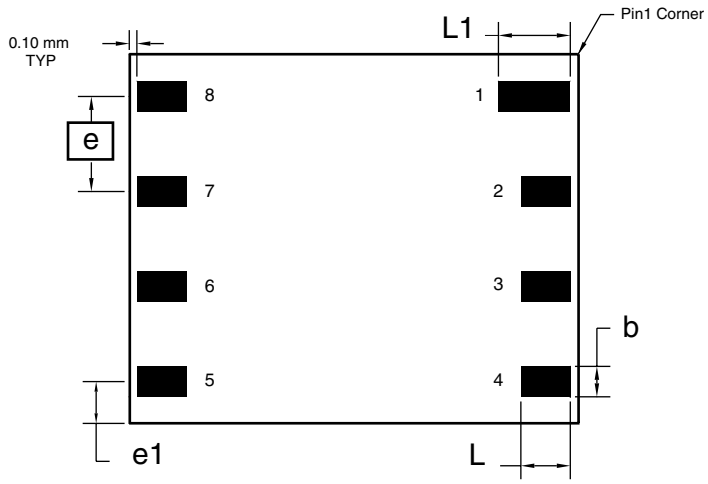
Package Type	
8CN4	8-lead, 6 mm x 6 mm x 1 mm, Leadless Array Package (LAP) – Pin-compatible with 8-lead SOIC/VOID Packages
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
44A	44-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)

8CN4 – LAP



Top View

Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

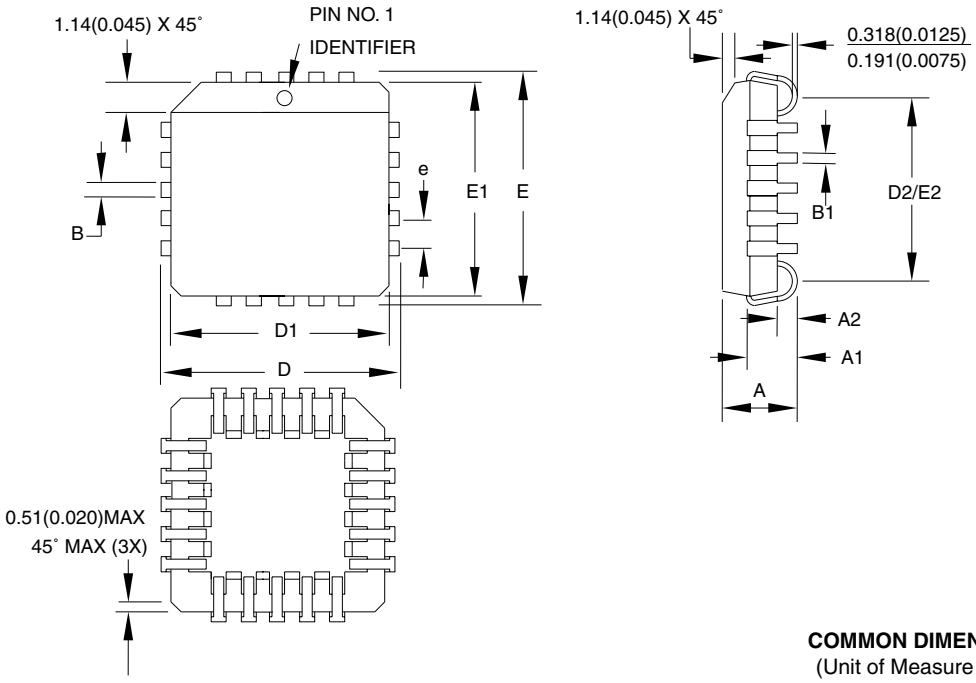
SYMBOL	MIN	NOM	MAX	NOTE
A	0.94	1.04	1.14	
A1	0.30	0.34	0.38	
b	0.45	0.50	0.55	1
D	5.89	5.99	6.09	
E	4.89	5.99	6.09	
e	1.27 BSC			
e1	1.10 REF			
L	0.95	1.00	1.05	1
L1	1.25	1.30	1.35	1

Note: 1. Metal Pad Dimensions.

11/14/01

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **8CN4**, 8-lead (6 x 6 x 1.04 mm Body), Lead Pitch 1.27 mm, Leadless Array Package (LAP)	**DRAWING NO.** 8CN4	**REV.** A

20J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

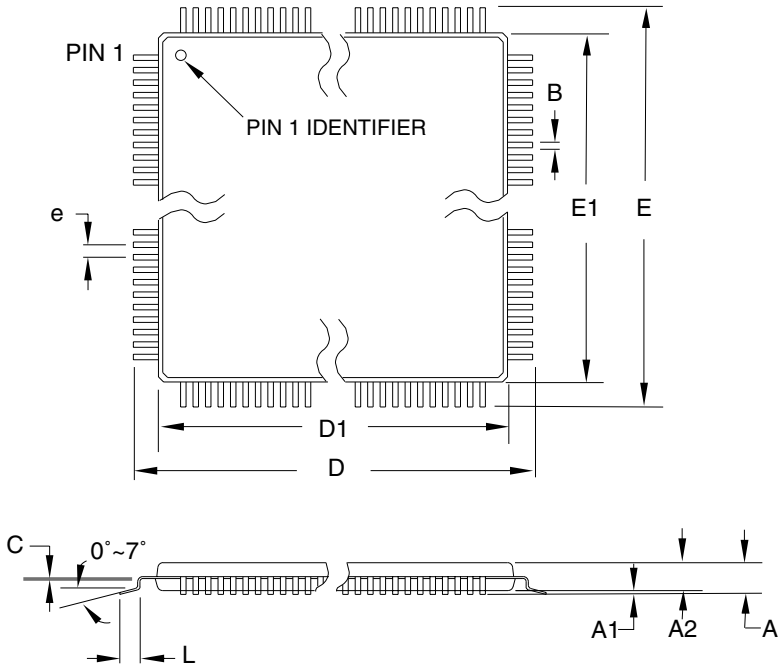
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

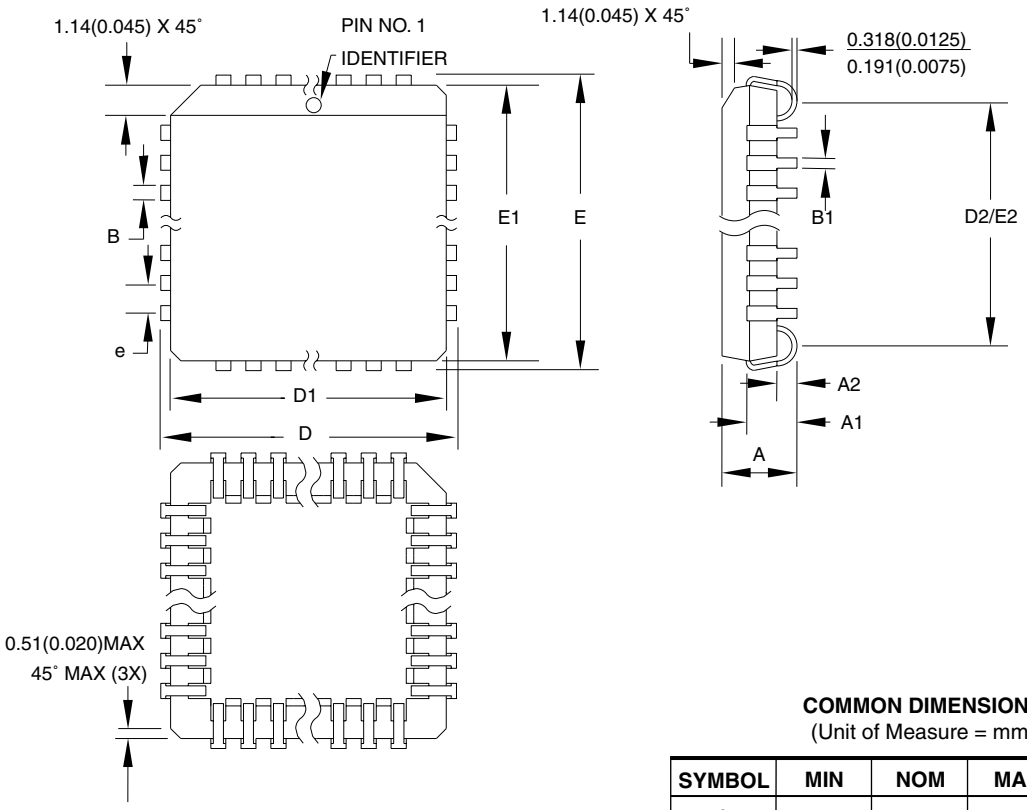
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
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