EPSON

SPC7212F0A

SCSI Controller IC

Preliminary

- Conforming to SCSI-2
- Synchronous/Asynchronous Transfer Mode Compatible
- SCAM Lv. 1

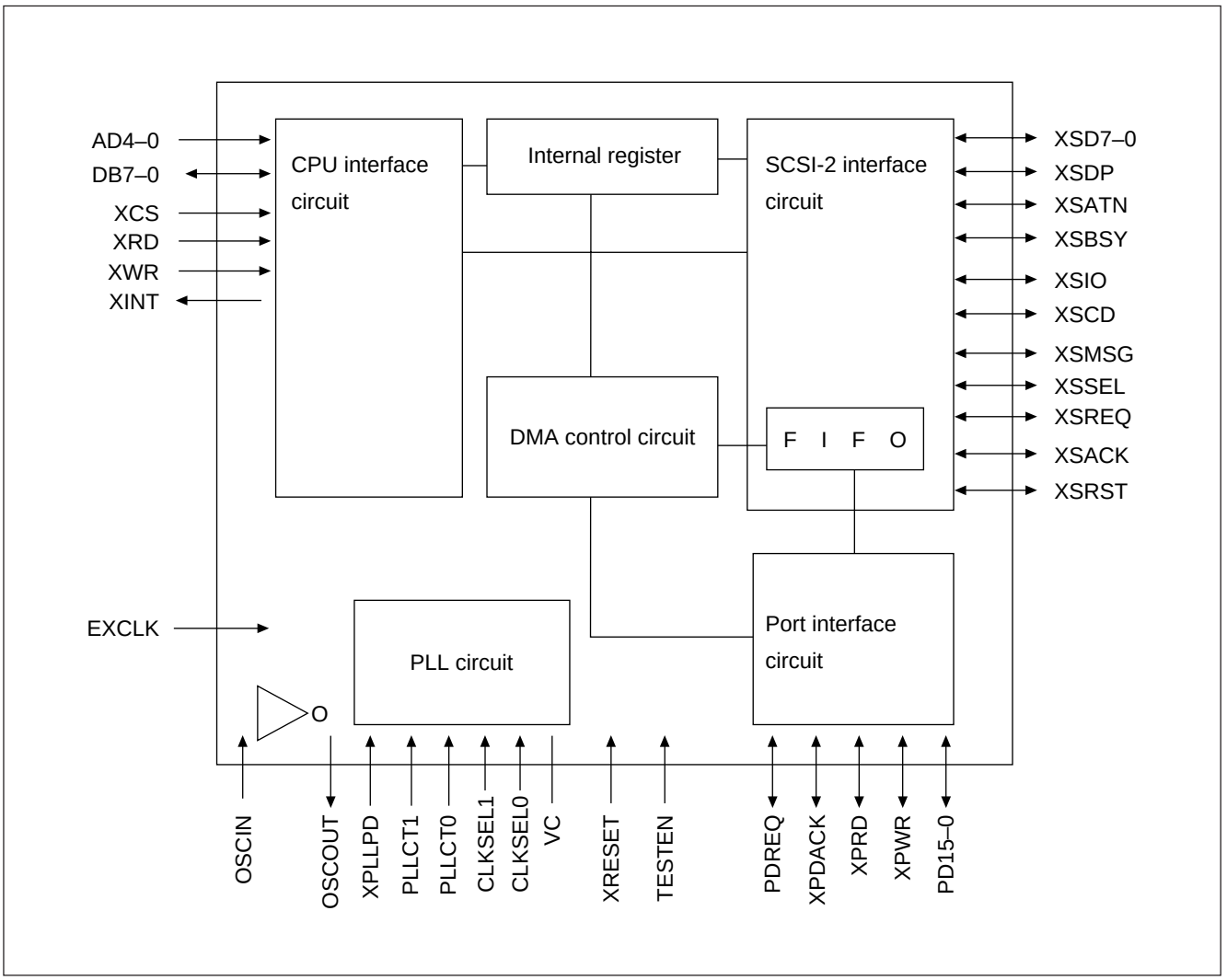
■ OVERVIEW

SPC7212F0A is the SCSI-2 interface control LSI for SCAM. It has an interface that can connect with a general CPU, PLL circuit that generates 40 MHz internal system clocks, and port interface circuit that transfers 8-bit/16-bit selectable external port data and outputs SCSI-2 data signals from the SCSI interface circuit.

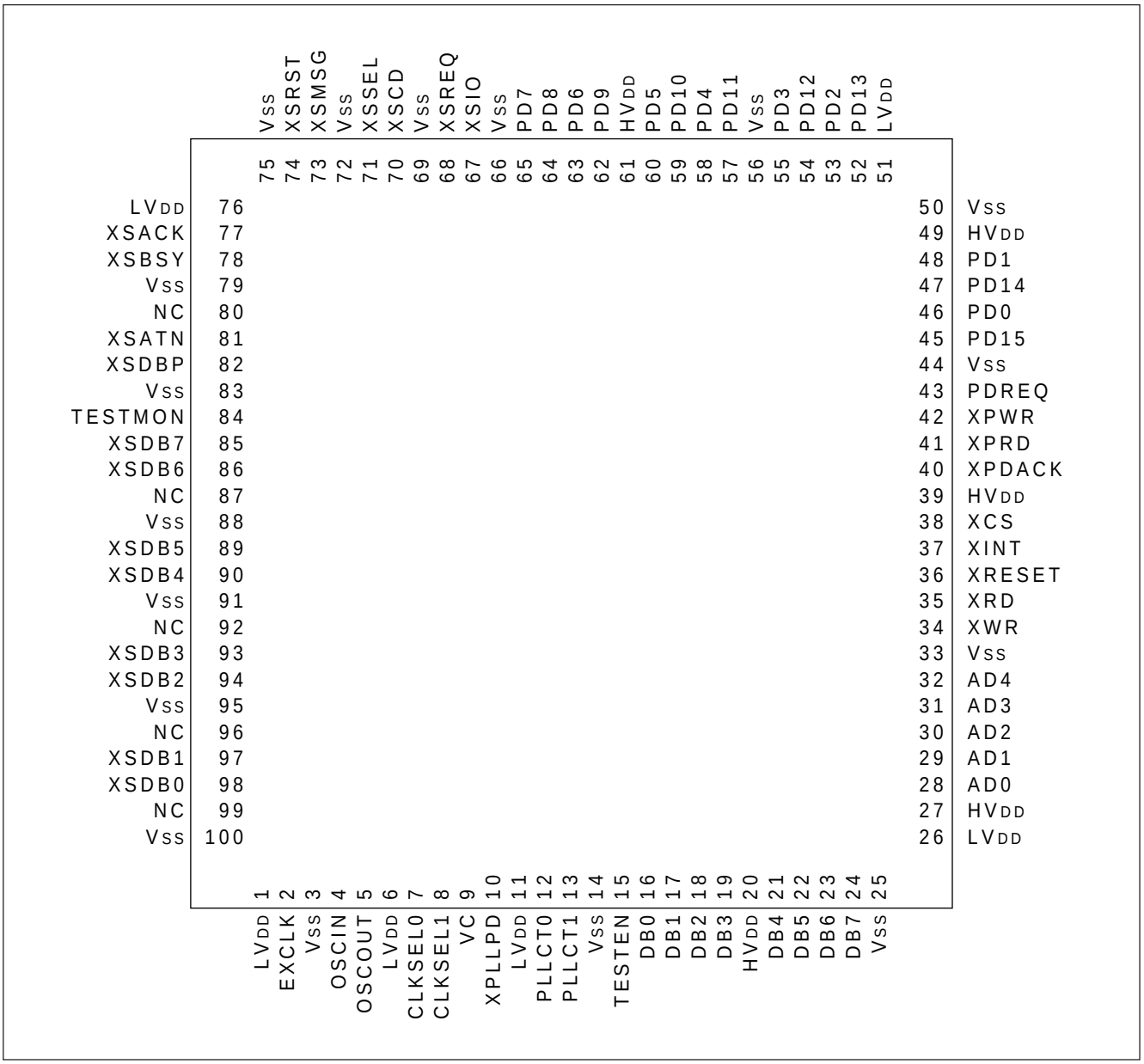
■ FEATURES

- Conforming to SCSI-2
- Synchronous/asynchronous transfer mode
  - Synchronous mode 10 MB/s
  - Asynchronous mode 5 MB/s
- Supporting SCAM Lv. 1
  - The firmware can support Lv. 2.
- Phase-controlled automatic processing function
- Built-in single-ended driver
- General CPU interface
- Built-in 20/22.5/40 MHz oscillation circuit
- Built-in PLL circuit
- 5/3.3 V power supply voltage
- QFP 15- to 100-pin package

■ BLOCK DIAGRAM



■ PIN ASSIGNMENT



■ PINS

The control signal that prefixes a pin name with “X” is low active.

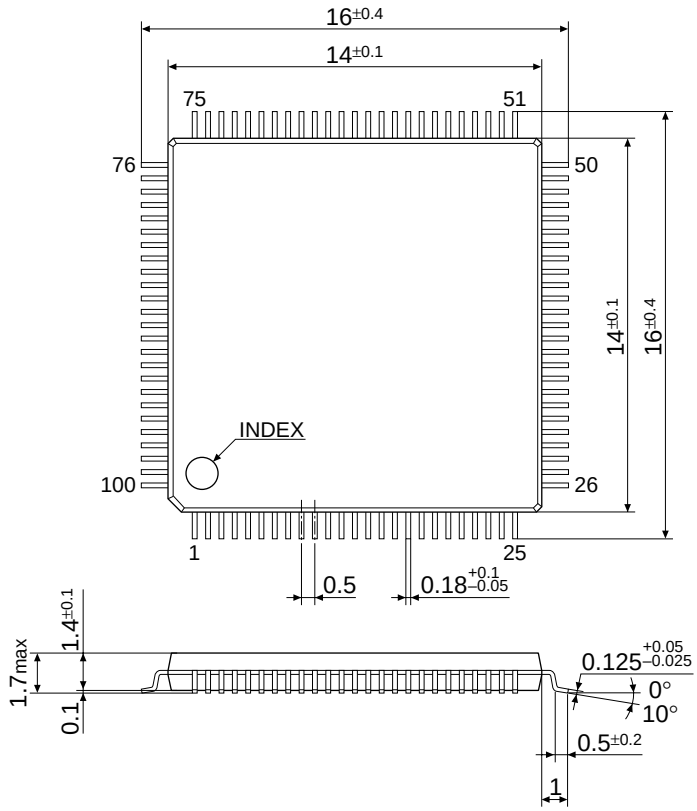
Pin number	Pin name	I/O	Function	Remarks
SCSI interfaces				
98	XSDB0	I/Ood	SCSI data signals (SD0 to SD7)	Drive performance 48mA
97	XSDB1			"
94	XSDB2			"
93	XSDB3			"
90	XSDB4			"
89	XSDB5			"
86	XSDB6			"
85	XSDB7			"
82	XSDBP		SCSI data parity signal	"
81	XSATN	I/Ood	SCSI ATN signal	"
78	XSBSY	I/Ood	SCSI BSY signal	"
77	XSACK	Is/Ood	SCSI ACK signal	"
74	XSRST	I/Ood	SCSI RST signal	"
73	XSMSG	I/Ood	SCSI MSG signal	"
71	XSSEL	I/Ood	SCSI SEL signal	"
70	XSCD	I/Ood	SCSI C/D signal	"
68	XSREQ	Is/Ood	SCSI REQ signal	"
67	XSIO	I/Ood	SCSI I/O signal	"
Port interfaces				
41	XPRD	Is/O	Port read signal	Drive performance 3mA
42	XPWR	Is/O	Port write signal	Drive performance 3mA
43	PDREQ	Is/O	Port DMA request signal (Negative logic operation is also enabled.)	Drive performance 6mA
40	XPDACK	Is/O	Port DMA acknowledge signal	Drive performance 3mA
46	PD0	I/O	Port DML data bus signals (PD0 to 15)	Drive performance 3mA
48	PD1			"
53	PD2			"
55	PD3			"
58	PD4			"
60	PD5			"
63	PD6			"
65	PD7			"
64	PD8		*PD8 to 15: Connect with Low(GND) when not used.	"
62	PD9			"
59	PD10			"
57	PD11			"
54	PD12			"
52	PD13			"
47	PD14			"
45	PD15			"

Pin number	Pin name	I/O	Function	Remarks
CPU Interface				
28	AD0	Ipu	Address input pins (AD0 to AD4)	
29	AD1			
30	AD2			
31	AD3			
32	AD4			
16	DB0	Ipu/O	Data pins (BD0 to BD7)	Drive performance 3mA
17	DB1			"
18	DB2			"
19	DB3			"
21	DB4			"
22	DB5			"
23	DB6			"
24	DB7			"
38	XCS	Ispu	Chip select signal for internal register access	
37	XINT	Otr	Interrupt request output signal	Drive performance 6mA
35	XRD	Ispu	Data read signal	
34	XWR	Ispu	Data write signal	
Others				
4	OSCIN	I	Built-in oscillation circuit input (40, 20, or 22.5 MHz)	
5	OSCOUT	O	Built-in oscillation circuit output	
84	TESTMON	O	Test monitor output (Usually: open "Low" output)	Drive performance 2mA
36	XRESET	Ipu	System reset input signal	
15	TESTEN	Ipd	Test pin (Usually connects with Low (GND).)	
7	CLKSEL0	I	Input clock selection Low(GND): OSCIN/Hi (LV_{DD}): EXCLK input	
8	CLKSEL1	I	System clock selection Low (GND): PLL output/Hi (LV_{DD}): CLKSEL0 selection signal	
12	PLLCT0	I	PLL operation control pin Depends on input clocks.	
13	PLLCT1	I	PLL operation control pin Depends on input clocks.	
2	EXCLK	I	5 V level external clock input pin (Connects with Low(GND) when not used.)	
10	XPLLPD	I	PLL power-down pin Low (GND): PLL power-down mode/Hi (LV_{DD}): PLL operation	
9	VC	0	Internal VC0 control pin	
80, 87, 92, 96, 99	NC	—	Does not connect with IC chips. (Usually: open)	
HV_{DD} : 5v (5)				
20, 27, 39, 49, 61	HV_{DD}	P	Power supply for 5 V interfaces	
LV_{DD} : 3.3V (6)				
1, 6, 11, 26, 51, 76	LV_{DD}	P	Power supply for internal operation	
V_{SS} : 0v (17)				
3, 14, 25, 33, 44, 50, 56, 66, 69, 72, 75, 79, 83, 88, 91, 95, 100	V_{SS}	P	GND	

(Note) I: Input
Is: Schmitt input
Ipu: Pull-up input
Ispu: Pull-up Schmitt input
Ipd: Pull-down input
O: Output
Ood: Open drain output
Otr: Tri-state output

■ PACKAGE DIMENSIONS

Plastic QFP15-100 pin



Unit:mm

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