

RL78/G1A

User's Manual: Hardware

16-Bit Single-Chip Microcontrollers

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

Readers

This manual is intended for user engineers who wish to understand the functions of the RL78/G1A and design and develop application systems and programs for these devices. The target products are as follows.

- 25-pin: R5F10E8x (x = A, C, D, E)
- 32-pin: R5F10EBx (x = A, C, D, E)
- 48-pin: R5F10EGx (x = A, C, D, E)
- 64-pin: R5F10ELx (x = C, D, E)

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The RL78/G1A manual is separated into two parts: this manual and the instructions edition (common to the RL78 Microcontroller).

RL78/G1A User's Manual (This Manual)	RL78 Microcontroller User's Manual Instructions

• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
 - Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.
- How to interpret the register format:
 - For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler.
- To know details of the RL78 Microcontroller instructions:
 - Refer to the separate document **RL78 Microcontroller Instructions User's Manual (R01US0015E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representations:	$\overline{\text{xxx}}$ (overscore over pin and signal name)
Note:	Footnote for item marked with Note in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representations:	Binary ...xxxx or xxxxB
	Decimal ...xxxx
	Hexadecimal ...xxxH

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
RL78/G1A User's Manual Hardware	This manual
RL78 Microcontroller Instructions User's Manual	R01US0015E

Documents Related to Flash Memory Programming

Document Name	Document No.
PG-FP5 Flash Memory Programmer User's Manual	R20UT0008E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Other Documents

Document Name	Document No.
RENESAS MICROCOMPUTER GENERAL CATALOG	R01CS0001E
Semiconductor Device Mount Manual	Note
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the "Semiconductor Device Mount Manual" website (<http://www.renesas.com/prod/package/manual/index.html>).

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CHAPTER 1 OUTLINE

1.1 Features

- Minimum instruction execution time can be changed from high speed (0.03125 μ s: @ 32 MHz operation with high-speed on-chip oscillator) to ultra low-speed (30.5 μ s: @ 32.768 kHz operation with subsystem clock)
- General-purpose register: 8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 banks)
- ROM: 16 to 64 KB, RAM: 2 to 4 KB, Data flash memory: 4 KB
- On-chip high-speed on-chip oscillator
 - Select from 32 MHz (TYP.), 24 MHz (TYP.), 16 MHz (TYP.), 12 MHz (TYP.), 8 MHz (TYP.), 4 MHz (TYP.), and 1 MHz (TYP.)
- On-chip single-power-supply flash memory (with prohibition of block erase/writing function)
- Self-programming (with boot swap function/flash shield window function)
- On-chip debug function
- On-chip power-on-reset (POR) circuit and voltage detector (LVD)
- On-chip watchdog timer (operable with the dedicated low-speed on-chip oscillator)
- On-chip multiplier and divider/multiply-accumulator
 - 16 bits $\times$ 16 bits = 32 bits (Unsigned or signed)
 - 32 bits $\div$ 32 bits = 32 bits (Unsigned)
 - 16 bits $\times$ 16 bits + 32 bits = 32 bits (Unsigned or signed)
- On-chip key interrupt function
- On-chip clock output/buzzer output controller
- On-chip BCD adjustment
- I/O ports: 19 to 56 (N-ch open drain: 2 to 4)
- Timer
 - 16-bit timer: 8 channels
 - Watchdog timer: 1 channel
 - Real-time clock: 1 channel (Correction clock output)
 - 12-bit interval timer: 1 channel
- Serial interface
 - CSI
 - UART/UART (LIN-bus supported)
 - I²C/Simplified I²C communication
- Different potential interface: Can connect to a 2.5 V device when operating at 3.0 V to 3.6 V
- 8/12-bit resolution A/D converter (V_{DD} , EV_{DD} , AV_{DD} = 1.6 to 3.6 V): 13 to 28 channels
- Standby function: HALT, STOP, SNOOZE mode
- Power supply voltage: V_{DD} = 1.6 to 3.6 V
- Operating ambient temperature: Consumer application T_A = -40 to +85°C,
Industrial application T_A = -40 to +105°C

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

O ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G1A			
			25 pins	32 pins	48 pins	64 pins
64 KB	4 KB	4 KB ^{Note}	R5F10E8E	R5F10EBE	R5F10EGE	R5F10ELE
48 KB	4 KB	3 KB	R5F10E8D	R5F10EBD	R5F10EGD	R5F10ELD
32 KB	4 KB	2 KB	R5F10E8C	R5F10EBC	R5F10EGC	R5F10ELC
16 KB	4 KB	2 KB	R5F10E8A	R5F10EBA	R5F10EGA	–

Note This is about 3 KB when the self-programming function and data flash function are used. (For details, see **CHAPTER 3**)

1.2 Ordering Information

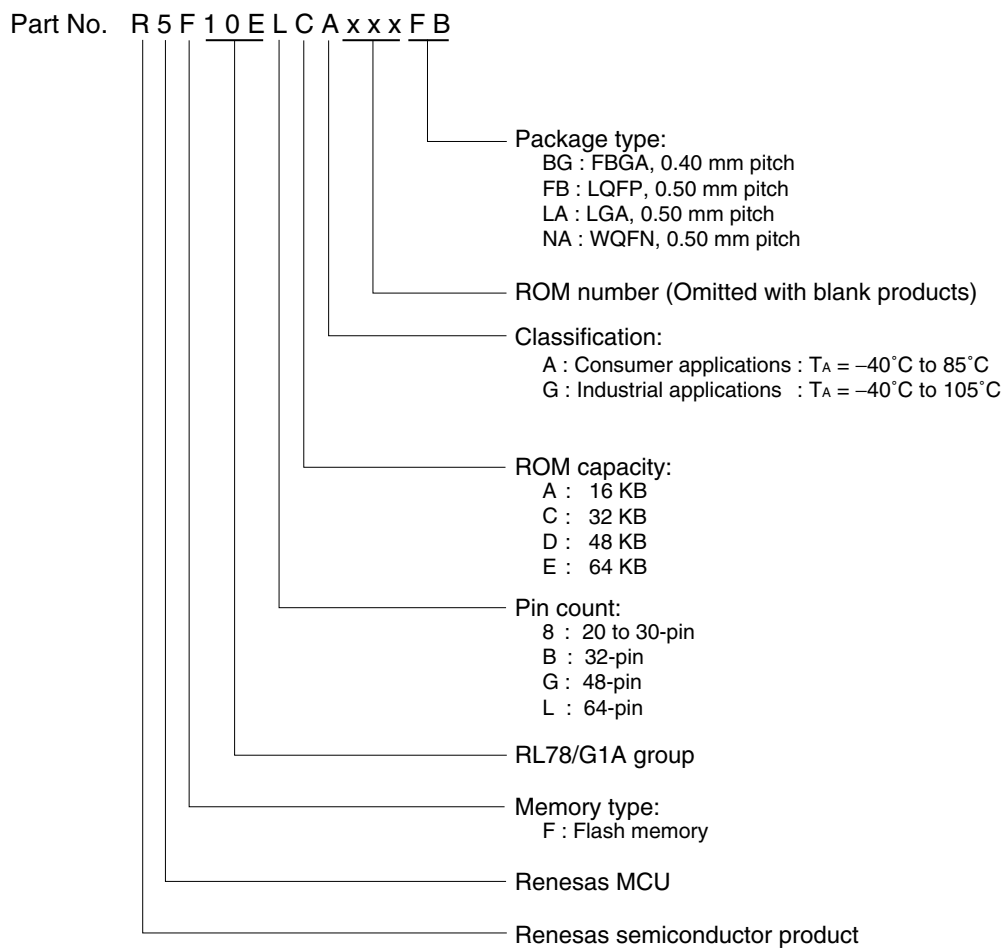
- Flash memory version (lead-free product)

<R>	Pin count	Package	Data flash	Classification	Part Number
	25 pins	25-pin plastic FLGA (3 × 3)	Mounted	Consumer application (to 85°C) ^{Note 1}	R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA,
				Industrial application (to 105°C) ^{Note 2}	R5F10E8AGLA, R5F10E8CGLA, R5F10E8DGLA, R5F10E8EGLA,
	32 pins	32-pin plastic WQFN (5 × 5)	Mounted	Consumer application (to 85°C) ^{Note 1}	R5F10EBAANA, R5F10EBCANA, R5F10EBDANA, R5F10EBEANA
				Industrial application (to 105°C) ^{Note 2}	R5F10EBAGNA, R5F10EBCGNA, R5F10EBDGNA, R5F10EBEGNA
	48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	Mounted	Consumer application (to 85°C) ^{Note 1}	R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB
				Industrial application (to 105°C) ^{Note 1}	R5F10EBAGNA, R5F10EBCGNA, R5F10EBDGNA, R5F10EBEGNA
		48-pin plastic WQFN (7 × 7)	Mounted	Consumer application (to 85°C) ^{Note 1}	R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA
				Industrial application (to 105°C) ^{Note 2}	R5F10EGAGNA, R5F10EGCGNA, R5F10EGDGNA, R5F10EGEGNA
	64 pins	64-pin plastic LQFP (fine pitch) (10 × 10)	Mounted	Consumer application (to 85°C) ^{Note 1}	R5F10ELCAFB, R5F10ELDADF, R5F10ELEAFB
				Industrial application (to 105°C) ^{Note 1}	R5F10ELCGFB, R5F10ELDGFB, R5F10ELEGFB
		64-pin plastic FBGA (4 × 4)	Mounted	Consumer application (to 85°C) ^{Note 1}	R5F10ELCABG, R5F10ELDABG, R5F10ELEABG,
				Industrial application (to 105°C) ^{Note 2}	R5F10ELCGBG, R5F10ELDGBG, R5F10ELEGBG,

Notes 1. In development

2. In planning

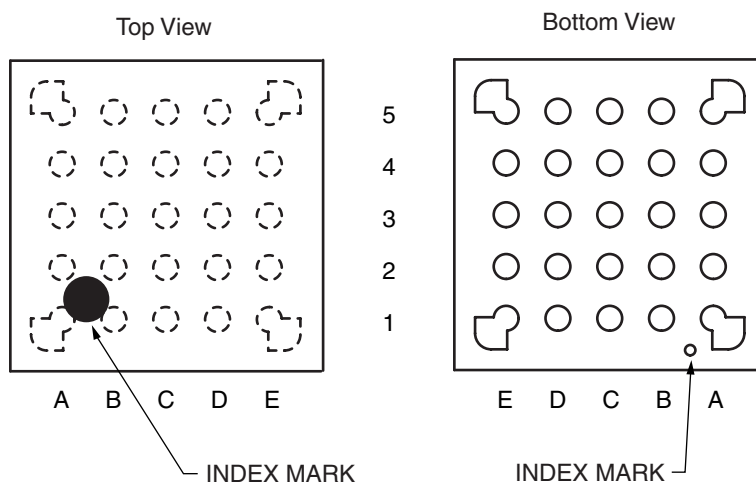
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Figure 1-1. Part Number, Memory Size, and Package of RL78/G1A

1.3 Pin Configuration (Top View)

1.3.1 25-pin products

- 25-pin plastic FLGA (3 × 3)



	A	B	C	D	E	
5	P40/TOOL0	RESET	P03/ANI16/ RxD1/TO00/ (KR1)	P23/ANI3/ (KR3)	AV _{SS}	5
4	P122/X2/ EXCLK	P137/INTP0	P02/ANI17/ TxD1/TI00/ (KR0)	P22/ANI2/ (KR2)	AV _{DD}	4
3	P121/X1	V _{DD}	P21/ANI1/ AV _{REFM}	P11/ANI20/ SI00/SDA00/ RxD0/ TOOLRxD	P10/ANI18/ SCK00/SCL00	3
2	REGC	V _{SS}	P30/ANI27/ SCK11/SCL11/ INTP3	P51/ANI25/ SO11/INTP2	P50/ANI26/ SI11/SDA11 INTP1	2
1	P60/SCLA0	P61/SDAA0	P31/ANI29/TI03/ TO03/PCLBUZ0 /INTP4	P12/ANI21/ SO00/TxD0/ TOOLTxD	P20/ANI0/ AV _{REFP}	1
	A	B	C	D	E	

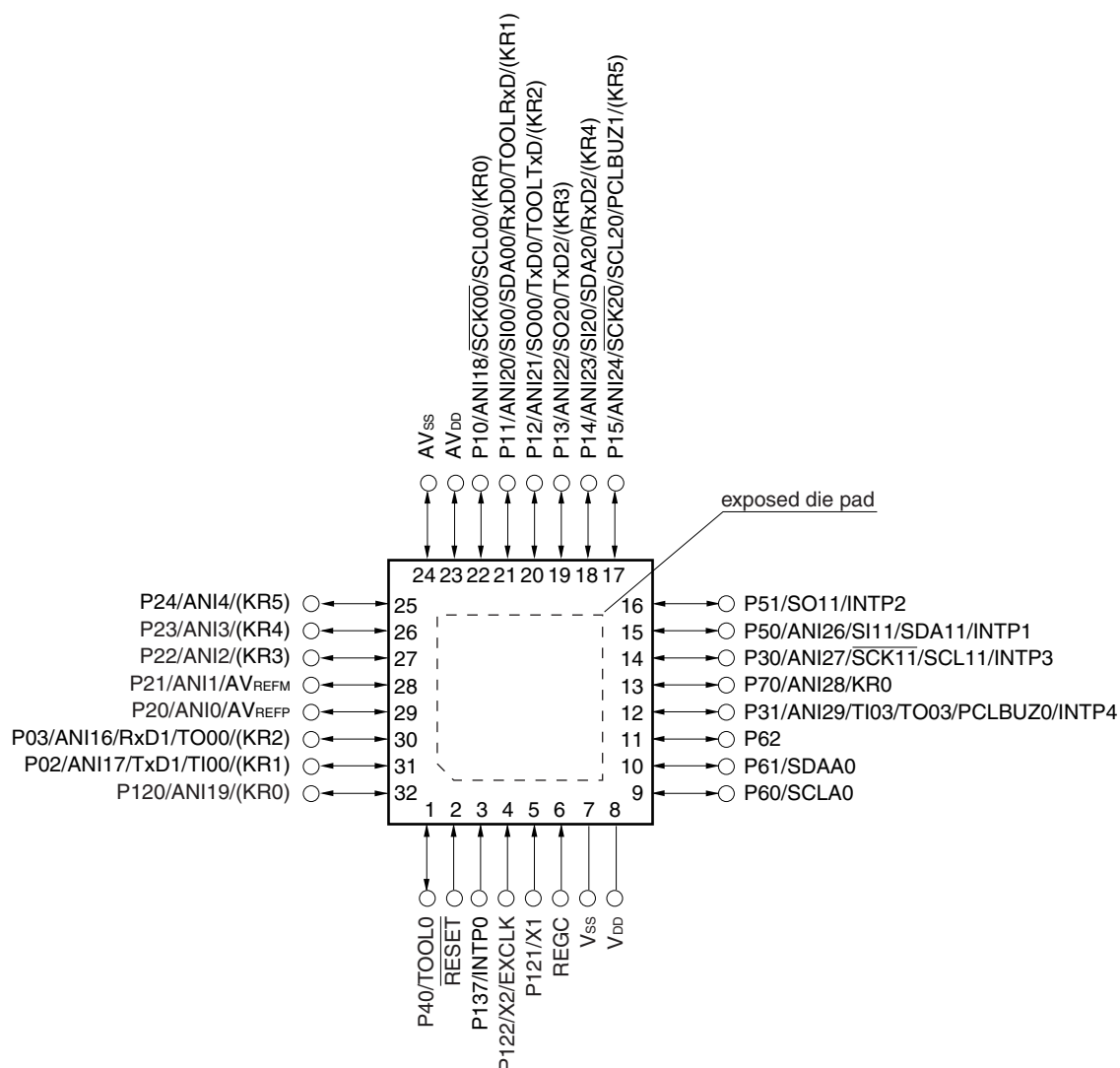
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 32-pin products

- 32-pin plastic WQFN (fine pitch) (5 × 5)



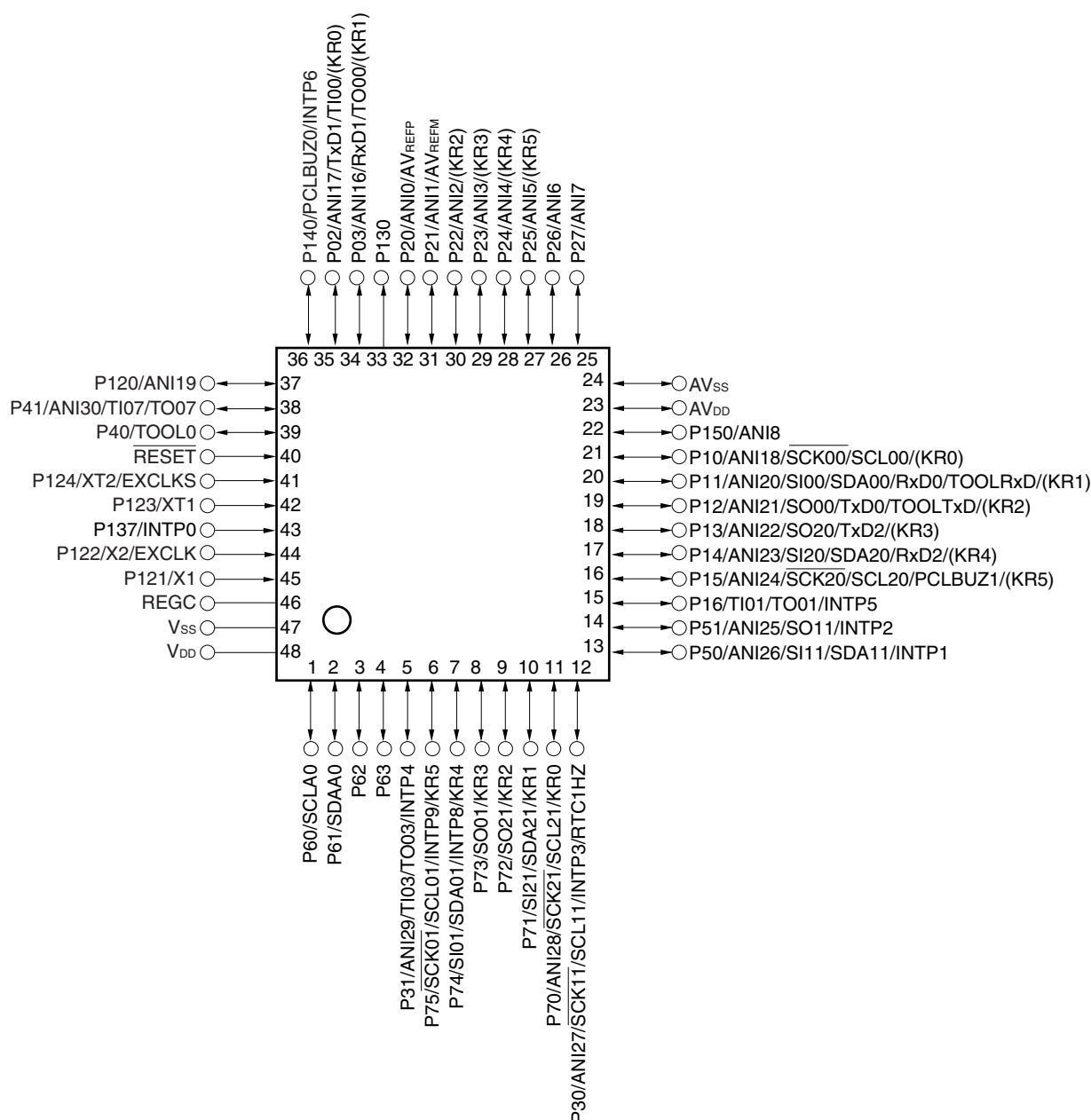
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.3 48-pin products

- 48-pin plastic LQFP (fine pitch) (7 × 7)

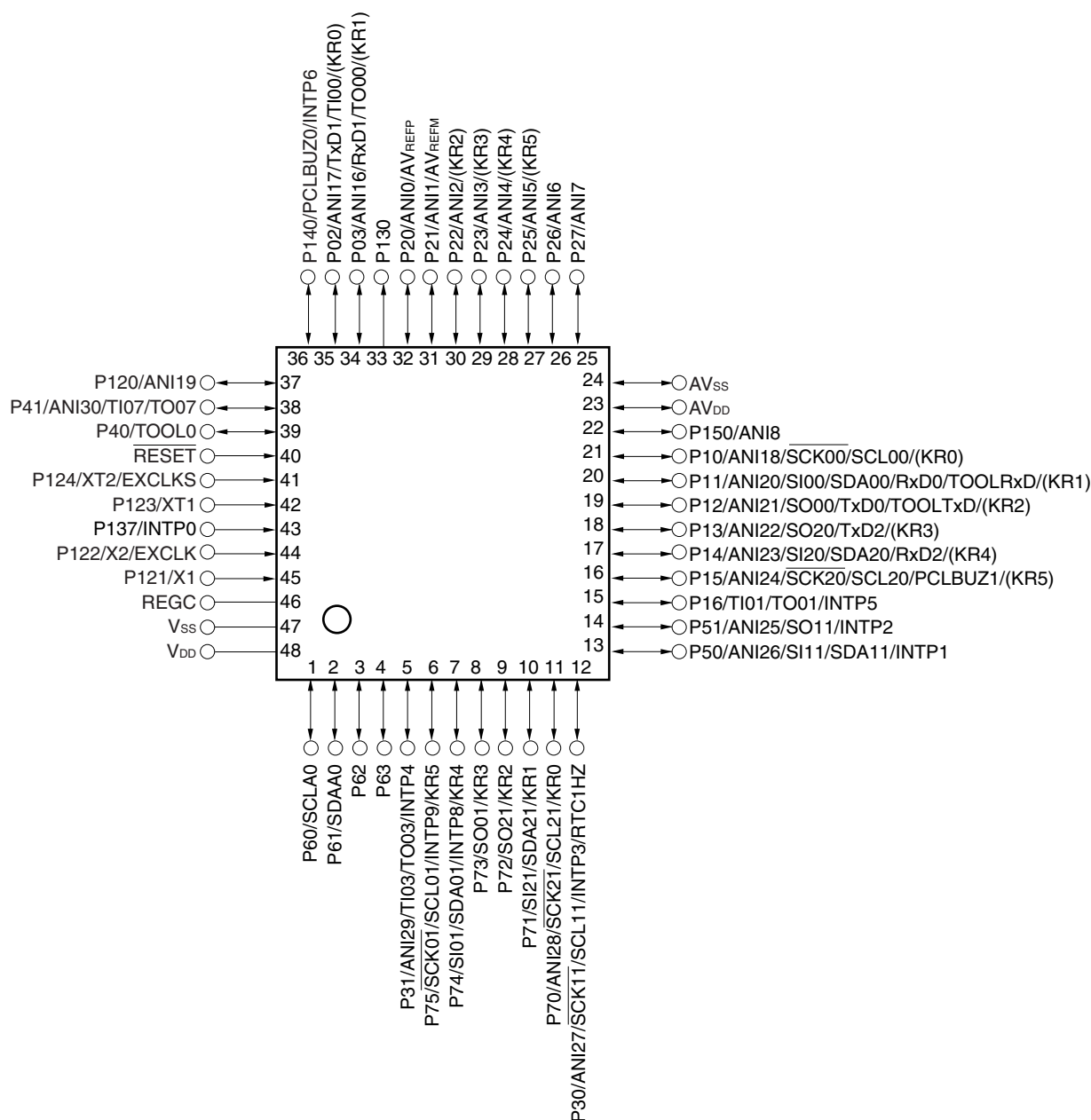


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 48-pin plastic WQFN (7 × 7)



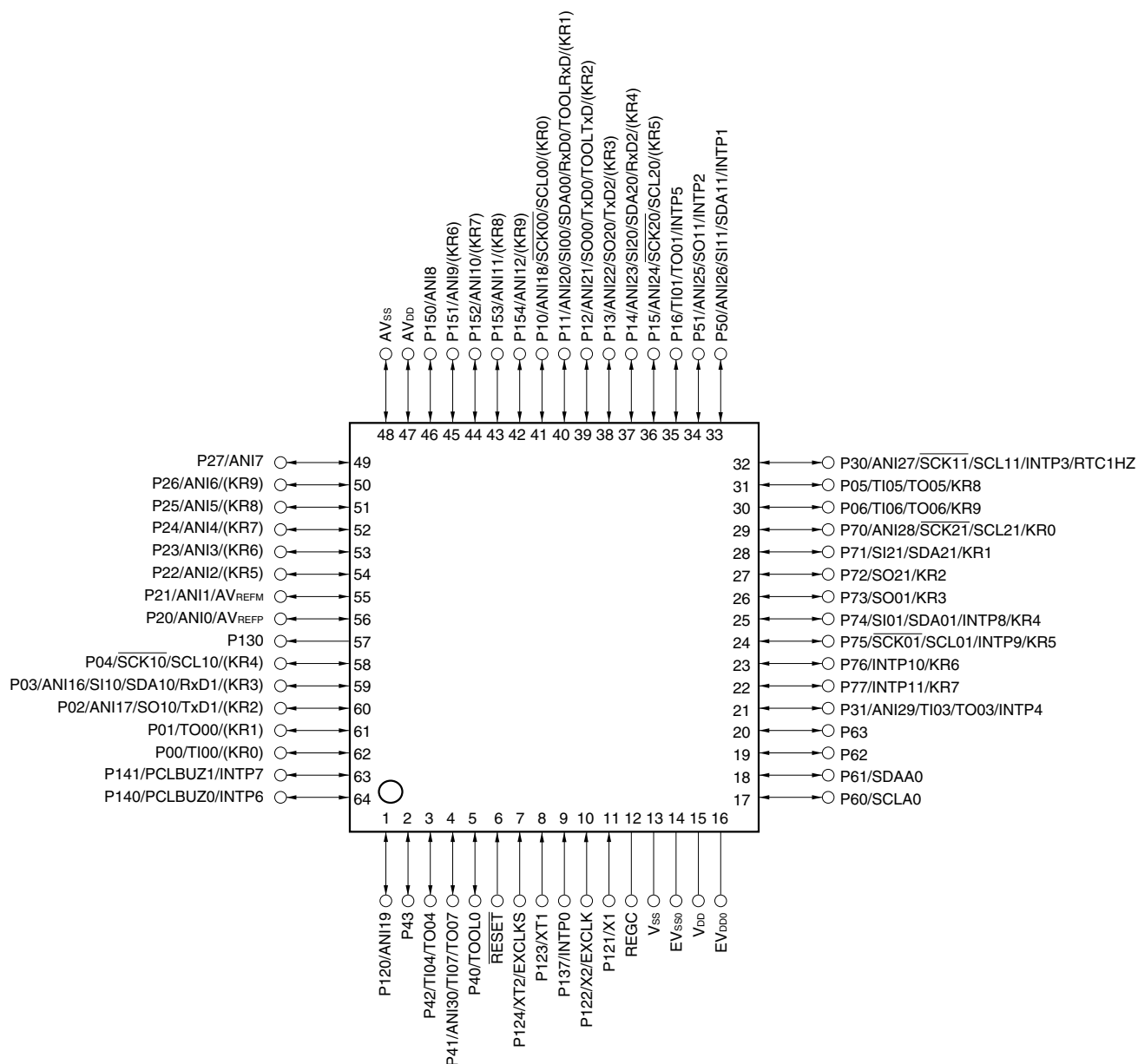
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.4 64-pin products

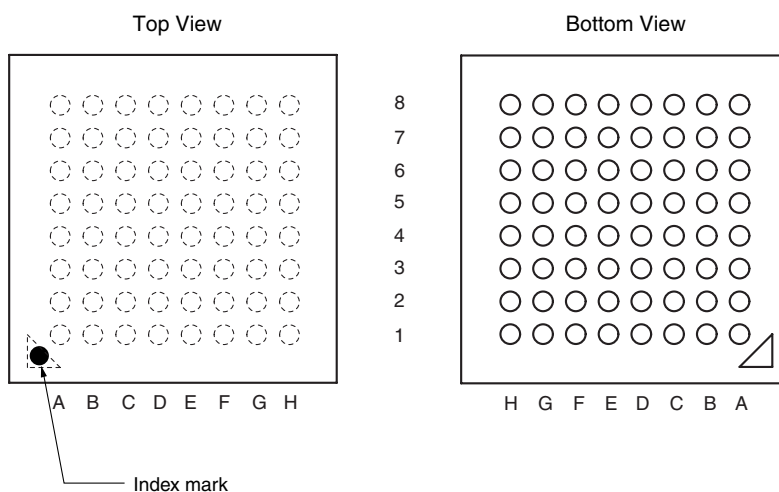
- 64-pin plastic LQFP (fine pitch) (10 × 10)



- Cautions 1.** Make EV_{SS0} pin the same potential as V_{SS} pin.
- 2.** Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
- 3.** Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

- Remarks 1.** For pin identification, see 1.4 Pin Identification.
- 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
- 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 64-pin plastic FBGA (4 × 4)



Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P05/TI05/TO05/KR8	C1	P51/ANI25/SO11/INTP2	E1	P153/ANI11/(KR8)	G1	AV _{DD}
A2	P30/ANI27/SCK11/SCL11/INTP3/RTC1HZ	C2	P71/SI21/SDA21/KR1	E2	P154/ANI12/(KR9)	G2	P25/ANI5/(KR8)
A3	P70/ANI28/SCK21/SCL21/KR0	C3	P74/SI01/SDA01/INTP8/KR4	E3	P10/ANI18/SCK00/SCL00/(KR0)	G3	P24/ANI4/(KR7)
A4	P75/SCK01/SCL01/INTP9/KR5	C4	P16/TI01/TO01/INTP5	E4	P11/ANI20/SI00/SDA00/RxD0/TOOLRxD/(KR1)	G4	P22/ANI2/(KR5)
A5	P77/INTP11/KR7	C5	P15/ANI24/SCK20/SCL20/(KR5)	E5	P03/ANI16/SI10/SDA10/RxD1/(KR3)	G5	P130
A6	P61/SDAA0	C6	P63	E6	P41/ANI30/TI07/TO07	G6	P02/ANI17/SO10/TxD1/(KR2)
A7	P60/SCLA0	C7	V _{SS}	E7	RESET	G7	P00/TI00/(KR0)
A8	EV _{DD0}	C8	P121/X1	E8	P137/INTP0	G8	P124/XT2/EXCLKS
B1	P50/ANI26/SI11/SDA11/INTP1	D1	P13/ANI22/SO20/TxD2/(KR3)	F1	P150/ANI8	H1	AV _{SS}
B2	P72/SO21/KR2	D2	P06/TI06/TO06/KR9	F2	P151/ANI9/(KR6)	H2	P27/ANI7
B3	P73/SO01/KR3	D3	P12/ANI21/SO00/TxD0/TOOLTxD/(KR2)	F3	P152/ANI10/(KR7)	H3	P26/ANI6/(KR9)
B4	P76/INTP10/KR6	D4	P14/ANI23/SI20/SDA20/RxD2/(KR4)	F4	P21/ANI1/AV _{REFM}	H4	P23/ANI3/(KR6)
B5	P31/ANI29/TI03/TO03/INTP4	D5	P42/TI04/TO04	F5	P04/SCK10/SCL10/(KR4)	H5	P20/ANI0/AV _{REFP}
B6	P62	D6	P40/TOOL0	F6	P43	H6	P141/PCLBUZ1/INTP7
B7	V _{DD}	D7	REGC	F7	P01/TO00/(KR1)	H7	P140/PCLBUZ0/INTP6
B8	EV _{SS0}	D8	P122/X2/EXCLK	F8	P123/XT1	H8	P120/ANI19

- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

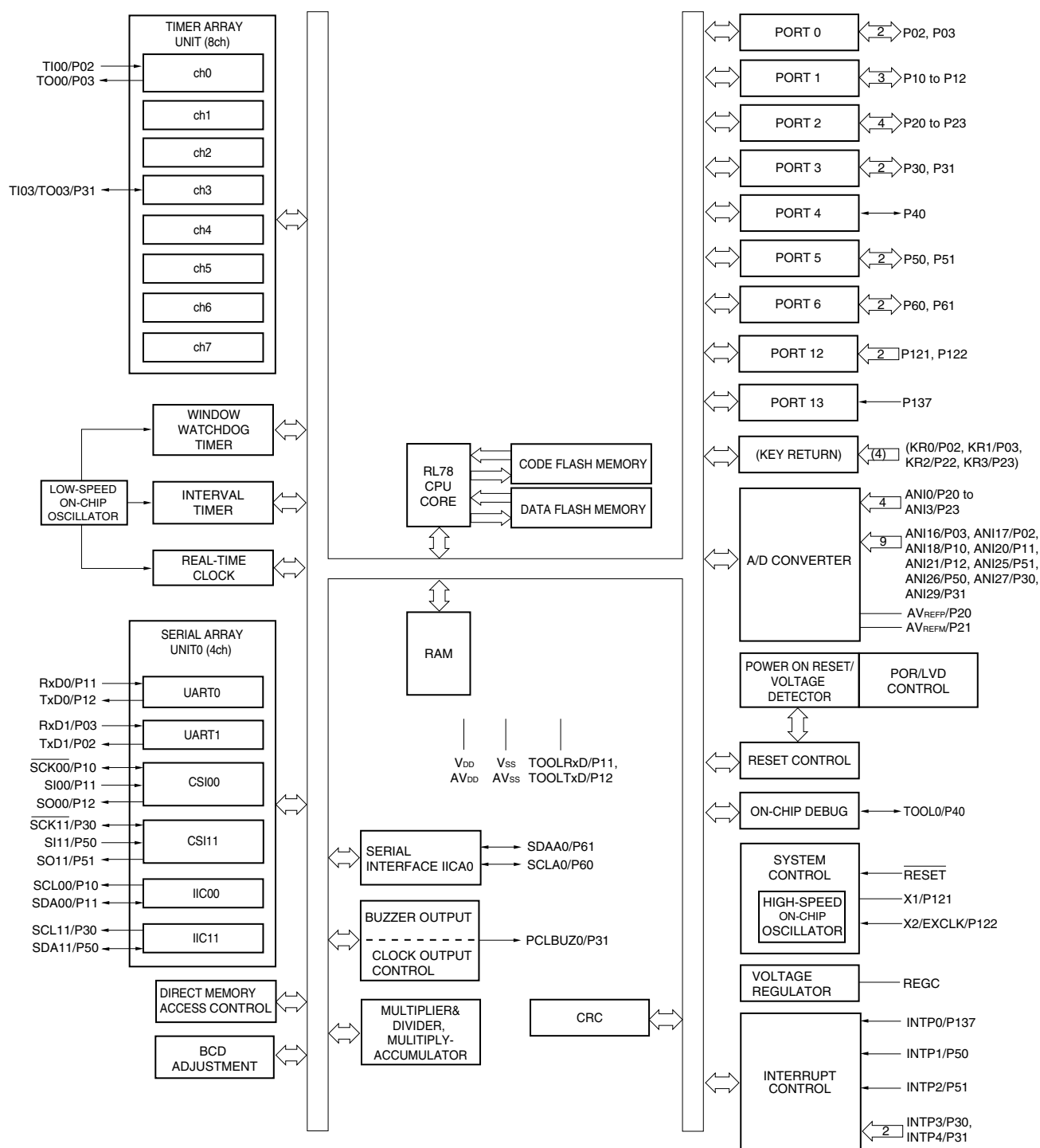
- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

ANI0 to ANI12,		PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output
ANI16 to ANI30:	Analog input	REGC:	Regulator capacitance
AV _{DD} :	Analog power supply	$\overline{\text{RESET}}$:	Reset
AV _{SS} :	Analog ground	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AV _{REFM} :	A/D converter reference potential (– side) input	RxD0 to RxD2:	Receive data
AV _{REFP} :	A/D converter reference potential (+ side) input	$\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK10}}$, $\overline{\text{SCK11}}$, $\overline{\text{SCK20}}$, $\overline{\text{SCK21}}$:	Serial clock input/output
EV _{DD0} :	Power supply for port	SCLA0, SCL00, SCL01, SCL10, SCL11, SCL20, SCL21:	Serial clock output
EV _{SS0} :	Ground for port	SDAA0, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21:	Serial data input/output
EXCLK:	External clock input (main system clock)	SI00, SI01, SI10, SI11, SI20, SI21:	Serial data input
EXCLKS:	External clock input (subsystem clock)	SO00, SO01, SO10, SO11, SO20, SO21:	Serial data output
INTP0 to INTP11:	External interrupt input	TI00, TI01, TI03 to TI07:	Timer input
KR0 to KR9:	Key return	TO00, TO01, TO03 to TO07:	Timer output
P00 to P06:	Port 0	TOOL0:	Data input/output for tool
P10 to P16:	Port 1	TOOLRxD, TOOLTxD:	Data input/output for external device
P20 to P27:	Port 2	TxD0 to TxD2:	Transmit data
P30, P31:	Port 3	V _{DD} :	Power supply
P40 to P43:	Port 4	V _{SS} :	Ground
P50, P51:	Port 5	X1, X2:	Crystal oscillator (main system clock)
P60 to P63:	Port 6	XT1, XT2:	Crystal oscillator (subsystem clock)
P70 to P77:	Port 7		
P120 to P124:	Port 12		
P130, P137:	Port 13		
P140, P141:	Port 14		
P150 to P154:	Port 15		

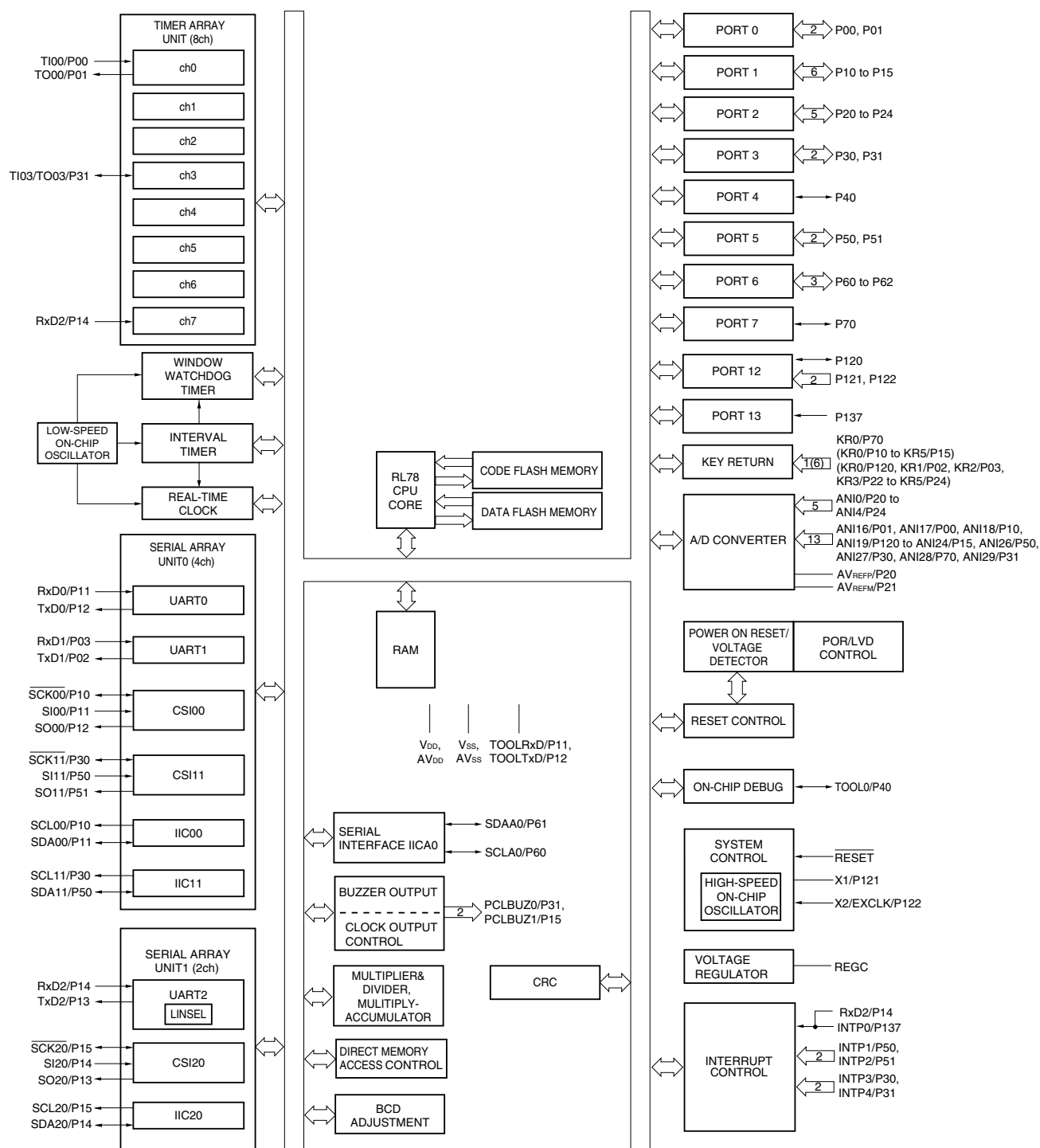
1.5 Block Diagram

<R> 1.5.1 25-pin products



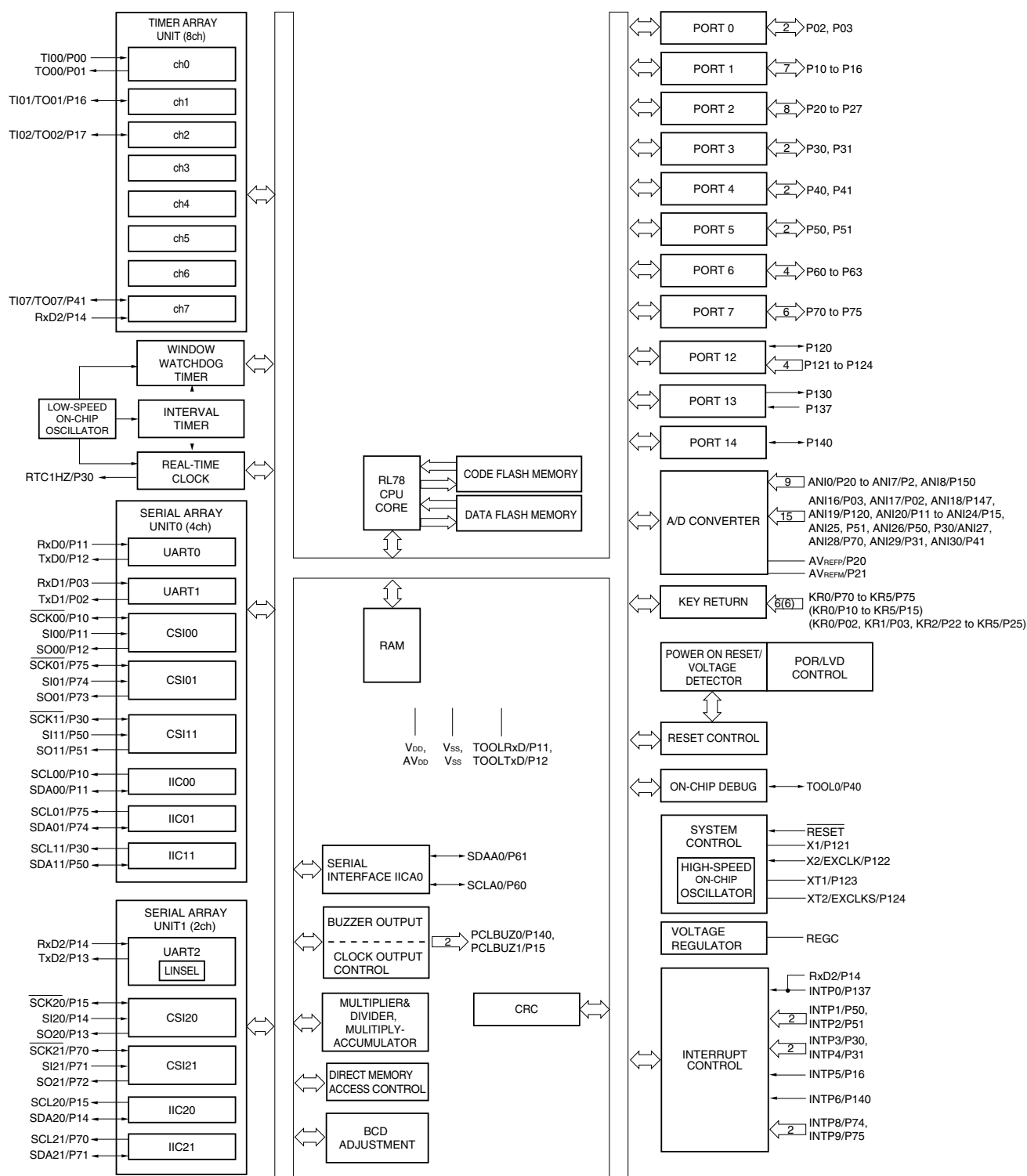
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> 1.5.2 32-pin products



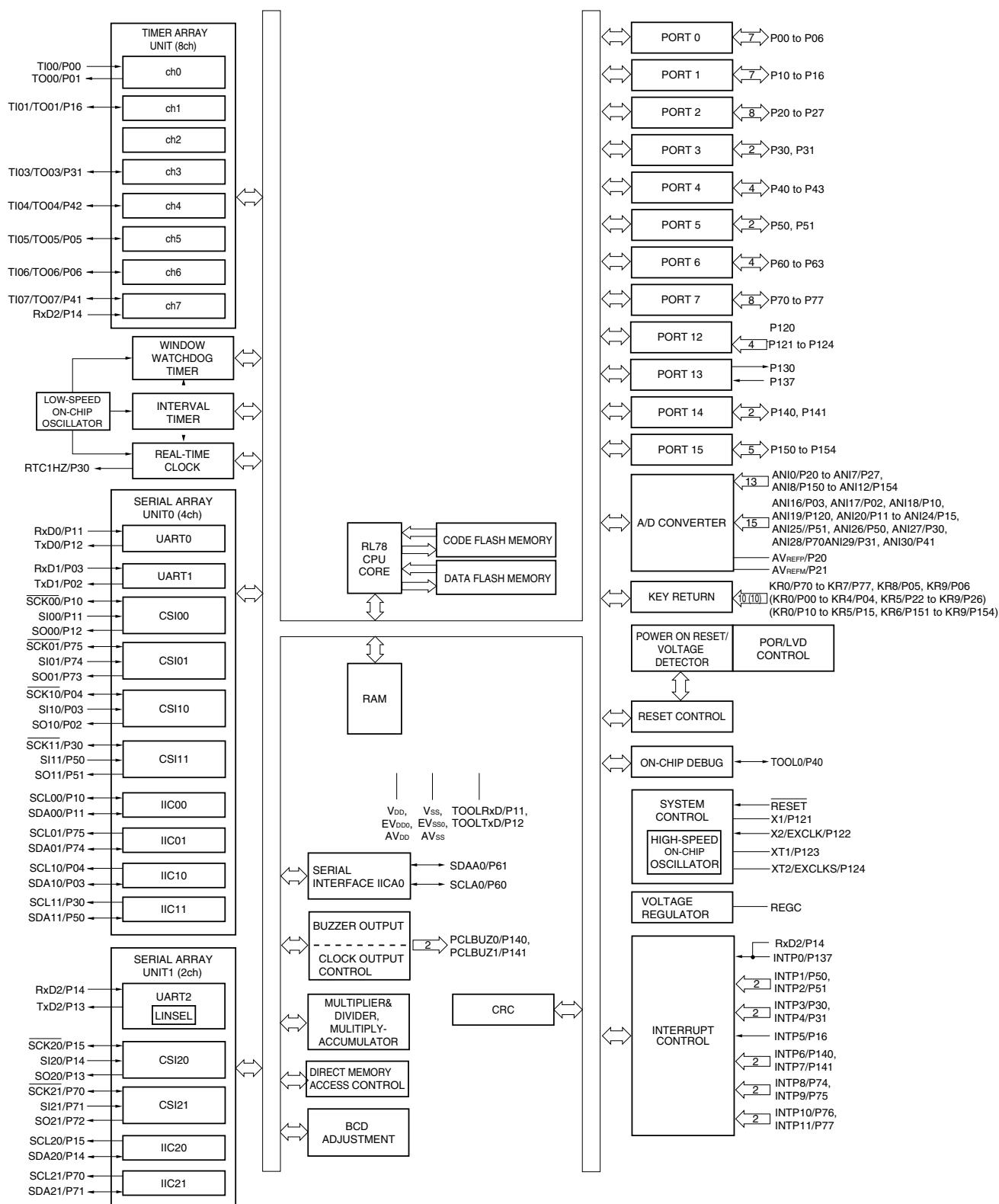
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> 1.5.3 48-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> 1.5.4 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.6 Outline of Functions

(1/2)

Item		25-pin	32-pin	48-pin	64-pin
		R5F10E8x	R5F10EBx	R5F10EGx	R5F10ELx
Code flash memory (KB)		16 to 64	16 to 64	16 to 64	32 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2 to 4 ^{Note1}	2 to 4 ^{Note1}	2 to 4 ^{Note1}	2 to 4 ^{Note1}
Memory space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V _{DD} = 2.7 to 3.6 V, 1 to 8 MHz: V _{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V _{DD} = 1.6 to 1.8 V			
	High-speed on-chip oscillator	HS (High-speed main) mode : 1 to 32 MHz (V _{DD} = 2.7 to 3.6 V), HS (High-speed main) mode : 1 to 16 MHz (V _{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode : 1 to 8 MHz (V _{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode : 1 to 4 MHz (V _{DD} = 1.6 to 3.6 V)			
Subsystem clock		–		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V _{DD} = 1.6 to 3.6 V	
Low-speed on-chip oscillator		15 kHz (TYP.): V _{DD} = 1.6 to 3.6 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		–		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	19	26	42	56
	CMOS I/O	14	20	32	46
	CMOS input	3	3	5	5
	CMOS output	–	–	1	1
	N-ch open-drain I/O (6 V tolerance)	2	3	4	4
Timer	16-bit timer	8 channels			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	–		1 channel	
	12-bit interval timer (IT)	1 channel			
	Timer output	2 channels (PWM outputs: 1 ^{Note2})		4 channels (PWM outputs: 3 ^{Note2})	7 channels (PWM outputs: 6 ^{Note2})
	RTC output	–		1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)	

- Notes**
- In the case of the 4 KB, this is about 3 KB when the self-programming function and data flash function are used. (For details, see **CHAPTER 3**)
 - The number of outputs varies, depending on the setting.

(2/2)

Item				
	25-pin R5F10E8x	32-pin R5F10EBx	48-pin R5F10EGx	64-pin R5F10ELx
Clock output/buzzer output	1	2	2	2
	2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{\text{MAIN}} = 20 \text{ MHz}$ operation)		2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{\text{MAIN}} = 20 \text{ MHz}$ operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{\text{SUB}} = 32.768 \text{ kHz}$ operation)	
8/12-bit resolution A/D converter	13 channels	18 channels	24 channels	28 channels
Serial interface	[25-pin products] - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel [32-pin products] - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel - CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel [48-pin products] - CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel - CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels [64-pin products] - CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels - CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels - CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels			
I ² C bus	1 channel	1 channel	1 channel	1 channel
Multiplier and divider/multiply-accumulator	16 bits $\times$ 16 bits = 32 bits (Unsigned or signed) 32 bits $\div$ 32 bits = 32 bits (Unsigned) 16 bits $\times$ 16 bits + 32 bits = 32 bits (Unsigned or signed)			
DMA controller	2 channels			
Vectored interrupt sources	Internal	24	27	27
	External	6	6	10
Key interrupt	0 ch (4 ch) ^{Note 1}	1 ch (6 ch) ^{Note 1}	6 ch	10 ch
Reset	- Reset by $\overline{\text{RESET}}$ pin - Internal reset by watchdog timer - Internal reset by power-on-reset - Internal reset by voltage detector - Internal reset by illegal instruction execution ^{Note 2} - Internal reset by RAM parity error - Internal reset by illegal-memory access			
Power-on-reset circuit	- Power-on-reset: TYP. 1.51 V - Power-down-reset: TYP. 1.50 V			
Voltage detector	- Rising edge : 1.67 V to 3.14 V (12 stages) - Falling edge : 1.63 V to 3.06 V (12 stages)			
On-chip debug function	Provided			
Power supply voltage	$V_{\text{DD}} = 1.6 \text{ to } 3.6 \text{ V}$			
Operating ambient temperature	A: Consumer application : $T_{\text{A}} = -40 \text{ to } +85^{\circ}\text{C}$, G: Industrial application : $T_{\text{A}} = -40 \text{ to } +105^{\circ}\text{C}$			

Notes 1. Can be used by the Peripheral I/O redirection register (PIOR).

2. The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

CHAPTER 2 PIN FUNCTIONS

2.1 Port Function

Pin I/O buffer power supplies depend on the product. The relationship between these power supplies and the pins is shown below.

<R>

Table 2-1. Pin I/O Buffer Power Supplies

(1) 25-pin products

Power Supply	Corresponding Pins
V _{DD}	Port pins other than P20 to P23 • $\overline{\text{RESET}}$, REGC
AV _{DD}	• P20 to P23

(2) 32-pin products

Power Supply	Corresponding Pins
V _{DD}	Port pins other than P20 to P24 • $\overline{\text{RESET}}$, REGC
AV _{DD}	• P20 to P24

(3) 48-pin products

Power Supply	Corresponding Pins
V _{DD}	Port pins other than P20 to P27, P150 • $\overline{\text{RESET}}$, REGC
AV _{DD}	• P20 to P27, P150

(4) 64-pin products

Power Supply	Corresponding Pins
EV _{DD0}	Port pins other than P20 to P27, P121 to P124, P137, and P150 to P154
V _{DD}	• P121 to P124, P137 • $\overline{\text{RESET}}$, REGC
AV _{DD}	• P20 to P27, and P150 to P154

2.1.1 25-pin products

Function Name	I/O	Function	After Reset	Alternate Function
P02	I/O	Port 0. 2-bit I/O port. Input of P03 can be set to TTL input buffer. Output of P02 and P03 can be set to N-ch open-drain output (V_{DD} tolerance). Can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Analog input port	ANI17/TI00/TxD1/(KR0)
P03				ANI16/TO00/RxD1/(KR1)
P10	I/O	Port 1. 3-bit I/O port. Input of P10 and P11 can be set to TTL input buffer. Output of P10 to P12 can be set to N-ch open-drain output (V_{DD} tolerance). Can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Input port	ANI18/SCK00/SCL00
P11				ANI20/SI00/RxD0/TOOLRxD/SDA00
P12				ANI21/SO00/TxD0/TOOLTxD
P20	I/O	Port 2. 4-bit I/O port. Can be set to analog input ^{Note 2} . Input/output can be specified in 1-bit units.	Analog input port	ANI0/AV _{REFP}
P21				ANI1/AV _{REFM}
P22				ANI2/(KR2)
P22				ANI3/(KR3)
P30	I/O	Port 3. 2-bit I/O port. Can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Analog input port	ANI27/INTP3/SCK11/SCL11
P31				ANI29/TI03/TO03/INTP4/PCLBUZ0
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P50	I/O	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (V_{DD} tolerance). Can be set to analog input ^{Note 1} . Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Analog input port	ANI26/INTP1/SI11/SDA11
P51				ANI25/INTP2/SO11
P60	I/O	Port 6. 2-bit I/O port. Output of P60 and P61 can be set to N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCLA0
P61				SDAA0
P121	Input	Port 12. 2-bit input port.	Input port	X1
P122				X2/EXCLK
P137	Input	Port 13. 1-bit output port and 1-bit input port.	Input port	INTP0

<R> **Notes 1.** Specify the each pin as either analog input or digital I/O in port mode control register X (PMCX) (This register can be specified in 1-bit unit).

<R> **2.** Specify the each pin as either analog input or digital I/O in A/D port configuration register (ADPC).

2.1.2 32-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P02	I/O	Port 0. 2-bit I/O port.	Analog input port	ANI17/TI00/TxD1/(KR1)
P03		Input of P03 can be set to TTL input buffer. Output of P02 and P03 can be set to N-ch open-drain output (V_{DD} tolerance). Can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.		ANI16/TO00/RxD1/(KR2)
P10	I/O	Port 1. 6-bit I/O port.	Analog input port	ANI18/SCK00/SCL00/(KR0)
P11		Input of P10, P11, P14, and P15 can be set to TTL input buffer.		ANI20/SI00/RxD0/TOOLRxD/SDA00/(KR1)
P12		Output of P10 to P15 can be set to N-ch open-drain output (V_{DD} tolerance).		ANI21/SO00/TxD0/TOOLTxD/(KR2)
P13		Can be set to analog input ^{Note 1} .		ANI22/TxD2/SO20/(KR3)
P14		Input/output can be specified in 1-bit units.		ANI23/RxD2/SI20/SDA20/(KR4)
P15		Use of an on-chip pull-up resistor can be specified by a software setting at input port.		ANI24/PCLBUZ1/SCK20/SCL20/(KR5)
P20	I/O	Port 2. 5-bit I/O port.	Analog input port	ANI0/AV _{REFP}
P21		Can be set to analog input ^{Note 2} .		ANI1/AV _{REFM}
P22		Input/output can be specified in 1-bit units.		ANI2/(KR3)
P23				ANI3/(KR4)
P24				ANI4/(KR5)
P30	I/O	Port 3. 2-bit I/O port.	Analog input port	ANI27/INTP3/SCK11/SCL11
P31		P30 and P31 can be set to analog input. Can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.		ANI29/TI03/TO03/INTP4/PCLBUZ0
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified ^{Note 1} . Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Input port	TOOL0

<R> **Notes 1.** Specify the each pin as either analog input or digital I/O in port mode control register X (PMCX) (This register can be specified in 1-bit unit).

<R> **2.** Specify the each pin as either analog input or digital I/O in A/D port configuration register (ADPC).

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2.1.3 48-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P02	I/O	Port 0. 2-bit I/O port. Input of P03 can be set to TTL input buffer. Output of P02 and P03 can be set to N-ch open-drain output (V_{DD} tolerance). Can be set to analog input. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port ^{Note 1} .	Analog input port	ANI17/TI00/TxD1/(KR0)
P03				ANI16/TO00/RxD1/(KR1)
P10	I/O	Port 1. 7-bit I/O port. Input of P10, P11, and P14 to P16 can be set to TTL input buffer. Output of P10 to P15 can be set to N-ch open-drain output (V_{DD} tolerance). P10 to P15 can be set to analog input. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port ^{Note 1} .	Analog input port	ANI18/SCK00/SCL00/(KR0)
P11				ANI20/SI00/RxD0/TOOLRxD/SDA00/(KR1)
P12				ANI21/SO00/TxD0/TOOLTxD/(KR2)
P13				ANI22/TxD2/SO20/(KR3)
P14				ANI23/RxD2/SI20/SDA20/(KR4)
P15				ANI24/PCLBUZ1/SCK20/SCL20/(KR5)
P16			Input port	TI01/TO01/INTP5
P20	I/O	Port 2. 8-bit I/O port. Can be set to analog input ^{Note 2} . Input/output can be specified in 1-bit units.	Analog input port	ANI0/AV _{REFP}
P21				ANI1/AV _{REFM}
P22				ANI2/(KR2)
P23				ANI3/(KR3)
P24				ANI4/(KR4)
P25				ANI5/(KR5)
P26				ANI6
P27				ANI7
P30	I/O	Port 3. 2-bit I/O port. Can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Analog input port	ANI27/INTP3/RTC1HZ/SCK11/SCL11
P31				ANI29/TI03/TO03/INTP4
P40	I/O	Port 4. 2-bit I/O port. P41 can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Input port	TOOL0
P41			Analog input port	ANI30/TI07/TO07

<R> **Notes 1.** Specify the each pin as either analog input or digital I/O in port mode control register X (PMCX) (This register can be specified in 1-bit unit).

<R> **2.** Specify the each pin as either analog input or digital I/O in A/D port configuration register (ADPC).

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2.1.4 64-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 7-bit I/O port. Input of P01, P03, and P04 can be set to TTL input buffer. Output of P02 to P04 can be set to N-ch open-drain output (V_{DD} tolerance). P02 and P03 can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Input port	TI00/(KR0)
P01				TO00/(KR1)
P02			Analog input port	ANI17/SO10/TxD1/(KR2)
P03				ANI16/SI10/RxD1/SDA10/(KR3)
P04			Input port	SCK10/SCL10/(KR4)
P05				TI05/TO05/KR8
P06				TI06/TO06/KR9
P10	I/O	Port 1. 7-bit I/O port. Input of P10, P11, and P14 to P16 can be set to TTL input buffer. Output of P10 to P15 can be set to N-ch open-drain output (V_{DD} tolerance). P10 to P15 can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Analog input port	ANI18/SCK00/SCL00/(KR0)
P11				ANI20/SI00/RxD0/TOOLRxD/SDA00/(KR1)
P12				ANI21/SO00/TxD0/TOOLTxD/(KR2)
P13				ANI22/TxD2/SO20/(KR3)
P14				ANI23/RxD2/SI20/SDA20/(KR4)
P15				ANI24/SCK20/SCL20/(KR5)
P16			Input port	TI01/TO01/INTP5
P20	I/O	Port 2. 8-bit I/O port. Can be set to analog input ^{Note 2} . Input/output can be specified in 1-bit units.	Analog input port	ANI0/AV _{REFP}
P21				ANI1/AV _{REFM}
P22				ANI2/(KR5)
P23				ANI3/(KR6)
P24				ANI4/(KR7)
P25				ANI5/(KR8)
P26				ANI6/(KR9)
P27				ANI7
P30	I/O	Port 3. 2-bit I/O port. Can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Analog input port	ANI27/INTP3/RTC1HZ/SCK11/SCL11
P31				ANI29/TI03/TO03/INTP4
P40	I/O	Port 4. 4-bit I/O port. P41 can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Input port	TOOL0
P41			Analog input port	ANI30/TI07/TO07
P42			Input port	TI04/TO04
P43				—

<R> **Notes 1.** Specify the each pin as either analog input or digital I/O in port mode control register X (PMCX) (This register can be specified in 1-bit unit).

<R> **2.** Specify the each pin as either analog input or digital I/O in A/D port configuration register (ADPC).

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P50	I/O	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (V _{DD} tolerance). Can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Analog input port	ANI26/INTP1/SI11/SDA11
P51				ANI25/INTP2/SO11
P60	I/O	Port 6. 4-bit I/O port. Output of P60 to P63 can be set to N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCLA0
P61				SDAA0
P62				—
P63				—
P70	I/O	Port 7. 8-bit I/O port. Output of P71 and P74 can be set to N-ch open-drain output (V _{DD} tolerance). P70 can be set to analog input ^{Note 1} . Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Analog input port	ANI28/KR0/SCK21/SCL21
P71			Input port	KR1/SI21/SDA21
P72				KR2/SO21
P73				KR3/SO01
P74				KR4/INTP8/SI01/SDA01
P75				KR5/INTP9/SCK01/SCL01
P76				KR6/INTP10
P77				KR7/INTP11
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. P120 can be set to analog input ^{Note 1} . For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port.	Analog input port	ANI19
P121	Input		Input port	X1
P122				X2/EXCLK
P123				XT1
P124				XT2/EXCLKS
P130	Output	Port 13. 1-bit output port and 1-bit input port.	Output port	—
P137	Input		Input port	INTP0
P140	I/O	Port 14. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.	Input port	PCLBUZ0/INTP6
P141				PCLBUZ1/INTP7
P150	I/O	Port 15. 5-bit I/O port. Can be set to analog input ^{Note 2} . Input/output can be specified in 1-bit units.	Analog input port	ANI8
P151				ANI9/(KR6)
P152				ANI10/(KR7)
P153				ANI11/(KR8)
P154				ANI12/(KR9)

<R> **Notes 1.** Specify the each pin as either analog input or digital I/O in port mode control register X (PMCX) (This register can be specified in 1-bit unit).

<R> **2.** Specify the each pin as either analog input or digital I/O in A/D port configuration register (ADPC).

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

<R> 2.2 Functions Other than Port Pins

2.2.1 With functions for each product

(1/4)

Function Name	64-pin	48-pin	32-pin	25-pin
ANI0	√	√	√	√
ANI1	√	√	√	√
ANI2	√	√	√	√
ANI3	√	√	√	√
ANI4	√	√	√	–
ANI5	√	√	–	–
ANI6	√	√	–	–
ANI7	√	√	–	–
ANI8	√	√	–	–
ANI9	√	–	–	–
ANI10	√	–	–	–
ANI11	√	–	–	–
ANI12	√	–	–	–
ANI16	√	√	√	√
ANI17	√	√	√	√
ANI18	√	√	√	√
ANI19	√	√	√	–
ANI20	√	√	√	√
ANI21	√	√	√	√
ANI22	√	√	√	–
ANI23	√	√	√	–
ANI24	√	√	√	–
ANI25	√	√	–	√
ANI26	√	√	√	√
ANI27	√	√	√	√
ANI28	√	√	√	–
ANI29	√	√	√	√
ANI30	√	√	–	–
INTP0	√	√	√	√
INTP1	√	√	√	√
INTP2	√	√	√	√
INTP3	√	√	√	√
INTP4	√	√	√	√
INTP5	√	√	–	–
INTP6	√	√	–	–
INTP7	√	–	–	–
INTP8	√	√	–	–
INTP9	√	√	–	–
INTP10	√	–	–	–
INTP11	√	–	–	–

(2/4)

Function Name	64-pin	48-pin	32-pin	25-pin
KR0	√	√	√	(√)
KR1	√	√	(√)	(√)
KR2	√	√	(√)	(√)
KR3	√	√	(√)	(√)
KR4	√	√	(√)	–
KR5	√	√	(√)	–
KR6	√	–	–	–
KR7	√	–	–	–
KR8	√	–	–	–
KR9	√	–	–	–
PCLBUZ0	√	√	√	√
PCLBUZ1	√	√	√	–
REGC	√	√	√	√
RTC1HZ	√	√	–	–
RESET	√	√	√	√
RxD0	√	√	√	√
RxD1	√	√	√	√
RxD2	√	√	√	–
SCK00	√	√	√	√
SCK01	√	√	–	–
SCK10	√	–	–	–
SCK11	√	√	√	√
SCK20	√	√	√	–
SCK21	√	√	–	–
SCLA0	√	√	√	√
SCL00	√	√	√	√
SCL01	√	√	–	–
SCL10	√	–	–	–
SCL11	√	√	√	√
SCL20	√	√	√	–
SCL21	√	√	–	–
SDAA0	√	√	√	√
SDA00	√	√	√	√
SDA01	√	√	–	–
SDA10	√	–	–	–
SDA11	√	√	√	√
SDA20	√	√	√	–
SDA21	√	√	–	–

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(3/4)

Function Name	64-pin	48-pin	32-pin	25-pin
SI00	√	√	√	√
SI01	√	√	—	—
SI10	√	—	—	—
SI11	√	√	√	√
SI20	√	√	√	—
SI21	√	√	—	—
SO00	√	√	√	√
SO01	√	√	—	—
SO10	√	—	—	—
SO11	√	√	√	√
SO20	√	√	√	—
SO21	√	√	—	—
TI01	√	√	—	—
TI03	√	√	√	√
TI04	√	—	—	—
TI05	√	—	—	—
TI06	√	—	—	—
TI07	√	√	—	—
TO00	√	√	√	√
TO01	√	√	—	—
TO03	√	√	√	√
TO04	√	—	—	—
TO05	√	—	—	—
TO06	√	—	—	—
TO07	√	√	—	—
TxD0	√	√	√	√
TxD1	√	√	√	√
TxD2	√	√	√	—
X1	√	√	√	√
X2	√	√	√	√
EXCLK	√	√	√	√
EXCLKS	√	√	—	—
TI00	√	√	√	√
XT1	√	√	—	—
XT2	√	√	—	—

(4/4)

Function Name	64-pin	48-pin	32-pin	25-pin
V _{DD}	√	√	√	√
EV _{DD0}	√	—	—	—
AV _{DD}	√	√	√	√
AV _{REFP}	√	√	√	√
AV _{REFM}	√	√	√	√
V _{SS}	√	√	√	√
EV _{SS0}	√	—	—	—
AV _{SS}	√	√	√	√
TOOLRxD	√	√	√	√
TOOLTxD	√	√	√	√
TOOL0	√	√	√	√

2.2.2 Pins for each product (pins other than port pins)

(1/2)

Function Name	I/O	Function
ANI0 to ANI12, ANI16 to ANI30	Input	A/D converter analog input (see Figure 11-46. Analog Input Pin Connection)
INTP0 to INTP11	Input	External interrupt request input The valid edge can be specified : Rising edge, falling edge, or both rising and falling edges)
KR0 to KR9	Input	Key interrupt input
PCLBUZ0, PCLBUZ1	Output	Clock output/buzzer output
REGC	–	Pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin at the shortest distance to V _{SS} via a capacitor (0.47 to 1 μ F). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.
RTC1HZ	Output	Real-time clock correction clock (1 Hz) output
$\overline{\text{RESET}}$	Input	This is the active-low system reset input pin. When the external reset pin is not used, connect this pin directly or via a resistor to V _{DD} .
RxD0 to RxD2	Input	Serial data input pins of serial interface UART0 to UART2
TxD0 to TxD2	Output	Serial data output pins of serial interface UART0 to UART2
$\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK10}}$, $\overline{\text{SCK11}}$, $\overline{\text{SCK20}}$, $\overline{\text{SCK21}}$	I/O	Serial clock I/O pins of serial interface CSI00, CSI01, CSI10, CSI11, CSI20, and CSI21
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21	Output	Serial clock output pins of serial interface IIC00, IIC01, IIC10, IIC11, IIC20, and IIC21
SDA00, SDA01, SDA10, SDA11, SDA20, SDA21	I/O	Serial data I/O pins of serial interface IIC00, IIC01, IIC10, IIC11, IIC20, and IIC21
SI00, SI01, SI10, SI11, SI20, SI21	Input	Serial data input pins of serial interface CSI00, CSI01, CSI10, CSI11, CSI20, and CSI21
SO00, SO01, SO10, SO11, SO20, SO21	Output	Serial data output pins of serial interface CSI00, CSI01, CSI10, CSI11, CSI20, and CSI21
SCLA0	I/O	Serial clock I/O pins of serial interface IICA
SDAA0	I/O	Serial data I/O pins of serial interface IICA
TI00 to TI07	Input	The pins for inputting an external count clock/capture trigger to 16-bit timers 00 to 07
TO00 to TO07	Output	Timer output pins of 16-bit timers 00 to 07
X1, X2	–	Resonator connection for main system clock
EXCLK	Input	External clock input for main system clock
XT1, XT2	–	Resonator connection for subsystem clock
EXCLKS	Input	External clock input for subsystem clock

(2/2)

Function Name	I/O	Function
V _{DD}	–	<25-pin, 32-pin 48-pin> Positive power supply for port pin other than P20 to P27, P150 and <u>RESET</u>, REGC pin. <64-pin > Positive power supply for P121 to P124, P137 and <u>RESET</u>, REGC pin.
EV _{DD0}	–	Positive power supply for ports (other than P20 to P27, P121 to P124, P137, P150 to P156)
AV _{DD}	–	Positive power supply for P20 to P27, P150 to P154, and A/D converter
AV _{REFP}	Input	A/D converter reference potential (+ side) input
AV _{REFM}	Input	A/D converter reference potential (– side) input Make AV _{REFM} pin the same potential as AV _{SS} and V _{SS} pin.
V _{SS}	–	<25-pin, 32-pin, 48-pin> Ground potential for port pin other than P20 to P27, P150 and <u>RESET</u>, REGC pin. <64-pin> Ground potential for P121 to P124, P137 and <u>RESET</u>, REGC pin.
EV _{SS0}	–	Ground potential for ports (other than P20 to P27, P121 to P124, P137, P150 to P154) Make EV _{SS0} pin the same potential as V _{SS} pin.
AV _{SS}	–	Ground potential for A/D converter, P20 to P27, and P150 to P154. Use this pin with the same potential as EV _{SS0} , and V _{SS} .
TOOLRxD	Input	UART reception pin for the external device connection used during flash memory programming
TOOLTxD	Output	UART transmission pin for the external device connection used during flash memory programming
TOOL0	I/O	Data I/O for flash memory programmer/debugger

Caution After reset release, the relationships between P40/TOOL0 and the operating mode are as follows.

Table 2-2. Relationships Between P40/TOOL0 and Operation Mode After Reset Release

P40/TOOL0	Operating mode
EV _{DD0}	Normal operation mode
0 V	Flash memory programming mode

For details, see 25.5 Programming Method.

Remark Use bypass capacitors (about 0.1 μ F) as noise and latch up countermeasures with relatively thick wires at the shortest distance to V_{DD} to V_{SS}, EV_{DD0} to EV_{SS0} lines.

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-3 shows the types of pin I/O circuits and the recommended connections of unused pins.

<R> **Remark** The pins mounted depend on the product. Refer to **1.3 Pin Configuration (Top View)** and **2.1 Port Function**.

Table 2-3. Connection of Unused Pins (64-pin products) (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI00/(KR0)	5-AN	I/O	Input: Independently connect to EV _{DD0} or EV _{SS0} via a resistor. Output: Leave open
P01/TO00/(KR1)			
P02/ANI17/SO10/TxD1/(KR2)	11-U		
P03/ANI16/SI10/RxD1/SDA10/(KR3)	11-V		
P04/ $\overline{\text{SCK10}}$ /SCL10/(KR4)	5-AN		
P05/TI05/TO05/KR8	8-R		
P06/TI06/TO06/KR9			
P10/ANI18/ $\overline{\text{SCK00}}$ /SCL00/(KR0)	11-V		
P11/ANI20/SI00/RxD0/TOOLRxD/SDA00/(KR1)			
P12/ANI21/SO00/TxD0/TOOLTxD/(KR2)	11-U		
P13/ANI22/TxD2/SO20/(KR3)			
P14/ANI23/RxD2/SI20/SDA20/(KR4)	11-V		
P15/ANI24/ $\overline{\text{SCK20}}$ /SCL20/(KR5)			
P16/TI01/TO01/INTP5	5-AN		
P20/ANI0/AV _{REFP}	11-T		Input: Independently connect to AV _{DD} or AV _{SS} via a resistor. Output: Leave open.
P21/ANI1/AV _{REFM}			
P22/ANI2/(KR5)	11-G		
P23/ANI3/(KR6)			
P24/ANI4/(KR7)			
P25/ANI5/(KR8)			
P26/ANI6/(KR9)			
P27/ANI7			
P30/ANI27/INTP3/RTC1HZ/ $\overline{\text{SCK11}}$ /SCL11	11-U		Input: Independently connect to EV _{DD0} or EV _{SS0} via a resistor. Output: Leave open.
P31/ANI29/TI03/TO03/INTP4			

Remarks 1. With products not provided with an EV_{DD0}, or EV_{SS0} pin, replace EV_{DD0} with V_{DD}, or replace EV_{SS0} with V_{SS}.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

Table 2-3. Connection of Unused Pins (64-pin products) (2/2)

	Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
<R>	P40/TOOL0	8-R	I/O	Input: Independently connect to EV _{DD0} or leave open. Output: Leave open.
	P41/ANI30/TI07/TO07	11-U		Input: Independently connect to EV _{DD0} or EV _{SS0} via a resistor. Output: Leave open.
	P42/TI04/TO04	8-R		
	P43			
	P50/ANI26/INTP1/SI11/SDA11	11-U		
	P51/ANI25/SO11/INTP2			
	P60/SCLA0	13-R		Input: Independently connect to EV _{DD0} or EV _{SS0} via a resistor. Output: Set the port's output latch to 0 and leave the pins open, or set the port's output latch to 1 and independently connect the pins to EV _{DD0} or EV _{SS0} via a resistor.
	P61/SDAA0			
	P62			
	P63			
	P70/ANI28/KR0/ $\overline{\text{SCK21}}$ /SCL21	11-U		Input: Independently connect to EV _{DD0} or EV _{SS0} via a resistor. Output: Leave open.
	P71/KR1/SI21/SDA21	8-R		
	P72/KR2/SO21			
	P73/KR3/SO01			
	P74/KR4/INTP8/SI01/SDA01			
	P75/KR5/INTP9/ $\overline{\text{SCK01}}$ /SCL01			
	P76/KR6/INTP10	5-AN		
	P77/KR7/INTP11	8-R		
	P120/ANI19	11-U		Input: Independently connect to EV _{DD0} or EV _{SS0} via a resistor. Output: Leave open.
	P121/X1	37-C	Input	
P122/X2/EXCLK				
P123/XT1				
P124/XT2/EXCLKS				
P130	3-C	Output	Leave open.	
P137/INTP0	2	Input	Independently connect to V _{DD} or V _{SS} via a resistor.	
P140/PCLBUZ0/INTP6	8-R	I/O	Input: Independently connect to EV _{DD0} or EV _{SS0} via a resistor. Output: Leave open.	
P141/PCLBUZ1/INTP7				
P150/ANI8	11-G	I/O	Input: Independently connect to AV _{DD} or AV _{SS} via a resistor. Output: Leave open.	
P151/ANI9/(KR6)				
P152/ANI10/(KR7)				
P153/ANI11/(KR8)				
P154/ANI12/(KR9)				
$\overline{\text{RESET}}$	2	Input	Connect directly or via a resistor to V _{DD} .	
REGC	—	—	Connect to V _{SS} via capacitor (0.47 to 1 μF).	

Remark With products not provided with an EV_{DD0}, or EV_{SS0} pin, replace EV_{DD0} with V_{DD}, or replace EV_{SS0} with V_{SS}.

Figure 2-1. Pin I/O Circuit List (1/2)

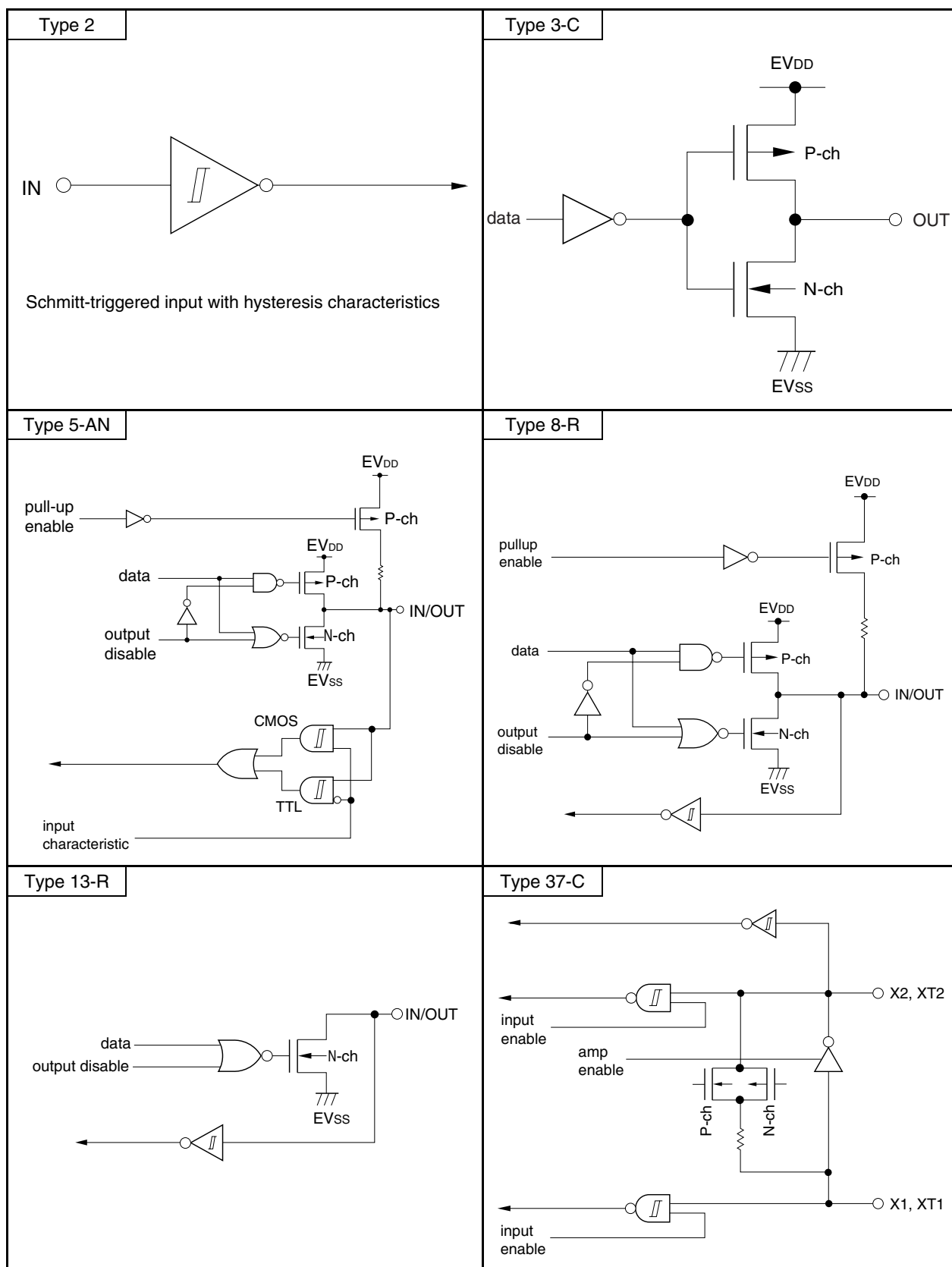
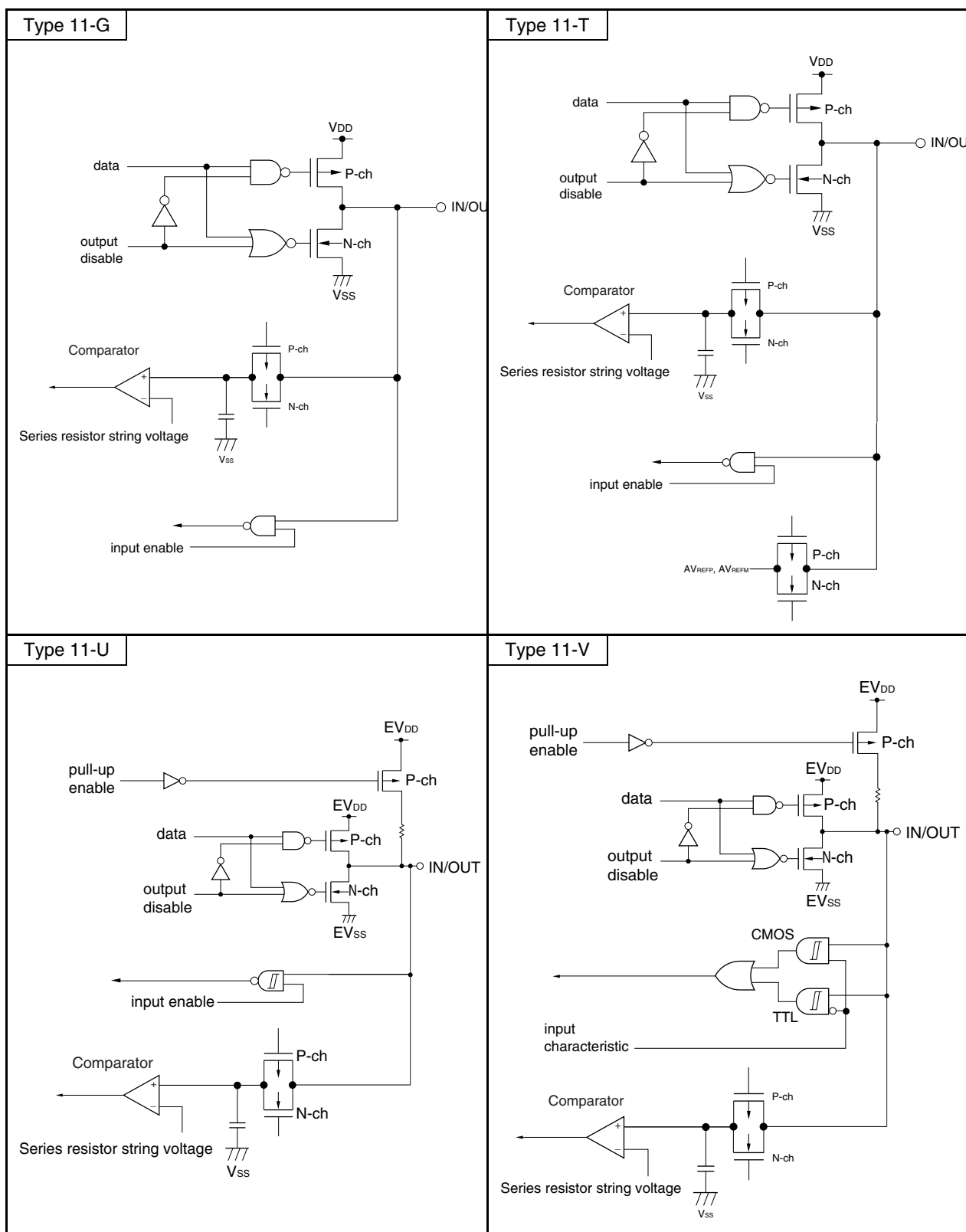


Figure 2-1. Pin I/O Circuit List (2/2)

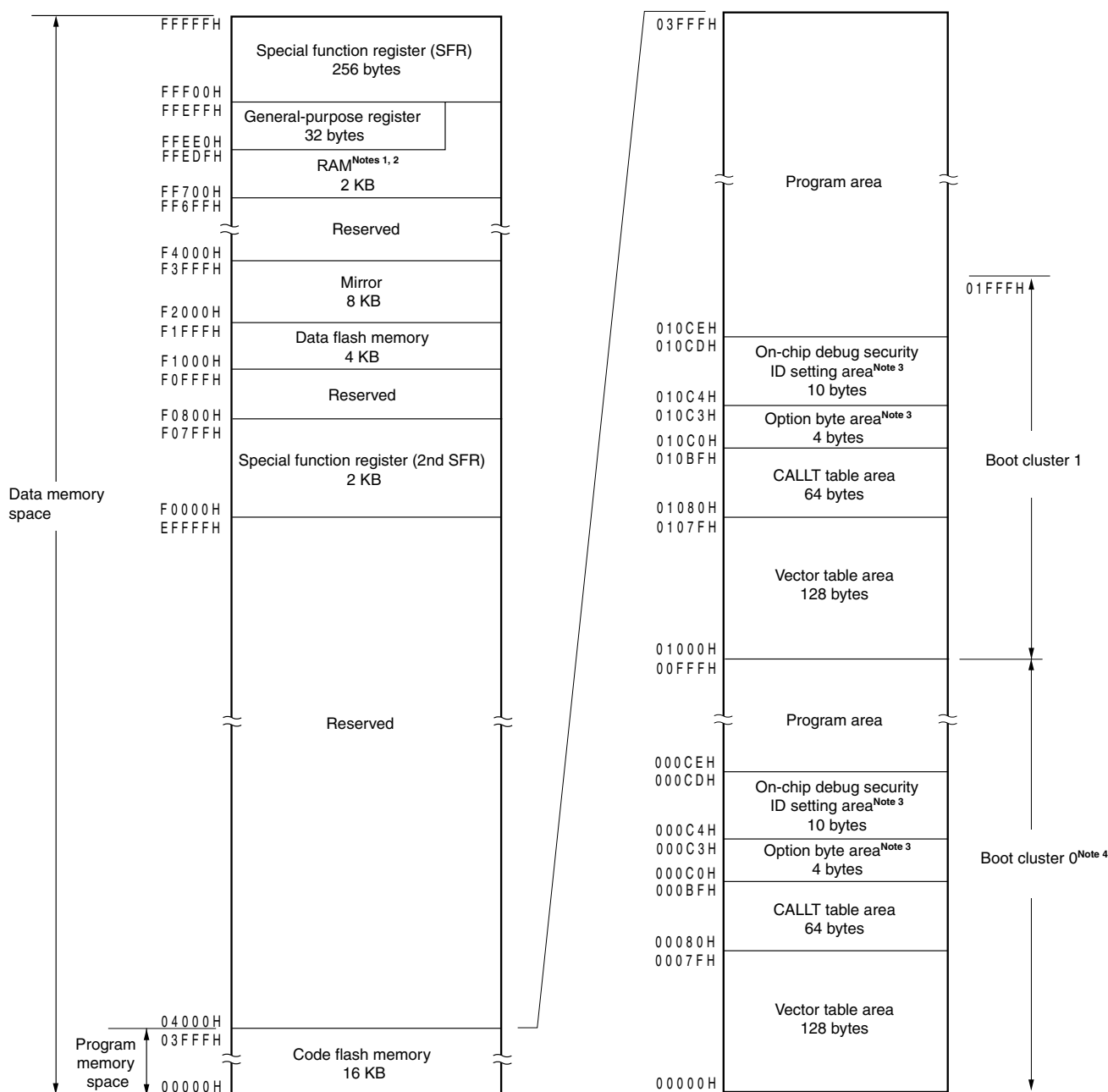


CHAPTER 3 CPU ARCHITECTURE

3.1 Memory Space

Products in the RL78/G1A can access a 1 MB memory space. Figures 3-1 to 3-4 show the memory maps.

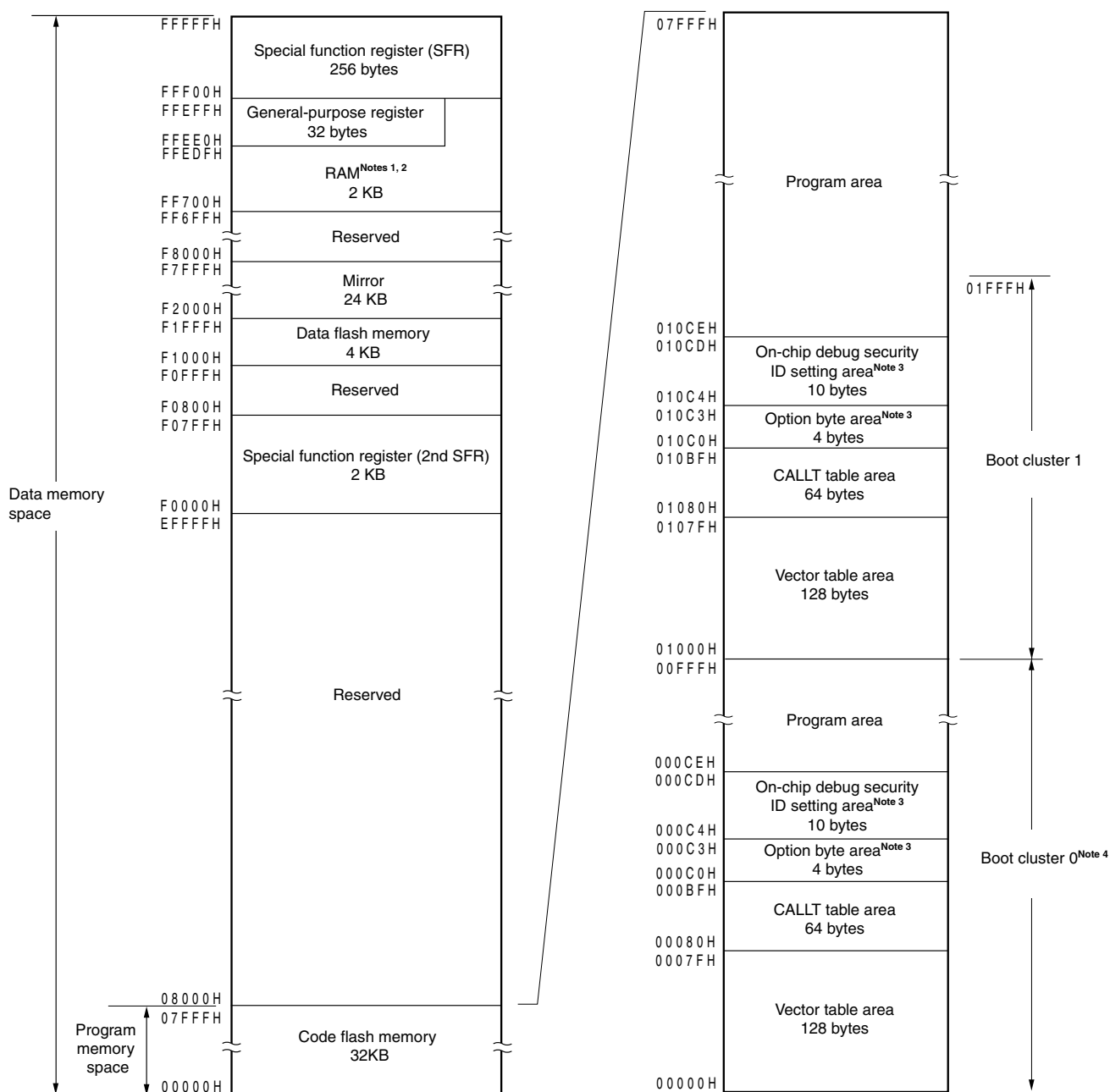
Figure 3-1. Memory Map (R5F10ExA (x = 8, B, G))



- <R> **Notes**
1. Use of the area FFE20H to FFEDFH is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.
 2. Instructions can be executed from the RAM area excluding the general-purpose register area.
 3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.
 4. Writing boot cluster 0 can be prohibited depending on the setting of security (see 25.6 Security Setting).

<R> **Caution** When a reset occurs, use RAM parity error reset generation enabled (RPERDIS = 0). If RAM parity error resets to use are enabled (RPERDIS = 0), be sure to initialize the RAM area whose data is to be accessed and the RAM area from which to execute instructions + 10 bytes. Reset signal generation enable RAM parity error reset generation. For detail, refer to 22.3.3 RAM parity error detection function.

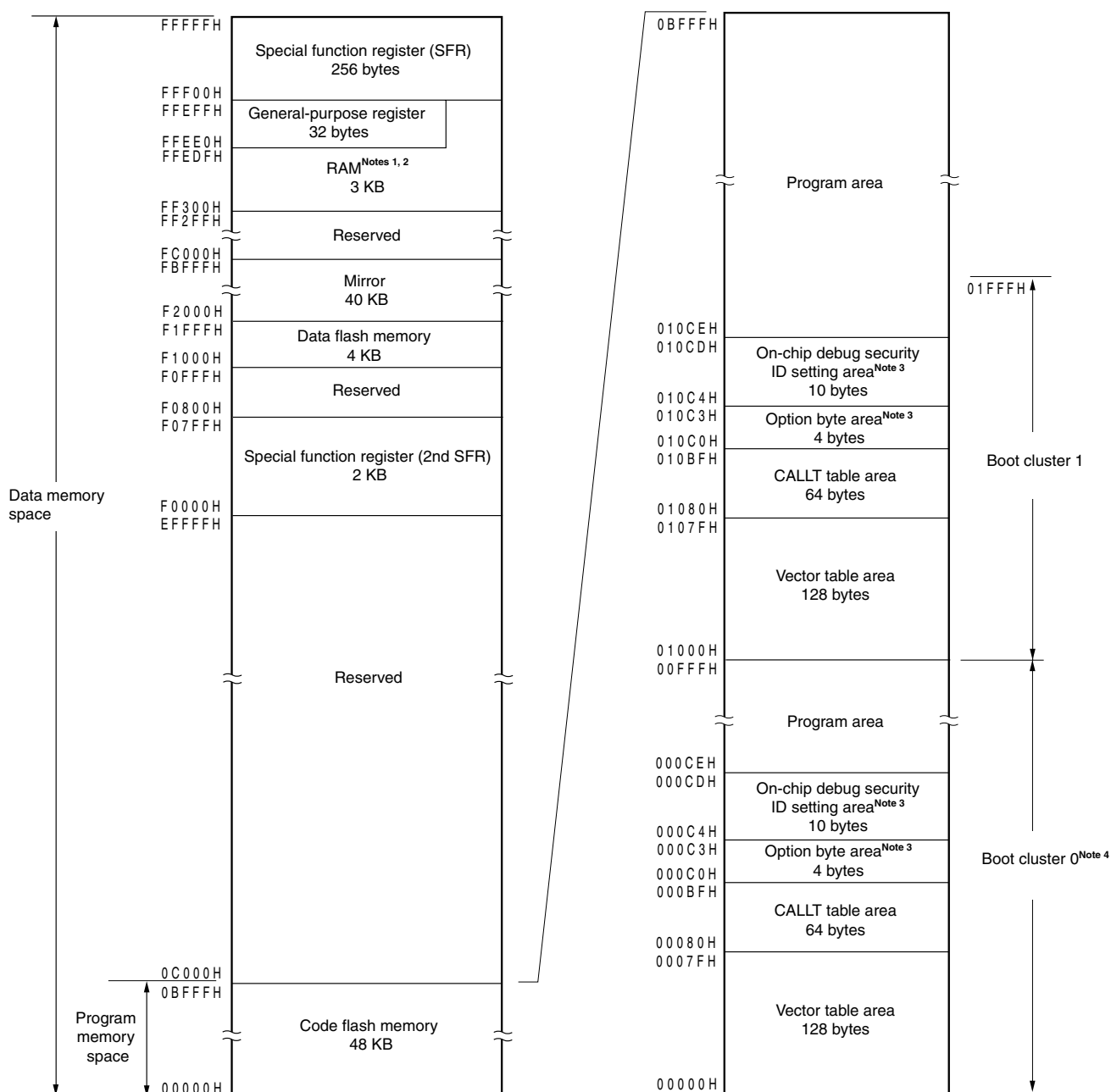
Figure 3-2. Memory Map (R5F10ExC (x = 8, B, G, L))



- <R> **Notes**
1. Use of the area FFE20H to FFEDFH is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.
 2. Instructions can be executed from the RAM area excluding the general-purpose register area.
 3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.
 4. Writing boot cluster 0 can be prohibited depending on the setting of security (see 25.6 Security Setting).

<R> **Caution** When a reset occurs, use RAM parity error reset generation enabled (RPERDIS = 0). If RAM parity error resets to use are enabled (RPERDIS = 0), be sure to initialize the RAM area whose data is to be accessed and the RAM area from which to execute instructions + 10 bytes. Reset signal generation enable RAM parity error reset generation. For detail, refer to 22.3.3 RAM parity error detection function.

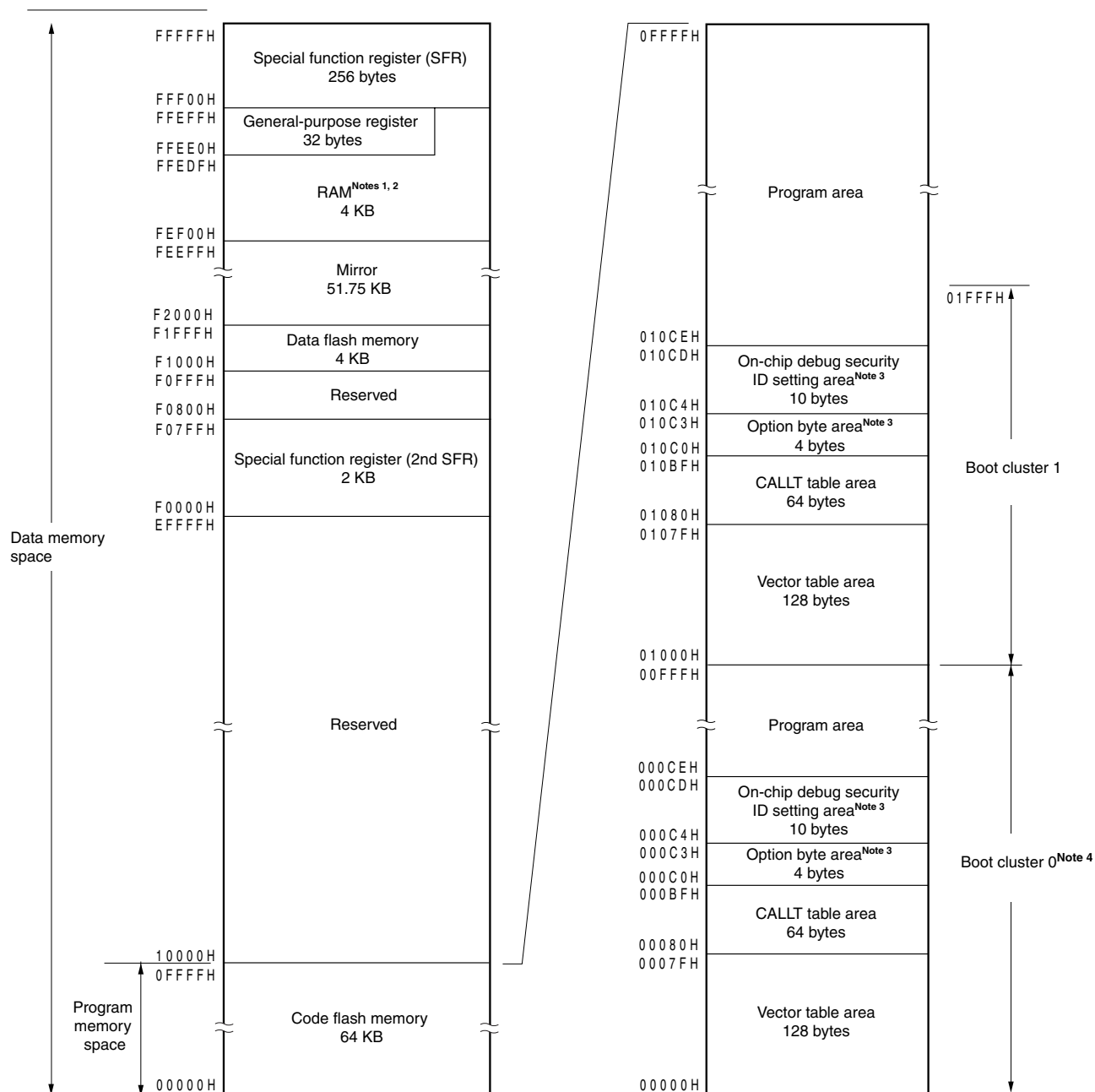
Figure 3-3. Memory Map (R5F10ExD (x = 8, B, G, L))



- <R> **Notes**
1. Use of the area FFE20H to FFEDFH and FF300H to FF309H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.
 2. Instructions can be executed from the RAM area excluding the general-purpose register area.
 3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.
 4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **25.6 Security Setting**).

<R> **Caution** When a reset occurs, use RAM parity error reset generation enabled (RPERDIS = 0). If RAM parity error resets to use are enabled (RPERDIS = 0), be sure to initialize the RAM area whose data is to be accessed and the RAM area from which to execute instructions + 10 bytes. Reset signal generation enable RAM parity error reset generation. For detail, refer to 22.3.3 RAM parity error detection function.

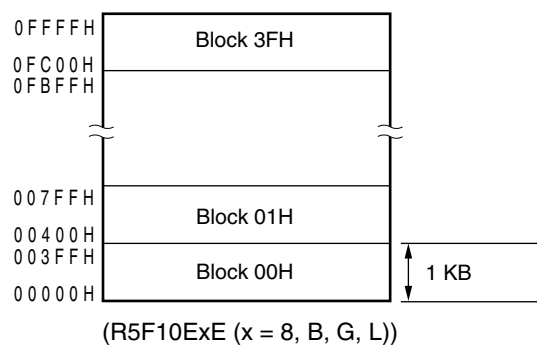
Figure 3-4. Memory Map (R5F10ExE (x = 8, B, G, L))



- <R> **Notes**
1. Use of the area FFE20H to FFEDFH and FEF00H to FF309H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.
 2. Instructions can be executed from the RAM area excluding the general-purpose register area.
 3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.
 4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **25.6 Security Setting**).

<R> **Caution** When a reset occurs, use RAM parity error reset generation enabled (RPERDIS = 0). If RAM parity error resets to use are enabled (RPERDIS = 0), be sure to initialize the RAM area whose data is to be accessed and the RAM area from which to execute instructions + 10 bytes. Reset signal generation enable RAM parity error reset generation. For detail, refer to 22.3.3 RAM parity error detection function.

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see Table 3-1 Correspondence Between Address Values and Block Numbers in Flash Memory.



Correspondence between the address values and block numbers in the flash memory are shown below.

Table 3-1. Correspondence Between Address Values and Block Numbers in Flash Memory

Address Value	Block Number	Address Value	Block Number
00000H to 003FFH	00H	08000H to 083FFH	20H
00400H to 007FFH	01H	08400H to 087FFH	21H
00800H to 00BFFH	02H	08800H to 08BFFH	22H
00C00H to 00FFFH	03H	08C00H to 08FFFH	23H
01000H to 013FFH	04H	09000H to 093FFH	24H
01400H to 017FFH	05H	09400H to 097FFH	25H
01800H to 01BFFH	06H	09800H to 09BFFH	26H
01C00H to 01FFFH	07H	09C00H to 09FFFH	27H
02000H to 023FFH	08H	0A000H to 0A3FFH	28H
02400H to 027FFH	09H	0A400H to 0A7FFH	29H
02800H to 02BFFH	0AH	0A800H to 0ABFFH	2AH
02C00H to 02FFFH	0BH	0AC00H to 0AFFFH	2BH
03000H to 033FFH	0CH	0B000H to 0B3FFH	2CH
03400H to 037FFH	0DH	0B400H to 0B7FFH	2DH
03800H to 03BFFH	0EH	0B800H to 0BBFFH	2EH
03C00H to 03FFFH	0FH	0BC00H to 0BFFFH	2FH
04000H to 043FFH	10H	0C000H to 0C3FFH	30H
04400H to 047FFH	11H	0C400H to 0C7FFH	31H
04800H to 04BFFH	12H	0C800H to 0CBFFH	32H
04C00H to 04FFFH	13H	0CC00H to 0CFFFH	33H
05000H to 053FFH	14H	0D000H to 0D3FFH	34H
05400H to 057FFH	15H	0D400H to 0D7FFH	35H
05800H to 05BFFH	16H	0D800H to 0DBFFH	36H
05C00H to 05FFFH	17H	0DC00H to 0DFFFH	37H
06000H to 063FFH	18H	0E000H to 0E3FFH	38H
06400H to 067FFH	19H	0E400H to 0E7FFH	39H
06800H to 06BFFH	1AH	0E800H to 0EBFFH	3AH
06C00H to 06FFFH	1BH	0EC00H to 0EFFFH	3BH
07000H to 073FFH	1CH	0F000H to 0F3FFH	3CH
07400H to 077FFH	1DH	0F400H to 0F7FFH	3DH
07800H to 07BFFH	1EH	0F800H to 0FBFFH	3EH
07C00H to 07FFFH	1FH	0FC00H to 0FFFFH	3FH

Remark R5F10ExA (x = 8, B, G) : Block numbers 00H to 0FH
R5F10ExC (x = 8, B, G, L) : Block numbers 00H to 1FH
R5F10ExD (x = 8, B, G, L) : Block numbers 00H to 2FH
R5F10ExE (x = 8, B, G, L) : Block numbers 00H to 3FH

<R>

3.1.1 Internal program memory space

The internal program memory space stores the program and table data. The RL78/G1A products incorporate internal ROM (flash memory), as shown below.

Table 3-2. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
R5F10ExA (x = 8, B, G)	Flash memory	16384 × 8 bits (00000H to 03FFFFH)
R5F10ExC (x = 8, B, G, L)		32768 × 8 bits (00000H to 07FFFFH)
R5F10ExD (x = 8, B, G, L)		49152 × 8 bits (00000H to 0BFFFFH)
R5F10ExE (x = 8, B, G, L)		65536 × 8 bits (00000H to 0FFFFH)

The internal program memory space is divided into the following areas.

(1) Vector table area

The 128-byte area 00000H to 0007FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area. Furthermore, the interrupt jump address is a 64 K address of 00000H to 0FFFFH, because the vector code is assumed to be 2 bytes.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

To use the boot swap function, set a vector table also at 01000H to 0107FH.

Table 3-3. Vector Table (1/2)

Vector Table Address	Interrupt Source	64-pin	48-pin	32-pin	25-pin
0000H	RESET, POR, LVD, WDT, TRAP, IAW, RPE	√	√	√	√
0004H	INTWDTI/INTSRO	√	√	√	√
0006H	INTLVI	√	√	√	√
0008H	INTP0	√	√	√	√
000AH	INTP1	√	√	√	√
000CH	INTP2	√	√	√	√
000EH	INTP3	√	√	√	√
0010H	INTP4	√	√	√	√
0012H	INTP5	√	√	—	—
0014H	INTST2/INTCSI20/INTIIC20	√	√	√	—
0016H	INTSR2/INTCSI21/INTIIC21	√	√	Note 1	—
0018H	INTSRE2	√	√	√	—
001AH	INTDMA0	√	√	√	√
001CH	INTDMA1	√	√	√	√
001EH	INTST0/INTCSI00/INTIIC00	√	√	√	√
0020H	INTSR0/INTCSI01/INTIIC01	√	√	Note 2	Note 2
0022H	INTSRE0	√	√	√	√
	INTTM01H	√	√	√	√
0024H	INTST1/INTCSI10/INTIIC10	√	Note 3	Note 3	Note 3
0026H	INTSR1/INTCSI11/INTIIC11	√	√	√	√
0028H	INTSRE1	√	√	√	√
	INTTM03H	√	√	√	√
002AH	INTIICA0	√	√	√	√
002CH	INTTM00	√	√	√	√
002EH	INTTM01	√	√	√	√
0030H	INTTM02	√	√	√	√
0032H	INTTM03	√	√	√	√
0034H	INTAD	√	√	√	√
0036H	INTRTC	√	√	√	√
0038H	INTIT	√	√	√	√
003AH	INTKR	√	√	√	Note 4

Notes 1. INTSR2 only.

2. INTSR0 only.

3. INTSR1 only.

4. When setting the peripheral I/O redirection register (PIOR).

Table 3-3. Vector Table (2/2)

Vector Table Address	Interrupt Source	64-pin	48-pin	32-pin	25-pin
0042H	INTTM04	√	√	√	√
0044H	INTTM05	√	√	√	√
0046H	INTTM06	√	√	√	√
0048H	INTTM07	√	√	√	√
004AH	INTP6	√	√	–	–
004CH	INTP7	√	–	–	–
004EH	INTP8	√	√	–	–
0050H	INTP9	√	√	–	–
0052H	INTP10	√	–	–	–
0054H	INTP11	√	–	–	–
005EH	INTMD	√	√	√	√
0062H	INTFL	√	√	√	√
007EH	BRK	√	√	√	√

(2) CALLT instruction table area

The 64-byte area 00080H to 000BFH can store the subroutine entry address of a 2-byte call instruction (CALLT). Set the subroutine entry address to a value in a range of 00000H to 0FFFFH (because an address code is of 2 bytes).

To use the boot swap function, set a CALLT instruction table also at 01080H to 010BFH.

(3) Option byte area

A 4-byte area of 000C0H to 000C3H can be used as an option byte area. Set the option byte at 010C0H to 010C3H when the boot swap is used. For details, see **CHAPTER 24 OPTION BYTE**.

(4) On-chip debug security ID setting area

A 10-byte area of 000C4H to 000CDH and 010C4H to 010CDH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 000C4H to 000CDH when the boot swap is not used and at 000C4H to 000CDH and 010C4H to 010CDH when the boot swap is used. For details, see **CHAPTER 26 ON-CHIP DEBUG FUNCTION**.

3.1.2 Mirror area

The RL78/G1A mirrors the code flash area of 00000H to 0FFFFH, to F0000H to FFFFFH. The products with 96 KB or more flash memory mirror the code flash area of 00000H to 0FFFFH or 10000H to 1FFFFH, to F0000H to FFFFFH (the code flash area to be mirrored is set by the processor mode control register (PMC)).

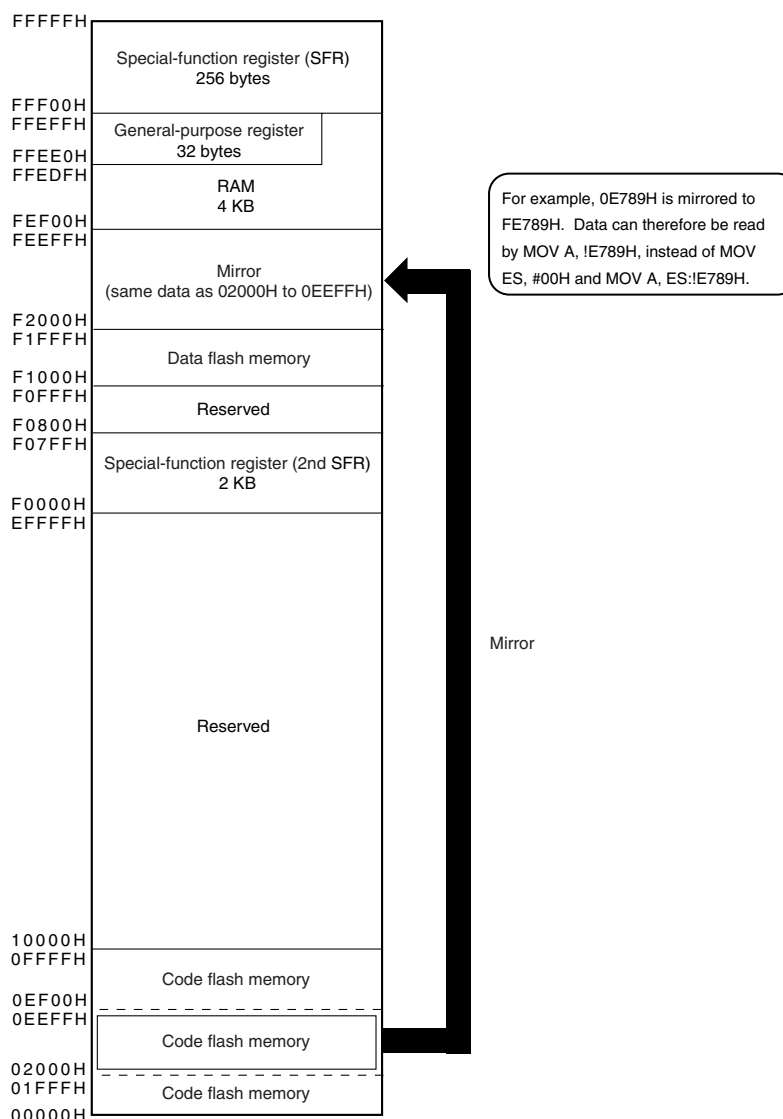
By reading data from F0000H to FFFFFH, an instruction that does not have the ES register as an operand can be used, and thus the contents of the code flash can be read with the shorter code. However, the code flash area is not mirrored to the SFR, extended SFR, RAM, and use prohibited areas.

See **3.1 Memory Space** for the mirror area of each product.

The mirror area can only be read and no instruction can be fetched from this area.

The following show examples.

Example R5F10ExE (x = 8, B, G, L) (Flash memory: 64 KB, RAM: 4 KB)



The PMC register is described below.

- **Processor mode control register (PMC)**

This register sets the flash memory space for mirroring to area from F0000H to FFFFFH.

The PMC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 3-5. Format of Configuration of Processor Mode Control Register (PMC)

Address: FFFFEH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
PMC	0	0	0	0	0	0	0	MAA

MAA	Selection of flash memory space for mirroring to area from F0000H to FFFFFH
0	00000H to 0FFFFH is mirrored to F0000H to FFFFFH
1	Setting is prohibited

- Cautions**
1. Be sure to clear bit 0 (MAA) of this register to 0 (default value).
 2. Set the PMC register only once during the initial settings prior to operating the DMA controller.
Rewriting the PMC register other than during the initial settings is prohibited.
 3. After setting the PMC register, wait for at least one instruction and access the mirror area.

3.1.3 Internal data memory space

The RL78/G1A products incorporate the following RAMs.

Table 3-4. Internal RAM Capacity

Part Number	Internal RAM
R5F10ExA (x = 8, B, G)	2048 × 8 bits (FF700H to FFEFFH)
R5F10ExC (x = 8, B, G, L)	
R5F10ExD (x = 8, B, G, L)	3072 × 8 bits (FF300H to FFEFFH)
R5F10ExE (x = 8, B, G, L)	4096 × 8 bits (FEF00H to FFEFFH)

The internal RAM can be used as a data area and a program area where instructions are written and executed. Four general-purpose register banks consisting of eight 8-bit registers per bank are assigned to the 32-byte area of FFEE0H to FFEFFH of the internal RAM area. However, instructions cannot be executed by using the general-purpose registers.

The internal RAM is used as stack memory.

- Cautions**
1. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.
 2. The internal RAM in the following products cannot be used as stack memory when using the self-programming function and data flash function.

<R>

R5F10ExA (x = 8, B, G): FFE20H to FFEDFH
 R5F10ExC (x = 8, B, G, L): FFE20H to FFEDFH
 R5F10ExD (x = 8, B, G, L): FFE20H to FFEDFH, FF300H to FF309H
 R5F10ExE (x = 8, B, G, L): FFE20H to FFEDFH, FEF00H to FF309H

3.1.4 Special function register (SFR) area

On-chip peripheral hardware special function registers (SFRs) are allocated in the area FFF00H to FFFFFH (see **Table 3-5** in **3.2.4 Special function registers (SFRs)**).

Caution Do not access addresses to which SFRs are not assigned.

3.1.5 Extended special function register (2nd SFR: 2nd Special Function Register) area

On-chip peripheral hardware special function registers (2nd SFRs) are allocated in the area F0000H to F07FFH (see **Table 3-6** in **3.2.5 Extended Special function registers (2nd SFRs: 2nd Special Function Registers)**).

SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

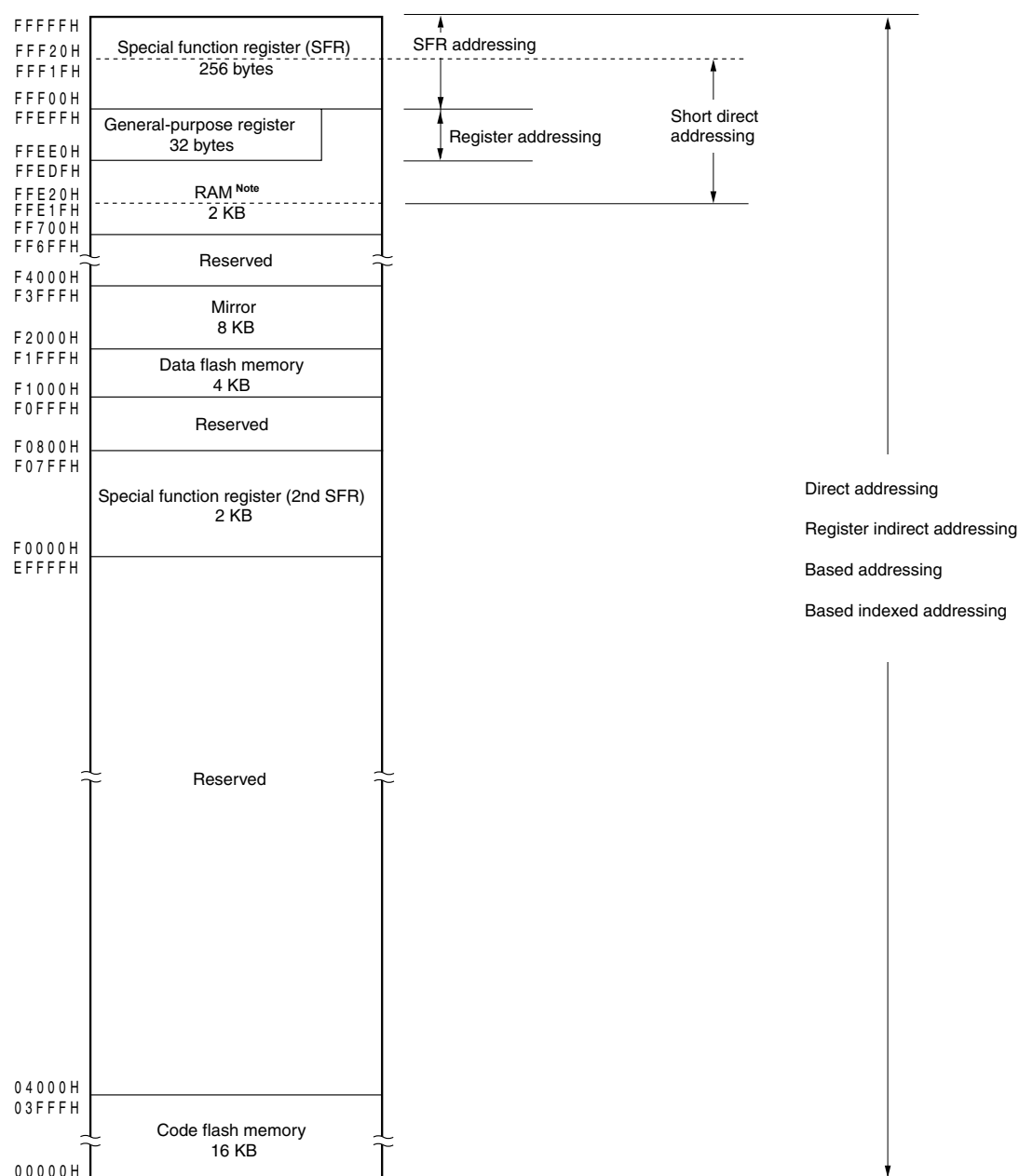
Caution Do not access addresses to which extended SFRs are not assigned.

3.1.6 Data memory addressing

Addressing refers to the method of specifying the address of the instruction to be executed next or the address of the register or memory relevant to the execution of instructions.

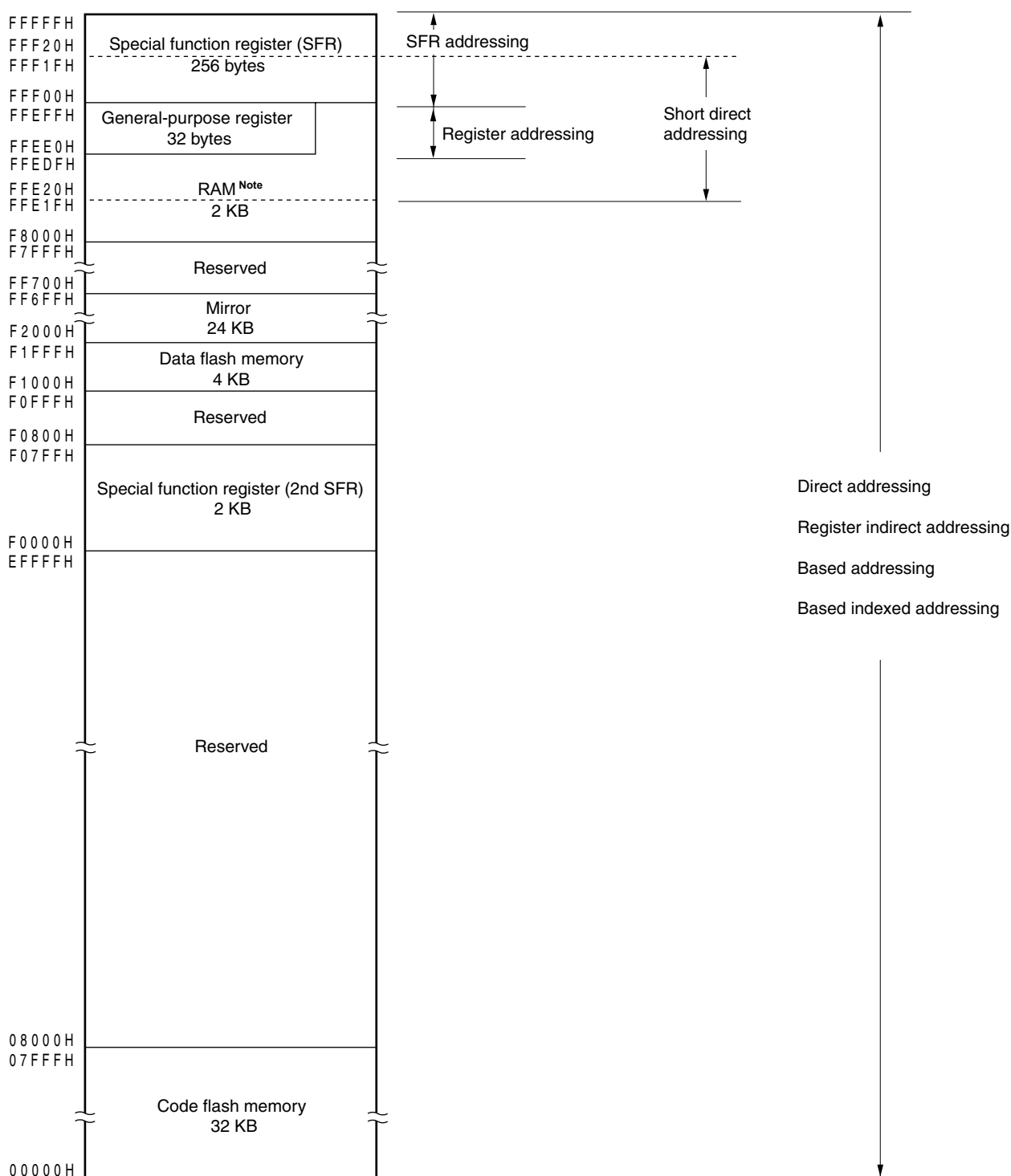
Several addressing modes are provided for addressing the memory relevant to the execution of instructions for the RL78/G1A, based on operability and other considerations. For areas containing data memory in particular, special addressing methods designed for the functions of the special function registers (SFR) and general-purpose registers are available for use. Figures 3-6 to 3-9 show correspondence between data memory and addressing. For details of each addressing, see **3.4 Addressing for Processing Data Addresses**.

Figure 3-6. Correspondence Between Data Memory and Addressing (R5F10ExA (x = 8, B, G))



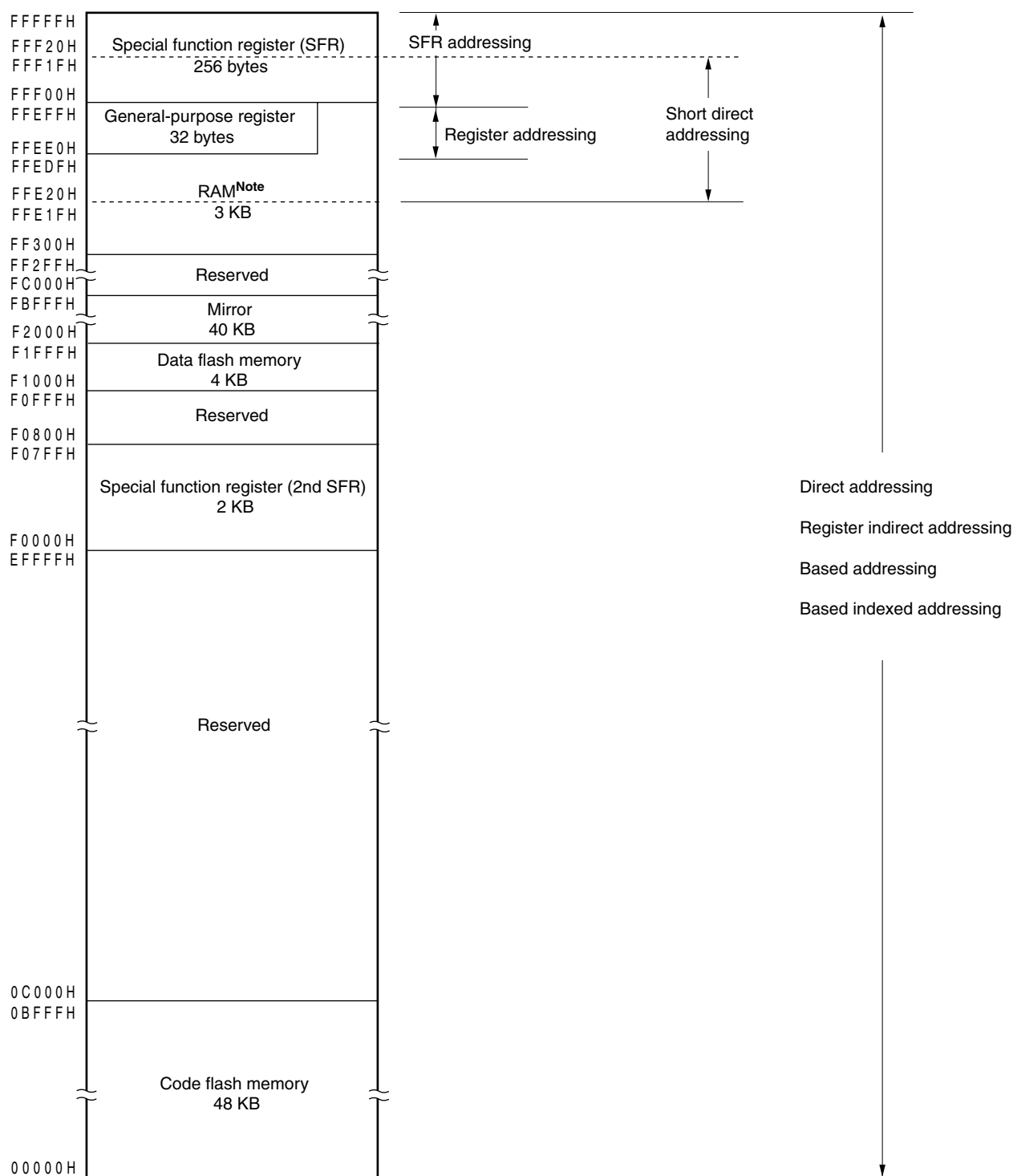
<R> **Note** Use of the area FFE20H to FFEDFH is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.

<R> **Caution** When a reset occurs, use RAM parity error reset generation enabled (RPERDIS = 0). If RAM parity error resets to use are enabled (RPERDIS = 0), be sure to initialize the RAM area whose data is to be accessed and the RAM area from which to execute instructions + 10 bytes. Reset signal generation enable RAM parity error reset generation. For detail, refer to 22.3.3 RAM parity error detection function.

Figure 3-7. Correspondence Between Data Memory and Addressing (R5F10ExC (x = 8, B, G, L))

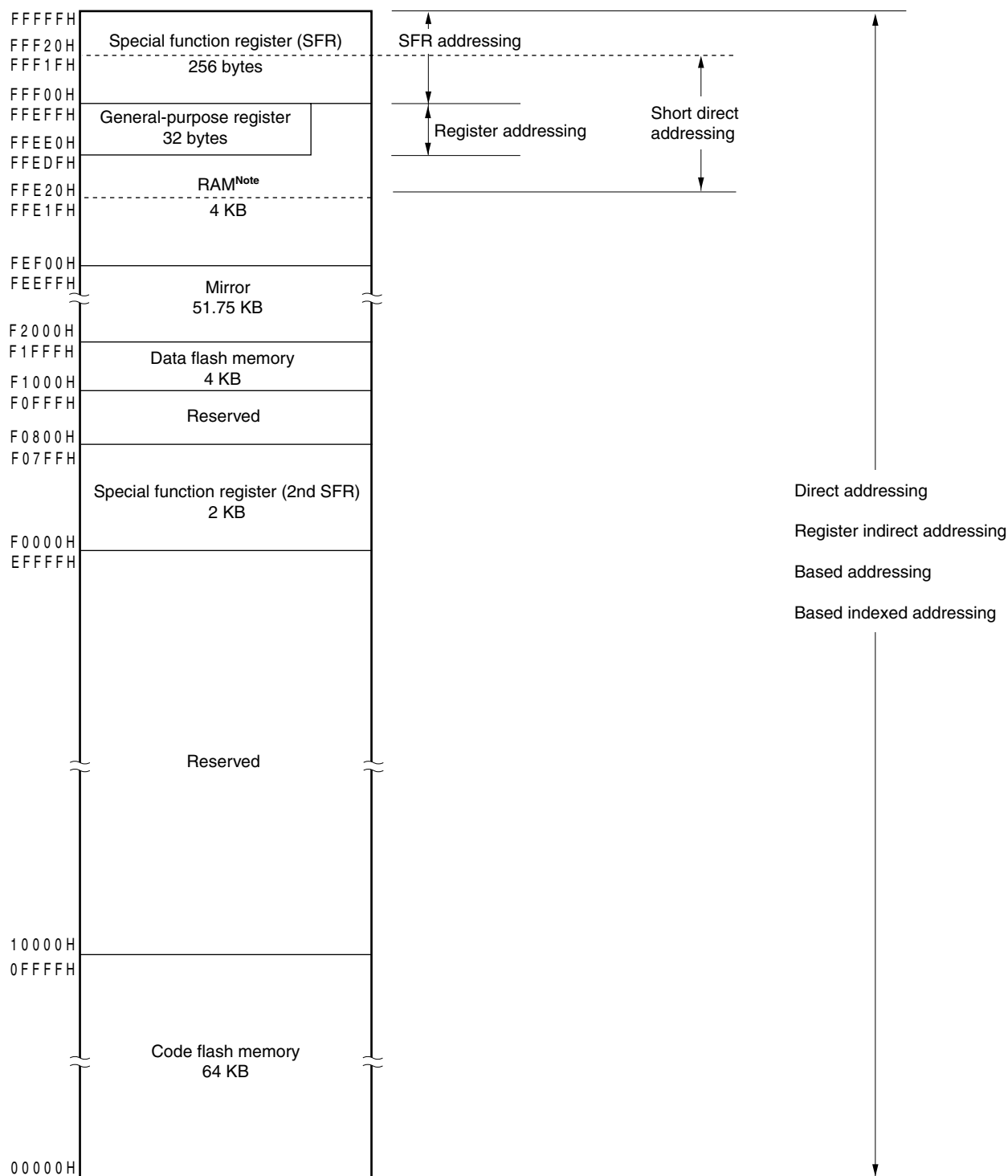
<R> **Note** Use of the area FFE20H to FFE0H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.

<R> **Caution** When a reset occurs, use RAM parity error reset generation enabled (RPERDIS = 0). If RAM parity error resets to use are enabled (RPERDIS = 0), be sure to initialize the RAM area whose data is to be accessed and the RAM area from which to execute instructions + 10 bytes. Reset signal generation enable RAM parity error reset generation. For detail, refer to 22.3.3 RAM parity error detection function.

Figure 3-8. Correspondence Between Data Memory and Addressing (R5F10ExD (x = 8, B, G, L))

<R> **Note** Use of the area FFE20H to FFEDFH and FF300H to FF309H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.

<R> **Caution** When a reset occurs, use RAM parity error reset generation enabled (RPERDIS = 0). If RAM parity error resets to use are enabled (RPERDIS = 0), be sure to initialize the RAM area whose data is to be accessed and the RAM area from which to execute instructions + 10 bytes. Reset signal generation enable RAM parity error reset generation. For detail, refer to 22.3.3 RAM parity error detection function.

Figure 3-9. Correspondence Between Data Memory and Addressing (R5F10ExE (x = 8, B, G, L))

<R> **Note** Use of the area FFE20H to FFE0FH and FEF00H to FF309H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.

<R> **Caution** When a reset occurs, use RAM parity error reset generation enabled (RPERDIS = 0). If RAM parity error resets to use are enabled (RPERDIS = 0), be sure to initialize the RAM area whose data is to be accessed and the RAM area from which to execute instructions + 10 bytes. Reset signal generation enable RAM parity error reset generation. For detail, refer to 22.3.3 RAM parity error detection function.

3.2 Processor Registers

The RL78/G1A products incorporate the following processor registers.

3.2.1 Control registers

The control registers control the program sequence, statuses and stack memory. The control registers consist of a program counter (PC), a program status word (PSW) and a stack pointer (SP).

(1) Program counter (PC)

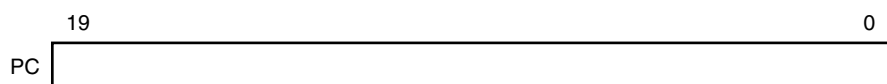
The program counter is a 20-bit register that holds the address information of the next program to be executed.

In normal operation, PC is automatically incremented according to the number of bytes of the instruction to be fetched.

When a branch instruction is executed, immediate data and register contents are set.

Reset signal generation sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 3-10. Format of Program Counter

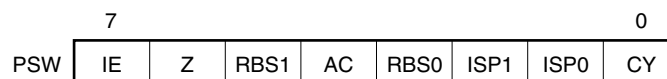


(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags set/reset by instruction execution.

Program status word contents are stored in the stack area upon vectored interrupt request is acknowledged or PUSH PSW instruction execution and are restored upon execution of the RETB, RETI and POP PSW instructions. Reset signal generation sets the PSW register to 06H.

Figure 3-11. Format of Program Status Word



(a) Interrupt enable flag (IE)

This flag controls the interrupt request acknowledge operations of the CPU.

When 0, the IE flag is set to the interrupt disabled (DI) state, and all maskable interrupt requests are disabled.

When 1, the IE flag is set to the interrupt enabled (EI) state and interrupt request acknowledgment is controlled with an in-service priority flag (ISP1, ISP0), an interrupt mask flag for various interrupt sources, and a priority specification flag.

The IE flag is reset (0) upon DI instruction execution or interrupt acknowledgment and is set (1) upon EI instruction execution.

(b) Zero flag (Z)

When the operation result is zero, this flag is set (1). It is reset (0) in all other cases.

(c) Register bank select flags (RBS0, RBS1)

These are 2-bit flags to select one of the four register banks.

In these flags, the 2-bit information that indicates the register bank selected by SEL RBn instruction execution is stored.

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flags (ISP1, ISP0)

This flag manages the priority of acknowledgeable maskable vectored interrupts. Vectored interrupt requests specified lower than the value of ISP0 and ISP1 flags by the priority specification flag registers (PRn0L, PRn0H, PRn1L, PRn1H, PRn2L, PRn2H) (see **16.3.3**) can not be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

Remark n = 0, 1

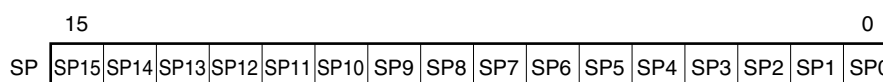
(f) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal RAM area can be set as the stack area.

Figure 3-12. Format of Stack Pointer



The SP is decremented ahead of write (save) to the stack memory and is incremented after read (restored) from the stack memory.

Each stack operation saves data as shown in Figure 3-13.

- Cautions**
1. Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.
 2. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space as a stack area.
 3. The internal RAM in the following products cannot be used as stack memory when using the self-programming function and data flash function.

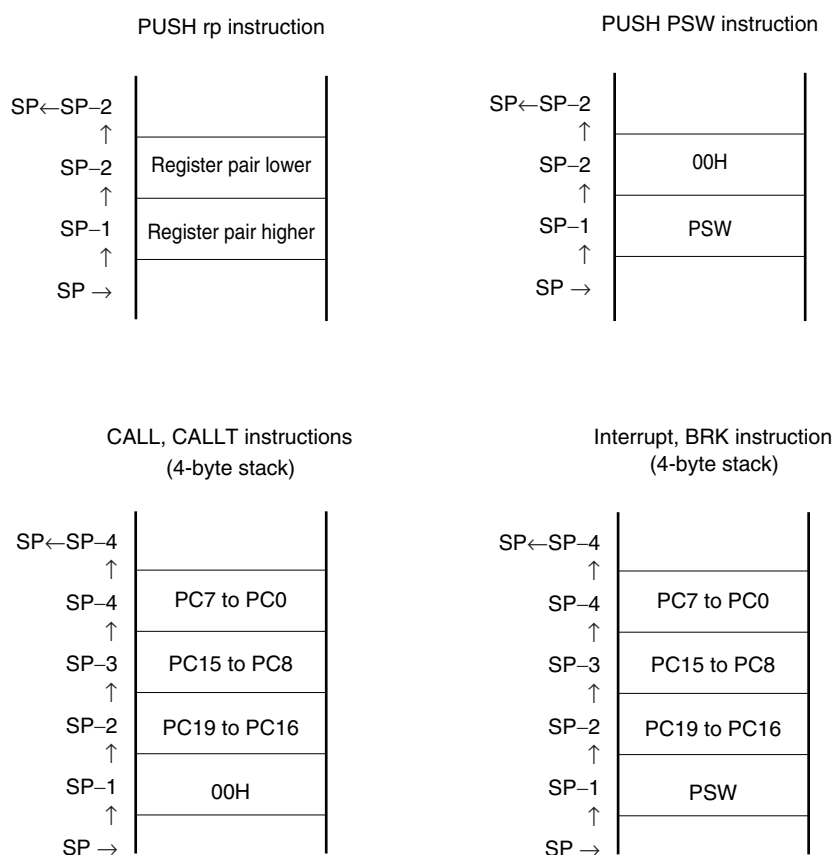
<R>

R5F10ExA (x = 8, B, G): FFE20H to FFEDFH

R5F10ExC (x = 8, B, G, L): FFE20H to FFEDFH

R5F10ExD (x = 8, B, G, L): FFE20H to FFEDFH, FF300H to FF309H

R5F10ExE (x = 8, B, G, L): FFE20H to FFEDFH, FEF00H to FF309H

Figure 3-13. Data to Be Saved to Stack Memory

3.2.2 General-purpose registers

General-purpose registers are mapped at particular addresses (FFEE0H to FFEFFH) of the data memory. The general-purpose registers consists of 4 banks, each bank consisting of eight 8-bit registers (X, A, C, B, E, D, L, and H).

Each register can be used as an 8-bit register, and two 8-bit registers can also be used in a pair as a 16-bit register (AX, BC, DE, and HL).

These registers can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

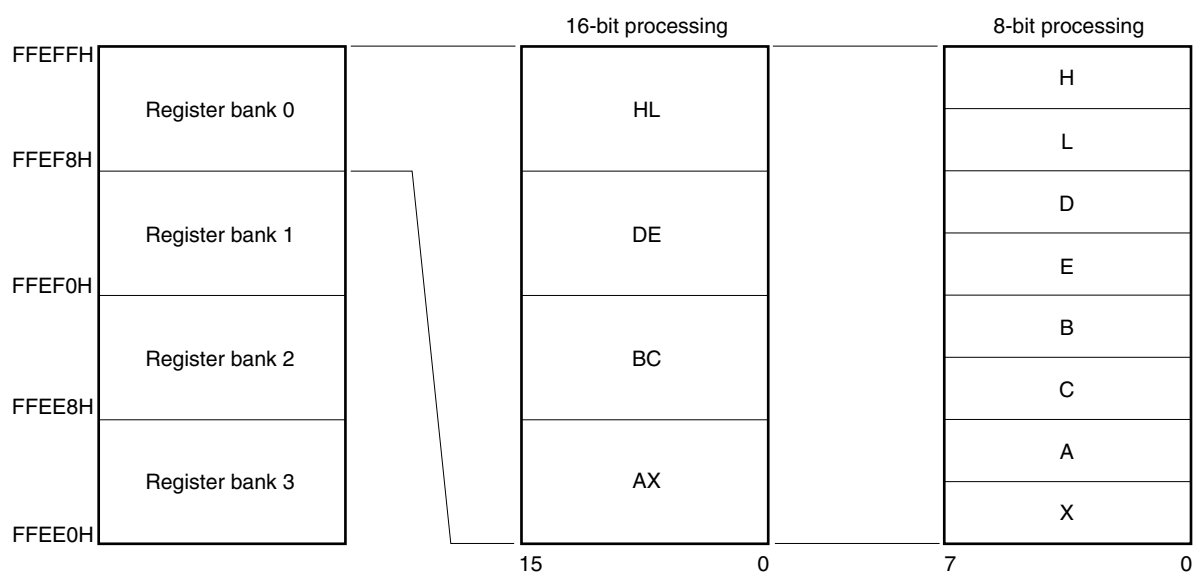
Register banks to be used for instruction execution are set by the CPU control instruction (SEL RBn). Because of the 4-register bank configuration, an efficient program can be created by switching between a register for normal processing and a register for interrupts for each bank.

Caution It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.

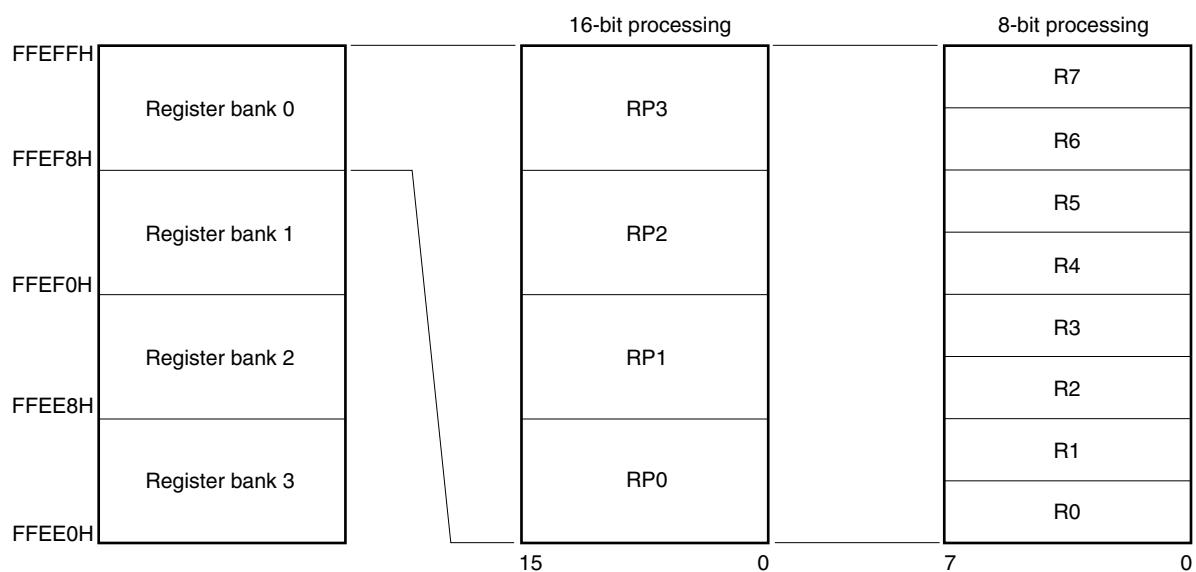
<R>

Figure 3-14. Configuration of General-Purpose Registers

(a) Function name



(b) Absolute name



3.2.3 ES and CS registers

The ES register is used for data access and the CS register is used to specify the higher address when a branch instruction is executed.

The default value of the ES register after reset is 0FH, and that of the CS register is 00H.

Figure 3-15. Configuration of ES and CS Registers

	7	6	5	4	3	2	1	0
ES	0	0	0	0	ES3	ES2	ES1	ES0

	7	6	5	4	3	2	1	0
CS	0	0	0	0	CS3	CP2	CP1	CP0

3.2.4 Special function registers (SFRs)

Unlike a general-purpose register, each SFR has a special function.

SFRs are allocated to the FFF00H to FFFFFH area.

SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit). This manipulation can also be specified with an address.
- 8-bit manipulation
Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr). This manipulation can also be specified with an address.
- 16-bit manipulation
Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (sfrp). When specifying an address, describe an even address.

Table 3-5 gives a list of the SFRs. The meanings of items in the table are as follows.

- Symbol
Symbol indicating the address of a special function register. It is a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler. When using the assembler, debugger, and simulator, symbols can be written as an instruction operand.
- R/W
Indicates whether the corresponding SFR can be read or written.
R/W: Read/write enable
R: Read only
W: Write only
- Manipulable bit units
“√” indicates the manipulable bit unit (1, 8, or 16). “–” indicates a bit unit for which manipulation is not possible.
- After reset
Indicates each register status upon reset signal generation.

Caution Do not access addresses to which extended SFRs are not assigned.

Remark For extended SFRs (2nd SFRs), see 3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers).

Table 3-5. SFR List (1/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
FFF00H	Port register 0	P0	R/W	√	√	–	00H
FFF01H	Port register 1	P1	R/W	√	√	–	00H
FFF02H	Port register 2	P2	R/W	√	√	–	00H
FFF03H	Port register 3	P3	R/W	√	√	–	00H
FFF04H	Port register 4	P4	R/W	√	√	–	00H
FFF05H	Port register 5	P5	R/W	√	√	–	00H
FFF06H	Port register 6	P6	R/W	√	√	–	00H
FFF07H	Port register 7	P7	R/W	√	√	–	00H
FFF0CH	Port register 12	P12	R/W	√	√	–	Undefined
FFF0DH	Port register 13	P13	R/W	√	√	–	Undefined
FFF0EH	Port register 14	P14	R/W	√	√	–	00H
FFF0FH	Port register 15	P15	R/W	√	√	–	00H
FFF10H	Serial data register 00	TXD0/ SIO00	R/W	–	√	√	0000H
FFF11H		–		–	–		
FFF12H	Serial data register 01	RXD0/ SIO01	R/W	–	√	√	0000H
FFF13H		–		–	–		
FFF18H	Timer data register 00	TDR00	R/W	–	–	√	0000H
FFF19H							
FFF1AH	Timer data register 01	TDR01L	R/W	–	√	√	00H
FFF1BH		TDR01H		–	√		00H
FFF1EH	12-bit A/D conversion result register	ADCR	R	–	–	√	0000H
FFF1FH	8-bit A/D conversion result register	ADCRH	R	–	√	–	00H
FFF20H	Port mode register 0	PM0	R/W	√	√	–	FFH
FFF21H	Port mode register 1	PM1	R/W	√	√	–	FFH
FFF22H	Port mode register 2	PM2	R/W	√	√	–	FFH
FFF23H	Port mode register 3	PM3	R/W	√	√	–	FFH
FFF24H	Port mode register 4	PM4	R/W	√	√	–	FFH
FFF25H	Port mode register 5	PM5	R/W	√	√	–	FFH
FFF26H	Port mode register 6	PM6	R/W	√	√	–	FFH
FFF27H	Port mode register 7	PM7	R/W	√	√	–	FFH
FFF2CH	Port mode register 12	PM12	R/W	√	√	–	FFH
FFF2EH	Port mode register 14	PM14	R/W	√	√	–	FFH
FFF2FH	Port mode register 15	PM15	R/W	√	√	–	FFH
FFF30H	A/D converter mode register 0	ADM0	R/W	√	√	–	00H
FFF31H	Analog input channel specification register	ADS	R/W	√	√	–	00H
FFF32H	A/D converter mode register 1	ADM1	R/W	√	√	–	00H

Table 3-5. SFR List (2/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFF34H	Key return control register	KRCTL		R/W	√	√	—	00H
FFF35H	Key return flag register	KRF		R/W	√	√	—	00H
FFF36H	Key return mode control register 1	KRM1		R/W	√	√	—	00H
FFF37H	Key return mode control register 0	KRM0		R/W	√	√	—	00H
FFF38H	External interrupt rising edge enable register 0	EGP0		R/W	√	√	—	00H
FFF39H	External interrupt falling edge enable register 0	EGN0		R/W	√	√	—	00H
FFF3AH	External interrupt rising edge enable register 1	EGP1		R/W	√	√	—	00H
FFF3BH	External interrupt falling edge enable register 1	EGN1		R/W	√	√	—	00H
FFF44H	Serial data register 02	TXD1/ SIO10	SDR02	R/W	—	√	√	0000H
FFF45H		—			—	—		
FFF46H	Serial data register 03	RXD1/ SIO11	SDR03	R/W	—	√	√	0000H
FFF47H		—			—	—		
FFF48H	Serial data register 10	TXD2/ SIO20	SDR10	R/W	—	√	√	0000H
FFF49H		—			—	—		
FFF4AH	Serial data register 11	RXD2/ SIO21	SDR11	R/W	—	√	√	0000H
FFF4BH		—			—	—		
FFF50H	IICA shift register 0	IICA0		R/W	—	√	—	00H
FFF51H	IICA status register 0	IICS0		R	√	√	—	00H
FFF52H	IICA flag register 0	IICF0		R/W	√	√	—	00H
FFF64H	Timer data register 02	TDR02		R/W	—	—	√	0000H
FFF65H								
FFF66H	Timer data register 03	TDR03L	TDR03	R/W	—	√	√	00H
FFF67H		TDR03H			—	√	—	00H
FFF68H	Timer data register 04	TDR04		R/W	—	—	√	0000H
FFF69H								
FFF6AH	Timer data register 05	TDR05		R/W	—	—	√	0000H
FFF6BH								
FFF6CH	Timer data register 06	TDR06		R/W	—	—	√	0000H
FFF6DH								
FFF6EH	Timer data register 07	TDR07		R/W	—	—	√	0000H
FFF6FH								

Table 3-5. SFR List (3/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
FFF90H	Interval timer control register	ITMC	R/W	–	–	√	0FFFH
FFF91H							
FFF92H	Second count register	SEC	R/W	–	√	–	00H
FFF93H	Minute count register	MIN	R/W	–	√	–	00H
FFF94H	Hour count register	HOURL	R/W	–	√	–	12H ^{Note 1}
FFF95H	Week count register	WEEK	R/W	–	√	–	00H
FFF96H	Day count register	DAY	R/W	–	√	–	01H
FFF97H	Month count register	MONTH	R/W	–	√	–	01H
FFF98H	Year count register	YEAR	R/W	–	√	–	00H
FFF99H	Watch error correction register	SUBCUD	R/W	–	√	–	00H
FFF9AH	Alarm minute register	ALARMWMM	R/W	–	√	–	00H
FFF9BH	Alarm hour register	ALARMWH	R/W	–	√	–	12H
FFF9CH	Alarm week register	ALARMWW	R/W	–	√	–	00H
FFF9DH	Real-time clock control register 0	RTCC0	R/W	√	√	–	00H
FFF9EH	Real-time clock control register 1	RTCC1	R/W	√	√	–	00H
FFFA0H	Clock operation mode control register	CMC	R/W	–	√	–	00H
FFFA1H	Clock operation status control register	CSC	R/W	√	√	–	C0H
FFFA2H	Oscillation stabilization time counter status register	OSTC	R	√	√	–	00H
FFFA3H	Oscillation stabilization time select register	OSTS	R/W	–	√	–	07H
FFFA4H	System clock control register	CKC	R/W	√	√	–	00H
FFFA5H	Clock output select register 0	CKS0	R/W	√	√	–	00H
FFFA6H	Clock output select register 1	CKS1	R/W	√	√	–	00H
FFFA8H	Reset control flag register	RESF	R	–	√	–	Undefined ^{Note 2}
FFFA9H	Voltage detection register	LVIM	R/W	√	√	–	00H ^{Note 3}
FFFAAH	Voltage detection level register	LVIS	R/W	√	√	–	00H/01H/81H ^{Note 4}
FFFABH	Watchdog timer enable register	WDTE	R/W	–	√	–	1AH/9AH ^{Note 5}
FFFACH	CRC input register	CRCIN	R/W	–	√	–	00H
FFFB0H	DMA SFR address register 0	DSA0	R/W	–	√	–	00H
FFFB1H	DMA SFR address register 1	DSA1	R/W	–	√	–	00H

- Notes**
1. The value of this register is 00H if the AMPM bit (bit 3 of real-time clock control register 0 (RTCC0)) is set to 1 after reset.
 2. The reset value of the RESF register varies depending on the reset source.
 3. The reset value of the LVIM register varies depending on the reset source.
 4. The reset value of the LVIS register varies depending on the reset source and the setting of the option byte.
 5. The reset value of the WDTE register is determined by the setting of the option byte.

Table 3-5. SFR List (4/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFFB2H	DMA RAM address register 0L	DRA0L	DRA0	R/W	–	√	√	00H
FFFB3H	DMA RAM address register 0H	DRA0H		R/W	–	√		00H
FFFB4H	DMA RAM address register 1L	DRA1L	DRA1	R/W	–	√	√	00H
FFFB5H	DMA RAM address register 1H	DRA1H		R/W	–	√		00H
FFFB6H	DMA byte count register 0L	DBC0L	DBC0	R/W	–	√	√	00H
FFFB7H	DMA byte count register 0H	DBC0H		R/W	–	√		00H
FFFB8H	DMA byte count register 1L	DBC1L	DBC1	R/W	–	√	√	00H
FFFB9H	DMA byte count register 1H	DBC1H		R/W	–	√		00H
FFFB AH	DMA mode control register 0	DMC0		R/W	√	√	–	00H
FFFB BH	DMA mode control register 1	DMC1		R/W	√	√	–	00H
FFFB CH	DMA operation control register 0	DRC0		R/W	√	√	–	00H
FFFB DH	DMA operation control register 1	DRC1		R/W	√	√	–	00H
FFFD0H	Interrupt request flag register 2L	IF2L	IF2	R/W	√	√	√	00H
FFFD1H	Interrupt request flag register 2H	IF2H		R/W	√	√		00H
FFFD2H	Interrupt request flag register 3L	IF3L	IF3	R/W	√	√	√	00H
FFFD4H	Interrupt mask flag register 2L	MK2L	MK2	R/W	√	√	√	FFH
FFFD5H	Interrupt mask flag register 2H	MK2H		R/W	√	√		FFH
FFFD6H	Interrupt mask flag register 3L	MK3L	MK3	R/W	√	√	√	FFH
FFFD8H	Priority specification flag register 02L	PR02L	PR02	R/W	√	√	√	FFH
FFFD9H	Priority specification flag register 02H	PR02H		R/W	√	√		FFH
FFFDCH	Priority specification flag register 12L	PR12L	PR12	R/W	√	√	√	FFH
FFDDH	Priority specification flag register 12H	PR12H		R/W	√	√		FFH
FFFE0H	Interrupt request flag register 0L	IF0L	IF0	R/W	√	√	√	00H
FFFE1H	Interrupt request flag register 0H	IF0H		R/W	√	√		00H
FFFE2H	Interrupt request flag register 1L	IF1L	IF1	R/W	√	√	√	00H
FFFE3H	Interrupt request flag register 1H	IF1H		R/W	√	√		00H
FFFE4H	Interrupt mask flag register 0L	MK0L	MK0	R/W	√	√	√	FFH
FFFE5H	Interrupt mask flag register 0H	MK0H		R/W	√	√		FFH
FFFE6H	Interrupt mask flag register 1L	MK1L	MK1	R/W	√	√	√	FFH
FFFE7H	Interrupt mask flag register 1H	MK1H		R/W	√	√		FFH
FFFE8H	Priority specification flag register 00L	PR00L	PR00	R/W	√	√	√	FFH
FFFE9H	Priority specification flag register 00H	PR00H		R/W	√	√		FFH

Table 3-5. SFR List (5/5)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFFEAH	Priority specification flag register 01L	PR01L	PR01	R/W	√	√	√	FFH
FFFEBH	Priority specification flag register 01H	PR01H		R/W	√	√		FFH
FFFECH	Priority specification flag register 10L	PR10L	PR10	R/W	√	√	√	FFH
FFFEDH	Priority specification flag register 10H	PR10H		R/W	√	√		FFH
FFFEEH	Priority specification flag register 11L	PR11L	PR11	R/W	√	√	√	FFH
FFFEFH	Priority specification flag register 11H	PR11H		R/W	√	√		FFH
FFFF0H	Multiplication/division data register A (L)	MDAL		R/W	—	—	√	0000H
FFFF1H								
FFFF2H	Multiplication/division data register A (H)	MDAH		R/W	—	—	√	0000H
FFFF3H								
FFFF4H	Multiplication/division data register B (H)	MDBH		R/W	—	—	√	0000H
FFFF5H								
FFFF6H	Multiplication/division data register B (L)	MDBL		R/W	—	—	√	0000H
FFFF7H								
FFFEH	Processor mode control register	PMC		R/W	√	√	—	00H

Remark For extended SFRs (2nd SFRs), see **Table 3-6 Extended SFR (2nd SFR) List**.

3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)

Unlike a general-purpose register, each extended SFR (2nd SFR) has a special function.

Extended SFRs are allocated to the F0000H to F07FFH area. SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

Extended SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (!addr16.bit). This manipulation can also be specified with an address.
- 8-bit manipulation
Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (!addr16). This manipulation can also be specified with an address.
- 16-bit manipulation
Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (!addr16). When specifying an address, describe an even address.

Table 3-6 gives a list of the extended SFRs. The meanings of items in the table are as follows.

- Symbol
Symbol indicating the address of an extended SFR. It is a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler. When using the assembler, debugger, and simulator, symbols can be written as an instruction operand.
- R/W
Indicates whether the corresponding extended SFR can be read or written.
R/W: Read/write enable
R: Read only
W: Write only
- Manipulable bit units
“√” indicates the manipulable bit unit (1, 8, or 16). “—” indicates a bit unit for which manipulation is not possible.
- After reset
Indicates each register status upon reset signal generation.

Caution Do not access addresses to which extended SFRs are not assigned.

Remark For SFRs in the SFR area, see 3.2.4 Special function registers (SFRs).

Table 3-6. Extended SFR (2nd SFR) List (1/6)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F0010H	A/D converter mode register 2	ADM2	R/W	√	√	–	00H
F0011H	Conversion result comparison upper limit setting register	ADUL	R/W	–	√	–	FFH
F0012H	Conversion result comparison lower limit setting register	ADLL	R/W	–	√	–	00H
F0013H	A/D test register	ADTES	R/W	–	√	–	00H
F0030H	Pull-up resistor option register 0	PU0	R/W	√	√	–	00H
F0031H	Pull-up resistor option register 1	PU1	R/W	√	√	–	00H
F0033H	Pull-up resistor option register 3	PU3	R/W	√	√	–	00H
F0034H	Pull-up resistor option register 4	PU4	R/W	√	√	–	01H
F0035H	Pull-up resistor option register 5	PU5	R/W	√	√	–	00H
F0037H	Pull-up resistor option register 7	PU7	R/W	√	√	–	00H
F003CH	Pull-up resistor option register 12	PU12	R/W	√	√	–	00H
F003EH	Pull-up resistor option register 14	PU14	R/W	√	√	–	00H
F0040H	Port input mode register 0	PIM0	R/W	√	√	–	00H
F0041H	Port input mode register 1	PIM1	R/W	√	√	–	00H
F0050H	Port output mode register 0	POM0	R/W	√	√	–	00H
F0051H	Port output mode register 1	POM1	R/W	√	√	–	00H
F0055H	Port output mode register 5	POM5	R/W	√	√	–	00H
F0057H	Port output mode register 7	POM7	R/W	√	√	–	00H
F0060H	Port mode control register 0	PMC0	R/W	√	√	–	FFH
F0061H	Port mode control register 1	PMC1	R/W	√	√	–	FFH
F0063H	Port mode control register 3	PMC3	R/W	√	√	–	FFH
F0064H	Port mode control register 4	PMC4	R/W	√	√	–	FFH
F0065H	Port mode control register 5	PMC5	R/W	√	√	–	FFH
F0067H	Port mode control register 7	PMC7	R/W	√	√	–	FFH
F006CH	Port mode control register 12	PMC12	R/W	√	√	–	FFH
F0070H	Noise filter enable register 0	NFEN0	R/W	√	√	–	00H
F0071H	Noise filter enable register 1	NFEN1	R/W	√	√	–	00H
F0073H	Input switch control register	ISC	R/W	√	√	–	00H
F0074H	Timer input select register 0	TIS0	R/W	–	√	–	00H
F0076H	A/D port configuration register	ADPC	R/W	–	√	–	00H
F0077H	Peripheral I/O redirection register	PIOR	R/W	–	√	–	00H
F0078H	Invalid memory access detection control register	IAWCTL	R/W	–	√	–	00H

Table 3-6. Extended SFR (2nd SFR) List (2/6)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F007CH	Global analog input disable register	GAIDIS	R/W	√	√	–	00H
F007DH	Global digital input disable register	GDIDIS	R/W	√	√	–	00H
F0090H	Data flash control register	DFLCTL	R/W	√	√	–	00H
F00A0H	High-speed on-chip oscillator trimming register	HIOTRM	R/W	–	√	–	Note
F00A8H	High-speed on-chip oscillator frequency select register	HOCODIV	R/W	–	√	–	Undefined
F00E0H	Multiplication/division data register C (L)	MDCL	R/W	–	–	√	0000H
F00E2H	Multiplication/division data register C (H)	MDCH	R/W	–	–	√	0000H
F00E8H	Multiplication/division control register	MDUC	R/W	√	√	–	00H
F00F0H	Peripheral enable register 0	PER0	R/W	√	√	–	00H
F00F3H	Operation speed mode control register	OSMC	R/W	–	√	–	00H
F00F5H	RAM parity error control register	RPECTL	R/W	√	√	–	00H
F00FEH	BCD adjust result register	BCDADJ	R	–	√	–	Undefined
F0100H	Serial status register 00	SSR00L	SSR00	R	–	√	0000H
F0101H		–			–	–	
F0102H	Serial status register 01	SSR01L	SSR01	R	–	√	0000H
F0103H		–			–	–	
F0104H	Serial status register 02	SSR02L	SSR02	R	–	√	0000H
F0105H		–			–	–	
F0106H	Serial status register 03	SSR03L	SSR03	R	–	√	0000H
F0107H		–			–	–	
F0108H	Serial flag clear trigger register 00	SIR00L	SIR00	R/W	–	√	0000H
F0109H		–			–	–	
F010AH	Serial flag clear trigger register 01	SIR01L	SIR01	R/W	–	√	0000H
F010BH		–			–	–	
F010CH	Serial flag clear trigger register 02	SIR02L	SIR02	R/W	–	√	0000H
F010DH		–			–	–	
F010EH	Serial flag clear trigger register 03	SIR03L	SIR03	R/W	–	√	0000H
F010FH		–			–	–	

Note The reset value differs for each chip.

Table 3-6. Extended SFR (2nd SFR) List (3/6)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F0110H	Serial mode register 00	SMR00	R/W	–	–	√	0020H	
F0111H								
F0112H	Serial mode register 01	SMR01	R/W	–	–	√	0020H	
F0113H								
F0114H	Serial mode register 02	SMR02	R/W	–	–	√	0020H	
F0115H								
F0116H	Serial mode register 03	SMR03	R/W	–	–	√	0020H	
F0117H								
F0118H	Serial communication operation setting register 00	SCR00	R/W	–	–	√	0087H	
F0119H								
F011AH	Serial communication operation setting register 01	SCR01	R/W	–	–	√	0087H	
F011BH								
F011CH	Serial communication operation setting register 02	SCR02	R/W	–	–	√	0087H	
F011DH								
F011EH	Serial communication operation setting register 03	SCR03	R/W	–	–	√	0087H	
F011FH								
F0120H	Serial channel enable status register 0	SE0L	SE0	R	√	√	√	0000H
F0121H		–			–	–		
F0122H	Serial channel start register 0	SS0L	SS0	R/W	√	√	√	0000H
F0123H		–			–	–		
F0124H	Serial channel stop register 0	ST0L	ST0	R/W	√	√	√	0000H
F0125H		–			–	–		
F0126H	Serial clock select register 0	SPS0L	SPS0	R/W	–	√	√	0000H
F0127H		–			–	–		
F0128H	Serial output register 0	SO0		R/W	–	–	√	0F0FH
F0129H								
F012AH	Serial output enable register 0	SOE0L	SOE0	R/W	√	√	√	0000H
F012BH		–			–	–		
F0134H	Serial output level register 0	SOL0L	SOL0	R/W	–	√	√	0000H
F0135H		–			–	–		
F0138H	Serial standby control register 0	SSC0L	SSC0	R/W	–	√	√	0000H
		–			–	–		
F0140H	Serial status register 10	SSR10L	SSR10	R	–	√	√	0000H
F0141H		–			–	–		
F0142H	Serial status register 11	SSR11L	SSR11	R	–	√	√	0000H
F0143H		–			–	–		
F0148H	Serial flag clear trigger register 10	SIR10L	SIR10	R/W	–	√	√	0000H
F0149H		–			–	–		
F014AH	Serial flag clear trigger register 11	SIR11L	SIR11	R/W	–	√	√	0000H
F014BH		–			–	–		

Table 3-6. Extended SFR (2nd SFR) List (4/6)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F0150H	Serial mode register 10	SMR10		R/W	–	–	√	0020H
F0151H								
F0152H	Serial mode register 11	SMR11		R/W	–	–	√	0020H
F0153H								
F0158H	Serial communication operation setting register 10	SCR10		R/W	–	–	√	0087H
F0159H								
F015AH	Serial communication operation setting register 11	SCR11		R/W	–	–	√	0087H
F015BH								
F0160H	Serial channel enable status register 1	SE1L	SE1	R	√	√	√	0000H
F0161H		–			–	–		
F0162H	Serial channel start register 1	SS1L	SS1	R/W	√	√	√	0000H
F0163H		–			–	–		
F0164H	Serial channel stop register 1	ST1L	ST1	R/W	√	√	√	0000H
F0165H		–			–	–		
F0166H	Serial clock select register 1	SPS1L	SPS1	R/W	–	√	√	0000H
F0167H		–			–	–		
F0168H	Serial output register 1	SO1		R/W	–	–	√	0F0FH
F0169H								
F016AH	Serial output enable register 1	SOE1L	SOE1	R/W	√	√	√	0000H
F016BH		–			–	–		
F0174H	Serial output level register 1	SOL1L	SOL1	R/W	–	√	√	0000H
F0175H		–			–	–		
F0180H	Timer counter register 00	TCR00		R	–	–	√	FFFFH
F0181H								
F0182H	Timer counter register 01	TCR01		R	–	–	√	FFFFH
F0183H								
F0184H	Timer counter register 02	TCR02		R	–	–	√	FFFFH
F0185H								
F0186H	Timer counter register 03	TCR03		R	–	–	√	FFFFH
F0187H								
F0188H	Timer counter register 04	TCR04		R	–	–	√	FFFFH
F0189H								
F018AH	Timer counter register 05	TCR05		R	–	–	√	FFFFH
F018BH								
F018CH	Timer counter register 06	TCR06		R	–	–	√	FFFFH
F018DH								
F018EH	Timer counter register 07	TCR07		R	–	–	√	FFFFH
F018FH								

Table 3-6. Extended SFR (2nd SFR) List (5/6)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F0190H	Timer mode register 00	TMR00		R/W	–	–	√	0000H
F0191H								
F0192H	Timer mode register 01	TMR01		R/W	–	–	√	0000H
F0193H								
F0194H	Timer mode register 02	TMR02		R/W	–	–	√	0000H
F0195H								
F0196H	Timer mode register 03	TMR03		R/W	–	–	√	0000H
F0197H								
F0198H	Timer mode register 04	TMR04		R/W	–	–	√	0000H
F0199H								
F019AH	Timer mode register 05	TMR05		R/W	–	–	√	0000H
F019BH								
F019CH	Timer mode register 06	TMR06		R/W	–	–	√	0000H
F019DH								
F019EH	Timer mode register 07	TMR07		R/W	–	–	√	0000H
F019FH								
F01A0H	Timer status register 00	TSR00L	TSR00	R	–	√	√	0000H
F01A1H		–			–	–		
F01A2H	Timer status register 01	TSR01L	TSR01	R	–	√	√	0000H
F01A3H		–			–	–		
F01A4H	Timer status register 02	TSR02L	TSR02	R	–	√	√	0000H
F01A5H		–			–	–		
F01A6H	Timer status register 03	TSR03L	TSR03	R	–	√	√	0000H
F01A7H		–			–	–		
F01A8H	Timer status register 04	TSR04L	TSR04	R	–	√	√	0000H
F01A9H		–			–	–		
F01AAH	Timer status register 05	TSR05L	TSR05	R	–	√	√	0000H
F01ABH		–			–	–		
F01ACH	Timer status register 06	TSR06L	TSR06	R	–	√	√	0000H
F01ADH		–			–	–		
F01AEH	Timer status register 07	TSR07L	TSR07	R	–	√	√	0000H
F01AFH		–			–	–		

Table 3-6. Extended SFR (2nd SFR) List (6/6)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F01B0H	Timer channel enable status register 0	TE0L	TE0	R	√	√	√	0000H
F01B1H		—			—	—		
F01B2H	Timer channel start register 0	TS0L	TS0	R/W	√	√	√	0000H
F01B3H		—			—	—		
F01B4H	Timer channel stop register 0	TT0L	TT0	R/W	√	√	√	0000H
F01B5H		—			—	—		
F01B6H	Timer clock select register 0	TPS0		R/W	—	—	√	0000H
F01B7H								
F01B8H	Timer output register 0	TO0L	TO0	R/W	—	√	√	0000H
F01B9H		—			—	—		
F01BAH	Timer output enable register 0	TOE0L	TOE0	R/W	√	√	√	0000H
F01BBH		—			—	—		
F01BCH	Timer output level register 0	TOL0L	TOL0	R/W	—	√	√	0000H
F01BDH		—			—	—		
F01BEH	Timer output mode register 0	TOM0L	TOM0	R/W	—	√	√	0000H
F01BFH		—			—	—		
F0230H	IICA control register 00	IICCTL00	R/W	√	√	—	00H	F0230H
F0231H	IICA control register 01	IICCTL01	R/W	√	√	—	00H	F0231H
F0232H	IICA low-level width setting register 0	IICWL0	R/W	—	√	—	FFH	F0232H
F0233H	IICA high-level width setting register 0	IICWH0	R/W	—	√	—	FFH	F0233H
F0234H	Slave address register 0	SVA0	R/W	—	√	—	00H	F0234H
F02F0H	Flash memory CRC control register	CRC0 CTL	R/W	√	√	—	00H	F02F0H
F02F2H	Flash memory CRC operation result register	PGCR CL	R/W	—	—	√	0000H	F02F2H
F02FAH	CRC data register	CRCD	R/W	—	—	√	0000H	F02FAH

Remark For SFRs in the SFR area, see Table 3-5 SFR List.

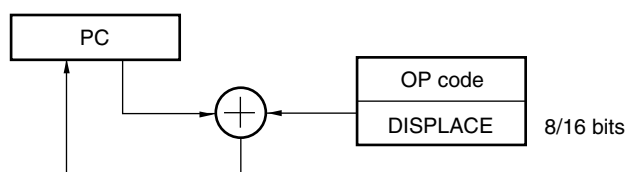
3.3 Instruction Address Addressing

3.3.1 Relative addressing

[Function]

Relative addressing stores in the program counter (PC) the result of adding a displacement value included in the instruction word (signed complement data: -128 to $+127$ or -32768 to $+32767$) to the program counter (PC)'s value (the start address of the next instruction), and specifies the program address to be used as the branch destination. Relative addressing is applied only to branch instructions.

Figure 3-16. Outline of Relative Addressing



3.3.2 Immediate addressing

[Function]

Immediate addressing stores immediate data of the instruction word in the program counter, and specifies the program address to be used as the branch destination.

For immediate addressing, CALL !!addr20 or BR !!addr20 is used to specify 20-bit addresses and CALL !addr16 or BR !addr16 is used to specify 16-bit addresses. 0000 is set to the higher 4 bits when specifying 16-bit addresses.

Figure 3-17. Example of CALL !!addr20/BR !!addr20

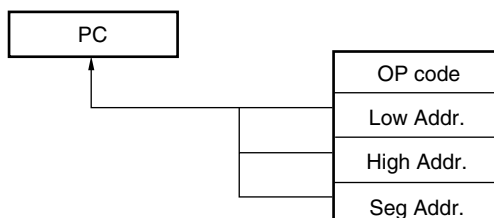
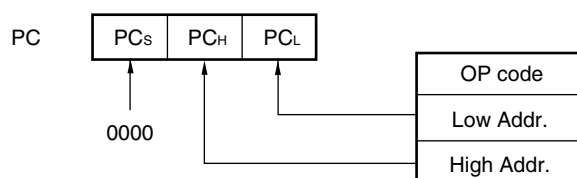


Figure 3-18. Example of CALL !addr16/BR !addr16



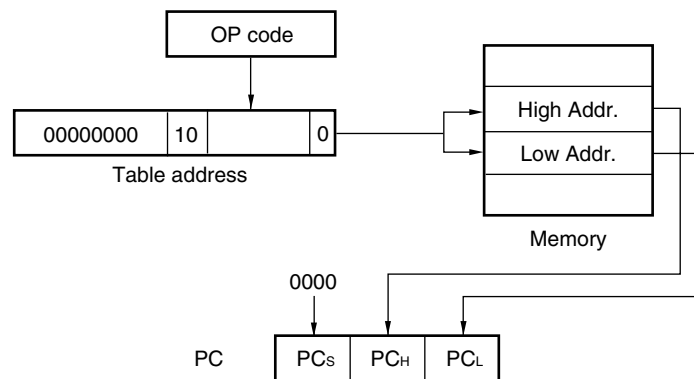
3.3.3 Table indirect addressing

[Function]

Table indirect addressing specifies a table address in the CALLT table area (0080H to 00BFH) with the 5-bit immediate data in the instruction word, stores the contents at that table address and the next address in the program counter (PC) as 16-bit data, and specifies the program address. Table indirect addressing is applied only for CALLT instructions.

In the RL78 microcontrollers, branching is enabled only to the 64 KB space from 00000H to 0FFFFH.

Figure 3-19. Outline of Table Indirect Addressing

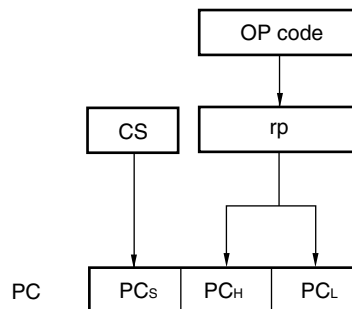


3.3.4 Register direct addressing

[Function]

Register direct addressing stores in the program counter (PC) the contents of a general-purpose register pair (AX/BC/DE/HL) and CS register of the current register bank specified with the instruction word as 20-bit data, and specifies the program address. Register direct addressing can be applied only to the CALL AX, BC, DE, HL, and BR AX instructions.

Figure 3-20. Outline of Register Direct Addressing



3.4 Addressing for Processing Data Addresses

3.4.1 Implied addressing

[Function]

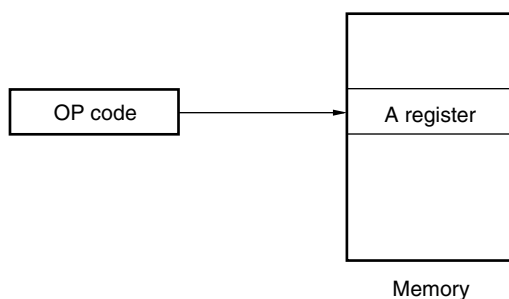
Instructions for accessing registers (such as accumulators) that have special functions are directly specified with the instruction word, without using any register specification field in the instruction word.

[Operand format]

Because implied addressing can be automatically employed with an instruction, no particular operand format is necessary.

Implied addressing can be applied only to MULU X.

Figure 3-21. Outline of Implied Addressing



3.4.2 Register addressing

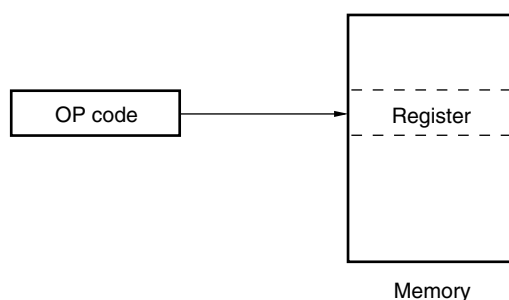
[Function]

Register addressing accesses a general-purpose register as an operand. The instruction word of 3-bit long is used to select an 8-bit register and the instruction word of 2-bit long is used to select a 16-bit register.

[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

Figure 3-22. Outline of Register Addressing



3.4.3 Direct addressing

[Function]

Direct addressing uses immediate data in the instruction word as an operand address to directly specify the target address.

[Operand format]

Identifier	Description
ADDR16	Label or 16-bit immediate data (only the space from F0000H to FFFFFH is specifiable)
ES: ADDR16	Label or 16-bit immediate data (higher 4-bit addresses are specified by the ES register)

Figure 3-23. Example of ADDR16

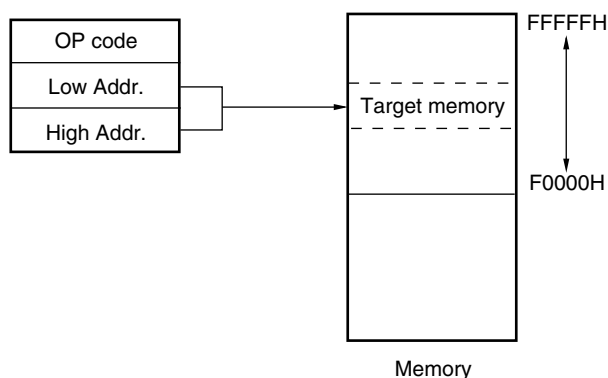
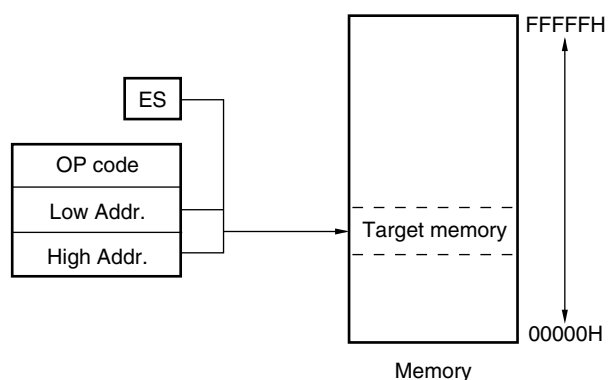


Figure 3-24. Example of ES:ADDR16



3.4.4 Short direct addressing

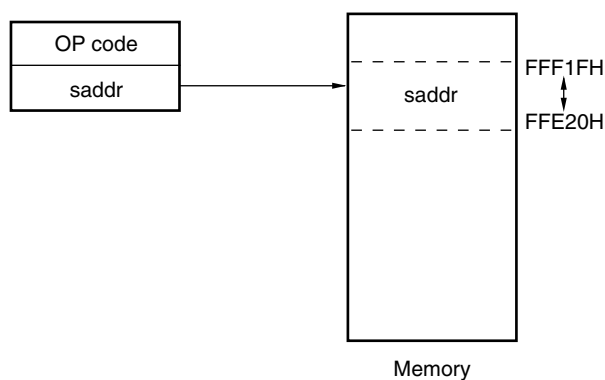
[Function]

Short direct addressing directly specifies the target addresses using 8-bit data in the instruction word. This type of addressing is applied only to the space from FFE20H to FFF1FH.

[Operand format]

Identifier	Description
SADDR	Label, FFE20H to FFF1FH immediate data, or 0FE20H to 0FF1FH immediate data (only the space from FFE20H to FFF1FH is specifiable)
SADDRP	Label, FFE20H to FFF1FH immediate data, or 0FE20H to 0FF1FH immediate data (even address only) (only the space from FFE20H to FFF1FH is specifiable)

Figure 3-25. Outline of Short Direct Addressing



Remark SADDR and SADDRP are used to describe the values of addresses FE20H to FF1FH with 16-bit immediate data (higher 4 bits of actual address are omitted), and the values of addresses FFE20H to FFF1FH with 20-bit immediate data.

Regardless of whether SADDR or SADDRP is used, addresses within the space from FFE20H to FFF1FH are specified for the memory.

3.4.5 SFR addressing

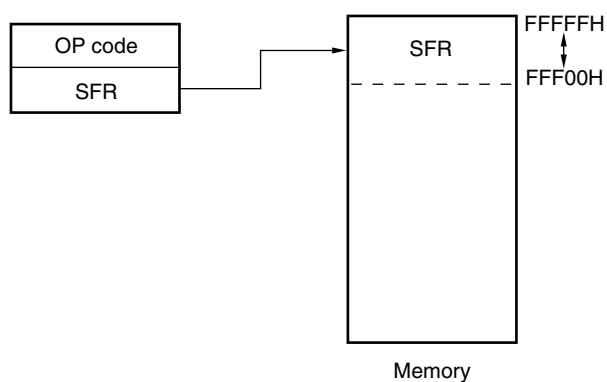
[Function]

SFR addressing directly specifies the target SFR addresses using 8-bit data in the instruction word. This type of addressing is applied only to the space from FFF00H to FFFFFH.

[Operand format]

Identifier	Description
SFR	SFR name
SFRP	16-bit-manipulatable SFR name (even address only)

Figure 3-26. Outline of SFR Addressing



3.4.6 Register indirect addressing

[Function]

Register indirect addressing directly specifies the target addresses using the contents of the register pair specified with the instruction word as an operand address.

[Operand format]

Identifier	Description
–	[DE], [HL] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[DE], ES:[HL] (higher 4-bit addresses are specified by the ES register)

Figure 3-27. Example of [DE], [HL]

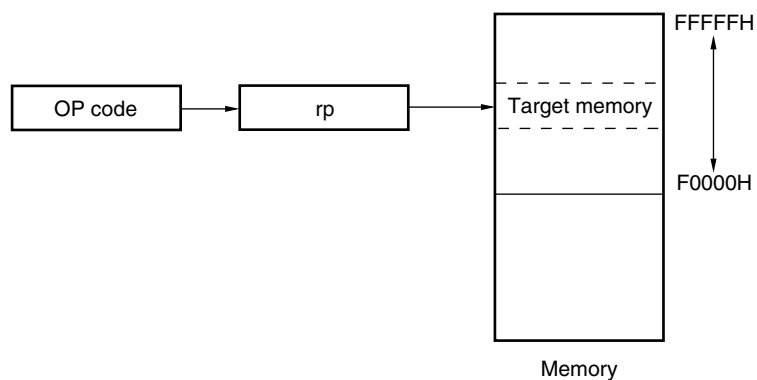
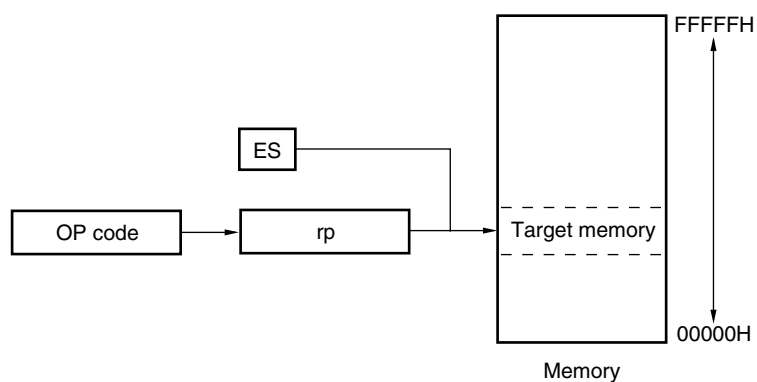


Figure 3-28. Example of ES:[DE], ES:[HL]



3.4.7 Based addressing

[Function]

Based addressing uses the contents of a register pair specified with the instruction word as a base address, and 8-bit immediate data or 16-bit immediate data as offset data. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
–	[HL + byte], [DE + byte], [SP + byte] (only the space from F0000H to FFFFFH is specifiable)
–	word[B], word[C] (only the space from F0000H to FFFFFH is specifiable)
–	word[BC] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[HL + byte], ES:[DE + byte] (higher 4-bit addresses are specified by the ES register)
–	ES:word[B], ES:word[C] (higher 4-bit addresses are specified by the ES register)
–	ES:word[BC] (higher 4-bit addresses are specified by the ES register)

Figure 3-29. Example of [SP+byte]

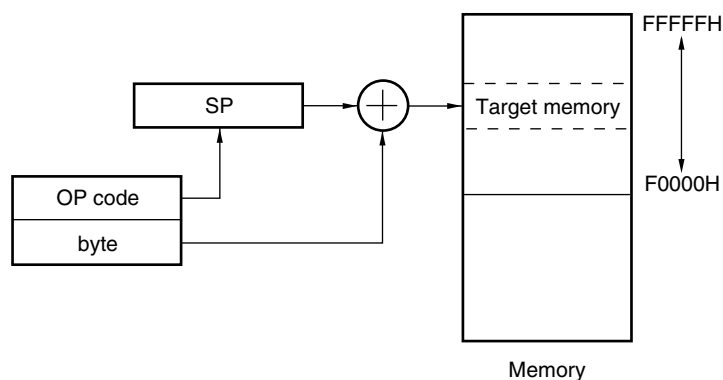


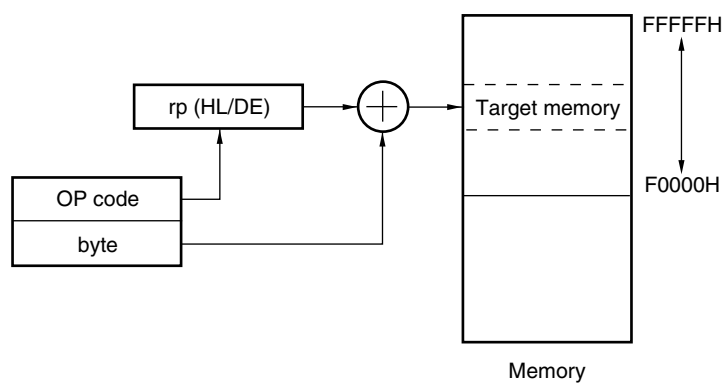
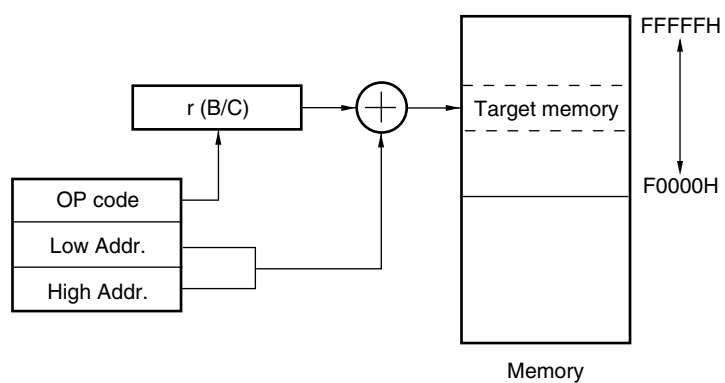
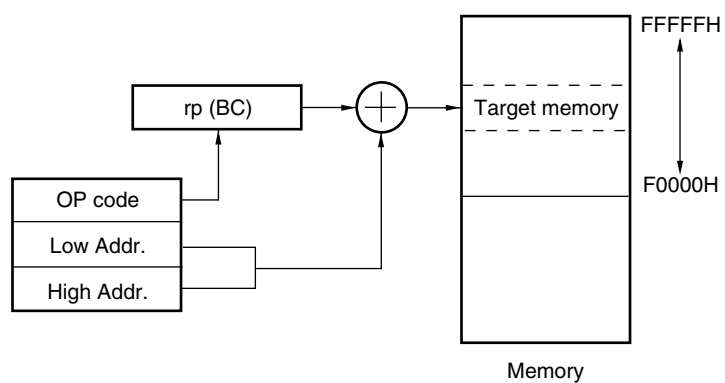
Figure 3-30. Example of [HL + byte], [DE + byte]**Figure 3-31. Example of word[B], word[C]****Figure 3-32. Example of word[BC]**

Figure 3-33. Example of ES:[HL + byte], ES:[DE + byte]

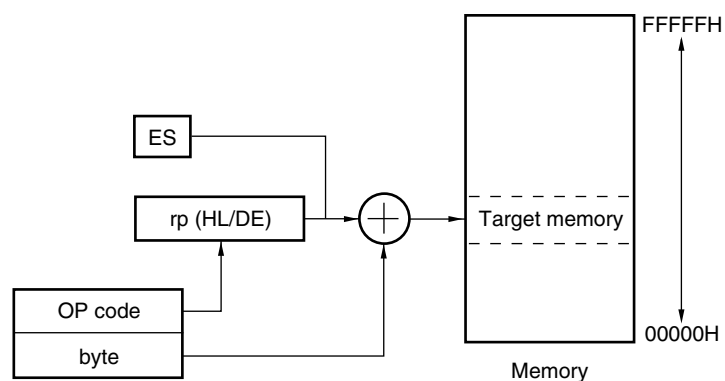


Figure 3-34. Example of ES:word[B], ES:word[C]

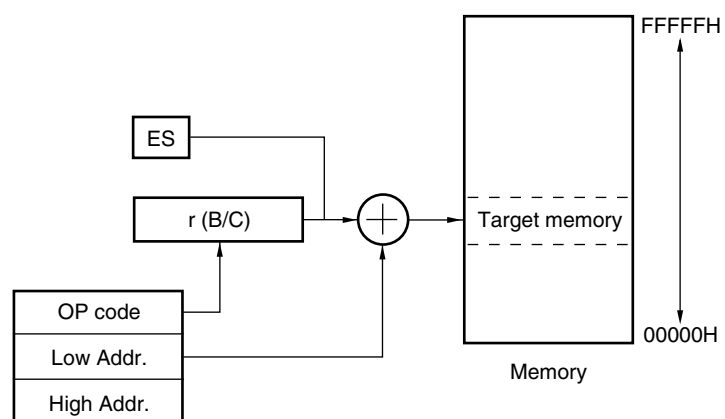
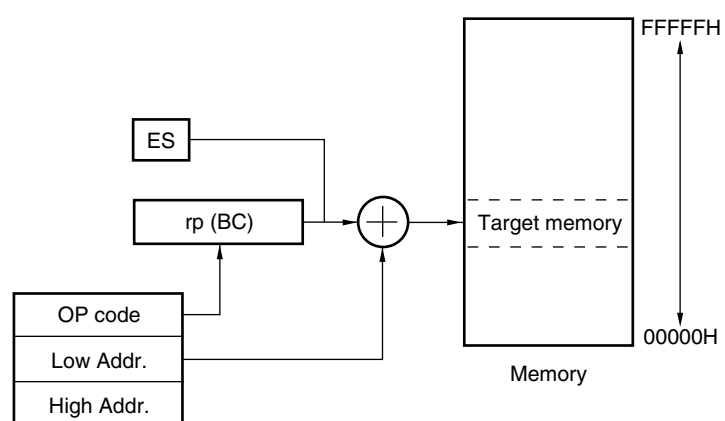


Figure 3-35. Example of ES:word[BC]



3.4.8 Based indexed addressing

[Function]

Based indexed addressing uses the contents of a register pair specified with the instruction word as the base address, and the content of the B register or C register similarly specified with the instruction word as offset address. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
–	[HL+B], [HL+C] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[HL+B], ES:[HL+C] (higher 4-bit addresses are specified by the ES register)

Figure 3-36. Example of [HL+B], [HL+C]

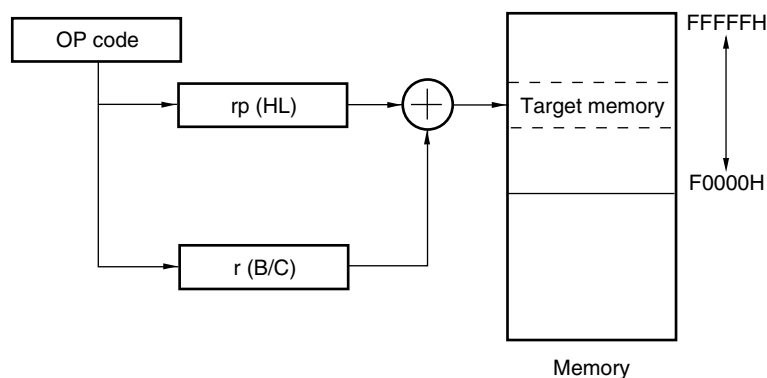
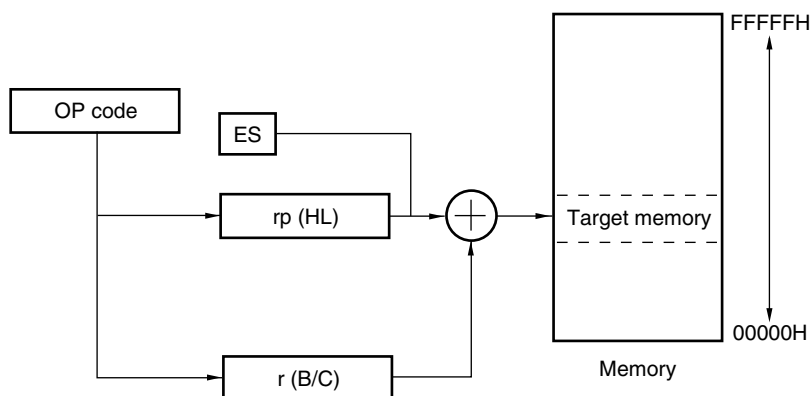


Figure 3-37. Example of ES:[HL+B], ES:[HL+C]



3.4.9 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents. This addressing is automatically employed when the PUSH, POP, subroutine call, and return instructions are executed or the register is saved/restored upon generation of an interrupt request.

Stack addressing is applied only to the internal RAM area.

[Operand format]

Identifier	Description
–	PUSH AX/BC/DE/HL POP AX/BC/DE/HL CALL/CALLT RET BRK RETB (Interrupt request generated) RETI

CHAPTER 4 PORT FUNCTIONS

4.1 Port Functions

<R> The RL78/G1A microcontrollers are provided with digital I/O ports, which enable variety of control operations.

In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS**.

4.2 Port Configuration

Ports include the following hardware.

Table 4-1. Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0 to PM7, PM12, PM14, PM15) Port registers (P0 to P7, P12 to P15) Pull-up resistor option registers (PU0, PU1, PU3 to PU5, PU7, PU12, PU14) Port input mode registers (PIM0, PIM1) Port output mode registers (POM0, POM1, POM5, POM7) Port mode control registers (PMC0, PMC1, PMC3 to PMC5, PMC7, PMC12) A/D port configuration register (ADPC) Peripheral I/O redirection register (PIOR) Global digital input disable register (GDIDIS) Global analog input disable register (GAIDIS)
Port	• 25-pin products Total: 19 (CMOS I/O: 14, CMOS input: 3, N-ch open drain I/O: 2) • 32-pin products Total: 26 (CMOS I/O: 20, CMOS input: 3, N-ch open drain I/O: 3) • 48-pin products Total: 42 (CMOS I/O: 32, CMOS input: 5, CMOS output: 1, N-ch open drain I/O: 4) • 64-pin products Total: 56 (CMOS I/O: 46, CMOS input: 5, CMOS output: 1, N-ch open drain I/O: 4)
Pull-up resistor	• 25-pin products Total: 10 • 32-pin products Total: 16 • 48-pin products Total: 23 • 64-pin products Total: 32

Caution Most of the following descriptions in this chapter use the 64-pin products with the 00H setting in peripheral I/O redirection register (PIOR) as an example.

4.2.1 Port 0

Port 0 is an I/O port with an output latch. Port 0 can be set to the input mode or output mode in 1-bit units using port mode register 0 (PM0). When the P00 to P06 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 0 (PU0).

Input to the P00, P01, P03 and P04 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 0 (PIM0).

Output from the P02 to P04 pins can be specified as N-ch open-drain output (V_{DD} tolerance^{Note 1}/ EV_{DD} tolerance^{Note 2}) in 1-bit units using port output mode register 0 (POM0).

Input to the P02 and P03 pins can be specified as analog input or digital input in 1-bit units, using port mode control register 0 (PMC0).

This port can also be used for timer I/O, A/D converter analog input, serial interface data I/O, clock I/O, and key interrupt input.

When reset signal is generated, the following configuration will be set.

- P00, P01 and P04 to P06 pins ... Input mode
- P02 and P03 pins ... Analog input

Notes 1. When 25- to 48-pin products

2. When 64-pin products

Table 4-2. Settings of Registers When Using Port 0

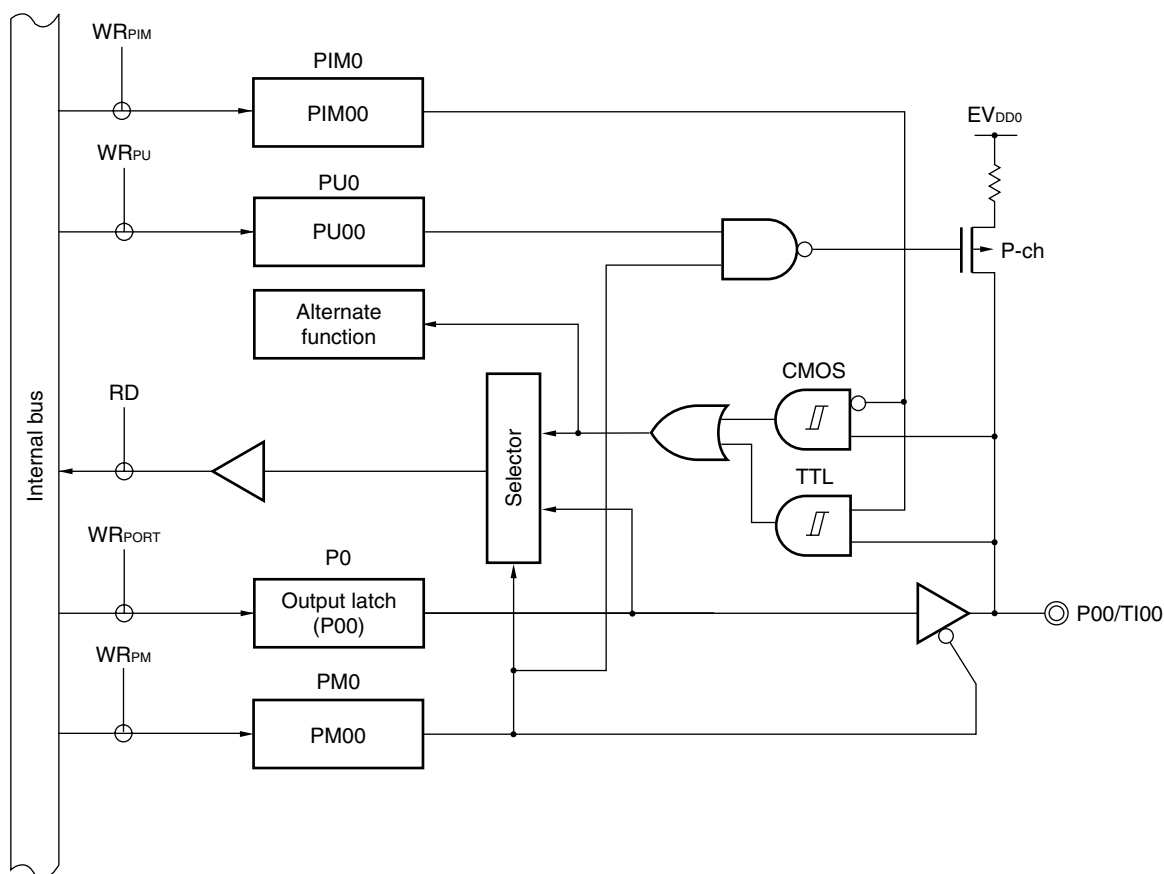
Name	I/O	PM0×	PIM0×	POM0×	PMC0×	Alternate Function Setting	Remark
P00	Input	1	0	–	–	×	CMOS input
		0	1			×	TTL input
	Output	0	×			×	
P01	Input	1	0	–	–	×	CMOS input
		1	1			×	TTL input
	Output	0	×			TO00 output = 0 ^{Note 1}	
P02	Input	1	–	×	0	×	
	Output	0		0	0	SO10/TxD1 output = 1 ^{Note 2}	CMOS output
		0		1	0		N-ch O.D. output
P03	Input	1	0	×	0	×	CMOS input
		1	1	×	0	×	TTL input
	Output	0	×	0	0	SDA10 output = 1 ^{Note 2}	CMOS output
		0	×	1	0		N-ch O.D. output
P04	Input	1	0	×	–	×	CMOS input
		1	1	×		×	TTL input
	Output	0	×	0		SCK10/SCL10 output = 1 ^{Note 2}	CMOS output
		0	×	1			N-ch O.D. output
P05, P06	Input	1	–	–	–	×	
	Output	0				TO05 output, TO06 output = 0	

- Notes 1.** To use P01/TO00, P05/TI05/TO05/KR8, P06/TI06/TO06/KR9 as a general-purpose port, set bits 0, 5, 6 (TO00, TO05, TO06) of timer output register 0 (TO0) and bits 0, 5, 6 (TOE00, TOE05, TOE06) of timer output enable register 0 (TOE0) to “0”, which is the same as their default status setting.
- 2.** To use P02/SO10/TxD1/ANI17, P03/SI10/RxD1/SDA10/ANI16, or P04/SCK10/SCL10 as a general-purpose port, set serial channel enable status register 0 (SE0), serial output register 0 (SO0) and serial output enable register 0 (SOE0) to the default status.

Remark ×: don't care
 PM0×: Port mode register 0
 PIM0×: Port input mode register 0
 POM0×: Port output mode register 0
 PMC0×: Port mode control register 0

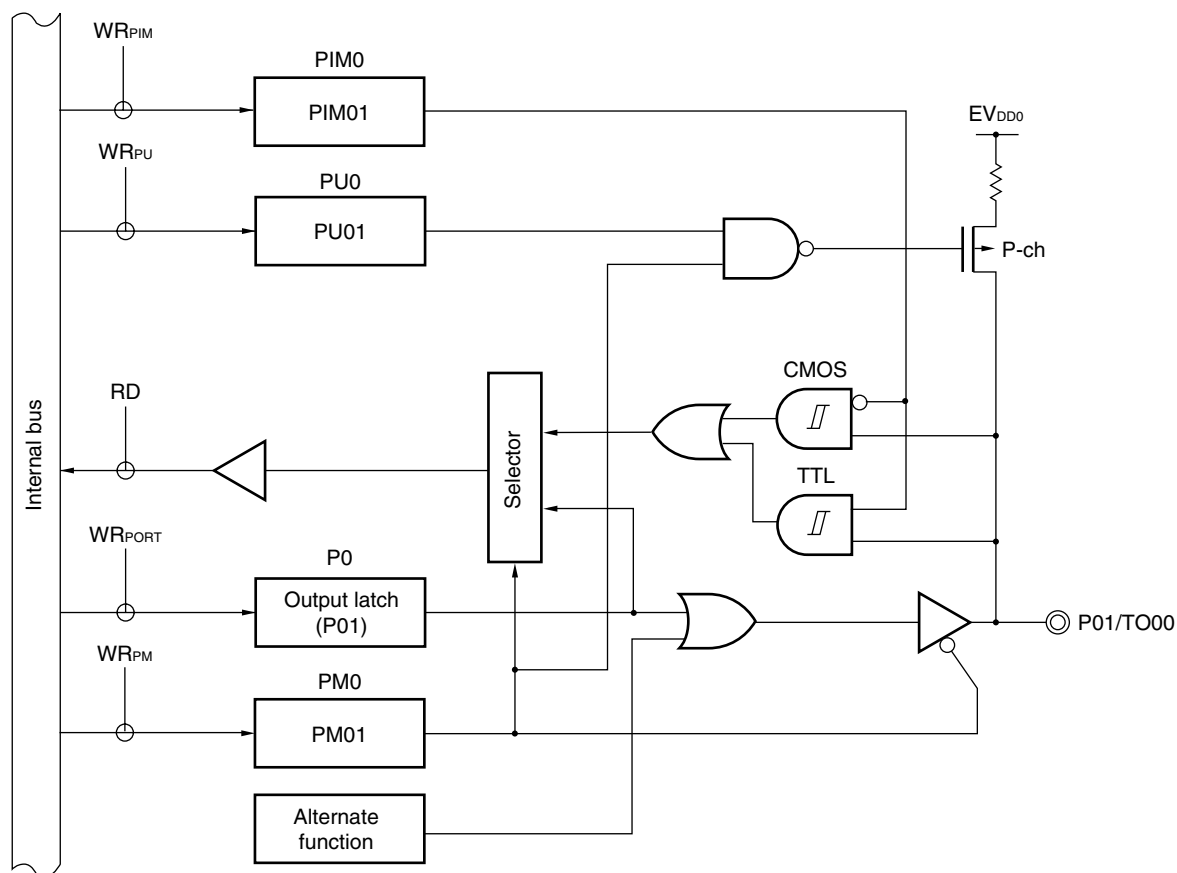
For example, figures 4-1 to 4-6 show block diagrams of port 0 for 64-pin products when PIOR = 00H.

Figure 4-1. Block Diagram of P00



- P0: Port register 0
- PU0: Pull-up resistor option register 0
- PM0: Port mode register 0
- PIM0: Port input mode register 0
- RD: Read signal
- WR_{xx} : Write signal

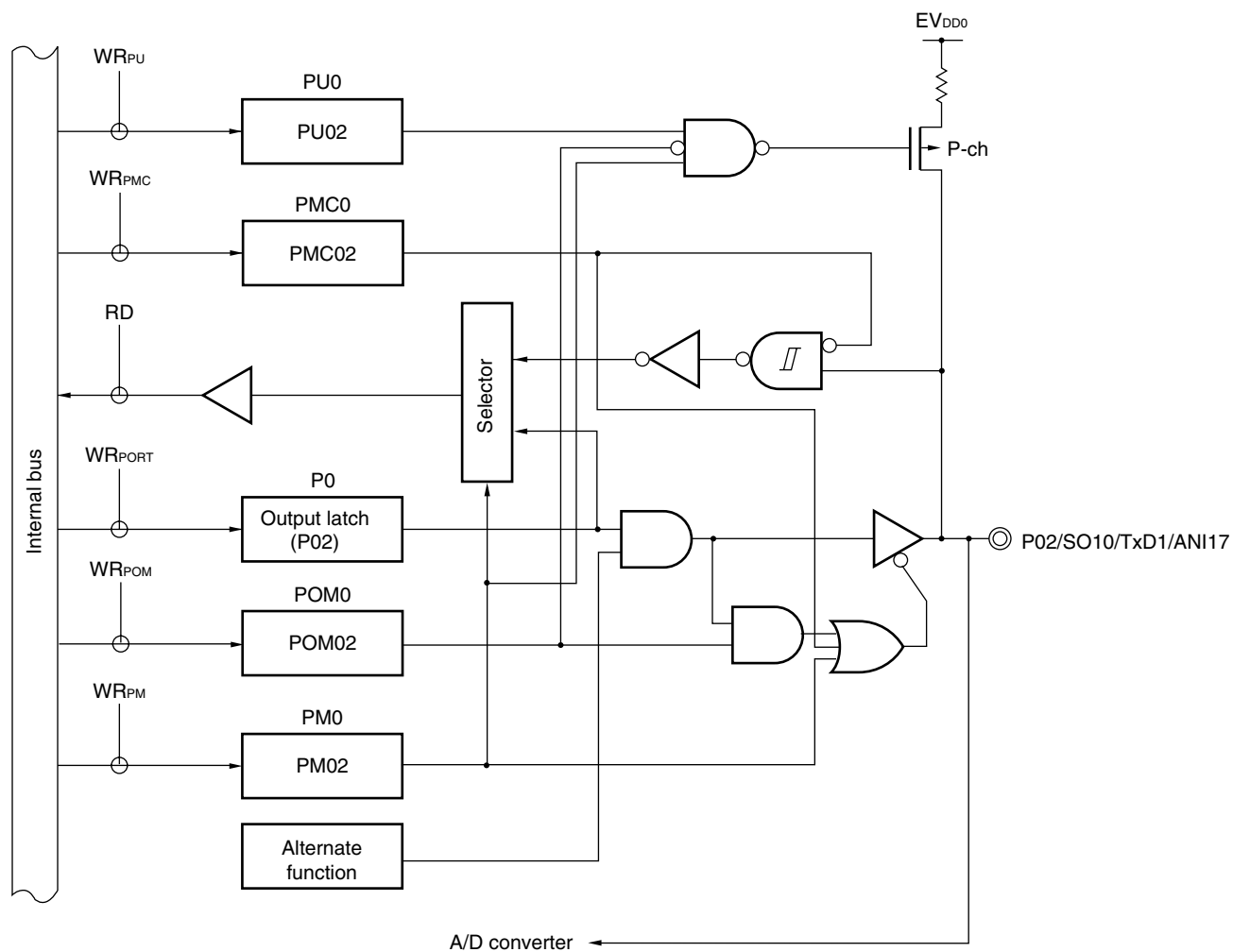
Figure 4-2. Block Diagram of P01



P0: Port register 0
 PU0: Pull-up resistor option register 0
 PM0: Port mode register 0
 PIM0: Port input mode register 0
 RD: Read signal
 WR_{xx} : Write signal

<R>

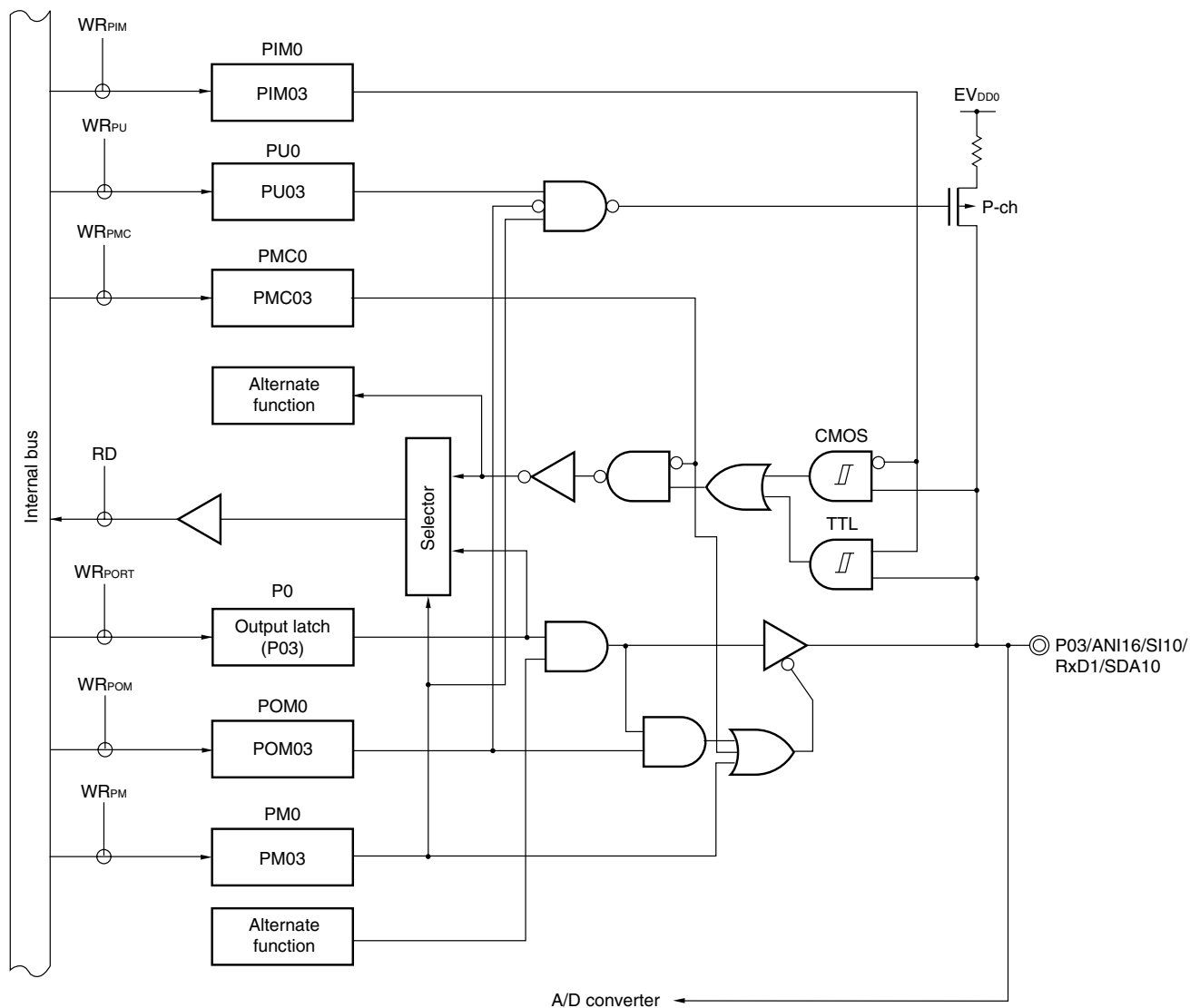
Figure 4-3. Block Diagram of P02



P0: Port register 0
 PU0: Pull-up resistor option register 0
 PM0: Port mode register 0
 POM0: Port output mode register 0
 PMC0: Port mode control register 0
 RD: Read signal
 WR_{xx}: Write signal

<R>

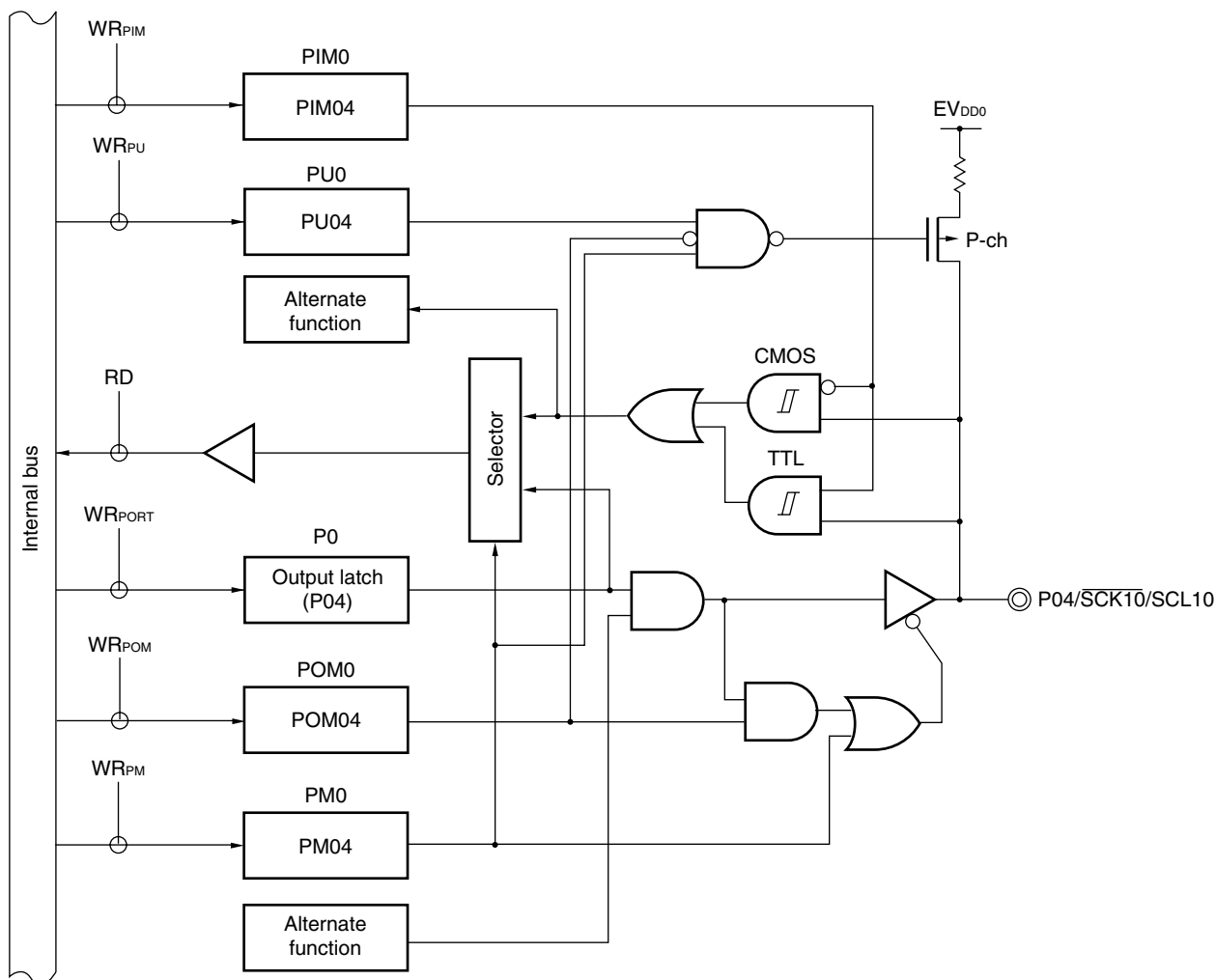
Figure 4-4. Block Diagram of P03



P0: Port register 0
 PU0: Pull-up resistor option register 0
 PM0: Port mode register 0
 PIM0: Port input mode register 0
 POM0: Port output mode register 0
 PMC0: Port mode control register 0
 RD: Read signal
 WR_{xx}: Write signal

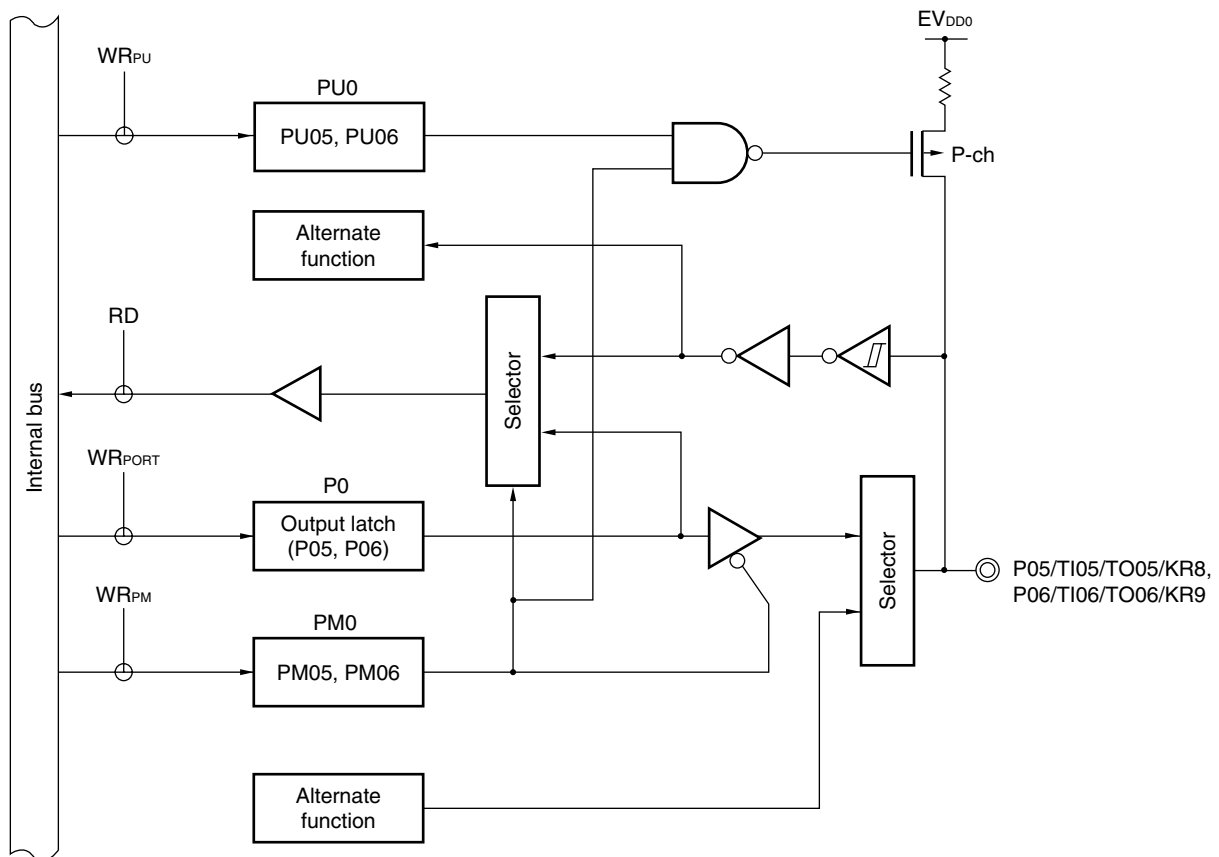
<R>

Figure 4-5. Block Diagram of P04



P0: Port register 0
 PU0: Pull-up resistor option register 0
 PM0: Port mode register 0
 PIM0: Port input mode register 0
 POM0: Port output mode register 0
 RD: Read signal
 WR_{xx}: Write signal

Figure 4-6. Block Diagram of P05, P01



P0: Port register 0
 PU0: Pull-up resistor option register 0
 PM0: Port mode register 0
 RD: Read signal
 WR_{xx}: Write signal

4.2.2 Port 1

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P16 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

Input to the P10, P11, and P14 to P16 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 1 (PIM1).

Output from the P10 to P15 pins can be specified as N-ch open-drain output (V_{DD} tolerance^{Note 1}/ EV_{DD} tolerance^{Note 2}) in 1-bit units using port output mode register 1 (POM1).

When the P10 to P15 pins are used as input, specify them as either digital or analog in Port mode control register 1 (PMC1). This register can be specified in 1-bit unit.

This port can also be used for A/D converter analog input, serial interface data I/O, clock I/O, programming UART I/O, timer I/O, and external interrupt request input.

When reset signal is generated, the following configuration will be set.

- P10 to P15 pins ... Analog input
- P16 pin ... Input mode

Notes 1. When 25- to 48-pin products

2. When 64-pin products

Table 4-3. Settings of Registers When Using Port 1

Name	I/O	PM1×	PIM1×	POM1×	PMC×	Alternate Function Setting	Remark
P10	Input	1	0	×	0	×	CMOS input
		1	1	×	0	×	TTL input
	Output	0	×	0	0	$\overline{\text{SCK00/SCL00}}$ output = 1 ^{Note 1}	CMOS output
		0	×	1	0		N-ch O.D. output
P11	Input	1	0	×	0	×	CMOS input
		1	1	×	0	×	TTL input
	Output	0	×	0	0	SDA00 output = 1 ^{Note 1}	CMOS output
		0	×	1	0		N-ch O.D. output
P12	Input	1	—	×	0	×	CMOS input
	Output	0		0	0	SO00/TxD1 output = 1 ^{Note 1}	CMOS output
		0		1	0		N-ch O.D. output
P13	Input	1	—	×	0	×	CMOS input
	Output	0		0	0	TxD2/SO20 output = 1 ^{Note 1}	CMOS output
		0		1	0		N-ch O.D. output
P14	Input	1	0	×	0	×	CMOS input
		1	1	×	0	×	TTL input
	Output	0	×	0	0	SDA20 output = 1 ^{Note 1}	CMOS output
		0	×	1	0		N-ch O.D. output
P15	Input	1	0	×	0	×	CMOS input
		1	1	×	0	×	TTL input
	Output	0	×	0	0	$\overline{\text{SCK20/SCL20}}$ output = 1 ^{Note 1}	CMOS output
		0	×	1	0		N-ch O.D. output
P16	Input	1	0	—	—	×	CMOS input
		1	1			×	TTL input
	Output	0	×			TO01 output = 0 ^{Note 2}	

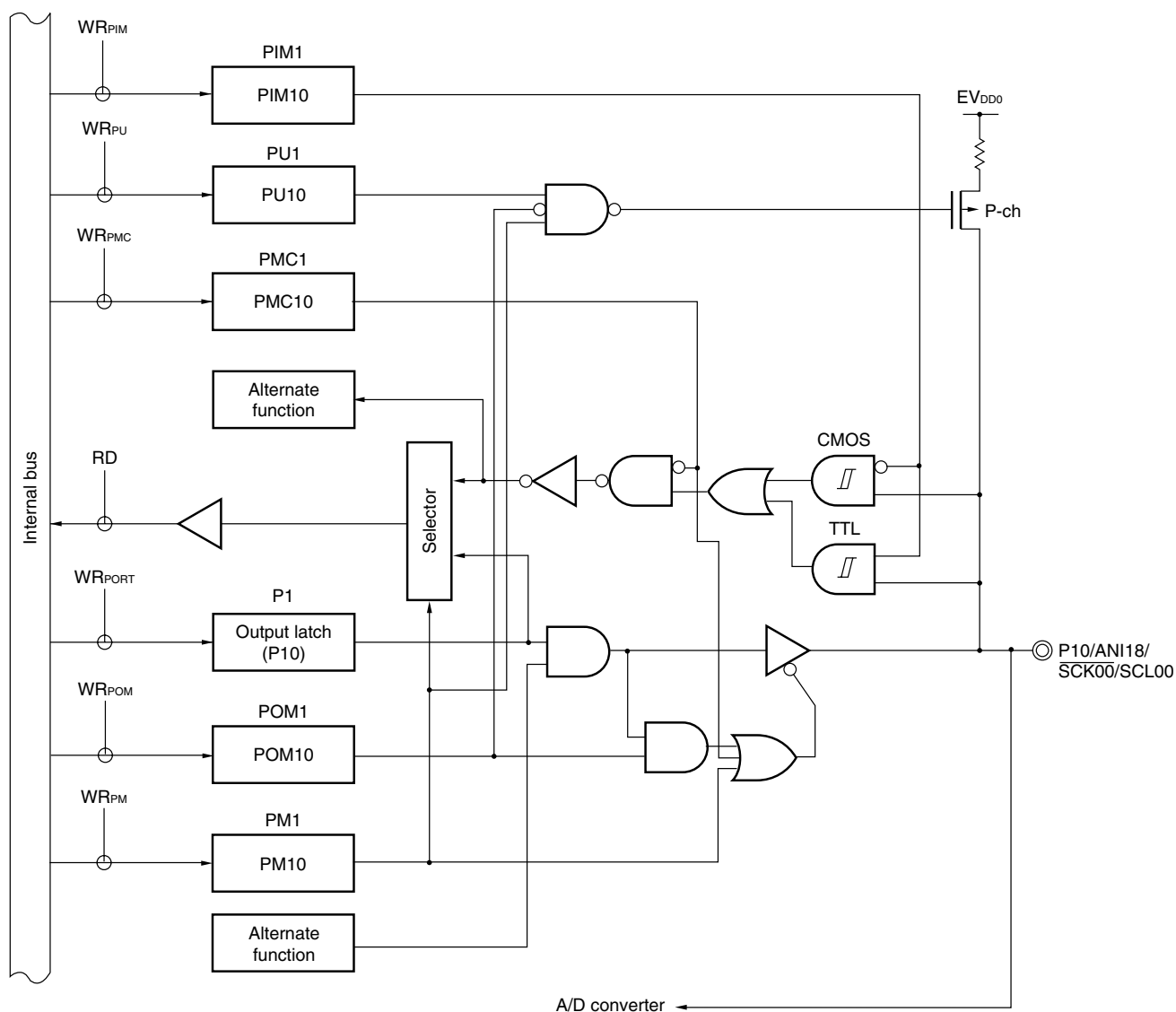
- Notes 1.** P10/ANI18/ $\overline{\text{SCK00/SCL00}}$, P11/ANI20/SI00/RxD0/TOOLRxD/SDA00, P12/ANI21/SO00/TxD0/TOOLTxD, P13/ANI22/TxD2/SO20, P14/ANI23/RxD2/SI20/SDA20, or P15/ANI24/ $\overline{\text{SCK20/SCL20}}$ as a general-purpose port, set serial channel enable status register m (SEm), serial output register m (SOM) and serial output enable register m (SOEm) to the default status (m = 0, 1).
- 2.** To use P16/TI01/TO01/INTP5 as a general-purpose port, set bit 1 (TO01) of timer output register 0 (TO0) and bit 1 (TOE01) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

Remark ×: don't care
 PM1×: Port mode register 1
 PIM1×: Port input mode register 1
 POM1×: Port output mode register 1
 PMC1×: Port mode control register 1

For example, figures 4-7 to 4-13 show block diagrams of port 1 for 64-pin products when PIOR = 00H.

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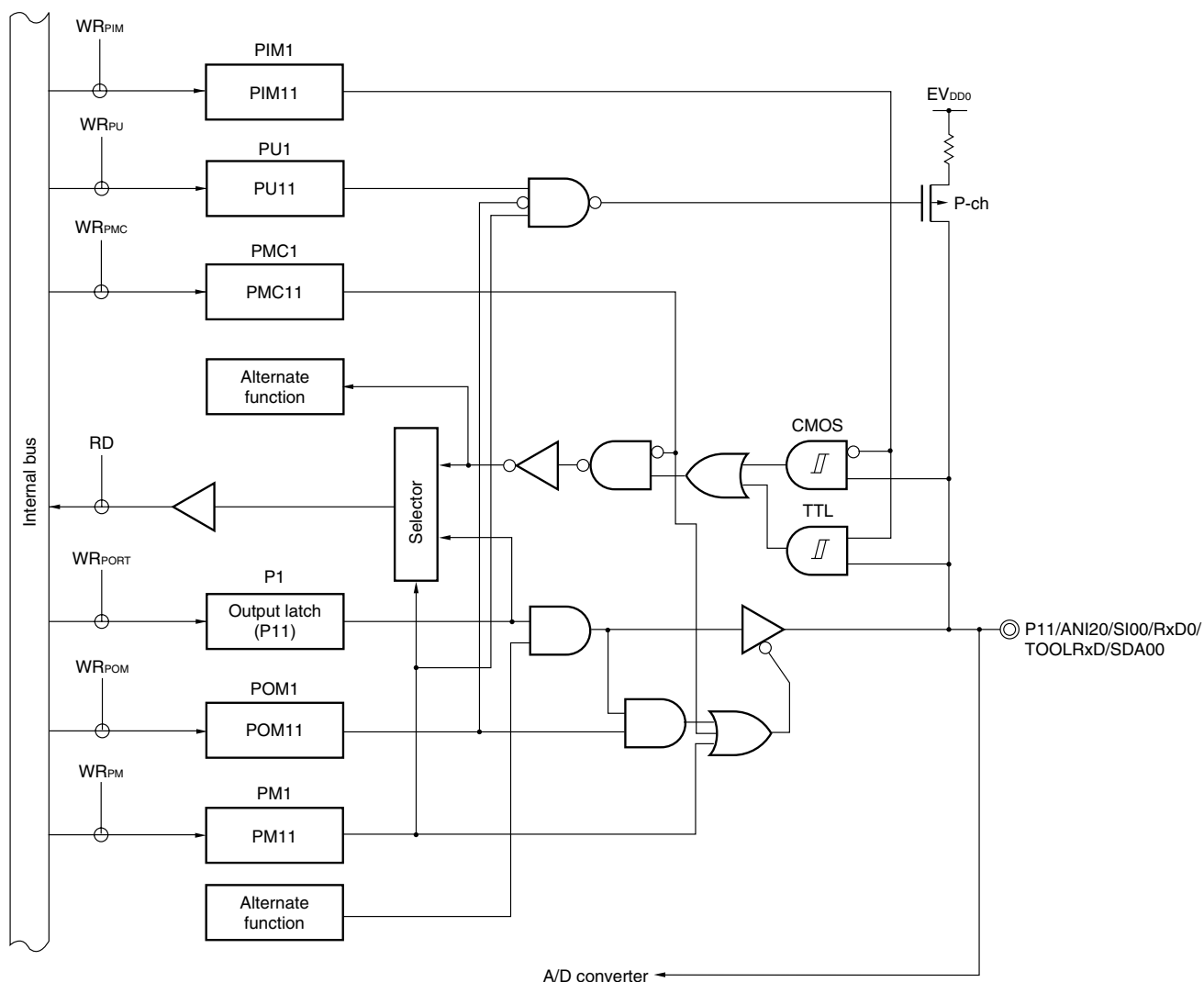
Figure 4-7. Block Diagram of P10



- P1: Port register 1
- PU1: Pull-up resistor option register 1
- PM1: Port mode register 1
- PIM1: Port input mode register 1
- POM1: Port output mode register 1
- PMC1: Port mode control register 1
- RD: Read signal
- WR_{xx} : Write signal

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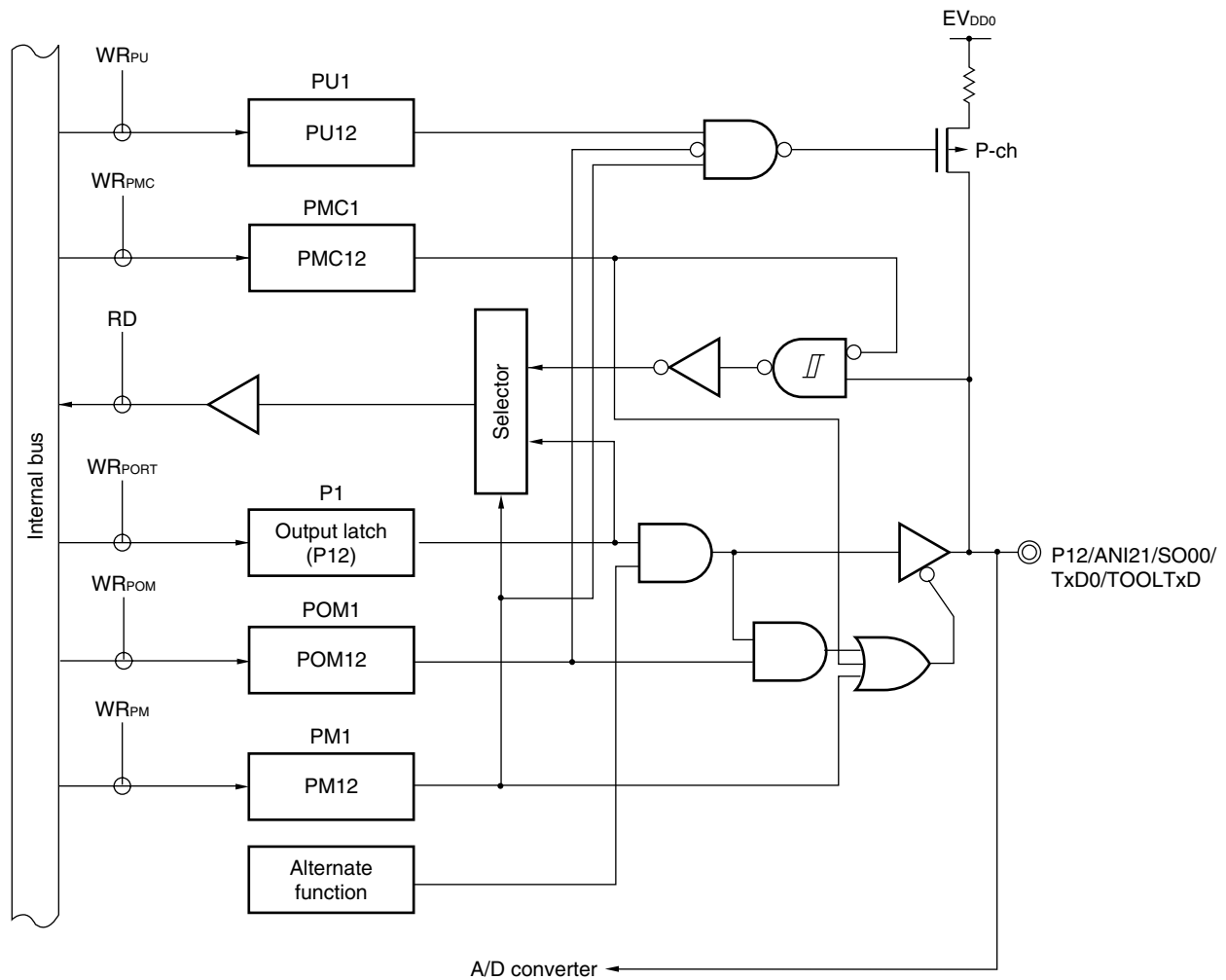
Figure 4-8. Block Diagram of P11



- P1: Port register 1
 PU1: Pull-up resistor option register 1
 PM1: Port mode register 1
 PIM1: Port input mode register 1
 POM1: Port output mode register 1
 PMC1: Port mode control register 1
 RD: Read signal
 WR_{xx} : Write signal

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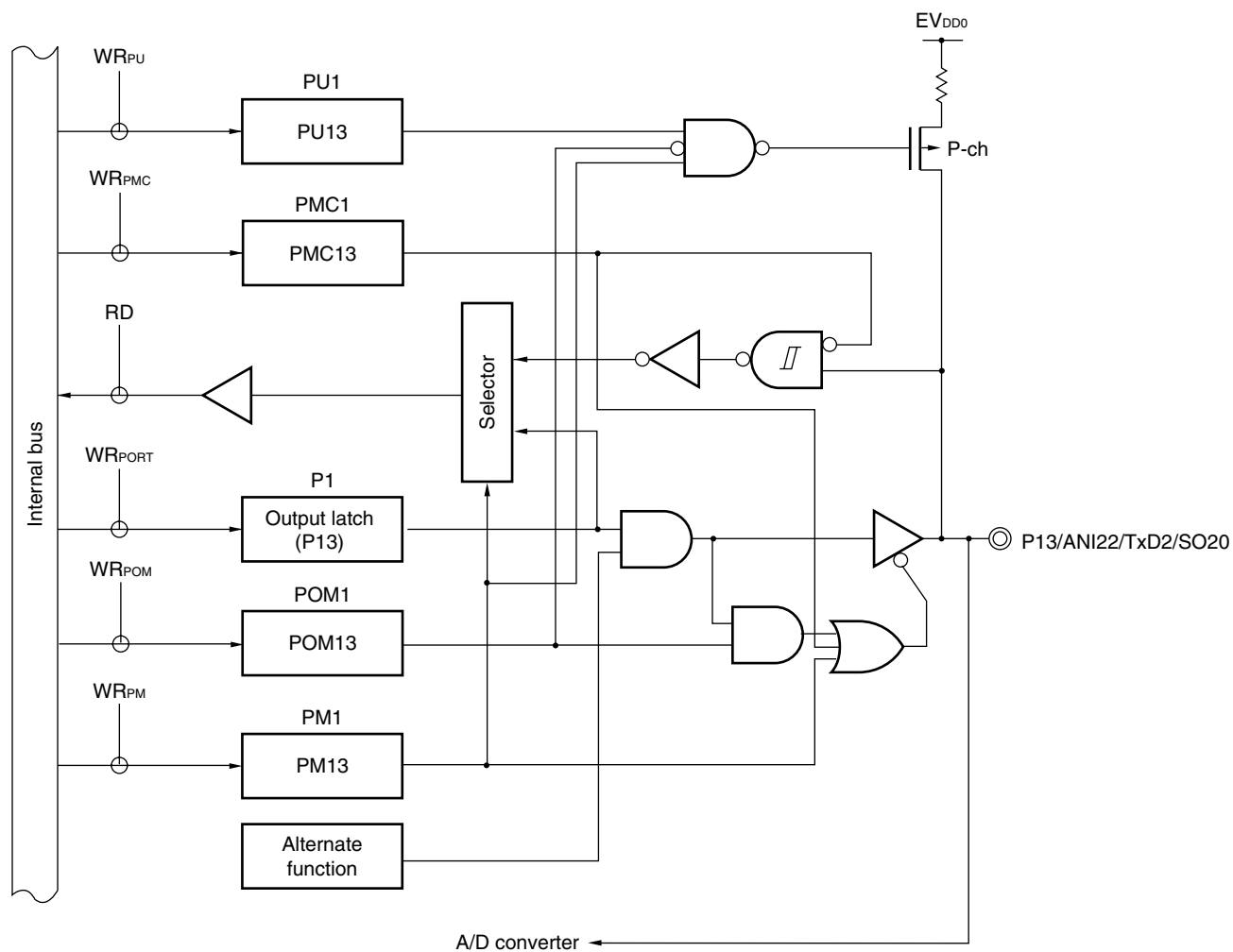
Figure 4-9. Block Diagram of P12



P1:	Port register 1
PU1:	Pull-up resistor option register 1
PM1:	Port mode register 1
POM1:	Port output mode register 1
PMC1:	Port mode control register 1
RD:	Read signal
WR _{xx} :	Write signal

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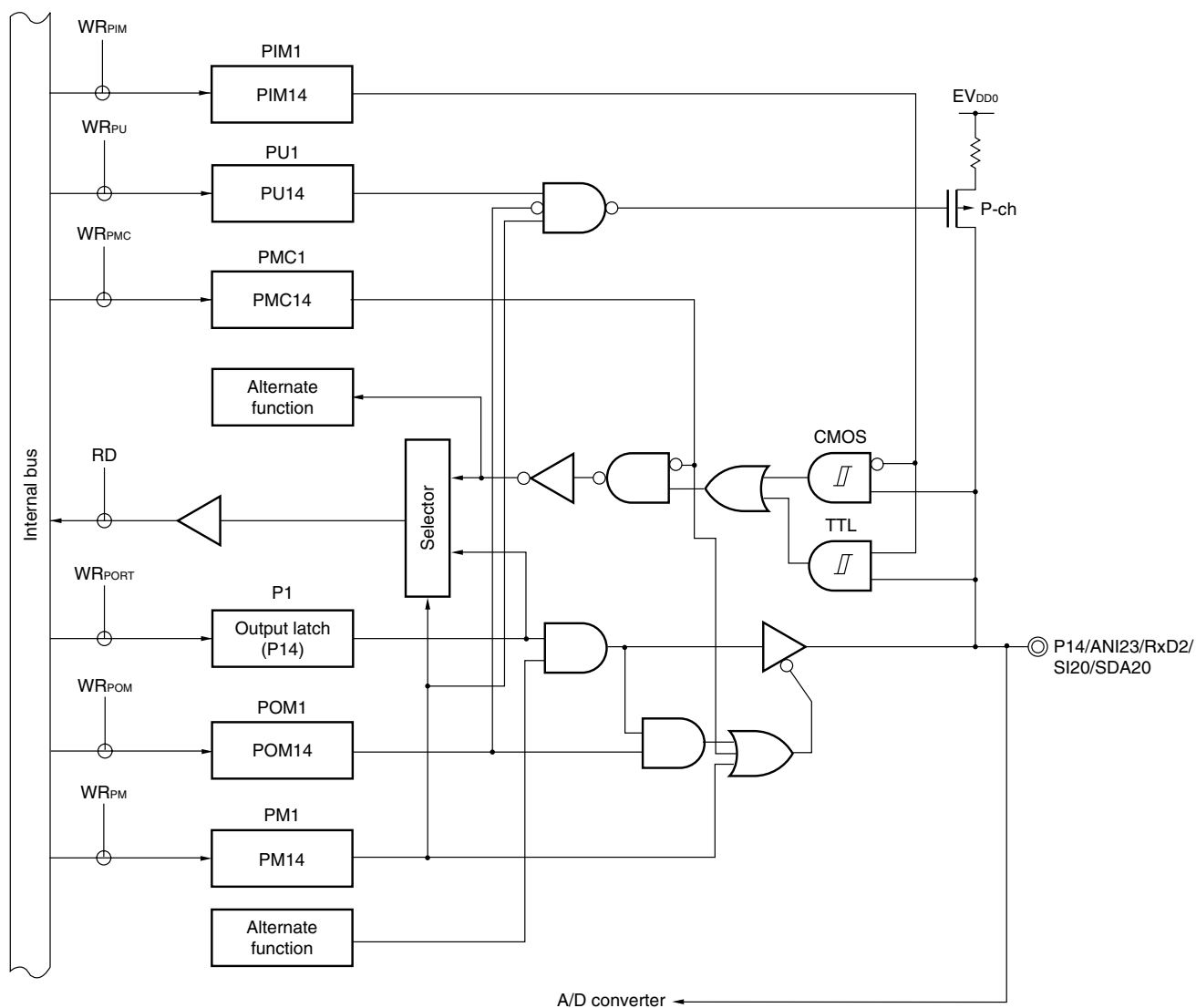
Figure 4-10. Block Diagram of P13



- P1: Port register 1
 PU1: Pull-up resistor option register 1
 PM1: Port mode register 1
 POM1: Port output mode register 1
 PMC1: Port mode control register 1
 RD: Read signal
 WR_{xx} : Write signal

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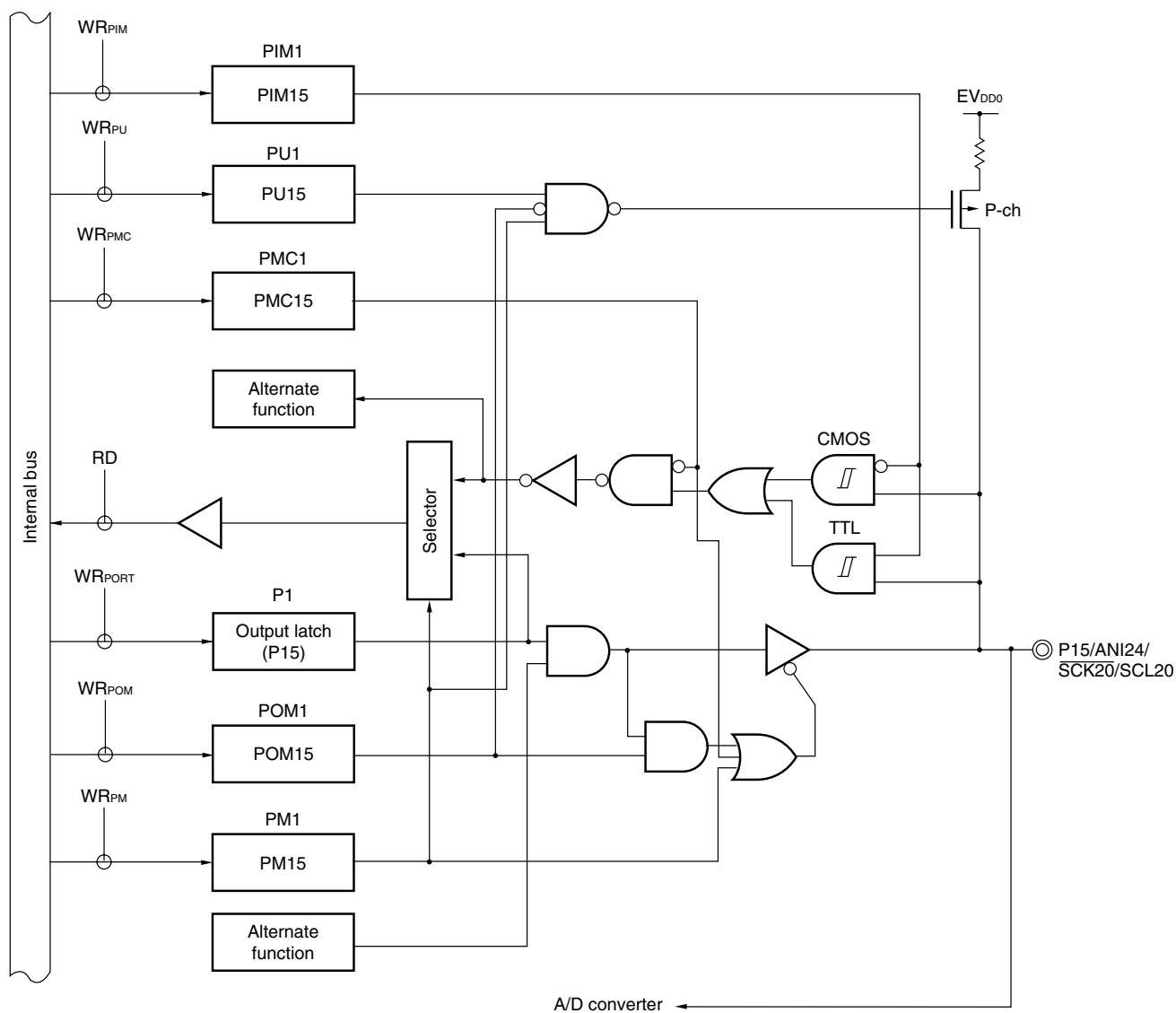
Figure 4-11. Block Diagram of P14



- P1: Port register 1
 PU1: Pull-up resistor option register 1
 PM1: Port mode register 1
 PIM1: Port input mode register 1
 POM1: Port output mode register 1
 PMC1: Port mode control register 1
 RD: Read signal
 WR_{xx} : Write signal

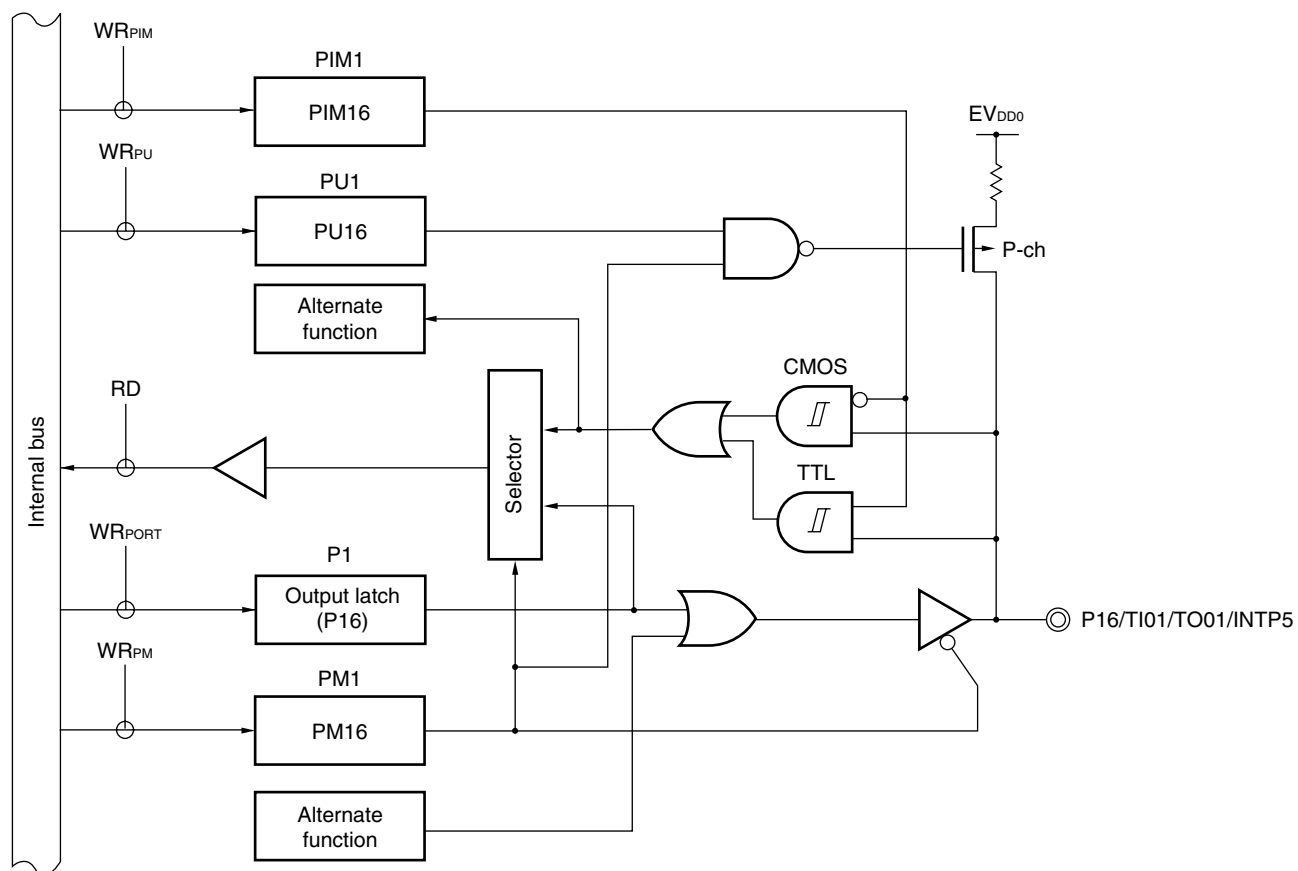
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Figure 4-12. Block Diagram of P15



- P1: Port register 1
 PU1: Pull-up resistor option register 1
 PM1: Port mode register 1
 PIM1: Port input mode register 1
 POM1: Port output mode register 1
 PMC1: Port mode control register 1
 RD: Read signal
 WR_{xx} : Write signal

Figure 4-13. Block Diagram of P16



- P1: Port register 1
 PU1: Pull-up resistor option register 1
 PM1: Port mode register 1
 PIM1: Port input mode register 1
 RD: Read signal
 WR_{xx} : Write signal

4.2.3 Port 2

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2).

This port can also be used for A/D converter analog input and reference voltage input.

To use P20/ANI0 to P27/ANI7 as digital input pins, set them in the digital I/O mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM2 register. Use these pins starting from the upper bit.

To use P20/ANI0 to P27/ANI7 as digital output pins, set them in the digital I/O mode by using the ADPC register and in <R> the output mode by using the PM2 register. Use these pins starting from the upper bit.

To use P20/ANI0 to P27/ANI7 as analog input pins, set them in the analog input mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM2 register. Use these pins starting from the lower bit.

Table 4-4. Settings of Registers When Using Port 2

Name	I/O	PM2 _x	ADPC	Alternate Function Setting	Remark
P2n	Input	1	01 to n+1H	—	To use P2n as a port, use these pins from a higher bit.
	Output	0	01 to n+1H		

Remark ×: don't care
 PM2_x: Port mode register 2
 ADPC: A/D port configuration register

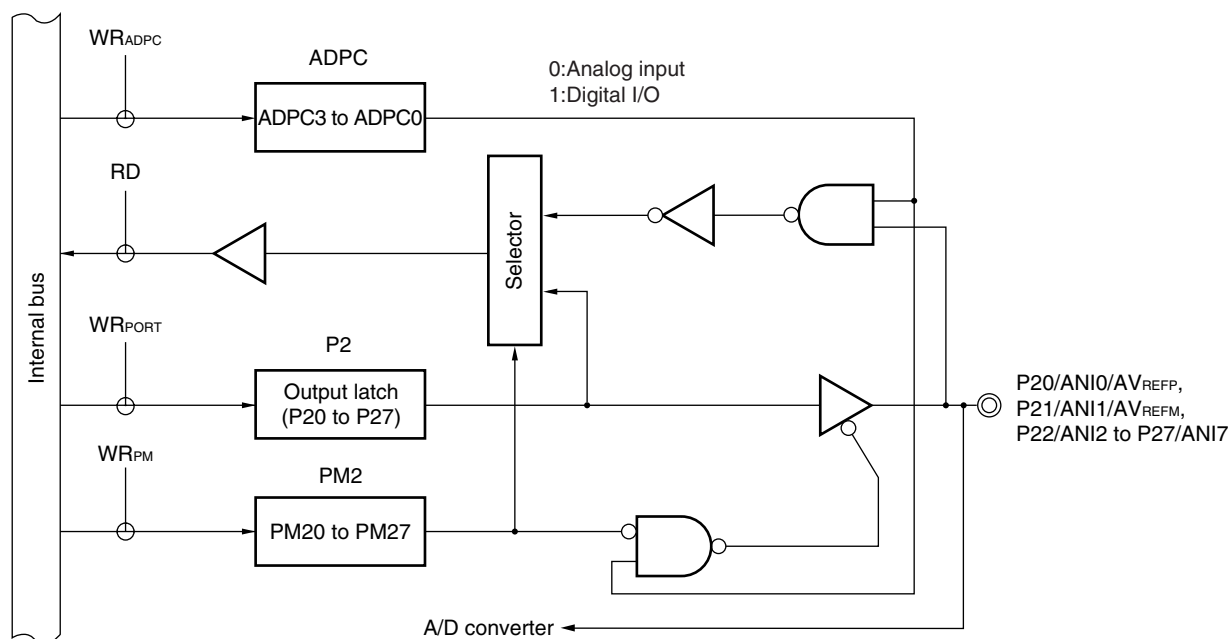
Table 4-5. Setting Functions of P20/ANI0 to P27/ANI7 Pins

ADPC Register	PM2 Register	ADS Register	P20/ANI0 to P27/ANI7 Pins
Digital I/O selection	Input mode	—	Digital input
	Output mode	—	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

All P20/ANI0 to P27/ANI7 are set in the analog input mode when the reset signal is generated.

For example, figure 4-14 shows a block diagram of port 2 for 64-pin products when PIOR = 00H.

Figure 4-14. Block Diagram of P20 to P27



ADPC: A/D port configuration register

P2: Port register 2

PM2: Port mode register 2

RD: Read signal

WR_{xx}: Write signal

4.2.4 Port 3

Port 3 is an I/O port with an output latch. Port 3 can be set to the input mode or output mode in 1-bit units using port mode register 3 (PM3). When the P30, P31 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 3 (PU3).

Input to the P30, P31 pins can be specified as analog input or digital input in 1-bit units, using port mode control register 3 (PMC3).

This port can also be used for A/D converter analog input, external interrupt request input, real-time clock correction clock output, serial interface data I/O, clock I/O, and timer I/O.

Reset signal generation sets P30, P31 to analog input.

Table 4-6. Settings of Registers When Using Port 3

Name	I/O	PM3×	PMC3×	Alternate Function Setting	Remark
P30	Input	1	0	×	
	Output	0	0	RTC1HZ output = 0 ^{Note 1} SCK11/SCL11 output = 0 ^{Note 2}	
P31	Input	1	0	×	
	Output	0	0	TO03 output = 0 ^{Note 3}	

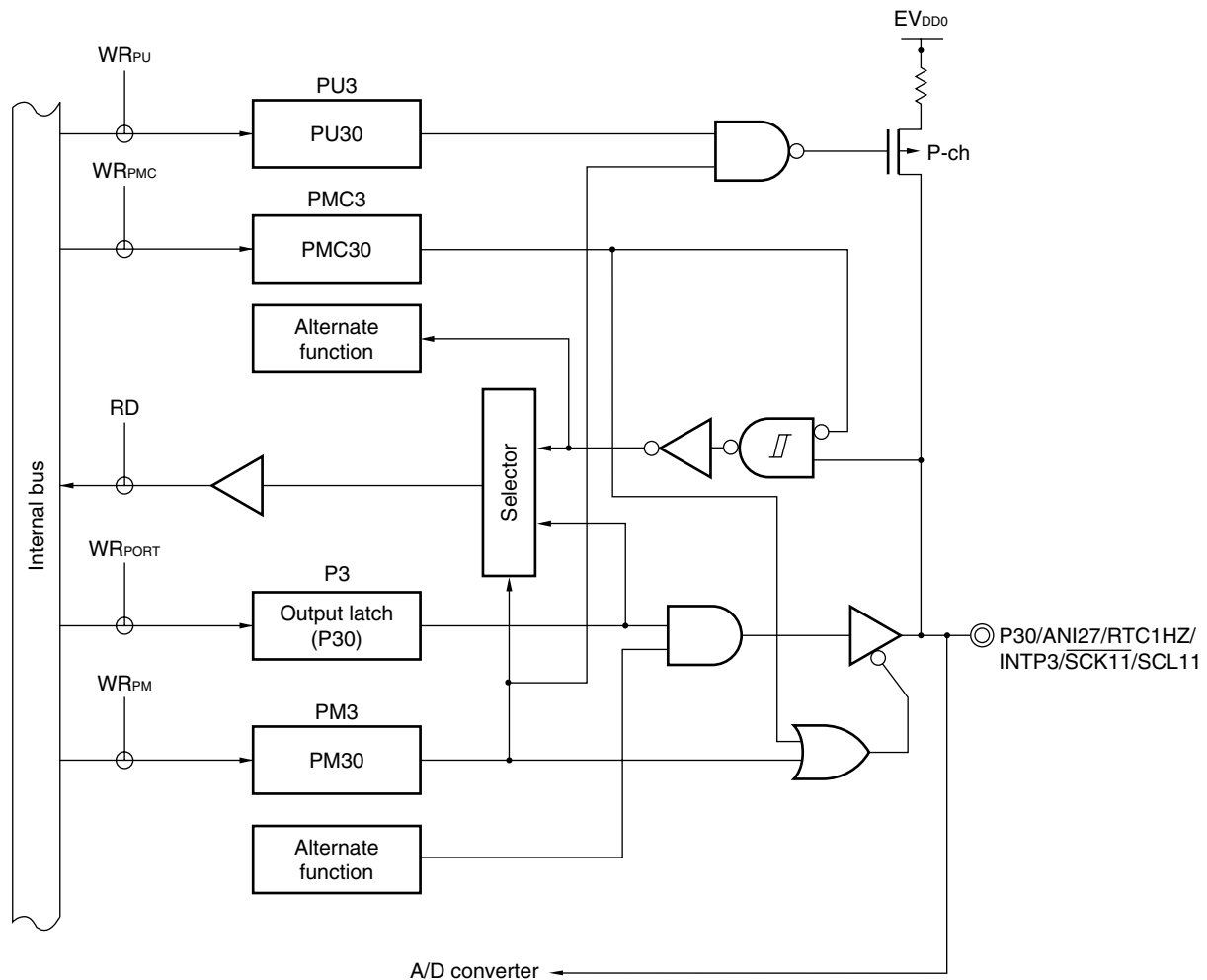
- Notes**
1. To use P30/ANI27/INTP3/RTC1HZ/SCK11/SCL11 as a general-purpose port in 48-, 64-pin products, set bit 5 (RCLOE1) of real-time clock control register 0 (RTCC0) to "0", which is the same as its default status setting.
 2. To use P30/ANI27/INTP3/RTC1HZ/SCK11/SCL11 as a general-purpose port, set serial channel enable status register 0 (SE0), serial output register 0 (SO0) and serial output enable register 0 (SOE0) to the default status.
 3. To use P31/ANI29/TI03/TO03/INTP4 as a general-purpose port, set bit 3 (TO03) of timer output register 0 (TO0) and bit 3 (TOE03) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

Remark

- ×: don't care
- PM3×: Port mode register 3
- PMC3×: Port mode control register 3

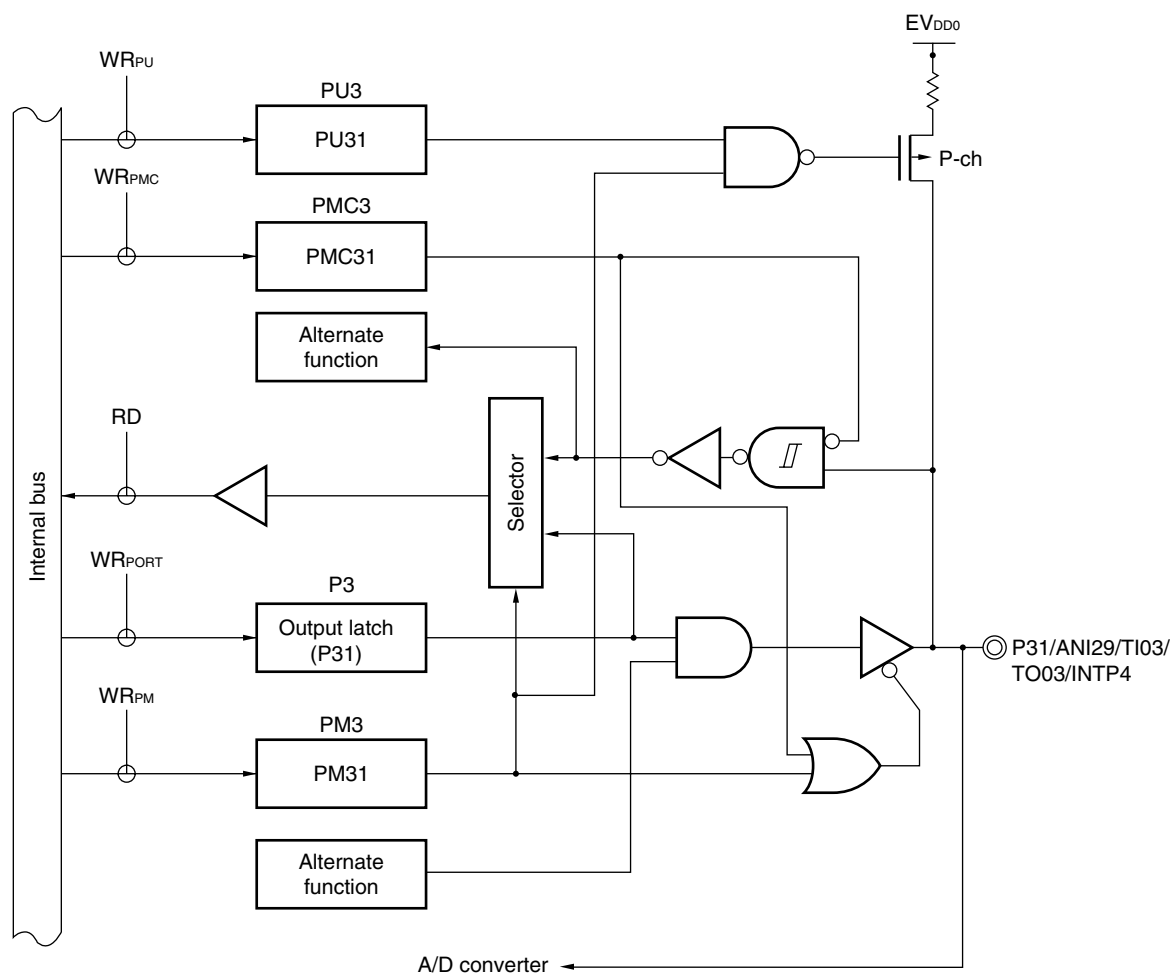
For example, figures 4-15 and 4-16 show block diagrams of port 3 for 64-pin products.

Figure 4-15. Block Diagram of P30



P3:	Port register 3
PU3:	Pull-up resistor option register 3
PM3:	Port mode register 3
PMC3:	Port mode control register 3
RD:	Read signal
WR _{xx} :	Write signal

Figure 4-16. Block Diagram of P31



- P3:** Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
PMC3: Port mode control register 3
RD: Read signal
 WR_{xx} : Write signal

4.2.5 Port 4

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P43 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 4 (PU4).

When the P40 pin is used as input, specify them as either digital or analog in Port mode control register 4 (PMC4). This register can be specified in 1-bit unit.

This port can also be used for A/D converter analog input, timer I/O, data I/O for a flash memory programmer/debugger. Reset signal generation sets port 4 to input mode.

Table 4-7. Settings of Registers When Using Port 4

Name	I/O	PM4×	PMC4×	Alternate Function Setting	Remark
P40	Input	1	—	×	
	Output	0		×	
P41	Input	1	0	×	
	Output	0	0	TO07 output = 0 ^{Note}	
P42	Input	1	—	×	
	Output	0		TO04 output = 0 ^{Note}	
P43	Input	1	—	×	
	Output	0		×	

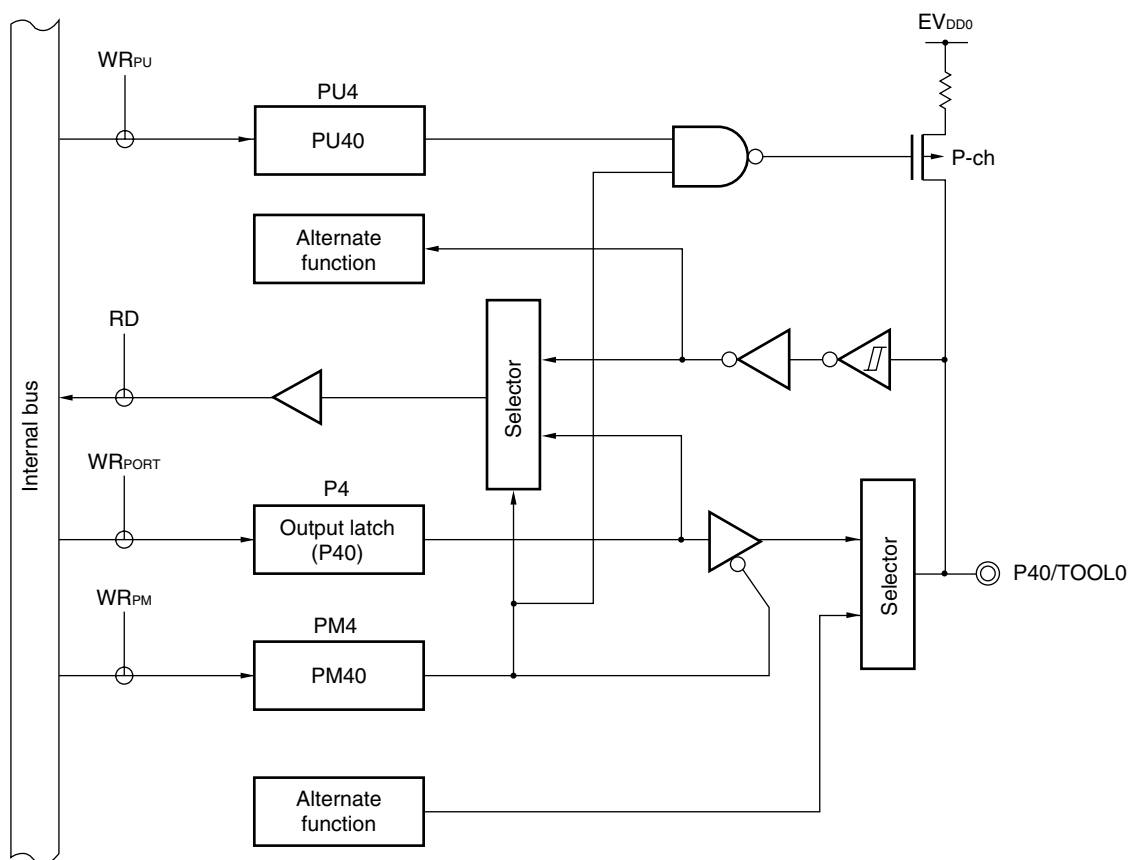
Note To use P41/ANI30/TI07/TO07 or P42/TI04/TO04 as a general-purpose port, set bits 4 and 7 (TO04, TO07) of timer output register 0 (TO0) and bits 4 and 7 (TOE04, TOE07) of timer output enable register 0 (TOE0) to “0”, which is the same as their default status setting.

Caution When a tool is connected, the P40 pin cannot be used as a port pin.

Remark ×: don't care
 PM4×: Port mode register 4
 PMC4×: Port mode control register 4

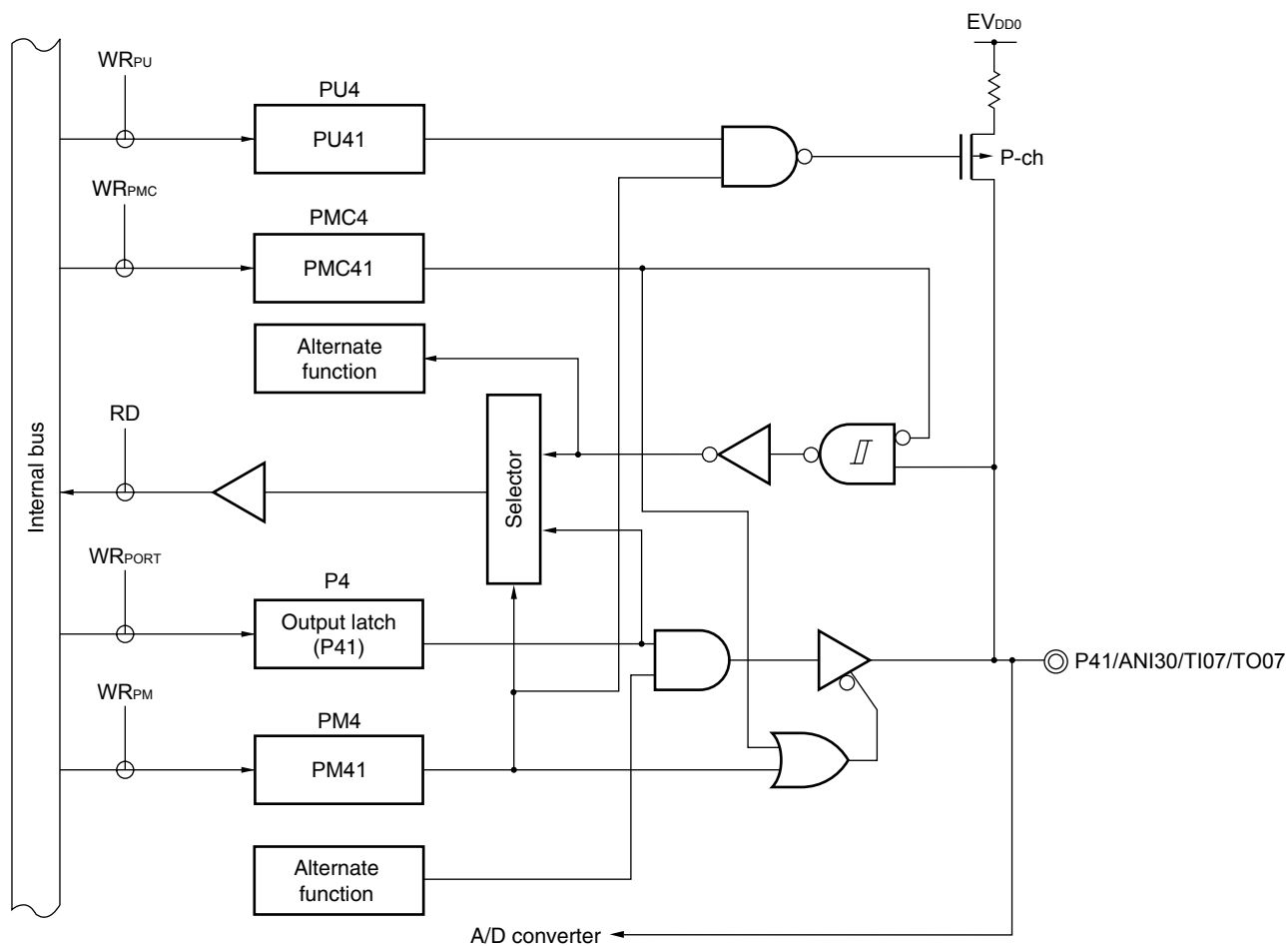
For example, figures 4-17 to 4-20 show block diagrams of port 4 for 64-pin products.

Figure 4-17. Block Diagram of P40



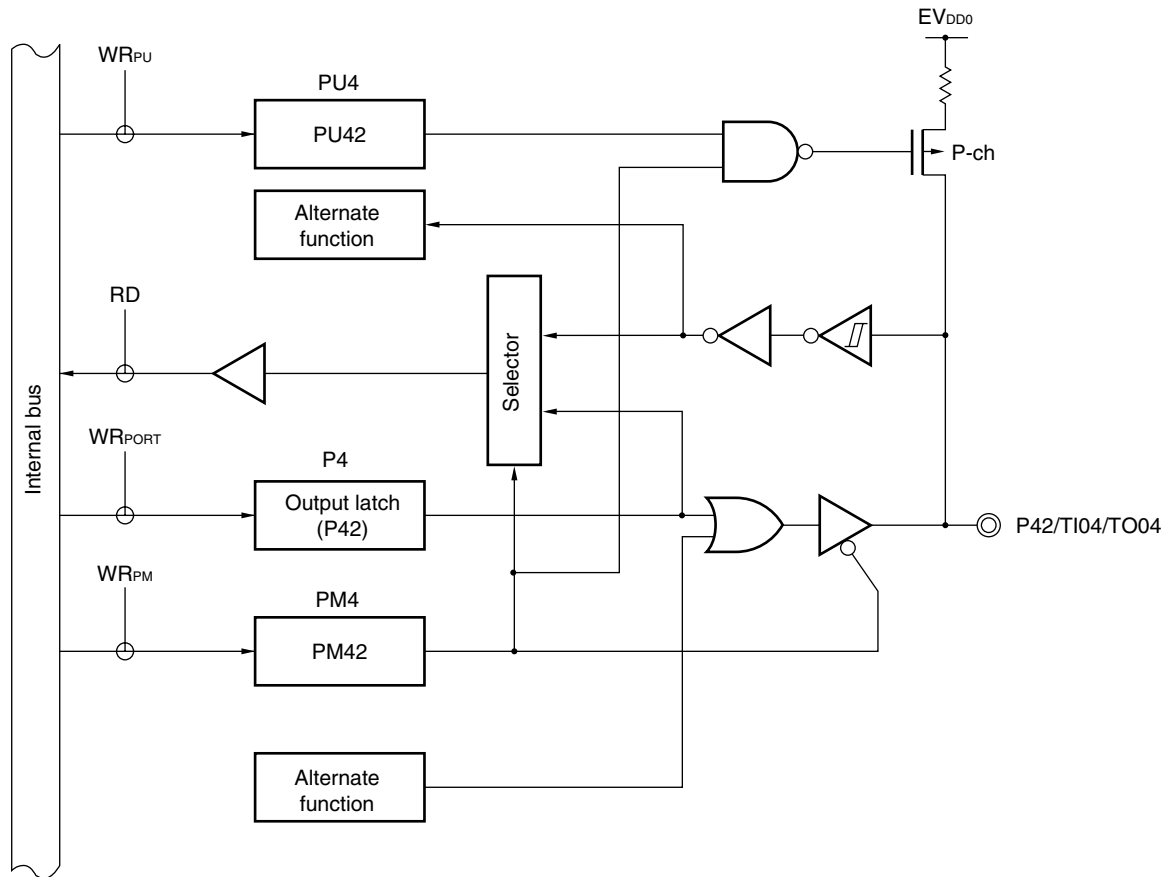
- P4: Port register 4
- PU4: Pull-up resistor option register 4
- PM4: Port mode register 4
- RD: Read signal
- WR_{xx} : Write signal

Figure 4-18. Block Diagram of P41



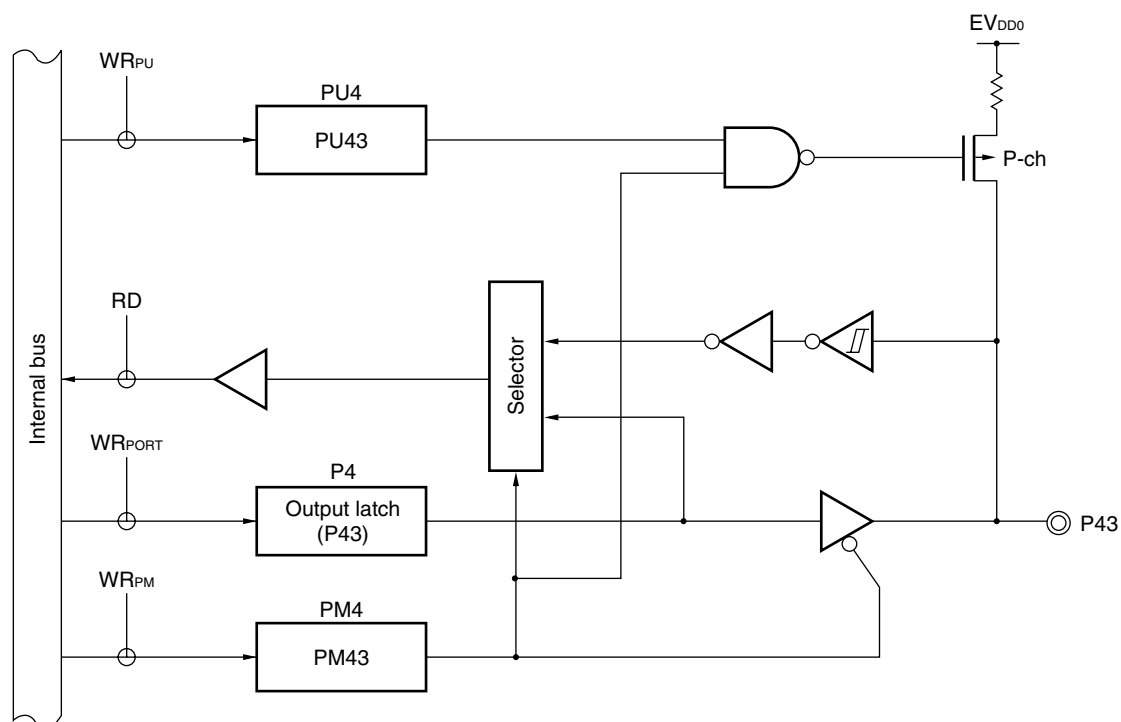
- P4: Port register 4
 PU4: Pull-up resistor option register 4
 PM4: Port mode register 4
 PMC4: Port mode control register 4
 RD: Read signal
 WR_{xx} : Write signal

Figure 4-19. Block Diagram of P42



P4:	Port register 4
PU4:	Pull-up resistor option register 4
PM4:	Port mode register 4
RD:	Read signal
WR _{xx} :	Write signal

Figure 4-20. Block Diagram of P43



P4: Port register 4
 PU4: Pull-up resistor option register 4
 PM4: Port mode register 4
 RD: Read signal
 WR_{xx} : Write signal

4.2.6 Port 5

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units using port mode register 5 (PM5). When the P50, P51 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

Output from the P50 pin can be specified as N-ch open-drain output (V_{DD} tolerance^{Note 1}/ EV_{DD} tolerance^{Note 2}) in 1-bit units using port output mode register 5 (POM5).

When the P50 pin is used as input, specify them as either digital or analog in Port mode control register 5 (PMC5). This register can be specified in 1-bit unit.

This port can also be used for A/D converter analog input, external interrupt request input, serial interface data I/O.

Reset signal generation sets port 5 to input mode.

Notes 1. When 25- to 48-pin products

2. When 64-pin products

Table 4-8. Settings of Registers When Using Port 5

Name	I/O	PM5×	POM5×	PMC5×	Alternate Function Setting	Remark
P50	Input	1	×	0	×	
	Output	0	0	0	SDA11 output = 1 ^{Note}	CMOS output
		0	1	0		N-ch O.D. output
P51	Input	1	—	0	×	
	Output	0		0	SO11 output = 1 ^{Note}	

Note P50/ANI26/INTP1/SI11/SDA11, P51/ANI25/INTP2/SO11 as a general-purpose port, set serial channel enable status register 0 (SE0), serial output register 0 (SO0) and serial output enable register 0 (SOE0) to the default status.

Remark ×: don't care

PM5×: Port mode register 5

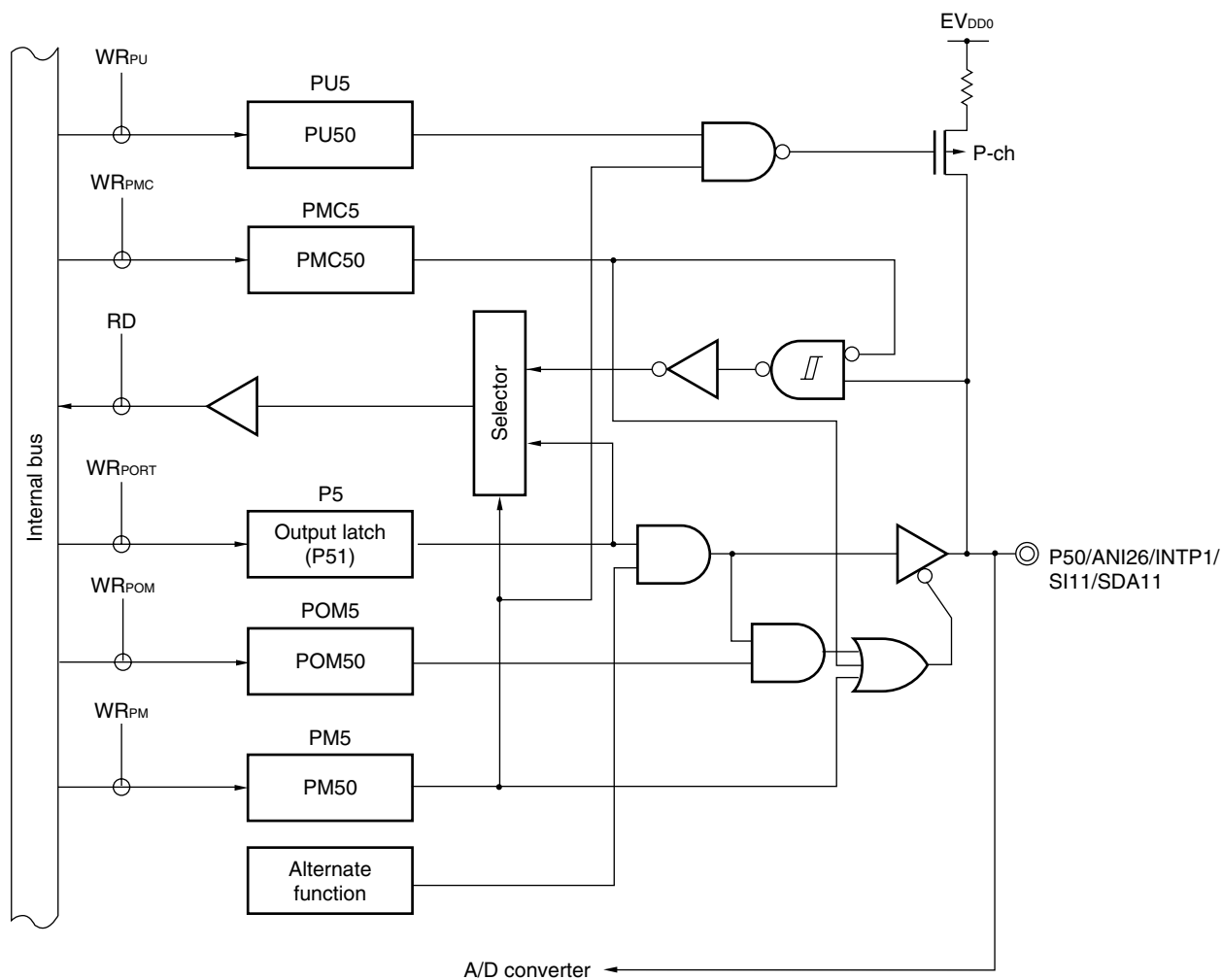
POM5×: Port output mode register 5

PMC5×: Port mode control register 5

For example, figures 4-21 and 4-22 show block diagrams of port 5 for 64-pin products.

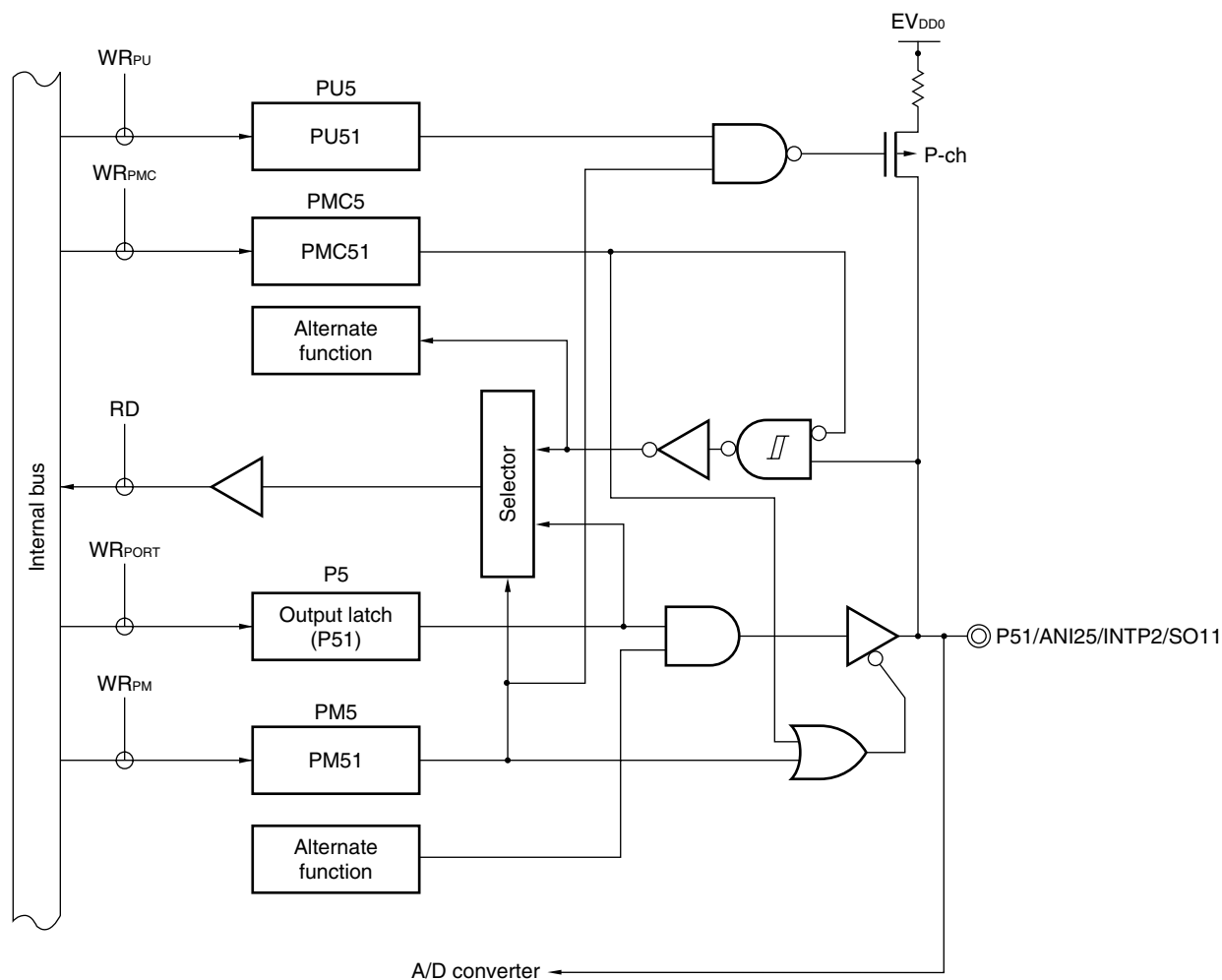
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Figure 4-21. Block Diagram of P50



- P5: Port register 5
- PU5: Pull-up resistor option register 5
- PM5: Port mode register 5
- POM5: Port output mode register 5
- PMC5: Port mode control register 5
- RD: Read signal
- WR_{xx} : Write signal

Figure 4-22. Block Diagram of P51



P5: Port register 5
 PU5: Pull-up resistor option register 5
 PM5: Port mode register 5
 PMC5: Port mode control register 5
 RD: Read signal
 WR_{xx} : Write signal

4.2.7 Port 6

Port 6 is an I/O port with an output latch. Port 6 can be set to the input mode or output mode in 1-bit units using port mode register 6 (PM6).

The output of the P60 to P63 pins is N-ch open-drain output (6 V tolerance).

This port can also be used for serial interface data I/O and clock I/O.

Reset signal generation sets port 6 to input mode.

Table 4-9. Settings of Registers When Using Port 6

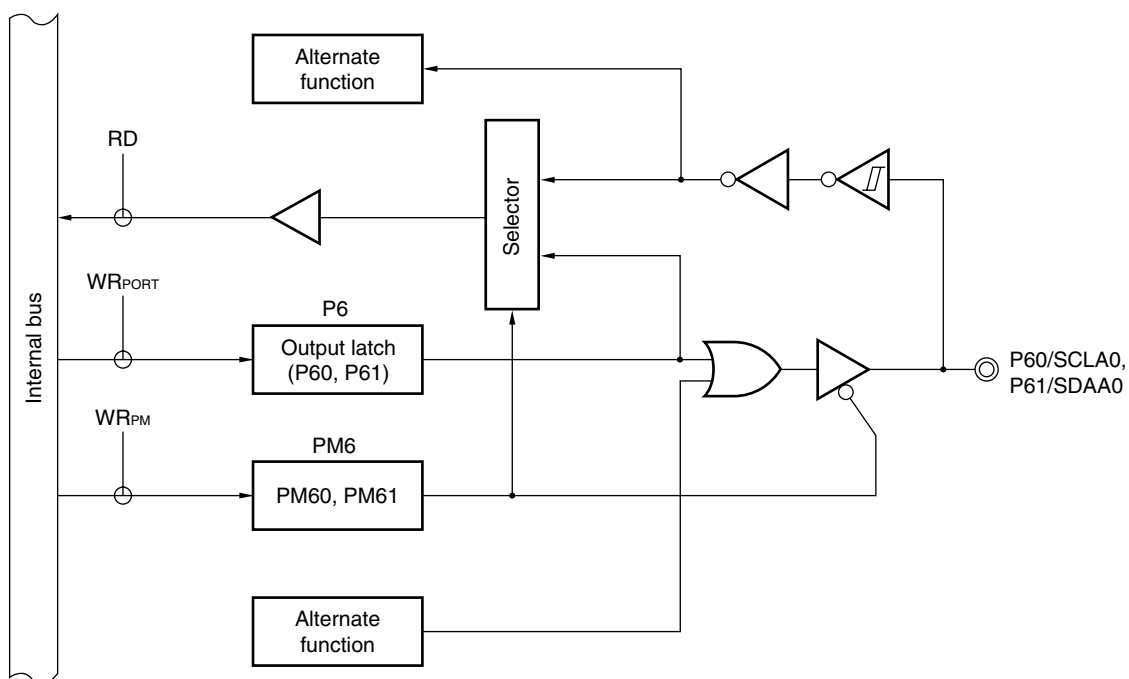
Name	I/O	PM6×	Alternate Function Setting	Remark
P60	Input	1	SCLA0 output = 0 ^{Note}	
	Output	0		
P61	Input	1	SDAA0 output = 0 ^{Note}	
	Output	0		
P62	Input	1	—	
	Output	0		
P63	Input	1	—	
	Output	0		

Note Stop the operation of serial interface IICA when using P60/SCLA0 and P61/SDAA0 as general-purpose ports.

Remark ×: don't care
PM6×: Port mode register 6

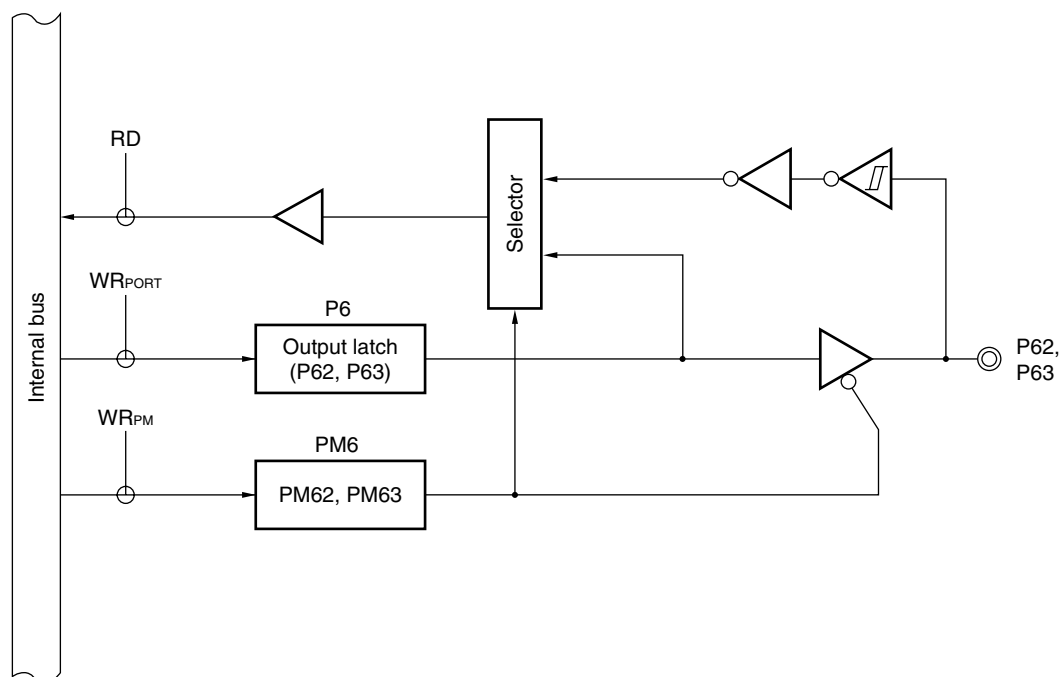
For example, figures 4-23 and 4-24 show block diagrams of port 6 for 64-pin products.

Figure 4-23. Block Diagram of P60, P61



P6: Port register 6
 PM6: Port mode register 6
 RD: Read signal
 WR_{xx}: Write signal

Figure 4-24. Block Diagram of P62, P63



P6: Port register 6
 PM6: Port mode register 6
 RD: Read signal
 WR_{xx}: Write signal

4.2.8 Port 7

Port 7 is an I/O port with an output latch. Port 7 can be set to the input mode or output mode in 1-bit units using port mode register 7 (PM7). When used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 7 (PU7).

Output from the P71 and P74 pins can be specified as N-ch open-drain output (V_{DD} tolerance^{Note 1}/EV_{DD} tolerance^{Note 2}) in 1-bit units using port output mode register 7 (POM7).

When the P70 pin is used as input, specify them as either digital or analog in Port mode control register 7 (PMC7). This register can be specified in 1-bit unit.

This port can also be used for A/D converter analog input, key interrupt input, serial interface data I/O, clock I/O, and external interrupt request input.

Reset signal generation sets port 7 to input mode.

- Notes 1.** When 25- to 48-pin products
2. When 64-pin products

Table 4-10. Settings of Registers When Using Port 7

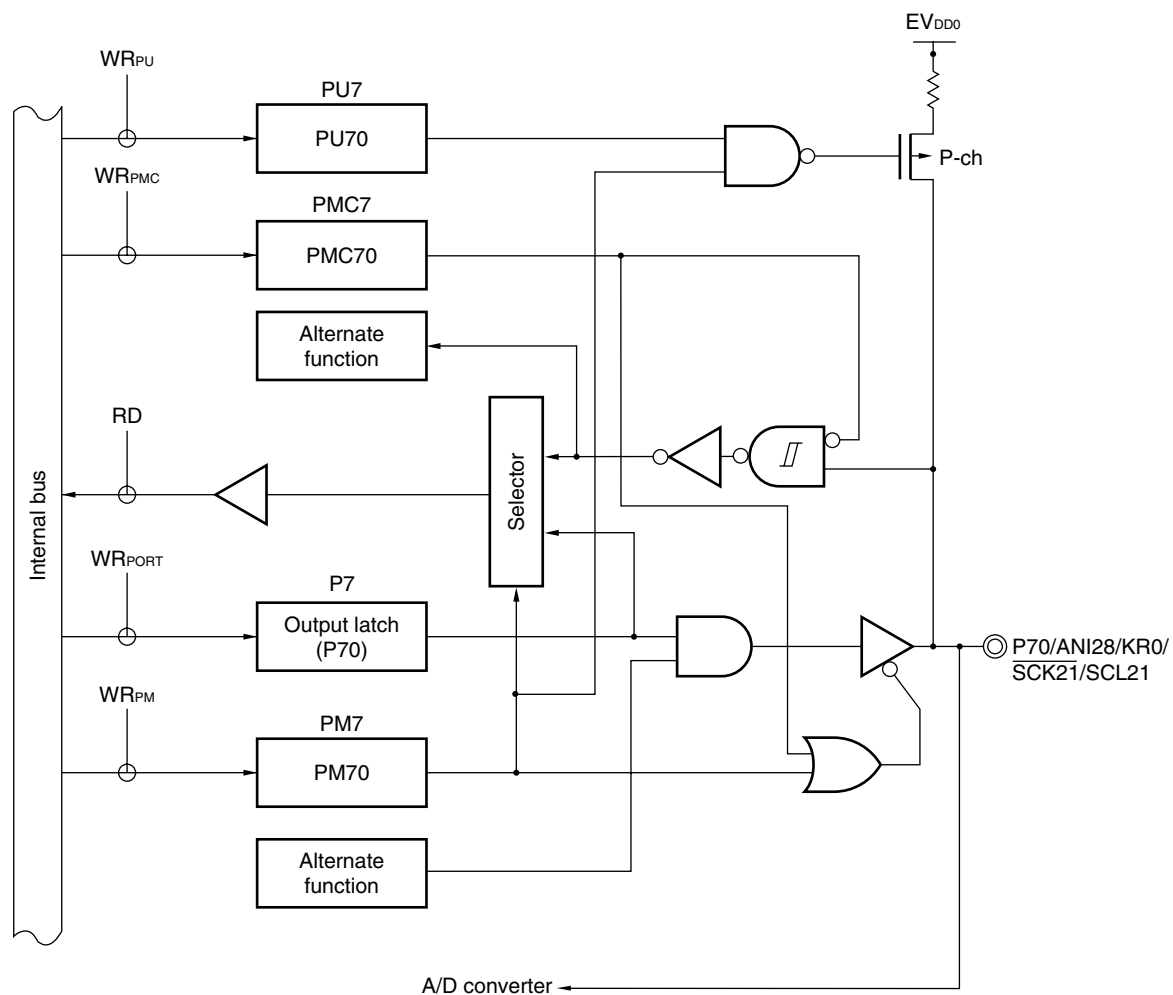
Name	I/O	PM7×	POM7×	PMC7×	Alternate Function Setting	Remark
P70	Input	1	–	0	×	
	Output	0		0	SCK21/SCL21 output = 1 ^{Note 1}	
P71	Input	1	×	–	×	
	Output	0	0		SDA21 output = 1 ^{Note 1}	CMOS output
		0	1			N-ch O.D. output
P72	Input	1	–	–	×	
	Output	0			SO21 output = 1 ^{Note 1}	
P73	Input	1	–	–	×	
	Output	0			SO01 output = 1 ^{Note 2}	
P74	Input	1	×	–	×	
	Output	0	0		SDA01 output = 1 ^{Note 2}	CMOS output
		0	1			N-ch O.D. output
P75	Input	1	–	–	×	
	Output	0			SCK01/SCL01 output = 1 ^{Note 2}	
P76	Input	1	–	–	×	
	Output	0			×	
P77	Input	1	–	–	×	
	Output	0			×	

- Notes 1.** To use P70/ANI28/KR0/SCK21/SCL21, P71/KR1/SI21/SDA21 or P72/KR2/SO21 as a general-purpose port, set serial channel enable status register 1 (SE1), serial output register 1 (SO1) and serial output enable register 1 (SOE1) to the default status.
- 2.** To use P73 to P75 as a general-purpose port, set serial channel enable status register 0 (SE0), serial output register 0 (SO0) and serial output enable register 0 (SOE0) to the default status.

Remark ×: don't care
 PM7×: Port mode register 7
 POM7×: Port output mode register 7
 PMC7×: Port mode control register 7

For example, figures 4-25 to 4-30 show block diagrams of port 7 for 64-pin products when PIOR = 00H.

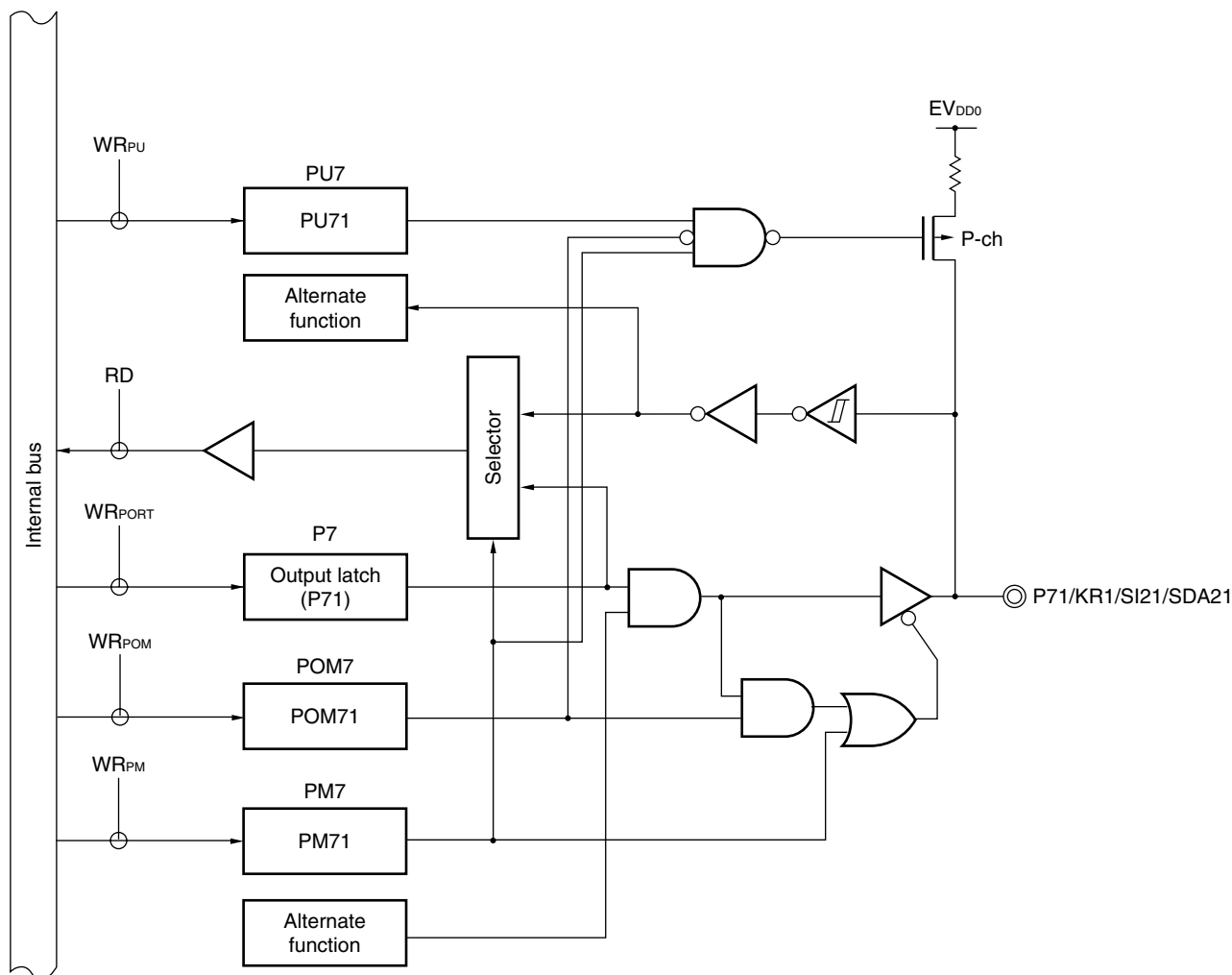
Figure 4-25. Block Diagram of P70



- P7: Port register 7
- PU7: Pull-up resistor option register 7
- PM7: Port mode register 7
- PMC7: Port mode control register 7
- RD: Read signal
- WR_{xx} : Write signal

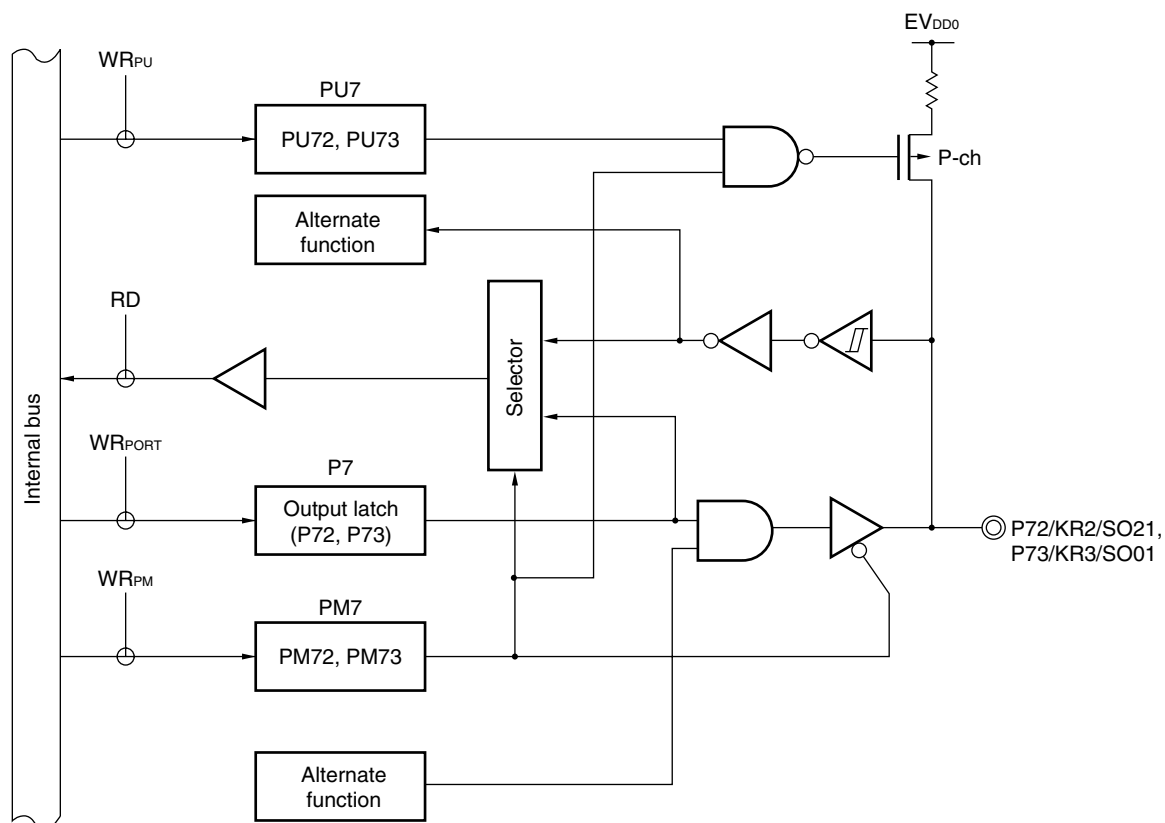
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Figure 4-26 Block Diagram of P71



P7: Port register 7
 PU7: Pull-up resistor option register 7
 PM7: Port mode register 7
 POM7: Port output mode register 7
 RD: Read signal
 WR_{xx}: Write signal

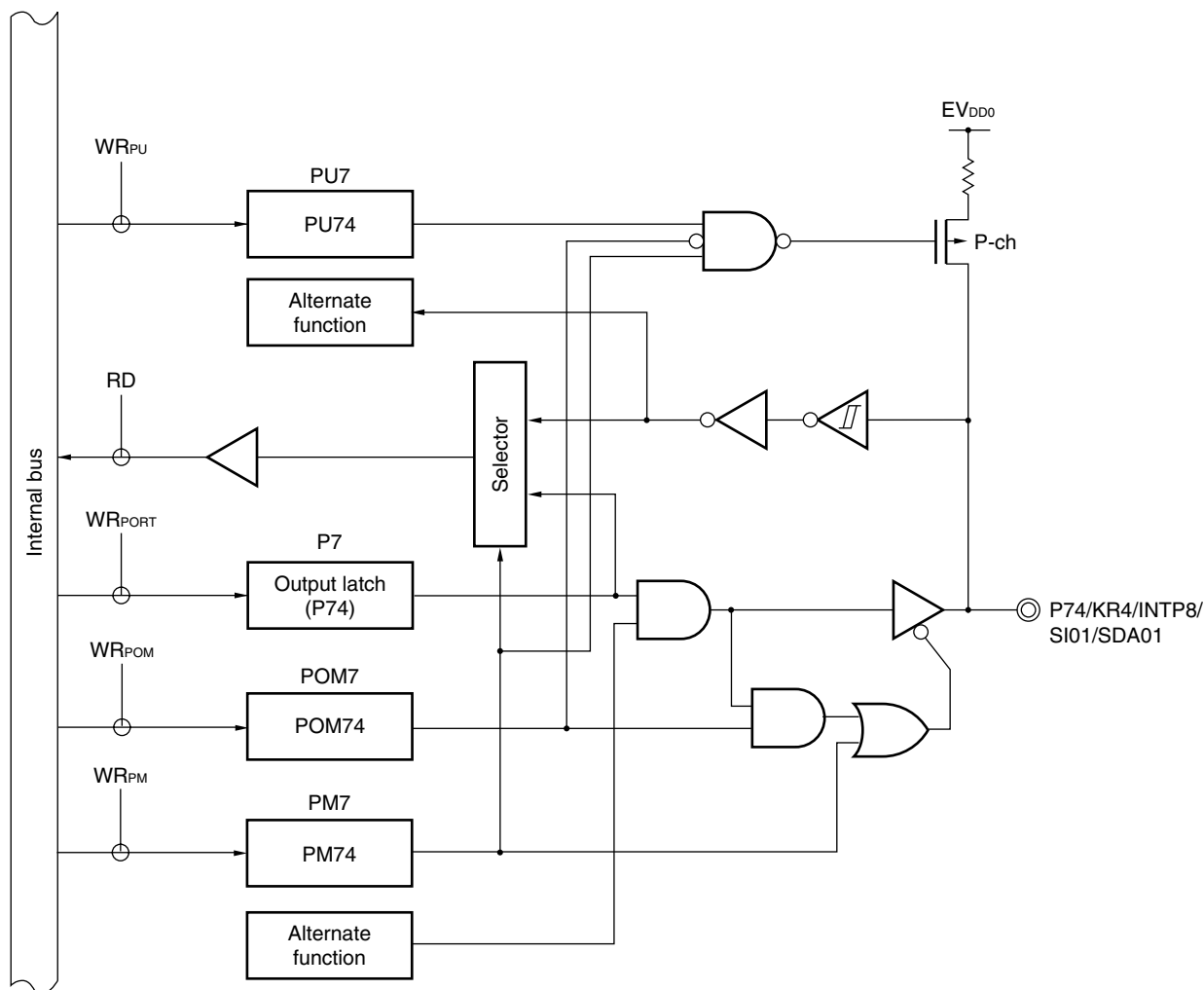
Figure 4-27. Block Diagrams of P72, P73



P7: Port register 7
 PU7: Pull-up resistor option register 7
 PM7: Port mode register 7
 RD: Read signal
 WR_{xx}: Write signal

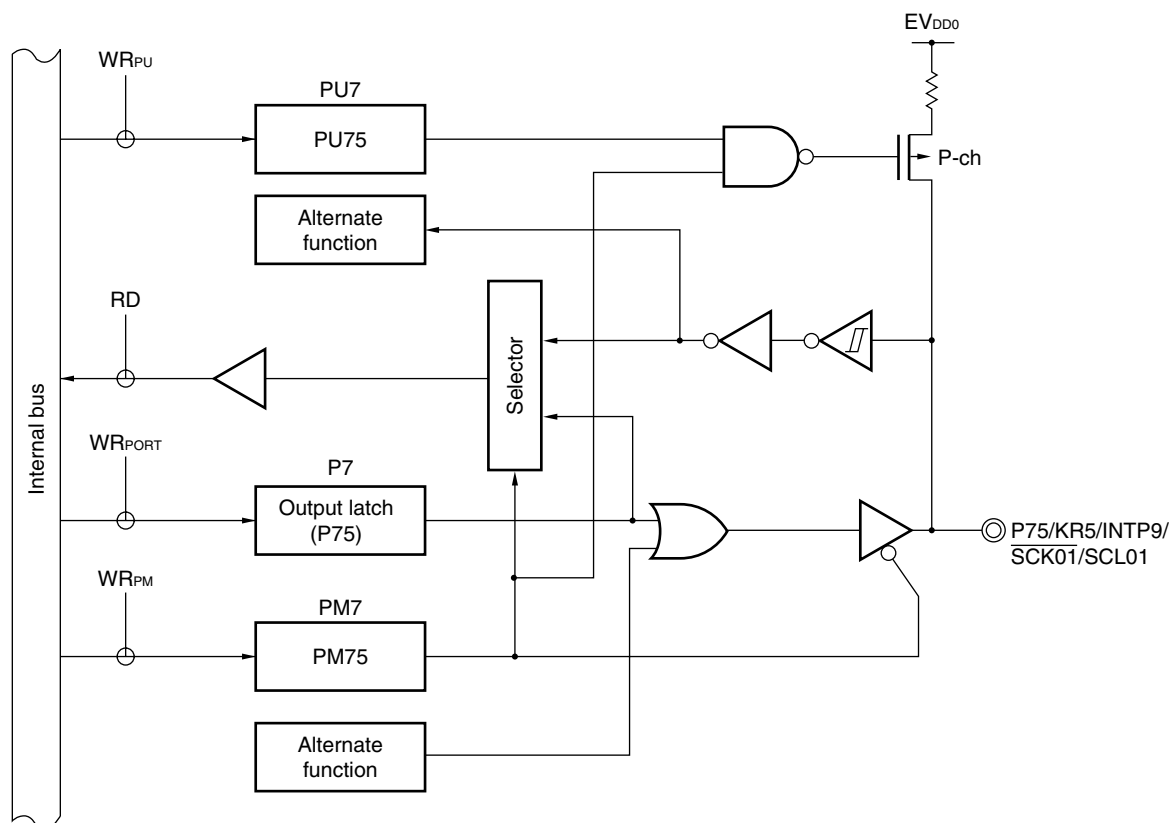
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Figure 4-28. Block Diagram of P74



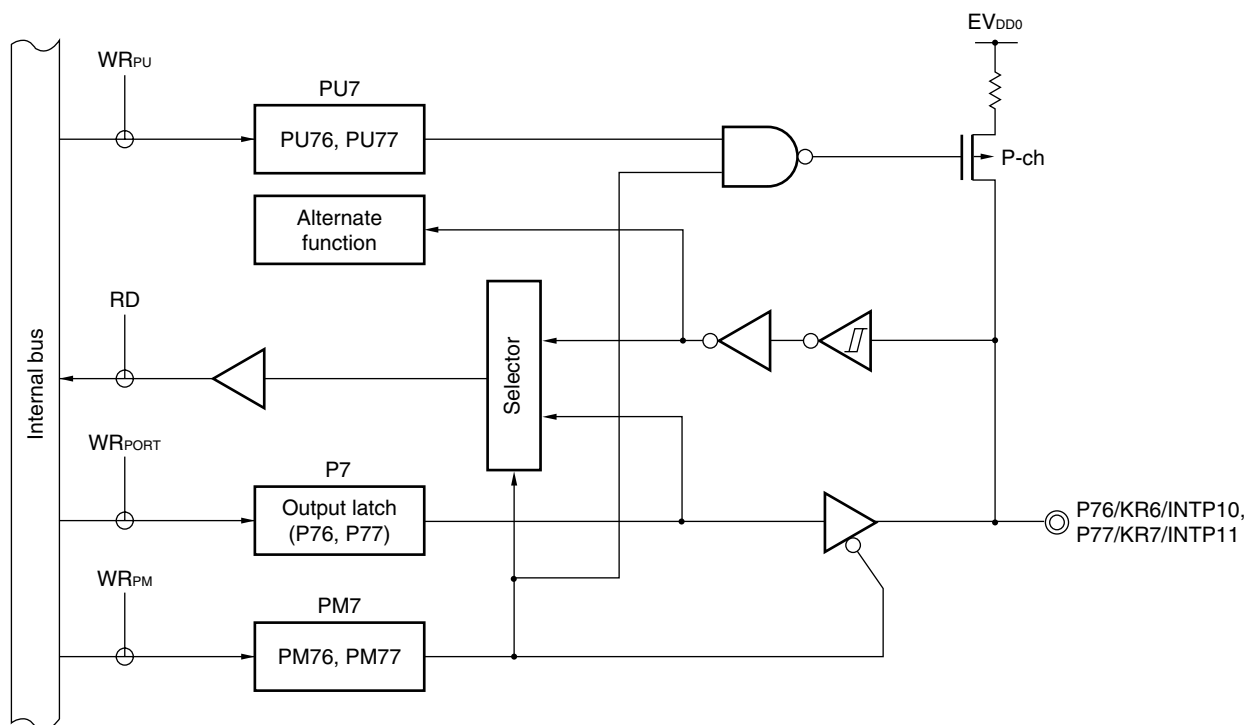
P7: Port register 7
 PU7: Pull-up resistor option register 7
 PM7: Port mode register 7
 POM7: Port output mode register 7
 RD: Read signal
 WR_{xx}: Write signal

Figure 4-29. Block Diagram of P75



P7: Port register 7
 PU7: Pull-up resistor option register 7
 PM7: Port mode register 7
 RD: Read signal
 WR_{xx} : Write signal

Figure 4-30. Block Diagrams of P76, P77



P7: Port register 7
 PU7: Pull-up resistor option register 7
 PM7: Port mode register 7
 RD: Read signal
 WR_{xx} : Write signal

4.2.9 Port 12

P120 is an I/O port with an output latch. Port 12 can be set to the input mode or output mode in 1-bit units using port mode register 12 (PM12). When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P124 are 4-bit input only ports.

Input to the P120 pin can be specified as analog input or digital input in 1-bit units, using port mode control register 12 (PMC12).

This port can also be used for A/D converter analog input, connecting resonator for main system clock, connecting resonator for subsystem clock, external clock input for main system clock, and external clock input for subsystem clock.

Reset signal generation sets P120 to analog input, and sets P121 to P124 to input mode.

Table 4-11. Settings of Registers When Using Port 12

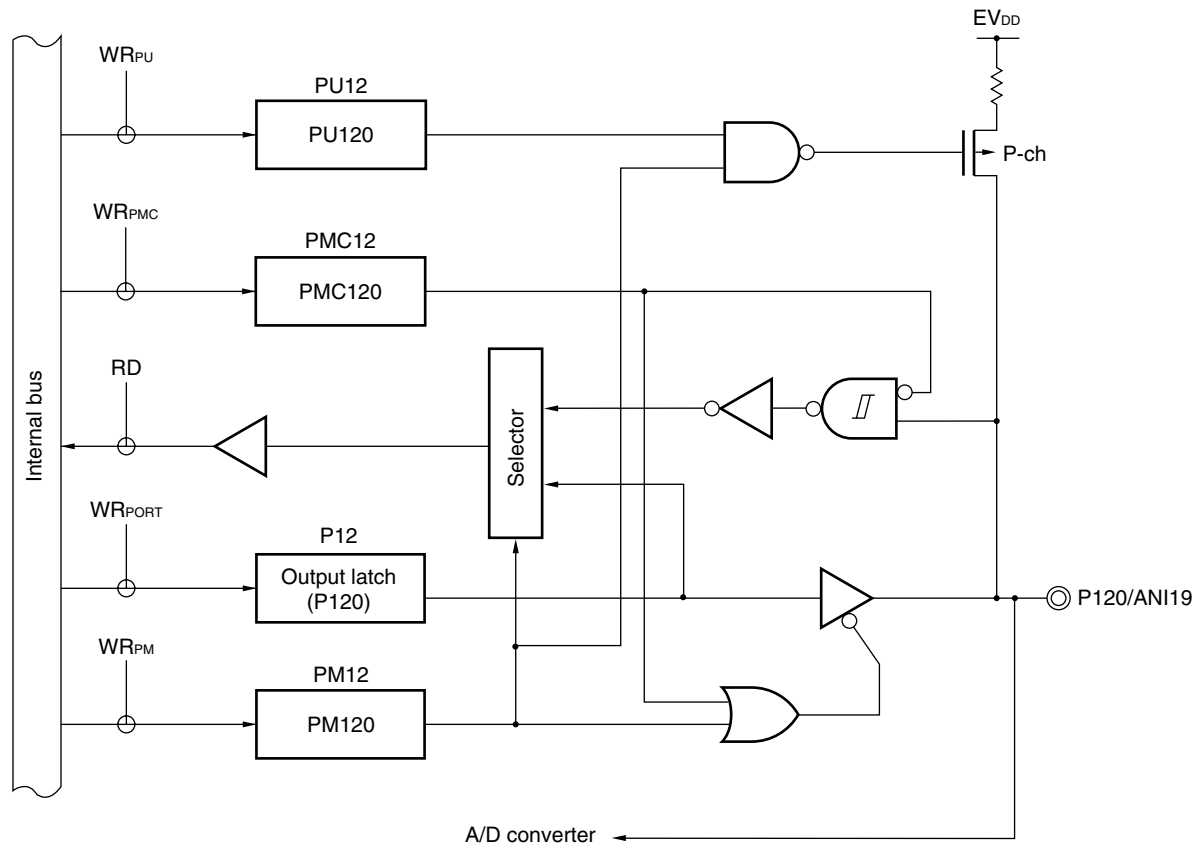
Name	I/O	PM12×	PMC12×	Alternate Function Setting	Remark
P120	Input	1	0	×	
	Output	0	0	×	
P121	Input	—	—	OSCSEL bit of CMC register = 0 or EXCLK bit = 1	
P122	Input	—	—	OSCSEL bit of CMC register = 0	
P123	Input	—	—	OSCSELS bit of CMC register = 0 or EXCLKS bit = 1	
P124	Input	—	—	OSCSELS bit of CMC register = 0	

Caution The function setting on P121 to P124 is available only once after the reset release. The port once set for connection to an X1, XT1 oscillator, external clock input cannot be used as an input port unless the reset is performed.

Remark ×: don't care
 PM12×: Port mode register 12
 PMC12×: Port mode control register 12

For example, figures 4-31 to 4-33 show block diagrams of port 12 for 64-pin products when PIOR = 00H.

Figure 4-31. Block Diagram of P120



- P12: Port register 12
- PU12: Pull-up resistor option register 12
- PM12: Port mode register 12
- PMC12: Port mode control register 12
- RD: Read signal
- WR_{xx} : Write signal

Figure 4-32. Block Diagram of P121 and P122

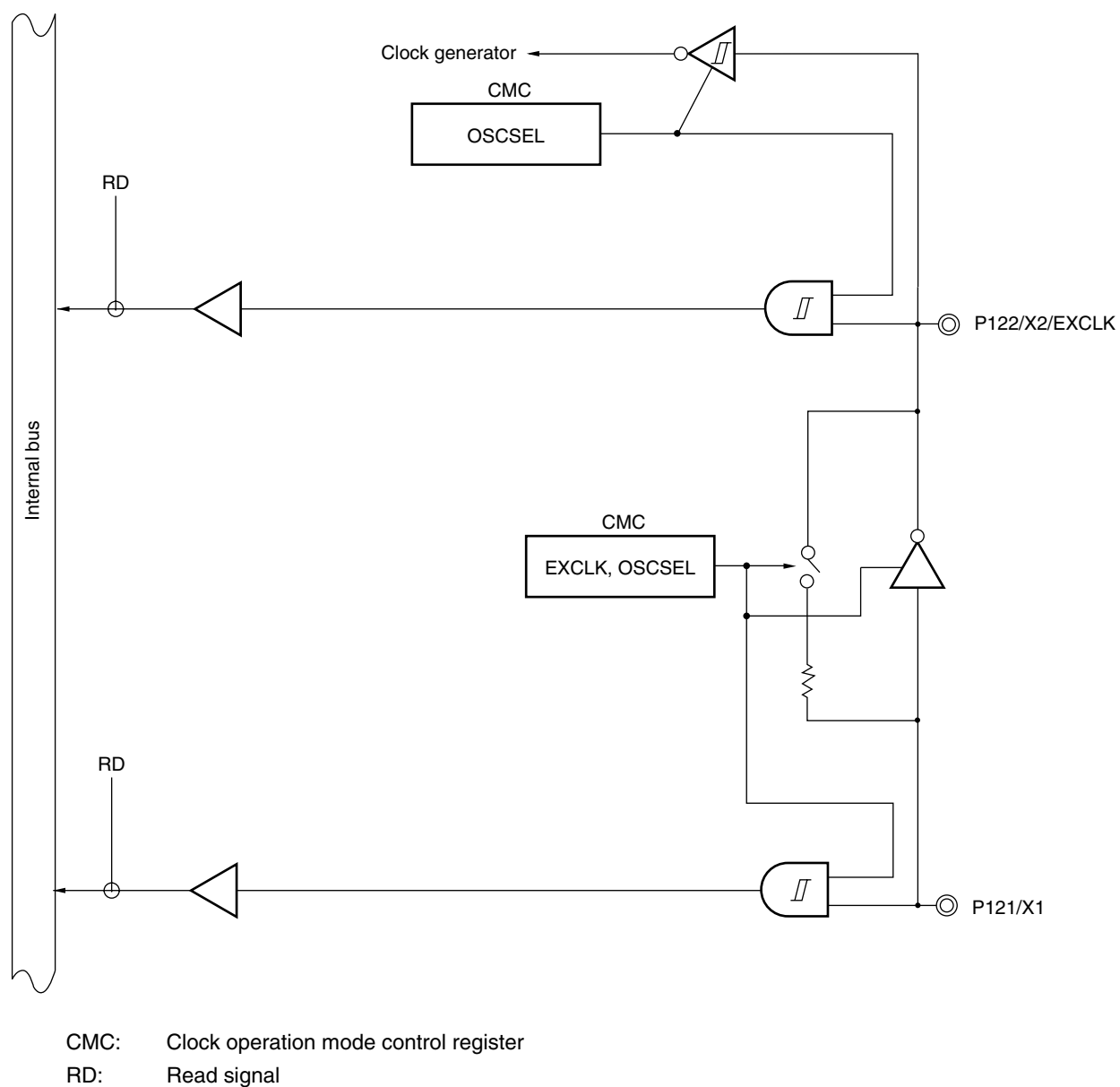
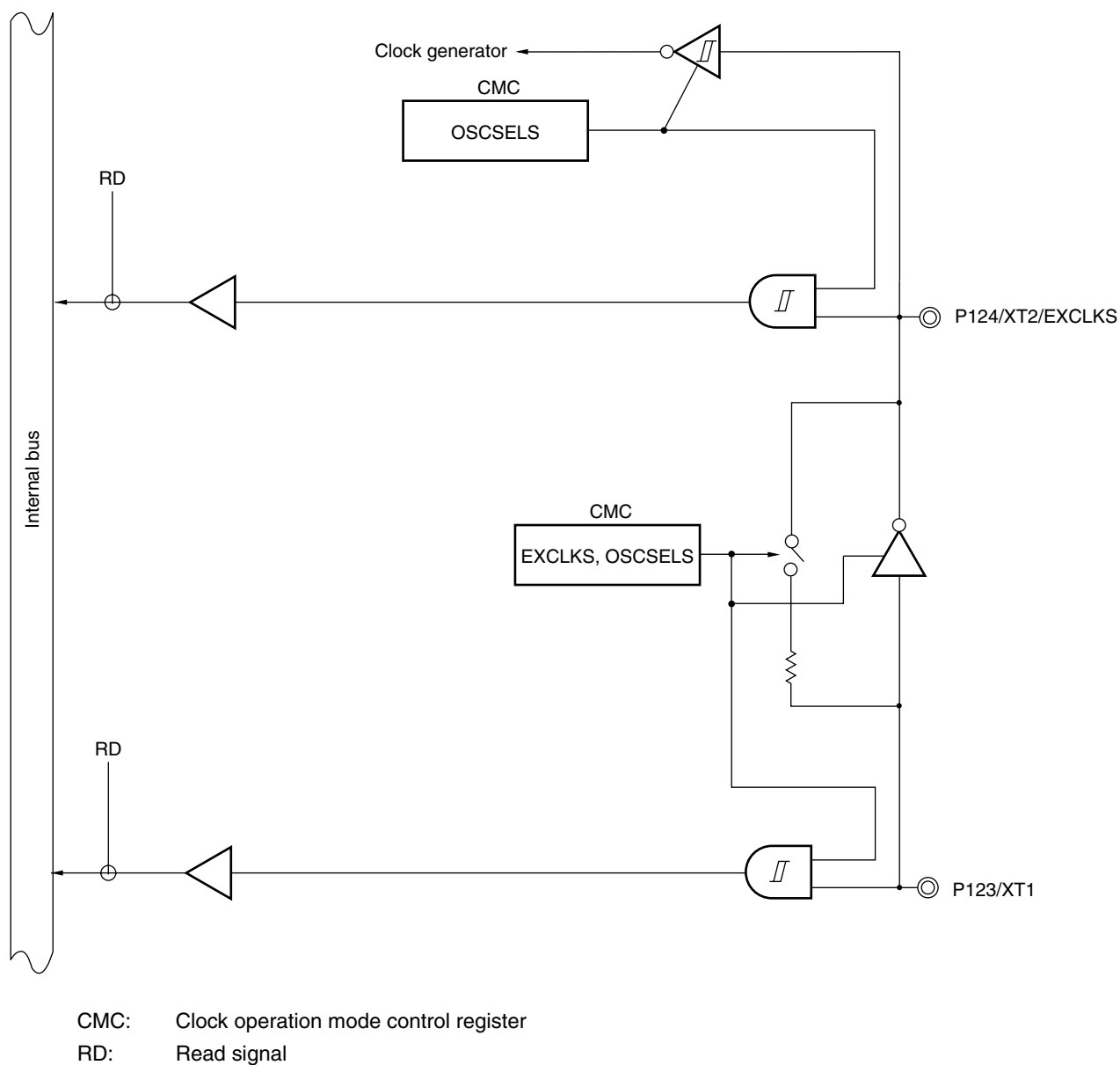


Figure 4-33. Block Diagram of P123 and P124



4.2.10 Port 13

P130 is a 1-bit output-only port with an output latch.

P137 is a 1-bit input-only port.

P130 is fixed an output port, and P137 is fixed an input ports.

This port can also be used for external interrupt request input.

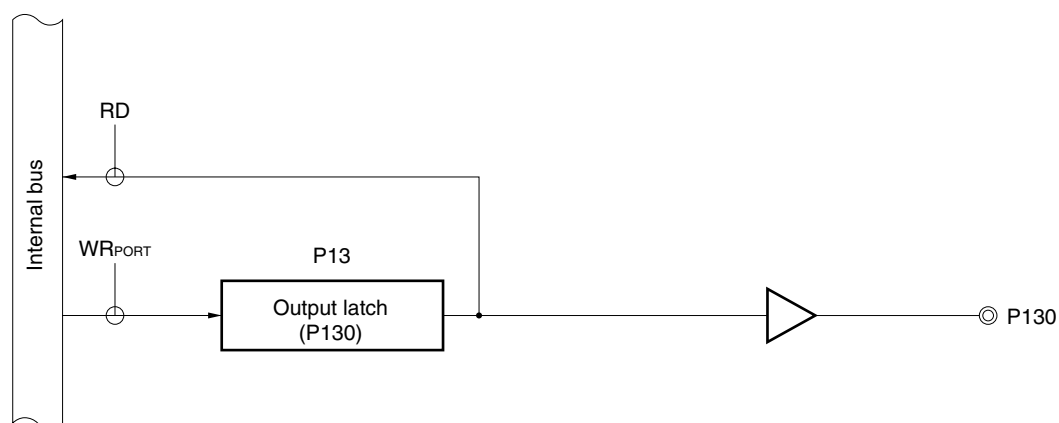
Table 4-12. Settings of Registers When Using Port 13

Name	I/O	Alternate Function Setting	Remark
P130	Output	—	
P137	Input	×	

Remark × : don't care

Figures 4-34 and 4-35 show block diagrams of port 13.

Figure 4-34. Block Diagram of P130



P13: Port register 13

RD: Read signal

WR_{xx}: Write signal

Remark When reset is effected, P130 outputs a low level. If P130 is set to output a high level before reset is effected, the output signal of P130 can be dummy-output as the CPU reset signal.

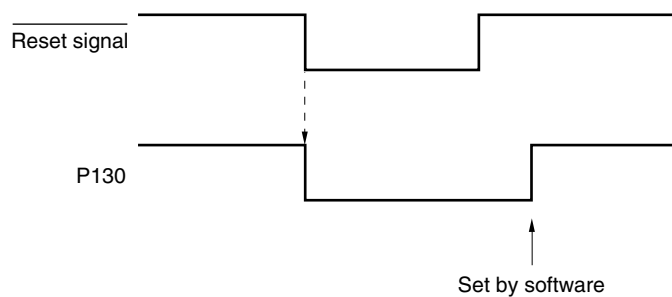
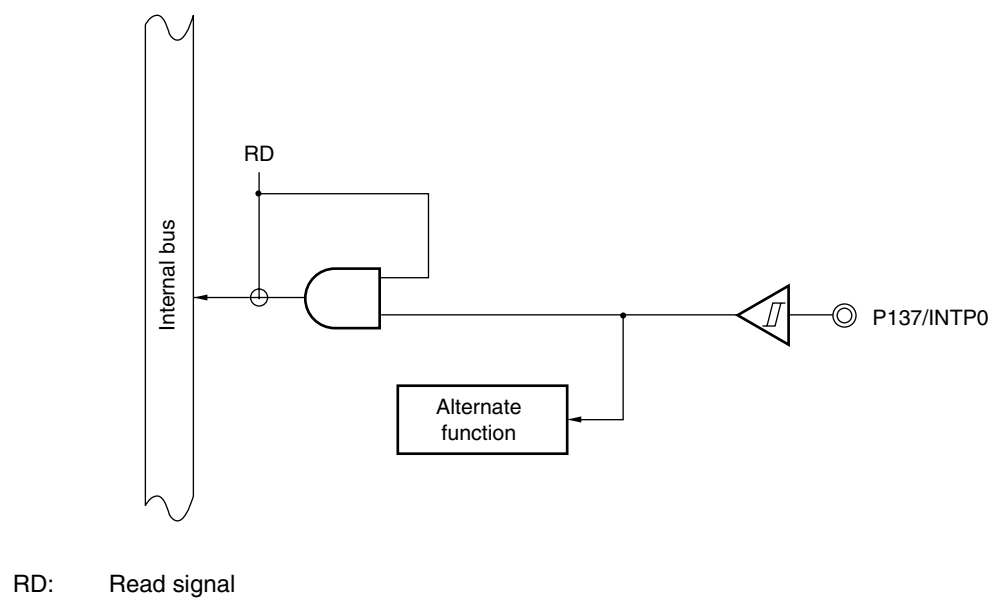


Figure 4-35. Block Diagram of P137



4.2.11 Port 14

Port 14 is an I/O port with an output latch. Port 14 can be set to the input mode or output mode in 1-bit units using port mode register 14 (PM14). When the P140, P141 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 14 (PU14).

This port can also be used for clock/buzzer output, and external interrupt request input, Reset signal generation sets P140, P141 to input mode.

Table 4-13. Settings of Registers When Using Port 14

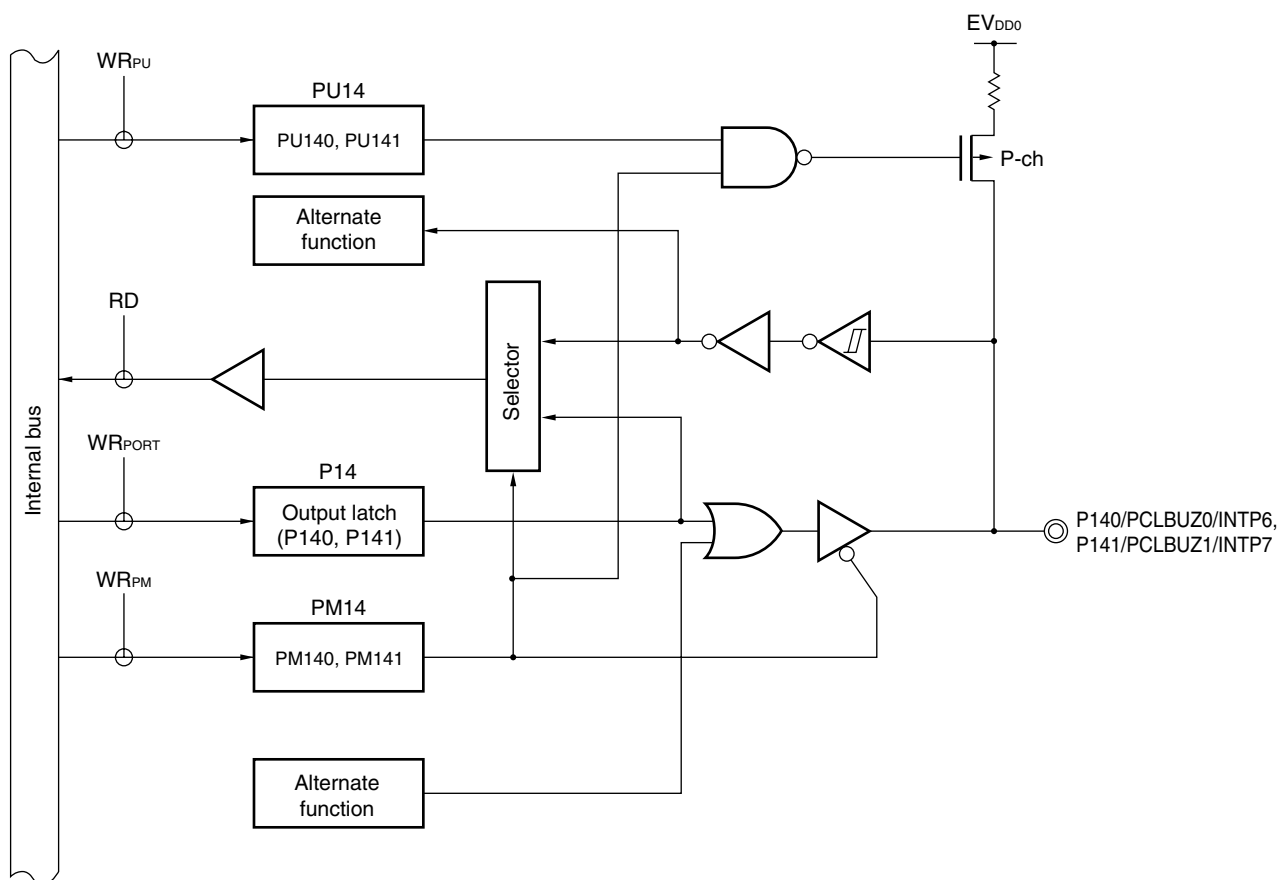
Name	I/O	PM14×	Alternate Function Setting	Remark
P140	Input	1	×	
	Output	0	PCLBUZ0 output ^{Note}	
P141	Input	1	×	
	Output	0	PCLBUZ1 output = 0 ^{Note}	

Note To use P140/PCLBUZ0/INTP6 or P141/PCLBUZ1/INTP7 as a general-purpose port, set bit 7 of clock output select registers 0 and 1 (CKS0, CKS1) to "0", which is the same as their default status settings.

Remark ×: don't care
PM14×: Port mode register 14

For example, figure 4-36 shows block diagrams of port 14 for 64-pin products.

Figure 4-36. Block Diagram of P140 and P141



P14: Port register 14
 PU14: Pull-up resistor option register 14
 PM14: Port mode register 14
 RD: Read signal
 WR_{xx}: Write signal

4.2.12 Port 15

Port 15 is an I/O port with an output latch. Port 15 can be set to the input mode or output mode in 1-bit units using port mode register 15 (PM15).

This port can also be used for A/D converter analog input.

To use P150/ANI8 to P154/ANI12 as digital input pins, set them in the digital I/O mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM15 register. Use these pins starting from the upper bit.

To use P150/ANI8 to P154/ANI12 as digital output pins, set them in the digital I/O mode by using the ADPC register and <R> in the output mode by using the PM15 register. Use these pins starting from the upper bit.

To use P150/ANI8 to P154/ANI12 as analog input pins, set them in the analog input mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM15 register. Use these pins starting from the lower bit.

Table 4-14. Settings of Registers When Using Port 15

Name	I/O	PM15×	ADPC	Alternate Function Setting	Remark
P15n	Input	1	01H to n+9H	—	To use P15n as a port, use these pins from a higher bit.
	Output	0			

- Remarks 1.** ×: don't care
 PM15×: Port mode register 15
 ADPC: A/D port configuration register
- 2.** n = 0 to 4

Table 4-15. Setting Functions of P150/ANI8 to P154/ANI12 Pins

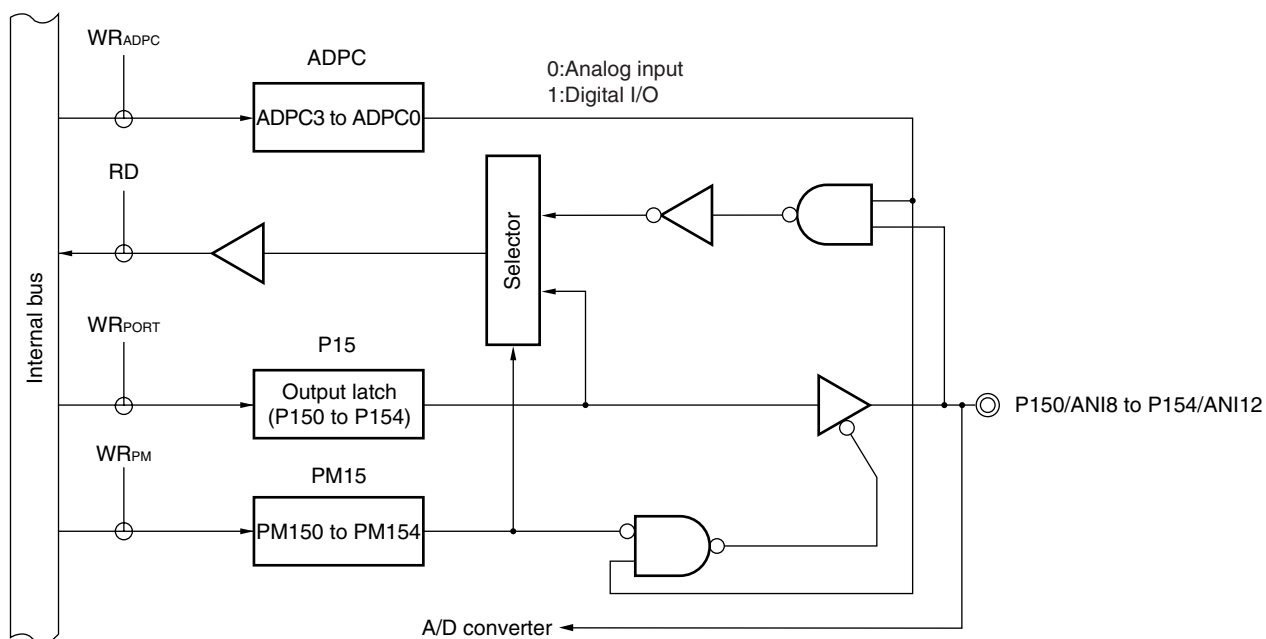
ADPC Register	PM15 Register	ADS Register	P150/ANI8 to P154/ANI12 Pins
Digital I/O selection	Input mode	—	Digital input
	Output mode	—	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

All P150/ANI8 to P154/ANI12 are set in the analog input mode when the reset signal is generated.

Figure 4-37 shows a block diagram of port 15.

For example, figures 4-37 shows block diagrams of port 15 for 64-pin products.

Figure 4-37. Block Diagram of P150 to P154



ADPC: A/D port configuration register

P15: Port register 15

PM15: Port mode register 15

RD: Read signal

WR_{xx}: Write signal

4.3 Registers Controlling Port Function

Port functions are controlled by the following registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- Port input mode registers (PIMxx)
- Port output mode registers (POMxx)
- Port mode control registers (PMCxx)
- A/D port configuration register (ADPC)
- Peripheral I/O redirection register (PIOR)
- Global digital input disable register (GDIDIS)
- Global analog input disable register (GAIDIS)

<R> **Caution** The undefined bits in each register vary by product and must be used with their initial value.

Table 4-16. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (1/2)

Port		Bit name						64-pin	48-pin	32-pin	25-pin
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register				
Port 0	0	PM00	P00	PU00	PIM00	–	–	√	–	–	–
	1	PM01	P01	PU01	PIM01	–	–	√	–	–	–
	2	PM02	P02	PU02	–	POM02	PMC02	√	√	√	√
	3	PM03	P03	PU03	PIM03	POM03	PMC03	√	√	√	√
	4	PM04	P04	PU04	PIM04	POM04	–	√	–	–	–
	5	PM05	P05	PU05	–	–	–	√	–	–	–
	6	PM06	P06	PU06	–	–	–	√	–	–	–
Port 1	0	PM10	P10	PU10	PIM10	POM10	PMC10	√	√	√	√
	1	PM11	P11	PU11	PIM11	POM11	PMC11	√	√	√	√
	2	PM12	P12	PU12	–	POM12	PMC12	√	√	√	√
	3	PM13	P13	PU13	–	POM13	PMC13	√	√	√	–
	4	PM14	P14	PU14	PIM14	POM14	PMC14	√	√	√	–
	5	PM15	P15	PU15	PIM15	POM15	PMC15	√	√	√	–
	6	PM16	P16	PU16	PIM16	–	–	√	√	–	–
Port 2	0	PM20	P20	–	–	–	–	√	√	√	√
	1	PM21	P21	–	–	–	–	√	√	√	√
	2	PM22	P22	–	–	–	–	√	√	√	√
	3	PM23	P23	–	–	–	–	√	√	√	√
	4	PM24	P24	–	–	–	–	√	√	√	–
	5	PM25	P25	–	–	–	–	√	√	–	–
	6	PM26	P26	–	–	–	–	√	√	–	–
	7	PM27	P27	–	–	–	–	√	√	–	–

Table 4-16. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (2/2)

Port		Bit name						64-pin	48-pin	32-pin	25-pin
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register				
Port 3	0	PM30	P30	PU30	–	–	PMC30	√	√	√	√
	1	PM31	P31	PU31	–	–	PMC31	√	√	√	√
Port 4	0	PM40	P40	PU40	–	–	–	√	√	√	√
	1	PM41	P41	PU41	–	–	PMC41	√	√	–	–
	2	PM42	P42	PU42	–	–	–	√	–	–	–
	3	PM43	P43	PU43	–	–	–	√	–	–	–
Port 5	0	PM50	P50	PU50	–	POM50	PMC50	√	√	√	√
	1	PM51	P51	PU51	–	–	PMC51	√	√	√	√
Port 6	0	PM60	P60	–	–	–	–	√	√	√	√
	1	PM61	P61	–	–	–	–	√	√	√	√
	2	PM62	P62	–	–	–	–	√	√	√	–
	3	PM63	P63	–	–	–	–	√	√	–	–
Port 7	0	PM70	P70	PU70	–	–	PMC70	√	√	√	–
	1	PM71	P71	PU71	–	POM71	–	√	√	–	–
	2	PM72	P72	PU72	–	–	–	√	√	–	–
	3	PM73	P73	PU73	–	–	–	√	√	–	–
	4	PM74	P74	PU74	–	POM74	–	√	√	–	–
	5	PM75	P75	PU75	–	–	–	√	√	–	–
	6	PM76	P76	PU76	–	–	–	√	–	–	–
	7	PM77	P77	PU77	–	–	–	√	–	–	–
Port 12	0	PM120	P120	PU120	–	–	PMC120	√	√	√	–
	1	–	P121	–	–	–	–	√	√	√	√
	2	–	P122	–	–	–	–	√	√	√	√
	3	–	P123	–	–	–	–	√	√	–	–
	4	–	P124	–	–	–	–	√	√	–	–
Port 13	0	–	P130	–	–	–	–	√	√	–	–
	7	–	P137	–	–	–	–	√	√	√	√
Port 14	0	PM140	P140	PU140	–	–	–	√	√	–	–
	1	PM141	P141	PU141	–	–	–	√	–	–	–
Port 15	–	PM150	P150	–	–	–	–	√	√	–	–
	–	PM151	P151	–	–	–	–	√	–	–	–
	–	PM152	P152	–	–	–	–	√	–	–	–
	–	PM153	P153	–	–	–	–	√	–	–	–
	–	PM154	P154	–	–	–	–	√	–	–	–

The format of each register is described below. The description here uses the 64-pin products as an example.

For the registers mounted on others than 64-pin products, refer to **table 4-16**.

4.3.1 Port mode registers (PMxx)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

When port pins are used as alternate-function pins, set the port mode register by referencing **4.5 Settings of Port Related Register When Using Alternate Function**.

Figure 4-38. Format of Port Mode Register (64-pin products)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	1	1	PM31	PM30	FFF23H	FFH	R/W
PM4	1	1	1	1	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
PM5	1	1	1	1	1	1	PM51	PM50	FFF25H	FFH	R/W
PM6	1	1	1	1	PM63	PM62	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM14	1	1	1	1	1	1	PM141	PM140	FFF2EH	FFH	R/W
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150	FFF2FH	FFH	R/W
PMmn	Pmn pin I/O mode selection (m = 0 to 7, 12, 14, 15; n = 0 to 7)										
0	Output mode (output buffer on)										
1	Input mode (output buffer off)										

Caution Be sure to set bit 7 of the PM0 register, bit 7 of the PM1 register, bits 7 to 2 of the PM3 register, bits 7 to 4 of the PM4 register, bits 7 to 2 of the PM5 register, bits 7 to 4 of the PM6 register, bits 7 to 1 of the PM12 register, bits 7 to 2 of the PM14 register, and bits 7 to 5 of the PM15 register to “1”.

4.3.2 Port registers (Pxx)

These registers set the output latch value of a port.

If the data is read in the input mode, the pin level is read. If it is read in the output mode, the output latch value is read^{Note}.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Note If P02, P03, P10 to P15, P20 to P27, P30, P31, P41, P50, P51, P70, P120, and P150 to P154 are set up as analog inputs of the A/D converter, when a port is read while in the input mode, 0 is always returned, not the pin level.

Figure 4-39. Format of Port Register (64-pin products)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	P06	P05	P04	P03	P02	P01	P00	FFF00H	00H (output latch)	R/W
P1	0	P16	P15	P14	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	0	0	0	0	0	0	P31	P30	FFF03H	00H (output latch)	R/W
P4	0	0	0	0	P43	P42	P41	P40	FFF04H	00H (output latch)	R/W
P5	0	0	0	0	0	0	P51	P50	FFF05H	00H (output latch)	R/W
P6	0	0	0	0	P63	P62	P61	P60	FFF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FFF0CH	Undefined	R/W ^{Note}
P13	P137	0	0	0	0	0	0	P130	FFF0DH	Note 2	R/W ^{Note}
P14	0	0	0	0	0	0	P141	P140	FFF0EH	00H (output latch)	R/W
P15	0	0	0	P154	P153	P152	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Notes 1. P121 to P124, and P137 are read-only.

2. P137 : Undefined

P1301: 0 (output latch)

Remark m = 0 to 7, 12 to 15; n = 0 to 7

4.3.3 Pull-up resistor option registers (PUxx)

These registers specify whether the on-chip pull-up resistors are to be used or not. On-chip pull-up resistors can be used in 1-bit units only for the bits set to input mode ($PM_{mn} = 1$ and $POM_{mn} = 0$) for the pins to which the use of an on-chip pull-up resistor has been specified in these registers. On-chip pull-up resistors cannot be connected to bits set to $\langle R \rangle$ output mode and bits used as alternate-function output pins and analog setting ($PMC = 1$, $ADPC = 1$), regardless of the settings of these registers.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H (Only PU4 is set to 01H).

$\langle R \rangle$ **Caution** When a port with the PIM_n register is input from different potential device to TTL buffer, pull up to the power supply of the different potential device via a external pull-up resistor by setting $PUM_n = 0$.

Figure 4-40. Format of Pull-up Resistor Option Register (64-pin products)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	PU06	PU05	PU04	PU03	PU02	PU01	PU00	F0030H	00H	R/W
PU1	0	PU16	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU3	0	0	0	0	0	0	PU31	PU30	F0033H	00H	R/W
PU4	0	0	0	0	PU43	PU42	PU41	PU40	F0034H	01H	R/W
PU5	0	0	0	0	0	0	PU51	PU50	F0035H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	F003CH	00H	R/W
PU14	0	0	0	0	0	0	PU141	PU140	F003EH	00H	R/W
PUMn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 5, 7, 12, 14; n = 0 to 7)										
0	On-chip pull-up resistor not connected										
1	On-chip pull-up resistor connected										

4.3.4 Port input mode registers (PIMxx)

These registers set the input buffer in 1-bit units.

TTL input buffer can be selected during serial communication with an external device of the different potential.

Port input mode registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 4-41. Format of Port Input Mode Register (64-pin products)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PIM0	0	0	0	PIM04	PIM03	0	PIM01	PIM00	F0040H	00H	R/W
PIM1	0	PIM16	PIM15	PIM14	PIM13	0	PIM11	PIM10	F0041H	00H	R/W
PIMmn	Pmn pin input buffer selection (m = 0, 1 ; n = 0, 1, 3 to 6)										
0	Normal input buffer										
1	TTL input buffer										

4.3.5 Port output mode registers (POMxx)

These registers set the output mode in 1-bit units.

N-ch open drain output (V_{DD} tolerance^{Note 1}/EV V_{DD} tolerance^{Note 2}) mode can be selected during serial communication with an external device of the different potential, and for the SDA00, SDA01, SDA10, SDA11, SDA20, and SDA21 pins during simplified I²C communication with an external device of the same potential.

<R> In addition, POMxx register is set with PUxx register, whether or not to use the on-chip pull-up resistor.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 4-42. Format of Port Input Mode Register (64-pin products)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM0	0	0	0	POM04	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W
POM5	0	0	0	0	0	0	0	POM50	F0055H	00H	R/W
POM7	0	0	0	POM74	0	0	POM71	0	F0057H	01H	R/W
<R>	POMmn	Pmn pin output mode selection (m = 0, 1, 4, 5, 7; n = 0 to 5)									
	0	Normal output mode Enable to the PUmn bit (when input mode)									
	1	N-ch open-drain output (V_{DD} tolerance ^{Note 1} /EV V_{DD} tolerance ^{Note 2}) mode Disable to the PUmn bit									

Notes 1. When 25 to 48 pin products

2. When 64 pin products

4.3.6 Port mode control registers (PMC0, PMC1, PMC3 to PMC5, PMC7, PMC12)

These registers set the P02, P03, P10 to P15, P30, P31, P41, P50, P51, P70, and P120 digital I/O/analog input in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to FFH.

Figure 4-43. Format of Port Mode Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC3	1	1	1	1	1	1	PMC31	PMC30	F0063H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC5	1	1	1	1	1	1	PMC51	PMC50	F0065H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W
PMC12	1	1	1	1	1	1	1	PMC120	F006CH	FFH	R/W

PMCmn	Pmn pin digital I/O/analog input selection (m = 0, 1, 3 to 5, 7, 12; n = 0 to 5)
0	Digital I/O (alternate function other than analog input)
1	Analog input

- <R> **Cautions 1.** Set the channel used for A/D conversion to the input mode by using port mode registers 0, 1, 3 to 5, 7, 12 (PM0, PM1, PM3 to PM5, PM7, PM12).
- <R> **2.** Do not set the pin set by the PMC register as digital I/O by the analog input channel specification register (ADS).

4.3.7 A/D port configuration register (ADPC)

This register switches the P20/ANI0 to P27/ANI7, and P150/ANI8 to P154/ANI12 pins to digital I/O of port or analog input of A/D converter.

The ADPC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 4-44. Format of A/D Port Configuration Register (ADPC)

Address: F0076H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching												
				ANI12/P154	ANI11/P153	ANI10/P152	ANI9/P151	ANI8/P150	ANI7/P27	ANI6/P26	ANI5/P25	ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	1	0	D	D	D	D	D	D	D	D	D	D	D	D	A
0	0	1	1	D	D	D	D	D	D	D	D	D	D	D	A	A
0	1	0	0	D	D	D	D	D	D	D	D	D	D	A	A	A
0	1	0	1	D	D	D	D	D	D	D	D	D	A	A	A	A
0	1	1	0	D	D	D	D	D	D	D	D	A	A	A	A	A
0	1	1	1	D	D	D	D	D	D	D	A	A	A	A	A	A
1	0	0	0	D	D	D	D	D	D	A	A	A	A	A	A	A
1	0	0	1	D	D	D	D	D	A	A	A	A	A	A	A	A
1	0	1	0	D	D	D	D	A	A	A	A	A	A	A	A	A
1	0	1	1	D	D	D	A	A	A	A	A	A	A	A	A	A
1	1	0	0	D	D	A	A	A	A	A	A	A	A	A	A	A
1	1	0	1	D	A	A	A	A	A	A	A	A	A	A	A	A
1	1	1	0	A	A	A	A	A	A	A	A	A	A	A	A	A
1	1	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A

- <R> **Cautions**
1. Set the port to analog input by ADPC register to the input mode by using port mode registers 2, 15 (PM2, PM15).
 2. Do not set the pin set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

4.3.8 Peripheral I/O redirection register (PIOR)

This register is used to specify whether to enable or disable the peripheral I/O redirect function.

This function is used to switch ports to which alternate functions are assigned.

<R> Use the PIOR register to assign a port to the function to redirect and enable the function.

In addition, can be changed the settings for redirection until its function enable operation. The PIOR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 4-45. Format of Peripheral I/O Redirection Register (PIOR)

Address: F0077H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR	0	0	0	0	0	0	PIOR1	PIOR0

Function	64-pin				48-pin				32-pin				25-pin			
	Setting value of PIOR1, PIOR0				Setting value of PIOR1, PIOR0				Setting value of PIOR1, PIOR0				Setting value of PIOR1, PIOR0			
	0, 0	0, 1	1, 0	1, 1	0, 0	0, 1	1, 0	1, 1	0, 0	0, 1	1, 0	1, 1	0, 0	0, 1	1, 0	1, 1
<R> KR0	P70	Setting prohibited	P00	P10	P70	Setting prohibited	P02	P10	P70	Setting prohibited	P120	P10	—	Setting prohibited	P02	Setting prohibited
KR1	P71		P01	P11	P71		P03	P11	—		P02	P11	—		P03	
KR2	P72		P02	P12	P72		P22	P12	—		P03	P12	—		P22	
KR3	P73		P03	P13	P73		P23	P13	—		P22	P13	—		P23	
KR4	P74		P04	P14	P74		P24	P14	—		P23	P14	—		—	
KR5	P75		P22	P15	P75		P25	P15	—		P24	P15	—		—	
KR6	P76		P23	P151	—		—	—	—		—	—	—		—	
KR7	P77		P24	P152	—		—	—	—		—	—	—		—	
KR8	P05		P25	P153	—		—	—	—		—	—	—		—	
KR9	P06		P26	P154	—		—	—	—		—	—	—		—	

4.3.9 Global digital input disable register (GDIDIS)

This register is used to prevent through-current flowing from the input buffers when EV_{DD0} is 0 V.

By setting the GDIDIS0 bit to 1, input to any input buffer connected to EV_{DD0} is prohibited, preventing through-current from flowing when the power supply connected to EV_{DD0} is turned off.

When using the GDIDIS register, be sure to set the GDIDIS0 bit to 1 before turning off the EV_{DD0} power supply, and then clear the GDIDIS0 bit to 0 after turning on the EV_{DD0} power supply.

The GDIDIS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

<R> **Remark** GDIDIS register is equipped with 64-pin products.

Figure 4-46. Format of Global Digital Input Disable Register (GDIDIS)

Address: F007DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
GDIDIS	0	0	0	0	0	0	0	GDIDIS0

GDIDIS0	Setting of input buffers when EV_{DD} is 0 V
0	Input to input buffers permitted (default)
1	Input to input buffers prohibited. No through-current flows to the input buffers.

4.3.10 Global analog input disable register (GAIDIS)

<R> This register is used to prevent through-current flowing from the input buffers when AV_{DD} is 0 V.

By setting the GAIDIS0 bit to 1, input to any input buffer connected to AV_{DD} is prohibited, preventing through-current from flowing when the power supply connected to AV_{DD} is turned off.

When using the GAIDIS register, be sure to set the GAIDIS0 bit to 1 before turning off the AV_{DD} power supply, and then clear the GAIDIS0 bit to 0 after turning on the AV_{DD} power supply.

Set GAIDIS0 to 0 after applying power to AV_{DD} .

The GAIDIS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 4-47. Format of Global Analog Input Disable Register (GAIDIS)

Address: F007CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
GAIDIS	0	0	0	0	0	0	0	GAIDIS0

GAIDIS0	Setting of input buffers
0	Input to input buffers permitted (default)
1	Input to input buffers prohibited. No through-current flows to the input buffers.

4.4 Port Function Operations

Port operations differ depending on whether the input or output mode is set, as shown below.

4.4.1 Writing to I/O port

(1) Output mode

A value is written to the output latch by a transfer instruction, and the output latch contents are output from the pin.

Once data is written to the output latch, it is retained until data is written to the output latch again.

The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

<R> A value is written to the output latch by a transfer instruction, but since the output buffer is off, the pin status does not change. Therefore, byte data can be written to the ports used for both input and output.

Once data is written to the output latch, it is retained until data is written to the output latch again.

The data of the output latch is cleared when a reset signal is generated.

4.4.2 Reading from I/O port

(1) Output mode

The output latch contents are read by a transfer instruction. The output latch contents do not change.

(2) Input mode

The pin status is read by a transfer instruction. The output latch contents do not change.

4.4.3 Operations on I/O port

(1) Output mode

An operation is performed on the output latch contents, and the result is written to the output latch. The output latch contents are output from the pins.

Once data is written to the output latch, it is retained until data is written to the output latch again.

The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

<R> The pin level is read and an operation is performed on its contents. The result of the operation is written to the output latch, but since the output buffer is off, the pin status does not change. Therefore, byte data can be written to the ports used for both input and output.

The data of the output latch is cleared when a reset signal is generated.

4.4.4 Connecting to external device with different potential (1.8 V or 2.5 V)

It is possible to connect to an external device with a different potential by changing EV_{DD} of the RL78/G1A to accord with the power supply voltage of the connected device. Even when using an RL78/G1A microcontroller that has no EV_{DD0} pin or whose EV_{DD0} pin potential cannot be changed to the voltage of the connected device, I/O connection with an external device operating on 1.8 V or 2.5 V is still possible by using the serial interface or general-purpose port feature of ports 0, 1, and 7.

External Device	EV_{DD}	No EV_{DD}
2.5 V	$3.3\text{ V} \leq EV_{DD} < 3.6\text{ V}$, $3.3\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $EV_{DD} \leq V_{DD}$	$3.3\text{ V} \leq V_{DD} \leq 3.6\text{ V}$
1.8 V	$1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$, $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $EV_{DD} \leq V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 3.3\text{ V}$

Regarding inputs, Normal (CMOS)/TTL input buffer switching is possible on a bit-by-bit basis by the port input mode registers (PIM0, PIM1, PIM4, PIM5, PIM8, PIM14).

Moreover, regarding outputs, different potentials can be supported by switching the output buffer to the N-ch open drain (V_{DD} tolerance^{Note 1}/ EV_{DD} tolerance^{Note 2}) by the port output mode registers (POM0, POM1, POM4, POM5, POM8, POM14).

Following, describes the connection of a serial interface.

- Notes 1.** For 25- to 48-pin products
2. For 64-pin products

(1) Setting procedure when using I/O pins of UART0 to UART2, CSI00, CSI10, and CSI20 functions

(a) Use as 1.8 V or 2.5 V input port

- <1> Externally pull up the pin to be used to the power supply of the target device, as necessary on-chip pull-up resistors cannot be used.

In case of UART0:	P11
In case of UART1:	P03
In case of UART2:	P14
In case of CSI00:	P10, P11
In case of CSI10:	P03, P04
In case of CSI20:	P14, P15

- <2> After reset release, the port is set to the input mode (Hi-Z).
 <3> Set the corresponding bit of the PIM0 and PIM1 registers to 1 to switch to the TTL input buffer.
 <4> The microcontroller can then operate on V_{IH} and V_{IL} corresponding to an operating voltage of 1.8 V or 2.5 V.

(b) Use as 1.8 V, 2.5 V output port

<1> Pull up externally the pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).

In case of UART0: P12
 In case of UART1: P02
 In case of UART2: P13
 In case of CSI00: P10, P12
 In case of CSI10: P02, P04
 In case of CSI20: P13, P15

<2> After reset release, the port mode changes to the input mode (Hi-Z).

<3> Set the output latch of the corresponding port to 1.

<4> Set the corresponding bit of the POM0 and POM1 registers to 1 to set the N-ch open drain output (V_{DD} tolerance^{Note 1}/EV_{DD} tolerance^{Note 2}) mode.

<5> Set the output mode by manipulating the PM0 and PM1 registers.
 At this time, the output data is high level, so the pin is in the Hi-Z state.

<6> Can be communication by setting the serial array unit.

Notes 1. When 25 to 48 pin products

2. When 64 pin products

(2) Setting procedure when using I/O pins of IIC00, IIC10, and IIC20 functions

<1> Externally pull up the pin to be used (on-chip pull-up resistor cannot be used).

In case of IIC00: P10, P11
 In case of IIC10: P03, P04
 In case of IIC20: P14, P15

<2> After reset release, the port mode is the input mode (Hi-Z).

<3> Set the output latch of the corresponding port to 1.

<4> Set the corresponding bit of the POM0 and POM1 registers to 1 to set the N-ch open drain output (V_{DD} tolerance^{Note 1}/EV_{DD} tolerance^{Note 2}) mode.

<R> <5> Set the corresponding bit of the PIM0, and PIM1 registers to 1 to switch the TTL input buffer.

<6> Set the corresponding bit of the PM0 and PM1 registers to the output mode (data I/O is possible in the output mode).

At this time, the output data is high level, so the pin is in the Hi-Z state.

<7> Enable the operation of the serial array unit and set the mode to the simplified I²C mode.

Notes 1. When 25 to 48 pin products

2. When 64 pin products

4.5 Settings of Port Related Register When Using Alternate Function

To use the alternate function of a port pin, set the port mode register, and output latch as shown in Table 4-17.

<R> **Caution** If the output function of an alternate function is assigned to a pin that is also used as an output pin, the output of the unused alternate function must be set to its initial state. See 4.6.2 for details about the applicable units and how to handle such pins.

Table 4-17. Settings of Port Related Register When Using Alternate Function (1/4)

Pin Name	Alternate Function		PIOR0, PIOR1	POMxx	PMCxx	PMxx	Pxx
	Function Name	I/O					
P00	TI00	Input	×	–	–	1	×
	(KR0)	Input	1, 0	–	–	1	×
P01	TO00	Output	×	–	–	0	0
	(KR1)	Input	1, 0	–	–	1	×
P02	ANI17 ^{Note 1}	Input	×	×	1	1	×
	SO10	Output	×	0/1	0	0	1
	TxD1	Output	×	0/1	0	0	1
	(KR2)	Input	1, 0	×	0	1	×
P03	ANI16 ^{Note 1}	Input	×	×	1	1	×
	SI10	Input	×	×	0	1	×
	RxD1	Input	×	×	0	1	×
	SDA10	I/O	×	1	0	0	1
	(KR3)	Input	1, 0	×	–	1	×
P04	SCK10	Input	×	×	–	1	×
		Output	×	0/1	–	0	1
	SCL10	Output	×	0/1	–	0	1
	(KR4)	Input	1, 0	×	–	1	×
P05	TI05	Input	×	–	–	1	×
	TO05	Output	×	–	–	0	1
	KR8	Input	0, 0	–	–	1	×
P06	TI06	Input	×	–	–	1	×
	TO06	Output	×	–	–	0	1
	KR9	Input	0, 0	–	–	1	×

- Remarks**
1. ×: don't care
PIOR0, PIOR1: Bits 0, 1 of peripheral I/O redirection register
POMxx: Port output mode register
PMCxx: Port mode control register
PMxx: Port mode register
Pxx: Port output latch
 2. The relationship between pins and their alternate functions shown in this table indicates the relationship when a 64-pin product is used. In other products, alternate functions might be assigned to different pins, but even in this case, the PIORx, POMxx, PMCxx, PMxx, and Pxx set in the same way.
 3. Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection register (PIOR).

(The **Note 1** is described after the last table.)

Table 4-17. Settings of Port Related Register When Using Alternate Function (2/4)

Pin Name	Alternate Function		PIOR0, PIOR1	POM _{xx}	PMC _{xx}	PM _{xx}	P _{xx}
	Function Name	I/O					
P10	ANI18 ^{Note 1}	Input	×	×	1	1	×
	SCK00	Input	×	×	0	1	×
		Output	×	0/1	0	0	1
	SCL00	Output	×	0/1	0	0	1
	(KR0)	Input	1, 1	×	0	1	×
P11	ANI20 ^{Note 1}	Input	×	×	1	1	×
	SI00	Input	×	×	0	1	×
	RxD0	Input	×	×	0	1	×
	TOOLRxD	Input	×	×	0	1	×
	SDA00	I/O	×	1	0	0	1
	(KR1)	Input	1, 1	×	0	1	×
P12	ANI21 ^{Note 1}	Input	×	×	1	1	×
	SO00	Output	×	0/1	0	0	1
	TxD0	Output	×	0/1	0	0	1
	TOOLTxD	Output	×	0/1	0	0	1
	(KR2)	Input	1, 1	×	0	1	×
P13	ANI22 ^{Note 1}	Input	×	×	1	1	×
	TxD2	Output	×	0/1	0	0	1
	SO20	Output	×	0/1	0	0	1
	(KR3)	Input	1, 1	×	0	1	×
P14	ANI23 ^{Note 1}	Input	×	×	1	1	×
	RxD2	Input	×	×	0	1	×
	SI20	Input	×	×	0	1	×
	SDA20	I/O	×	1	0	0	1
	(KR4)	Input	1, 1	×	0	1	×
P15 ^{Note 3}	ANI24 ^{Note 1}	Input	×	×	1	1	×
	SCK20	Input	0	×	0	1	×
		Output	0	0/1	0	0	1
	SCL20	Output	0	0/1	0	0	1
	(KR5)	Input	1, 1	×	0	1	×
P16 ^{Note 3}	TI01	Input	×	—	—	1	×
	TO01	Output	×	—	—	0	0
	INTP5	Input	×	—	—	1	×

Remarks 1. ×: don't care

PIOR0, PIOR1: Bits 0, 1 of peripheral I/O redirection register

POM_{xx}: Port output mode register

PMC_{xx}: Port mode control register

PM_{xx}: Port mode register

P_{xx}: Port output latch

2. The relationship between pins and their alternate functions shown in this table indicates the relationship when a 64-pin product is used. In other products, alternate functions might be assigned to different pins, but even in this case, the PIOR_x, POM_{xx}, PMC_{xx}, PM_{xx}, and P_{xx} set in the same way.

3. Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection register (PIOR).

(The Notes 2 and 3 are described after the last table.)

Table 4-17. Settings of Port Related Register When Using Alternate Function (3/4)

Pin Name	Alternate Function		PIOR0, PIOR1	POM _{xx}	PMC _{xx}	PM _{xx}	P _{xx}
	Function Name	I/O					
P20 ^{Note 2}	ANI0 ^{Note 2}	Input	×	—	—	1	×
	AV _{REFP} ^{Note 2}	Input	×	—	—	1	×
P21 ^{Note 2}	ANI1 ^{Note 2}	Input	×	—	—	1	×
	AV _{REFM} ^{Note 2}	Input	×	—	—	1	×
P22 to P26 ^{Note 2}	ANI2 to ANI6 ^{Note 2}	Input	×	—	—	1	×
	(KR2) to (KR6) ^{Note 2}	Input	1, 0	—	—	1	×
P27 ^{Note 2}	ANI7 ^{Note 2}	Input	×	—	—	1	×
P30 ^{Note 3}	ANI27 ^{Note 1}	Input	×	—	1	1	×
	INTP3	Input	×	—	0	1	×
	RTC1HZ	Output	×	—	0	0	0
	SCK20	Input	×	—	0	1	×
		Output	×	—	0	0	1
	SCL20	Output	×	—	0	0	1
P31 ^{Note 3}	ANI29 ^{Note 1}	Input	×	—	1	1	×
	TI03	Input	×	—	0	1	×
	TO03	Output	×	—	0	0	0
	INTP4	Input	×	—	0	1	×
P40	TOOL0	I/O	×	—	—	×	×
P41	ANI30 ^{Note 1}	Input	×	—	1	1	×
	TI07	Input	×	—	0	1	×
	TO07	Output	×	—	0	0	0
P42	TI04	Input	×	—	—	1	×
	TO04	Output	×	—	—	0	0
P50	ANI26 ^{Note 1}	Input	×	×	1	1	×
	INTP1	Input	×	×	0	1	×
	SI11	Input	×	×	0	1	×
	SDA11	I/O	×	1	0	0	1
P51	ANI25 ^{Note 1}	Input	×	—	1	1	×
	INTP2	Input	×	—	0	1	×
	SO11	Output	×	—	0	0	1
P60	SCLA0	I/O	×	—	—	0	0
P61	SDAA0	I/O	×	—	—	0	0

Remarks 1. ×: don't care

PIOR0, PIOR1: Bits 0, 1 of peripheral I/O redirection register

POM_{xx}: Port output mode register

PMC_{xx}: Port mode control register

PM_{xx}: Port mode register

P_{xx}: Port output latch

2. The relationship between pins and their alternate functions shown in this table indicates the relationship when a 64-pin product is used. In other products, alternate functions might be assigned to different pins, but even in this case, the PIOR_x, POM_{xx}, PMC_{xx}, PM_{xx}, and P_{xx} set in the same way.

3. Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection register (PIOR).

(The Notes 1, 3 are described after the last table.)

Table 4-17. Settings of Port Related Register When Using Alternate Function (4/4)

Pin Name	Alternate Function		PIOR0, PIOR1	POM _{xx}	PMC _{xx}	PM _{xx}	P _{xx}
	Function Name	I/O					
P70	ANI28	Input	×	—	1	1	×
	KR0	Input	0, 0	—	0	1	×
	SCK21	Input	×	—	0	1	×
		Output	×	—	0	0	1
	SCL21	Output	×	—	0	0	1
P71	KR1	Input	0, 0	×	—	1	×
	SI21	Input	×	×	—	1	×
	SDA21	I/O	×	1	—	0	1
P72	KR2	Input	0, 0	—	—	1	×
	SO21	Output	×	—	—	0	1
P73	KR3	Input	0, 0	—	—	1	×
	SO01	Output	×	—	—	0	1
P74	KR4	Input	0, 0	×	—	1	×
	INTP8	Input	×	×	—	1	×
	SI01	Input	×	×	—	1	×
	SDA01	I/O	×	1	—	0	1
P75	KR5	Input	0, 0	—	—	1	×
	INTP9	Input	×	—	—	1	×
	SCK01	Input	×	—	—	1	×
		Output	×	—	—	0	1
	SCL01	Output	×	—	—	0	1
P76, P77	KR6, KR7	Input	0, 0	—	—	1	×
	INTP10, INTP11	Input	×	—	—	1	×
P120	ANI19 ^{Note 1}	Input	×	—	1	1	×
P137	INTP0	Input	×	—	—	—	×
P140	PCLBUZ0	Output	×	—	—	0	0
	INTP6	Input	×	—	—	1	×
P141	PCLBUZ1	Output	×	—	—	0	0
	INTP7	Input	×	—	—	1	×
P150 ^{Note 2}	ANI8 ^{Note 2}	Input	×	—	—	1	×
P151 to P154 ^{Note 2}	ANI9 to ANI12 ^{Note 2}	Input	×	—	—	1	×
	(KR6) to (KR9)	Input	1, 1	—	—	1	×

Remarks 1. ×: don't care

PIOR0, PIOR1: Bits 0, 1 of peripheral I/O redirection register

POM_{xx}: Port output mode register

PMC_{xx}: Port mode control register

PM_{xx}: Port mode register

P_{xx}: Port output latch

2. The relationship between pins and their alternate functions shown in this table indicates the relationship when a 64-pin product is used. In other products, alternate functions might be assigned to different pins, but even in this case, the PIOR_x, POM_{xx}, PMC_{xx}, PM_{xx}, and P_{xx} set in the same way.

3. Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection register (PIOR).

- Notes** 1. The functions of the ANI16/P03, ANI17/P02, ANI18/P10, ANI19/P120, ANI20/P11 to ANI24/P15, ANI25/P50, ANI26/P51, ANI27/P30, ANI28/P70, ANI29/P31, and ANI30/P41 pins can be selected by using the port mode control registers 0, 1, 3, 4, 5, 7, 12, 14 (PMC0, PMC1, PMC3, PMC5, PMC7, PMC12), analog input channel specification register (ADS), and port mode registers 0, 1, 3, 4, 5, 7, 12 (PM0, PM1, PM3, PM5, PM6, PM7, PM12).

Table 4-18. Setting Functions of ANI16/P03, ANI17/P02, ANI18/P10, ANI19/P120, ANI20/P11 to ANI24/P15, ANI25/P50, ANI26/P51, ANI27/P30, ANI28/P70, ANI29/P31, and ANI30/P41 pins

PMC0, PMC1, PMC3, PMC4, PMC5, PMC7, PMC12 Registers	PM0, PM1, PM3, PM4, PM5, PM7, PM12 Registers	ADS Register	ANI16/P03, ANI17/P02, ANI18/P10, ANI19/P120, ANI20/P11 to ANI24/P15, ANI25/P50, ANI26/P51, ANI27/P30, ANI28/P70, ANI29/P31, ANI30/P41 Pins
Digital I/O selection	Input mode	×	Digital input
	Output mode	×	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

2. The functions of the ANI0/P20 to ANI7/P27, ANI8/P150 to ANI12/P154 pins can be selected by using the A/D port configuration register (ADPC), analog input channel specification register (ADS), and port mode registers 2, 15 (PM2, PM15).

Table 4-19. Setting Functions of ANI0/P20 to ANI7/P27, ANI8/P150 to ANI12/P154 pins

ADPC Register	PM2, PM5 Register	ADS Register	ANI0/P20 to ANI7/P27, ANI8/P150 to ANI12/P154 Pins
Digital I/O selection	Input mode	×	Digital input
	Output mode	×	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

3. In the products other than 64-pin products, multiple alternate output functions are assigned to the pins. In such cases, the output from the alternate functions that are not used in any settings except the one indicated in **table 4-17** must be set to the same value as the one in the initial status. For more detail about the targets and the method of processing, refer to the section **4.6.2**.

Remark ×: don't care

4.6 Cautions When Using Port Function

4.6.1 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P10 is an output port, P11 to P16 are input ports (all pin statuses are high level), and the port latch value of port 1 is 00H, if the output of output port P10 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 1 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the RL78/G1A.

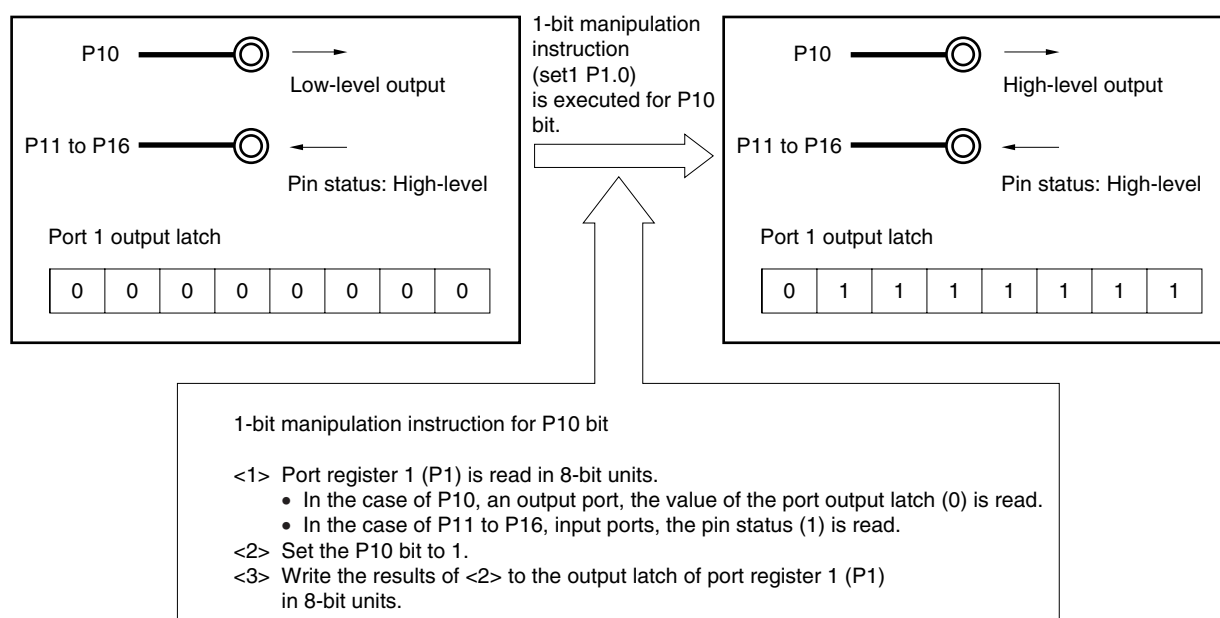
- <1> The Pn register is read in 8-bit units.
- <2> The targeted one bit is manipulated.
- <3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P10, which is an output port, is read, while the pin statuses of P11 to P16, which are input ports, are read. If the pin statuses of P11 to P16 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 4-48. Bit Manipulation Instruction (P10)



<R> 4.6.2 Notes on specifying the pin settings

If the output function of an alternate function is assigned to a pin that is also used as an output pin, the output of the unused alternate function must be set to its initial state so as to prevent conflicting outputs. For details about the alternate output function, see 4.5 Settings of Port Related Register When Using Alternate Function.

No specific setting is required for input pins because the output function of their alternate functions is disabled (the buffer output is Hi-Z).

Table 4-20. Handling of Unused Alternate Functions

Affected Unit	Output or I/O Pins of Unused Alternate Functions	Handling of Unused Alternate Functions
Timer array units	TOmn	Make sure that bit n (TOmn) of timer output register m (TOM) and bit n (TOEmn) of timer output enable register m (TOEm) are set to their initial value (0).
Clock/buzzer output circuit	PCLBUZn	Make sure that bit 7 (PCLOEn) of clock output select register n (CKSn) is set to its initial value (0).
Serial array units	$\overline{\text{SCKmn}}$, SCLmn	Make sure that bit n (SEmn) of serial channel enable status register m (SEm), and bit n+8 (CKOmn) of serial output register m (SOM) are set to their initial value (0 for SEmn and 1 for CKOmn).
Real-time clock register	RTC1HZ	Make sure that bit 5 (RCLOE1) of real-time clock control register 0 (RTCC0) is set to their initial value (0).

Example: P15/ANI24/PCLBUZ1/ $\overline{\text{SCK20}}$ /SCL20/(KR5) pin of 32-pin and 48-pin products

(1) When the pin is used as SCL20 output

- P15: Specify the output mode by setting PM16 of port mode register 1 to 0.
 ANI24, KR5: These are input pins, so this note does not apply.
 $\overline{\text{SCK20}}$: Changing the operation mode does not enable alternate functions assigned to pins on the same serial channel, and this note does not apply to such pins
 PCLBUZ1: This is an output pin, set PCLOEn of clock output select registers n (CKSn) to 0.

(2) When the pin is used as PCLBUZ1 output

- P15: Specify the output mode by setting PM16 of port mode register 1 to 0.
 ANI24, KR5: These are input pins, so this note does not apply.
 $\overline{\text{SCK20}}$: This is an I/O pin, so set SE10^{Note}, and CKO10 of serial array unit 1 to 0, and 0.
 SCL20: This is an alternate functions assigned to pins on the same serial channel at $\overline{\text{SCK20}}$, so use the same settings as the $\overline{\text{SCK20}}$.

Note SEm register is read-only because of the status register.

The STmn bit of STm register write to 1, SEmn bit is cleared.

Like SCL20 when using the P15/ANI24/PCLBUZ1/ $\overline{\text{SCK20}}$ /SCL20/(KR5) pin as the $\overline{\text{SCK20}}$ I/O pin, changing the operation mode does not enable alternate functions assigned to pins on the same serial channel, and this note does not apply to such pins. (If the CSI function is specified (MD102 = MD101 = 0), the pin does not function as a simplified I²C pin, and therefore SCL20 output is invalid.)

Disabling the unused functions, including blocks that are only used for input or do not have I/O, is recommended to lower power consumption.

CHAPTER 5 CLOCK GENERATOR

The presence or absence of connecting resonator pin for main system clock, connecting resonator pin for subsystem clock, external clock input pin for main system clock, and external clock input pin for subsystem clock, depends on the product.

Output pin	25, 32-pin	48, 64-pin
X1, X2 pins	√	√
EXCLK pin	√	√
XT1, XT2 pins	–	√
EXCLKS pin	–	√

Note The 25 and 32-pin products don't have the subsystem clock.

5.1 Functions of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.

The following three kinds of system clocks and clock oscillators are selectable.

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of $f_x = 1$ to 20 MHz by connecting a resonator to X1 and X2.

Oscillation can be stopped by executing the STOP instruction or setting of the MSTOP bit (bit 7 of the clock operation status control register (CSC)).

<2> High-speed on-chip oscillator

The frequency at which to oscillate can be selected from among $f_{IH} = 32, 24, 16, 12, 8, 4$, or 1 MHz (typ.) by using the option byte (000C2H). After a reset release, the CPU always starts operating with this high-speed on-chip oscillator clock. Oscillation can be stopped by executing the STOP instruction or setting the HIOSTOP bit (bit 0 of the CSC register).

<R> The frequency specified by using an option byte can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV). For details about the frequency, see Figure 5-9 Format of High-speed On-chip Oscillator Frequency Select Register (HOCODIV).

The frequencies that can be specified for the high-speed on-chip oscillator by using the option byte and the high-speed on-chip oscillator frequency select register (HOCODIV) are shown below.

Power Supply Voltage	Flash Operation Mode	Oscillation Frequency (MHz)									
		1	2	3	4	6	8	12	16	24	32
$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	HS (high-speed main) mode	√	√	√	√	√	√	√	√	√	√
$2.4\text{ V} \leq V_{DD} < 3.6\text{ V}$		√	√	√	√	√	√	√	√	–	–
$1.8\text{ V} \leq V_{DD} < 3.6\text{ V}$	LS (low-speed main) mode	√	√	√	√	√	√	–	–	–	–
$1.6\text{ V} \leq V_{DD} < 3.6\text{ V}$	LV (low-voltage main) mode	√	√	–	√	–	–	–	–	–	–

An external main system clock ($f_{EX} = 1$ to 20 MHz) can also be supplied from the EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or setting of the MSTOP bit.

As the main system clock, a high-speed system clock (X1 clock or external main system clock) or high-speed on-chip oscillator clock can be selected by setting of the MCM0 bit (bit 4 of the system clock control register (CKC)).

(2) Subsystem clock**• XT1 clock oscillator**

This circuit oscillates a clock of $f_{XT} = 32.768$ kHz by connecting a 32.768 kHz resonator to XT1 and XT2. Oscillation can be stopped by setting the XTSTOP bit (bit 6 of the clock operation status control register (CSC)).

An external subsystem clock ($f_{EXS} = 32.768$ KHz) can also be supplied from the EXCLKS/XT2/P124 pin. An external subsystem clock input can be disabled by the setting of the XTSTOP bit.

(3) Low-speed on-chip oscillator clock (Low-speed on-chip oscillator)

This circuit oscillates a clock of $f_{IL} = 15$ kHz (TYP.).

The low-speed on-chip oscillator clock cannot be used as the CPU clock.

Only the following peripheral hardware runs on the low-speed on-chip oscillator clock.

- Watchdog timer
- Real-time clock
- 12-bit interval timer

This clock operates when bit 4 (WDTON) of the option byte (000C0H), bit 4 (WUTMMCK0) of the operation speed mode control register (OSMC), or both are set to 1.

However, when WDTON = 1, WUTMMCK0 = 0, and bit 0 (WDSTBYON) of the option byte (000C0H) is 0, oscillation of the low-speed on-chip oscillator stops if the HALT or STOP instruction is executed.

Caution The low-speed on-chip oscillator clock (f_{IL}) can only be selected as the real-time clock operation clock when the fixed-cycle interrupt function is used.

Remark

f_X :	X1 clock oscillation frequency
f_{IH} :	High-speed on-chip oscillator clock frequency
f_{EX} :	External main system clock frequency
f_{XT} :	XT1 clock oscillation frequency
f_{EXS} :	External subsystem clock frequency
f_{IL} :	Low-speed on-chip oscillator clock frequency

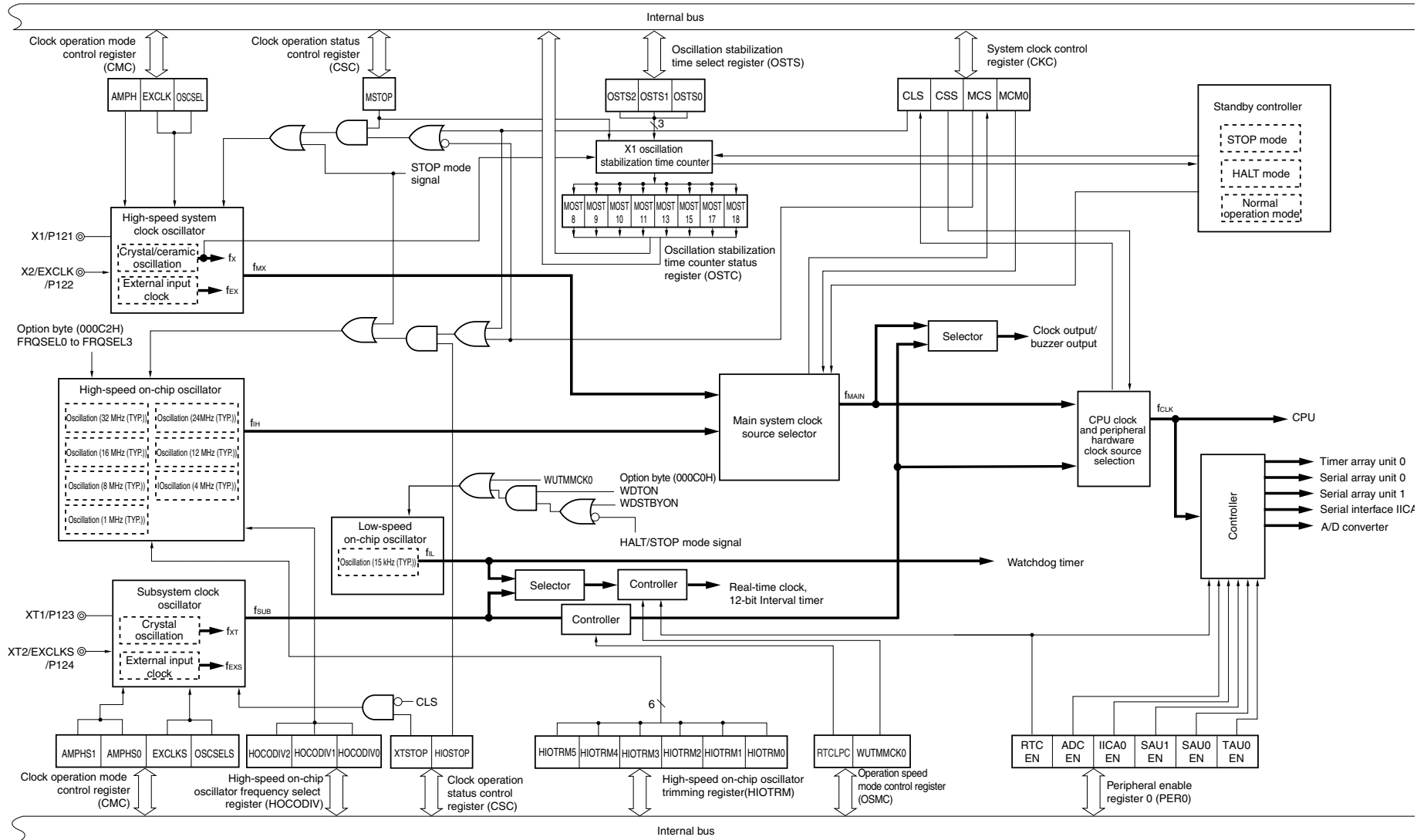
5.2 Configuration of Clock Generator

The clock generator includes the following hardware.

Table 5-1. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode control register (CMC) System clock control register (CKC) Clock operation status control register (CSC) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS) Peripheral enable register 0 (PER0) Operation speed mode control register (OSMC) High-speed on-chip oscillator frequency select register (HOCODIV) High-speed on-chip oscillator trimming register (HIOTRM)
Oscillators	X1 oscillator XT1 oscillator High-speed on-chip oscillator Low-speed on-chip oscillator

Figure 5-1. Block Diagram of Clock Generator



(Remark is listed on the next page after next.)

Remark	fx:	X1 clock oscillation frequency
	f_{IH}:	High-speed on-chip oscillator clock frequency
	f_{EX}:	External main system clock frequency
	f_{MX}:	High-speed system clock frequency
	f_{MAIN}:	Main system clock frequency
	f_{XT}:	XT1 clock oscillation frequency
	f_{EXS}:	External subsystem clock frequency
	f_{SUB}:	Subsystem clock frequency
	f_{CLK}:	CPU/peripheral hardware clock frequency
	f_{IL}:	Low-speed on-chip oscillator clock frequency

5.3 Registers Controlling Clock Generator

The following nine registers are used to control the clock generator.

- Clock operation mode control register (CMC)
- System clock control register (CKC)
- Clock operation status control register (CSC)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)
- Peripheral enable register 0 (PER0)
- Operation speed mode control register (OSMC)
- High-speed on-chip oscillator frequency select register (HOCODIV)
- High-speed on-chip oscillator trimming register (HIOTRM)

5.3.1 Clock operation mode control register (CMC)

This register is used to set the operation mode of the X1/P121, X2/EXCLK/P122, XT1/P123, and XT2/EXCLKS/P124 pins, and to select a gain of the oscillator.

The CMC register can be written only once by an 8-bit memory manipulation instruction after reset release. This register can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 5-2. Format of Clock Operation Mode Control Register (CMC)

Address: FFFA0H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL	EXCLKS	OSCSELS	0	AMPHS1	AMPHS0	AMPH

EXCLK	OSCSEL	High-speed system clock pin operation mode	X1/P121 pin	X2/EXCLK/P122 pin
0	0	Input port mode	Input port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

EXCLKS	OSCSELS	Subsystem clock pin operation mode	XT1/P123 pin	XT2/EXCLKS/P124 pin
0	0	Input port mode	Input port	
0	1	XT1 oscillation mode	Crystal resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

AMPHS1	AMPHS0	XT1 oscillator oscillation mode selection
0	0	Low power consumption oscillation (default)
0	1	Normal oscillation
1	0	Ultra-low power consumption oscillation
1	1	Setting prohibited

AMPH	Control of X1 clock oscillation frequency
0	1 MHz ≤ f _x ≤ 10 MHz
1	10 MHz < f _x ≤ 20 MHz

Note As the XT oscillator becomes oscillation mode with lower power consumption, then its oscillation margin becomes smaller.

- Cautions**
1. The CMC register can be written only once after reset release, by an 8-bit memory manipulation instruction. When using the CMC register with its initial value (00H), be sure to set the register to 00H after a reset ends in order to prevent malfunction due to a program loop. Such a malfunction becomes unrecoverable when a value other than 00H is mistakenly written.
 2. After reset release, set the CMC register before X1 or XT1 oscillation is started as set by the clock operation status control register (CSC).
 3. Be sure to set the AMPH bit to 1 if the X1 clock oscillation frequency exceeds 10 MHz.
 4. Specify the settings for the AMPH, AMPHS1, and AMPHS0 bits while f_{IH} is selected as f_{CLK} after a reset ends (before f_{CLK} is switched to f_{MX} or f_{SUB}).
 5. Oscillation stabilization time of f_{XT}, counting on the software.
 6. Although the maximum system clock frequency is 32 MHz, the maximum frequency of the X1 oscillator is 20 MHz.

(Cautions and Remark are given on the next page.)

7. The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption. Note the following points when designing the circuit.
- Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.
 - Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the ultra-low power consumption oscillation (AMPHS1, AMPHS0 = 1, 0) is selected.
 - Configure the circuit of the circuit board, using material with little wiring resistance.
 - Place a ground pattern that has the same potential as V_{SS} as much as possible near the XT1 oscillator.
 - Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.
 - The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.
 - When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.

Remark fx: X1 clock frequency

5.3.2 System clock control register (CKC)

This register is used to select a CPU/peripheral hardware clock and a main system clock.

The CKC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 5-3. Format of System Clock Control Register (CKC)

Address: FFFA4H After reset: 00H R/W^{Note 1}

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
CKC	CLS	CSS	MCS	MCM0	0	0	0	0
CLS	Status of CPU/peripheral hardware clock (f_{CLK})							
0	Main system clock (f_{MAIN})							
1	Subsystem clock (f_{SUB})							
CSS	Selection of CPU/peripheral hardware clock (f_{CLK})							
0	Main system clock (f_{MAIN})							
1 ^{Note 2}	Subsystem clock (f_{SUB})							
MCS	Status of Main system clock (f_{MAIN})							
0	High-speed on-chip oscillator clock (f_{IH})							
1	High-speed system clock (f_{MX})							
MCM0 ^{Note 2}	Main system clock (f_{MAIN}) operation control							
0	Selects the high-speed on-chip oscillator clock (f_{IH}) as the main system clock (f_{MAIN})							
1	Selects the high-speed system clock (f_{MX}) as the main system clock (f_{MAIN})							

Notes 1. Bits 7 and 5 are read-only.

2. Changing the value of the MCM0 bit is prohibited while the CSS bit is set to 1.

Cautions 1. Be sure to set bit 3 to 0 to 0.

- The clock set by the CSS bit is supplied to the CPU and peripheral hardware. If the CPU clock is changed, therefore, the clock supplied to peripheral hardware (except the real-time clock, 12-bit interval timer, clock output/buzzer output, and watchdog timer) is also changed at the same time. Consequently, stop each peripheral function when changing the CPU/peripheral hardware clock.
- If the subsystem clock is used as the peripheral hardware clock, the operations of the A/D converter and IICA are not guaranteed. For the operating characteristics of the peripheral hardware, refer to the chapters describing the various peripheral hardware as well as CHAPTER 29 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$) (TARGET), CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$) (TARGET).

Remark f_{IH} : High-speed on-chip oscillator clock frequency
 f_{MX} : High-speed system clock frequency
 f_{MAIN} : Main system clock frequency
 f_{SUB} : Subsystem clock frequency

5.3.3 Clock operation status control register (CSC)

This register is used to control the operations of the high-speed system clock, high-speed on-chip oscillator clock, and subsystem clock (except the low-speed on-chip oscillator clock).

The CSC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to C0H.

Figure 5-4. Format of Clock Operation Status Control Register (CSC)

Address: FFFA1H After reset: C0H R/W

Symbol	<7>	<6>	5	4	3	2	1	<0>
CSC	MSTOP	XTSTOP	0	0	0	0	0	HIOSTOP

MSTOP	High-speed system clock operation control		
	X1 oscillation mode	External clock input mode	Input port mode
0	X1 oscillator operating	External clock from EXCLK pin is valid	Input port
1	X1 oscillator stopped	External clock from EXCLK pin is invalid	

XTSTOP	Subsystem clock operation control		
	XT1 oscillation mode	External clock input mode	Input port mode
0	XT1 oscillator operating	External clock from EXCLKS pin is valid	Input port
1	XT1 oscillator stopped	External clock from EXCLKS pin is invalid	

HIOSTOP	High-speed on-chip oscillator clock operation control		
0	High-speed on-chip oscillator operating		
1	High-speed on-chip oscillator stopped		

- Cautions**
1. After reset release, set the clock operation mode control register (CMC) before setting the CSC register.
 2. Set the oscillation stabilization time select register (OSTS) before setting the MSTOP bit to 0 after releasing reset. Note that if the OSTS register is being used with its default settings, the OSTS register is not required to be set here.
 3. To start X1 oscillation as set by the MSTOP bit, check the oscillation stabilization time of the X1 clock by using the oscillation stabilization time counter status register (OSTC).
 4. When starting XT1 oscillation by setting the XSTOP bit, wait for oscillation of the subsystem clock to stabilize by setting a wait time using software.
 5. Do not stop the clock selected for the CPU peripheral hardware clock (f_{CLK}) with the OSC register.
 6. The setting of the flags of the register to stop clock oscillation (invalidate the external clock input) and the condition before clock oscillation is to be stopped are as Table 5-2.

Table 5-2. Stopping Clock Method

Clock	Condition Before Stopping Clock (Invalidating External Clock Input)	Setting of CSC Register Flags
X1 clock	CPU and peripheral hardware clocks operate with a clock other than the high-speed system clock. (CLS = 0 and MCS = 0, or CLS = 1)	MSTOP = 1
External main system clock		
XT1 clock	CPU and peripheral hardware clocks operate with a clock other than the subsystem clock. (CLS = 0)	XTSTOP = 1
External subsystem clock		
High-speed on-chip oscillator clock	CPU and peripheral hardware clocks operate with a clock other than the high-speed on-chip oscillator clock. (CLS = 0 and MCS = 1, or CLS = 1)	HIOSTOP = 1

5.3.4 Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter.

The X1 clock oscillation stabilization time can be checked in the following case,

- If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating.

The OSTC register can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset signal is generated, the STOP instruction and MSTOP (bit 7 of clock operation status control register (CSC)) = 1 clear the OSTC register to 00H.

Remark The oscillation stabilization time counter starts counting in the following cases.

- When oscillation of the X1 clock starts (EXCLK, OSCSEL = 0, 1 → MSTOP = 0)
- When the STOP mode is released

Figure 5-5. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFFA2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18

MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18	Oscillation stabilization time status		
									$f_x = 10 \text{ MHz}$	$f_x = 20 \text{ MHz}$
0	0	0	0	0	0	0	0	$2^8/f_x \text{ max.}$	25.6 μs max.	12.8 μs max.
1	0	0	0	0	0	0	0	$2^9/f_x \text{ min.}$	25.6 μs min.	12.8 μs min.
1	1	0	0	0	0	0	0	$2^9/f_x \text{ min.}$	51.2 μs min.	25.6 μs min.
1	1	1	0	0	0	0	0	$2^{10}/f_x \text{ min.}$	102.4 μs min.	51.2 μs min.
1	1	1	1	0	0	0	0	$2^{11}/f_x \text{ min.}$	204.8 μs min.	102.4 μs min.
1	1	1	1	1	0	0	0	$2^{13}/f_x \text{ min.}$	819.2 μs min.	409.6 μs min.
1	1	1	1	1	1	0	0	$2^{15}/f_x \text{ min.}$	3.27 ms min.	1.64 ms min.
1	1	1	1	1	1	1	0	$2^{17}/f_x \text{ min.}$	13.11 ms min.	6.55 ms min.
1	1	1	1	1	1	1	1	$2^{18}/f_x \text{ min.}$	26.21 ms min.	13.11 ms min.

Cautions 1. After the above time has elapsed, the bits are set to 1 in order from the MOST8 bit and remain 1.

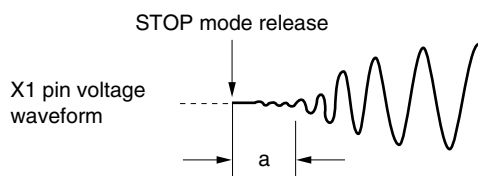
2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the oscillation stabilization time select register (OSTS).

In the following cases, set the oscillation stabilization time of the OSTS register to the value greater than the count value which is to be checked by the OSTC register.

- If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating.

(Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_x : X1 clock oscillation frequency

5.3.5 Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation automatically waits for the time set using the OSTS register after the STOP mode is released.

When the high-speed on-chip oscillator clock is selected as the CPU clock, confirm with the oscillation stabilization time counter status register (OSTC) that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using the OSTC register.

The OSTS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets the OSTS register to 07H.

Figure 5-6. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFFA3H After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				$f_x = 10 \text{ MHz}$	$f_x = 20 \text{ MHz}$
0	0	0	$2^8/f_x$	25.6 μs	12.8 μs
0	0	1	$2^9/f_x$	51.2 μs	25.6 μs
0	1	0	$2^{10}/f_x$	102.4 μs	51.2 μs
0	1	1	$2^{11}/f_x$	204.8 μs	102.4 μs
1	0	0	$2^{13}/f_x$	819.2 μs	409.6 μs
1	0	1	$2^{15}/f_x$	3.27 ms	1.64 ms
1	1	0	$2^{17}/f_x$	13.11 ms	6.55 ms
1	1	1	$2^{18}/f_x$	26.21 ms	13.11 ms

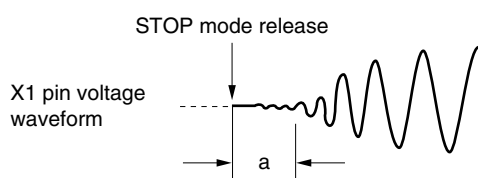
Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.

2. Change the setting of the OSTS register before setting the MSTOP bit of the clock operation status control register (CSC) to 0.
3. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.
4. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the OSTS register.

In the following cases, set the oscillation stabilization time of the OSTS register to the value greater than the count value which is to be checked by the OSTC register after the oscillation starts.

- If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating. (Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)

5. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_x : X1 clock oscillation frequency

5.3.6 Peripheral enable register 0 (PER0)

These registers are used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

To use the peripheral functions below, which are controlled by this register, set (1) the bit corresponding to each function before specifying the initial settings of the peripheral functions.

- Real-time clock, 12-bit interval timer
- A/D converter
- Serial interface IICA0
- Serial array unit 1
- Serial array unit 0
- Timer array unit 0

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 5-7. Format of Peripheral Enable Register 0 (PER0) (1/3)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	IICA0EN	SAU1EN Note	SAU0EN	0	TAU0EN

RTCEN	Control of real-time clock (RTC) and 12-bit interval timer input clock supply
0	Stops input clock supply. • SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be written. • The real-time clock (RTC) and 12-bit interval timer are in the reset status.
1	Enables input clock supply. • SFR used by the real-time clock (RTC) and 12-bit interval timer can be read and written.

Note 32, 48, and 64-pin products only.

Caution Be sure to clear the following bits to 0.

25-pin products: bits 1, 3, 6

32, 48, 64-pin products: bits 1, 6

Figure 5-7. Format of Peripheral Enable Register 0 (PER0) (2/3)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	IICA0EN	SAU1EN Note	SAU0EN	0	TAU0EN

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. - SFR used by the A/D converter cannot be written. - The A/D converter is in the reset status.
1	Enables input clock supply. SFR used by the A/D converter can be read and written.

IICA0EN	Control of serial interface IICA0 input clock supply
0	Stops input clock supply. - SFR used by the serial interface IICA0 cannot be written. - The serial interface IICA0 is in the reset status.
1	Enables input clock supply. SFR used by the serial interface IICA0 can be read and written.

SAU1EN	Control of serial array unit 1 input clock supply
0	Stops input clock supply. - SFR used by the serial array unit 1 cannot be written. - The serial array unit 1 is in the reset status.
1	Enables input clock supply. SFR used by the serial array unit 1 can be read and written.

Note 32, 48, and 64-pin products only.**Caution** Be sure to clear the following bits to 0.

25-pin products: bits 1, 3, 6

32, 48, 64-pin products: bits 1, 6

Figure 5-7. Format of Peripheral Enable Register 0 (PER0) (3/3)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	IICA0EN	SAU1EN Note	SAU0EN	0	TAU0EN

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops input clock supply. - SFR used by the serial array unit 0 cannot be written. - The serial array unit 0 is in the reset status.
1	Enables input clock supply. SFR used by the serial array unit 0 can be read and written.

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. - SFR used by timer array unit 0 cannot be written. - Timer array unit 0 is in the reset status.
1	Enables input clock supply. SFR used by timer array unit 0 can be read and written.

Note 32, 48, and 64-pin products only.**Caution** Be sure to clear the following bits to 0.

25-pin products: bits 1, 3, 6

32, 48, 64-pin products: bits 1, 6

5.3.7 Operation speed mode control register (OSMC)

This register is used to reduce power consumption by stopping unnecessary clock functions.

If the RTCLPC bit is set to 1, power consumption can be reduced, because clock supply to the peripheral functions, except the real-time clock and 12-bit interval timer, is stopped in STOP mode or HALT mode while subsystem clock is selected as CPU clock. Set bit 7 (RTCEN) of peripheral enable registers 0 (PER0) to 1 before this setting.

In addition, the OSMC register can be used to select the operation clock of the real-time clock and 12-bit interval timer.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 5-8. Format of Operation Speed Mode Control Register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

RTCLPC	Setting in STOP mode or HALT mode while subsystem clock is selected as CPU clock
0	Enables supply of subsystem clock to peripheral functions (See Table 18-1 for peripheral functions whose operations are enabled.)
1	Stops supply of subsystem clock to peripheral functions other than real-time clock and 12-bit interval timer.

WUTMMCK0	Selection of operation clock for real-time clock and 12-bit interval timer.
0	Subsystem clock (f_{SUB})
1	Low-speed on-chip oscillator clock (f_{IL})

5.3.8 High-speed on-chip oscillator frequency select register (HOCODIV)

The frequency of the high-speed on-chip oscillator which is set by an option byte (000C2H) can be changed by using high-speed on-chip oscillator frequency select register (HOCODIV). However, the selectable frequency depends on the FRQSEL3 bit of the option byte (000C2H).

The HOCODIV register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to default value (undefined).

Figure 5-9. Format of High-speed On-chip Oscillator Frequency Select Register (HOCODIV)

Address: F00A8H After reset: undefined R/W

Symbol	7	6	5	4	3	2	1	0
HOCODIV	0	0	0	0	0	HOCODIV2	HOCODIV1	HOCODIV0

HOCODIV2	HOCODIV1	HOCODIV0	High-Speed On-Chip Oscillator Clock Frequency	
			FRQSEL3 Bit is 0	FRQSEL3 Bit of is 1
0	0	0	24 MHz	32 MHz
0	0	1	12 MHz	16 MHz
0	1	0	6 MHz	8 MHz
0	1	1	3 MHz	4 MHz
1	0	0	Setting prohibited	2 MHz
1	0	1	Setting prohibited	1 MHz
Other than above			Setting prohibited	

Cautions 1. When changing the frequency by using the HOCODIV register, specify a frequency in the voltage range corresponding to the flash operating mode specified in the option byte (000C2H).

Option Byte (000C2H) Value		Flash Operation Mode	Operating Frequency Range	Operating Voltage Range
CMODE1	CMODE0			
0	0	LV (low-voltage main) mode	1 to 4 MHz	1.6 to 3.6 V
1	0	LS (low-speed main) mode	1 to 8 MHz	1.8 to 3.6 V
1	1	HS (high-speed main) mode	1 to 16 MHz	2.4 to 3.6 V
			1 to 32 MHz	2.7 to 3.6 V

2. Change the HOCODIV register value while the high-speed on-chip oscillator clock (f_{IH}) is selected as the CPU/peripheral hardware clock (f_{CLK}).
3. After the frequency is changed using the HOCODIV register, the new frequency is applied after the period below has elapsed.
 - Three clock cycles at the frequency before change
 - Up to three wait cycles of CPU/peripheral hardware clock at the frequency after change

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

This register is used to adjust the accuracy of the high-speed on-chip oscillator.

With self-measurement of the high-speed on-chip oscillator frequency via a timer using high-accuracy external clock input (timer array unit), and so on, the accuracy can be adjusted.

The HIOTRM register can be set by an 8-bit memory manipulation instruction.

Caution The frequency will vary if the temperature and V_{DD} pin voltage change after accuracy adjustment. When the temperature and V_{DD} voltage change, accuracy adjustment must be executed regularly or before the frequency accuracy is required.

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: **Note** R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	↑
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
• • •						
1	1	1	1	1	0	↓
1	1	1	1	1	1	Maximum speed

Note The reset value differs for each chip.

5.4 System Clock Oscillator

5.4.1 X1 oscillator

The X1 oscillator oscillates with a crystal resonator or ceramic resonator (1 to 20 MHz) connected to the X1 and X2 pins.

An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

To use the X1 oscillator, set bits 7 and 6 (EXCLK, OSCSEL) of the clock operation mode control register (CMC) as follows.

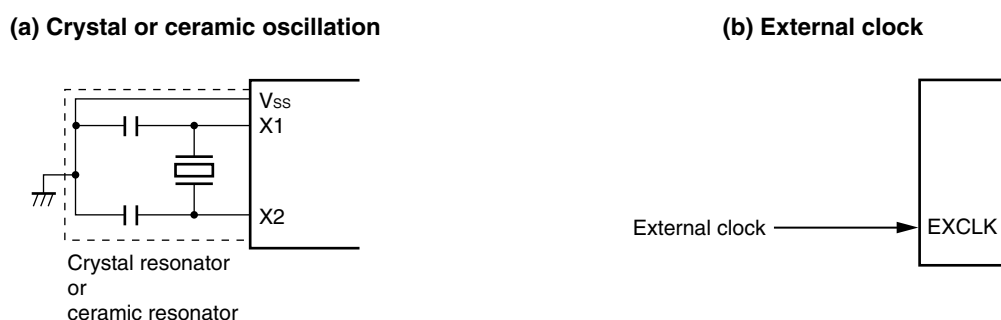
- Crystal or ceramic oscillation: EXCLK, OSCSEL = 0, 1
- External clock input: EXCLK, OSCSEL = 1, 1

When the X1 oscillator is not used, set the input port mode (EXCLK, OSCSEL = 0, 0).

When the pins are not used as input port pins, either, see **Table 2-3 Connection of Unused Pins (64-pin products)**.

Figure 5-11 shows an example of the external circuit of the X1 oscillator.

Figure 5-11. Example of External Circuit of X1 Oscillator



Cautions are listed on the next page.

5.4.2 XT1 oscillator

The XT1 oscillator oscillates with a crystal resonator (standard: 32.768 kHz) connected to the XT1 and XT2 pins.

To use the XT1 oscillator, set bit 4 (OSCSELS) of the clock operation mode control register (CMC) to 1.

An external clock can also be input. In this case, input the clock signal to the EXCLKS pin.

To use the XT1 oscillator, set bits 5 and 4 (EXCLKS, OSCSELS) of the clock operation mode control register (CMC) as follows.

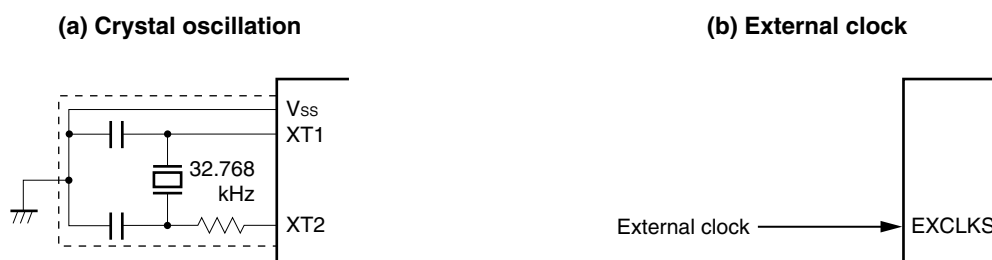
- Crystal or ceramic oscillation: EXCLKS, OSCSELS = 0, 1
- External clock input: EXCLKS, OSCSELS = 1, 1

When the XT1 oscillator is not used, set the input port mode (EXCLKS, OSCSELS = 0, 0).

When the pins are not used as input port pins, either, see **Table 2-3 Connection of Unused Pins (64-pin products)**.

Figure 5-12 shows an example of the external circuit of the XT1 oscillator.

Figure 5-12. Example of External Circuit of XT1 Oscillator



Caution 1. When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in the Figures 5-10 and 5-11 to avoid an adverse effect from wiring capacitance.

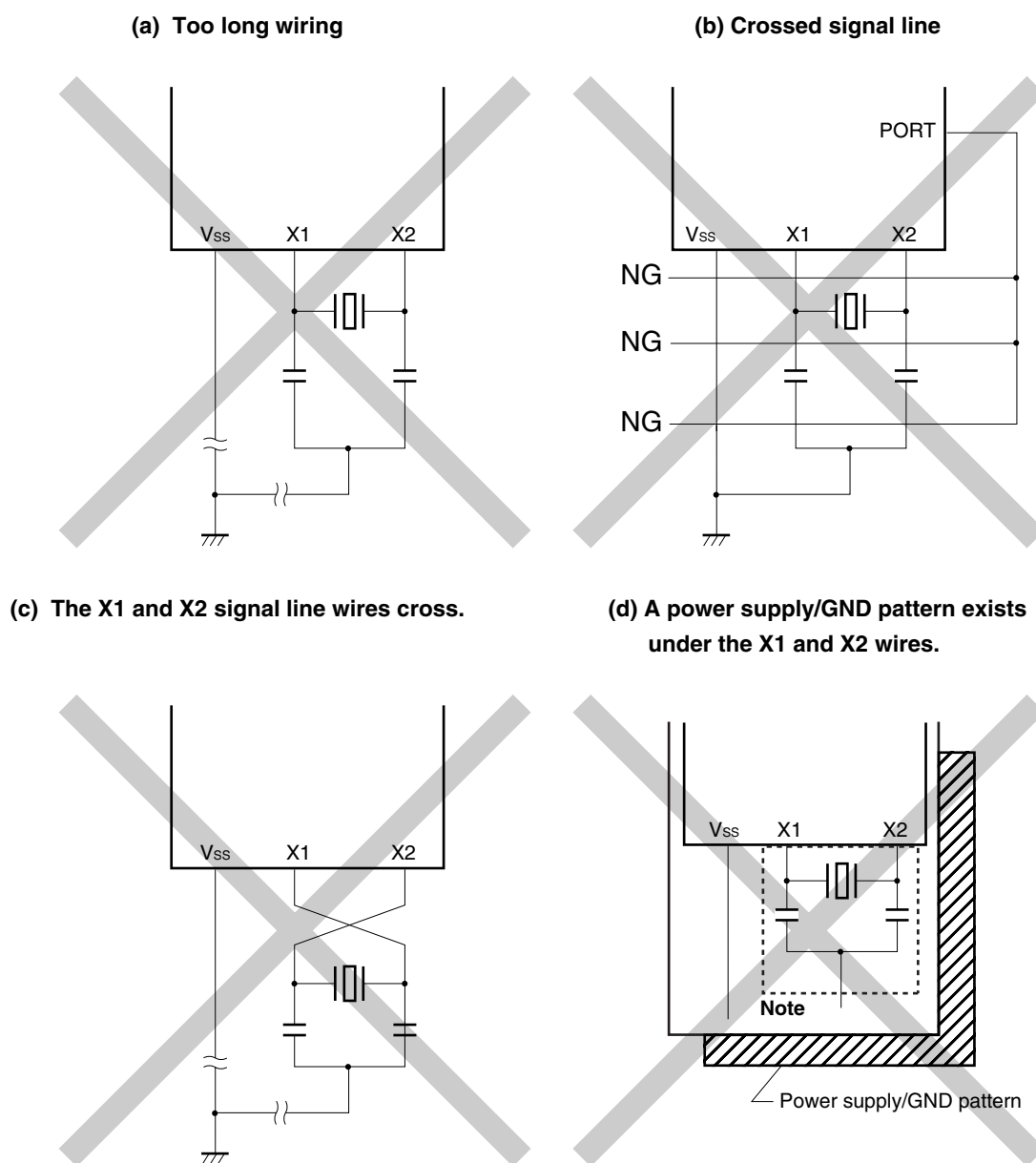
- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS} . Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption. Note the following points when designing the circuit.

- Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.
- Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the ultra-low power consumption oscillation (AMPHS1, AMPHS0 = 1, 0) is selected.
- Configure the circuit of the circuit board, using material with little wiring resistance.
- Place a ground pattern that has the same potential as V_{SS} as much as possible near the XT1 oscillator.
- Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.
- The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.
- When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.

Figure 5-13 shows examples of incorrect resonator connection.

Figure 5-13. Examples of Incorrect Resonator Connection (1/2)



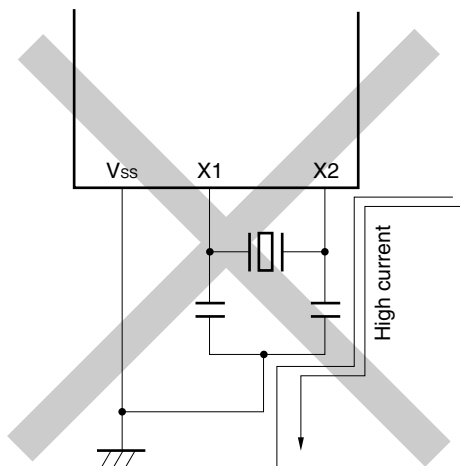
Note Do not place a power supply/GND pattern under the wiring section (section indicated by a broken line in the figure) of the X1 and X2 pins and the resonators in a multi-layer board or double-sided board.

Do not configure a layout that will cause capacitance elements and affect the oscillation characteristics.

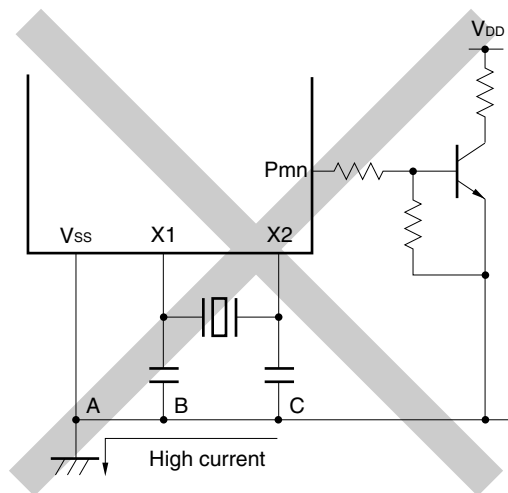
Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

Figure 5-13. Examples of Incorrect Resonator Connection (2/2)

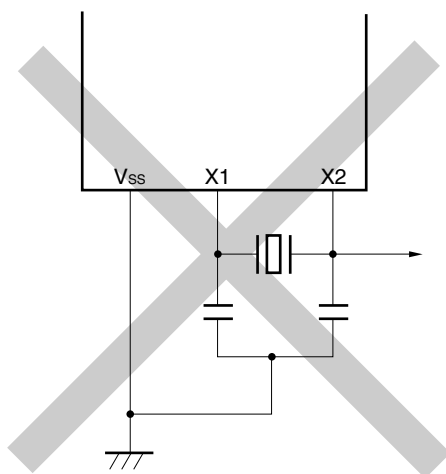
(e) Wiring near high alternating current



(f) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)



(g) Signals are fetched



Caution When X2 and XT1 are wired in parallel, the crosstalk noise of X2 may increase with XT1, resulting in malfunctioning.

Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

5.4.3 High-speed on-chip oscillator

The high-speed on-chip oscillator is incorporated in the RL78/G1A. The frequency can be selected from among 32, 24, 16, 12, 8, 4, or 1 MHz by using the option byte (000C2H). Oscillation can be controlled by bit 0 (HIOSTOP) of the clock operation status control register (CSC). The high-speed on-chip oscillator automatically starts oscillating after reset release.

5.4.4 Low-speed on-chip oscillator

The low-speed on-chip oscillator is incorporated in the RL78/G1A.

The low-speed on-chip oscillator clock is used only as the watchdog timer, real-time clock, and 12-bit interval timer clock. The low-speed on-chip oscillator clock cannot be used as the CPU clock.

This clock operates when bit 4 (WDTON) of the option byte (000C0H), bit 4 (WUTMMCK0) of the operation speed mode control register (OSMC), or both are set to 1.

Unless the watchdog timer is stopped and WUTMMCK0 is a value other than zero, oscillation of the low-speed on-chip oscillator continues. While the watchdog timer operates, the low-speed on-chip oscillator clock does not stop even if the program freezes.

5.5 Clock Generator Operation

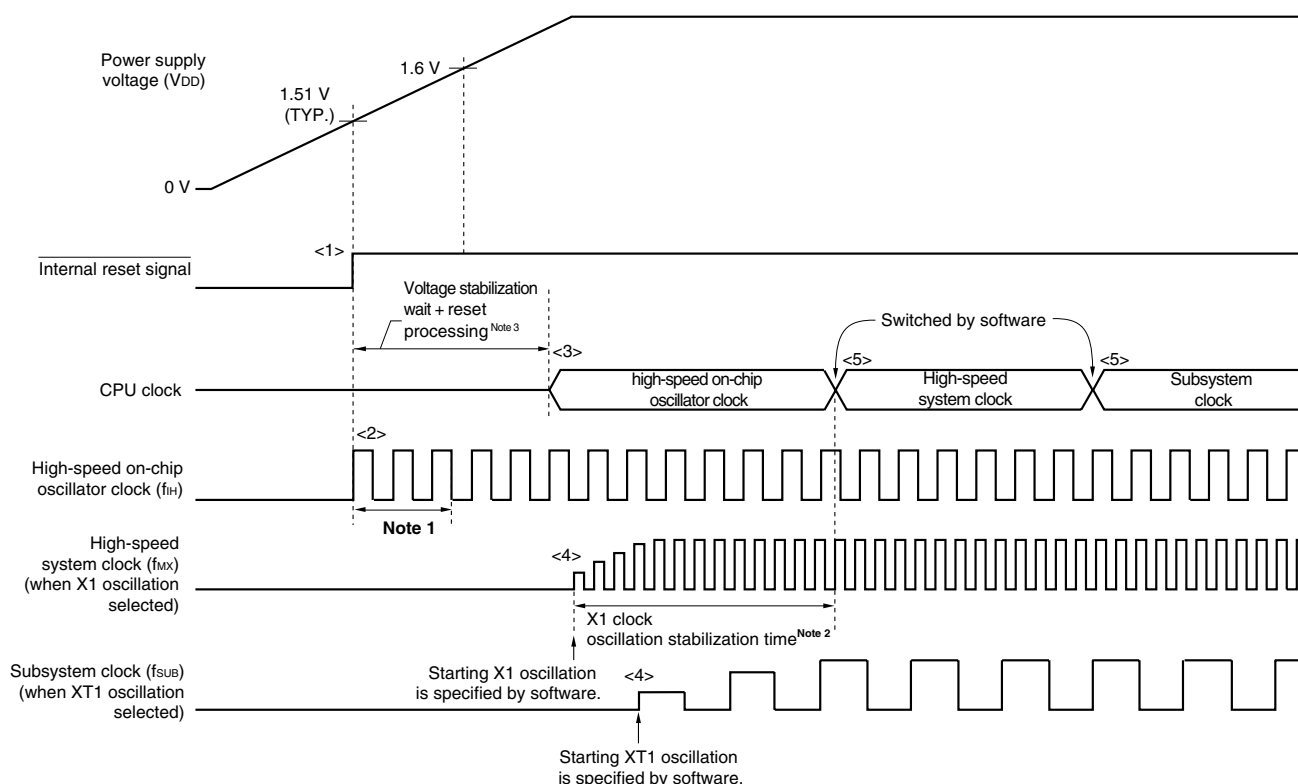
The clock generator generates the following clocks and controls the operation modes of the CPU, such as standby mode (see **Figure 5-1**).

- Main system clock f_{MAIN}
 - High-speed system clock f_{MX}
 - X1 clock f_X
 - External main system clock f_{EX}
 - High-speed on-chip oscillator clock f_{IH}
- Subsystem clock f_{SUB}
 - XT1 clock f_{XT}
 - External subsystem clock f_{EXS}
- Low-speed on-chip oscillator clock f_{IL}
- CPU/peripheral hardware clock f_{CLK}

The CPU starts operation when the high-speed on-chip oscillator starts outputting after a reset release in the RL78/G1A.

When the power supply voltage is turned on, the clock generator operation is shown in Figure 5-14.

Figure 5-14. Clock Generator Operation When Power Supply Voltage Is Turned On



- <1> When the power is turned on, an internal reset signal is generated by the power-on-reset (POR) circuit.
- <2> When the power supply voltage exceeds 1.51 V (TYP.), the reset is released and the high-speed on-chip oscillator automatically starts oscillation.
- <3> The CPU starts operation on the high-speed on-chip oscillator clock after a reset processing such as waiting for the voltage of the power supply or regulator to stabilize has been performed after reset release.
- <4> Set the start of oscillation of the X1 or XT1 clock via software (see 5.6.2 Example of setting X1 oscillation clock and 5.6.3 Example of setting XT1 oscillation clock).
- <5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see 5.6.2 Example of setting X1 oscillation clock and 5.6.3 Example of setting XT1 oscillation clock).

Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

2. When releasing a reset, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC).

<R> 3. Refer to 20.3 Operation of Power-on-reset Circuit at voltage stabilization wait + POR processing time.

Caution It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

5.6 Controlling Clock

5.6.1 Example of setting high-speed on-chip oscillator

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the high-speed on-chip oscillator clock. The frequency of the high-speed on-chip oscillator can be selected from 32, 24, 16, 12, 8, 4, and 1 MHz by using FRQSEL0 to FRQSEL3 of the option byte (000C2H).

[Option byte setting]

Address: 000C2H

Option byte (000C2H)	7	6	5	4	3	2	1	0
	CMODE1	CMODE0			FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0
	0/1	0/1	1	0	0/1	0/1	0/1	0/1

CMODE1	CMODE0	Setting of flash operation mode	
0	0	LV (low voltage main) mode	$V_{DD} = 1.6\text{ V to }3.6\text{ V @ }1\text{ MHz to }4\text{ MHz}$
1	0	LS (low speed main) mode	$V_{DD} = 1.8\text{ V to }3.6\text{ V @ }1\text{ MHz to }8\text{ MHz}$
1	1	HS (high speed main) mode	$V_{DD} = 2.4\text{ V to }3.6\text{ V @ }1\text{ MHz to }16\text{ MHz}$ $V_{DD} = 2.7\text{ V to }3.6\text{ V @ }1\text{ MHz to }32\text{ MHz}$

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
1	0	0	0	32 MHz
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
1	0	1	1	4 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

[High-speed on-chip oscillator frequency select register (HOCODIV) setting]

Address: F00A8H

	7	6	5	4	3	2	1	0
HOCODIV	0	0	0	0	0	HOCODIV2	HOCODIV1	HOCODIV0

HOCODIV2	HOCODIV1	HOCODIV0	Selection of high-speed on-chip oscillator clock frequency	
			FRQSEL3 Bit is 0	FRQSEL3 Bit of is 1
0	0	0	24 MHz	32 MHz
0	0	1	12 MHz	16 MHz
0	1	0	6 MHz	8 MHz
0	1	1	3 MHz	4 MHz
1	0	0	Setting prohibited	2 MHz
1	0	1	Setting prohibited	1 MHz
Other than aboves			Setting prohibited	

5.6.2 Example of setting X1 oscillation clock

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the high-speed on-chip oscillator clock. To subsequently change the clock to the X1 oscillation clock, set the oscillator and start oscillation by using the oscillation stabilization time select register (OSTS) and clock operation mode control register (CMC) and clock operation status control register (CSC) and wait for oscillation to stabilize by using the oscillation stabilization time counter status register (OSTC). After the oscillation stabilizes, set the X1 oscillation clock to f_{CLK} by using the system clock control register (CKC).

[Register settings] Set the register in the order of <1> to <5> below.

- <R> <1> Set (1) the OSCSEL bit of the CMC register, except for the cases where $f_x > 10$ MHz, in such cases set (1) the AMPH bit, to operate the X1 oscillator.

	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL	EXCLKS	OSCSELS		AMPHS1	AMPHS0	AMPH
	0	1	0	0	0	0	0	1

AMPH bit: Set this bit to 0 if the X1 oscillation clock is 10 MHz or less.

- <2> Using the OSTS register, select the oscillation stabilization time of the X1 oscillator at releasing of the STOP mode.

Example: Setting values when a wait of at least 102.4 μ s is set based on a 10 MHz resonator.

	7	6	5	4	3	2	1	0
OSTS						OSTS2	OSTS1	OSTS0
	0	0	0	0	0	0	1	0

- <3> Clear (0) the MSTOP bit of the CSC register to start oscillating the X1 oscillator.

	7	6	5	4	3	2	1	0
CSC	MSTOP	XTSTOP						HIOSTOP
	0	1	0	0	0	0	0	0

- <4> Use the OSTC register to wait for oscillation of the X1 oscillator to stabilize.

Example: Wait until the bits reach the following values when a wait of at least 102.4 μ s is set based on a 10 MHz resonator.

	7	6	5	4	3	2	1	0
OSTC	MOST8	MOST9	MOST10	MOST11	MOST13	MOST15	MOST17	MOST18
	1	1	1	0	0	0	0	0

- <5> Use the MCM0 bit of the CKC register to specify the X1 oscillation clock as the CPU/peripheral hardware clock.

	7	6	5	4	3	2	1	0
CKC	CLS	CSS	MCS	MCM0				
	0	0	0	1	0	0	0	0

5.6.3 Example of setting XT1 oscillation clock

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the high-speed on-chip oscillator clock. To subsequently change the clock to the XT1 oscillation clock, set the oscillator and start oscillation by using the operation speed mode control register (OSMC), clock operation mode control register (CMC), and clock operation status control register (CSC), set the XT1 oscillation clock to f_{CLK} by using the system clock control register (CKC).

[Register settings] Set the register in the order of <1> to <5> below.

<1> To run only the real-time clock and 12-bit interval timer on the subsystem clock (ultra-low current consumption) when in the STOP mode or sub-HALT mode, set the RTCLPC bit to 1.

	7	6	5	4	3	2	1	0
OSMC	RTCLPC 0/1	0	0	WUTMMCK0 0	0	0	0	0

<2> Set (1) the OSCSELS bit of the CMC register to operate the XT1 oscillator.

	7	6	5	4	3	2	1	0
CMC	EXCLK 0	OSCSEL 0	EXCLKS 0	OSCSELS 1	0	AMPHS1 0/1	AMPHS0 0/1	AMPH 0

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

<3> Clear (0) the XTSTOP bit of the CSC register to start oscillating the XT1 oscillator.

	7	6	5	4	3	2	1	0
CSC	MSTOP 1	XTSTOP 0	0	0	0	0	0	HIOSTOP 0

<4> Use the timer function or another function to wait for oscillation of the subsystem clock to stabilize by using software.

<5> Use the CSS bit of the CKC register to specify the XT1 oscillation clock as the CPU/peripheral hardware clock.

	7	6	5	4	3	2	1	0
CKC	CLS 0	CSS 1	MCS 0	MCM0 0	0	0	0	0

5.6.4 CPU clock status transition diagram

Figure 5-15 shows the CPU clock status transition diagram of this product.

Figure 5-15. CPU Clock Status Transition Diagram

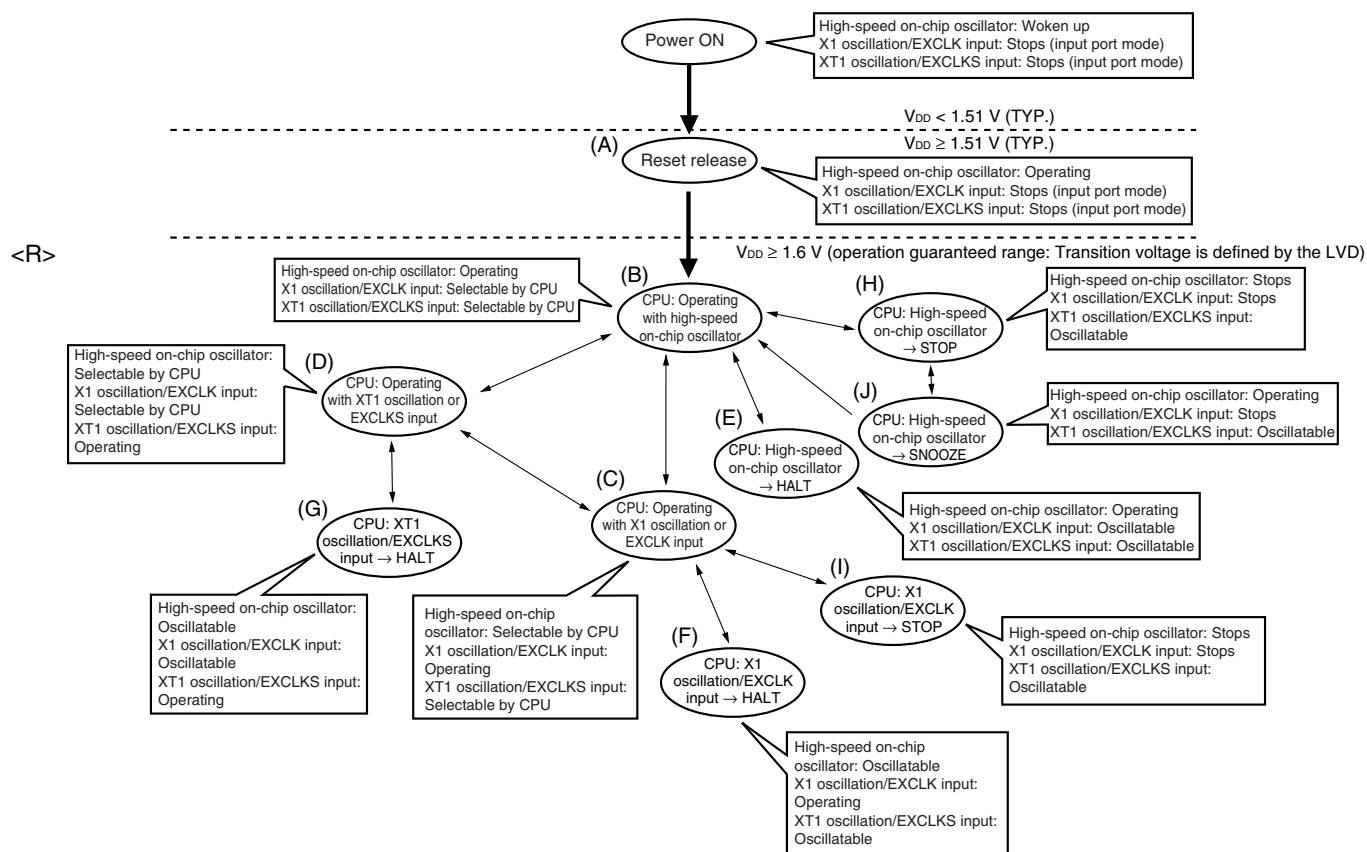


Table 5-3 shows transition of the CPU clock and examples of setting the SFR registers.

Table 5-3. CPU Clock Transition and SFR Register Setting Examples (1/5)

(1) CPU operating with high-speed on-chip oscillator clock (B) after reset release (A)

Status Transition	SFR Register Setting
(A) → (B)	SFR registers do not have to be set (default status after reset release).

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register Status Transition	CMC Register ^{Note}			OSTS Register	CSC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH		MSTOP		
(A) → (B) → (C) (X1 clock: 1 MHz ≤ f _x ≤ 10 MHz)	0	1	0	Note 2	0	Must be checked	1
(A) → (B) → (C) (X1 clock: 10 MHz < f _x ≤ 20 MHz)	0	1	1	Note 2	0	Must be checked	1
(A) → (B) → (C) (external main clock)	1	1	×	Note 2	0	Must not be checked	1

Notes 1. The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

2. Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 29 ELECTRICAL SPECIFICATIONS (T_A = −40 to +85°C) (TARGET), CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = −40 to +105°C) (TARGET)).

(3) CPU operating with subsystem clock (D) after reset release (A)

(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register Status Transition	CMC Register ^{Note}				CSC Register	Waiting for Oscillation Stabilization	CKC Register
	EXCLKS	OSCSELS	AMPHS1	AMPHS0	XTSTOP		CSS
(A) → (B) → (D) (XT1 clock)	0	1	0/1	0/1	0	Necessary	1
(A) → (B) → (D) (external sub clock)	1	1	×	×	0	Necessary	1

Note The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

Remarks 1. ×: don't care

2. (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-15.

Table 5-3. CPU Clock Transition and SFR Register Setting Examples (2/5)

(4) CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register Status Transition	CMC Register ^{Note 1}			OSTS Register	CSC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH		MSTOP		MCM0
(B) → (C) (X1 clock: $1\text{ MHz} \leq f_X \leq 10\text{ MHz}$)	0	1	0	Note 2	0	Must be checked	1
(B) → (C) (X1 clock: $10\text{ MHz} < f_X \leq 20\text{ MHz}$)	0	1	1	Note 2	0	Must be checked	1
(B) → (C) (external main clock)	1	1	×	Note 2	0	Must not be checked	1

Unnecessary if these registers are already set Unnecessary if the CPU is operating with the high-speed system clock

Notes 1. The clock operation mode control register (CMC) can be changed only once after reset release. This setting is not necessary if it has already been set.

2. Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time $\leq$ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 29 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$) (TARGET), CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$) (TARGET)).

(5) CPU clock changing from high-speed on-chip oscillator clock (B) to subsystem clock (D)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register Status Transition	CMC Register ^{Note}		CSC Register	Waiting for Oscillation Stabilization	CKC Register
	EXCLKS	OSCSELS	XTSTOP		CSS
(B) → (D) (XT1 clock)	0	1	0	Necessary	1
(B) → (D) (external sub clock)	1	1	0	Necessary	1

Unnecessary if the CPU is operating with the subsystem clock

Note The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

Remarks 1. x: don't care

2. (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-15.

Table 5-3. CPU Clock Transition and SFR Register Setting Examples (3/5)

(6) CPU clock changing from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register Status Transition	CSC Register	Oscillation accuracy stabilization time	CKC Register
	HIOSTOP		MCM0
(C) → (B)	0	30 μ s	0

Unnecessary if the CPU is operating with the
high-speed on-chip oscillator clock

(7) CPU clock changing from high-speed system clock (C) to subsystem clock (D)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register Status Transition	CSC Register	Waiting for Oscillation Stabilization	CKC Register
	XTSTOP		CSS
(C) → (D)	0	Necessary	1

Unnecessary if the CPU is operating with the
subsystem clock

(8) CPU clock changing from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register Status Transition	CSC Register	CKC Register	
	HIOSTOP	CSS	MCM0
(D) → (B)	0	0	0

Unnecessary if the CPU
is operating with the
high-speed on-chip
oscillator clock

Unnecessary if this
register is already set

Remark (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-15.

Table 5-3. CPU Clock Transition and SFR Register Setting Examples (4/5)

(9) CPU clock changing from subsystem clock (D) to high-speed system clock (C)

(Setting sequence of SFR registers) 

Setting Flag of SFR Register Status Transition	OSTS Register	CSC Register	OSTC Register	CKC Register	
		MSTOP		CSS	MCM0
(D) → (C) (X1 clock: 1 MHz ≤ f _x ≤ 10 MHz)	Note	0	Must be checked	0	1
(D) → (C) (X1 clock: 10 MHz < f _x ≤ 20 MHz)	Note	0	Must be checked	0	1
(D) → (C) (external main clock)	Note	0	Must not be checked	0	1


 Unnecessary if the CPU is operating with the high-speed system clock
 
 Unnecessary if these registers are already set

Note Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 29 ELECTRICAL SPECIFICATIONS (T_A = −40 to +85°C) (TARGET), CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = −40 to +105°C) (TARGET)).

(10) • HALT mode (E) set while CPU is operating with high-speed on-chip oscillator clock (B)

- HALT mode (F) set while CPU is operating with high-speed system clock (C)
- HALT mode (G) set while CPU is operating with subsystem clock (D)

Status Transition	Setting
(B) → (E) (C) → (F) (D) → (G)	Executing HALT instruction

Remark (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-15.

Table 5-3. CPU Clock Transition and SFR Register Setting Examples (5/5)

- (11) • STOP mode (H) set while CPU is operating with high-speed on-chip oscillator clock (B)
 • STOP mode (I) set while CPU is operating with high-speed system clock (C)

(Setting sequence) →

Status Transition		Setting		
(B) → (H)		Stopping peripheral functions that cannot operate in STOP mode	–	Executing STOP instruction
(C) → (I)	In X1 oscillation		Sets the OSTS register	
	External main system clock		–	

(12) CPU changing from STOP mode (H) to SNOOZE mode (J)

For details about the setting for switching from the STOP mode to the SNOOZE mode, see **11.8 SNOOZE Mode Function**, **12.5.7 SNOOZE mode function** and **12.6.3 SNOOZE mode function**.

Remark (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-15.

5.6.5 Condition before changing CPU clock and processing after changing CPU clock

Condition before changing the CPU clock and processing after changing the CPU clock are shown below.

Table 5-4. Changing CPU Clock (1/2)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
High-speed on-chip oscillator clock	X1 clock	Stabilization of X1 oscillation • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time	Operating current can be reduced by stopping high-speed on-chip oscillator (HIOSTOP = 1).
	External main system clock	Enabling input of external clock from the EXCLK pin • OSCSEL = 1, EXCLK = 1, MSTOP = 0	
	XT1 clock	Stabilization of XT1 oscillation • OSCSELS = 1, EXCLKS = 0, XTSTOP = 0 • After elapse of oscillation stabilization time	
	External subsystem clock	Enabling input of external clock from the EXCLKS pin • OSCSELS = 1, EXCLKS = 1, XTSTOP = 0	
<R> X1 clock	High-speed on-chip oscillator clock	Oscillation of high-speed on-chip oscillator • HIOSTOP = 0 • After elapse of oscillation accuracy stabilization time	X1 oscillation can be stopped (MSTOP = 1).
	External main system clock	Transition not possible	—
	XT1 clock	Stabilization of XT1 oscillation • OSCSELS = 1, EXCLKS = 0, XTSTOP = 0 • After elapse of oscillation stabilization time	X1 oscillation can be stopped (MSTOP = 1).
	External subsystem clock	Enabling input of external clock from the EXCLKS pin • OSCSELS = 1, EXCLKS = 1, XTSTOP = 0	X1 oscillation can be stopped (MSTOP = 1).
<R> External main system clock	High-speed on-chip oscillator clock	Oscillation of high-speed on-chip oscillator • HIOSTOP = 0 • After elapse of oscillation accuracy stabilization time	External main system clock input can be disabled (MSTOP = 1).
	X1 clock	Transition not possible	—
	XT1 clock	Stabilization of XT1 oscillation • OSCSELS = 1, EXCLKS = 0, XTSTOP = 0 • After elapse of oscillation stabilization time	External main system clock input can be disabled (MSTOP = 1).
	External subsystem clock	Enabling input of external clock from the EXCLKS pin • OSCSELS = 1, EXCLKS = 1, XTSTOP = 0	External main system clock input can be disabled (MSTOP = 1).

Table 5-5. Changing CPU Clock (2/2)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
XT1 clock	High-speed on-chip oscillator clock	Oscillation of high-speed on-chip oscillator and selection of high-speed on-chip oscillator clock as main system clock • HIOSTOP = 0, MCS = 0	XT1 oscillation can be stopped (XTSTOP = 1)
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from the EXCLK pin and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	
	External subsystem clock	Transition not possible	—
External subsystem clock	High-speed on-chip oscillator clock	Oscillation of high-speed on-chip oscillator and selection of high-speed on-chip oscillator clock as main system clock • HIOSTOP = 0, MCS = 0	External subsystem clock input can be disabled (XTSTOP = 1).
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from the EXCLK pin and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	
	XT1 clock	Transition not possible	—

5.6.6 Time required for switchover of CPU clock and system clock

By setting bits 4 and 6 (MCM0, CSS) of the system clock control register (CKC), the CPU clock can be switched (between the main system clock and the subsystem clock), and main system clock can be switched (between the high-speed on-chip oscillator clock and the high-speed system clock).

The actual switchover operation is not performed immediately after rewriting to the CKC register; operation continues on the pre-switchover clock for several clocks (see Table 5-5 to Table 5-7).

Whether the CPU is operating on the main system clock or the subsystem clock can be ascertained using bit 7 (CLS) of the CKC register. Whether the main system clock is operating on the high-speed system clock or high-speed on-chip oscillator clock can be ascertained using bit 5 (MCS) of the CKC register.

When the CPU clock is switched, the peripheral hardware clock is also switched.

Table 5-5. Maximum Time Required for System Clock Switchover

Clock A	Switching directions	Clock B	Remark
f_{IH}	$\longleftrightarrow$	f_{MX}	See Table 5-6
f_{MAIN}	$\longleftrightarrow$	f_{SUB}	See Table 5-7

Table 5-6. Maximum Number of Clocks Required for $f_{IH} \leftrightarrow f_{MX}$

Set Value Before Switchover		Set Value After Switchover	
MCM0		MCM0	
		0 ($f_{MAIN} = f_{IH}$)	1 ($f_{MAIN} = f_{MX}$)
0 ($f_{MAIN} = f_{IH}$)	$f_{MX} \geq f_{IH}$		2 clock
	$f_{MX} < f_{IH}$		$2f_{IH}/f_{MX}$ clock
1 ($f_{MAIN} = f_{MX}$)	$f_{MX} \geq f_{IH}$	$2f_{MX}/f_{IH}$ clock	
	$f_{MX} < f_{IH}$	2 clock	

Table 5-7. Maximum Number of Clocks Required for $f_{MAIN} \leftrightarrow f_{SUB}$

Set Value Before Switchover		Set Value After Switchover	
CSS		CSS	
		0 ($f_{CLK} = f_{MAIN}$)	1 ($f_{CLK} = f_{SUB}$)
0 ($f_{CLK} = f_{MAIN}$)			$1 + 2f_{MAIN}/f_{SUB}$ clock
1 ($f_{CLK} = f_{SUB}$)		3 clock	

Remarks 1. The number of clocks listed in Table 5-6 and Table 5-7 is the number of CPU clocks before switchover.

<R> **2.** Calculate the number of clocks in **Table 5-6** and **Table 5-7** by removing the decimal portion.

Example When switching the main system clock from the high-speed system clock to the high-speed on-chip oscillator clock (@ oscillation with $f_{IH} = 8$ MHz, $f_{MX} = 10$ MHz)

$$2f_{MX}/f_{IH} = 2 (10/8) = 2.5 \rightarrow 3 \text{ clocks}$$

5.6.7 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

Table 5-7. Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
High-speed on-chip oscillator clock	MCS = 1 or CLS = 1 (The CPU is operating on a clock other than the high-speed on-chip oscillator clock.)	HIOSTOP = 1
X1 clock	MCS = 0 or CLS = 1 (The CPU is operating on a clock other than the high-speed system clock.)	MSTOP = 1
External main system clock		
XT1 clock	CLS = 0 (The CPU is operating on a clock other than the subsystem clock.)	XTSTOP = 1
External subsystem clock		

<R> 5.7 Resonator and Oscillator Constants

The resonators for which the operation is verified and their oscillator constants are shown below.

- Cautions**
1. The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. Be sure to apply to the resonator manufacturer for evaluation on the actual circuit before using these constants for your application. Also apply to the resonator manufacturer for re-evaluation on the actual circuit if you have changed the make of the microcontroller or the board.
 2. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the RL78/G13 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

Figure 5-15. External Circuit Example



(1) X1 oscillation:

As of September, 2012 (1/3)

Manufacturer	Resonator	Part Number	SMD/ Lead	Frequency (MHz)	Flash operation mode ^{Note 1}	Recommended Circuit Constants ^{Note 2} (reference)			Oscillation Voltage Range (V)	
						C1 (pF)	C2 (pF)	Rd (kΩ)	MIN.	MAX.
Murata Manufacturing Co., Ltd.	Ceramic resonator	CSTCC2M00G56-R0	SMD	2.0	LV	(47)	(47)	0	1.6	3.6
		CSTCR4M00G55-R0	SMD	4.0		(39)	(39)	0		
		CSTLS4M00G53-B0	Lead			(15)	(15)	0		
		CSTCC2M00G56-R0	SMD	2.0	LS	(47)	(47)	0	1.8	3.6
		CSTCR4M00G55-R0	SMD	4.0		(39)	(39)	0		
		CSTLS4M00G53-B0	Lead			(15)	(15)	0		
		CSTCR4M19G55-R0	SMD	4.194		(39)	(39)	0		
		CSTLS4M19G53-B0	Lead			(15)	(15)	0		
		CSTCR4M91G53-R0	SMD	4.915		(15)	(15)	0		
		CSTLS4M91G53-B0	Lead			(15)	(15)	0		
		CSTCR5M00G53-R0	SMD	5.0		(15)	(15)	0		
		CSTLS5M00G53-B0	Lead			(15)	(15)	0		
		CSTCR6M00G53-R0	SMD	6.0		(15)	(15)	0		
		CSTLS6M00G53-B0	Lead			(15)	(15)	0		
		CSTCE8M00G52-R0	SMD	8.0		(10)	(10)	0		
		CSTLS8M00G53-B0	Lead			(15)	(15)	0		

- Notes 1.** Set the flash operation mode by using CMODE1 and CMODE0 bits of the option byte (000C2H/010C2H).
- 2.** Values in parentheses in the C1, C2 columns indicate an internal capacitance.

Remark Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (High speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 32 MHz

$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 16 MHz

LS (Low speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 8 MHz

LV (Low voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 4 MHz

(1) X1 oscillation:

As of September, 2012 (2/3)

Manufacturer	Resonator	Part Number	SMD/ Lead	Frequency (MHz)	Flash operation mode ^{Note 1}	Recommended Circuit Constants ^{Note 2} (reference)			Oscillation Voltage Range (V)	
						C1 (pF)	C2 (pF)	Rd (kΩ)	MIN.	MAX.
Murata Manufacturing Co., Ltd.	Ceramic resonator	CSTCC2M00G56-R0	SMD	2.0	HS	(47)	(47)	0	2.4	3.6
		CSTCR4M00G55-R0	SMD	4.0		(39)	(39)	0		
		CSTLS4M00G53-B0	Lead			(15)	(15)	0		
		CSTCR4M19G55-R0	SMD	4.194		(39)	(39)	0		
		CSTLS4M19G53-B0	Lead			(15)	(15)	0		
		CSTCR4M91G53-R0	SMD	4.915		(15)	(15)	0		
		CSTLS4M91G53-B0	Lead			(15)	(15)	0		
		CSTCR5M00G53-R0	SMD	5.0		(15)	(15)	0		
		CSTLS5M00G53-B0	Lead			(15)	(15)	0		
		CSTCR6M00G53-R0	SMD	6.0		(15)	(15)	0		
		CSTLS6M00G53-B0	Lead			(15)	(15)	0		
		CSTCE8M00G52-R0	SMD	8.0		(10)	(10)	0		
		CSTLS8M00G53-B0	Lead			(15)	(15)	0		
		CSTCE8M38G52-R0	SMD	8.388		(10)	(10)	0		
		CSTLS8M38G53-B0	Lead			(15)	(15)	0		
		CSTCE10M0G52-R0	SMD	10.0		(10)	(10)	0		
		CSTLS10M0G53-B0	Lead			(15)	(15)	0		
		CSTCE12M0G52-R0	SMD	12.0		(10)	(10)	0		
		CSTCE16M0V53-R0	SMD	16.0		(15)	(15)	0		
		CSTLS16M0X51-B0	Lead			(5)	(5)	0		
		CSTCE20M0V51-R0	SMD	20.0		(5)	(5)	0	2.7	3.6
		CSTLS20M0X51-B0	Lead			(5)	(5)	0		

- Notes 1.** Set the flash operation mode by using CMODE1 and CMODE0 bits of the option byte (000C2H/010C2H).
- 2.** Values in parentheses in the C1, C2 columns indicate an internal capacitance.

Remark Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (High speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 32 MHz

$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 16 MHz

LS (Low speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 8 MHz

LV (Low voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 4 MHz

(1) X1 oscillation:

As of September, 2012 (3/3)

Manufacturer	Resonator	Part Number	SMD/ Lead	Frequency (MHz)	Flash operation mode ^{Note 1}	Recommended Circuit Constants ^{Note 2} (reference)			Oscillation Voltage Range (V)	
						C1 (pF)	C2 (pF)	Rd (kΩ)	MIN.	MAX.
KYOCERA KINSEKI Corporation	Ceramic resonator	PBRV4.00MR50Y000	SMD	4.0	LV	15	15	0	1.6	3.6
		PBRV4.00MR50Y000	SMD	4.0	LS	15	15	0	1.8	3.6
		PRQV8.00CR5010Y000	SMD	8.0		10	10	0		
		PRQV8.00CR5010Y000	SMD	8.0	HS	10	10	0	2.4	3.6
Nihon Dempa Kogyo Co., Ltd.	Crystal resonator	NX8045GE	SMD	4.0	LV	6	6	0	1.6	3.6
		NX8045GE	SMD	4.0	LS	6	6	0	1.8	3.6
		NX8045GB	SMD	8.0		0	0	0		
		NX8045GB	SMD	8.0	HS	0	0	0	2.4	3.6
		NX3225GB	SMD	16.0		1	1	0		
		NX2520SA	SMD	20.0		0	0	0		

- Notes 1.** Set the flash operation mode by using CMODE1 and CMODE0 bits of the option byte (000C2H/010C2H).
- 2.** Values in parentheses in the C1, C2 columns indicate an internal capacitance.

Remark Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (High speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 32 MHz

$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 16 MHz

LS (Low speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 8 MHz

LV (Low voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 4 MHz

CHAPTER 6 TIMER ARRAY UNIT

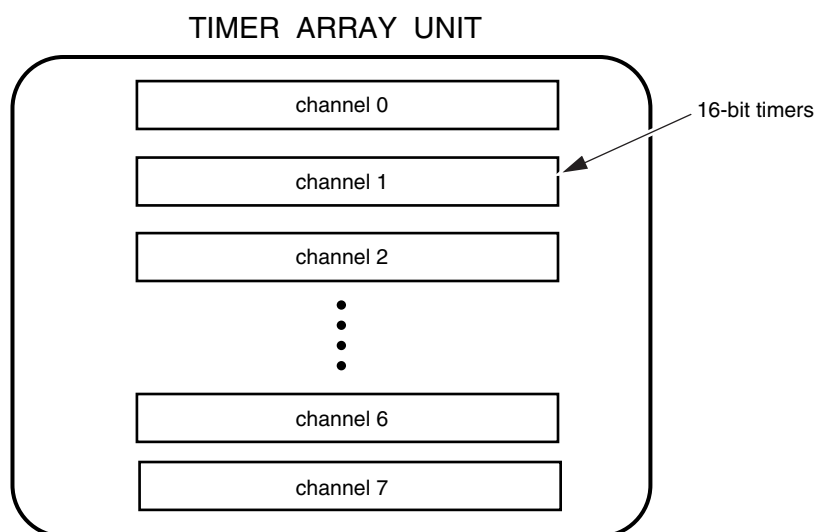
The timer array unit is provided in all products (Unit 0, Channels 0 to 7).

Units	Channels	25, 32, 48, 64-pin
Unit 0	Channel 0	√
	Channel 1	√
	Channel 2	√
	Channel 3	√
	Channel 4	√
	Channel 5	√
	Channel 6	√
	Channel 7	√

- Cautions**
1. The presence or absence of timer I/O pins depends on the product. See Table 6-2 Timer I/O Pins provided in Each Product for details.
 2. Most of the following descriptions in this chapter use the 64-pin products as an example.

The timer array unit has eight 16-bit timers.

Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more “channels” can be used to create a high-accuracy timer.



For details about each function, see the table below.

Independent channel operation function	Simultaneous channel operation function
- Interval timer (→ refer to 6.7.1) - Square wave output (→ refer to 6.7.1) - External event counter (→ refer to 6.7.2) - Divider ^{Note} (→ refer to 6.7.3) - Input pulse interval measurement (→ refer to 6.7.4) - Measurement of high-/low-level width of input signal (→ refer to 6.7.5) - Delay counter (→ refer to 6.7.6)	- One-shot pulse output(→ refer to 6.8.1) - PWM output(→ refer to 6.8.2) - Multiple PWM output(→ refer to 6.8.3)

Note Only channel 0 of unit 0.

It is possible to use the 16-bit timer of channels 1 and 3 of the units 0 as two 8-bit timers (higher and lower). The functions that can use channels 1 and 3 as 8-bit timers are as follows:

- Interval timer (higher/lower 8-bit timer only)/square wave output (lower 8-bit timer only)
- External event counter (lower 8-bit timer only)
- Delay counter (lower 8-bit timer only)

Channel 7 of unit 0 can be used to realize LIN-bus communication operating in combination with UART2 of the serial array unit (32, 48, and 64-pin products only).

6.1 Functions of Timer Array Unit

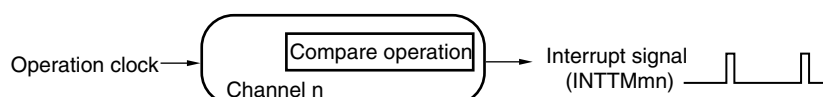
Timer array unit has the following functions.

6.1.1 Independent channel operation function

By operating a channel independently, it can be used for the following purposes without being affected by the operation mode of other channels.

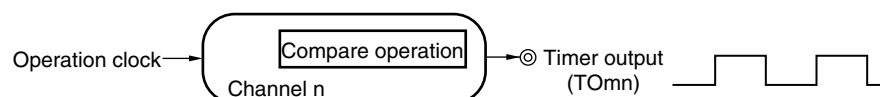
(1) Interval timer

Each timer of a unit can be used as a reference timer that generates an interrupt (INTTMmn) at fixed intervals.



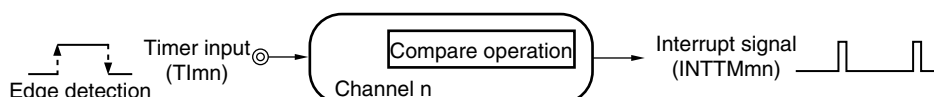
(2) Square wave output

A toggle operation is performed each time INTTMmn interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TOMn).



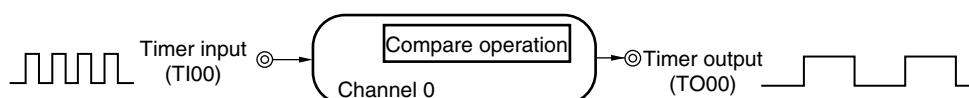
(3) External event counter

Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TIMn) has reached a specific value.



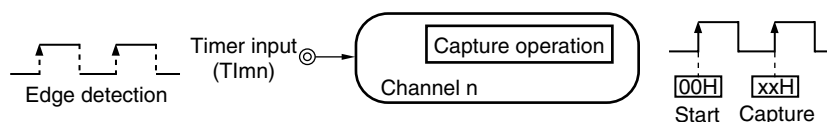
(4) Divider function (channel 0 only)

A clock input from a timer input pin (TI00) is divided and output from an output pin (TOM0).



(5) Input pulse interval measurement

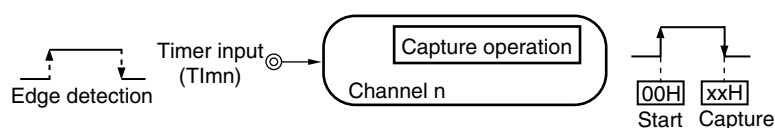
Counting is started by the valid edge of a pulse signal input to a timer input pin (TIMn). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.



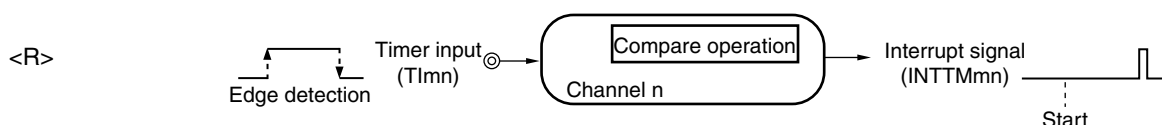
(Note, Caution, and Remark are listed on the next page.)

(6) Measurement of high-/low-level width of input signal

Counting is started by a single edge of the signal input to the timer input pin (TImn), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.

**(7) Delay counter**

Counting is started at the valid edge of the signal input to the timer input pin (TImn), and an interrupt is generated after any delay period.



Remarks 1 m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

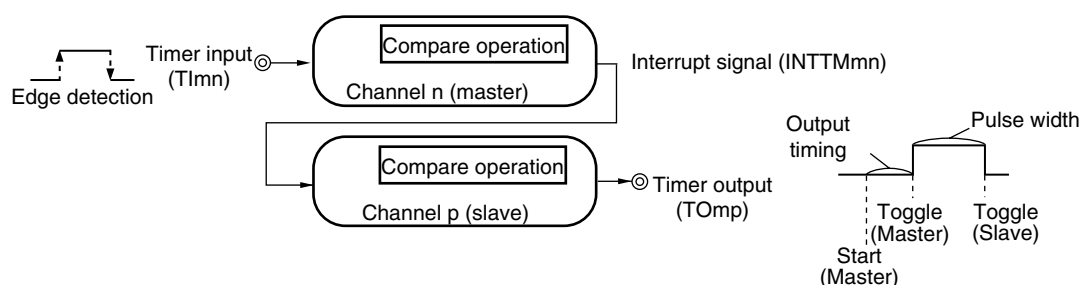
2. The presence or absence of timer I/O pins of channel 0 to 7 depends on the product. See **Table 6-2 Timer I/O Pins provided in Each Product** for details.

6.1.2 Simultaneous channel operation function

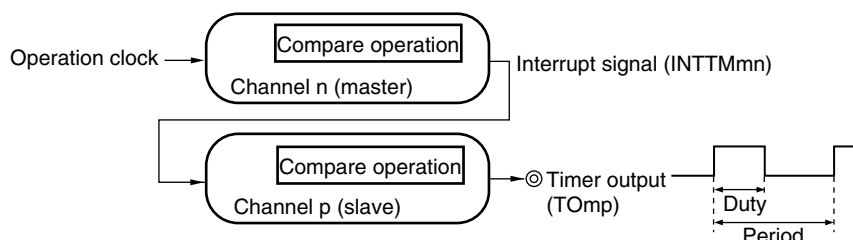
By using the combination of a master channel (a reference timer mainly controlling the cycle) and slave channels (timers operating according to the master channel), channels can be used for the following purposes.

(1) One-shot pulse output

Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.

**(2) PWM (Pulse Width Modulation) output**

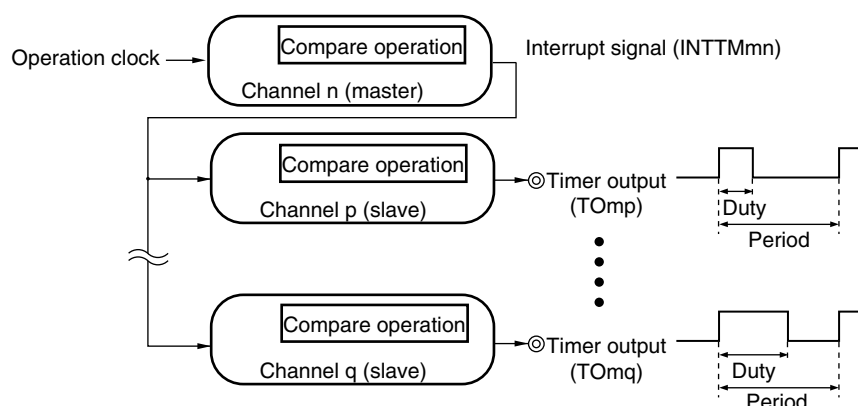
Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.



(Caution is listed on the next page.)

(3) Multiple PWM (Pulse Width Modulation) output

By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.



<R> **Caution** For details about the rules of simultaneous channel operation function, see 6.4.1 Basic rules of simultaneous channel operation function.

Remark m: Unit number ($m = 0$), n: Channel number ($n = 0$ to 7 (however, timer input pin (TImn), timer output pin (TOmn) : $n = 0, 1, 3$ to 7)), p, q: Slave channel number ($n < p < q \leq 7$)

6.1.3 8-bit timer operation function (channels 1 and 3 only)

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels. This function can only be used for channels 1 and 3.

Caution There are several rules for using 8-bit timer operation function.
For details, see 6.4.2 Basic rules of 8-bit timer operation function (channels 1 and 3 only).

6.1.4 LIN-bus supporting function (channel 7 of unit 0 only)

Timer array unit is used to check whether signals received in LIN-bus communication match the LIN-bus communication format.

(1) Detection of wakeup signal

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD2) of UART2 and the count value of the timer is captured at the rising edge. In this way, a low-level width can be measured. If the low-level width is greater than a specific value, it is recognized as a wakeup signal.

(2) Detection of break field

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD2) of UART2 after a wakeup signal is detected, and the count value of the timer is captured at the rising edge. In this way, a low-level width is measured. If the low-level width is greater than a specific value, it is recognized as a break field.

(3) Measurement of pulse width of sync field

After a break field is detected, the low-level width and high-level width of the signal input to the serial data input pin (RxD2) of UART2 are measured. From the bit interval of the sync field measured in this way, a baud rate is calculated.

Remark For details about setting up the operations used to implement the LIN-bus, see **6.3.13 Input switch control register (ISC)** and **6.7.5 Operation as input signal high-/low-level width measurement**.

6.2 Configuration of Timer Array Unit

Timer array unit includes the following hardware.

Table 6-1. Configuration of Timer Array Unit

Item	Configuration
Timer/counter	Timer count register mn (TCRmn)
Register	Timer data register mn (TDRmn)
Timer input	TI00, TI01, TI03 to TI07 ^{Note 1} , RxD2 pin (for LIN-bus)
Timer output	TO00, TO01, TO03 to TO07 ^{Note 1} , output controller
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Timer clock select register m (TPSm) • Timer channel enable status register m (TEm) • Timer channel start register m (TSM) • Timer channel stop register m (TTm) • Timer input select register 0 (TIS0) • Timer output enable register m (TOEm) • Timer output register m (TOM) • Timer output level register m (TOLm) • Timer output mode register m (TOMm) <Registers of each channel> • Timer mode register mn (TMRmn) • Timer status register mn (TSRmn) • Input switch control register (ISC) • Noise filter enable registers 1 (NFEN1) • Port mode control register (PMCxx)^{Note 2} • Port mode register (PMxx)^{Note 2} • Port register (Pxx)^{Note 2}

Notes 1. The presence or absence of timer I/O pins of channel 0 to 7 depends on the product. See **Table 6-2 Timer I/O Pins provided in Each Product** for details.

2. The Port mode control register (PMCxx), port mode registers (PMxx) and port registers (Pxx) to be set differ depending on the product. for details, see **6. 3. 15 Port mode registers 0, 1, 3, 4 (PM0, PM1, PM3, PM4)**.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

The presence or absence of timer I/O pins in each timer array unit channel depends on the product.

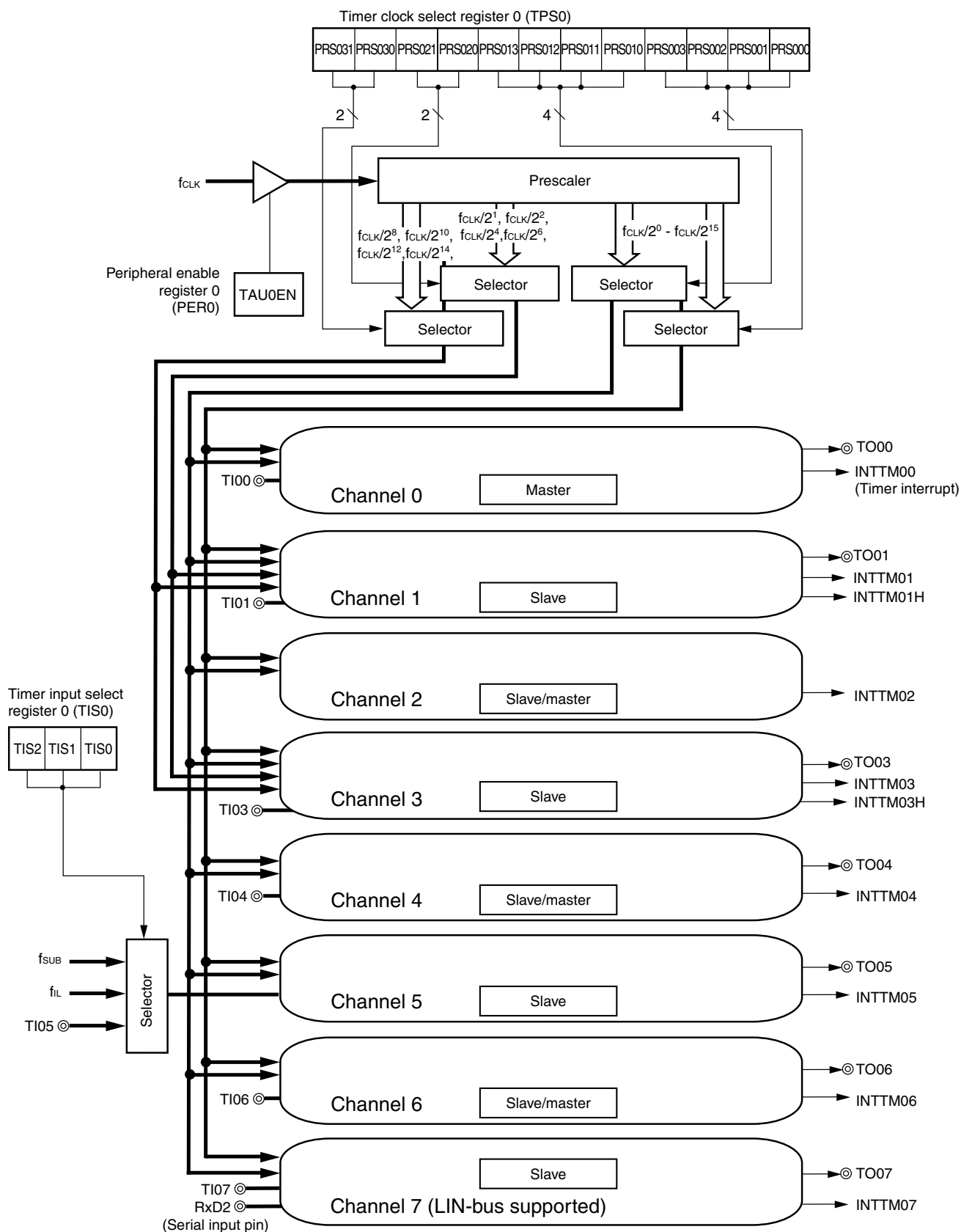
Table 6-2. Timer I/O Pins provided in Each Product

Timer array unit channels		I/O Pins of Each Product			
		64-pin	48-pin	32-pin	25-pin
Unit 0	Channel 0	P00/TI00, P01/TO00			
	Channel 1	P16/TI01/TO01		–	
	Channel 2	–			
	Channel 3	P31/TI03/TO03 ^{Note}			
	Channel 4	P42/TI04/TO04	–		
	Channel 5	P05/TI05/TO05	–		
	Channel 6	P06/TI06/TO06	–		
	Channel 7	P41/TI07/TO07		–	

- Remarks**
1. When timer input and timer output are shared by the same pin, either only timer input or only timer output can be used.
 2. –: There is no timer I/O pin, but the channel is available. (However, the channel can only be used as an interval timer.)
 ×: The channel is not available.

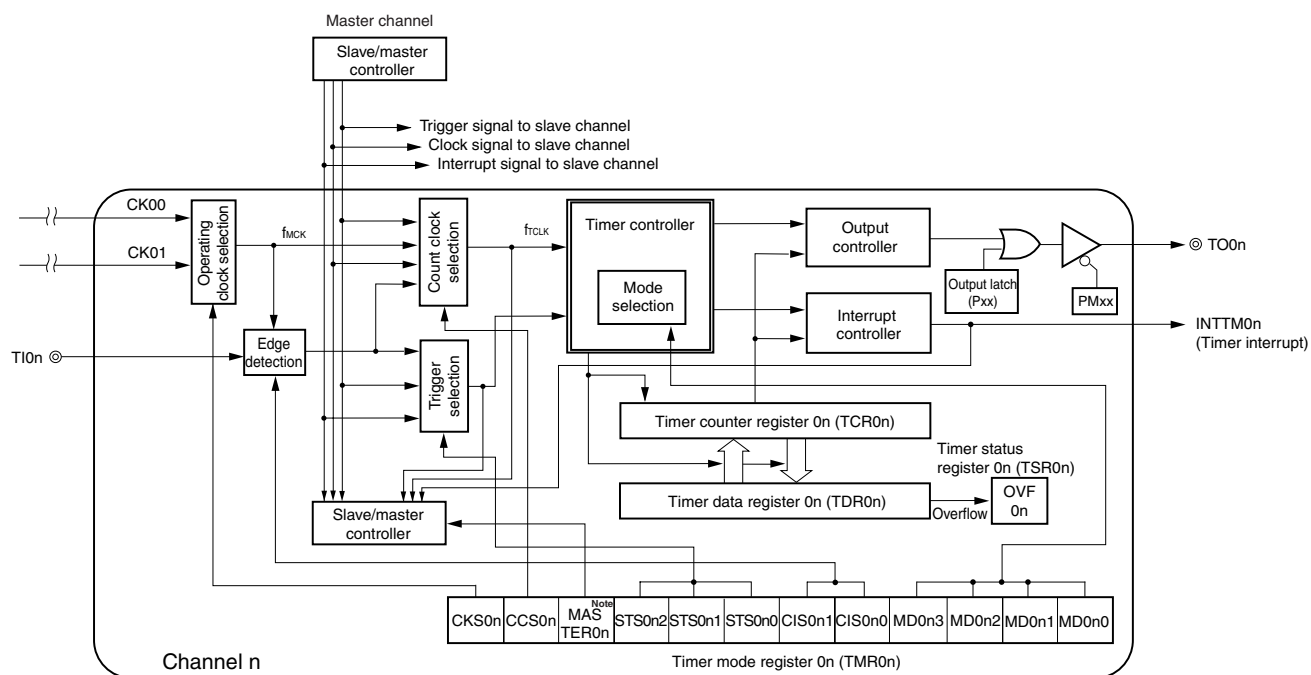
Figure 6-1 shows the block diagrams of the timer array unit.

Figure 6-1. Entire Configuration of Timer Array Unit 0 (Example: 64-pin products)

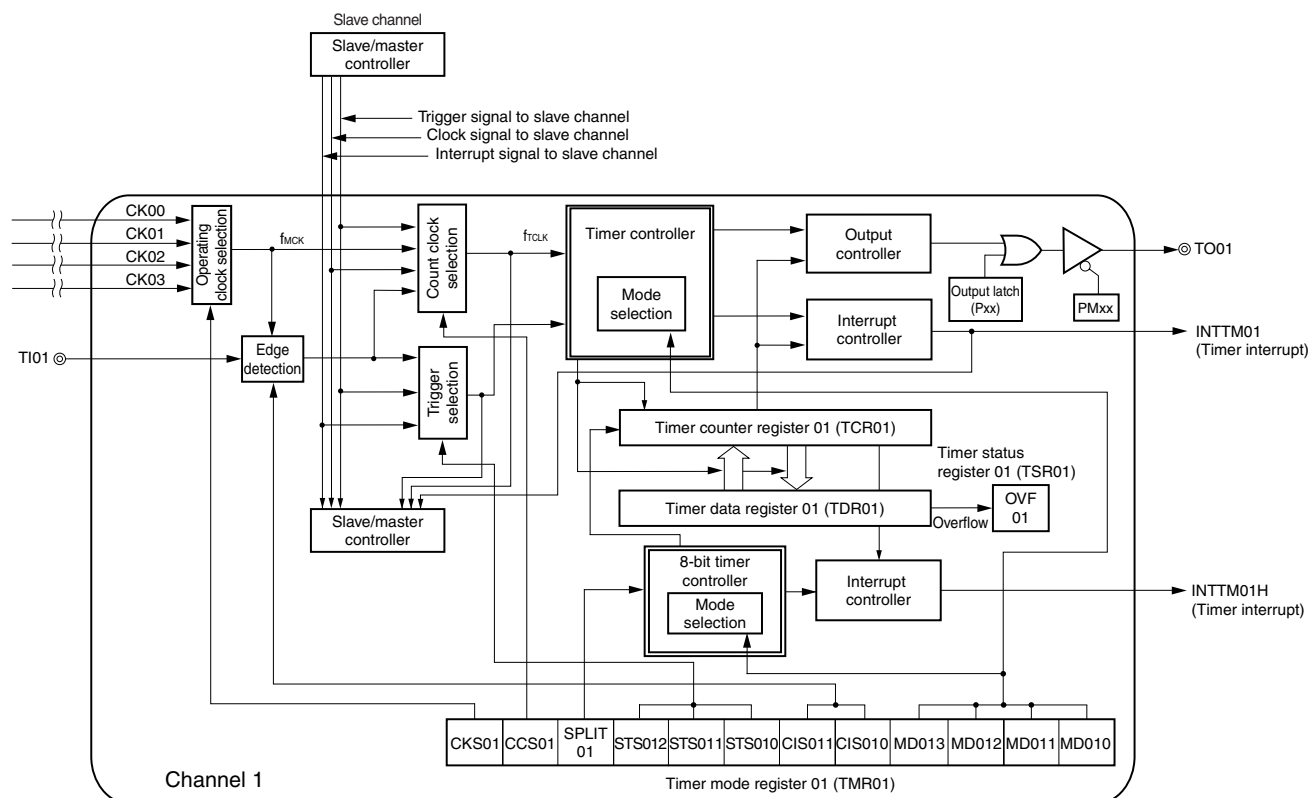


Remark f_{SUB} : Subsystem clock frequency
 f_{IL} : Low-speed on-chip oscillator clock frequency

<R>

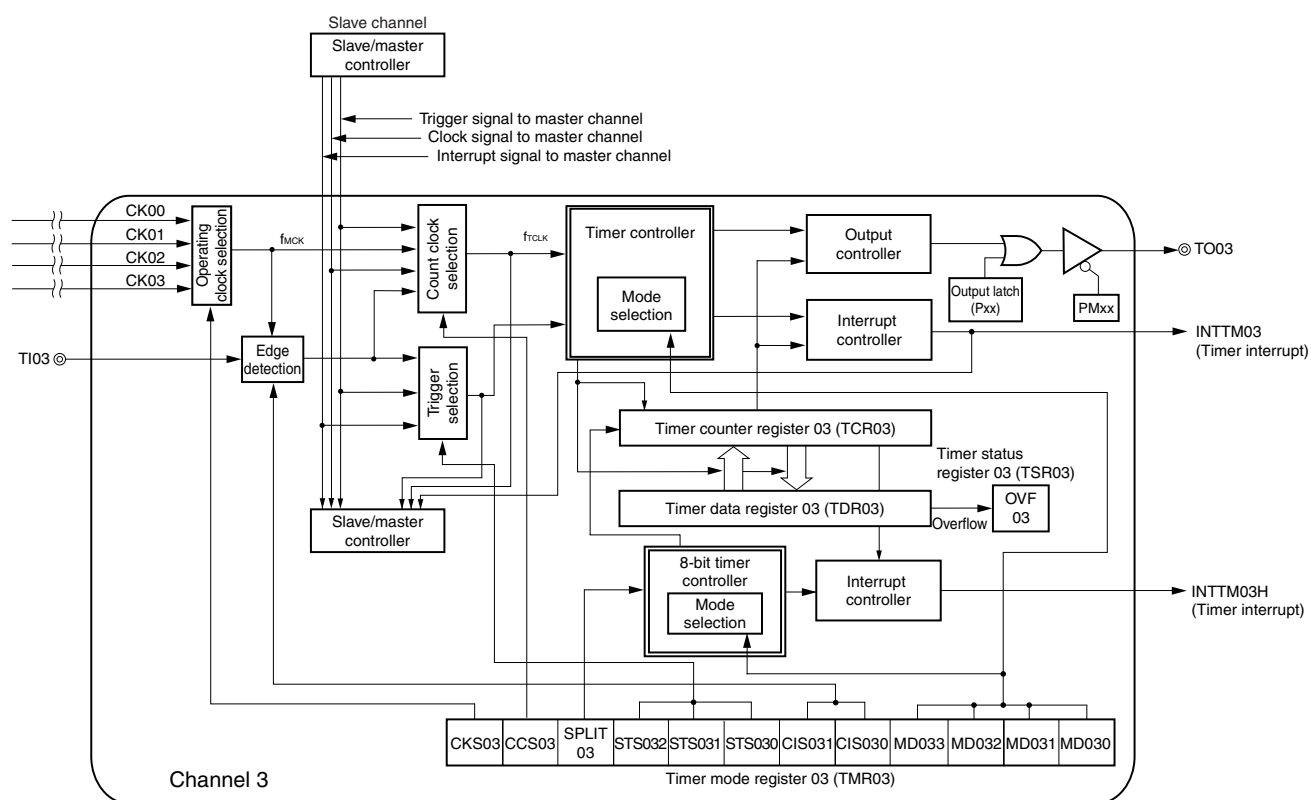
Figure 6-2. Internal Block Diagram of Channel 0, 2, 4, 6 of Timer Array Unit 0**Note** n = 2, 4, 6 only**Remark** n = 0, 2, 4, 6

<R>

Figure 6-3. Internal Block Diagram of Channel 1 of Timer Array Unit 0

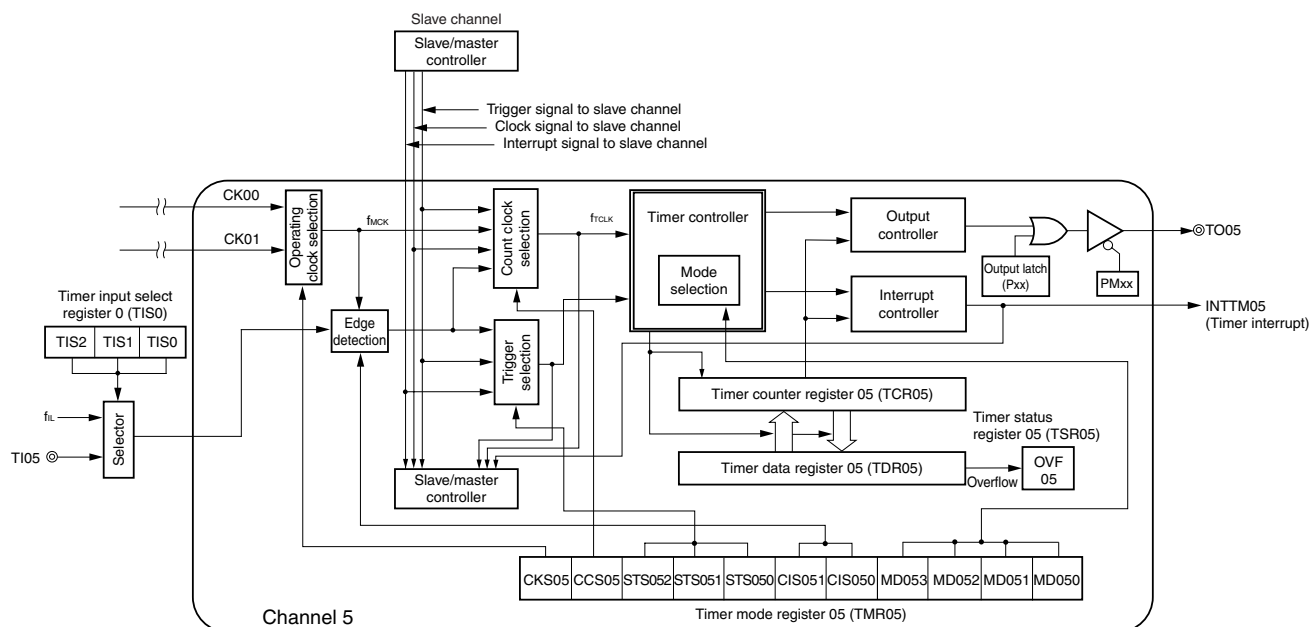
<R>

Figure 6-4. Internal Block Diagram of Channel 3 of Timer Array Unit 0

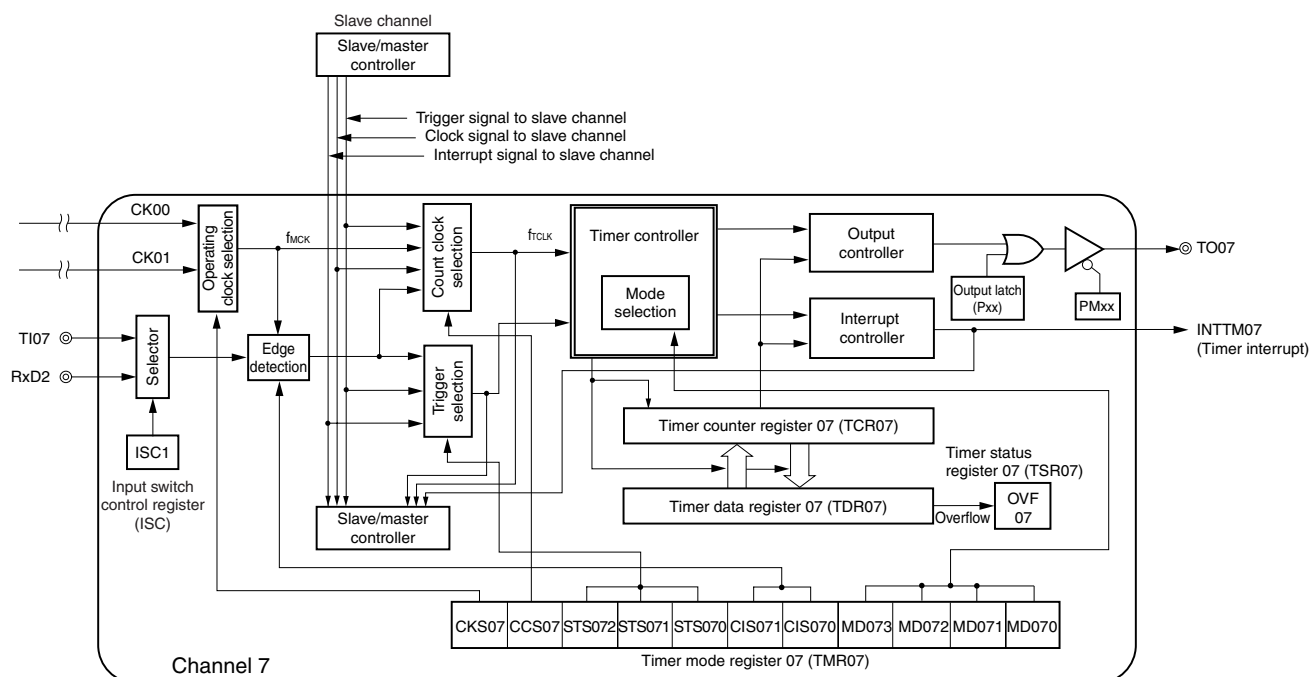


<R>

Figure 6-5. Internal Block Diagram of Channel 5 of Timer Array Unit 0



<R>

Figure 6-6. Internal Block Diagram of Channel 7 of Timer Array Unit 0**6.2.1 Timer count register mn (TCRmn)**

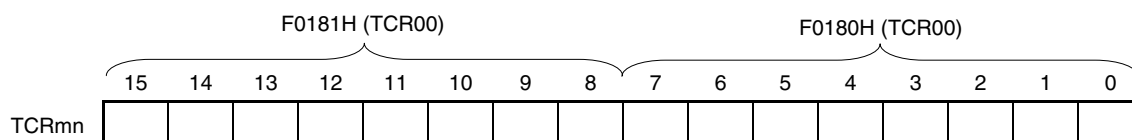
The TCRmn register is a 16-bit read-only register and is used to count clocks.

The value of this counter is incremented or decremented in synchronization with the rising edge of a count clock.

Whether the counter is incremented or decremented depends on the operation mode that is selected by the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn) (refer to **6.3.3 Timer mode register mn (TMRmn)**).

Figure 6-7. Format of Timer Count Register mn (TCRmn)

Address: F0180H, F0181H (TCR00) to F018EH, F018FH (TCR07), After reset: FFFFH R
F01C0H, F01C1H (TCR10) to F01CEH, F01CFH (TCR17)



Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

The count value can be read by reading timer count register mn (TCRmn).

The count value is set to FFFFH in the following cases.

- When the reset signal is generated
- When the TAUmEN bit of peripheral enable register 0 (PER0) is cleared
- When counting of the slave channel has been completed in the PWM output mode
- When counting of the slave channel has been completed in the delay count mode
- When counting of the master/slave channel has been completed in the one-shot pulse output mode
- When counting of the slave channel has been completed in the multiple PWM output mode

The count value is cleared to 0000H in the following cases.

- When the start trigger is input in the capture mode
- When capturing has been completed in the capture mode

Caution The count value is not captured to timer data register mn (TDRmn) even when the TCRmn register is read.

The TCRmn register read value differs as follows according to operation mode changes and the operating status.

Table 6-3. Timer Count Register mn (TCRmn) Read Value in Various Operation Modes

<R>	Operation Mode	Count Mode	Timer count register mn (TCRmn) Read Value ^{Note}			
			Value if the operation mode was changed after releasing reset	Value if the operation was count operation paused (TTmn = 1)	Value if the operation mode was changed after count operation paused (TTmn = 1)	Value when waiting for a start trigger after one count
	Interval timer mode	Count down	FFFFH	Value if stop	Undefined	–
	Capture mode	Count up	0000H	Value if stop	Undefined	–
	Event counter mode	Count down	FFFFH	Value if stop	Undefined	–
	One-count mode	Count down	FFFFH	Value if stop	Undefined	FFFFH
	Capture & one-count mode	Count up	0000H	Value if stop	Undefined	Capture value of TDRmn register + 1

Note This indicates the value read from the TCRmn register when channel n has stopped operating as a timer (TEmn = 0) and has been enabled to operate as a counter (TSmn = 1). The read value is held in the TCRmn register until the count operation starts.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.2.2 Timer data register mn (TDRmn)

This is a 16-bit register from which a capture function and a compare function can be selected.

The capture or compare function can be switched by selecting an operation mode by using the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn).

The value of the TDRmn register can be changed at any time.

This register can be read or written in 16-bit units.

In addition, for the TDRm1 and TDRm3 registers, while in the 8-bit timer mode (when the SPLIT bits of timer mode registers 01 and 03 (TMRm1, TMRm3) are 1), it is possible to read or write the data in 8-bit units, with TDRm1H and TDRm3H used as the higher 8 bits, and TDRm1L and TDRm3L used as the lower 8 bits.

Reset signal generation clears this register to 0000H.

Figure 6-8. Format of Timer Data Register mn (TDRmn) (n = 0, 2, 4 to 7)

Address: FFF18H, FFF19H (TDR00), FFF64H, FFF65H (TDR02), After reset: 0000H R/W
 FFF68H, FFF69H (TDR04) to FFF6EH, FFF6FH (TDR07)

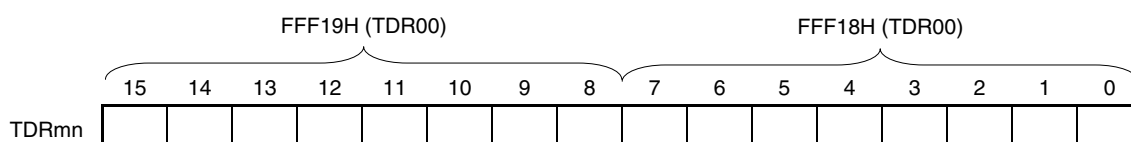
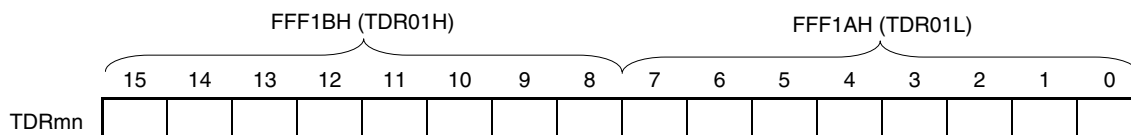


Figure 6-9. Format of Timer Data Register mn (TDRmn) (n = 1, 3)

Address: FFF1AH, FFF1BH (TDR01), FFF65H, FFF67H (TDR03) After reset: 0000H R/W



(i) When timer data register mn (TDRmn) is used as compare register

Counting down is started from the value set to the TDRmn register. When the count value reaches 0000H, an interrupt signal (INTTMmn) is generated. The TDRmn register holds its value until it is rewritten.

Caution The TDRmn register does not perform a capture operation even if a capture trigger is input, when it is set to the compare function.

(ii) When timer data register mn (TDRmn) is used as capture register

The count value of timer count register mn (TCRmn) is captured to the TDRmn register when the capture trigger is input.

A valid edge of the TImn pin can be selected as the capture trigger. This selection is made by timer mode register mn (TMRmn).

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

6.3 Registers Controlling Timer Array Unit

Timer array unit is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Timer clock select register m (TPSm)
- Timer mode register mn (TMRmn)
- Timer status register mn (TSRmn)
- Timer channel enable status register m (TEm)
- Timer channel start register m (TSm)
- Timer channel stop register m (TTm)
- Timer input select register 0 (TIS0)
- Timer output enable register m (TOEm)
- Timer output register m (TOM)
- Timer output level register m (TOLm)
- Timer output mode register m (TOMm)
- Input switch control register (ISC)
- Noise filter enable registers 1 (NFEN1)
- Port mode control register (PMCxx)^{Note}
- Port mode register (PMxx)^{Note}
- Port register (Pxx)^{Note}

Note The port mode registers (PMxx) and port registers (Pxx) to be set differ depending on the product. For details, see 6.3.15 Port mode registers 0, 1, 3, 4 (PM0, PM1, PM3, PM4).

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the timer array unit 0 is used, be sure to set bit 0 (TAU0EN) of this register to 1.

When the timer array unit 1 is used, be sure to set bit 1 (TAU1EN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6-10. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	IICA0EN	SAU1EN ^{Note}	SAU0EN	0	TAU0EN

TAU1EN	Control of timer array unit 1 input clock
0	Stops supply of input clock. - SFR used by the timer array unit 1 cannot be written. - The timer array unit 1 is in the reset status.
1	Supplies input clock. SFR used by the timer array unit 1 can be read/written.

TAU0EN	Control of timer array 0 unit input clock
0	Stops supply of input clock. - SFR used by the timer array unit 0 cannot be written. - The timer array unit 0 is in the reset status.
1	Supplies input clock. SFR used by the timer array unit 0 can be read/written.

Notes 32, 48, and 64-pin products only.

- Cautions**
- When setting the timer array unit, be sure to set the TAU1EN bit to 1 first. If TAU1EN = 0, writing to a control register of timer array unit is ignored, and all read values are default values (except for the timer input select register 0 (TIS0), input switch control register (ISC), noise filter enable register 1 (NFEN1), port mode control registers 0, 1, 3, 4 (PMC0, PMC1, PMC3, PMC4), port mode registers 0, 1, 3, 4 (PM0, PM1, PM3, PM4), and port registers 0, 1, 3, 4 (P0, P1, P3, P4)).
 - Be sure to clear the following bits to 0.
 - 25-pin products: bits 1, 3, 6
 - 32, 48, 64-pin products: bits 1, 6

6.3.2 Timer clock select register m (TPSm)

The TPSm register is a 16-bit register that is used to select two types or four types of operation clocks (CKm0, CKm1) that are commonly supplied to each channel from external prescaler. CKm1 is selected by using bits 7 to 4 of the TPSm register, and CKm0 is selected by using bits 3 to 0. In addition, for channel 1 and 3, CKm2 is selected by using bits 9 and 8 of the TPSm register, and CKm3 is selected by using bits 13 and 12.

Rewriting of the TPSm register during timer operation is possible only in the following cases.

If the PRSm00 to PRSm03 bits can be rewritten ($n = 0$ to 7):

All channels for which CKm0 is selected as the operation clock ($CKSmn1, CKSmn0 = 0, 0$) are stopped ($TEmn = 0$).

If the PRSm10 to PRSm13 bits can be rewritten ($n = 0$ to 7):

All channels for which CKm1 is selected as the operation clock ($CKSmn1, CKSmn0 = 0, 1$) are stopped ($TEmn = 0$).

If the PRSm20 and PRSm21 bits can be rewritten ($n = 1, 3$):

All channels for which CKm2 is selected as the operation clock ($CKSmn1, CKSmn0 = 1, 0$) are stopped ($TEmn = 0$).

If the PRSm30 and PRSm31 bits can be rewritten ($n = 1, 3$):

All channels for which CKm3 is selected as the operation clock ($CKSmn1, CKSmn0 = 1, 1$) are stopped ($TEmn = 0$).

The TPSm register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 6-11. Format of Timer Clock Select register m (TPSm) (1/2)

Address: F01B6H, F01B7H (TPS0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPSm	0	0	PRS m31	PRS m30	0	0	PRS m21	PRS m20	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00

PRS mk3	PRS mk2	PRS mk1	PRS mk0		Selection of operation clock (CKmk) ^{Note} (k = 0, 1)				
					f _{CLK} = 2 MHz	f _{CLK} = 5 MHz	f _{CLK} = 10 MHz	f _{CLK} = 20 MHz	f _{CLK} = 32 MHz
0	0	0	0	f _{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	32 MHz
0	0	0	1	f _{CLK} /2	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	f _{CLK} /2 ²	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	f _{CLK} /2 ³	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	f _{CLK} /2 ⁴	125 kHz	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	f _{CLK} /2 ⁵	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	1 MHz
0	1	1	0	f _{CLK} /2 ⁶	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz
0	1	1	1	f _{CLK} /2 ⁷	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	250 kHz
1	0	0	0	f _{CLK} /2 ⁸	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	f _{CLK} /2 ⁹	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	f _{CLK} /2 ¹⁰	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	1	1	f _{CLK} /2 ¹¹	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
1	1	0	0	f _{CLK} /2 ¹²	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	f _{CLK} /2 ¹³	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	f _{CLK} /2 ¹⁴	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	f _{CLK} /2 ¹⁵	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

<R> **Note** When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), stop timer array unit (TTm = 00FFH).

Cautions 1. Be sure to clear bits 15, 14, 11, 10 to "0".

<R> **2.** If f_{CLK} (undivided) is selected as the operation clock (CKmk) and TDRnm is set to 0000H (n = 0 or 1, m = 0 to 7), interrupt requests output from timer array units are not detected.

Remarks 1. f_{CLK}: CPU/peripheral hardware clock frequency

<R> **2.** Waveform of the clock to be selected in the TPSm register which becomes high level for one period of f_{CLK} from its rising edge (m = 1 to 15). For details, see 6.5.1 Count clock (f_{CLK}).

Figure 6-11. Format of Timer Clock Select register m (TPSm) (2/2)

Address: F01B6H, F01B7H (TPS0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPSm	0	0	PRS m31	PRS m30	0	0	PRS m21	PRS m20	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00

PRS m21	PRS m20		Selection of operation clock (CKm2) ^{Note}				
			f _{CLK} = 2 MHz	f _{CLK} = 5 MHz	f _{CLK} = 10 MHz	f _{CLK} = 20 MHz	f _{CLK} = 32 MHz
0	0	f _{CLK} /2	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	1	f _{CLK} /2 ²	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
1	0	f _{CLK} /2 ⁴	125 kHz	312.5 kHz	625 MHz	1.25 MHz	2 MHz
1	1	f _{CLK} /2 ⁶	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz

PRS m31	PRS m30	Selection of operation clock (CKm3) ^{Note}					
		f _{CLK} = 2 MHz	f _{CLK} = 5 MHz	f _{CLK} = 10 MHz	f _{CLK} = 20 MHz	f _{CLK} = 32 MHz	
0	0	f _{CLK} /2 ⁸	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
0	1	f _{CLK} /2 ¹⁰	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	f _{CLK} /2 ¹²	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	f _{CLK} /2 ¹⁴	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), stop timer array unit (TTm = 00FFH).

The timer array unit must also be stopped if the operating clock (f_{MCK}) specified by using the CKSmn0, and CKSmn1 bits or the valid edge of the signal input from the TImn pin is selected as the count clock (f_{CLK}).

Caution Be sure to clear bits 15, 14, 11, 10 to “0”.

By using channels 1 and 3 in the 8-bit timer mode and specifying CKm2 or CKm3 as the operation clock, the interval times shown in Table 6-4 can be achieved by using the interval timer function.

Table 6-4. Interval Times Available for Operation Clock CKSm2 or CKSm3

Clock		Interval time (f _{CLK} = 32 MHz)			
		10 μs ^{Note}	100 μs ^{Note}	1 ms ^{Note}	10 ms ^{Note}
CKm2	f _{CLK} /2	√	—	—	—
	f _{CLK} /2 ²	√	—	—	—
	f _{CLK} /2 ⁴	√	√	—	—
	f _{CLK} /2 ⁶	√	√	—	—
CKm3	f _{CLK} /2 ⁸	—	√	√	—
	f _{CLK} /2 ¹⁰	—	√	√	—
	f _{CLK} /2 ¹²	—	—	√	√
	f _{CLK} /2 ¹⁴	—	—	√	√

Note The margin is within 5 %.

Remarks 1. f_{CLK}: CPU/peripheral hardware clock frequency

2. For details of asignal of f_{CLK}/2ⁱ selected with the TPSm register, see **6.5.1 Count clock (f_{CLK})**.

6.3.3 Timer mode register mn (TMRmn)

The TMRmn register sets an operation mode of channel n. This register is used to select the operation clock (f_{MCK}), select the count clock, select the master/slave, select the 16 or 8-bit timer (only for channels 1 and 3), specify the start trigger and capture trigger, select the valid edge of the timer input, and specify the operation mode (interval, capture, event counter, one-count, or capture and one-count).

Rewriting the TMRmn register is prohibited when the register is in operation (when TEMn = 1). However, bits 7 and 6 (CISmn1, CISmn0) can be rewritten even while the register is operating with some functions (when TEMn = 1) (for details, see **6.7 Independent Channel Operation Function of Timer Array Unit** and **6.8 Simultaneous Channel Operation Function of Timer Array Unit**).

The TMRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Caution The bits mounted depend on the channels in the bit 11 of TMRmn register.

TMRm2, TMRm4, TMRm6: MASTERmn bit (n = 2, 4, 6)

TMRm1, TMRm3: SPLITmn bit (n = 1, 3)

TMRm0, TMRm5, TMRm7: Fixed to 0

Figure 6-12. Format of Timer Mode Register mn (TMRmn) (1/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAST ERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0 ^{Note}	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

CKS mn1	CKS mn0	Selection of operation clock (f_{MCK}) of channel n
0	0	Operation clock CKm0 set by timer clock select register m (TPSm)
0	1	Operation clock CKm2 set by timer clock select register m (TPSm)
1	0	Operation clock CKm1 set by timer clock select register m (TPSm)
1	1	Operation clock CKm3 set by timer clock select register m (TPSm)
Operation clock (f_{MCK}) is used by the edge detector. A count clock (f_{CLK}) and a sampling clock are generated depending on the setting of the CCSmn bit.		
The operation clocks CKm2 and CKm3 can only be selected for channels 1 and 3.		

CCS mn	Selection of count clock (f_{CLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin In channel 5, Valid edge of input signal selected by TIS0
Count clock (f_{CLK}) is used for the timer/counter, output controller, and interrupt controller.	

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.**Cautions 1.** Be sure to clear bits 13, 5, and 4 to "0".

- 2.** The timer array unit must be stopped (TTm = 00FFH) if the clock selected for f_{CLK} is changed (by changing the value of the system clock control register (CKC)), even if the operating clock specified by using the CKSmn0 and CKSmn1 bits (f_{MCK}) or the valid edge of the signal input from the TImn pin is selected as the count clock (f_{CLK}).

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

Figure 6-12. Format of Timer Mode Register mn (TMRmn) (2/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAST ERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0 ^{Note}	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

(Bit 11 of TMRmn (n = 2, 4, 6))

MAS TER mn	Selection between using channel n independently or simultaneously with another channel(as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only the channel 2, 4, 6 can be set as a master channel (MASTERmn = 1). Be sure to use channel 0, 5, 7 are fixed to 0 (Regardless of the bit setting, channel 0 operates as master, because it is the highest channel). Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.	

(Bit 11 of TMRmn (n = 1, 3))

SPLI Tmn	Selection of 8 or 16-bit timer operation for channels 1 and 3
0	Operates as 16-bit timer. (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

STS mn2	STS mn1	STS mn0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

Figure 6-12. Format of Timer Mode Register mn (TMRmn) (3/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAST ERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0 ^{Note}	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

CIS mn1	CIS mn0	Selection of TImn pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge
If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B.		

MD mn3	MD mn2	MD mn1	Operation mode of channel n	Corresponding function	Count operation of TCR
0	0	0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		
The operation of each mode varies depending on MDmn0 bit (see next table).					

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Note Bit 11 is fixed at 0 of read only, write is ignored.**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

Figure 6-12. Format of Timer Mode Register mn (TMRmn) (4/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAST ERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0 ^{Note}	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Operation mode (Value set by the MDmn3 to MDmn1 bits (see table above))	MD mn0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode ^{Note 1} (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation ^{Note 2} . At that time, interrupt is not generated, either.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

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Notes 1. Bit 11 is fixed at 0 of read only, write is ignored.**2.** In one-count mode, interrupt output (INTTmn) when starting a count operation and TOn output are not controlled.**3.** If the start trigger (TSmn = 1) is issued during operation, the counter is initialized, an interrupt is generated, and recounting is started (does not occur the interrupt request).**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOn) : n = 0, 1, 3 to 7))

6.3.4 Timer status register mn (TSRmn)

The TSRmn register indicates the overflow status of the counter of channel n.

The TSRmn register is valid only in the capture mode (MDmn3 to MDmn1 = 010B) and capture & one-count mode (MDmn3 to MDmn1 = 110B). See Table 6-5 for the operation of the OVF bit in each operation mode and set/clear conditions.

The TSRmn register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the TSRmn register can be set with an 8-bit memory manipulation instruction with TSRmnL.

Reset signal generation clears this register to 0000H.

Figure 6-13. Format of Timer Status Register mn (TSRmn)

Address: F01A0H, F01A1H (TSR00) to F01AEH, F01AFH (TSR07) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSRmn	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OVF

OVF	Counter overflow status of channel n
0	Overflow does not occur.
1	Overflow occurs.
When OVF = 1, this flag is cleared (OVF = 0) when the next value is captured without overflow.	

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Table 6-5. OVF Bit Operation and Set/Clear Conditions in Each Operation Mode

Timer operation mode	OVF bit	Set/clear conditions
• Capture mode	clear	When no overflow has occurred upon capturing
• Capture & one-count mode	set	When an overflow has occurred upon capturing
• Interval timer mode	clear	— (Use prohibited)
• Event counter mode	set	
• One-count mode		

Remark The OVF bit does not change immediately after the counter has overflowed, but changes upon the subsequent capture.

6.3.5 Timer channel enable status register m (TE_m)

The TE_m register is used to enable or stop the timer operation of each channel.

Each bit of the TE_m register corresponds to each bit of the timer channel start register m (TSM) and the timer channel stop register m (TTM). When a bit of the TSM register is set to 1, the corresponding bit of this register is set to 1. When a bit of the TTM register is set to 1, the corresponding bit of this register is cleared to 0.

The TE_m register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the TE_m register can be set with a 1-bit or 8-bit memory manipulation instruction with TE_mL.

Reset signal generation clears this register to 0000H.

Figure 6-14. Format of Timer Channel Enable Status register m (TE_m)

Address: F01B0H, F01B1H (TE₀) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TE _m	0	0	0	0	TEH _m 3	0	TEH _m 1	0	TE _m 7	TE _m 6	TE _m 5	TE _m 4	TE _m 3	TE _m 2	TE _m 1	TE _m 0

TEH 03	Indication of whether operation of the higher 8-bit timer is enabled or stopped when channel 3 is in the 8-bit timer mode
0	Operation is stopped.
1	Operation is enabled.

TEH 01	Indication of whether operation of the higher 8-bit timer is enabled or stopped when channel 1 is in the 8-bit timer mode
0	Operation is stopped.
1	Operation is enabled.

TE _m n	Indication of operation enable/stop status of channel n
0	Operation is stopped.
1	Operation is enabled.
This bit displays whether operation of the lower 8-bit timer for TE _m 1 and TE _m 3 is enabled or stopped when channel 1 or 3 is in the 8-bit timer mode.	

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.6 Timer channel start register m (TSm)

The TSm register is a trigger register that is used to initialize timer count register mn (TCRmn) and start the counting operation of each channel.

When a bit of this register is set to 1, the corresponding bit of timer channel enable status register m (TEm) is set to 1. The TSmn, TSHm1, TSHm3 bits are immediately cleared when operation is enabled (TEmn, TEHm1, TEHm3 = 1), because they are trigger bits.

The TSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TSm register can be set with a 1-bit or 8-bit memory manipulation instruction with TSmL.

Reset signal generation clears this register to 0000H.

Figure 6-15. Format of Timer Channel Start register m (TSm)

Address: F01B2H, F01B3H (TS0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSm	0	0	0	0	TSHm3	0	TSHm1	0	TSm7	TSm6	TSm5	TSm4	TSm3	TSm2	TSm1	TSm0

TSHm3	Trigger to enable operation (start operation) of the higher 8-bit timer when channel 3 is in the 8-bit timer mode
0	No trigger operation
1	The TEHm3 bit is set to 1 and the count operation becomes enabled. The TCRm3 register count operation start in the interval timer mode in the count operation enabled state (see Table 6-6 in 6.5.2 Start timing of counter).

TSHm1	Trigger to enable operation (start operation) of the higher 8-bit timer when channel 1 is in the 8-bit timer mode
0	No trigger operation
1	The TEHm1 bit is set to 1 and the count operation becomes enabled. The TCRm1 register count operation start in the interval timer mode in the count operation enabled state (see Table 6-6 in 6.5.2 Start timing of counter).

TSmn	Operation enable (start) trigger of channel n
0	No trigger operation
1	The TEmn bit is set to 1 and the count operation becomes enabled. The TCRmn register count operation start in the count operation enabled state varies depending on each operation mode (see Table 6-6 in 6.5.2 Start timing of counter). This bit is the trigger to enable operation (start operation) of the lower 8-bit timer for TSm1 and TSm3 when channel 1 or 3 is in the 8-bit timer mode.

Cautions 1. Be sure to clear bits 15 to 12, 10, 8 to "0"

2. When switching from a function that does not use TImn pin input to one that does, the following wait period is required from when timer mode register mn (TMRmn) is set until the TSmn (TSHm1, TSHm3) bit is set to 1.

When the TImn pin noise filter is enabled (TNFENmn = 1): Four cycles of the operation clock (fMCK)

When the TImn pin noise filter is disabled (TNFENmn = 0): Two cycles of the operation clock (fMCK)

Remarks 1. When the TSm register is read, 0 is always read.

2. m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

6.3.7 Timer channel stop register m (TTm)

The TTm register is a trigger register that is used to stop the counting operation of each channel.

When a bit of this register is set to 1, the corresponding bit of timer channel enable status register m (TEm) is cleared to 0. The TTmn, TTHm1, TTHm3 bits are immediately cleared when operation is stopped (TEmn, TEHm1, TEHm3 = 0), because they are trigger bits.

The TTm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TTm register can be set with a 1-bit or 8-bit memory manipulation instruction with TTmL.

Reset signal generation clears this register to 0000H.

Figure 6-16. Format of Timer Channel Stop register m (TTm)

Address: F01B4H, F01B5H (TT0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTm	0	0	0	0	TTHm 3	0	TTHm 1	0	TTm 7	TTm 6	TTm 5	TTm 4	TTm 3	TTm 2	TTm 1	TTm 0

TTH m3	Trigger to stop operation of the higher 8-bit timer when channel 3 is in the 8-bit timer mode
0	No trigger operation
1	TEHm3 bit clear to 0, to be count operation stop status.

TTH m1	Trigger to stop operation of the higher 8-bit timer when channel 1 is in the 8-bit timer mode
0	No trigger operation
1	TEHm1 bit clear to 0, to be count operation stop status.

TTm n	Operation stop trigger of channel n
0	No trigger operation
1	TEmn bit clear to 0, to be count operation stop status. This bit is the trigger to stop operation of the lower 8-bit timer for TTm1 and TTm3 when channel 1 or 3 is in the 8-bit timer mode.

Caution Be sure to clear bits 15 to 12, 10, 8 of the TTm register to “0”.

Remarks 1. When the TTm register is read, 0 is always read.

2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.8 Timer input select register 0 (TIS0)

The TIS0 register is used to select the channel 5 of unit 0 timer input..

The TIS0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6-17. Format of Timer Input Select register 0 (TIS0)

Address: F0074H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	0	0	0	0	0	TIS02	TIS01	TIS00

TIS02	TIS01	TIS00	Selection of timer input used with channel 5
0	0	0	Input signal of timer input pin (TI05)
0	0	1	
0	1	0	
0	1	1	
1	0	0	Low-speed on-chip oscillator clock (f_{IL})
1	0	1	Subsystem clock (f_{SUB})
Other than above			Setting prohibited

Caution High-level width, low-level width of timer input is selected, will require more than $1/f_{MCK} + 10$ ns.
Therefore, when selecting f_{SUB} to f_{CLK} (CSS bit of CKS register = 1), can not TIS02 bit set to 1.

6.3.9 Timer output enable register m (TOEm)

The TOEm register is used to enable or disable timer output of each channel.

Channel n for which timer output has been enabled becomes unable to rewrite the value of the TOmn bit of timer output register m (TOm) described later by software, and the value reflecting the setting of the timer output function through the count operation is output from the timer output pin (TOmn).

The TOEm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOEm register can be set with a 1-bit or 8-bit memory manipulation instruction with TOEmL.

Reset signal generation clears this register to 0000H.

Figure 6-18. Format of Timer Output Enable register m (TOEm)

Address: F01BAH, F01BBH (TOE0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOEm	0	0	0	0	0	0	0	0	TOE m7	TOE m6	TOE m5	TOE m4	TOE m3	0	TOE m1	TOE m0

TOE mn	Timer output enable/disable of channel n
0	Disable output of timer. Without reflecting on TOmn bit timer operation, to fixed the output. Writing to the TOmn bit is enabled, and level set to TOmn bit is output from the TOmn pin.
1	Enable output of timer. Reflected in the TOmn bit timer operation, to generate the output waveform. Writing to the TOmn bit is disabled (writing is ignored).

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Caution Be sure to clear bits 15 to 8 to “0”.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

6.3.10 Timer output register m (TOM)

The TOM register is a buffer register of timer output of each channel.

The value of each bit in this register is output from the timer output pin (TOMn) of each channel.

The TOMn bit of this register can be rewritten by software only when timer output is disabled (TOEmn = 0). When timer output is enabled (TOEmn = 1), rewriting this register by software is ignored, and the value is changed only by the timer operation.

To use the P00/TI00, P01/TO00, P16/TI01/TO01, P31/TI03/TO03, P42/TI04/TO04, P05/TI05/TO05, P06/TI06/TO06, P41/TI07/TO07 pin as a port function pin, set the corresponding TOMn bit to "0".

The TOM register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOM register can be set with an 8-bit memory manipulation instruction with TOML.

Reset signal generation clears this register to 0000H.

Figure 6-19. Format of Timer Output register m (TOM)

Address: F01B8H, F01B9H (TO0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOM	0	0	0	0	0	0	0	0	TOM 7	TOM 6	TOM 5	TOM 4	TOM 3	0	TOM 1	TOM 0

TOM n	Timer output of channel n
0	Timer output value is "0".
1	Timer output value is "1".

Caution Be sure to clear bits 15 to 8 to "0".

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TIMn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

6.3.11 Timer output level register m (TOLm)

The TOLm register is a register that controls the timer output level of each channel.

The setting of the inverted output of channel n by this register is reflected at the timing of set or reset of the timer output signal while the timer output is enabled (TOEmn = 1) in the Slave channel output mode (TOMmn = 1). In the master channel output mode (TOMmn = 0), this register setting is invalid.

The TOLm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOLm register can be set with an 8-bit memory manipulation instruction with TOLmL.

Reset signal generation clears this register to 0000H.

Figure 6-20. Format of Timer Output Level register m (TOLm)

Address: F01BCH, F01BDH (TOL0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOLm	0	0	0	0	0	0	0	0	TOL m7	TOL m6	TOL m5	TOL m4	TOL m3	0	TOL m1	0

TOL mn	Control of timer output level of channel n
0	Positive logic output (active-high)
1	Negative logic output (active-low)

Caution Be sure to clear bits 15 to 8, and 0 to “0”.

- Remarks 1.** If the value of this register is rewritten during timer operation, the timer output logic is inverted when the timer output signal changes next, instead of immediately after the register value is rewritten.
- 2.** m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

6.3.12 Timer output mode register m (TOMm)

The TOMm register is used to control the timer output mode of each channel.

When a channel is used for the independent channel operation function, set the corresponding bit of the channel to be used to 0.

When a channel is used for the simultaneous channel operation function (PWM output, one-shot pulse output, or multiple PWM output), set the corresponding bit of the master channel to 0 and the corresponding bit of the slave channel to 1.

The setting of each channel n by this register is reflected at the timing when the timer output signal is set or reset while the timer output is enabled ($TOEmn = 1$).

The TOMm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOMm register can be set with an 8-bit memory manipulation instruction with TOMmL.

Reset signal generation clears this register to 0000H.

Figure 6-21. Format of Timer Output Mode register m (TOMm)

Address: F01BEH, F01BFH (TOM0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOMm	0	0	0	0	0	0	0	0	TOM m7	TOM m6	TOM m5	TOM m4	TOM m3	0	TOM m1	0

TOM mn	Control of timer output mode of channel n
0	Master channel output mode (to produce toggle output by timer interrupt request signal (INTTMmn))
1	Slave channel output mode (output is set by the timer interrupt request signal (INTTMmn) of the master channel, and reset by the timer interrupt request signal (INTTM0p) of the slave channel)

Caution Be sure to clear bits 15 to 8, and 0 to “0”.

Remark m: Unit number (m = 0)

n: Channel number

n = 0 to 7 (n = 0, 2, 4, 6 for master channel)

p: Slave channel number

n < p ≤ 7

(For details of the relation between the master channel and slave channel, refer to **6.4.1 Basic rules of simultaneous channel operation function.**)

6.3.13 Input switch control register (ISC)

The ISC1 and ISC0 bits of the ISC register are used to implement LIN-bus communication operation by using channel 7 in association with the serial array unit. When the ISC1 bit is set to 1, the input signal of the serial data input pin (RxD2) is selected as a timer input signal.

The ISC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6-22. Format of Input Switch Control Register (ISC)

Address: F0073H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	0	0	0	0	ISC1	ISC0

ISC1	Switching channel 7 input of timer array unit
0	32, 48, and 64-pin products: Uses the input signal of the TI07 pin as a timer input (normal operation). 25-pin products: Do not use a timer input signal for channel 7.
1	Input signal of the RxD2 pin is used as timer input (detects the wakeup signal and measures the low width of the break field and the pulse width of the sync field). Setting is prohibited in the 25-pin products.

ISC0	Switching external interrupt (INTP0) input
0	Uses the input signal of the INTP0 pin as an external interrupt (normal operation).
1	Uses the input signal of the RxD2 pin as an external interrupt (wakeup signal detection).

Caution Be sure to clear bits 7 to 2 to “0”.

Remark When the LIN-bus communication function is used, select the input signal of the RxD2 pin by setting ISC1 to 1.

6.3.14 Noise filter enable register 1 (NFEN1)

The NFEN1 register is used to set whether the noise filter can be used for the timer input signal to each channel.

Enable the noise filter by setting the corresponding bits to 1 on the pins in need of noise removal.

When the noise filter is ON, match detection and synchronization of the 2 clocks is performed with the CPU/peripheral hardware clock (f_{MCK}). When the noise filter is OFF, only synchronization is performed with the CPU/peripheral hardware clock (f_{MCK}) ^{Note}.

The NFEN1 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Note For details, see **6.5.1 (2) When valid edge of input signal input from the TImn pin is selected (CCSmn = 1)** and **6.5.2 Start timing of counter**.

Figure 6-23. Format of Noise Filter Enable Register 1 (NFEN1)

Address: F0071H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN1	TNFEN07	TNFEN06	TNFEN05	TNFEN04	TNFEN03	0	TNFEN01	TNFEN00

TNFEN07	Enable/disable using noise filter of TI07/TO07/P41 pin or RxD2/P14 pin input signal ^{Note}
0	Noise filter OFF
1	Noise filter ON

TNFEN06	Enable/disable using noise filter of TI06/TO06/P06 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN05	Enable/disable using noise filter of TI05/TO05/P05 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN04	Enable/disable using noise filter of TI04/TO04/P42 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN03	Enable/disable using noise filter of TI03/TO03/P31 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN01	Enable/disable using noise filter of TI01/TO01/P16 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN00	Enable/disable using noise filter of TI00/P00 pin input signal
0	Noise filter OFF
1	Noise filter ON

Note The applicable pin can be switched by setting the ISC1 bit of the ISC register.

ISC1 = 0: Whether or not to use the noise filter of the TI07 pin can be selected.

ISC1 = 1: Whether or not to use the noise filter of the RxD2 pin can be selected.

Caution Be sure to clear bit 2 to “0”.

Remark The presence or absence of timer I/O pins of channel 0 to 7 depends on the product. See **Table 6-2 Timer I/O Pins provided in Each Product** for details.

6.3.15 Port mode registers 0, 1, 3, 4 (PM0, PM1, PM3, PM4)

These registers set input/output of ports 0, 1, 3, 4 in 1-bit units.

The presence or absence of timer I/O pins depends on the product. When using the timer array unit, set the following port mode registers according to the product used.

25 and 32-pin products: PM0, PM3

48 and 64-pin products: PM0, PM1, PM3, PM4

When using the ports (such as P01/TO00 and P16/TO01/TI01) to be shared with the timer output pin for timer output, set the port mode register (PMxx) bit and port register (Pxx) bit corresponding to each port to 0.

Example: When using P16/TO01/TI01 for timer output

Set the PM16 bit of port mode register 1 to 0.

Set the P16 bit of port register 1 to 0.

When using the ports (such as P00/TI00 and P16/TO01/TI01) to be shared with the timer input pin for timer input, set the port mode register (PMxx) bit corresponding to each port to 1. At this time, the port register (Pxx) bit may be 0 or 1.

Example: When using P16/TO01/TI01 for timer input

Set the PM16 bit of port mode register 1 to 1.

Set the P16 bit of port register 1 to 0 or 1.

The PM0, PM1, PM3, PM4 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark In the 25- and 32-pin products, TI00 (P00), TO00 (P01), TI03/TO03 (P31), and TI07/TO07 (P41) pins alternate analog input pins. When using the timer I/O function, the corresponding bit of the PMC0 register for switching digital I/O or analog input is sure to set to "0".

**Figure 6-24. Format of Port Mode Registers 0, 1, 3, 4 (PM0, PM1, PM3, PM4)
(64-pin products)**

Address: FFF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

Address: FFF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	1	1	PM31	PM30

Address: FFF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	1	1	1	1	PM43	PM42	PM41	PM40

PMmn	Pmn pin I/O mode selection (m = 0, 1, 3, 4; n = 0 to 6)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode registers 0, 1, 3, 4 of the 64-pin products. The format of the port mode register of other products, see **4.3.1 Port mode registers (PMxx)**.

6.4 Basic Rules of Timer Array Unit

6.4.1 Basic rules of simultaneous channel operation function

When simultaneously using multiple channels, namely, a combination of a master channel (a reference timer mainly counting the cycle) and slave channels (timers operating according to the master channel), the following rules apply.

- (1) Only an even channel (channel 0, 2, 4, etc.) can be set as a master channel.
- (2) Any channel, except channel 0, can be set as a slave channel.
- (3) The slave channel must be lower than the master channel.

Example: If channel 2 is set as a master channel, channel 3 or those that follow (channels 3, 4, 5, etc.) can be set as a slave channel.

- (4) Two or more slave channels can be set for one master channel.
- (5) When two or more master channels are to be used, slave channels with a master channel between them may not be set.

Example: If channels 0 and 4 are set as master channels, channels 1 to 3 can be set as the slave channels of master channel 0. Channels 5 to 7 cannot be set as the slave channels of master channel 0.

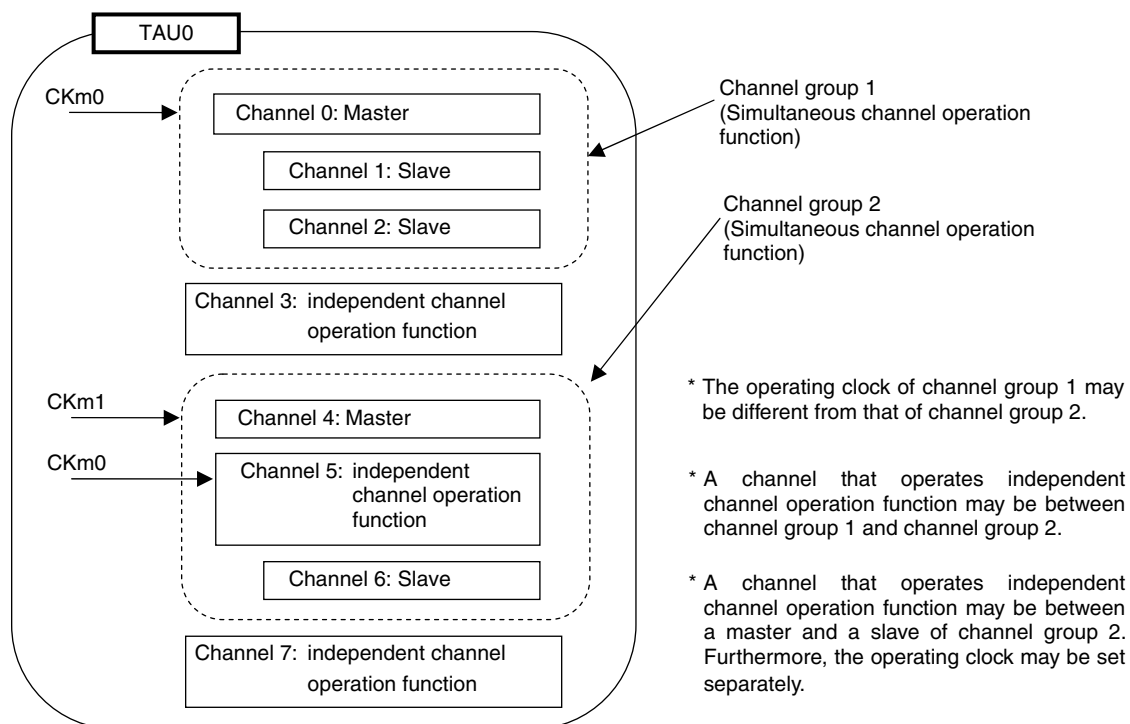
- (6) The operating clock for a slave channel in combination with a master channel must be the same as that of the master channel. The CKSmn0, CKSmn1 bits (bit 15, 14 of timer mode register mn (TMRmn)) of the slave channel that operates in combination with the master channel must be the same value as that of the master channel.
- (7) A master channel can transmit INTTMmn (interrupt), start software trigger, and count clock to the lower channels.
- (8) A slave channel can use INTTMmn (interrupt), a start software trigger, or the count clock of the master channel as a source clock, but cannot transmit its own INTTMmn (interrupt), start software trigger, or count clock to channels with lower channel numbers.
- (9) A master channel cannot use INTTMmn (interrupt), a start software trigger, or the count clock from the other higher master channel as a source clock.
- (10) To simultaneously start channels that operate in combination, the channel start trigger bit (TSMn) of the channels in combination must be set at the same time.
- (11) During the counting operation, a TSMn bit of a master channel or TSMn bits of all channels which are operating simultaneously can be set. It cannot be applied to TSMn bits of slave channels alone.
- (12) To stop the channels in combination simultaneously, the channel stop trigger bit (TTmn) of the channels in combination must be set at the same time.
- (13) CKm2/CKm3 cannot be selected while channels are operating simultaneously, because the operating clocks of master channels and slave channels have to be synchronized.
- (14) Timer mode register m0 (TMRm0) has no master bit (it is fixed as "0"). However, as channel 0 is the highest channel, it can be used as a master channel during simultaneous operation.

The rules of the simultaneous channel operation function are applied in a channel group (a master channel and slave channels forming one simultaneous channel operation function).

If two or more channel groups that do not operate in combination are specified, the basic rules of the simultaneous channel operation function in **6.4.1 Basic rules of simultaneous channel operation function** do not apply to the channel groups.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

Example



6.4.2 Basic rules of 8-bit timer operation function (channels 1 and 3 only)

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels.

This function can only be used for channels 1 and 3, and there are several rules for using it.

The basic rules for this function are as follows:

- (1) The 8-bit timer operation function applies only to channels 1 and 3.
- (2) When using 8-bit timers, set the SPLIT bit of timer mode register mn (TMRmn) to 1.
- (3) The higher 8 bits can be operated as the interval timer function.
- (4) At the start of operation, the higher 8 bits output INTTMm1H/INTTMm3H (an interrupt) (which is the same operation performed when MDmn0 is set to 1).
- (5) The operation clock of the higher 8 bits is selected according to the CKSmn1 and CKSmn0 bits of the lower-bit TMRmn register.
- (6) For the higher 8 bits, the TSHm1/TSHm3 bit is manipulated to start channel operation and the TTHm1/TTHm3 bit is manipulated to stop channel operation. The channel status can be checked using the TEHm1/TEHm3 bit.
- (7) The lower 8 bits operate according to the TMRmn register settings. The following three functions support operation of the lower 8 bits:
 - Interval timer function
 - External event counter function
 - Delay count function
- (8) For the lower 8 bits, the TSm1/TSm3 bit is manipulated to start channel operation and the TTm1/TTm3 bit is manipulated to stop channel operation. The channel status can be checked using the TEM1/TEM3 bit.
- (9) During 16-bit operation, manipulating the TSHm1, TSHm3, TTHm1, and TTHm3 bits is invalid. The TSm1, TSm3, TTm1, and TTm3 bits are manipulated to operate channels 1 and 3. The TEHm3 and TEHm1 bits are not changed.
- (10) For the 8-bit timer function, the simultaneous operation functions (one-shot pulse, PWM, and multiple PWM) cannot be used.

Remark m: Unit number (m = 0), n: Channel number (n = 1, 3)

6.5 Operation of Counter

6.5.1 Count clock (f_{CLK})

The count clock (f_{CLK}) of the timer array unit can be selected between following by CCSmn bit of timer mode register mn (TMRmn).

- Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
- Valid edge of input signal input from the TImn pin

Because the timer array unit is designed to operate in synchronization with f_{CLK} , the timings of the count clock (f_{CLK}) are shown below.

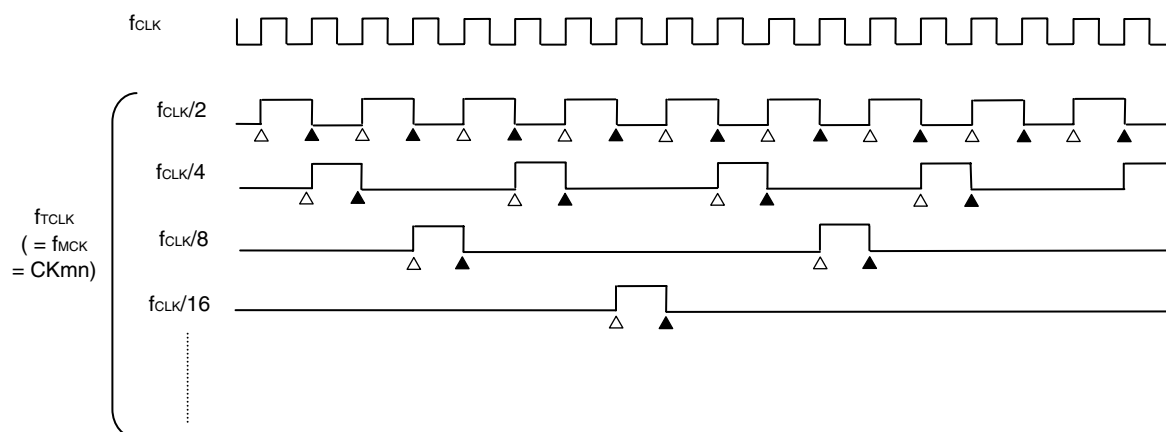
(1) When operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits is selected (CCSmn = 0)

<R>

The count clock (f_{CLK}) is between f_{CLK} to $f_{\text{CLK}}/2^{15}$ by setting of timer clock select register m (TPSm). When a divided f_{CLK} is selected, however, the clock selected in TPSmn register, but a signal which becomes high level for one period of f_{CLK} from its rising edge. When a f_{CLK} is selected, fixed to high level.

Counting of timer count register mn (TCRmn) delayed by one period of f_{CLK} from rising edge of the count clock, because of synchronization with f_{CLK} . But, this is described as “counting at rising edge of the count clock”, as a matter of convenience.

Figure 6-25. Timing of f_{CLK} and count clock (f_{CLK}) (When Ccsmn = 0)



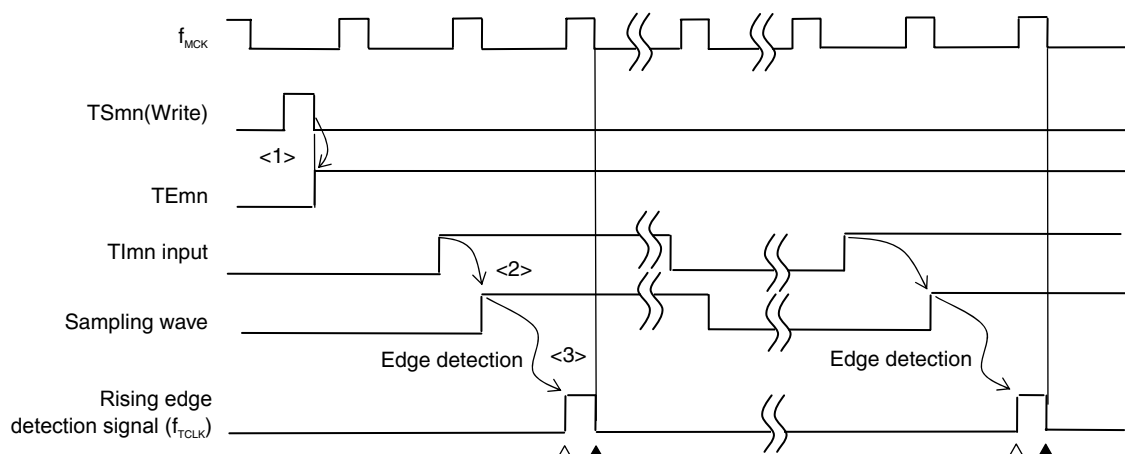
- Remarks**
1. Δ : Rising edge of the count clock
 $\blacktriangle$: Synchronization, increment/decrement of counter
 2. f_{CLK} : CPU/peripheral hardware clock
 3. m: Unit number ($m = 0$), n: Channel number ($n = 0$ to 7 (however, timer input pin (TImn), timer output pin (TOmn) : $n = 0, 1, 3$ to 7))

(2) When valid edge of input signal via the TImn pin is selected (CCSmn = 1)

The count clock (f_{TCLK}) becomes the signal that detects valid edge of input signal via the TImn pin and synchronizes next rising f_{MCK} . The count clock (f_{TCLK}) is delayed for 1 to 2 period of f_{MCK} from the input signal via the TImn pin (when a noise filter is used, the delay becomes 3 to 4 clock).

Counting of timer count register mn (TCRmn) delayed by one period of f_{CLK} from rising edge of the count clock, because of synchronization with f_{CLK} . But, this is described as “counting at valid edge of input signal via the TImn pin”, as a matter of convenience.

Figure 6-26. Timing of f_{CLK} and count clock (f_{TCLK}) (When CCSmn = 1, noise filter unused)



<1> Setting TSmn bit to 1 enables the timer to be started and to become wait state for valid edge of input signal via the TImn pin.

<2> The rise of input signal via the TImn pin is sampled by f_{MCK} .

<3> The edge is detected by the rising of the sampled signal and the detection signal (count clock) is output.

Remarks 1. Δ : Rising edge of the count clock

$\blacktriangle$: Synchronization, increment/decrement of counter

2. f_{CLK} : CPU/peripheral hardware clock

f_{MCK} : Operation clock of channel n

3. The waveform of the input signal via TImn pin of the input pulse interval measurement, the measurement of high/low width of input signal, and the delay counter, the one-shot pulse output are the same as that shown in Figure 6-22.

4. m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

6.5.2 Start timing of counter

Operation of timer count register mn (TCRmn) is enabled by setting of TSmn bit of timer channel start register m (TSM).

Operation from when counting is enabled to when timer count register mn (TCRmn) starts counting is shown in Table 6-6.

<R> **Table 6-6. Operations from Count Operation Enabled State to Timer count Register mn (TCRmn) Count Start**

Timer operation mode	Operation when TSmn = 1 is set
Interval timer mode	No operation is carried out from start trigger detection (TSmn=1) until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation (see 6.5.3 (1) Operation of interval timer mode).
Event counter mode	Writing 1 to the TSmn bit loads the value of the TDRmn register to the TCRmn register. If detect edge of TImn input. The subsequent count clock performs count down operation (see 6.5.3 (2) Operation of event counter mode).
Capture mode	No operation is carried out from start trigger detection (TSmn = 1) until count clock generation. The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation (see 6.5.3 (3) Operation of capture mode (input pulse interval measurement)).
One-count mode	The waiting-for-start-trigger state is entered by writing 1 to the TSmn bit while the timer is stopped (TEmn = 0). No operation is carried out from start trigger detection until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation (see 6.5.3 (4) Operation of one-count mode).
Capture & one-count mode	The waiting-for-start-trigger state is entered by writing 1 to the TSmn bit while the timer is stopped (TEmn = 0). No operation is carried out from start trigger detection until count clock generation. The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation (see 6.5.3 (5) Operation of capture & one-count mode (high-level interval measurement)).

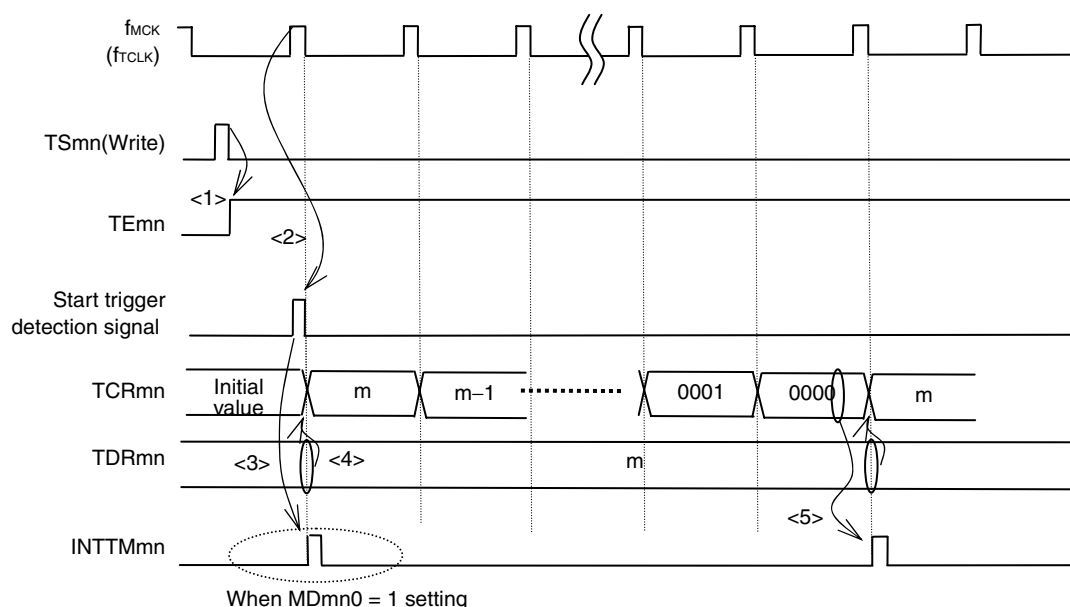
<R> 6.5.3 Operation of counter

Here, the counter operation in each mode is explained.

(1) Operation of interval timer mode

- <1> Operation is enabled ($TE_{mn} = 1$) by writing 1 to the TS_{mn} bit. Timer count register mn (TCR_{mn}) holds the initial value until count clock generation.
- <2> A start trigger is generated at the first count clock after operation is enabled.
- <3> When the MD_{mn0} bit is set to 1, $INTT_{mn}$ is generated by the start trigger.
- <4> By the first count clock after the operation enable, the value of timer data register mn (TDR_{mn}) is loaded to the TCR_{mn} register and counting starts in the interval timer mode.
- <5> When the TCR_{mn} register counts down and its count value is 0000H, $INTT_{mn}$ is generated and the value of timer data register mn (TDR_{mn}) is loaded to the TCR_{mn} register and counting keeps on.

Figure 6-27. Operation Timing (In Interval Timer Mode)

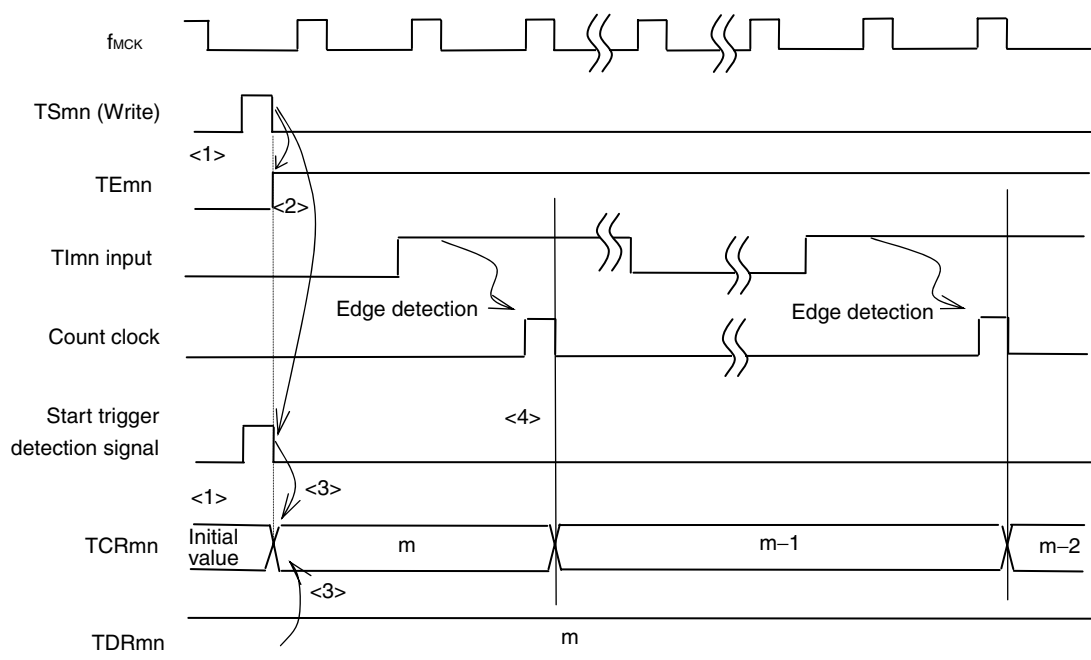


Caution In the operation in the first count clock cycle after writing the TS_{mn} bit, an error at a maximum of one count clock cycle occurs since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated when counting is started by setting $MD_{mn0} = 1$.

- Remarks**
1. f_{MCK} , the start trigger detection signal, and $INTT_{mn}$ become active between one clock in synchronization with f_{CLK} .
 2. m : Unit number ($m = 0$), n : Channel number ($n = 0$ to 7 (however, timer input pin (TI_{mn}), timer output pin (TO_{mn}) : $n = 0, 1, 3$ to 7))

(2) Operation of event counter mode

- <1> Timer count register mn (TCRmn) holds its initial value while operation is stopped ($TE_{mn} = 0$).
- <2> Operation is enabled ($TE_{mn} = 1$) by writing 1 to the TSmn bit.
- <3> As soon as 1 has been written to the TSmn bit and 1 has been set to the TE_{mn} bit, the value of timer data register mn (TDRmn) is loaded to the TCRmn register to start counting.
- <4> After that, the TCRmn register value is counted down according to the count clock of the valid edge of the TImn input.

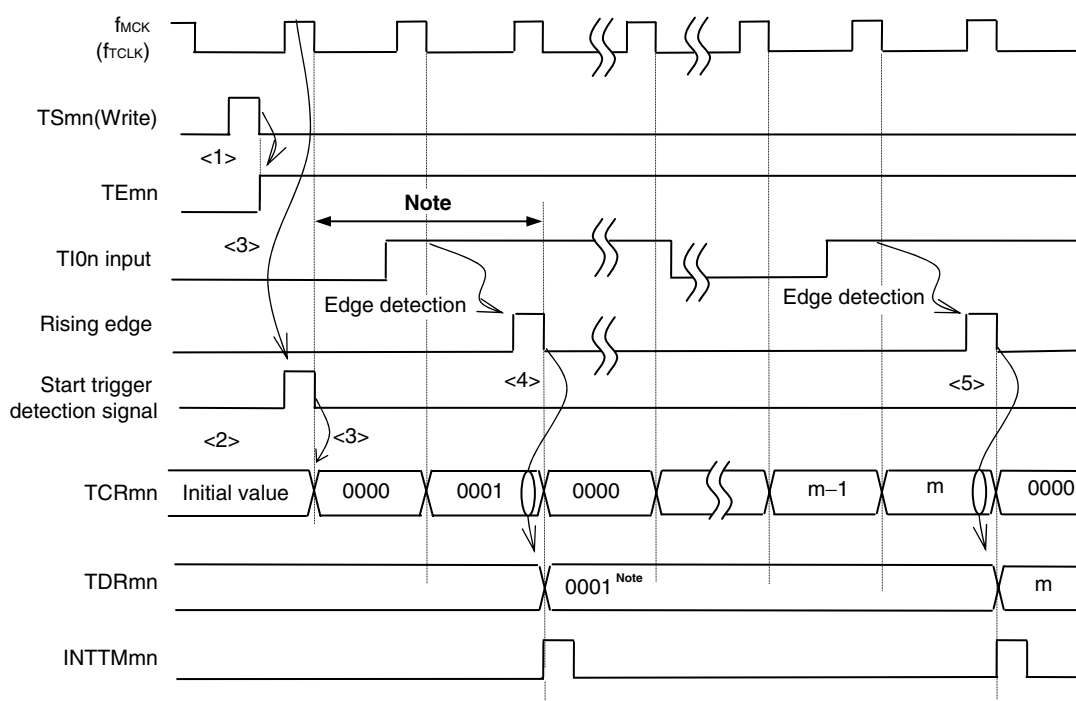
Figure 6-28. Operation Timing (In Event Counter Mode)

- Remarks 1.** The timing is shown in Figure 6-24 indicates while the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2 f_{MCK} cycles (it sums up to 3 to 4 cycles) later than the normal cycle of TImn input.
- 2.** m: Unit number ($m = 0$), n: Channel number ($n = 0$ to 7 (however, timer input pin (TImn), timer output pin (TOMn) : $n = 0, 1, 3$ to 7))

(3) Operation of capture mode (input pulse interval measurement)

- <1> Operation is enabled ($TE_{mn} = 1$) by writing 1 to the TS_{mn} bit.
- <2> Timer count register mn (TCR_{mn}) holds the initial value until count clock generation.
- <3> A start trigger is generated at the first count clock after operation is enabled. And the value of 0000H is loaded to the TCR_{mn} register and counting starts in the capture mode. (When the MD_{mn0} bit is set to 1, $INTTM_{mn}$ is generated by the start trigger.)
- <4> On detection of the valid edge of the TI_{mn} input, the value of the TCR_{mn} register is captured to timer data register mn (TDR_{mn}) and $INTTM_{mn}$ is generated. However, this capture value is no meaning. The TCR_{mn} register keeps on counting from 0000H.
- <5> On next detection of the valid edge of the TI_{mn} input, the value of the TCR_{mn} register is captured to timer data register mn (TDR_{mn}) and $INTTM_{mn}$ is generated.

<R> **Figure 6-29. Operation Timing (In Capture Mode : Input Pulse Interval Measurement)**



<R> **Note** If a clock has been input to TI_{mn} (the trigger exists) when capturing starts, counting starts when a trigger is detected, even if no edge is detected. Therefore, the first captured value (<4>) does not determine a pulse interval (in the above figure, 0001 just indicates two clock cycles but does not determine the pulse interval) and so the user can ignore it.

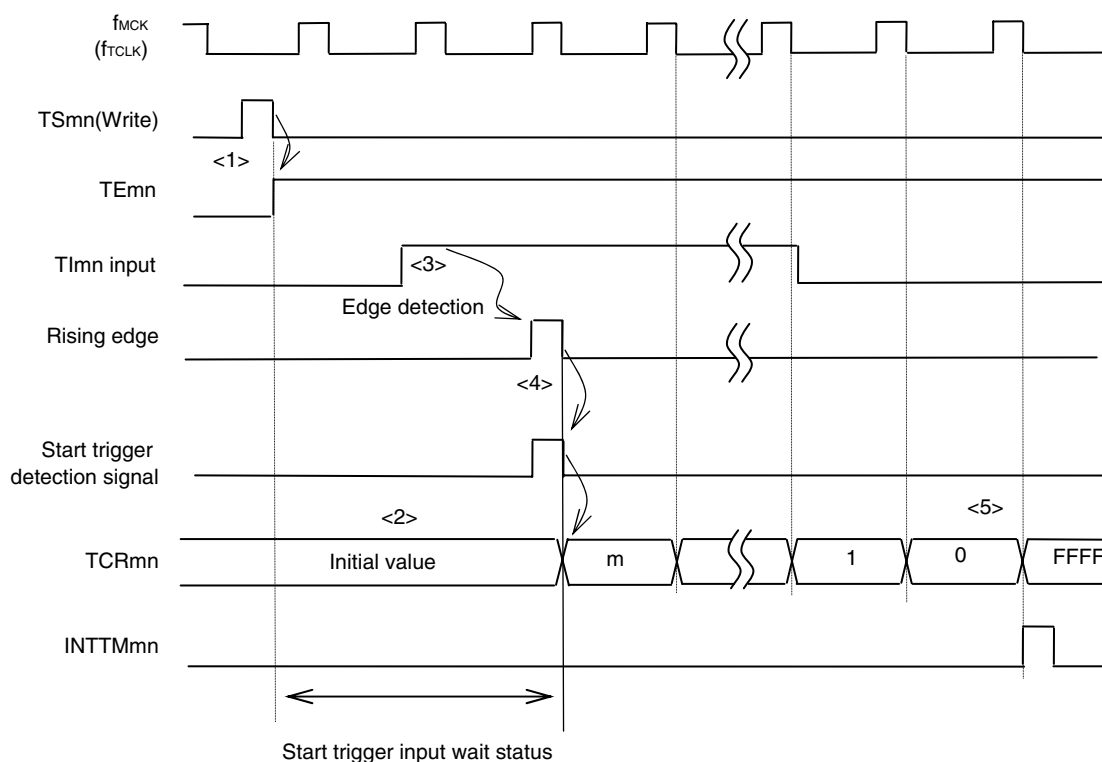
Caution In the first cycle operation of count clock after writing the TS_{mn} bit, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting $MD_{mn0} = 1$.

<R> **Remarks 1.** The timing is shown in Figure 6-25 indicates while the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2 f_{MCK} cycles (it sums up to 3 to 4 cycles) later than the normal cycle of TI_{mn} input.

2. m : Unit number ($m = 0$), n : Channel number ($n = 0$ to 7 (however, timer input pin (TI_{mn}), timer output pin (TO_{mn}) : $n = 0, 1, 3$ to 7))

(4) Operation of one-count mode

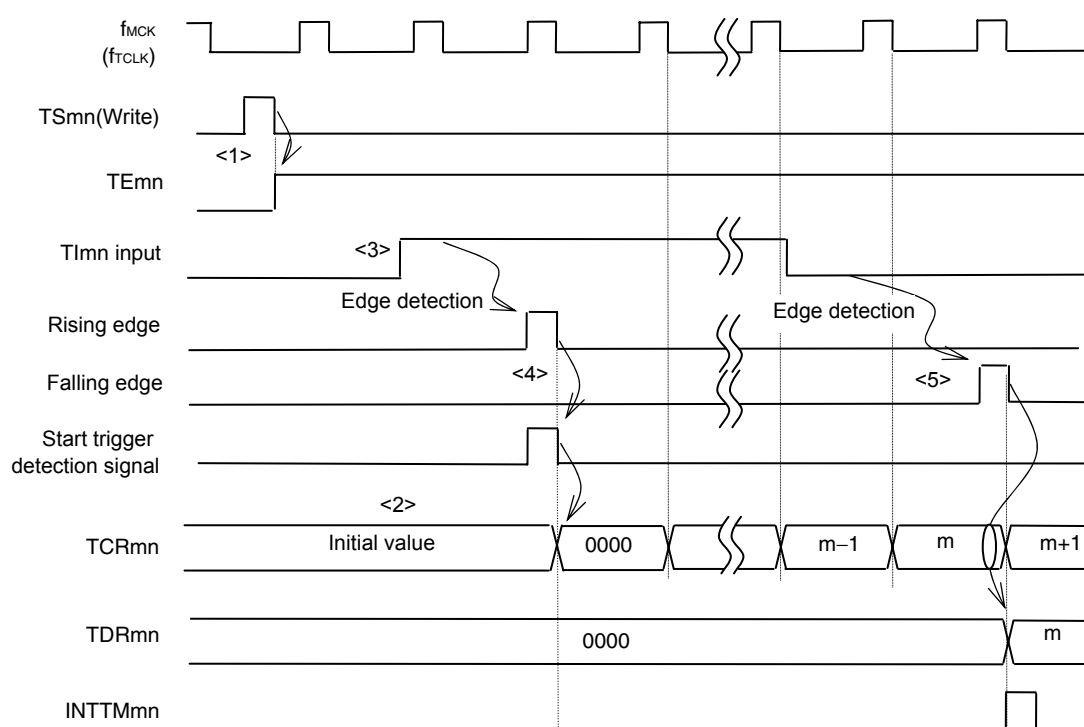
- <1> Operation is enabled ($TE_{mn} = 1$) by writing 1 to the TS_{mn} bit.
- <2> Timer count register mn (TCR_{mn}) holds the initial value until start trigger generation.
- <3> Rising edge of the TI_{mn} input is detected.
- <4> On start trigger detection, the value of timer data register mn (TDR_{mn}) is loaded to the TCR_{mn} register and count starts.
- <5> When the TCR_{mn} register counts down and its count value is 0000H, $INTTM_{mn}$ is generated and the value of the TCR_{mn} register becomes FFFFH and counting stops

Figure 6-30. Operation Timing (In One-count Mode)

- Remarks 1.** The timing is shown in Figure 6-26 indicates while the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2 f_{MCK} cycles (it sums up to 3 to 4 cycles) later than the normal cycle of TI_{mn} input. The error per one period occurs be the asynchronous between the period of the TI_{mn} input and that of the count clock (f_{MCK}).
- 2.** m : Unit number ($m = 0$), n : Channel number ($n = 0$ to 7 (however, timer input pin (TI_{mn}), timer output pin (TO_{mn}) : $n = 0, 1, 3$ to 7))

(5) Operation of capture & one-count mode (high-level width measurement)

- <1> Operation is enabled ($TE_{mn} = 1$) by writing 1 to the TS_{mn} bit of timer channel start register m (TS_m).
- <2> Timer count register mn (TCR_{mn}) holds the initial value until start trigger generation.
- <3> Rising edge of the TI_{mn} input is detected.
- <4> On start trigger detection, the value of 0000H is loaded to the TCR_{mn} register and count starts.
- <5> On detection of the falling edge of the TI_{mn} input, the value of the TCR_{mn} register is captured to timer data register mn (TDR_{mn}) and $INTTM_{mn}$ is generated.

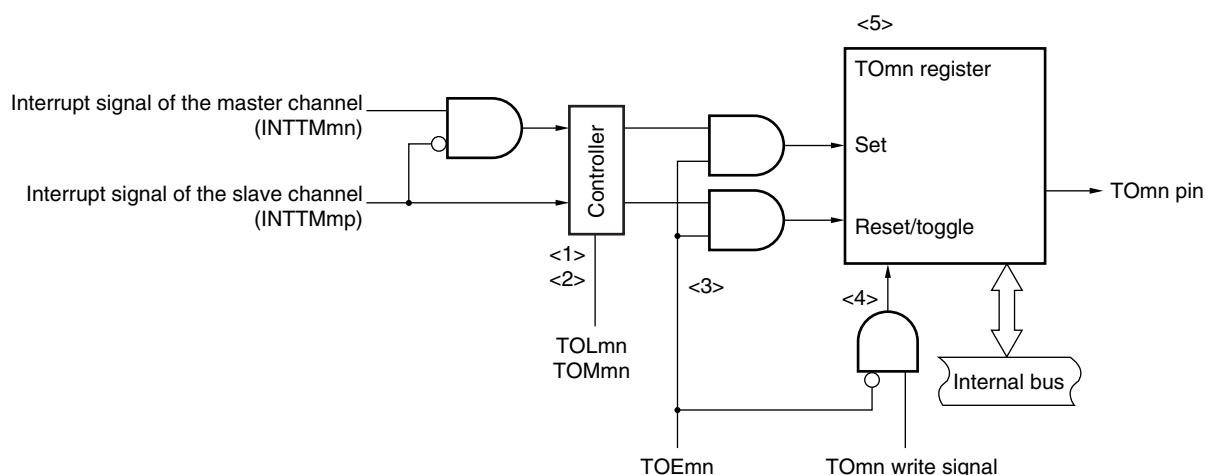
Figure 6-31. Operation Timing (In Capture & One-count Mode : High-level Width Measurement)

- <R> **Remarks 1.** The timing is shown in Figure 6-27 indicates while the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2 f_{MCK} cycles (it sums up to 3 to 4 cycles) later than the normal cycle of TI_{mn} input. The error per one period occurs be the asynchronous between the period of the TI_{mn} input and that of the count clock (f_{MCK}).
- 2.** m: Unit number ($m = 0$), n: Channel number ($n = 0$ to 7 (however, timer input pin (TI_{mn}), timer output pin (TO_{mn}) : $n = 0, 1, 3$ to 7))

6.6 Channel Output (TOMn pin) Control

6.6.1 TOMn pin output circuit configuration

Figure 6-32. Output Circuit Configuration



The following describes the TOMn pin output circuit.

- <1> When TOMmn = 0 (master channel output mode), the set value of timer output level register m (TOLm) is ignored and only INTTM0p (slave channel timer interrupt) is transmitted to timer output register m (TOM).
- <2> When TOMmn = 1 (slave channel output mode), both INTTMmn (master channel timer interrupt) and INTTM0p (slave channel timer interrupt) are transmitted to the TOM register.
At this time, the TOLm register becomes valid and the signals are controlled as follows:

When TOLmn = 0: Positive logic output (INTTMmn → set, INTTM0p → reset)

When TOLmn = 1: Negative logic output (INTTMmn → reset, INTTM0p → set)

When INTTMmn and INTTM0p are simultaneously generated, (0% output of PWM), INTTM0p (reset signal) takes priority, and INTTMmn (set signal) is masked.

- <3> While timer output is enabled (TOEmn = 1), INTTMmn (master channel timer interrupt) and INTTM0p (slave channel timer interrupt) are transmitted to the TOM register. Writing to the TOM register (TOMn write signal) becomes invalid.

When TOEmn = 1, the TOMn pin output never changes with signals other than interrupt signals.

To initialize the TOMn pin output level, it is necessary to set timer operation is stopped (TOEmn = 0) and to write a value to the TOM register.

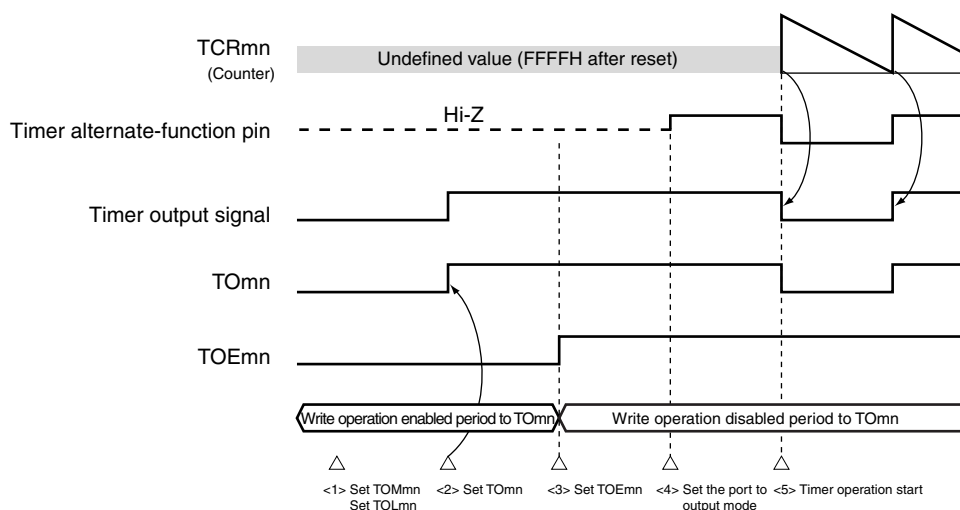
- <4> While timer output is disabled (TOEmn = 0), writing to the TOMn bit to the target channel (TOMn write signal) becomes valid. When timer output is disabled (TOEmn = 0), neither INTTMmn (master channel timer interrupt) nor INTTM0p (slave channel timer interrupt) is transmitted to the TOM register.
- <5> The TOM register can always be read, and the TOMn pin output level can be checked.

Remark m: Unit number (m = 0)
 n: Channel number
 n = 0, 1, 2 to 7 (n = 0, 4, 6 for master channel)
 p: Slave channel number
 n < p ≤ 7

6.6.2 TOMn Pin Output Setting

The following figure shows the procedure and status transition of the TOMn output pin from initial setting to timer operation start.

Figure 6-33. Status Transition from Timer Output Setting to Operation Start



<1> The operation mode of timer output is set.

- TOMmn bit (0: Master channel output mode, 1: Slave channel output mode)
- TOLmn bit (0: Positive logic output, 1: Negative logic output)

<2> The timer output signal is set to the initial status by setting timer output register m (TOM).

<3> The timer output operation is enabled by writing 1 to the TOEmn bit (writing to the TOM register is disabled).

<R> <4> The port is set to digital I/O by port mode control register (PMCxx) (see **6.3.15 Port mode registers 0, 1, 3, 4 (PM0, PM1, PM3, PM4)**).

<5> The port I/O setting is set to output (see **6.3.15 Port mode registers 0, 1, 3, 4 (PM0, PM1, PM3, PM4)**).

<6> The timer operation is enabled (TSmn = 1).

Remark m: Unit number (m = 0), n: Channel number (n = 0, 1, 3 to 7)

6.6.3 Cautions on Channel Output Operation

(1) Changing values set in the registers T_{Om}, T_{OEm}, and T_{OLm} during timer operation

Since the timer operations (operations of timer count register mn (TCR_{mn}) and timer data register mn (TDR_{mn})) are independent of the T_{Om}n output circuit and changing the values set in timer output register m (T_{Om}), timer output enable register m (T_{OEm}), and timer output level register m (T_{OLm}) does not affect the timer operation, the values can be changed during timer operation. To output an expected waveform from the T_{Om}n pin by timer operation, however, set the T_{Om}, T_{OEm}, T_{OLm}, and T_{OMm} registers to the values stated in the register setting example of each operation shown by 6.7 and 6.8.

When the values set to the T_{OEm}, and T_{OLm} registers (but not the T_{Om} register) are changed close to the occurrence of the timer interrupt (INTT_{Mmn}) of each channel, the waveform output to the T_{Om}n pin might differ, depending on whether the values are changed immediately before or immediately after the timer interrupt (INTT_{Mmn}) occurs.

Remark m: Unit number (m = 0), n: Channel number (n = 0, 1, 3 to 7)

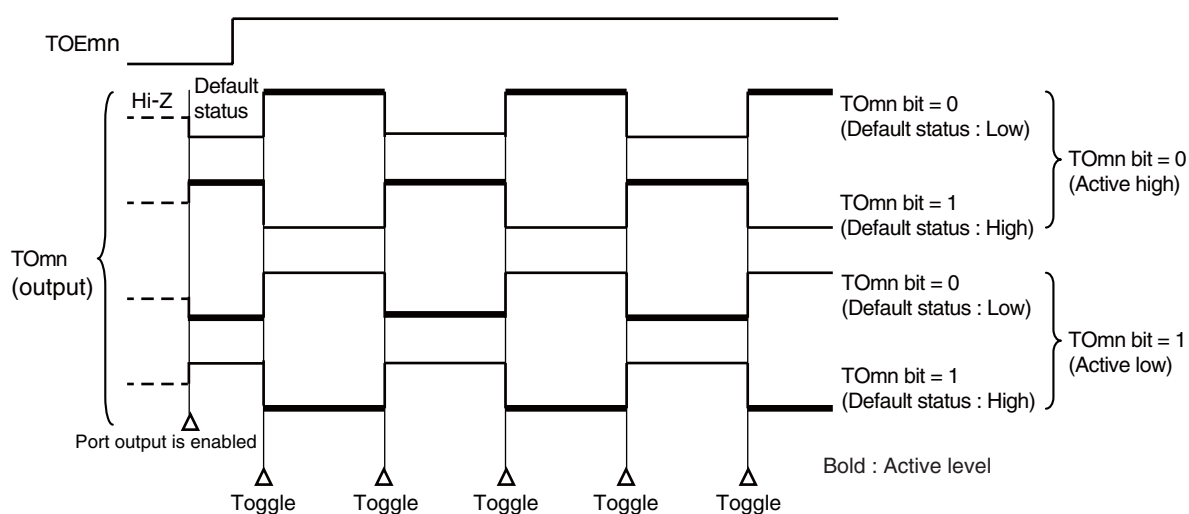
(2) Default level of TOMn pin and output level after timer operation start

The change in the output level of the TOMn pin when timer output register m (TOM) is written while timer output is disabled (TOEmn = 0), the initial level is changed, and then timer output is enabled (TOEmn = 1) before port output is enabled, is shown below.

(a) When operation starts with master channel output mode (TOMmn = 0) setting

The setting of timer output level register m (TOLm) is invalid when master channel output mode (TOMmn = 0). When the timer operation starts after setting the default level, the toggle signal is generated and the output level of the TOMn pin is reversed.

<R>

Figure 6-34. TOMn Pin Output Status at Toggle Output (TOMmn = 0)

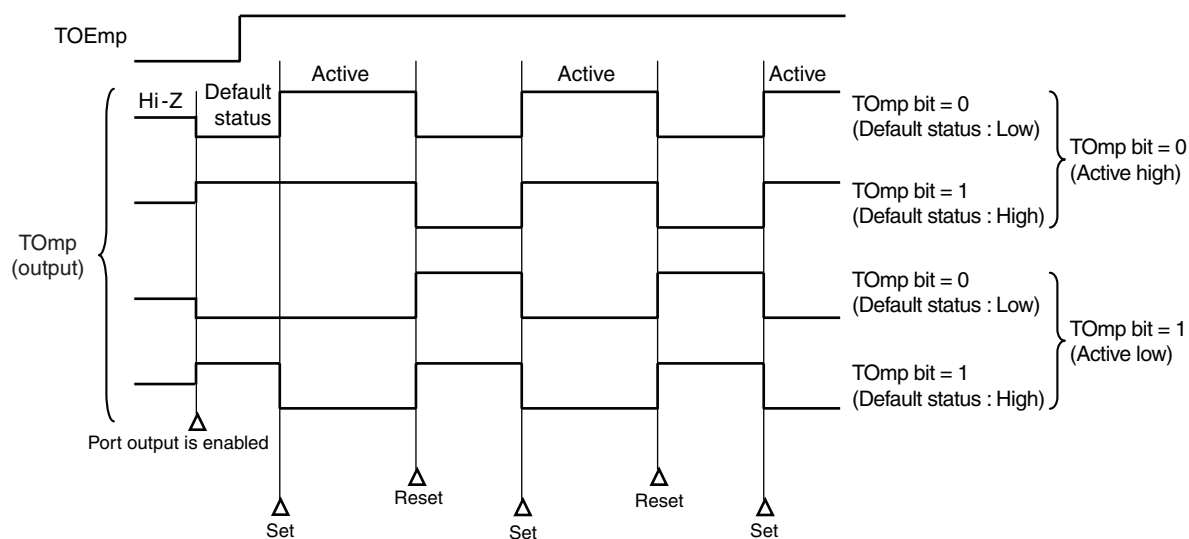
Remarks 1. Toggle: Reverse TOMn pin output status

2. m: Unit number (m = 0), n: Channel number (n = 0, 1, 3 to 7)

(b) When operation starts with slave channel output mode (TOMmp = 1) setting (PWM output)

When slave channel output mode (TOMmp = 1), the active level is determined by timer output level register m (TOLm) setting.

<R>

Figure 6-35. TOmp Pin Output Status at PWM Output (TOMmp = 1)

Remarks 1. Set: The output signal of the TOmp pin changes from inactive level to active level.

Reset: The output signal of the TOmp pin changes from active level to inactive level.

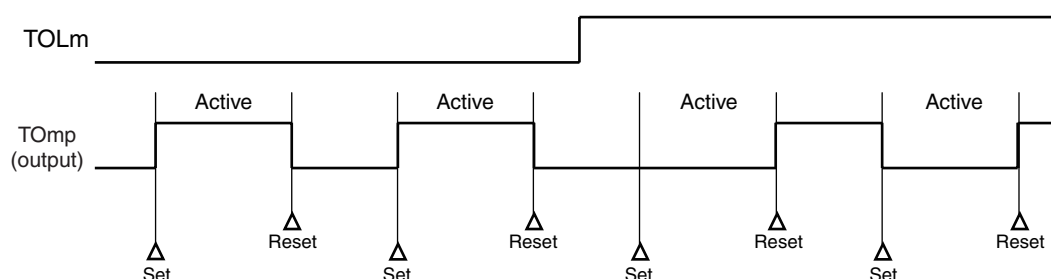
2. m: Unit number (m = 0), p: Channel number (p = 1, 3 to 7)

(3) Operation of TOMn pin in slave channel output mode (TOMmn = 1)**(a) When timer output level register m (TOLm) setting has been changed during timer operation**

When the TOLm register setting has been changed during timer operation, the setting becomes valid at the generation timing of the TOMn pin change condition. Rewriting the TOLm register does not change the output level of the TOMn pin.

The operation when TOMmn is set to 1 and the value of the TOLm register is changed while the timer is operating (TEMn = 1) is shown below.

<R> **Figure 6-36. Operation when TOLm Register Has Been Changed Contents during Timer Operation**



Remarks 1. Set: The output signal of the TOMn pin changes from inactive level to active level.

Reset: The output signal of the TOMn pin changes from active level to inactive level.

2. m: Unit number (m = 0), n: Channel number (n = 0, 1, 3 to 7)

(b) Set/reset timing

To realize 0%/100% output at PWM output, the TOMn pin/TOMn bit set timing at master channel timer interrupt (INTTMmn) generation is delayed by 1 count clock by the slave channel.

If the set condition and reset condition are generated at the same time, a higher priority is given to the latter.

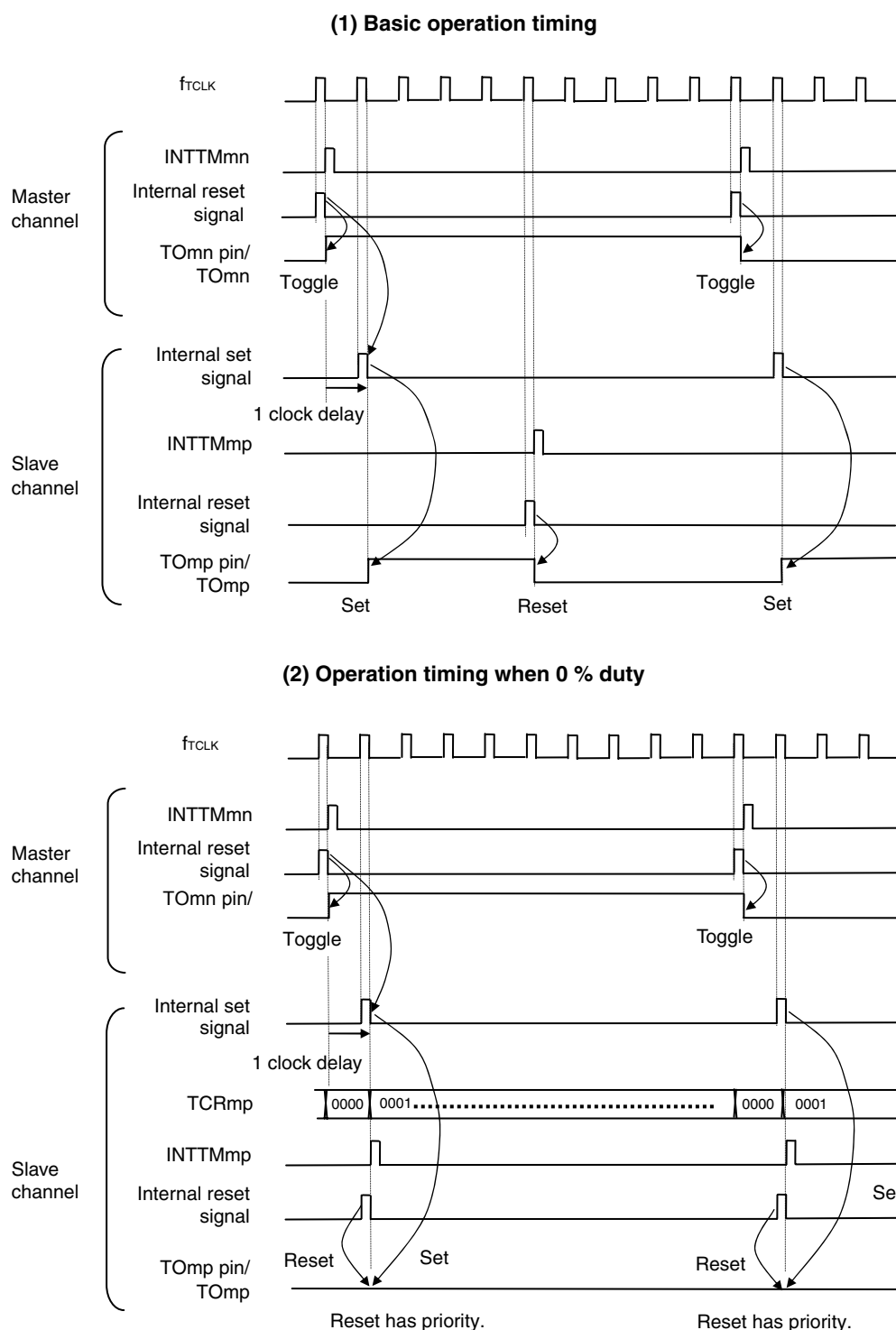
Figure 6-37 shows the set/reset operating statuses where the master/slave channels are set as follows.

Master channel: TOEmn = 1, TOMmn = 0, TOLmn = 0

Slave channel: TOEmp = 1, TOMmp = 1, TOLmp = 0

Remark m: Unit number (m = 0), n: Channel number (n = 0, 1, 3 to 7)

Figure 6-37. Set/Reset Timing Operating Statuses



Remarks 1. Internal reset signal: TOmn pin reset/toggle signal

Internal set signal: TOmn pin set signal

2. m: Unit number (m = 0)

n: Channel number

n = 0, 1, 3 to 7

p: Slave channel number

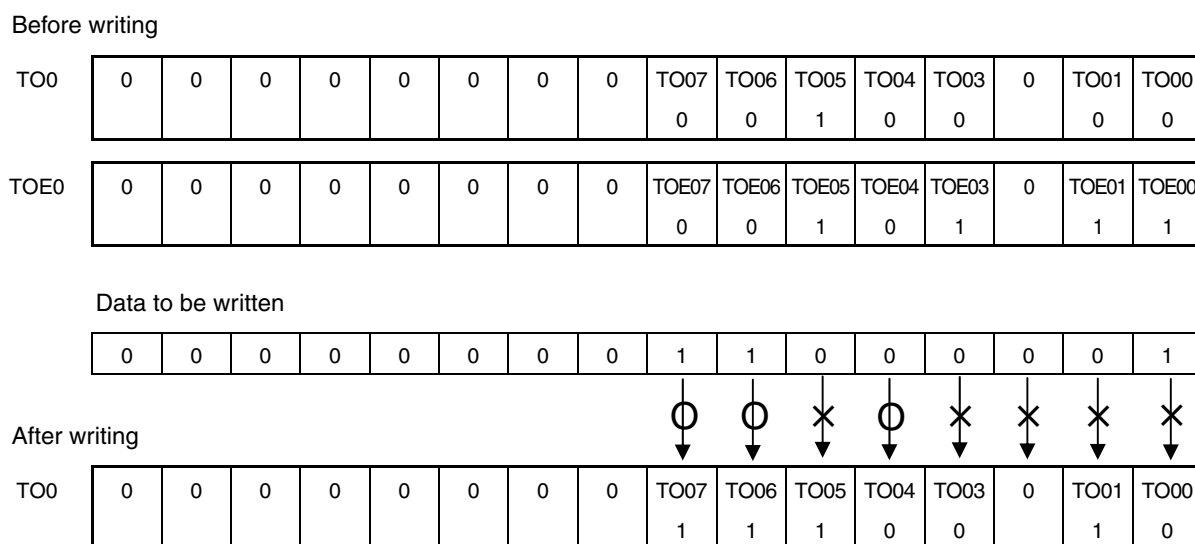
n < p ≤ 7

6.6.4 Collective manipulation of TOMn bit

In timer output register m (TOM), the setting bits for all the channels are located in one register in the same way as timer channel start register m (TSM). Therefore, the TOMn bit of all the channels can be manipulated collectively.

Only the desired bits can also be manipulated by enabling writing only to the TOMn bits (TOEmn = 0) that correspond to the relevant bits of the channel used to perform output (TOMn).

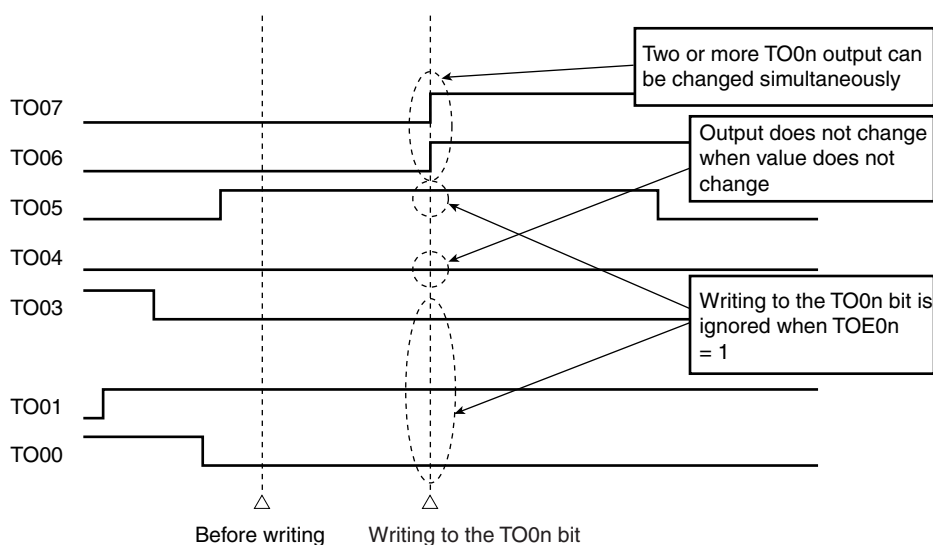
Figure 6-38 Example of TO0n Bit Collective Manipulation



Writing is done only to the TOMn bit with TOEmn = 0, and writing to the TOMn bit with TOEmn = 1 is ignored.

TOMn (channel output) to which TOEmn = 1 is set is not affected by the write operation. Even if the write operation is done to the TOMn bit, it is ignored and the output change by timer operation is normally done.

Figure 6-39. TO0n Pin Statuses by Collective Manipulation of TO0n Bit



(Caution and Remark are given on the next page.)

Caution While timer output is enabled ($TOEmn = 1$), even if the output by timer interrupt of each timer ($INTTMmn$) contends with writing to the $TOmn$ bit, output is normally done to the $TOmn$ pin.

Remark m: Unit number ($m = 0, 1$), n: Channel number ($n = 0, 1, 3$ to 7)

6.6.5 Timer Interrupt and $TOmn$ Pin Output at Operation Start

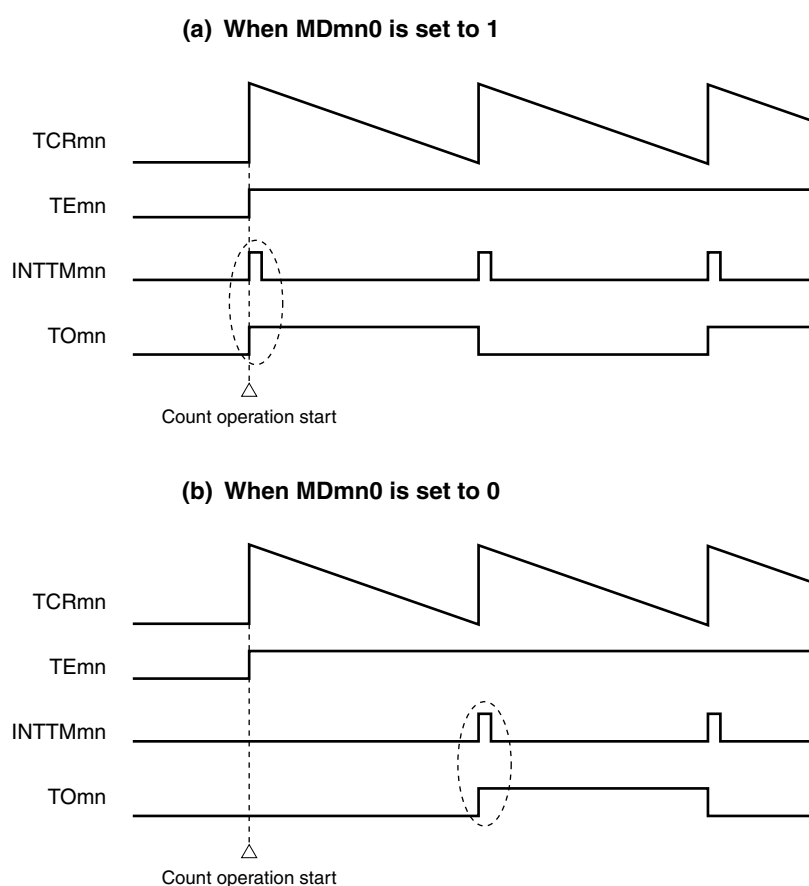
In the interval timer mode or capture mode, the $MDmn0$ bit in timer mode register mn ($TMRmn$) sets whether or not to generate a timer interrupt at count start.

When $MDmn0$ is set to 1, the count operation start timing can be known by the timer interrupt ($INTTMmn$) generation.

In the other modes, neither timer interrupt at count operation start nor $TOmn$ output is controlled.

Figure 6-40 shows operation examples when the interval timer mode ($TOEmn = 1$, $TOMmn = 0$) is set.

Figure 6-40. Operation examples of timer interrupt at count operation start and $TOmn$ output



When $MDmn0$ is set to 1, a timer interrupt ($INTTMmn$) is output at count operation start, and $TOmn$ performs a toggle operation.

When $MDmn0$ is set to 0, a timer interrupt ($INTTMmn$) is not output at count operation start, and $TOmn$ does not change either. After counting one cycle, $INTTMmn$ is output and $TOmn$ performs a toggle operation.

Remark m: Unit number ($m = 0$), n: Channel number ($n = 0, 1, 3$ to 7)

6.7 Independent Channel Operation Function of Timer Array Unit

6.7.1 Operation as interval timer/square wave output

(1) Interval timer

The timer array unit can be used as a reference timer that generates INTTMmn (timer interrupt) at fixed intervals. The interrupt generation period can be calculated by the following expression.

$\text{Generation period of INTTMmn (timer interrupt)} = \text{Period of count clock} \times (\text{Set value of TDRmn} + 1)$

(2) Operation as square wave output

TOMn performs a toggle operation as soon as INTTMmn has been generated, and outputs a square wave with a duty factor of 50%.

The period and frequency for outputting a square wave from TOMn can be calculated by the following expressions.

• Period of square wave output from TOMn = Period of count clock $\times$ (Set value of TDRmn + 1) $\times$ 2

• Frequency of square wave output from TOMn = Frequency of count clock / {(Set value of TDRmn + 1) $\times$ 2}

Timer count register mn (TCRmn) operates as a down counter in the interval timer mode.

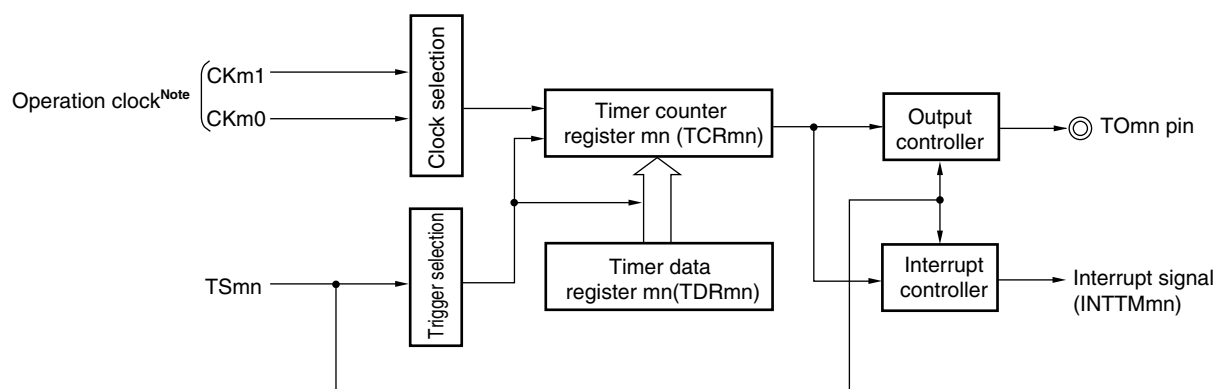
The TCRmn register loads the value of timer data register mn (TDRmn) at the first count clock after the channel start trigger bit (TSmn, TSHm1, TSHm3) of timer channel start register m (TSM) is set to 1. If the MDmn0 bit of timer mode register mn (TMRmn) is 0 at this time, INTTMmn is not output and TOMn is not toggled. If the MDmn0 bit of the TMRmn register is 1, INTTMmn is output and TOMn is toggled.

After that, the TCRmn register count down in synchronization with the count clock.

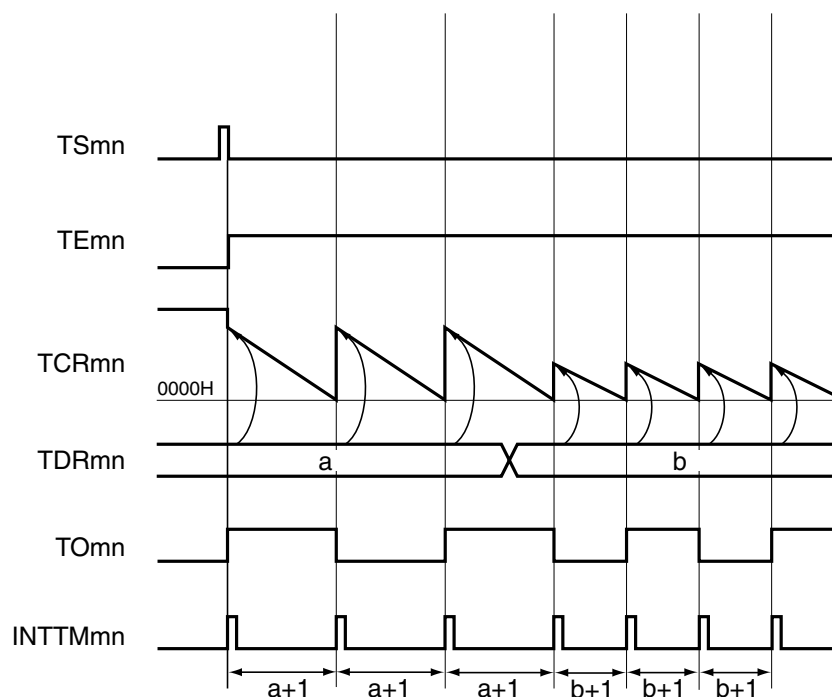
When TCRmn = 0000H, INTTMmn is output and TOMn is toggled at the next count clock. At the same time, the TCRmn register loads the value of the TDRmn register again. After that, the same operation is repeated.

The TDRmn register can be rewritten at any time. The new value of the TDRmn register becomes valid from the next period.

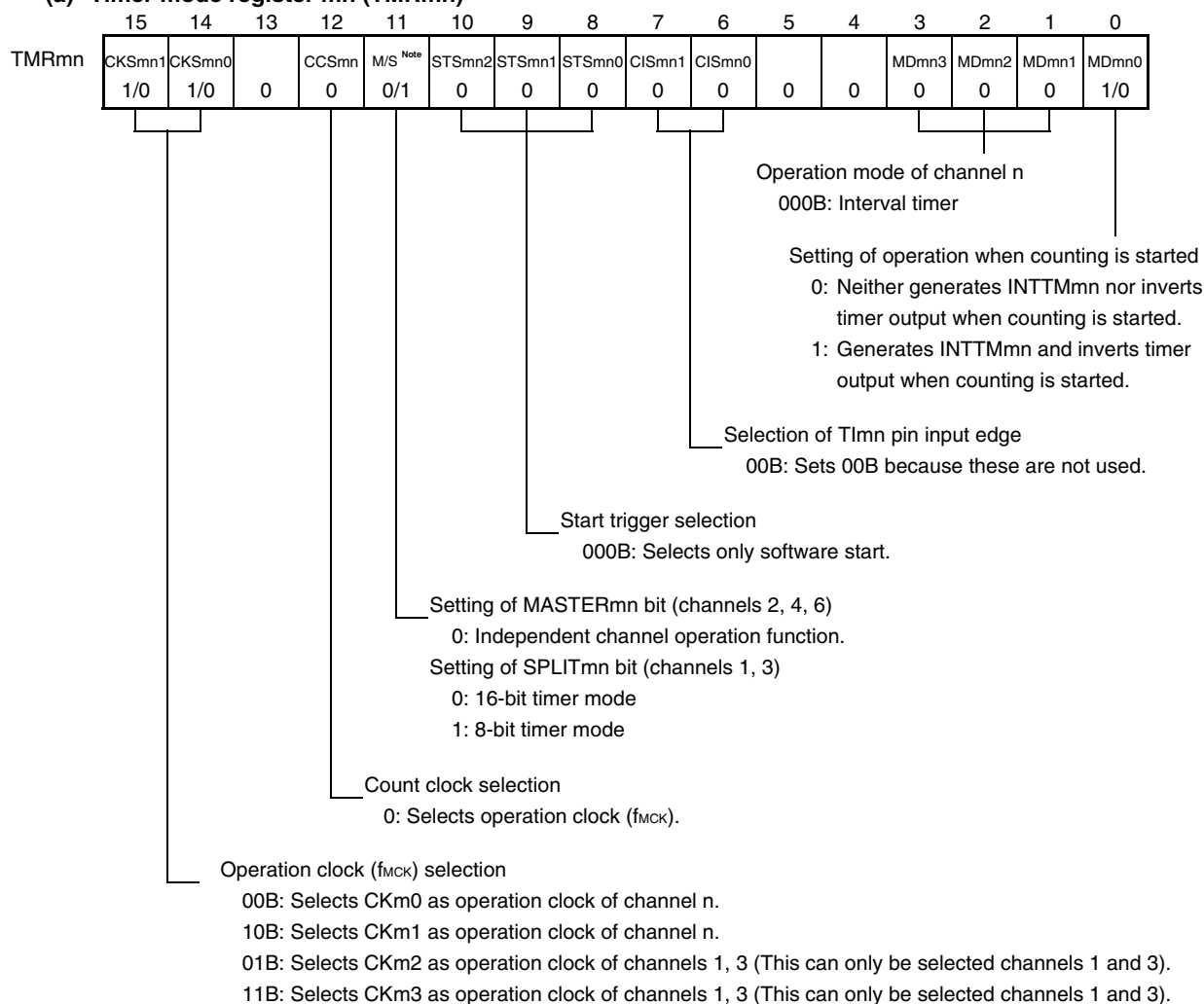
Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

Figure 6-41. Block Diagram of Operation as Interval Timer/Square Wave Output

Note When channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

Figure 6-42. Example of Basic Timing of Operation as Interval Timer/Square Wave Output (MDmn0 = 1)

- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))
 2. TSmn: Bit n of timer channel start register m (TSm)
 TEMn: Bit n of timer channel enable status register m (TEm)
 TCRmn: Timer count register mn (TCRmn)
 TDRmn: Timer data register mn (TDRmn)
 TOMn: TOMn pin output signal

Figure 6-43. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (1/2)**(a) Timer mode register mn (TMRmn)**

<R>

(b) Timer output register m (TOM)

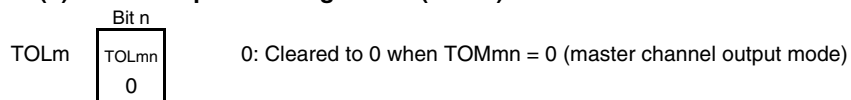
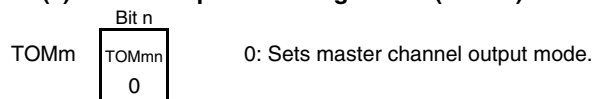
		Bit n
TOM	TOMn	0: Outputs 0 from TOMn.
	1/0	1: Outputs 1 from TOMn.

(c) Timer output enable register m (TOEm)

		Bit n
TOEm	TOEmn	0: Stops the TOMn output operation by counting operation.
	1/0	1: Enables the TOMn output operation by counting operation.

Note TMRm2, TMRm4, TMRm6: MASTERmn bit
 TMRm1, TMRm3: SPLITmn bit
 TMRm0, TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

Figure 6-43. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (2/2)**(d) Timer output level register m (TOLm)****(e) Timer output mode register m (TOMm)**

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

Figure 6-44. Operation Procedure of Interval Timer/Square Wave Output Function (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1.	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 to CKm3.	
Channel default setting	Sets timer mode register mn (TMRmn) (determines operation mode of channel). Sets interval (period) value to timer data register mn (TDRmn).	Channel stops operating. (Clock is supplied and some power is consumed.)
	To use the TOMn output Clears the TOMmn bit of timer output mode register m (TOMm) to 0 (master channel output mode). Clears the TOLmn bit to 0. Sets the TOMn bit and determines default level of the TOMn output.	The TOMn pin goes into Hi-Z output state.
	Sets the TOEmn bit to 1 and enables operation of TOMn. Clears the port register and port mode register to 0.	The TOMn default setting level is output when the port mode register is in the output mode and the port register is 0. TOMn does not change because channel stops operating. The TOMn pin outputs the TOMn set level.
Operation start	(Sets the TOEmn bit to 1 only if using TOMn output and resuming operation.). Sets the TSmn (TSHm1, TSHm3) bit to 1. The TSmn (TSHm1, TSHm3) bit automatically returns to 0 because it is a trigger bit.	TEmn (TEHm1, TEHm3) = 1, and count operation starts. Value of the TDRmn register is loaded to timer count register mn (TCRmn) at the count clock input. INTTMmn is generated and TOMn performs toggle operation if the MDmn0 bit of the TMRmn register is 1.
During operation	Set values of the TMRmn register, TOMmn, and TOLmn bits cannot be changed. Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TOM and TOEm registers can be changed.	Counter (TCRmn) counts down. When count value reaches 0000H, the value of the TDRmn register is loaded to the TCRmn register again and the count operation is continued. By detecting TCRmn = 0000H, INTTMmn is generated and TOMn performs toggle operation. After that, the above operation is repeated.
Operation stop	The TTmn (TTHm1, TTHm3) bit is set to 1. The TTmn (TTHm1, TTHm3) bit automatically returns to 0 because it is a trigger bit.	TEmn (TEHm1, TEHm3), and count operation stops. The TCRmn register holds count value and stops. The TOMn output is not initialized but holds current status.
	The TOEmn bit is cleared to 0 and value is set to the TOMn bit.	The TOMn pin outputs the TOMn bit set level.

(Remark is listed on the next page.)

Figure 6-44. Operation Procedure of Interval Timer/Square Wave Output Function (2/2)

	Software Operation	Hardware Status
TAU stop	To hold the TOMn pin output level Clears the TOMn bit to 0 after the value to be held is set to the port register. —————→	The TOMn pin output level is held by port function.
	When holding the TOMn pin output level is not necessary Setting not required. ----- The TAUmEN bit of the PER0 register is cleared to 0. —→	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOMn bit is cleared to 0 and the TOMn pin is set to port mode.)

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

6.7.2 Operation as external event counter

The timer array unit can be used as an external event counter that counts the number of times the valid input edge (external event) is detected in the TImn pin. When a specified count value is reached, the event counter generates an interrupt. The specified number of counts can be calculated by the following expression.

$$\text{Specified number of counts} = \text{Set value of TDRmn} + 1$$

Timer count register mn (TCRmn) operates as a down counter in the event counter mode.

The TCRmn register loads the value of timer data register mn (TDRmn) by setting any channel start trigger bit (TSMn, TSHm1, TSHm3) of timer channel start register m (TSM) to 1.

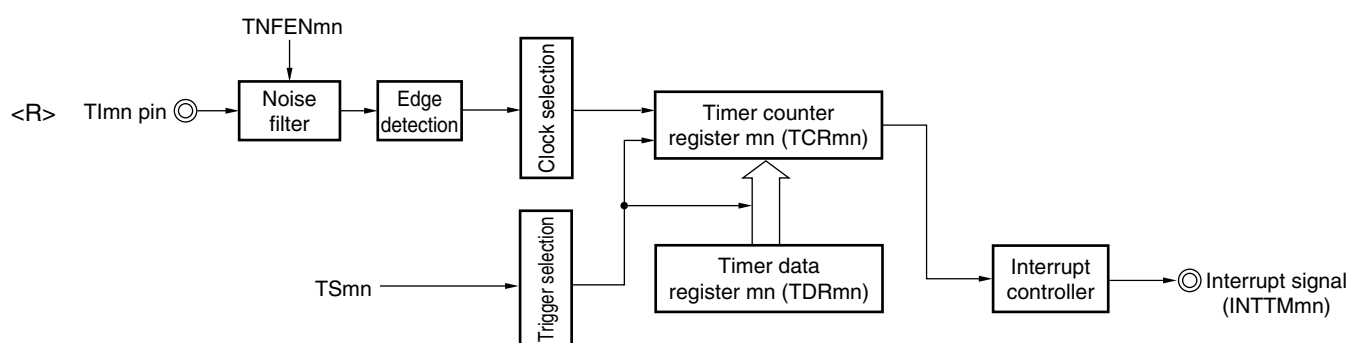
The TCRmn register counts down each time the valid input edge of the TImn pin has been detected. When TCRmn = 0000H, the TCRmn register loads the value of the TDRmn register again, and outputs INTTMmn.

After that, the above operation is repeated.

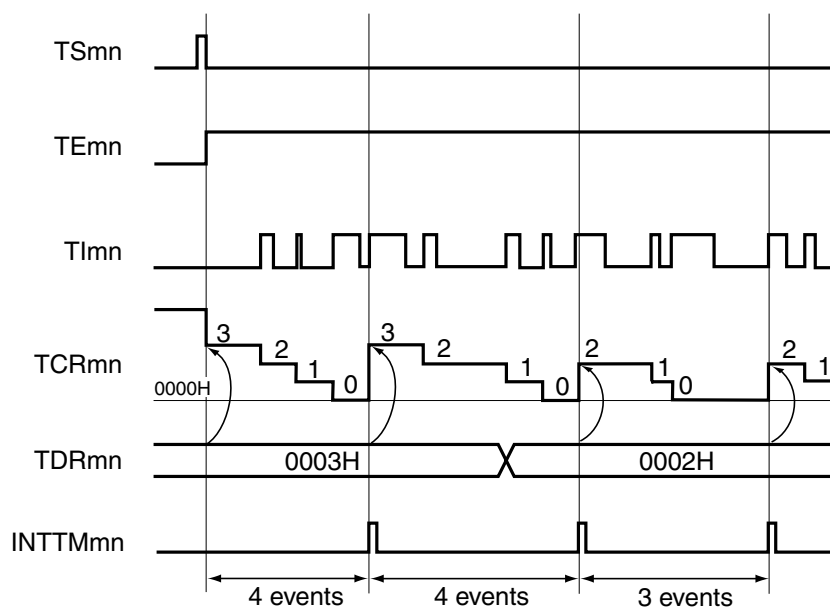
An irregular waveform that depends on external events is output from the TOmn pin. Stop the output by setting the TOEmn bit of timer output enable register m (TOEm) to 0.

The TDRmn register can be rewritten at any time. The new value of the TDRmn register becomes valid during the next count period.

Figure 6-45. Block Diagram of Operation as External Event Counter



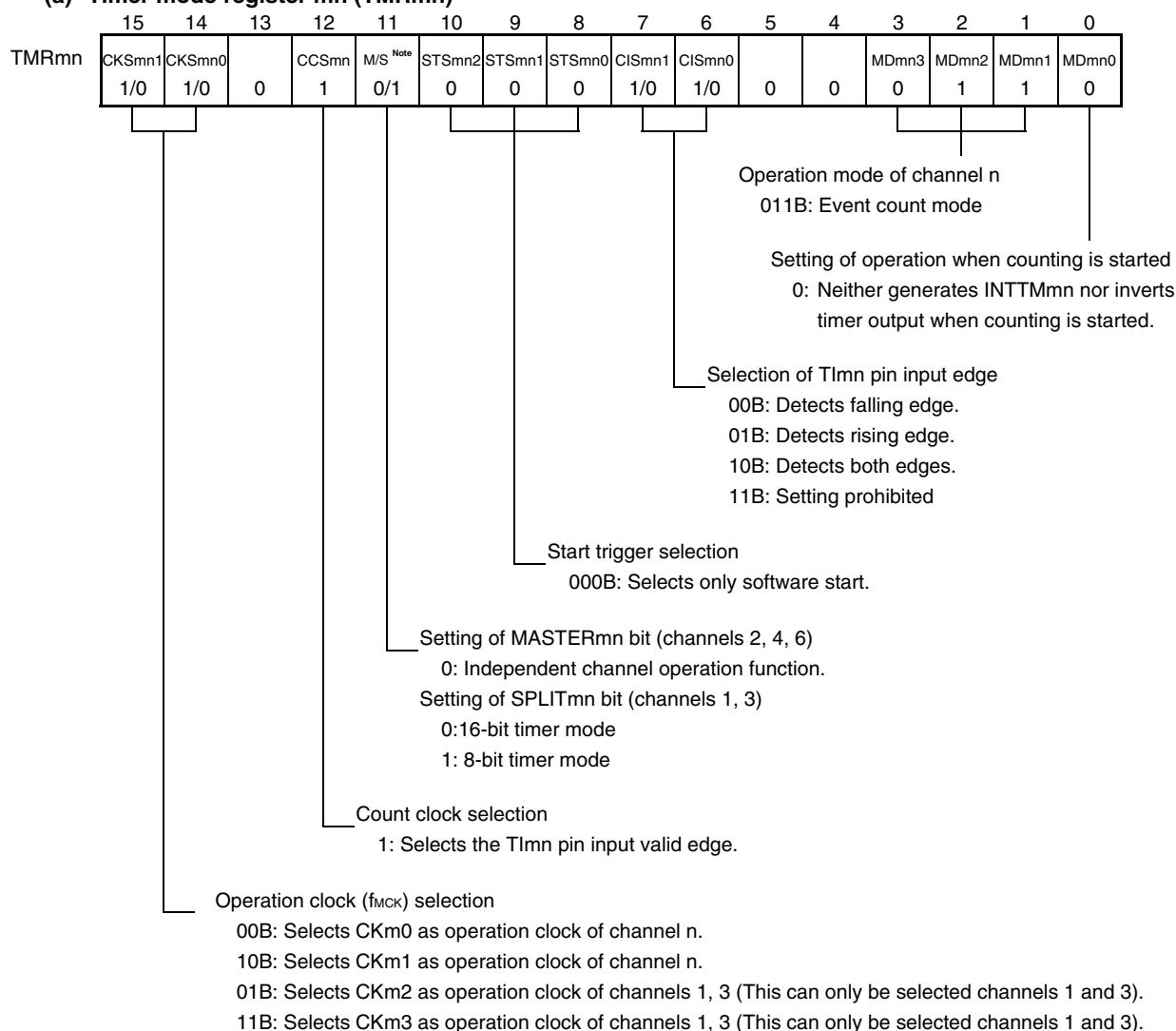
Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

Figure 6-46. Example of Basic Timing of Operation as External Event Counter

- Remarks 1.** m: Unit number ($m = 0$), n: Channel number ($n = 0$ to 7 (however, timer input pin (TImn), timer output pin (TOMn) : $n = 0, 1, 3$ to 7))
- 2.** TSmn: Bit n of timer channel start register m (TSM)
 TEmn: Bit n of timer channel enable status register m (TEM)
 TImn: TImn pin input signal
 TCRmn: Timer count register mn (TCRmn)
 TDRmn: Timer data register mn (TDRmn)

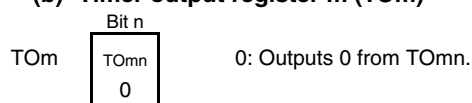
Figure 6-47. Example of Set Contents of Registers in External Event Counter Mode (1/2)

(a) Timer mode register mn (TMRmn)

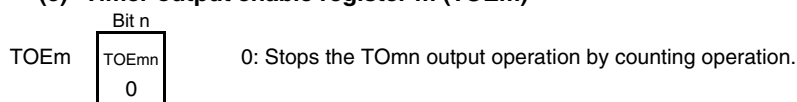


<R>

(b) Timer output register m (TOM)



(c) Timer output enable register m (TOEm)



Note TMRm2, TMRm4, TMRm6: MASTERmn bit
 TMRm1, TMRm3: SPLITmn bit
 TMRm0, TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

Figure 6-47. Example of Set Contents of Registers in External Event Counter Mode (2/2)**(d) Timer output level register m (TOLm)**

TOLm

Bit n
TOLmn
0

 0: Cleared to 0 when TOMmn = 0 (master channel output mode).

(e) Timer output mode register m (TOMm)

TOMm

Bit n
TOMmn
0

 0: Sets master channel output mode.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

<R>

Figure 6-48. Operation Procedure When External Event Counter Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1. —————→	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 to CKm3.	
Channel default setting	Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 0 (OFF) or 1 (ON). Sets timer mode register mn (TMRmn) (determines operation mode of channel). Sets number of counts to timer data register mn (TDRmn). Clears the TOEmn bit of timer output enable register m (TOEm) to 0.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. —————→ The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and count operation starts. Value of the TDRmn register is loaded to timer count register mn (TCRmn) and detection of the TImn pin input edge is awaited.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOMn, and TOEmn bits cannot be changed.	Counter (TCRmn) counts down each time input edge of the TImn pin has been detected. When count value reaches 0000H, the value of the TDRmn register is loaded to the TCRmn register again, and the count operation is continued. By detecting TCRmn = 0000H, the INTTMmn output is generated. After that, the above operation is repeated.
Operation stop	The TTmn bit is set to 1. —————→ The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops.
TAU stop	The TAUmEN bit of the PER0 register is cleared to 0. —————→	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

6.7.3 Operation as frequency divider (channel 0 of unit 0 only)

The timer array unit can be used as a frequency divider that divides a clock input to the TI00 pin and outputs the result from the TO00 pin.

The divided clock frequency output from TO00 can be calculated by the following expression.

- When rising edge/falling edge is selected:

$$\text{Divided clock frequency} = \text{Input clock frequency} / \{(\text{Set value of TDR00} + 1) \times 2\}$$
- When both edges are selected:

$$\text{Divided clock frequency} \equiv \text{Input clock frequency} / (\text{Set value of TDR00} + 1)$$

Timer count register 00 (TCR00) operates as a down counter in the interval timer mode.

After the channel start trigger bit (TS00) of timer channel start register 0 (TS0) is set to 1, the TCR00 register loads the value of timer data register 00 (TDR00) when the TI00 valid edge is detected.

If the MD000 bit of timer mode register 00 (TMR00) is 0 at this time, INTTM00 is not output and TO00 is not toggled. If the MD000 bit of timer mode register 00 (TMR00) is 1, INTTM00 is output and TO00 is toggled.

After that, the TCR00 register counts down at the valid edge of the TI00 pin. When TCR00 = 0000H, it toggles TO00. At the same time, the TCR00 register loads the value of the TDR00 register again, and continues counting.

If detection of both the edges of the TI00 pin is selected, the duty factor error of the input clock affects the divided clock period of the TO00 output.

The period of the TO00 output clock includes a sampling error of one period of the operation clock.

$$\text{Clock period of TO00 output} = \text{Ideal TO00 output clock period} \pm \text{Operation clock period (error)}$$

The TDR00 register can be rewritten at any time. The new value of the TDR00 register becomes valid during the next count period.

Figure 6-49. Block Diagram of Operation as Frequency Divider

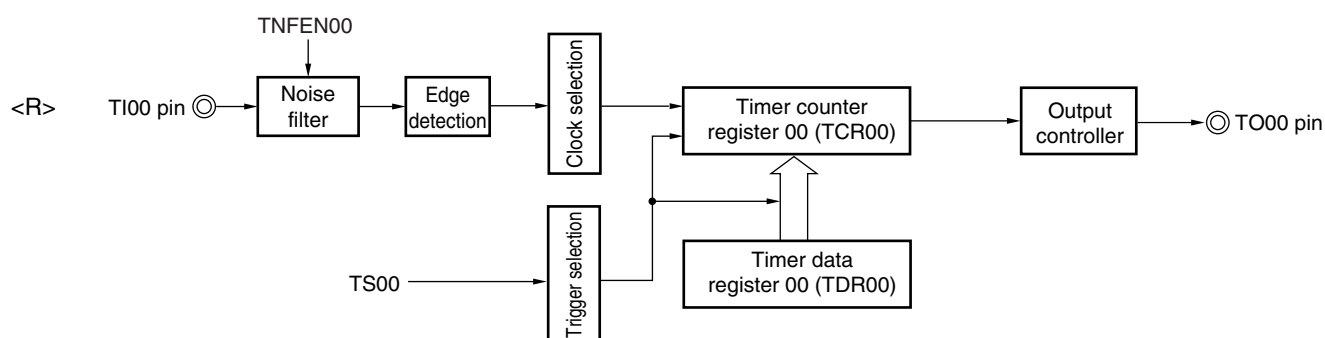
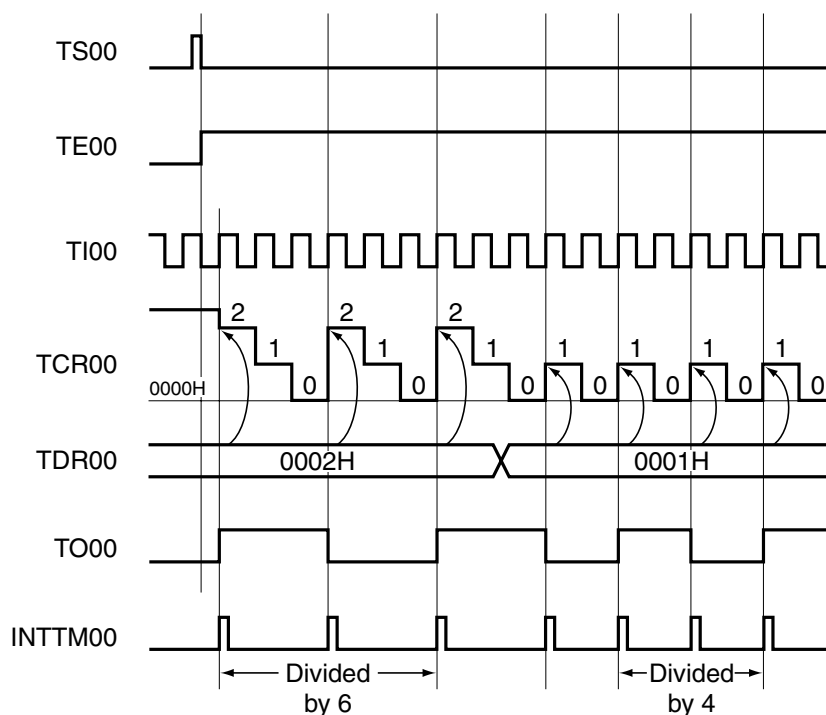
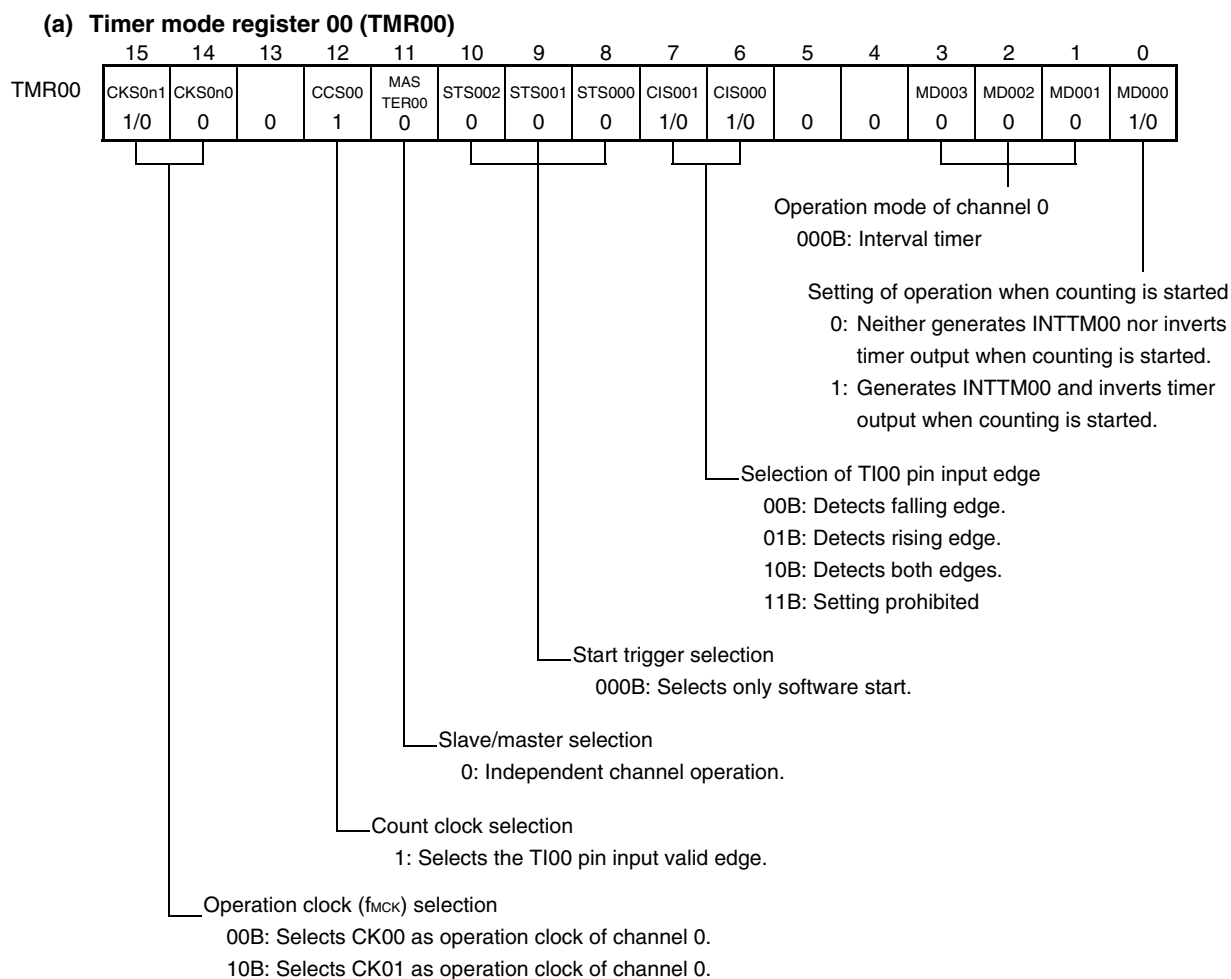


Figure 6-50. Example of Basic Timing of Operation as Frequency Divider (MD000 = 1)

- Remark**
- TS00: Bit n of timer channel start register 0 (TS0)
 - TE00: Bit n of timer channel enable status register 0 (TE0)
 - TI00: TI00 pin input signal
 - TCR00: Timer count register 00 (TCR00)
 - TDR00: Timer data register 00 (TDR00)
 - TO00: TO00 pin output signal

Figure 6-51. Example of Set Contents of Registers During Operation as Frequency Divider

**(b) Timer output register 0 (TO0)**

Bit 0	
TO0	TO00
	1/0
	0: Outputs 0 from TO00.
	1: Outputs 1 from TO00.

(c) Timer output enable register 0 (TOE0)

Bit 0	
TOE0	TOE00
	1/0
	0: Stops the TO00 output operation by counting operation.
	1: Enables the TO00 output operation by counting operation.

(d) Timer output level register 0 (TOL0)

Bit 0	
TOL0	TOL00
	0
	0: Cleared to 0 when TOM00 = 0 (master channel output mode)

(e) Timer output mode register 0 (TOM0)

Bit 0	
TOM0	TOM00
	0
	0: Sets master channel output mode.

<R>

Figure 6-52. Operation Procedure When Frequency Divider Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN bit of peripheral enable register 0 (PER0) to 1.	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register 0 (TPS0). Determines clock frequencies of CK00 to CK03.	
Channel default setting	Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 0 (OFF) or 1 (ON). Sets timer mode register 0n (TMR0n) (determines operation mode of channel and selects the detection edge). Sets interval (period) value to timer data register 00 (TDR00).	Channel stops operating. (Clock is supplied and some power is consumed.)
	Clears the TOM00 bit of timer output mode register 0 (TOM0) to 0 (master channel output mode). Clears the TOL00 bit to 0. Sets the TO00 bit and determines default level of the TO00 output.	The TO00 pin goes into Hi-Z output state.
	Sets the TOE00 bit to 1 and enables operation of TO00.	The TO00 default setting level is output when the port mode register is in output mode and the port register is 0.
	Clears the port register and port mode register to 0.	TO00 does not change because channel stops operating. The TO00 pin outputs the TO00 set level.
Operation start	Sets the TOE00 bit to 1 (only when operation is resumed). Sets the TS00 bit to 1. The TS00 bit automatically returns to 0 because it is a trigger bit.	TE00 = 1, and count operation starts. Value of the TDR00 register is loaded to timer count register 00 (TCR00) at the count clock input. INTTM00 is generated and TO00 performs toggle operation if the MD000 bit of the TMR00 register is 1.
During operation	Set value of the TDR00 register can be changed. The TCR00 register can always be read. The TSR00 register is not used. Set values of the TO0 and TOE0 registers can be changed. Set values of the TMR00 register, TOM00, and TOL00 bits cannot be changed.	Counter (TCR00) counts down. When count value reaches 0000H, the value of the TDR00 register is loaded to the TCR00 register again, and the count operation is continued. By detecting TCR00 = 0000H, INTTM00 is generated and TO00 performs toggle operation. After that, the above operation is repeated.
Operation stop	The TT00 bit is set to 1. The TT00 bit automatically returns to 0 because it is a trigger bit.	TE00 = 0, and count operation stops. The TCR00 register holds count value and stops. The TO00 output is not initialized but holds current status.
	The TOE00 bit is cleared to 0 and value is set to the TO00 bit.	The TO00 pin outputs the TO00 set level.
TAU stop	To hold the TO00 pin output level Clears the TO00 bit to 0 after the value to be held is set to the port register. When holding the TO00 pin output level is not necessary Setting not required.	The TO00 pin output level is held by port function.
	The TAU0EN bit of the PER0 register is cleared to 0.	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TO00 bit is cleared to 0 and the TO00 pin is set to port mode).

Operation is resumed.

6.7.4 Operation as input pulse interval measurement

The count value can be captured at the Tl_{mn} valid edge and the interval of the pulse input to Tl_{mn} can be measured. The pulse interval can be calculated by the following expression.

$$\text{Tl}_{mn} \text{ input pulse interval} = \text{Period of count clock} \times ((10000\text{H} \times \text{TSR}_{mn}:\text{OVF}) + (\text{Capture value of TDR}_{mn} + 1))$$

Caution The Tl_{mn} pin input is sampled using the operating clock selected with the CKS_{mn} bit of timer mode register mn (TMR_{mn}), so an error of up to one operating clock cycle occurs.

Timer count register mn (TCR_{mn}) operates as an up counter in the capture mode.

When the channel start trigger bit (TS_{mn}) of timer channel start register m (TS_m) is set to 1, the TCR_{mn} register counts up from 0000H in synchronization with the count clock.

When the Tl_{mn} pin input valid edge is detected, the count value of the TCR_{mn} register is transferred (captured) to timer data register mn (TDR_{mn}) and, at the same time, the TCR_{mn} register is cleared to 0000H, and the INTT_{mn} is output. If the counter overflows at this time, the OVF bit of timer status register mn (TSR_{mn}) is set to 1. If the counter does not overflow, the OVF bit is cleared. After that, the above operation is repeated.

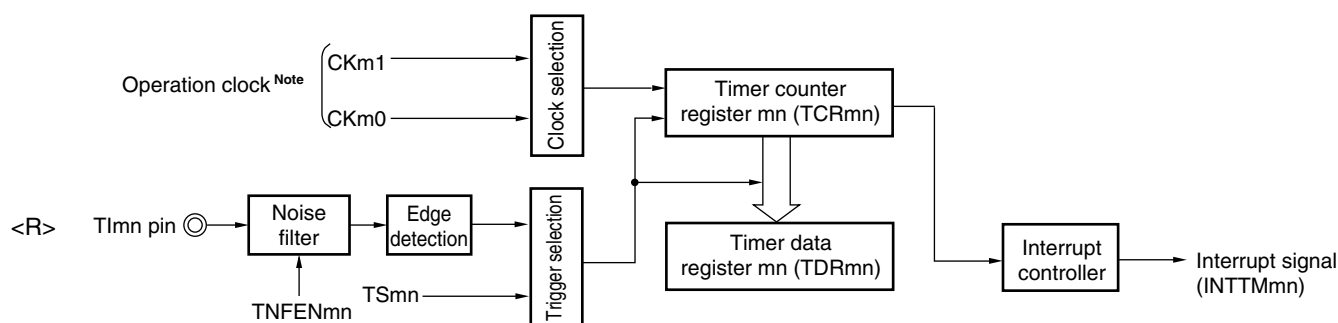
As soon as the count value has been captured to the TDR_{mn} register, the OVF bit of the TSR_{mn} register is updated depending on whether the counter overflows during the measurement period. Therefore, the overflow status of the captured value can be checked.

If the counter reaches a full count for two or more periods, it is judged to be an overflow occurrence, and the OVF bit of the TSR_{mn} register is set to 1. However, a normal interval value cannot be measured for the OVF bit, if two or more overflows occur.

Set the STS_{mn}2 to STS_{mn}0 bits of the TMR_{mn} register to 001B to use the valid edges of Tl_{mn} as a start trigger and a capture trigger.

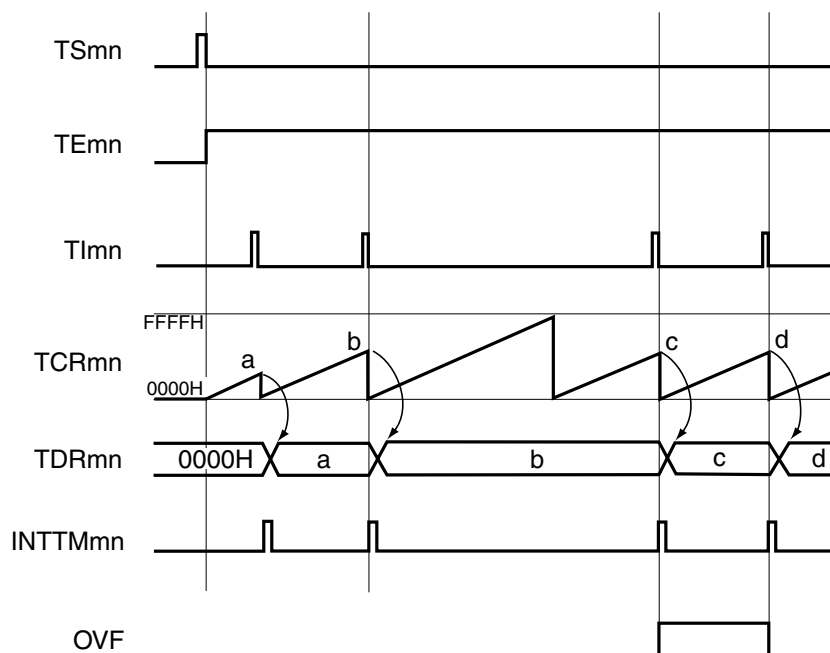
When TE_{mn} = 1, a software operation (TS_{mn} = 1) can be used as a capture trigger, instead of using the Tl_{mn} pin input.

Figure 6-53. Block Diagram of Operation as Input Pulse Interval Measurement



Note When channels 1 and 3, the clock can be selected from CK_{m0}, CK_{m1}, CK_{m2} and CK_{m3}.

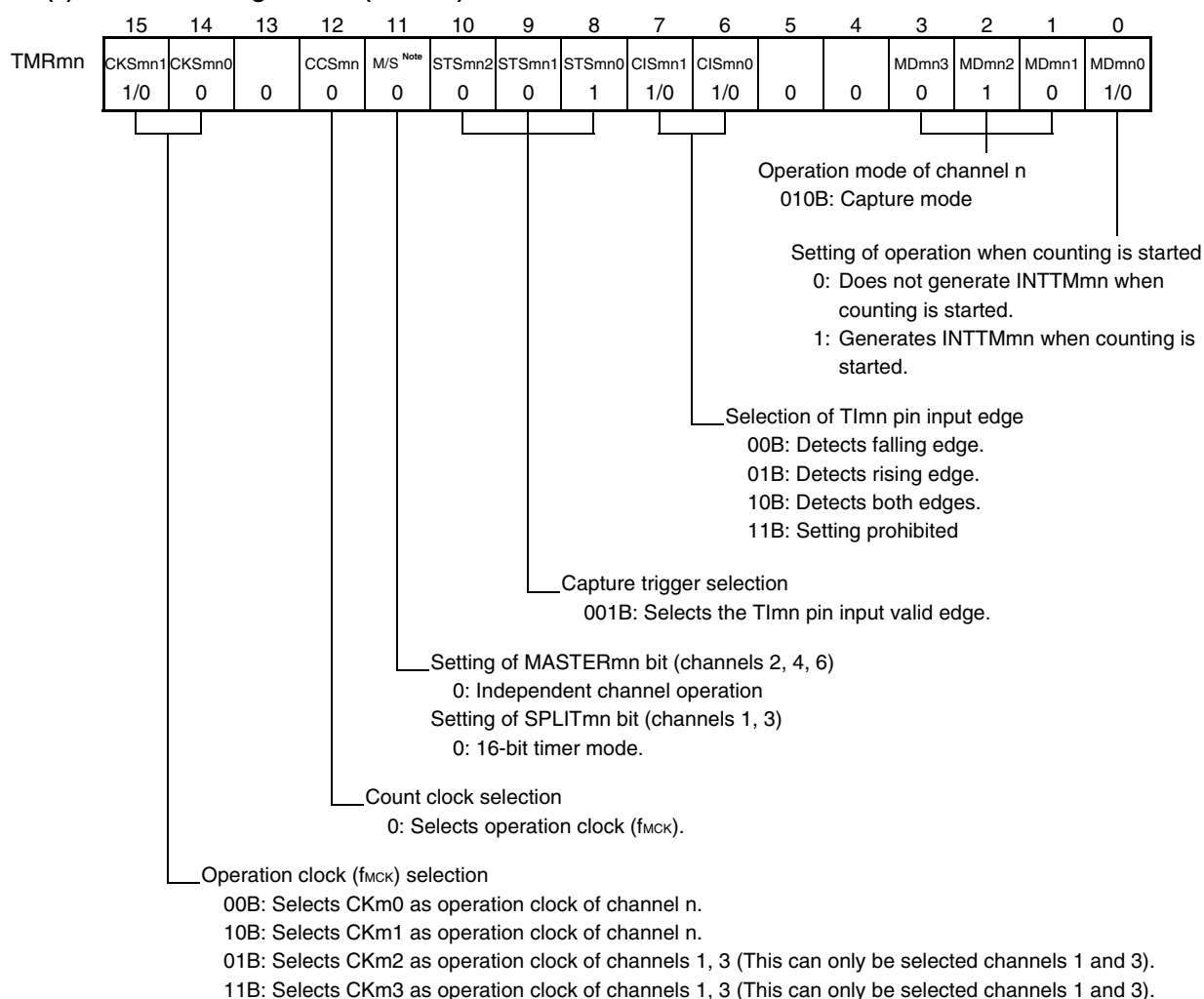
Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (Tl_{mn}), timer output pin (TO_{mn}) : n = 0, 1, 3 to 7))

Figure 6-54. Example of Basic Timing of Operation as Input Pulse Interval Measurement (MDmn0 = 0)

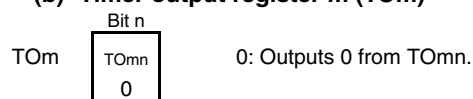
- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))
 2. TSmn: Bit n of timer channel start register m (TSm)
 TE mn: Bit n of timer channel enable status register m (TEm)
 TImn: TImn pin input signal
 TCRmn: Timer count register mn (TCRmn)
 TDRmn: Timer data register mn (TDRmn)
 OVf: Bit 0 of timer status register mn (TSRmn)

Figure 6-55. Example of Set Contents of Registers to Measure Input Pulse Interval

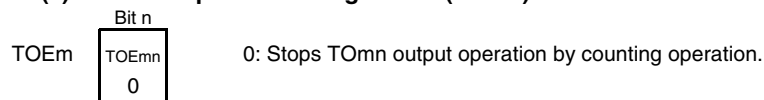
(a) Timer mode register mn (TMRmn)



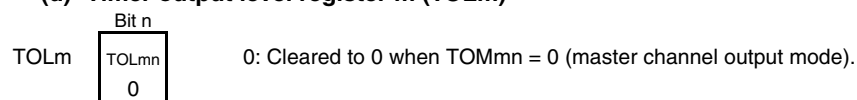
(b) Timer output register m (TOM)



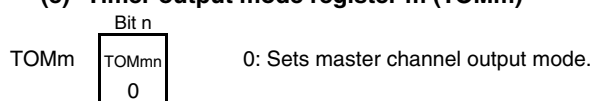
(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)



Note TMRm2, TMRm4, TMRm6: MASTERmn bit
 TMRm1, TMRm3: SPLITmn bit
 TMRm0, TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

<R> **Figure 6-56. Operation Procedure When Input Pulse Interval Measurement Function Is Used**

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1.	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 to CKm3.	
Channel default setting	Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 0 (OFF) or 1 (ON). Sets timer mode register mn (TMRmn) (determines operation mode of channel).	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets TSmn bit to 1. The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and count operation starts. Timer count register mn (TCRmn) is cleared to 0000H at the count clock input. When the MDmn0 bit of the TMRmn register is 1, INTTMmn is generated.
During operation	Set values of only the CISmn1 and CISmn0 bits of the TMRmn register can be changed. The TDRmn register can always be read. The TCRmn register can always be read. The TSRmn register can always be read. Set values of the TOMmn, TOLmn, TOMn, and TOEmn bits cannot be changed.	Counter (TCRmn) counts up from 0000H. When the TImn pin input valid edge is detected, the count value is transferred (captured) to timer data register mn (TDRmn). At the same time, the TCRmn register is cleared to 0000H, and the INTTMmn signal is generated. If an overflow occurs at this time, the OVF bit of timer status register mn (TSRmn) is set; if an overflow does not occur, the OVF bit is cleared. After that, the above operation is repeated.
Operation stop	The TTmn bit is set to 1. The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops. The OVF bit of the TSRmn register is also held.
TAU stop	The TAUmEN bit of the PER0 register is cleared to 0.	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

6.7.5 Operation as input signal high-/low-level width measurement

Caution When using a channel to implement the LIN-bus, set bit 1 (ISC1) of the input switch control register (ISC) to 1. In the following descriptions, read TImn as RxD2.

By starting counting at one edge of the TImn pin input and capturing the number of counts at another edge, the signal width (high-level width/low-level width) of TImn can be measured. The signal width of TImn can be calculated by the following expression.

$$\text{Signal width of TImn input} = \text{Period of count clock} \times ((10000\text{H} \times \text{TSRmn: OVF}) + (\text{Capture value of TDRmn} + 1))$$

Caution The TImn pin input is sampled using the operating clock selected with the CKSmn bit of timer mode register mn (TMRmn), so an error equivalent to one operation clock occurs.

Timer count register mn (TCRmn) operates as an up counter in the capture & one-count mode.

When the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, the TEmn bit is set to 1 and the TImn pin start edge detection wait status is set.

When the TImn pin input start edge (rising edge of the TImn pin input when the high-level width is to be measured) is detected, the counter counts up from 0000H in synchronization with the count clock. When the valid capture edge (falling edge of the TImn pin input when the high-level width is to be measured) is detected later, the count value is transferred to timer data register mn (TDRmn) and, at the same time, INTTMmn is output. If the counter overflows at this time, the OVF bit of timer status register mn (TSRmn) is set to 1. If the counter does not overflow, the OVF bit is cleared. The TCRmn register stops at the value "value transferred to the TDRmn register + 1", and the TImn pin start edge detection wait status is set. After that, the above operation is repeated.

As soon as the count value has been captured to the TDRmn register, the OVF bit of the TSRmn register is updated depending on whether the counter overflows during the measurement period. Therefore, the overflow status of the captured value can be checked.

If the counter reaches a full count for two or more periods, it is judged to be an overflow occurrence, and the OVF bit of the TSRmn register is set to 1. However, a normal interval value cannot be measured for the OVF bit, if two or more overflows occur.

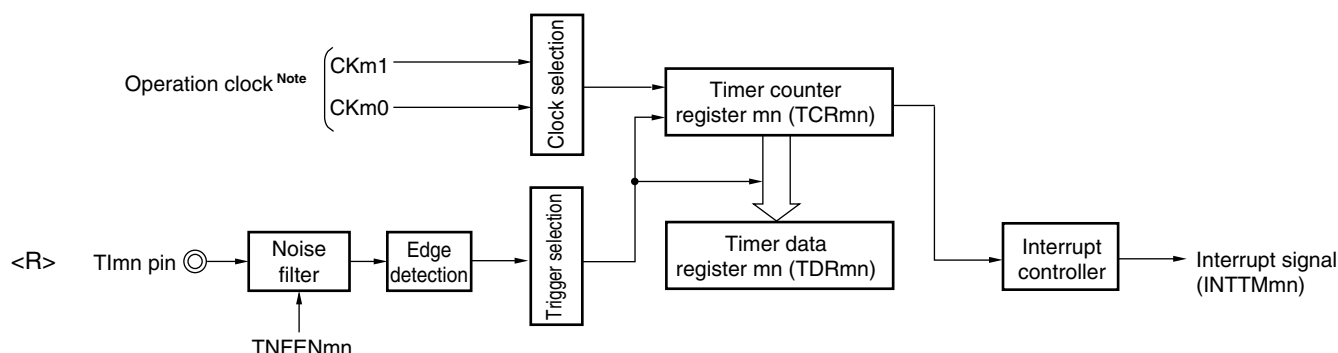
Whether the high-level width or low-level width of the TImn pin is to be measured can be selected by using the CISmn1 and CISmn0 bits of the TMRmn register.

Because this function is used to measure the signal width of the TImn pin input, the TSmn bit cannot be set to 1 while the TEmn bit is 1.

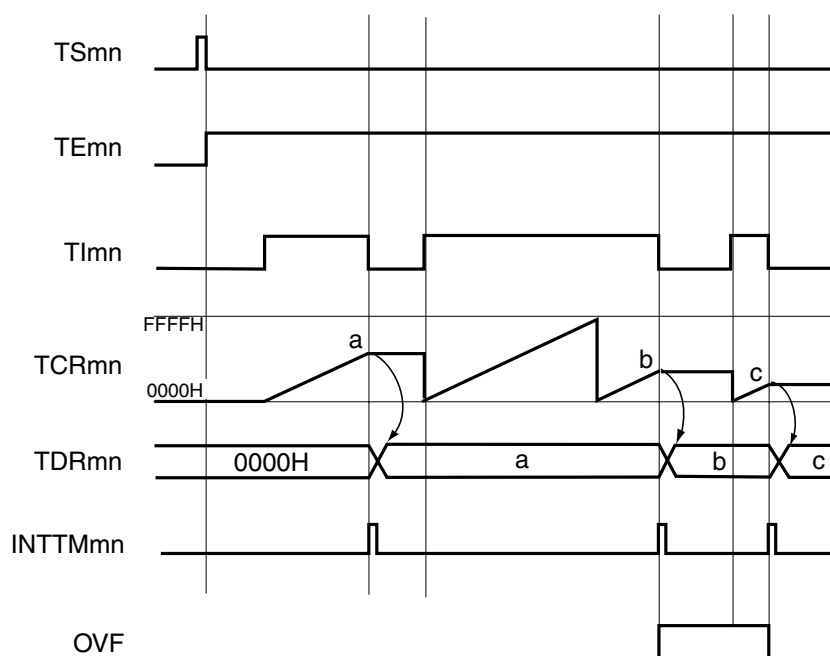
CISmn1, CISmn0 of TMRmn register = 10B: Low-level width is measured.

CISmn1, CISmn0 of TMRmn register = 11B: High-level width is measured.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

Figure 6-57. Block Diagram of Operation as Input Signal High-/Low-Level Width Measurement

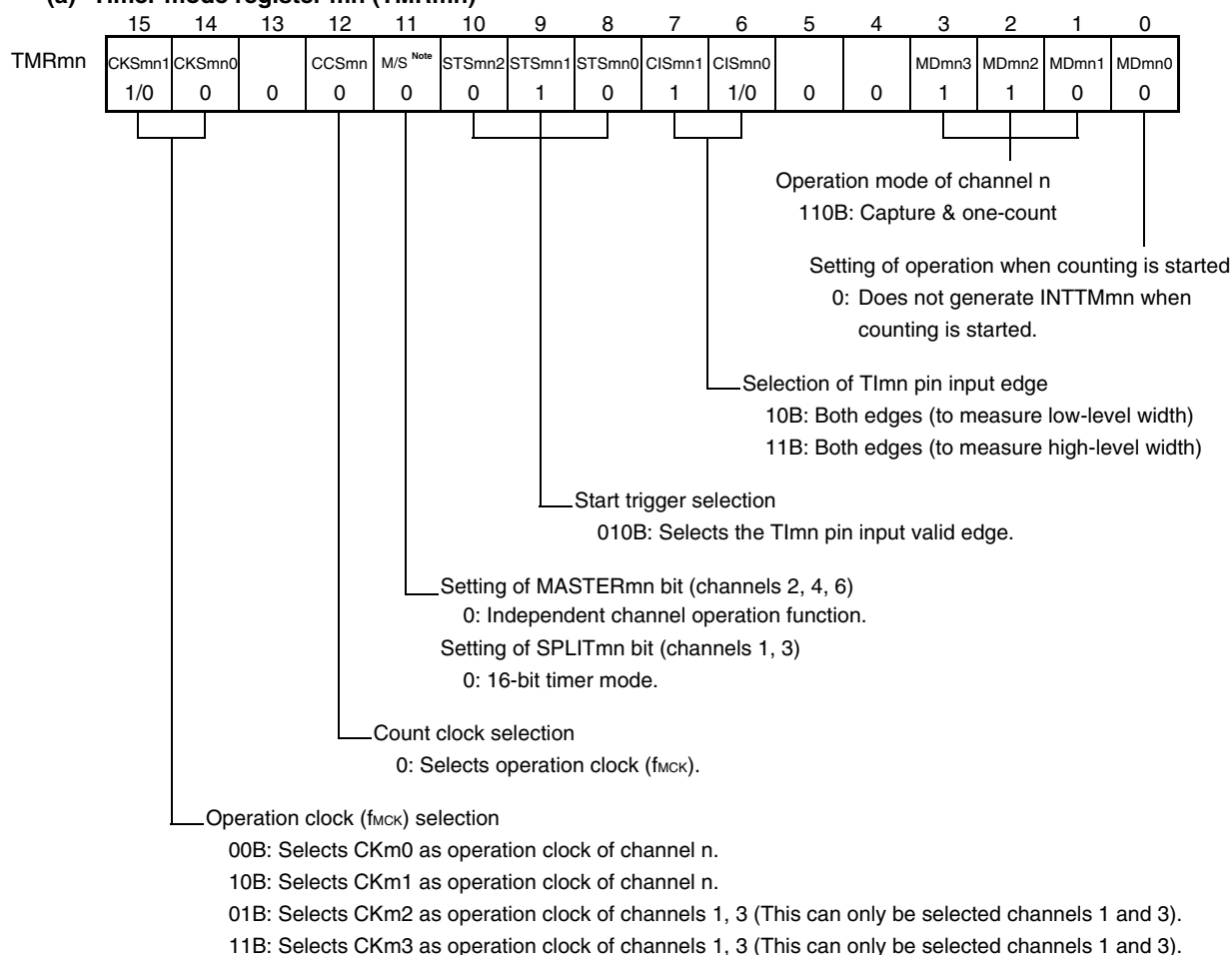
Note For channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

Figure 6-58. Example of Basic Timing of Operation as Input Signal High-/Low-Level Width Measurement

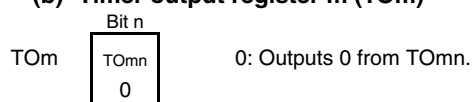
- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))
 2. TSmn: Bit n of timer channel start register m (TSM)
 - TE mn: Bit n of timer channel enable status register m (TEM)
 - TImn: TImn pin input signal
 - TCRmn: Timer count register mn (TCRmn)
 - TDRmn: Timer data register mn (TDRmn)
 - OVF: Bit 0 of timer status register mn (TSRmn)

<R> **Figure 6-59. Example of Set Contents of Registers to Measure Input Signal High-/Low-Level Width**

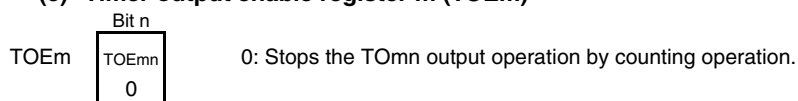
(a) Timer mode register mn (TMRmn)



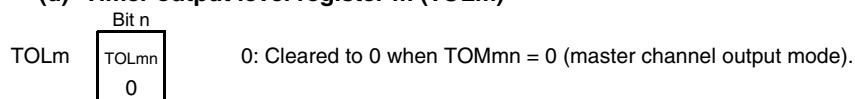
(b) Timer output register m (TOM)



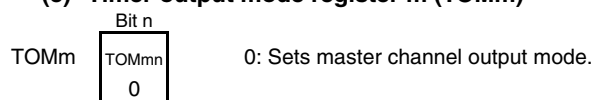
(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)



Note TMRm2, TMRm4, TMRm6: MASTERmn bit

TMRm1, TMRm3: SPLITmn bit

TMRm0, TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

<R> **Figure 6-60. Operation Procedure When Input Signal High-/Low-Level Width Measurement Function Is Used**

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1.	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 to CKm3.	
Channel default setting	Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 0 (OFF) or 1 (ON). Sets timer mode register mn (TMRmn) (determines operation mode of channel). Clears the TOEmn bit to 0 and stops operation of TOMn.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and the TImn pin start edge detection wait status is set.
	Detects the TImn pin input count start valid edge.	Clears timer count register mn (TCRmn) to 0000H and starts counting up.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOMn, and TOEmn bits cannot be changed.	When the TImn pin start edge is detected, the counter (TCRmn) counts up from 0000H. If a capture edge of the TImn pin is detected, the count value is transferred to timer data register mn (TDRmn) and INTTMmn is generated. If an overflow occurs at this time, the OVF bit of timer status register mn (TSRmn) is set; if an overflow does not occur, the OVF bit is cleared. The TCRmn register stops the count operation until the next TImn pin start edge is detected.
Operation stop	The TTmn bit is set to 1. The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops. The OVF bit of the TSRmn register is also held.
TAU stop	The TAUmEN bit of the PER0 register is cleared to 0.	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

6.7.6 Operation as delay counter

It is possible to start counting down when the valid edge of the TImn pin input is detected (an external event), and then generate INTTMmn (a timer interrupt) after any specified interval.

It can also generate INTTMmn (timer interrupt) at any interval by making a software set TSmn = 1 and the count down start during the period of TEMn = 1.

The interrupt generation period can be calculated by the following expression.

$$\text{Generation period of INTTMmn (timer interrupt)} = \text{Period of count clock} \times (\text{Set value of TDRmn} + 1)$$

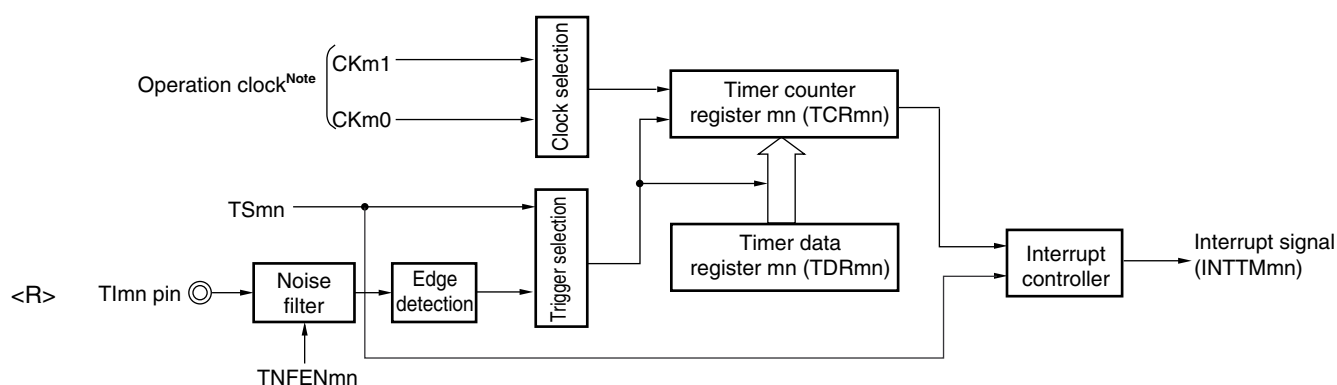
Timer count register mn (TCRmn) operates as a down counter in the one-count mode.

When the channel start trigger bit (TSmn, TSHm1, TSHm3) of timer channel start register m (TSM) is set to 1, the TEMn, TEHm1, TEHm3 bits are set to 1 and the TImn pin input valid edge detection wait status is set.

Timer count register mn (TCRmn) starts operating upon TImn pin input valid edge detection and loads the value of timer data register mn (TDRmn). The TCRmn register counts down from the value of the TDRmn register it has loaded, in synchronization with the count clock. When TCRmn = 0000H, it outputs INTTMmn and stops counting until the next TImn pin input valid edge is detected.

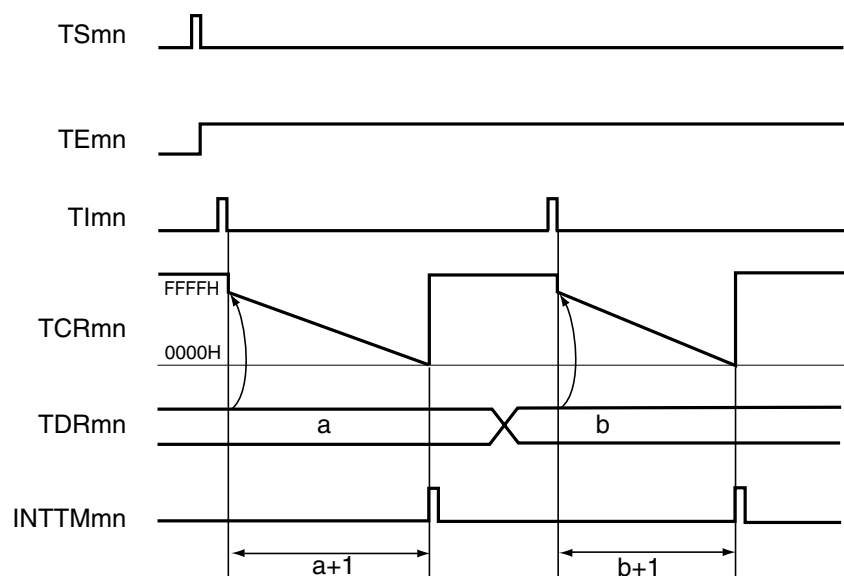
The TDRmn register can be rewritten at any time. The new value of the TDRmn register becomes valid from the next period.

Figure 6-61. Block Diagram of Operation as Delay Counter



Note For using channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

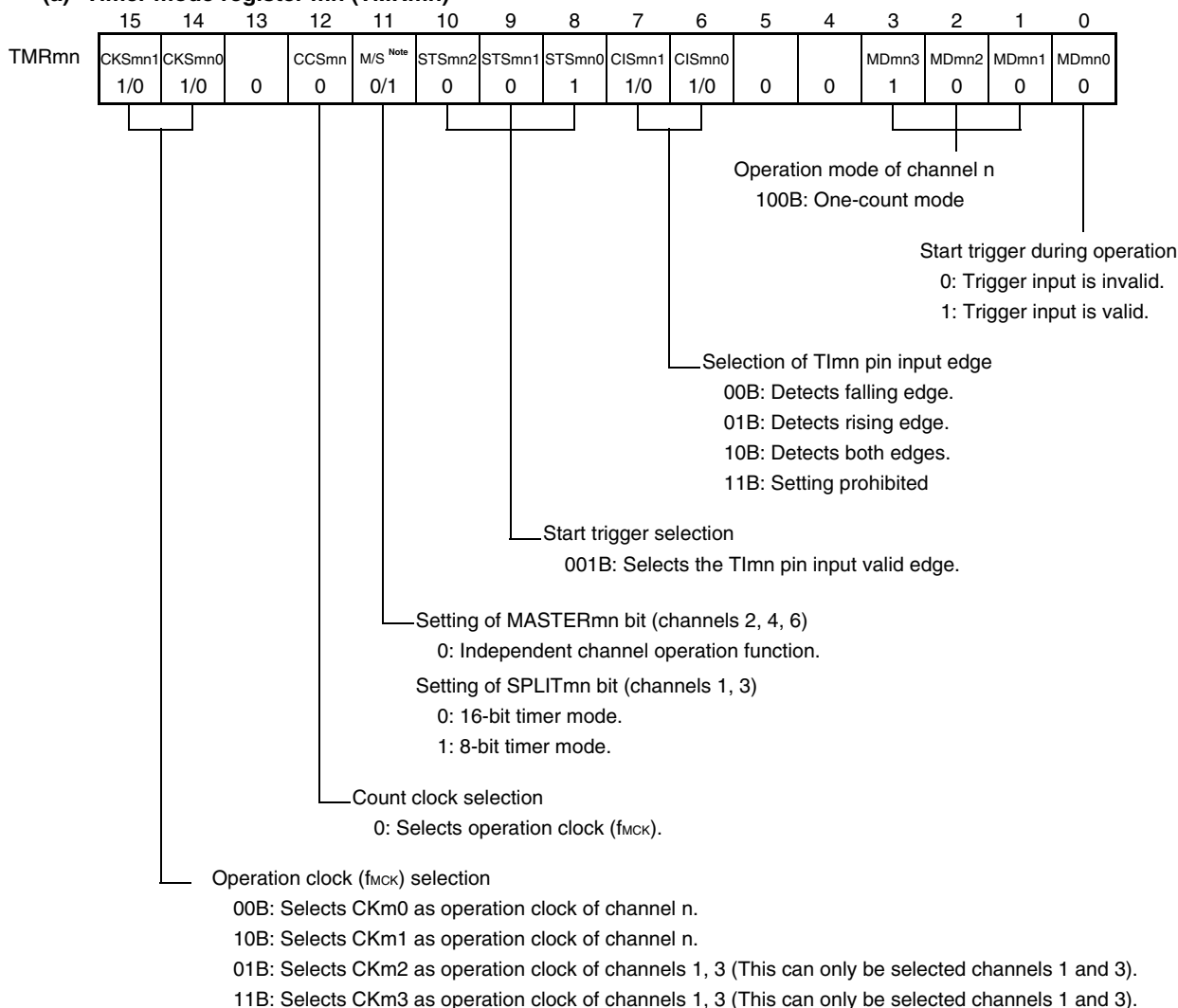
Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOMn) : n = 0, 1, 3 to 7))

Figure 6-62. Example of Basic Timing of Operation as Delay Counter

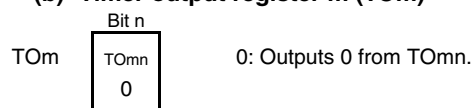
- Remarks 1.** m: Unit number ($m = 0$), n: Channel number ($n = 0$ to 7 (however, timer input pin (TImn), timer output pin (TOMn) : $n = 0, 1, 3$ to 7))
- 2.** TSmn: Bit n of timer channel start register m (TSm)
 TE mn: Bit n of timer channel enable status register m (TEm)
 TImn: TImn pin input signal
 TCRmn: Timer count register mn (TCRmn)
 TDRmn: Timer data register mn (TDRmn)

Figure 6-63. Example of Set Contents of Registers to Delay Counter (1/2)

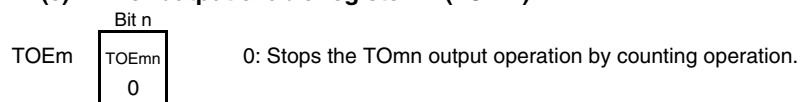
(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOM)



(c) Timer output enable register m (TOEm)



Note TMRm2, TMRm4, TMRm6: MASTERmn bit
 TMRm1, TMRm3: SPLITmn bit
 TMRm0, TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

Figure 6-63. Example of Set Contents of Registers to Delay Counter (2/2)**(d) Timer output level register m (TOLm)**

TOLm

Bit n
TOLmn
0

 0: Cleared to 0 when TOMmn = 0 (master channel output mode).

(e) Timer output mode register m (TOMm)

TOMm

Bit n
TOMmn
0

 0: Sets master channel output mode.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn) : n = 0, 1, 3 to 7))

<R>

Figure 6-64. Operation Procedure When Delay Counter Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1.	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 to CKm3.	
Channel default setting	Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 0 (OFF) or 1 (ON). Sets timer mode register mn (TMRmn) (determines operation mode of channel). INTTMmn output delay is set to timer data register mn (TDRmn). Clears the TOEmn bit to 0 and stops operation of TOMn.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and the TIln pin input valid edge detection wait status is set.
	Detects the TIln pin input valid edge.	Value of the TDRmn register is loaded to the timer count register mn (TCRmn).
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used.	The counter (TCRmn) counts down. When TCRmn counts down to 0000H, INTTMmn is output, and counting stops (which leaves TCRmn at 0000H) until the next TIln pin input.
Operation stop	The TTmn bit is set to 1. The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops.
TAU stop	The TAUmEN bit of the PER0 register is cleared to 0.	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TIln), timer output pin (TOmn) : n = 0, 1, 3 to 7))

6.8 Simultaneous Channel Operation Function of Timer Array Unit

6.8.1 Operation as one-shot pulse output function

By using two channels as a set, a one-shot pulse having any delay pulse width can be generated from the signal input to the TImn pin.

The delay time and pulse width can be calculated by the following expressions.

$$\begin{aligned}\text{Delay time} &= \{\text{Set value of TDRmn (master)} + 2\} \times \text{Count clock period} \\ \text{Pulse width} &= \{\text{Set value of TDRmp (slave)}\} \times \text{Count clock period}\end{aligned}$$

The master channel operates in the one-count mode and counts the delays. Timer count register mn (TCRmn) of the master channel starts operating upon start trigger detection and loads the value of timer data register mn (TDRmn).

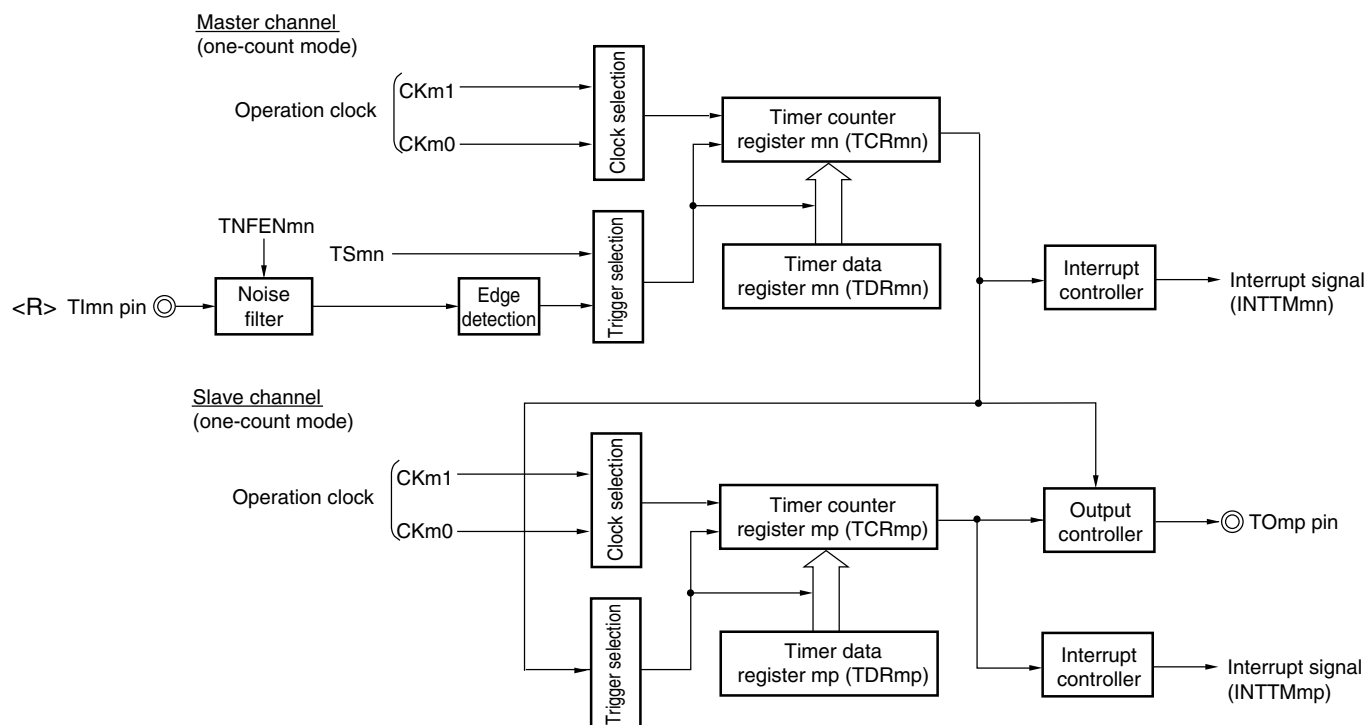
The TCRmn register counts down from the value of the TDRmn register it has loaded, in synchronization with the count clock. When TCRmn = 0000H, it outputs INTTMmn and stops counting until the next start trigger is detected.

The slave channel operates in the one-count mode and counts the pulse width. The TCRmp register of the slave channel starts operation using INTTMmn of the master channel as a start trigger, and loads the value of the TDRmp register. The TCRmp register counts down from the value of the TDRmp register it has loaded, in synchronization with the count value. When count value = 0000H, it outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) is detected. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

Instead of using the TImn pin input, a one-shot pulse can also be output using the software operation (TSmn = 1) as a start trigger.

Caution The timing of loading of timer data register mn (TDRmn) of the master channel is different from that of the TDRmp register of the slave channel. If the TDRmn and TDRmp registers are rewritten during operation, therefore, an illegal waveform is output. Rewrite the TDRmn register after INTTMmn is generated and the TDRmp register after INTTMmp is generated.

Remark m: Unit number (m = 0), n: Channel number (n = 0, 4, 6)
p: Slave channel number (n < p ≤ 7)
However, timer output pin (TOmp) : p = 1, 3 to 7

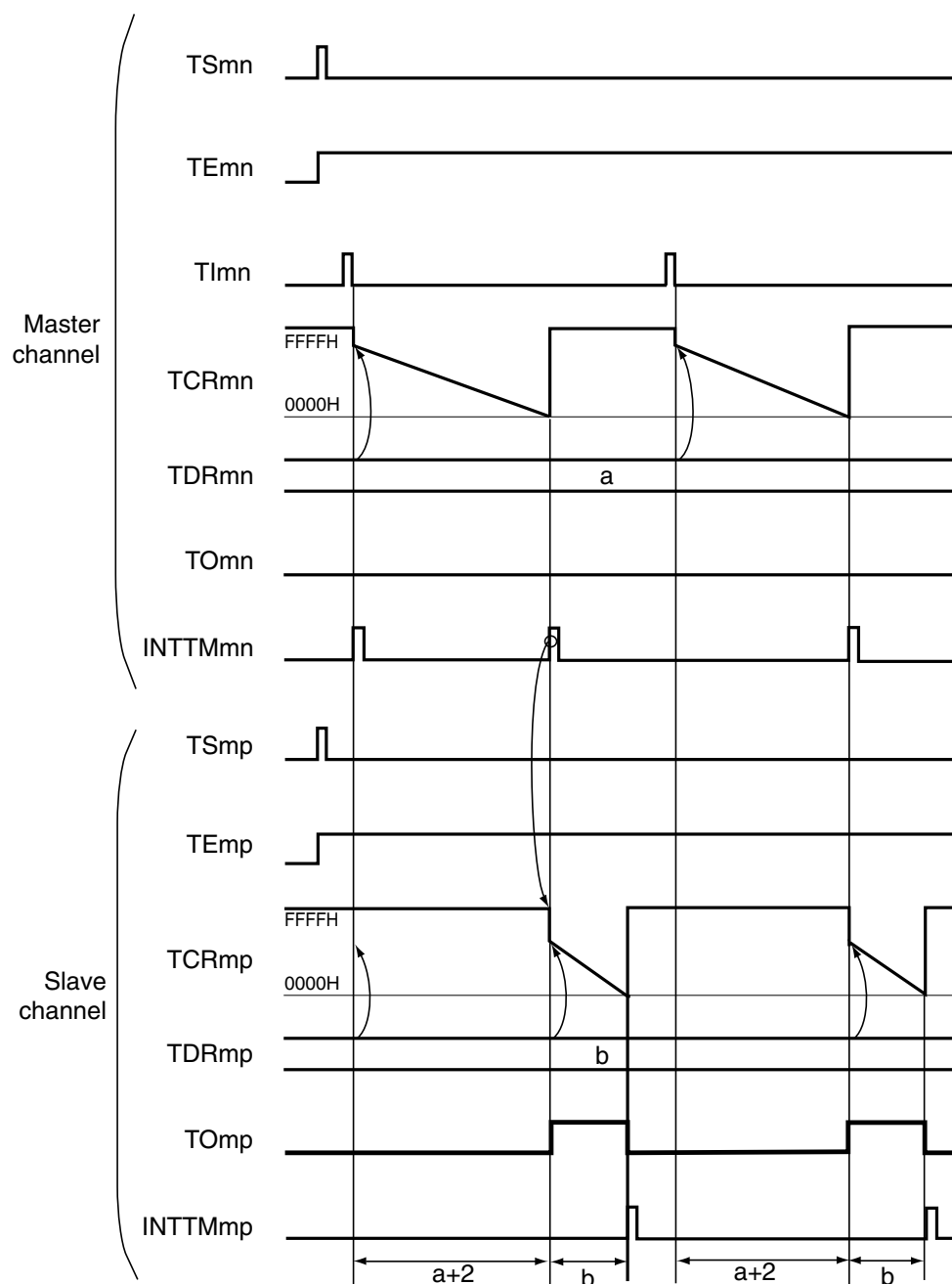
Figure 6-65. Block Diagram of Operation as One-Shot Pulse Output Function

Remark m: Unit number ($m = 0$), n: Channel number ($n = 0, 2, 4, 6$)

p: Slave channel number ($n < p \leq 7$)

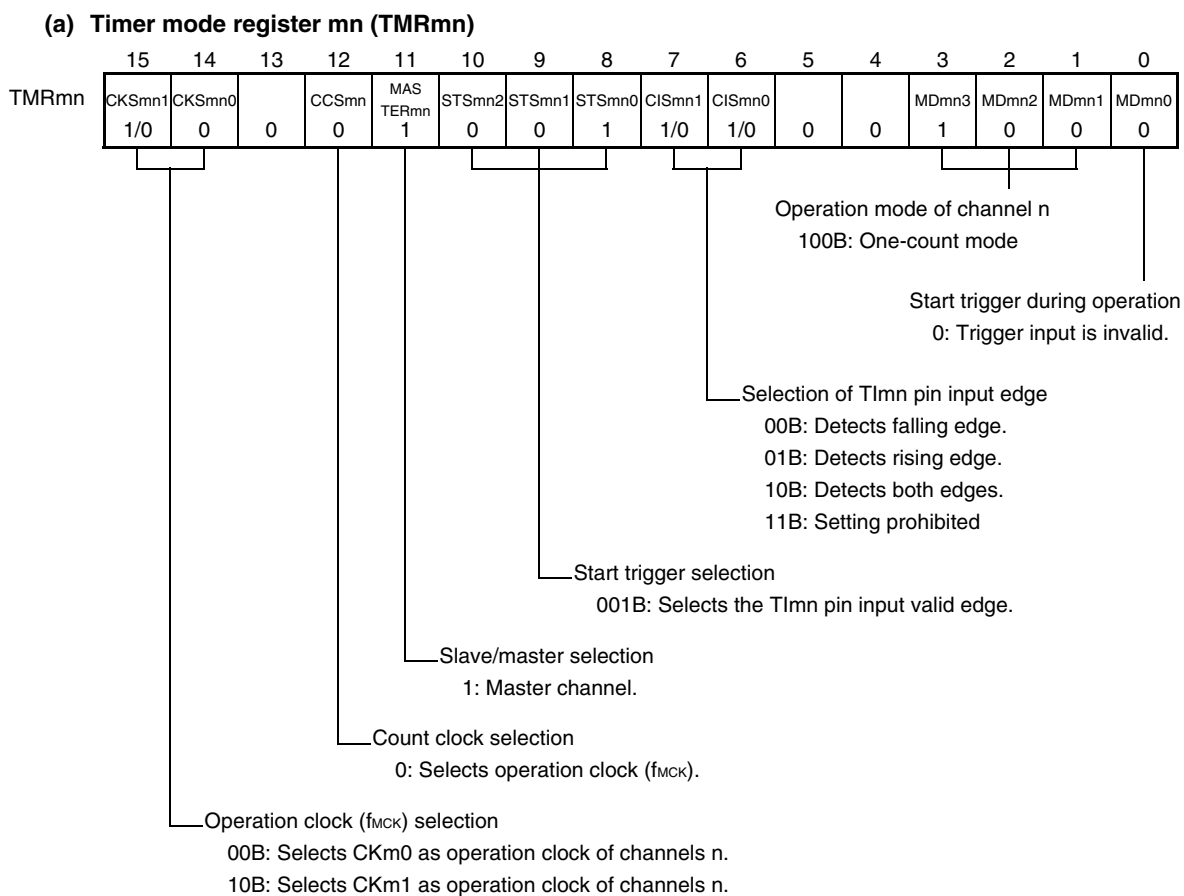
However, timer output pin (TO_{mp}) : $p = 1, 3$ to 7

Figure 6-66. Example of Basic Timing of Operation as One-Shot Pulse Output Function

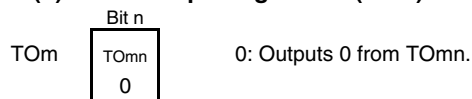


- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
 p: Slave channel number (n < p ≤ 7)
 However, timer output pin (TO_{mp}) : p = 1, 3 to 7
 2. TS_{mn}, TS_{mp}: Bit n, p of timer channel start register m (TS_m)
 TE_{mn}, TE_{mp}: Bit n, p of timer channel enable status register m (TE_m)
 TI_{mn}, TI_{mp}: TI_{mn} and TI_{mp} pins input signal
 TCR_{mn}, TCR_{mp}: Timer count registers mn, mp (TCR_{mn}, TCR_{mp})
 TDR_{mn}, TDR_{mp}: Timer data registers mn, mp (TDR_{mn}, TDR_{mp})
 TO_{mn}, TO_{mp}: TO_{mn} and TO_{mp} pins output signal

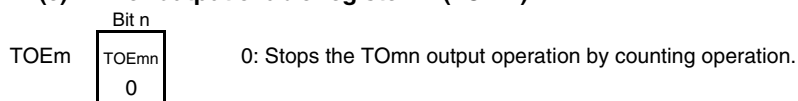
Figure 6-67. Example of Set Contents of Registers When One-Shot Pulse Output Function Is Used (Master Channel)



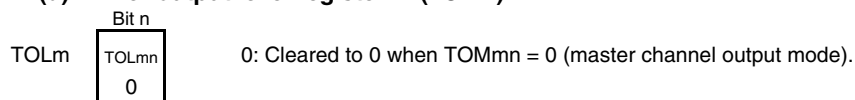
(b) Timer output register m (TOM)



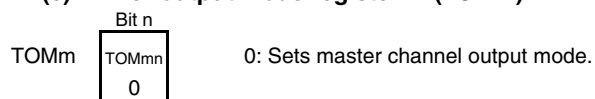
(c) Timer output enable register m (TOEm)



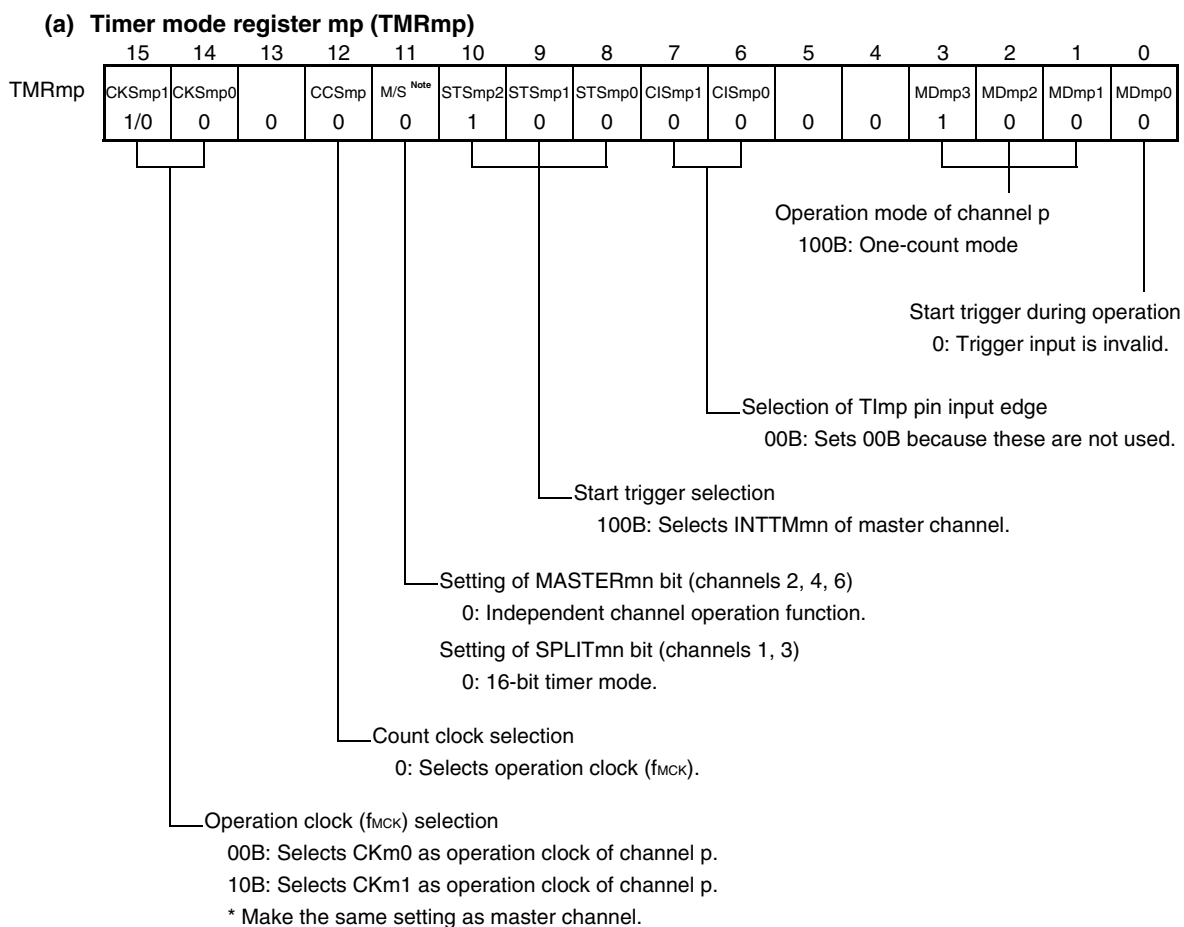
(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)



Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

<R> **Figure 6-68. Example of Set Contents of Registers When One-Shot Pulse Output Function Is Used (Slave Channel)****(b) Timer output register m (TOM)**

TOM	Bit p	
	TOMp	0: Outputs 0 from TOMp. 1: Outputs 1 from TOMp.
	1/0	

(c) Timer output enable register m (TOEm)

TOEm	Bit p	
	TOEmp	0: Stops the TOMp output operation by counting operation. 1: Enables the TOMp output operation by counting operation.
	1/0	

(d) Timer output level register m (TOLm)

TOLm	Bit p	
	TOLmp	0: Positive logic output (active-high) 1: Negative logic output (active-low)
	1/0	

(e) Timer output mode register m (TOMm)

TOMm	Bit p	
	TOMmp	1: Sets the slave channel output mode.
	1	

Note TMRm2, TMRm4, TMRm6: MASTERmn bit
 TMRm1, TMRm3: SPLITmp bit
 TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
 p: Slave channel number (n < p ≤ 7)
 However, timer output pin (TOMp) : p = 1, 3 to 7

Figure 6-69. Operation Procedure of One-Shot Pulse Output Function (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable registers 0 (PER0) to 1.	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 0 (OFF) or 1 (ON). Sets timer mode register mn, mp (TMRmn, TMRmp) of two channels to be used (determines operation mode of channels). An output delay is set to timer data register mn (TDRmn) of the master channel, and a pulse width is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of timer output mode register m (TOMm) is set to 1 (slave channel output mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output.	The TOmp pin goes into Hi-Z output state.
	Sets the TOEmp bit to 1 and enables operation of TOmp. Clears the port register and port mode register to 0.	The TOmp default setting level is output when the port mode register is in output mode and the port register is 0. TOmp does not change because channel stops operating. The TOmp pin outputs the TOmp set level.

(Note and Remark are listed on the next page.)

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Figure 6-69. Operation Procedure of One-Shot Pulse Output Function (2/2)

	Software Operation	Hardware Status
Operation start	Sets the TOEmp bit (slave) to 1 (only when operation is resumed).	The TEMn and TEm bits are set to 1 and the master channel enters the TImn input edge detection wait status. Counter stops operating.
	The TSmn (master) and TSmp (slave) bits of timer channel start register m (TSM) are set to 1 at the same time.	
	The TSmn and TSmp bits automatically return to 0 because they are trigger bits.	Master channel starts counting.
During operation	Set values of only the CISmn1 and CISmn0 bits of the TMRmn register can be changed.	Master channel loads the value of the TDRmn register to timer count register mn (TCRmn) when the TImn pin valid input edge is detected, and the counter starts counting down. When the count value reaches TCRmn = 0000H, the INTTMmn output is generated, and the counter stops until the next valid edge is input to the TImn pin.
	Set values of the TMRmp, TDRmn, TDRmp registers, TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed.	
Operation stop	The TCRmn and TCRmp registers can always be read.	The slave channel, triggered by INTTMmn of the master channel, loads the value of the TDRmp register to the TCRmp register, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
	The TSRmn and TSRmp registers are not used.	
TAU stop	Set values of the TOM and TOEm registers by slave channel can be changed.	The TOmp bit of slave channel is cleared to 0 and value is set to the TOmp bit.
	The TTmn (master) and TTmp (slave) bits are set to 1 at the same time.	
TAU stop	The TTmn and TTmp bits automatically return to 0 because they are trigger bits.	The TOmp pin outputs the TOmp set level.
	The TOEmp bit of slave channel is cleared to 0 and value is set to the TOmp bit.	
TAU stop	To hold the TOmp pin output level	The TOmp pin output level is held by port function.
	Clears the TOmp bit to 0 after the value to be held is set to the port register.	
TAU stop	When holding the TOmp pin output level is not necessary	Power-off status
	Setting not required.	
TAU stop	The TAUmEN bit of the PER0 register is cleared to 0.	All circuits are initialized and SFR of each channel is also initialized. (The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

p: Slave channel number (n < p ≤ 7)

However, timer output pin (TOmp) : p = 1, 3 to 7

6.8.2 Operation as PWM function

Two channels can be used as a set to generate a pulse of any period and duty factor.

The period and duty factor of the output pulse can be calculated by the following expressions.

Pulse period = {Set value of TDRmn (master) + 1} × Count clock period
 Duty factor [%] = {Set value of TDRmp (slave)} / {Set value of TDRmn (master) + 1} × 100
 0% output: Set value of TDRmp (slave) = 0000H
 100% output: Set value of TDRmp (slave) ≥ {Set value of TDRmn (master) + 1}

Remark The duty factor exceeds 100% if the set value of TDRmp (slave) > (set value of TDRmn (master) + 1), it summarizes to 100% output.

The master channel operates in the interval timer mode. If the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, an interrupt (INTTMmn) is output, the value set to timer data register mn (TDRmn) is loaded to timer count register mn (TCRmn), and the counter counts down in synchronization with the count clock. When the counter reaches 0000H, INTTMmn is output, the value of the TDRmn register is loaded again to the TCRmn register, and the counter counts down. This operation is repeated until the channel stop trigger bit (TTmn) of timer channel stop register m (TTm) is set to 1.

If two channels are used to output a PWM waveform, the period until the master channel counts down to 0000H is the PWM output (TOmp) cycle.

The slave channel operates in one-count mode. By using INTTMmn from the master channel as a start trigger, the TCRmp register loads the value of the TDRmp register and the counter counts down to 0000H. When the counter reaches 0000H, it outputs INTTMmp and waits until the next start trigger (INTTMmn from the master channel) is generated.

If two channels are used to output a PWM waveform, the period until the slave channel counts down to 0000H is the PWM output (TOmp) duty.

PWM output (TOmp) goes to the active level one clock after the master channel generates INTTMmn and goes to the inactive level when the TCRmp register of the slave channel becomes 0000H.

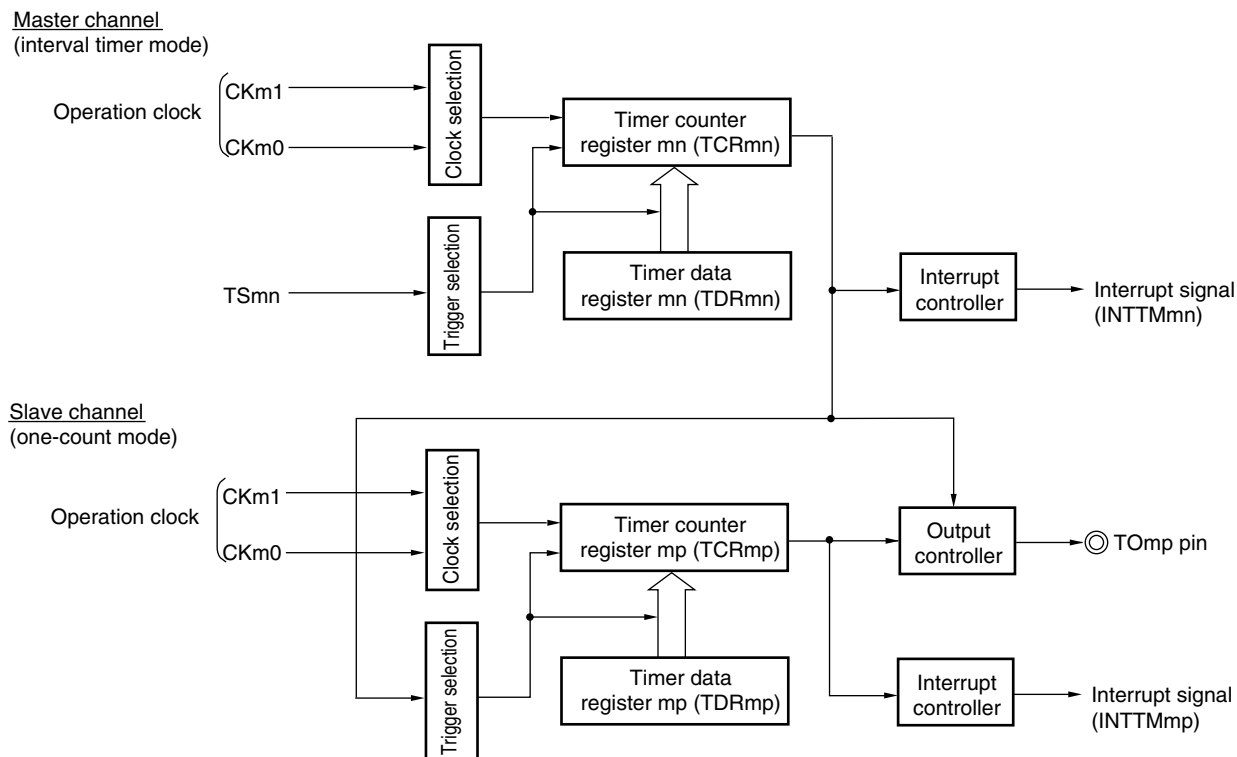
Caution To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel, a write access is necessary two times. The timing at which the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers is upon occurrence of INTTMmn of the master channel. Thus, when rewriting is performed split before and after occurrence of INTTMmn of the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, therefore, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel.

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

p: Slave channel number (n < p ≤ 7)

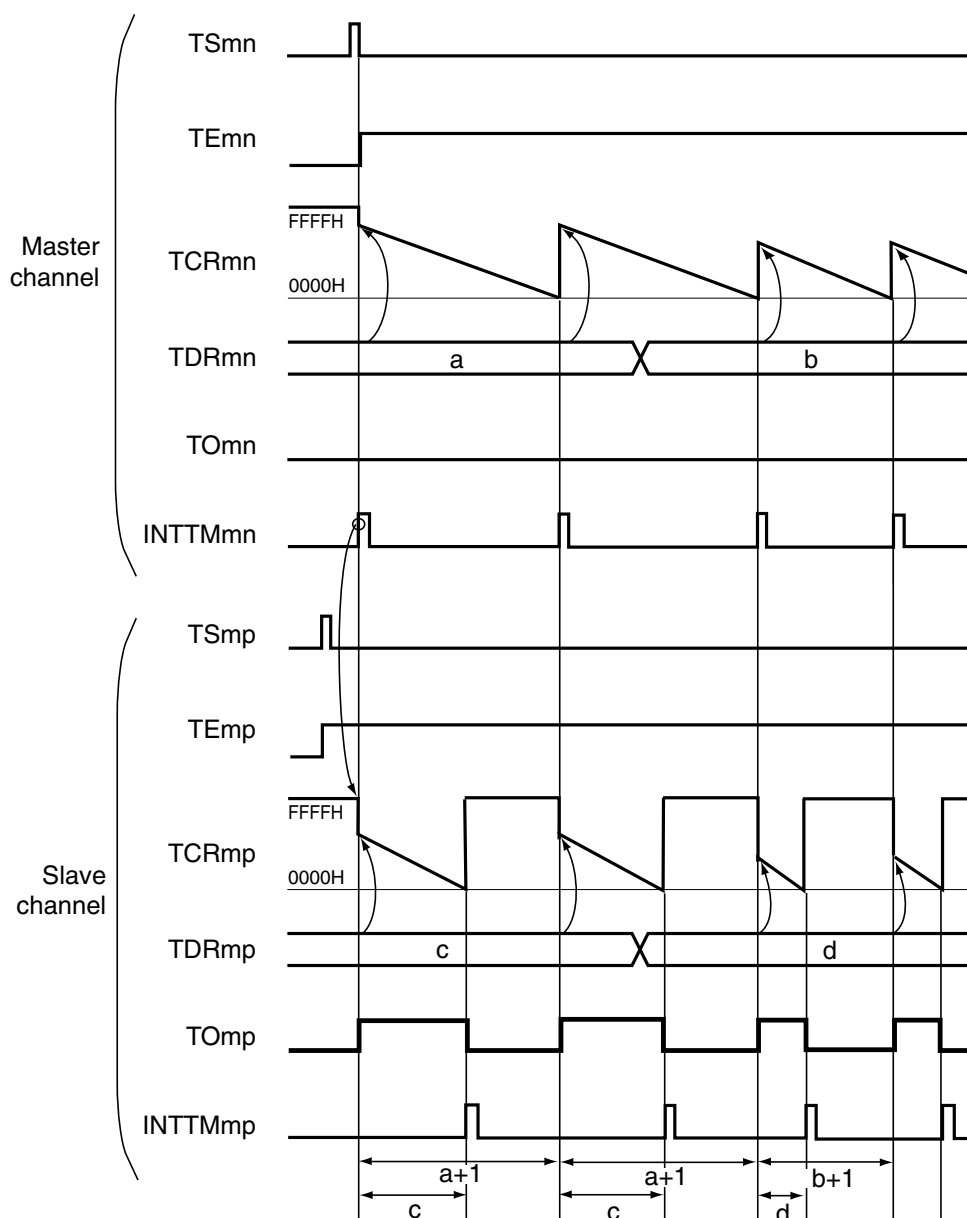
However, timer output pin (TOmp) : p = 1, 3 to 7

Figure 6-70. Block Diagram of Operation as PWM Function



Remark m: Unit number ($m = 0$), n: Channel number ($n = 0, 2, 4, 6$)
 p: Slave channel number ($n < p \leq 7$)
 However, timer output pin (TOmp) : $p = 1, 3$ to 7

Figure 6-71. Example of Basic Timing of Operation as PWM Function



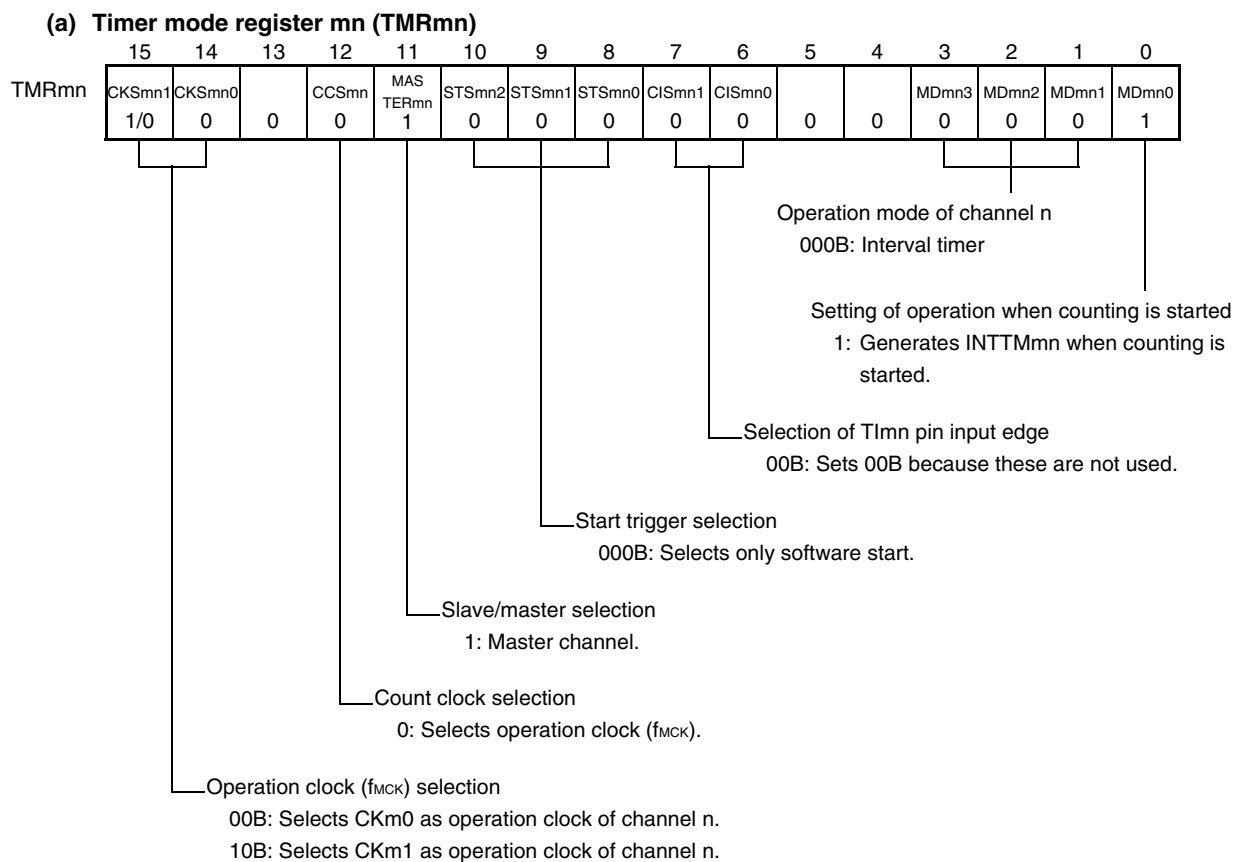
Remark 1. m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

p: Slave channel number (n < p ≤ 7)

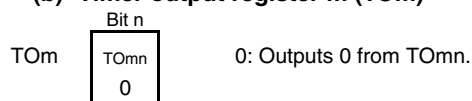
However, timer output pin (TOmp) : p = 1, 3 to 7

2. TSmn, TSmp: Bit n, p of timer channel start register m (TSm)
- TEmn, TEmp: Bit n, p of timer channel enable status register m (TEm)
- TCRmn, TCRmp: Timer count registers mn, mp (TCRmn, TCRmp)
- TDRmn, TDRmp: Timer data registers mn, mp (TDRmn, TDRmp)
- TOmn, TOmp: TOmn and TOmp pins output signal

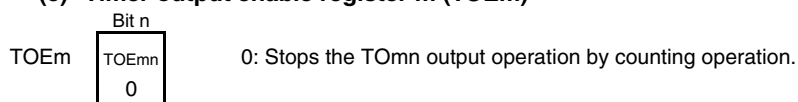
Figure 6-72. Example of Set Contents of Registers When PWM Function (Master Channel) Is Used



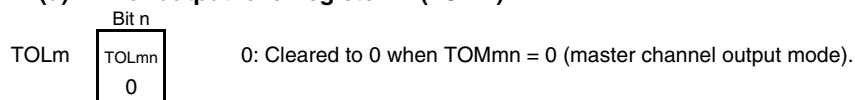
(b) Timer output register m (TOM)



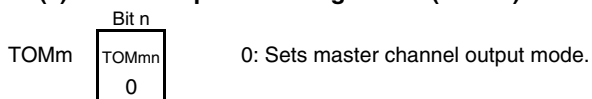
(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)

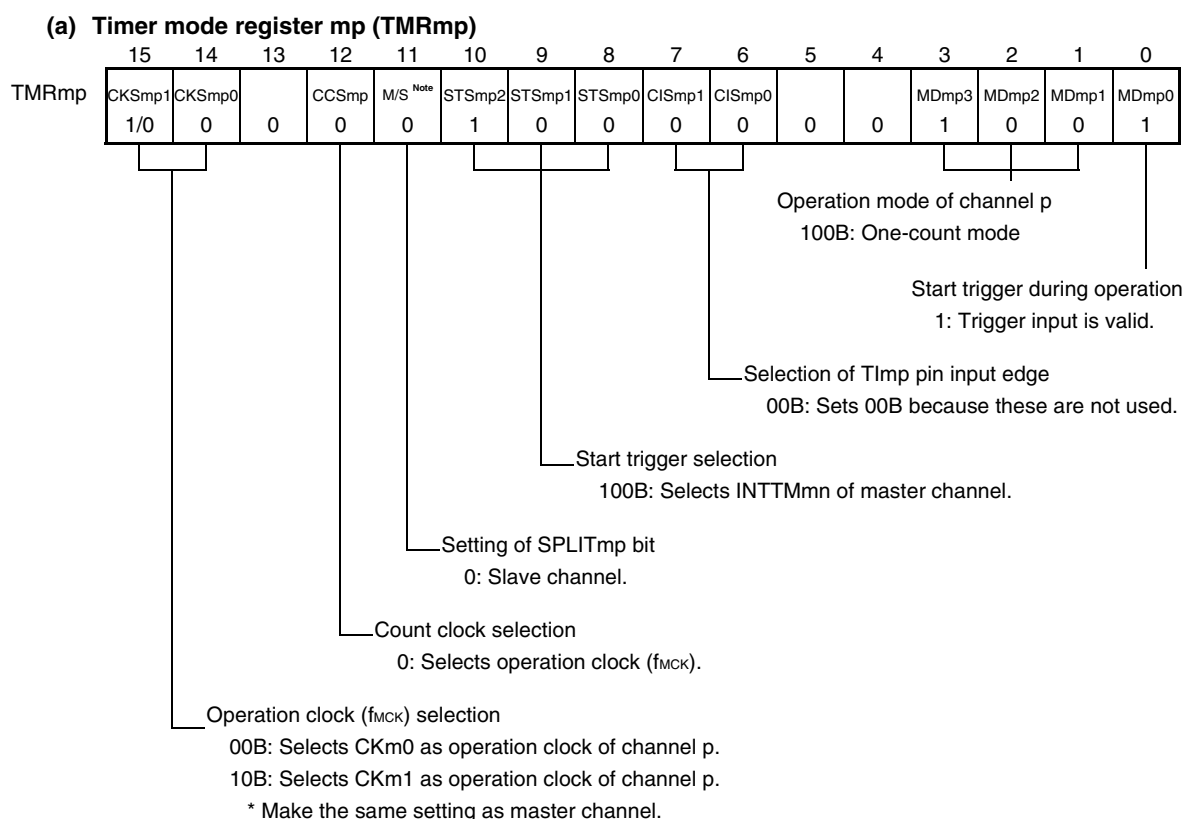


(e) Timer output mode register m (TOMm)



Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

Figure 6-73. Example of Set Contents of Registers When PWM Function (Slave Channel) Is Used



(b) Timer output register m (TOM)

TOM	Bit p	
	TOMp	
	1/0	0: Outputs 0 from TOMp. 1: Outputs 1 from TOMp.

(c) Timer output enable register m (TOEm)

TOEm	Bit p	
	TOEmp	
	1/0	0: Stops the TOMp output operation by counting operation. 1: Enables the TOMp output operation by counting operation.

(d) Timer output level register m (TOLm)

TOLm	Bit p	
	TOLmp	
	1/0	0: Positive logic output (active-high) 1: Negative logic output (active-low)

(e) Timer output mode register m (TOMm)

TOMm	Bit p	
	TOMmp	
	1	1: Sets the slave channel output mode.

Note TMRm5, TMRm7: Fixed to 0
 TMRm1, TMRm3: SPLITmp bit

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
 p: Slave channel number (n < p ≤ 7)
 However, timer output pin (TOMp) : p = 1, 3 to 7

Figure 6-74. Operation Procedure When PWM Function Is Used (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode registers mn, mp (TMRmn, TMRmp) of two channels to be used (determines operation mode of channels). An interval (period) value is set to timer data register mn (TDRmn) of the master channel, and a duty factor is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of timer output mode register m (TOMm) is set to 1 (slave channel output mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output. →	The TOmp pin goes into Hi-Z output state.
	Sets the TOEmp bit to 1 and enables operation of TOmp. → Clears the port register and port mode register to 0. →	The TOmp default setting level is output when the port mode register is in output mode and the port register is 0. TOmp does not change because channel stops operating. The TOmp pin outputs the TOmp set level.

(**Note** and **Remark** are listed on the next page.)

Figure 6-74. Operation Procedure When PWM Function Is Used (2/2)

	Software Operation	Hardware Status
Operation start	Sets the TOEmp bit (slave) to 1 (only when operation is resumed). The TSmn (master) and TSmp (slave) bits of timer channel start register m (TSM) are set to 1 at the same time. The TSmn and TSmp bits automatically return to 0 because they are trigger bits.	TEmn = 1, TEm = 1 ► When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.
During operation	Set values of the TMRmn and TMRmp registers, TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed. Set values of the TDRmn and TDRmp registers can be changed after INTTMmn of the master channel is generated. The TCRmn and TCRmp registers can always be read. The TSRmn and TSRmp registers are not used.	The counter of the master channel loads the TDRmn register value to timer count register mn (TCRmn), and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again. At the slave channel, the value of the TDRmp register is loaded to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn (master) and TTmp (slave) bits are set to 1 at the same time. The TTmn and TTmp bits automatically return to 0 because they are trigger bits. The TOEmp bit of slave channel is cleared to 0 and value is set to the TOmp bit.	TEmn, TEm = 0, and count operation stops. The TCRmn and TCRmp registers hold count value and stop. The TOmp output is not initialized but holds current status. ----- ► The TOmp pin outputs the TOmp set level.
TAU stop	To hold the TOmp pin output level Clears the TOmp bit to 0 after the value to be held is set to the port register. When holding the TOmp pin output level is not necessary Setting not required. The TAUmEN bit of the PER0 register is cleared to 0.	► The TOmp pin output level is held by port function. ----- ► Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

p: Slave channel number (n < p ≤ 7)

However, timer output pin (TOmp) : p = 1, 3 to 7

6.8.3 Operation as multiple PWM output function

By extending the PWM function and using multiple slave channels, many PWM waveforms with different duty values can be output.

For example, when using two slave channels, the period and duty factor of an output pulse can be calculated by the following expressions.

$$\begin{aligned}\text{Pulse period} &= \{\text{Set value of TDRmn (master)} + 1\} \times \text{Count clock period} \\ \text{Duty factor 1 [\%]} &= \{\text{Set value of TDRmp (slave 1)}\} / \{\text{Set value of TDRmn (master)} + 1\} \times 100 \\ \text{Duty factor 2 [\%]} &= \{\text{Set value of TDRmq (slave 2)}\} / \{\text{Set value of TDRmn (master)} + 1\} \times 100\end{aligned}$$

Remark Although the duty factor exceeds 100% if the set value of TDRmp (slave 1) > {set value of TDRmn (master) + 1} or if the {set value of TDRmq (slave 2)} > {set value of TDRmn (master) + 1}, it is summarized into 100% output.

Timer count register mn (TCRmn) of the master channel operates in the interval timer mode and counts the periods.

The TCRmp register of the slave channel 1 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmp pin. The TCRmp register loads the value of timer data register mp (TDRmp), using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmp = 0000H, TCRmp outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

In the same way as the TCRmp register of the slave channel 1, the TCRmq register of the slave channel 2 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOMq pin. The TCRmq register loads the value of the TDRmq register, using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmq = 0000H, the TCRmq register outputs INTTMmq and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOMq becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmq = 0000H.

When channel 0 is used as the master channel as above, up to six types of PWM signals can be output at the same time.

Caution To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel 1, write access is necessary at least twice. Since the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers after INTTMmn is generated from the master channel, if rewriting is performed separately before and after generation of INTTMmn from the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel (This applies also to the TDRmq register of the slave channel 2).

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)

p: Slave channel number 1, q: Slave channel number 2

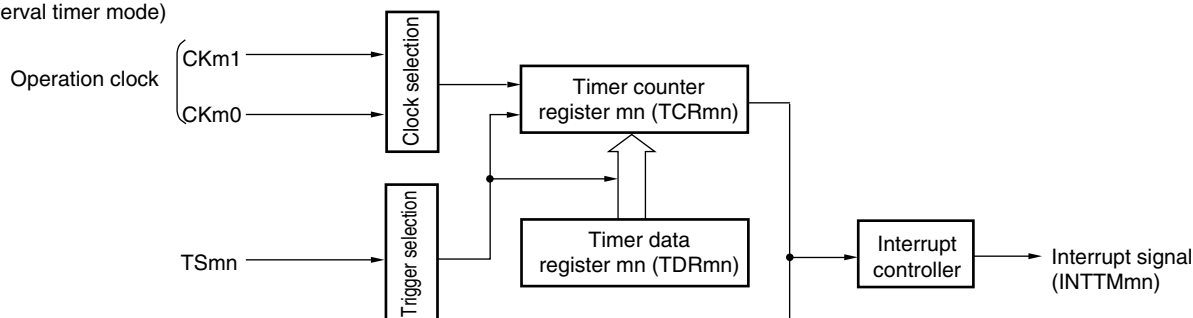
$n < p < q \leq 7$

However, timer output pin (TOmp, TOMq) : p = 1, 3 to 6, q = 3 to 7

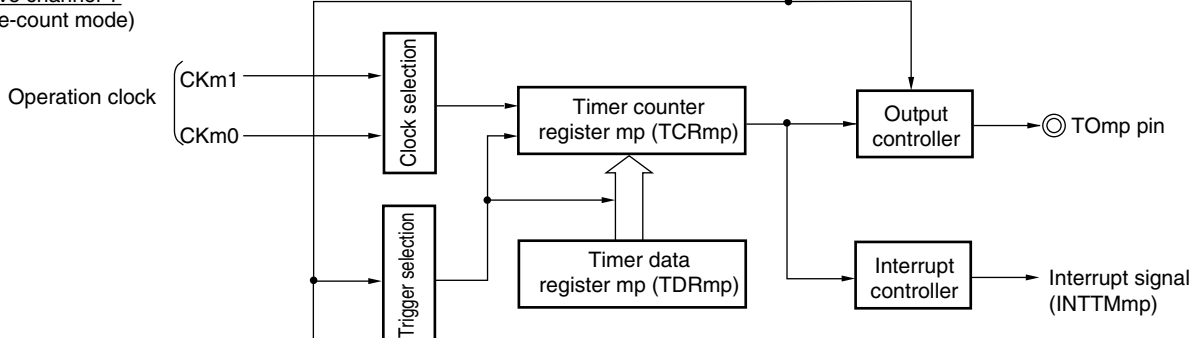
<R>

Figure 6-75. Block Diagram of Operation as Multiple PWM Output Function (output two types of PWMs)

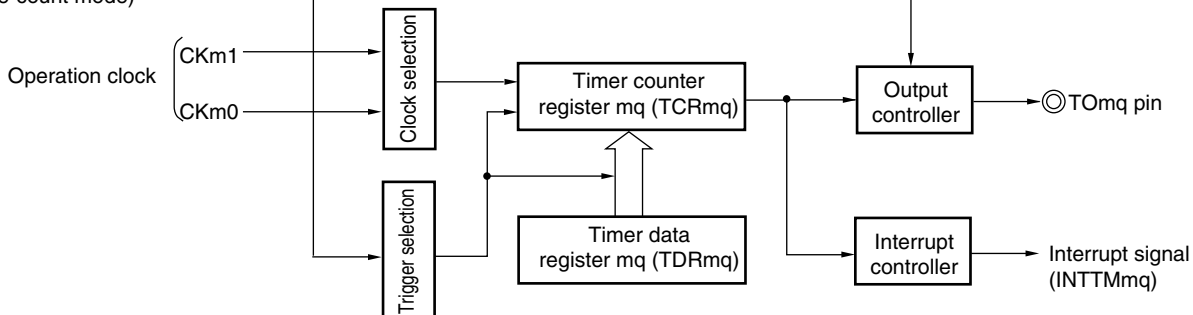
Master channel
(interval timer mode)



Slave channel 1
(one-count mode)



Slave channel 2
(one-count mode)



Remark m: Unit number ($m = 0$), n: Channel number ($n = 0, 2, 4$)

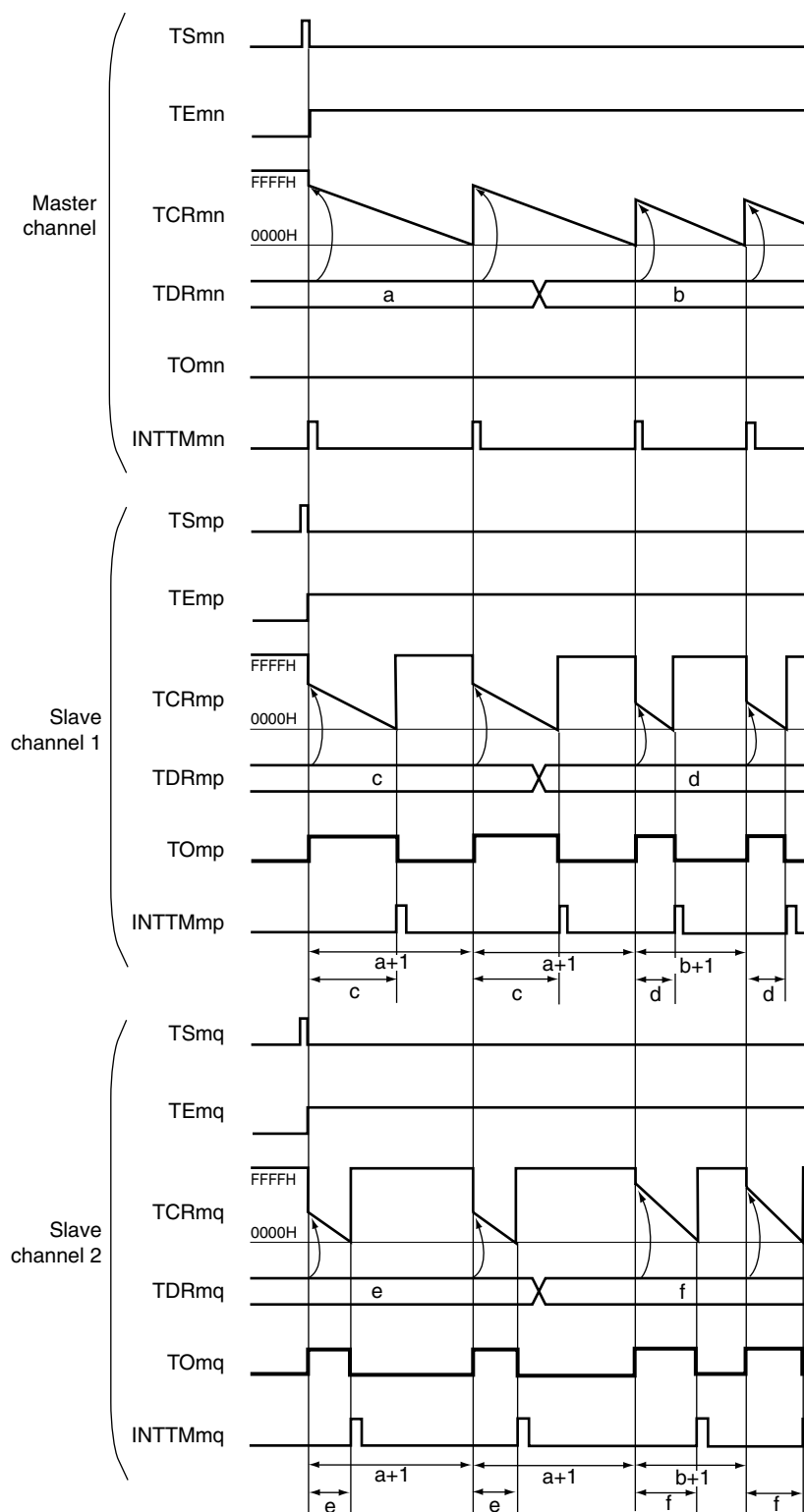
p: Slave channel number 1, q: Slave channel number 2

$n < p < q \leq 7$

However, timer output pin (TOMP, TOMQ) : $p = 1, 3$ to 6, $q = 3$ to 7

<R>

**Figure 6-76. Example of Basic Timing of Operation as Multiple PWM Output Function
(Output two types of PWMs)**



(Remark is listed on the next page.)

Remark 1. m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)

p: Slave channel number 1, q: Slave channel number 2

$n < p < q \leq 7$

However, timer output pin (TOmp, TOmq) : p = 1, 3 to 6, q = 3 to 7

2. TSmn, TSmp, TSmq: Bit n, p, q of timer channel start register m (TSM)

TEmn, TEmq, TEMq: Bit n, p, q of timer channel enable status register m (TEM)

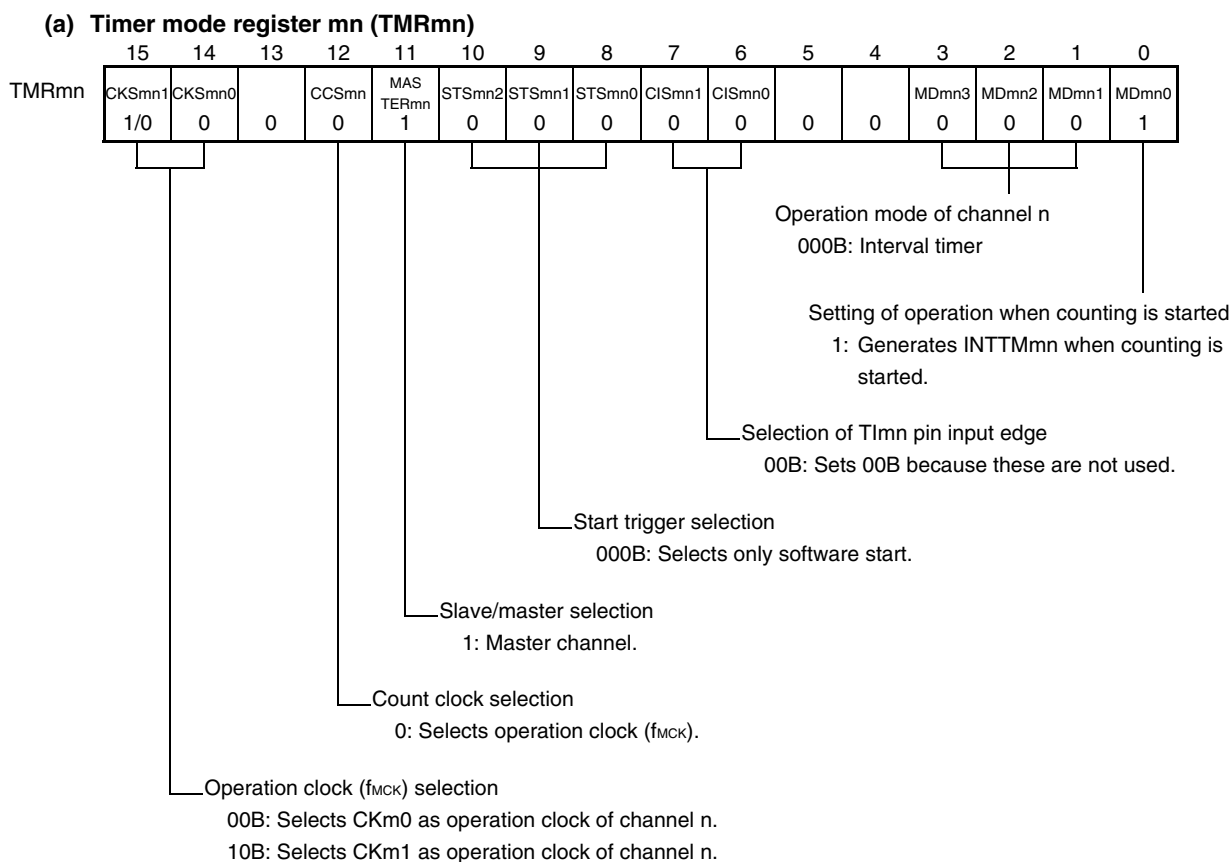
TCRmn, TCRmp, TCRmq: Timer count registers mn, mp, mq (TCRmn, TCRmp, TCRmq)

TDRmn, TDRmp, TDRmq: Timer data registers mn, mp, mq (TDRmn, TDRmp, TDRmq)

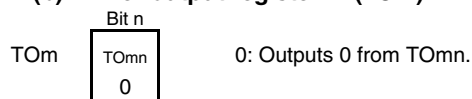
TOmn, TOmp, TOmq: TOmn, TOmp, and TOmq pins output signal

<R>

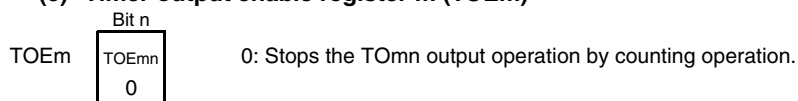
**Figure 6-77. Example of Set Contents of Registers
When Multiple PWM Output Function (Master Channel) Is Used**



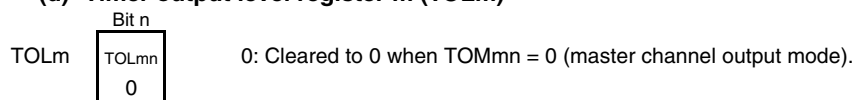
(b) Timer output register m (TOM)



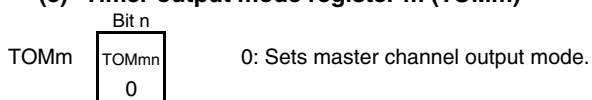
(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)



Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)

Figure 6-78. Example of Set Contents of Registers
When Multiple PWM Output Function (Slave Channel) Is Used (output two types of PWMs)

(a) Timer mode register mp, mq (TMRmp, TMRmq)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmp	CKSmp1	CKSmp0		CCSmp	M/S ^{Note}	STSmp2	STSmp1	STSmp0	CISmp1	CISmp0			MDmp3	MDmp2	MDmp1	MDmp0
	1/0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
TMRmq	CKSmq1	CKSmq0		CCSmq	M/S ^{Note}	STSmq2	STSmq1	STSmq0	CISmq1	CISmq0			MDmq3	MDmq2	MDmq1	MDmq0
	1/0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1

Operation mode of channel p, q
 100B: One-count mode

Start trigger during operation
 1: Trigger input is valid.

Selection of TImp and TImq pins input edge
 00B: Sets 00B because these are not used.

Start trigger selection
 100B: Selects INTTMmn of master channel.

Setting of MASTERmp, MASTERmq bits (channels 2, 4, 6)
 0: Independent channel operation function.

Setting of SPLITmp, SPLITmq bits (channels 1, 3)
 0: 16-bit timer mode.

Count clock selection
 0: Selects operation clock (f_{MCK}).

Operation clock (f_{MCK}) selection
 00B: Selects CKm0 as operation clock of channel p, q.
 10B: Selects CKm1 as operation clock of channel p, q.
 * Make the same setting as master channel.

(b) Timer output register m (TOM)

	Bit q	Bit p
TOM	TOmq	TOmp
	1/0	1/0

0: Outputs 0 from TOmp or TOmq.
 1: Outputs 1 from TOmp or TOmq.

(c) Timer output enable register m (TOEm)

	Bit q	Bit p
TOEm	TOEmq	TOEmp
	1/0	1/0

0: Stops the TOmp or TOmq output operation by counting operation.
 1: Enables the TOmp or TOmq output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit q	Bit p
TOLm	TOLmq	TOLmp
	1/0	1/0

0: Positive logic output (active-high)
 1: Negative logic output (active-low)

(e) Timer output mode register m (TOMm)

	Bit q	Bit p
TOMm	TOMmq	TOMmp
	1	1

1: Sets the slave channel output mode.

Note TMRm2, TMRm4, TMRm6: MASTERmp, MASTERmq bit
 TMRm1, TMRm3: SPLITmp, SPLITmq bit
 TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)
 p: Slave channel number 1, q: Slave channel number 2

n < p < q ≤ 7

However, timer output pin (TOmp, TOmq) : p = 1, 3 to 6, q = 3 to 7

<R>

Figure 6-79. Operation Procedure When Multiple PWM Output Function Is Used (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode registers mn, mp, 0q (TMRmn, TMRmp, TMRmq) of each channel to be used (determines operation mode of channels). An interval (period) value is set to timer data register mn (TDRmn) of the master channel, and a duty factor is set to the TDRmp and TDRmq registers of the slave channels.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channels. The TOMmp and TOMmq bits of timer output mode register m (TOMm) are set to 1 (slave channel output mode). Clears the TOLmp and TOLmq bits to 0. Sets the TOmp and TOMq bits and determines default level of the TOmp and TOMq outputs. →	The TOmp and TOMq pins go into Hi-Z output state.
	Sets the TOEmp and TOEmq bits to 1 and enables operation of TOmp and TOMq. →	The TOmp and TOMq default setting levels are output when the port mode register is in output mode and the port register is 0.
	Clears the port register and port mode register to 0. →	TOmp and TOMq do not change because channels stop operating. The TOmp and TOMq pins output the TOmp and TOMq set levels.

(Note and Remark are listed on the next page.)

Figure 6-79. Operation Procedure When Multiple PWM Output Function Is Used (2/2)

	Software Operation	Hardware Status
Operation start	(Sets the TOEmp and TOEmq (slave) bits to 1 only when resuming operation.) The TSmn bit (master), and TSmp and TSmq (slave) bits of timer channel start register m (TSM) are set to 1 at the same time. The TSmn, TSmp, and TSmq bits automatically return to 0 because they are trigger bits.	TEmn = 1, TEmq = 1 When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.
During operation	Set values of the TMRmn, TMRmp, TMRmq registers, TOMmn, TOMmp, TOMmq, TOLmn, TOLmp, and TOLmq bits cannot be changed. Set values of the TDRmn, TDRmp, and TDRmq registers can be changed after INTTMmn of the master channel is generated. The TCRmn, TCRmp, and TCRmq registers can always be read. The TSRmn, TSRmp, and TSR0q registers are not used.	The counter of the master channel loads the TDRmn register value to timer count register mn (TCRmn) and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again. At the slave channel 1, the values of the TDRmp register are transferred to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output levels of TOmp become active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. At the slave channel 2, the values of the TDRmq register are transferred to TCRmq register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output levels of TOMq become active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmq = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn bit (master), TTmp, and TTmq (slave) bits are set to 1 at the same time. The TTmn, TTmp, and TTmq bits automatically return to 0 because they are trigger bits.	TEmn, TEmq = 0, and count operation stops. The TCRmn, TCRmp, and TCRmq registers hold count value and stop. The TOmp and TOMq output are not initialized but hold current status.
	The TOEmp and TOEmq bits of slave channels are cleared to 0 and value is set to the TOmp and TOMq bits.	The TOmp and TOMq pins output the TOmp and TOMq set levels.
TAU stop	To hold the TOmp and TOMq pin output levels Clears the TOmp and TOMq bits to 0 after the value to be held is set to the port register. When holding the TOmp and TOMq pin output levels are not necessary Setting not required	The TOmp and TOMq pin output levels are held by port function.
	The TAUMEN bit of the PER0 register is cleared to 0.	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp and TOMq bits are cleared to 0 and the TOmp and TOMq pins are set to port mode.)

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)

p: Slave channel number 1, q: Slave channel number 2

$n < p < q \leq 7$

However, timer output pin (TOmp, TOMq) : p = 1, 3 to 6, q = 3 to 7

6.9 Cautions When Using Timer Array Unit

6.9.1 Cautions When Using Timer output

Depends on products, a pin is assigned a timer output and other alternate functions. In this case, outputs of the other alternate functions must be set in initial status.

(1) 25-pin and 32-pin products

(a) Using TO03 output assigned to the P31

So that the alternated PCLBUZ0 output becomes 0, not only set the port mode register (the PM31 bit) and the port register (the P31 bit) to 0, but also use the bit 7 (PCLOE0) of the clock output select register 0 (CKS0) with the same setting as the initial status.

CHAPTER 7 REAL-TIME CLOCK

7.1 Functions of Real-time Clock

The real-time clock has the following features.

- Having counters of year, month, week, day, hour, minute, and second, and can count up to 99 years.
- Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm: week, hour, minute)
- Pin output function of 1 Hz (48 and 64-pin products only)

Caution The count of year, month, week, day, hour, minutes and second can only be performed when a subsystem clock ($f_{SUB} = 32.768 \text{ kHz}$) is selected as the operation clock of the real-time clock. When the low-speed oscillation clock ($f_{IL} = 15 \text{ kHz}$) is selected, only the constant-period interrupt function is available. The 25- to 32-pin products have the constant-period interrupt function only, because these products have no subsystem clock. However, the constant-period interrupt interval when f_{IL} is selected will be calculated with the constant-period (the value selected with RTCC0 register) $\times f_{SUB}/f_{IL}$.

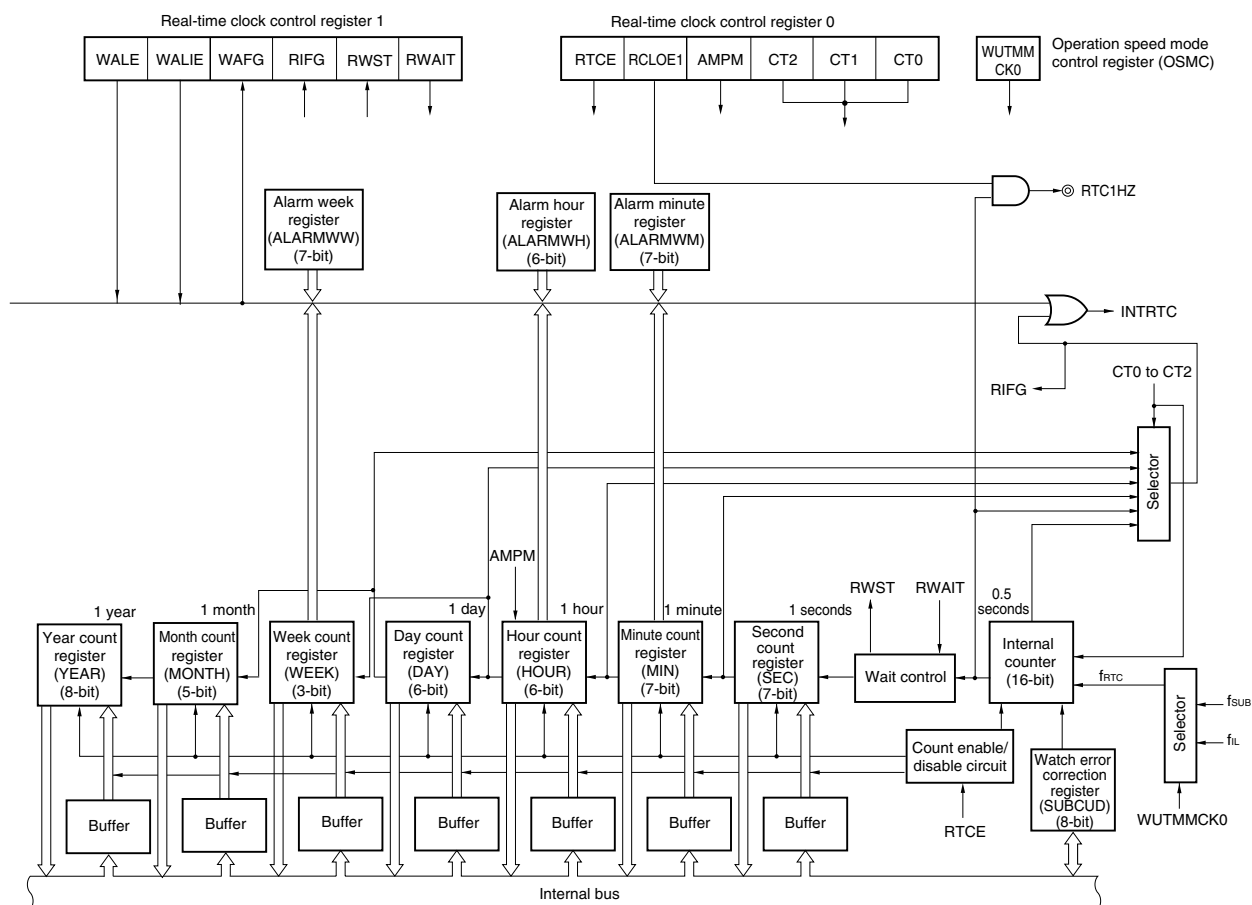
7.2 Configuration of Real-time Clock

The real-time clock includes the following hardware.

Table 7-1. Configuration of Real-time Clock

Item	Configuration
Counter	Counter (16-bit)
Control registers	Peripheral enable register 0 (PER0)
	Operation speed mode control register (OSMC)
	Real-time clock control register 0 (RTCC0)
	Real-time clock control register 1 (RTCC1)
	Second count register (SEC)
	Minute count register (MIN)
	Hour count register (HOUR)
	Day count register (DAY)
	Week count register (WEEK)
	Month count register (MONTH)
	Year count register (YEAR)
	Watch error correction register (SUBCUD)
	Alarm minute register (ALARMWM)
	Alarm hour register (ALARMWH)
	Alarm week register (ALARMWW)

Figure 7-1. Block Diagram of Real-time Clock



Caution The count of year, month, week, day, hour, minutes and second can only be performed when a subsystem clock ($f_{\text{SUB}} = 32.768 \text{ kHz}$) is selected as the operation clock of the real-time clock. When the low-speed oscillation clock ($f_{\text{IL}} = 15 \text{ kHz}$) is selected, only the constant-period interrupt function is available. The 25- to 32-pin products have the constant-period interrupt function only, because these products have no subsystem clock. However, the constant-period interrupt interval when f_{IL} is selected will be calculated with the constant-period (the value selected with RTCC0 register) $\times f_{\text{SUB}}/f_{\text{IL}}$.

7.3 Registers Controlling Real-time Clock

The real-time clock is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Operation speed mode control register (OSMC)
- Real-time clock control register 0 (RTCC0)
- Real-time clock control register 1 (RTCC1)
- Second count register (SEC)
- Minute count register (MIN)
- Hour count register (HOUR)
- Day count register (DAY)
- Week count register (WEEK)
- Month count register (MONTH)
- Year count register (YEAR)
- Watch error correction register (SUBCUD)
- Alarm minute register (ALARMWM)
- Alarm hour register (ALARMWH)
- Alarm week register (ALARMWW)

7.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the real-time clock is used, be sure to set bit 7 (RTCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-2. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	IICA0EN	SAU1EN Note	SAU0EN	0	TAU0EN

RTCEN	Control of real-time clock (RTC) and 12-bit interval timer input clock supply
0	Stops input clock supply. - SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be written. - The real-time clock (RTC) and 12-bit interval timer are in the reset status.
1	Enables input clock supply. SFR used by the real-time clock (RTC) and 12-bit interval timer can be read and written.

Note 32, 48, and 64-pin products only.

- Cautions**
1. When using the real-time clock, first set the RTCEN bit to 1, while oscillation of the input clock (f_{RTC}) is stable. If RTCEN = 0, writing to a control register of the real-time clock or 12-bit interval timer is ignored, and, even if the register is read, only the default value is read.
 2. The subsystem clock supply to peripheral functions other than the real-time clock and 12-bit interval timer can be stopped in STOP mode or HALT mode when the subsystem clock is used, by setting the RTCLPC bit of the operation speed mode control register (OSMC) to 1. In this case, set the RTCEN bit of the PER0 register to 1 and the other bits (bits 0 to 6) to 0.
 3. Be sure to clear the following bits to 0.
 - 25-pin products: bits 1, 3, 6
 - 32, 48, 64-pin products: bits 1, 6

7.3.2 Operation speed mode control register (OSMC)

The WUTMMCK0 bit can be used to select the real-time clock operation clock (f_{RTC}).

In addition, by stopping clock functions that are unnecessary, the RTCLPC bit can be used to reduce power consumption. For details about setting the RTCLPC bit, see **CHAPTER 5 CLOCK GENERATOR**.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-3. Format of Operation Speed Mode Control Register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

WUTMMCK0	Selection of operation clock (f_{RTC}) for real-time clock and 12-bit interval timer.
0	Subsystem clock (f_{SUB})
1	Low-speed on-chip oscillator clock (f_{IL})

Caution The count of year, month, week, day, hour, minutes and second can only be performed when a subsystem clock ($f_{SUB} = 32.768$ kHz) is selected as the operation clock of the real-time clock. When the low-speed oscillation clock ($f_{IL} = 15$ kHz) is selected, only the constant-period interrupt function is available. The 25- to 32-pin products have the constant-period interrupt function only, because these products have no subsystem clock. However, the constant-period interrupt interval when f_{IL} is selected will be calculated with the constant-period (the value selected with RTCC0 register) $\times f_{SUB}/f_{IL}$.

7.3.3 Real-time clock control register 0 (RTCC0)

The RTCC0 register is an 8-bit register that is used to start or stop the real-time clock operation, control the RTC1HZ pin, and set a 12- or 24-hour system and the constant-period interrupt function.

The RTCC0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-4. Format of Real-time Clock Control Register 0 (RTCC0)

Address: FFF9DH After reset: 00H R/W

Symbol	<7>	6	<5>	4	3	2	1	0
RTCC0	RTCE	0	RCLOE1	0	AMPM	CT2	CT1	CT0

RTCE	Real-time clock operation control
0	Stops counter operation.
1	Starts counter operation.

RCLOE1	RTC1HZ pin output control
0	Disables output of the RTC1HZ pin (1 Hz).
1	Enables output of the RTC1HZ pin (1 Hz).

AMPM	Selection of 12-/24-hour system
0	12-hour system (a.m. and p.m. are displayed.)
1	24-hour system
- Rewrite the AMPM bit value after setting the RWAIT bit (bit 0 of real-time clock control register 1 (RTCC1)) to 1. If the AMPM bit value is changed, the values of the hour count register (HOUR) change according to the specified time system. - Table 7-2 shows the displayed time digits that are displayed.	

CT2	CT1	CT0	Constant-period interrupt (INTRTC) selection
0	0	0	Does not use constant-period interrupt function.
0	0	1	Once per 0.5 s (synchronized with second count up)
0	1	0	Once per 1 s (same time as second count up)
0	1	1	Once per 1 m (second 00 of every minute)
1	0	0	Once per 1 hour (minute 00 and second 00 of every hour)
1	0	1	Once per 1 day (hour 00, minute 00, and second 00 of every day)
1	1	×	Once per 1 month (Day 1, hour 00 a.m., minute 00, and second 00 of every month)
When changing the values of the CT2 to CT0 bits while the counter operates (RTCE = 1), rewrite the values of the CT2 to CT0 bits after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, after rewriting the values of the CT2 to CT0 bits, enable interrupt servicing after clearing the RIFG and RTCIF flags.			

Caution Do not change the value of the RTCLOE1 bit when RTCE = 1.

Remark ×: don't care

7.3.4 Real-time clock control register 1 (RTCC1)

The RTCC1 register is an 8-bit register that is used to control the alarm interrupt function and the wait time of the counter.

The RTCC1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-5. Format of Real-time Clock Control Register 1 (RTCC1) (1/2)

Address: FFF9EH After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	0	WAFG	RIFG	0	RWST	RWAIT

WALE	Alarm operation control
0	Match operation is invalid.
1	Match operation is valid.
When setting a value to the WALE bit while the counter operates (RTCE = 1) and WALIE = 1, rewrite the WALE bit after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG and RTCIF flags after rewriting the WALE bit. When setting each alarm register (WALIE flag of real-time clock control register 1 (RTCC1), the alarm minute register (ALARMWM), the alarm hour register (ALARMWH), and the alarm week register (ALARMWW)), set match operation to be invalid ("0") for the WALE bit.	

WALIE	Control of alarm interrupt (INTRTC) function operation
0	Does not generate interrupt on matching of alarm.
1	Generates interrupt on matching of alarm.

WAFG	Alarm detection status flag
0	Alarm mismatch
1	Detection of matching of alarm
This is a status flag that indicates detection of matching with the alarm. It is valid only when WALE = 1 and is set to "1" one clock (32.768 kHz) after matching of the alarm is detected. This flag is cleared when "0" is written to it. Writing "1" to it is invalid.	

RIFG	Constant-period interrupt status flag
0	Constant-period interrupt is not generated.
1	Constant-period interrupt is generated.
This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to "1". This flag is cleared when "0" is written to it. Writing "1" to it is invalid.	

Figure 7-5. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

Address: FFF9EH After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	0	WAFG	RIFG	0	RWST	RWAIT

RWST	Wait status flag of real-time clock
0	Counter is operating.
1	Mode to read or write counter value
This status flag indicates whether the setting of the RWAIT bit is valid. Before reading or writing the counter value, confirm that the value of this flag is 1.	

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
This bit controls the operation of the counter. Be sure to write "1" to it to read or write the counter value. As the counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When RWAIT = 1, it takes up to 1 clock (f_{RTC}) until the counter value can be read or written (RWST = 1). When the counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up. However, when it wrote a value to second count register, it will not keep the overflow event.	

Caution If writing is performed to the RTCC1 register with a 1-bit manipulation instruction, the RIFG flag and WAFG flag may be cleared. Therefore, to perform writing to the RTCC1 register, be sure to use an 8-bit manipulation instruction. To prevent the RIFG flag and WAFG flag from being cleared during writing, disable writing by setting 1 to the corresponding bit. If the RIFG flag and WAFG flag are not used and the value may be changed, the RTCC1 register may be written by using a 1-bit manipulation instruction.

Remark Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

7.3.5 Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds. It counts up when the counter (16-bit) overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 59 to this register in BCD code.

The SEC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-6. Format of Second Count Register (SEC)

Address: FFF92H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SEC	0	SEC40	SEC20	SEC10	SEC8	SEC4	SEC2	SEC1

Caution When it reads or writes from/to the register while the counter is in operation ($RTCE = 1$), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

7.3.6 Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes. It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code.

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-7. Format of Minute Count Register (MIN)

Address: FFF93H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
MIN	0	MIN40	MIN20	MIN10	MIN8	MIN4	MIN2	MIN1

Caution When it reads or writes from/to the register while the counter is in operation ($RTCE = 1$), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

7.3.7 Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time clock control register 0 (RTCC0).

If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system.

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit is set to 1 after reset.

Figure 7-8. Format of Hour Count Register (HOUR)

Address: FFF94H After reset: 12H R/W

Symbol	7	6	5	4	3	2	1	0
HOUR	0	0	HOUR20	HOUR10	HOUR8	HOUR4	HOUR2	HOUR1

- Cautions**
1. Bit 5 (HOUR20) of the HOUR register indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).
 2. When it reads or writes from/to the register while the counter is in operation (RTCE = 1), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

Table 7-2 shows the relationship between the setting value of the AMPM bit, the hour count register (HOUR) value, and time.

Table 7-2. Displayed Time Digits

24-Hour Display (AMPM = 1)		12-Hour Display (AMPM = 1)	
Time	HOUR Register	Time	HOUR Register
0	00H	12 a.m.	12H
1	01H	1 a.m.	01H
2	02H	2 a.m.	02H
3	03H	3 a.m.	03H
4	04H	4 a.m.	04H
5	05H	5 a.m.	05H
6	06H	6 a.m.	06H
7	07H	7 a.m.	07H
8	08H	8 a.m.	08H
9	09H	9 a.m.	09H
10	10H	10 a.m.	10H
11	11H	11 a.m.	11H
12	12H	12 p.m.	32H
13	13H	1 p.m.	21H
14	14H	2 p.m.	22H
15	15H	3 p.m.	23H
16	16H	4 p.m.	24H
17	17H	5 p.m.	25H
18	18H	6 p.m.	26H
19	19H	7 p.m.	27H
20	20H	8 p.m.	28H
21	21H	9 p.m.	29H
22	22H	10 p.m.	30H
23	23H	11 p.m.	31H

The HOUR register value is set to 12-hour display when the AMPM bit is “0” and to 24-hour display when the AMPM bit is “1”.

In 12-hour display, the fifth bit of the HOUR register displays 0 for AM and 1 for PM.

7.3.8 Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.

It counts up when the hour counter overflows.

This counter counts as follows.

- 01 to 31 (January, March, May, July, August, October, December)
- 01 to 30 (April, June, September, November)
- 01 to 29 (February, leap year)
- 01 to 28 (February, normal year)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code.

The DAY register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Figure 7-9. Format of Day Count Register (DAY)

Address: FFF96H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
DAY	0	0	DAY20	DAY10	DAY8	DAY4	DAY2	DAY1

Caution When it reads or writes from/to the register while the counter is in operation ($RTCE = 1$), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

7.3.9 Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays. It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 06 to this register in BCD code.

The WEEK register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-10. Format of Week Count Register (WEEK)

Address: FFF95H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
WEEK	0	0	0	0	0	WEEK4	WEEK2	WEEK1

- Cautions** 1. The value corresponding to the month count register (MONTH) or the day count register (DAY) is not stored in the week count register (WEEK) automatically. After reset release, set the week count register as follow.

Day	WEEK
Sunday	00H
Monday	01H
Tuesday	02H
Wednesday	03H
Thursday	04H
Friday	05H
Saturday	06H

2. When it reads or writes from/to the register while the counter is in operation (RTCE = 1), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

7.3.10 Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months. It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code.

The MONTH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Figure 7-11. Format of Month Count Register (MONTH)

Address: FFF97H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
MONTH	0	0	0	MONTH10	MONTH8	MONTH4	MONTH2	MONTH1

Caution When it reads or writes from/to the register while the counter is in operation (RTCE = 1), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

7.3.11 Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years. It counts up when the month count register (MONTH) overflows.

Values 00, 04, 08, ..., 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the MONTH register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code.

The YEAR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-12. Format of Year Count Register (YEAR)

Address: FFF98H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
YEAR	YEAR80	YEAR40	YEAR20	YEAR10	YEAR8	YEAR4	YEAR2	YEAR1

Caution When it reads or writes from/to the register while the counter is in operation (RTCE = 1), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

7.3.12 Watch error correction register (SUBCUD)

This register is used to correct the watch with high accuracy when it is slow or fast by changing the value that overflows from the counter (16-bit) to the second count register (SEC) (reference value: 7FFFH).

The SUBCUD register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-13. Format of Watch Error Correction Register (SUBCUD)

Address: FFF99H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SUBCUD	DEV	F6	F5	F4	F3	F2	F1	F0

DEV	Setting of watch error correction timing
0	Corrects watch error when the second digits are at 00, 20, or 40 (every 20 seconds).
1	Corrects watch error only when the second digits are at 00 (every 60 seconds).
Writing to the SUBCUD register at the following timing is prohibited.	
- When DEV = 0 is set: For a period of SEC = 00H, 20H, 40H - When DEV = 1 is set: For a period of SEC = 00H	

F6	Setting of watch error correction value
0	Increases by $\{(F5, F4, F3, F2, F1, F0) - 1\} \times 2$.
1	Decreases by $\{((F5, F4, F3, F2, F1, F0) + 1) \times 2\}$.
When (F6, F5, F4, F3, F2, F1, F0) = (*, 0, 0, 0, 0, 0, *), the watch error is not corrected. * is 0 or 1.	
/F5 to /F0 are the inverted values of the corresponding bits (000011 when 111100).	
Range of correction value: (when F6 = 0) 2, 4, 6, 8, ..., 120, 122, 124	
(when F6 = 1) -2, -4, -6, -8, ..., -120, -122, -124	

The range of value that can be corrected by using the watch error correction register (SUBCUD) is shown below.

	DEV = 0 (correction every 20 seconds)	DEV = 1 (correction every 60 seconds)
Correctable range	-189.2 ppm to 189.2 ppm	-63.1 ppm to 63.1 ppm
Maximum excludes quantization error	± 1.53 ppm	± 0.51 ppm
Minimum resolution	± 3.05 ppm	± 1.02 ppm

Remark If a correctable range is -63.1 ppm or lower and 63.1 ppm or higher, set 0 to DEV.

7.3.13 Alarm minute register (ALARMWM)

This register is used to set minutes of alarm.

The ALARMWM register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Caution Set a decimal value of 00 to 59 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

Figure 7-14. Format of Alarm Minute Register (ALARMWM)

Address: FFF9AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWM	0	WM40	WM20	WM10	WM8	WM4	WM2	WM1

7.3.14 Alarm hour register (ALARMWH)

This register is used to set hours of alarm.

The ALARMWH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit is set to 1 after reset.

Caution Set a decimal value of 00 to 23, 01 to 12, or 21 to 32 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

Figure 7-15. Format of Alarm Hour Register (ALARMWH)

Address: FFF9BH After reset: 12H R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWH	0	0	WH20	WH10	WH8	WH4	WH2	WH1

Caution Bit 5 (WH20) of the ALARMWH register indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

7.3.15 Alarm week register (ALARMWW)

This register is used to set date of alarm.

The ALARMWW register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-16. Format of Alarm Week Register (ALARMWW)

Address: FFF9CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWW	0	WW6	WW5	WW4	WW3	WW2	WW1	WW0

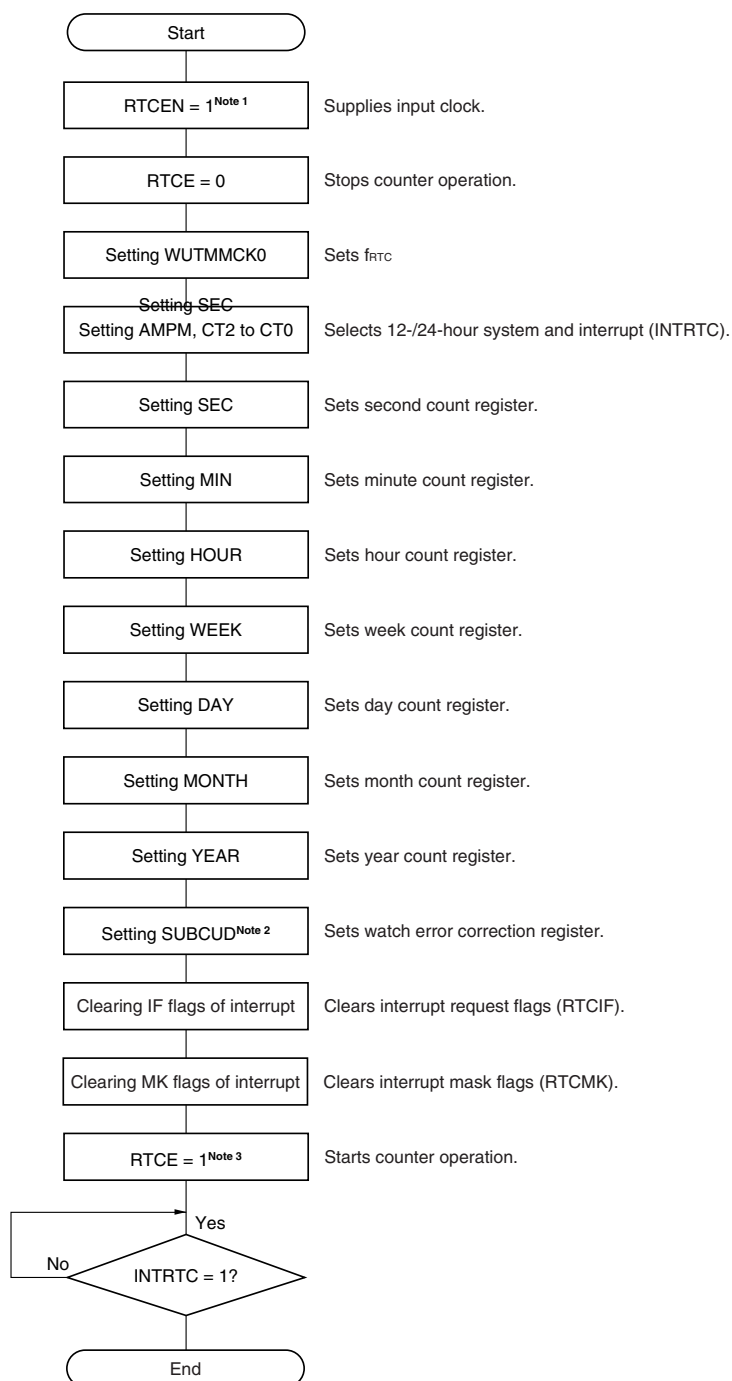
Here is an example of setting the alarm.

Time of Alarm	Day							12-Hour Display				24-Hour Display			
	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday	Hour 10	Hour 1	Minute 10	Minute 1	Hour 10	Hour 1	Minute 10	Minute 1
	W W 0	W W 1	W W 2	W W 3	W W 4	W W 5	W W 6								
Every day, 0:00 a.m.	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
Every day, 1:30 a.m.	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
Every day, 11:59 a.m.	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
Monday through Friday, 0:00 p.m.	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
Sunday, 1:30 p.m.	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
Monday, Wednesday, Friday, 11:59 p.m.	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

7.4 Real-time Clock Operation

7.4.1 Starting operation of real-time clock

Figure 7-17. Procedure for Starting Operation of Real-time Clock



Notes 1. First set the `RTCEN` bit to 1, while oscillation of the input clock (`fRTC`) is stable.

2. Set up the `SUBCUD` register only if the watch error must be corrected. For details about how to calculate the correction value, see **7.4.6 Example of watch error correction of real-time clock**.

3. Confirm the procedure described in **7.4.2 Shifting to HALT/STOP mode after starting operation** when shifting to HALT/STOP mode without waiting for `INTRTC = 1` after `RTCE = 1`.

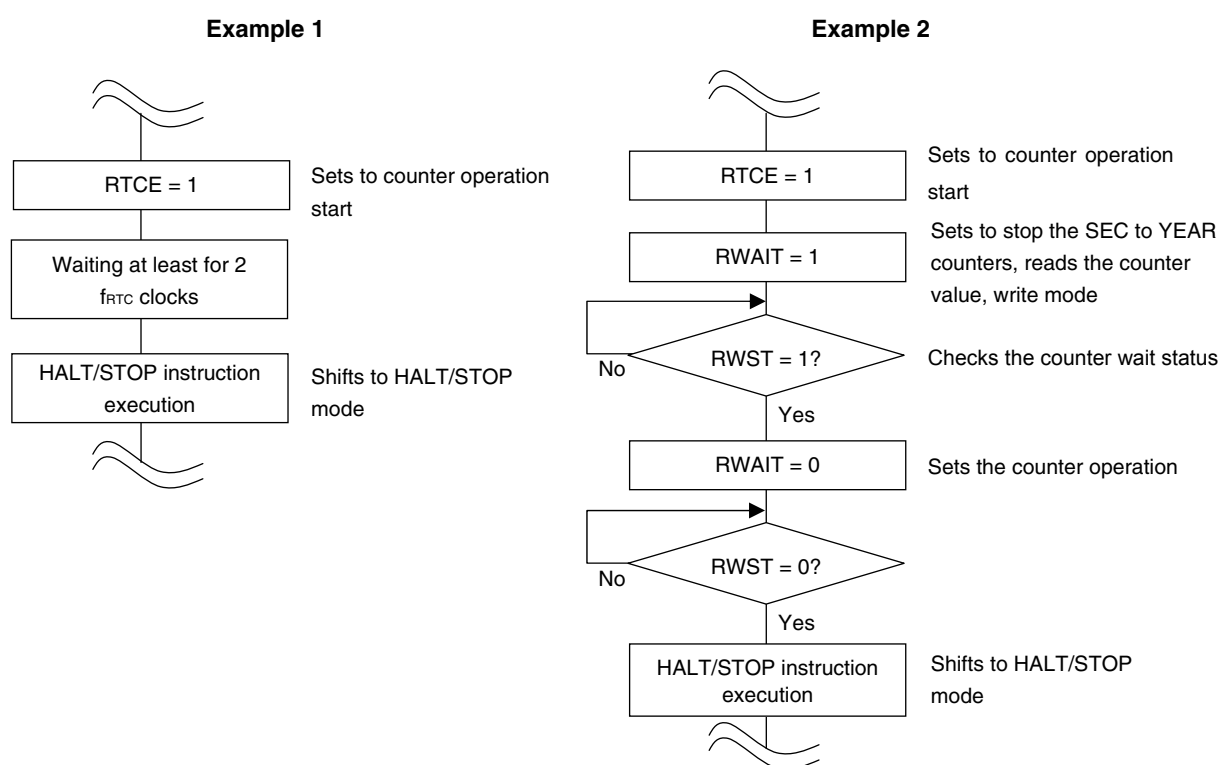
<R> 7.4.2 Shifting to HALT/STOP mode after starting operation

Perform one of the following processing when shifting to HALT/STOP mode immediately after setting the RTCE bit to 1.

However, after setting the RTCE bit to 1, this processing is not required when shifting to HALT/STOP mode after the INTRTC interrupt has occurred.

- Shifting to HALT/STOP mode when at least two input clocks (f_{RTC}) have elapsed after setting the RTCE bit to 1 (see **Figure 7-18, Example 1**).
- Checking by polling the RWST bit to become 1, after setting the RTCE bit to 1 and then setting the RWAIT bit to 1. Afterward, setting the RWAIT bit to 0 and shifting to HALT/STOP mode after checking again by polling that the RWST bit has become 0 (see **Figure 7-18, Example 2**).

Figure 7-18. Procedure for Shifting to HALT/STOP Mode After Setting RTCE bit to 1

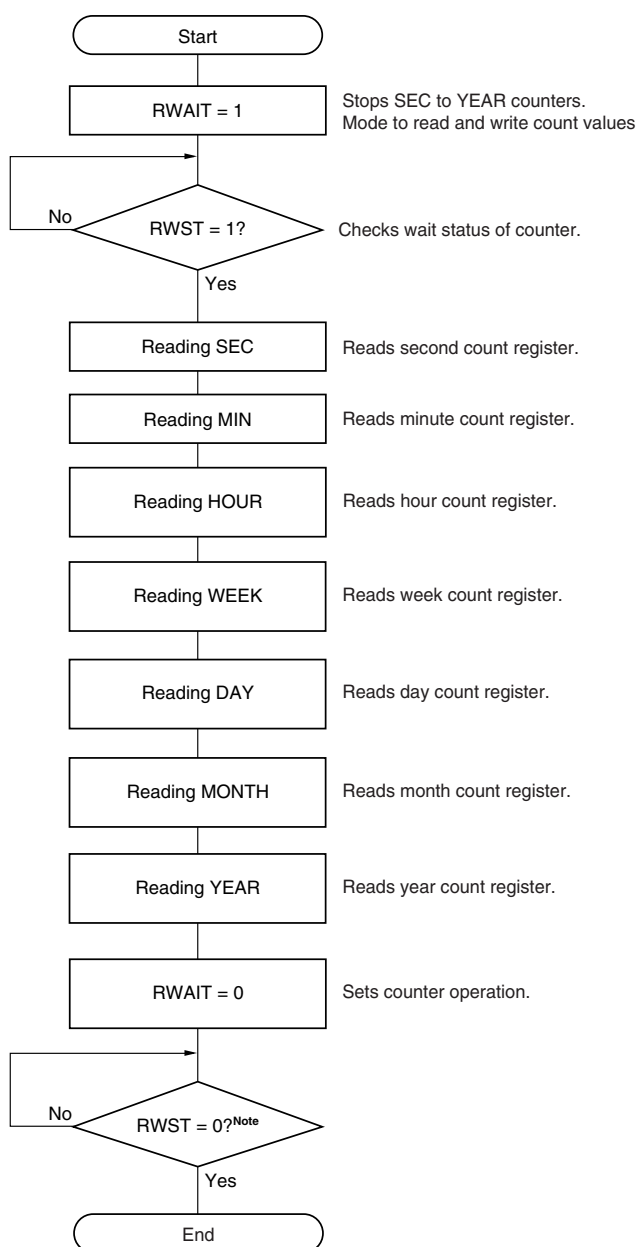


7.4.3 Reading/writing real-time clock

Read or write the counter after setting 1 to RWAIT first.

Set RWAIT to 0 after completion of reading or writing the counter.

Figure 7-19. Procedure for Reading Real-time Clock



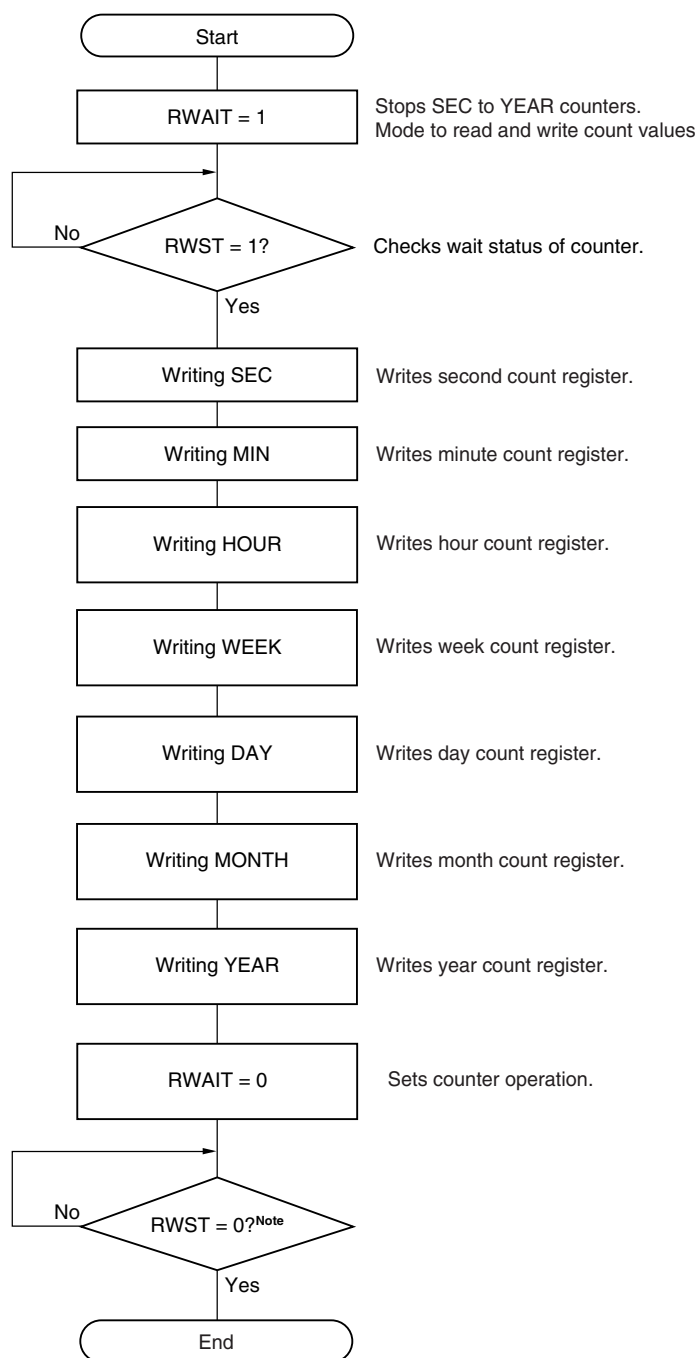
Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence.

All the registers do not have to read and only some registers may be read.

Figure 7-20. Procedure for Writing Real-time Clock



Note Be sure to confirm that RWST = 0 before setting STOP mode.

Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.

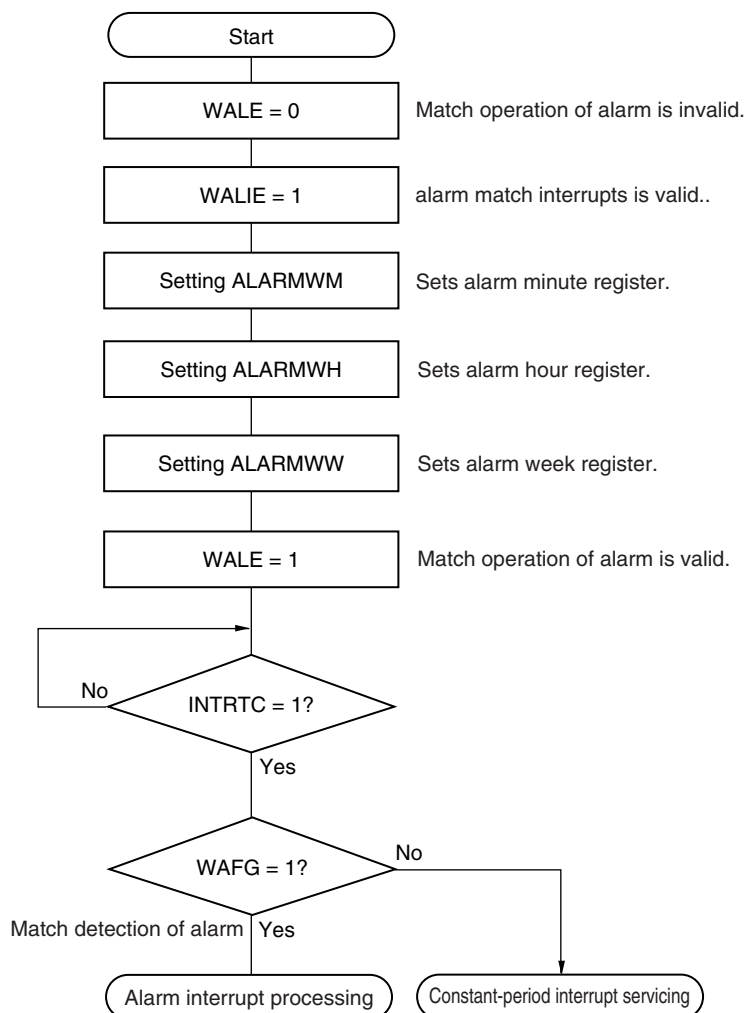
Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence.

All the registers do not have to be set and only some registers may be written.

7.4.4 Setting alarm of real-time clock

Set time of alarm after setting 0 to WALE (alarm operation invalid.) first.

Figure 7-21. Alarm processing Procedure

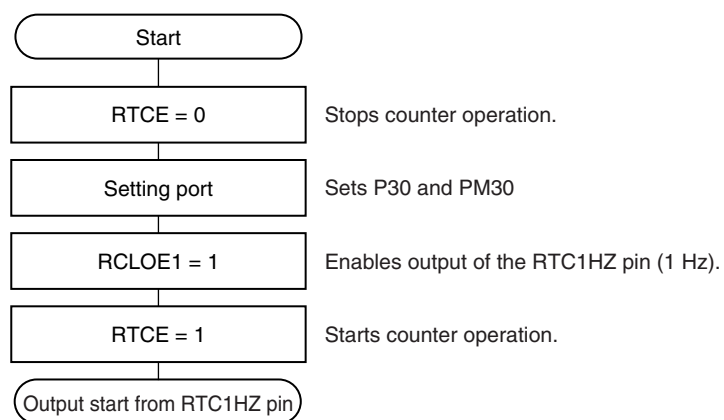


Remarks 1. The alarm week register (ALARMWW), alarm hour register (ALARMWH), and alarm week register (ALARMWW) may be written in any sequence.

- Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

7.4.5 1 Hz output of real-time clock

Figure 7-22. 1 Hz Output Setting Procedure



Caution First set the RTCEN bit to 1, while oscillation of the input clock (f_{SUB}) is stable.

7.4.6 Example of watch error correction of real-time clock

The watch can be corrected with high accuracy when it is slow or fast, by setting a value to the watch error correction register.

Example of calculating the correction value

The correction value used when correcting the count value of the counter (16-bit) is calculated by using the following expression.

Set the DEV bit to 0 when the correction range is –63.1 ppm or less, or 63.1 ppm or more.

(When DEV = 0)

$$\text{Correction value}^{\text{Note}} = \text{Number of correction counts in 1 minute} \div 3 = (\text{Oscillation frequency} \div \text{Target frequency} - 1) \times 32768 \times 60 \div 3$$

(When DEV = 1)

$$\text{Correction value}^{\text{Note}} = \text{Number of correction counts in 1 minute} = (\text{Oscillation frequency} \div \text{Target frequency} - 1) \times 32768 \times 60$$

Note The correction value is the watch error correction value calculated by using bits 6 to 0 of the watch error correction register (SUBCUD).

(When F6 = 0) Correction value = $\{(F5, F4, F3, F2, F1, F0) - 1\} \times 2$

(When F6 = 1) Correction value = $-\{(/F5, /F4, /F3, /F2, /F1, /F0) + 1\} \times 2$

When (F6, F5, F4, F3, F2, F1, F0) is (*, 0, 0, 0, 0, 0, *), watch error correction is not performed. “*” is 0 or 1. /F5 to /F0 are bit-inverted values (000011 when 111100).

- Remarks**
1. The correction value is 2, 4, 6, 8, ... 120, 122, 124 or –2, –4, –6, –8, ... –120, –122, –124.
 2. The oscillation frequency is the input clock (f_{RTC}).
It can be calculated from the output frequency of the RTC1HZ pin $\times$ 32768 when the watch error correction register is set to its initial value (00H).
 3. The target frequency is the frequency resulting after correction performed by using the watch error correction register.

Correction example

Example of correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm)

[Measuring the oscillation frequency]

The oscillation frequency^{Note} of each product is measured by outputting about 1 Hz from the RTC1HZ pin when the watch error correction register (SUBCUD) is set to its initial value (00H).

Note See **7.4.5 1 Hz output of real-time clock** for the setting procedure of outputting about 1 Hz from the RTC1HZ pin.

[Calculating the correction value]

(When the output frequency from the RTCCL pin is 0.9999817 Hz)

Oscillation frequency = $32768 \times 0.9999817 \approx 32767.4$ Hz

Assume the target frequency to be 32768 Hz (32767.4 Hz + 18.3 ppm) and DEV to be 1.

The expression for calculating the correction value when DEV is 1 is applied.

$$\begin{aligned} \text{Correction value} &= \text{Number of correction counts in 1 minute} \\ &= (\text{Oscillation frequency} \div \text{Target frequency} - 1) \times 32768 \times 60 \\ &= (32767.4 \div 32768 - 1) \times 32768 \times 60 \\ &= -36 \end{aligned}$$

[Calculating the values to be set to (F6 to F0)]

(When the correction value is -36)

If the correction value is 0 or less (when quickening), assume F6 to be 1.

Calculate (F5, F4, F3, F2, F1, F0) from the correction value.

$$\begin{aligned} -\{(\text{F5}, \text{F4}, \text{F3}, \text{F2}, \text{F1}, \text{F0}) - 1\} \times 2 &= -36 \\ (\text{F5}, \text{F4}, \text{F3}, \text{F2}, \text{F1}, \text{F0}) &= 17 \\ (\text{F5}, \text{F4}, \text{F3}, \text{F2}, \text{F1}, \text{F0}) &= (0, 1, 0, 0, 0, 1) \\ (\text{F5}, \text{F4}, \text{F3}, \text{F2}, \text{F1}, \text{F0}) &= (1, 0, 1, 1, 1, 0) \end{aligned}$$

Consequently, when correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm), setting the correction register such that DEV is 1 and the correction value is -36 (bits 6 to 0 of the SUBCUD register: 1101110) results in 32768 Hz (0 ppm).

Figure 7-23 shows the operation when (DEV, F6, F5, F4, F3, F2, F1, F0) is (1, 1, 1, 0, 1, 1, 1, 0).

CHAPTER 8 12-BIT INTERVAL TIMER

8.1 Functions of 12-bit Interval Timer

An interrupt (INTIT) is generated at any previously specified time interval. It can be utilized for wakeup from STOP mode and triggering an A/D converter's SNOOZE mode.

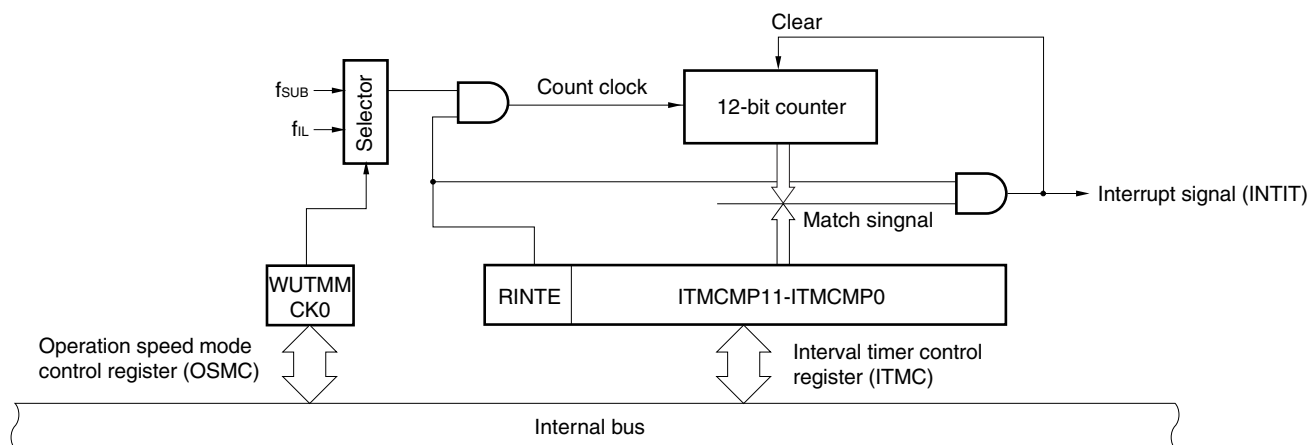
8.2 Configuration of 12-bit Interval Timer

The interval timer includes the following hardware.

Table 8-1. Configuration of 12-bit Interval Timer

Item	Configuration
Counter	12-bit counter
Control registers	Peripheral enable register 0 (PER0)
	Operation speed mode control register (OSMC)
	Interval timer control register (ITMC)

Figure 8-1. Block Diagram of 12-bit Interval Timer



8.3 Registers Controlling 12-bit Interval Timer

The 12-bit interval timer is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Operation speed mode control register (OSMC)
- Interval timer control register (ITMC)

8.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the 12-bit interval timer is used, be sure to set bit 7 (RTCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 8-2. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	IICA0EN	SAU1EN Note	SAU0EN	0	TAU0EN

RTCEN	Control of real-time clock (RTC) and 12-bit interval timer input clock supply
0	Stops input clock supply. • SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be written. • The real-time clock (RTC) and 12-bit interval timer are in the reset status.
1	Enables input clock supply. • SFR used by the real-time clock (RTC) and 12-bit interval timer can be read and written.

Note 32, 48, and 64-pin products only.

- Cautions**
1. When using the 12-bit interval timer, first set the RTCEN bit to 1, while oscillation of the input clock (f_{RTC}) is stable. If RTCEN = 0, writing to a control register of the real-time clock or 12-bit interval timer is ignored, and, even if the register is read, only the default value is read.
 2. Clock supply to peripheral functions other than the real-time clock and 12-bit interval timer can be stopped in STOP mode or HALT mode when the subsystem clock is used, by setting the RTCLPC bit of the operation speed mode control register (OSMC) to 1. In this case, set the RTCEN bit of the PER0 register to 1 and the other bits (bits 0 to 6) to 0.
 3. Be sure to clear the following bits to 0.
 - 25-pin products: bits 1, 3, 6
 - 32, 48, 64-pin products: bits 1, 6

8.3.2 Operation speed mode control register (OSMC)

The WUTMMCK0 bit can be used to select the 12-bit interval timer operation clock.

In addition, by stopping clock functions that are unnecessary, the RTCLPC bit can be used to reduce power consumption. For details about setting the RTCLPC bit, see **CHAPTER 5 CLOCK GENERATOR**.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 8-3. Format of Operation Speed Mode Control Register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

WUTMMCK0	Selection of operation clock for real-time clock and 12-bit interval timer.
0	Subsystem clock (f_{SUB})
1	Low-speed on-chip oscillator clock (f_{IL})

8.3.3 Interval timer control register (ITMC)

This register is used to set up the starting and stopping of the 12-bit interval timer operation and to specify the timer compare value.

The ITMC register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0FFFH.

Figure 8-4. Format of 12-bit Interval Timer Control Register (ITMC)

Address: FFF90H After reset: 0FFFH R/W

Symbol	15	14	13	12	11 to 0
ITMC	RINTE	0	0	0	ITCMP11 to ITCMP0

RINTE	12-bit interval timer operation control
0	Count operation stopped (count clear)
1	Count operation started

ITCMP11 to ITCMP0	Specification of the 12-bit interval timer compare value
001H	These bits generate an interrupt at the fixed cycle (count clock cycles x (ITCMP setting + 1)).
•	
•	
•	
FFFH	Setting prohibit
000H	

Example interrupt cycles when 001H or FFFH is specified for ITCMP11 to ITCMP0	
- ITCMP11 to ITCMP0 = 001H, count clock: when $f_{SUB} = 32.768 \text{ kHz}$ $1/32.768 \text{ [kHz]} \times (1 + 1) = 0.06103515625 \text{ [ms]} \cong 61.03 \text{ [}\mu\text{s]}$ - ITCMP11 to ITCMP0 = FFFH, count clock: when $f_{SUB} = 32.768 \text{ kHz}$ $1/32.768 \text{ [kHz]} \times (4095 + 1) = 125 \text{ [ms]}$	

- Cautions**
- Before changing the RINTE bit from 1 to 0, use the interrupt mask flag register to disable the INTIT interrupt servicing. When the operation starts (from 0 to 1) again, clear the ITIF flag, and then enable the interrupt servicing.
 - The value read from the RINTE bit is applied one count clock cycle after setting the RINTE bit.
 - When setting the RINTE bit to start operation of the counter after returning from a standby mode and then shifting to a standby mode again, either confirm that the value written to the RINTE bit has been applied, or make sure that at least one count clock cycle elapses between returning from a standby mode and shifting to a standby mode again.
 - Only change the setting of the ITCMP11 to ITCMP0 bits when RINTE = 0.
However, it is possible to change the settings of the ITCMP11 to ITCMP0 bits at the same time as when changing RINTE from 0 to 1 or 1 to 0.

8.4 12-bit Interval Timer Operation

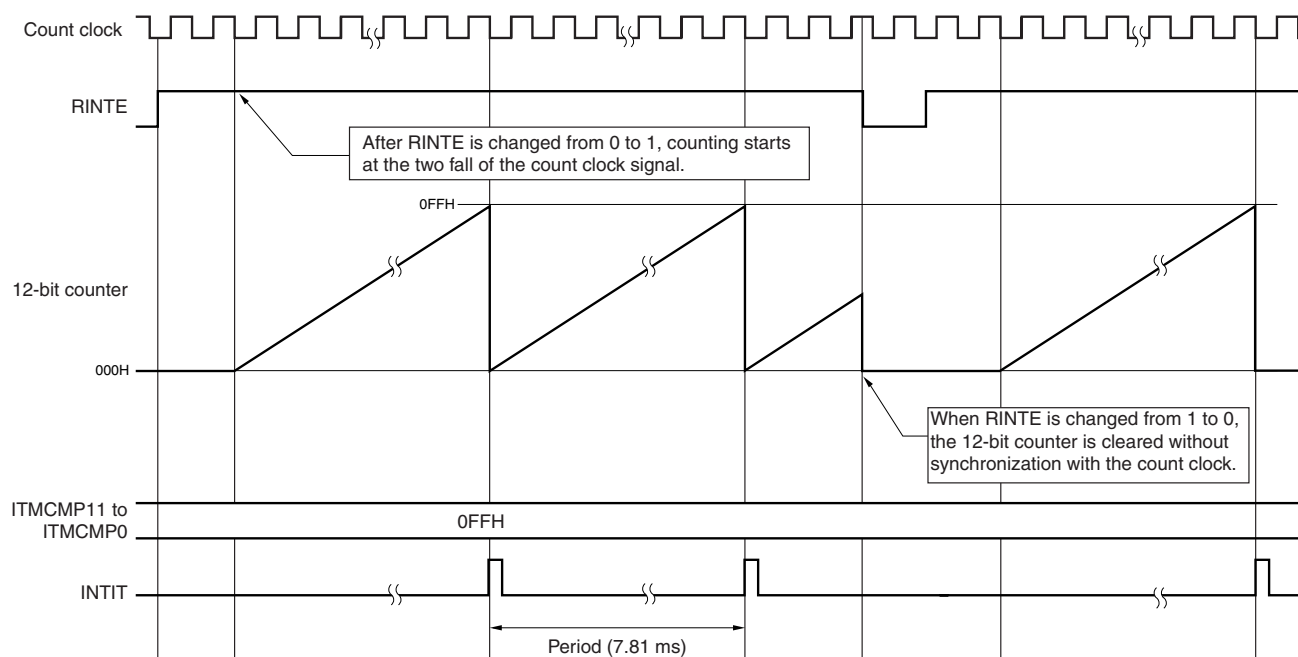
The count value specified for the ITCMP11 to ITCMP0 bits is used as an interval to operate an 12-bit interval timer that repeatedly generates interrupt requests (INTIT).

When the RINTE bit is set to 1, the 12-bit counter starts counting.

When the 12-bit counter value matches the value specified for the ITCMP11 to ITCMP0 bits, the 12-bit counter value is cleared to 0, counting continues, and an interrupt request signal (INTIT) is generated at the same time.

The basic operation of the 12-bit interval timer is as follows.

<R> **Figure 8-5. 12-bit Interval Timer Operation Timing (ITCMP11 to ITCMP0 = 0FFH, count clock: $f_{SUB} = 32.768$ kHz)**

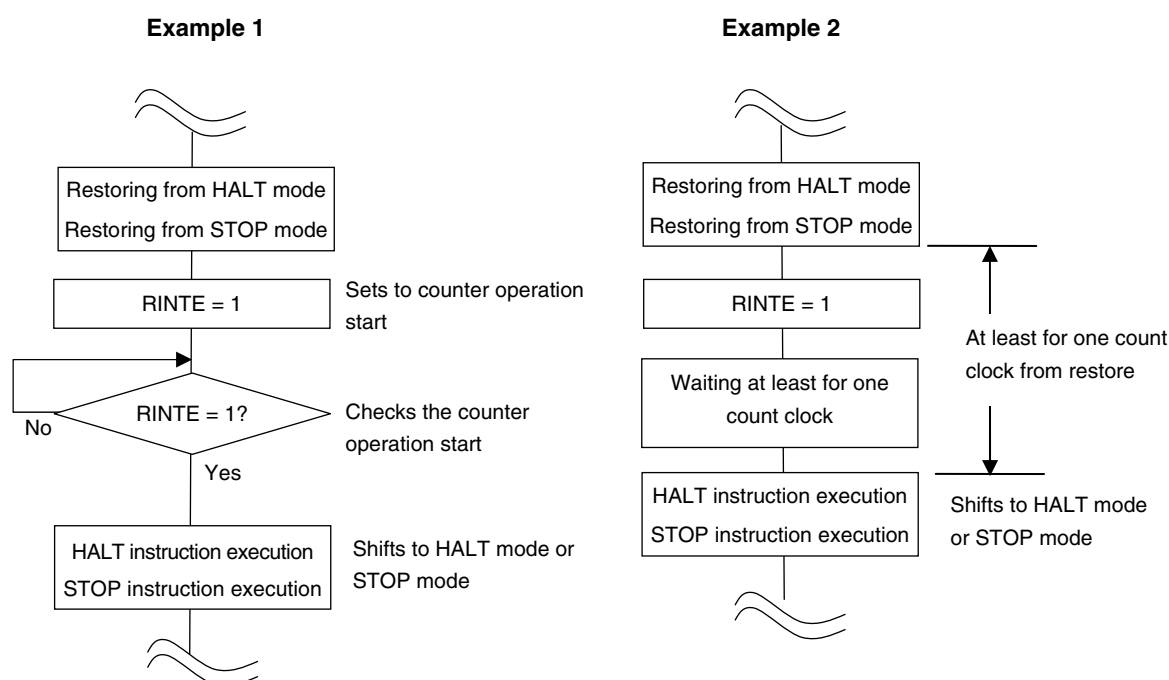


8.4.1 Starting counter operation after returning from HALT or STOP mode and then shifting to HALT or STOP mode again

When setting the RINTE bit to 1 to start operation of the counter after returning from the HALT or STOP mode and then shifting to the HALT or STOP mode again, either confirm that the value written to the RINTE bit (1) has been applied, or make sure that at least one count clock cycle elapses between returning from HALT or STOP mode and shifting to HALT or STOP mode again.

- After setting RINTE to 1, confirm that the RINTE bit value is actually 1 by polling the bit, and then shift to the HALT or STOP mode (see Example 1 in Figure 8-6).
- After setting RINTE to 1, wait for at least one cycle of the count clock to elapse before shifting to the HALT or STOP mode (see Example 2 in Figure 8-6).

Figure 8-6. Shifting to HALT or STOP Mode after Setting RINTE to 1



CHAPTER 9 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER

The number of output pins of the clock output and buzzer output controllers differs, depending on the product.

Output pin	25-pin	32, 48, 64-pin
PCLBUZ0	√	√
PCLBUZ1	—	√

Caution Most of the descriptions in this chapter use the 64-pin as an example.

9.1 Functions of Clock Output/Buzzer Output Controller

The clock output controller is intended for carrier output during remote controlled transmission and clock output for supply to peripheral ICs.

Buzzer output is a function to output a square wave of buzzer frequency.

One pin can be used to output a clock or buzzer sound.

Two output pins, PCLBUZ0 and PCLBUZ1, are available.

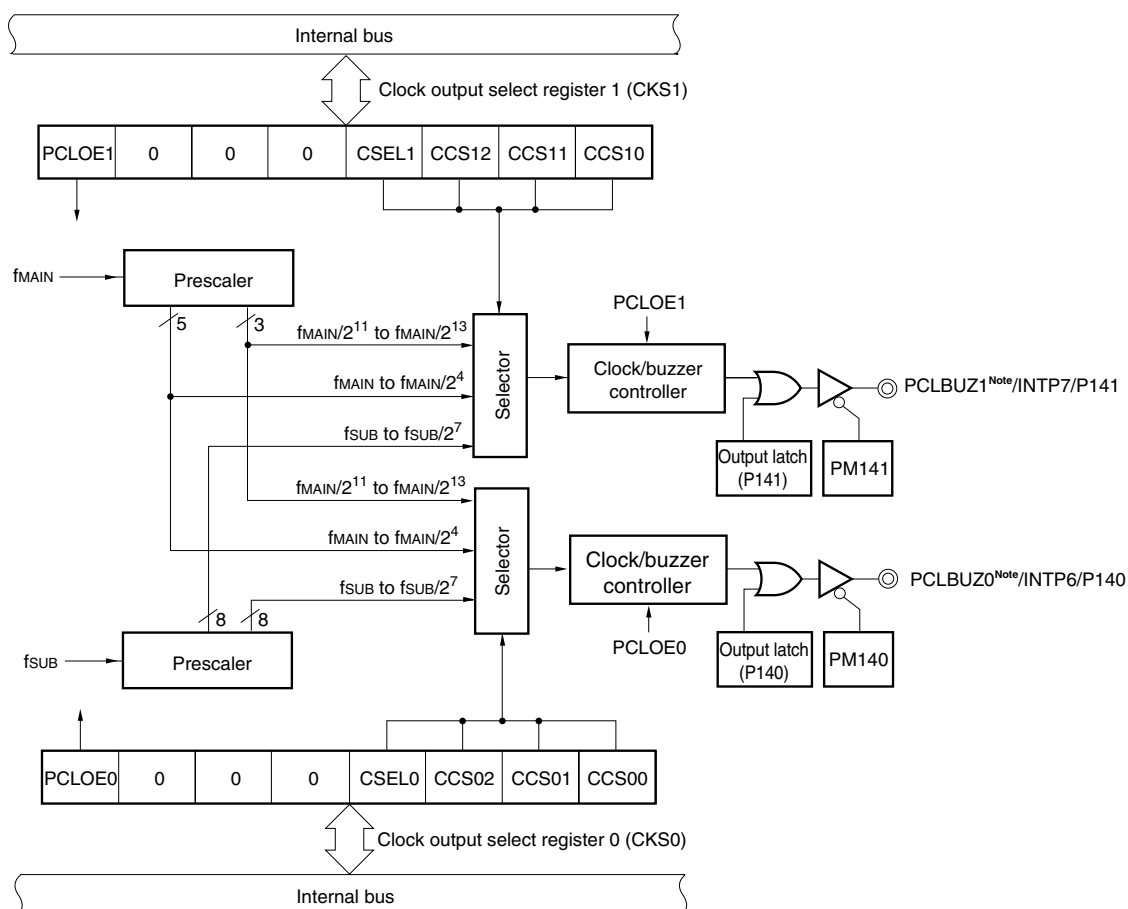
The PCLBUZn pin outputs a clock selected by clock output select register n (CKSn).

Figure 9-1 shows the block diagram of clock output/buzzer output controller.

<R> **Caution** The subsystem clock (f_{SUB}) cannot be output from the PCLBUZn pin if the system enters HALT mode while the CPU is operating on the subsystem clock (f_{SUB}) and the RTCLPC bit of the operation speed mode control register (OSMC) is 1.

Remark n = 0, 1

Figure 9-1. Block Diagram of Clock Output/Buzzer Output Controller



Note For output frequencies available from PCLBUZ0 and PCLBUZ1, refer to **29.4 AC Characteristics** and **30.4 AC Characteristics**.

Remark The clock output/buzzer output pins in above diagram shows the information of 64-pins products. In other cases, the name of pins, output latches (Pxx) and PMxx should be read differently (xx = 140 or 141).

9.2 Configuration of Clock Output/Buzzer Output Controller

The clock output/buzzer output controller includes the following hardware.

Table 9-1. Configuration of Clock Output/Buzzer Output Controller

Item	Configuration
Control registers	Clock output select registers n (CKSn) Port mode register 14 (PM14) Port register 14 (P14)

9.3 Registers Controlling Clock Output/Buzzer Output Controller

The following two registers are used to control the clock output/buzzer output controller.

- Clock output select registers n (CKSn)
- Port mode register 14 (PM14)

9.3.1 Clock output select registers n (CKSn)

These registers set output enable/disable for clock output or for the buzzer frequency output pin (PCLBUZn), and set the output clock.

Select the clock to be output from the PCLBUZn pin by using the CKSn register.

The CKSn register are set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 9-2. Format of Clock Output Select Register n (CKSn)

Address: FFFA5H (CKS0), FFFA6H (CKS1) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CKSn	PCLOEn	0	0	0	CSELn	CCSn2	CCSn1	CCSn0

PCLOEn	PCLBUZn pin output enable/disable specification
0	Output disable (default)
1	Output enable

CSELn	CCSn2	CCSn1	CCSn0	PCLBUZn pin output clock selection				
					f _{MAIN} = 5 MHz	f _{MAIN} = 10 MHz	f _{MAIN} = 20 MHz	f _{MAIN} = 32 MHz
0	0	0	0	f _{MAIN}	5 MHz	Setting prohibited ^{Note}	Setting prohibited ^{Note}	Setting prohibited ^{Note}
0	0	0	1	f _{MAIN} /2	2.5 MHz	5 MHz	Setting prohibited ^{Note}	Setting prohibited ^{Note}
0	0	1	0	f _{MAIN} /2 ²	1.25 MHz	2.5 MHz	5 MHz	8 MHz ^{Note}
0	0	1	1	f _{MAIN} /2 ³	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	f _{MAIN} /2 ⁴	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	f _{MAIN} /2 ¹¹	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
0	1	1	0	f _{MAIN} /2 ¹²	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
0	1	1	1	f _{MAIN} /2 ¹³	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	0	0	0	f _{SUB}	32.768 kHz			
1	0	0	1	f _{SUB} /2	16.384 kHz			
1	0	1	0	f _{SUB} /2 ²	8.192 kHz			
1	0	1	1	f _{SUB} /2 ³	4.096 kHz			
1	1	0	0	f _{SUB} /2 ⁴	2.048 kHz			
1	1	0	1	f _{SUB} /2 ⁵	1.024 kHz			
1	1	1	0	f _{SUB} /2 ⁶	512 Hz			
1	1	1	1	f _{SUB} /2 ⁷	256 Hz			

<R>

<R> **Note** Use the output clock within a range of 8 MHz. See 29.4 AC Characteristics and 30.4 AC Characteristics for details.

(Cautions and Remarks are listed on the next page.)

- Cautions**
1. Change the output clock after disabling clock output ($PCLOEn = 0$).
 2. To shift to STOP mode when the main system clock is selected ($CSELn = 0$), set $PCLOEn = 0$ before executing the STOP instruction. When the subsystem clock is selected ($CSELn = 1$), $PCLOEn = 1$ can be set because $RTCLPC$ of operation speed mode control register ($OSMC$) = 0 and the clock can be output in STOP mode.
 3. The subsystem clock (f_{SUB}) cannot be output from the $PCLBUZn$ pin if the system enters HALT mode while the CPU is operating on the subsystem clock (f_{SUB}) and the $RTCLPC$ bit of the operation speed mode control register ($OSMC$) is 1.

- Remarks**
1. $n = 0, 1$
 2. f_{MAIN} : Main system clock frequency
 f_{SUB} : Subsystem clock frequency

9.3.2 Port mode register 14 (PM14)

These registers set input/output of port in 1-bit units.

For example in 64-pin products, when using the P140/INTP6/PCLBUZ0 and P141/INTP7/PCLBUZ1 pins for clock output and buzzer output clear PM140 and PM141 bits and the output latches of P140 and P141 to 0.

The PM14 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark The clock output/buzzer output pins in above diagram shows the information of 64-pins products. In other cases, the name of pins, output latches (Pxx) and PMxx should be read differently (xx = 140 or 141).

Figure 9-3. Format of Port Mode Register 14 (PM14) (64-pin products)

Address:	FFF2EH	After reset:	FFH	R/W				
Symbol	7	6	5	4	3	2	1	0
PM14	1	1	1	1	1	1	PM141	PM140

PMmn	Pmn pin I/O mode selection (mn = 140, 141)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark For details of the port mode register other than 64-pin products, see **4. 3 Registers Controlling Port Function**.

9.4 Operations of Clock Output/Buzzer Output Controller

One pin can be used to output a clock or buzzer sound.

The PCLBUZ0 pin outputs a clock/buzzer selected by the clock output select register 0 (CKS0).

The PCLBUZ1 pin outputs a clock/buzzer selected by the clock output select register 1 (CKS1).

9.4.1 Operation as output pin

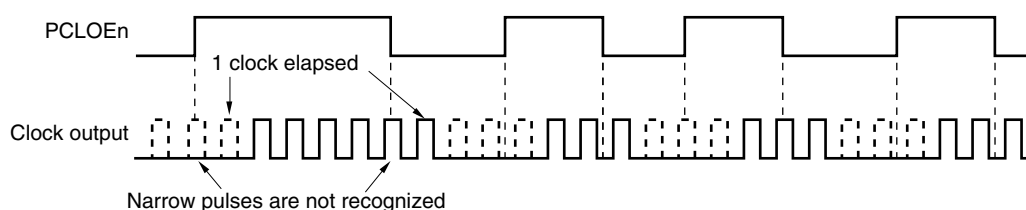
The PCLBUZn pin is output as the following procedure.

- <1> Select the output frequency with bits 0 to 3 (CCSn0 to CCSn2, CSELn) of the clock output select register (CKSn) of the PCLBUZn pin (output in disabled status).
- <2> Set bit 7 (PCLOEn) of the CKSn register to 1 to enable clock/buzzer output.

Remarks 1. The controller used for outputting the clock starts or stops outputting the clock one clock after enabling or disabling clock output (PCLOEn bit) is switched. At this time, pulses with a narrow width are not output. Figure 9-4 shows enabling or stopping output using the PCLOEn bit and the timing of outputting the clock.

2. n = 0, 1

Figure 9-4. Remote Control Output Application Example



<R> 9.5 Cautions of clock output/buzzer output controller

When the main system clock is selected for the PCLBUZn output (CSEL = 0), if STOP or HALT mode is entered within 1.5 main system clock cycles after the output is disabled (PCLOEn = 0), the PCLBUZn output width becomes shorter.

CHAPTER 10 WATCHDOG TIMER

10.1 Functions of Watchdog Timer

The watchdog timer operates on the low-speed on-chip oscillator clock.

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Program loop is detected in the following cases.

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than "ACH" is written to the WDTE register
- If data is written to the WDTE register during a window close period

When a reset occurs due to the watchdog timer, bit 4 (WDTRF) of the reset control flag register (RESF) is set to 1. For details of the RESF register, see **CHAPTER 19 RESET FUNCTION**.

<R> When $75\% \pm 1/2f_{IL}$ of the overflow time is reached, an interval interrupt can be generated.

10.2 Configuration of Watchdog Timer

The watchdog timer includes the following hardware.

Table 10-1. Configuration of Watchdog Timer

Item	Configuration
Control register	Watchdog timer enable register (WDTE)

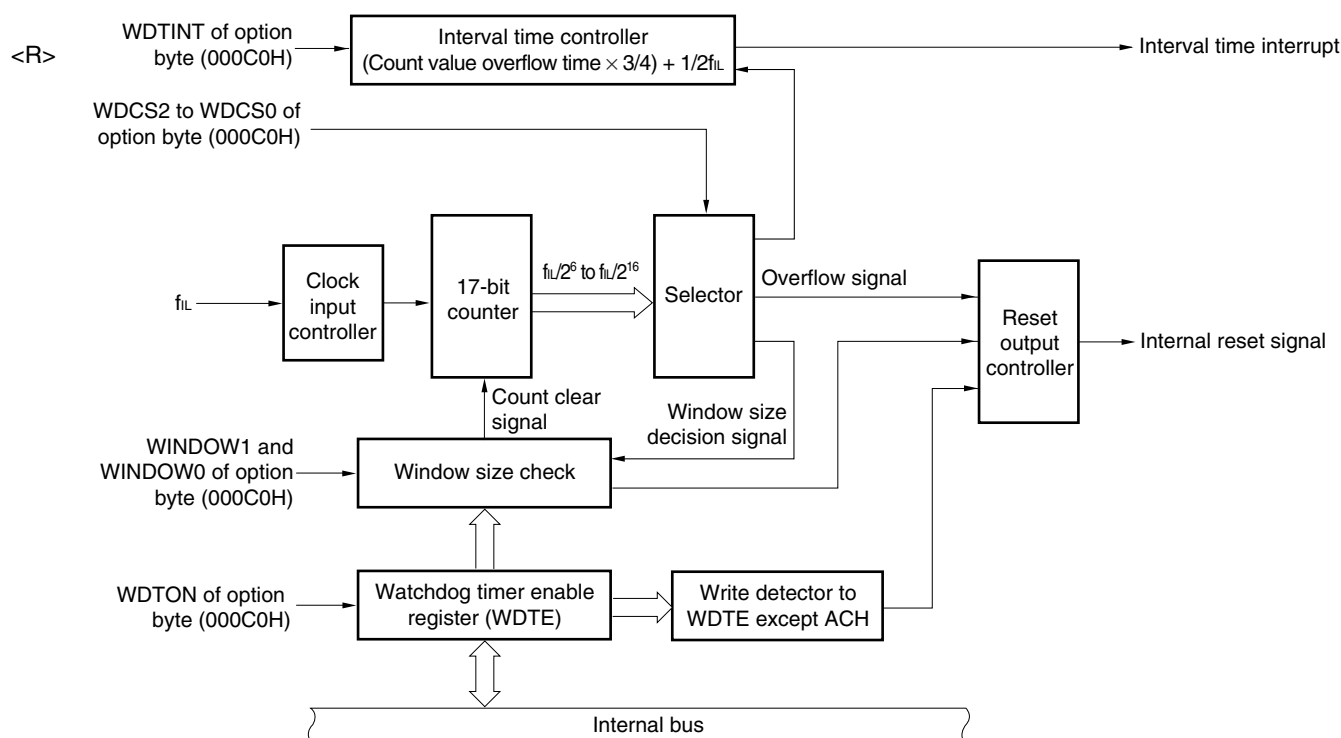
How the counter operation is controlled, overflow time, window open period, and interval interrupt are set by the option byte.

Table 10-2. Setting of Option Bytes and Watchdog Timer

Setting of Watchdog Timer	Option Byte (000C0H)
Watchdog timer interval interrupt	Bit 7 (WDTINT)
Window open period	Bits 6 and 5 (WINDOW1, WINDOW0)
Controlling counter operation of watchdog timer	Bit 4 (WDTON)
Overflow time of watchdog timer	Bits 3 to 1 (WDCS2 to WDCS0)
Controlling counter operation of watchdog timer (in HALT/STOP mode)	Bit 0 (WDSTBYON)

Remark For the option byte, see **CHAPTER 24 OPTION BYTE**.

Figure 10-1. Block Diagram of Watchdog Timer



10.3 Register Controlling Watchdog Timer

The watchdog timer is controlled by the watchdog timer enable register (WDTE).

10.3.1 Watchdog timer enable register (WDTE)

Writing “ACH” to the WDTE register clears the watchdog timer counter and starts counting again.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 9AH or 1AH^{Note}.

Figure 10-2. Format of Watchdog Timer Enable Register (WDTE)

Address: FFFABH	After reset: 9AH/1AH ^{Note}		R/W					
Symbol	7	6	5	4	3	2	1	0
WDTE								

Note The WDTE register reset value differs depending on the WDTON bit setting value of the option byte (000C0H). To operate watchdog timer, set the WDTON bit to 1.

WDTON Bit Setting Value	WDTE Register Reset Value
0 (watchdog timer count operation disabled)	1AH
1 (watchdog timer count operation enabled)	9AH

- Cautions**
1. If a value other than “ACH” is written to the WDTE register, an internal reset signal is generated.
 2. If a 1-bit memory manipulation instruction is executed for the WDTE register, an internal reset signal is generated.
 3. The value read from the WDTE register is 9AH/1AH (this differs from the written value (ACH)).

10.4 Operation of Watchdog Timer

10.4.1 Controlling operation of watchdog timer

1. When the watchdog timer is used, its operation is specified by the option byte (000C0H).
 - Enable counting operation of the watchdog timer by setting bit 4 (WDTON) of the option byte (000C0H) to 1 (the counter starts operating after a reset release) (for details, see **CHAPTER 24**).

WDTON	Watchdog Timer Counter
0	Counter operation disabled (counting stopped after reset)
1	Counter operation enabled (counting started after reset)

- Set an overflow time by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H) (for details, see **10.4.2** and **CHAPTER 24**).
 - Set a window open period by using bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (000C0H) (for details, see **10.4.3** and **CHAPTER 24**).
2. After a reset release, the watchdog timer starts counting.
 3. By writing “ACH” to the watchdog timer enable register (WDTE) after the watchdog timer starts counting and before the overflow time set by the option byte, the watchdog timer is cleared and starts counting again.
 4. After that, write the WDTE register the second time or later after a reset release during the window open period. If the WDTE register is written during a window close period, an internal reset signal is generated.
 5. If the overflow time expires without “ACH” written to the WDTE register, an internal reset signal is generated. An internal reset signal is generated in the following cases.
 - If a 1-bit manipulation instruction is executed on the WDTE register
 - If data other than “ACH” is written to the WDTE register

- Cautions**
1. When data is written to the watchdog timer enable register (WDTE) for the first time after reset release, the watchdog timer is cleared in any timing regardless of the window open time, as long as the register is written before the overflow time, and the watchdog timer starts counting again.
 2. If the watchdog timer is cleared by writing “ACH” to the WDTE register, the actual overflow time may be different from the overflow time set by the option byte by up to 2/f_{IL} seconds.
 3. The watchdog timer can be cleared immediately before the count value overflows.

Cautions 4. The operation of the watchdog timer in the HALT and STOP and SNOOZE modes differs as follows depending on the set value of bit 0 (WDSTBYON) of the option byte (000C0H).

	WDSTBYON = 0	WDSTBYON = 1
In HALT mode	Watchdog timer operation stops.	Watchdog timer operation continues.
In STOP mode		
In SNOOZE mode		

If WDSTBYON = 0, the watchdog timer resumes counting after the HALT or STOP mode is released. At this time, the counter is cleared to 0 and counting starts.

When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.

Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.

Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

10.4.2 Setting overflow time of watchdog timer

Set the overflow time of the watchdog timer by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H).

If an overflow occurs, an internal reset signal is generated. The present count is cleared and the watchdog timer starts counting again by writing "ACH" to the watchdog timer enable register (WDTE) during the window open period before the overflow time.

The following overflow times can be set.

Table 10-3. Setting of Overflow Time of Watchdog Timer

WDCS2	WDCS1	WDCS0	Overflow Time of Watchdog Timer (f _{IL} = 17.25 kHz (MAX.))
0	0	0	2 ⁶ /f _{IL} (3.71 ms)
0	0	1	2 ⁷ /f _{IL} (7.42 ms)
0	1	0	2 ⁸ /f _{IL} (14.84 ms)
0	1	1	2 ⁹ /f _{IL} (29.68 ms)
1	0	0	2 ¹¹ /f _{IL} (118.72 ms)
1	0	1	2 ¹³ /f _{IL} (474.90 ms)
1	1	0	2 ¹⁴ /f _{IL} (949.80 ms)
1	1	1	2 ¹⁶ /f _{IL} (3799.19 ms)

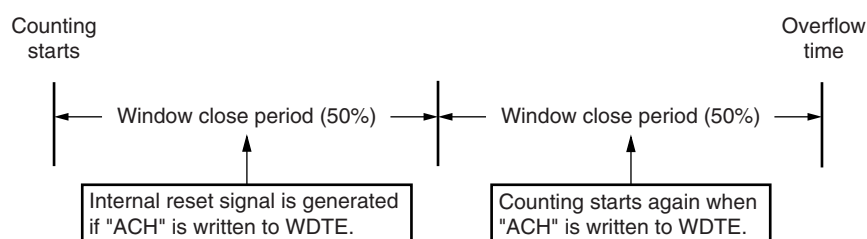
Remark f_{IL}: Low-speed on-chip oscillator clock frequency

10.4.3 Setting window open period of watchdog timer

Set the window open period of the watchdog timer by using bits 6 and 5 (WINDOW1, WINDOW0) of the option byte (000C0H). The outline of the window is as follows.

- If "ACH" is written to the watchdog timer enable register (WDTE) during the window open period, the watchdog timer is cleared and starts counting again.
- Even if "ACH" is written to the WDTE register during the window close period, an abnormality is detected and an internal reset signal is generated.

Example: If the window open period is 50%



Caution When data is written to the WDTE register for the first time after reset release, the watchdog timer is cleared in any timing regardless of the window open time, as long as the register is written before the overflow time, and the watchdog timer starts counting again.

The window open period can be set as follows.

Table 10-4. Setting Window Open Period of Watchdog Timer

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	0	Setting prohibited
0	1	50%
1	0	75%
1	1	100%

Caution When bit 0 (WDSTBYON) of the option byte (000C0H) = 0, the window open period is 100% regardless of the values of the WINDOW1 and WINDOW0 bits.

Remark If the overflow time is set to $2^9/f_{IL}$, the window close time and open time are as follows.

	Setting of Window Open Period		
	50%	75%	100%
Window close time	0 to 20.08 ms	0 to 10.04 ms	None
Window open time	20.08 to 29.68 ms	10.04 to 29.68 ms	0 to 29.68 ms

<When window open period is 50%>

- Overflow time:
 $2^9/f_{IL} \text{ (MAX.)} = 2^9/17.25 \text{ kHz} = 29.68 \text{ ms}$
- Window close time:
 $0 \text{ to } 2^9/f_{IL} \text{ (MIN.)} \times (1 - 0.5) = 0 \text{ to } 2^9/12.75 \text{ kHz} \times 0.5 = 0 \text{ to } 20.08 \text{ ms}$
- Window open time:
 $2^9/f_{IL} \text{ (MIN.)} \times (1 - 0.5) \text{ to } 2^9/f_{IL} \text{ (MAX.)} = 2^9/12.75 \text{ kHz} \times 0.5 \text{ to } 2^9/17.25 \text{ kHz} = 20.08 \text{ to } 29.68 \text{ ms}$

10.4.4 Setting watchdog timer interval interrupt

Depending on the setting of bit 7 (WDTINT) of an option byte (000C0H), an interval interrupt (INTWDTI) can be <R> generated when $75\% + 1/2f_{IL}$ of the overflow time is reached.

Table 10-5. Setting of Watchdog Timer Interval Interrupt

WDTINT	Use of Watchdog Timer Interval Interrupt
0	Interval interrupt is not used.
1	Interval interrupt is generated when $75\% + 1/2f_{IL}$ of overflow time is reached.

<R>

Caution When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.

Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.

Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

Remark The watchdog timer continues counting even after INTWDTI is generated (until ACH is written to the watchdog timer enable register (WDTE)). If ACH is not written to the WDTE register before the overflow time, an internal reset signal is generated.

CHAPTER 11 A/D CONVERTER

The number of analog input channels of the A/D converter differs, depending on the product.

			25-pin	32-pin	48-pin	64-pin
Analog input channels	Total		13 ch	18 ch	24 ch	28 ch
	High accuracy channel	Pins based on input buffer power supply AV_{DD}	4 ch (ANI0 to ANI3)	5 ch (ANI0 to ANI4)	9 ch (ANI0 to ANI8)	13 ch (ANI0 to ANI12)
	Standard channel	Pins based on input buffer power supply V_{DD}	9 ch (ANI16 to ANI18, ANI20, ANI21, ANI25 to ANI27, ANI29)	13 ch (ANI16 to ANI24, ANI26 to ANI29)	15 ch (ANI16 to ANI30)	–
		Pins based on input buffer power supply EV_{DD0}	–	–	–	15 ch (ANI16 to ANI30)

Remark Most of the following descriptions in this chapter use the 64-pin products as an example. With 25 to 48-pin products, replace EV_{DD0} with V_{DD} , or replace EV_{SS0} with V_{SS} .

11.1 Function of A/D Converter

The A/D converter converts analog input signals into digital values, and is configured to control analog inputs, including up to 28 channels of A/D converter analog inputs (ANI0 to ANI12 and ANI16 to ANI30). 12-bit resolution or 8-bit resolution can also be selected by using the ADTYP bit of A/D converter mode register 2 (ADM2).

The A/D converter has the following function.

• A/D conversion

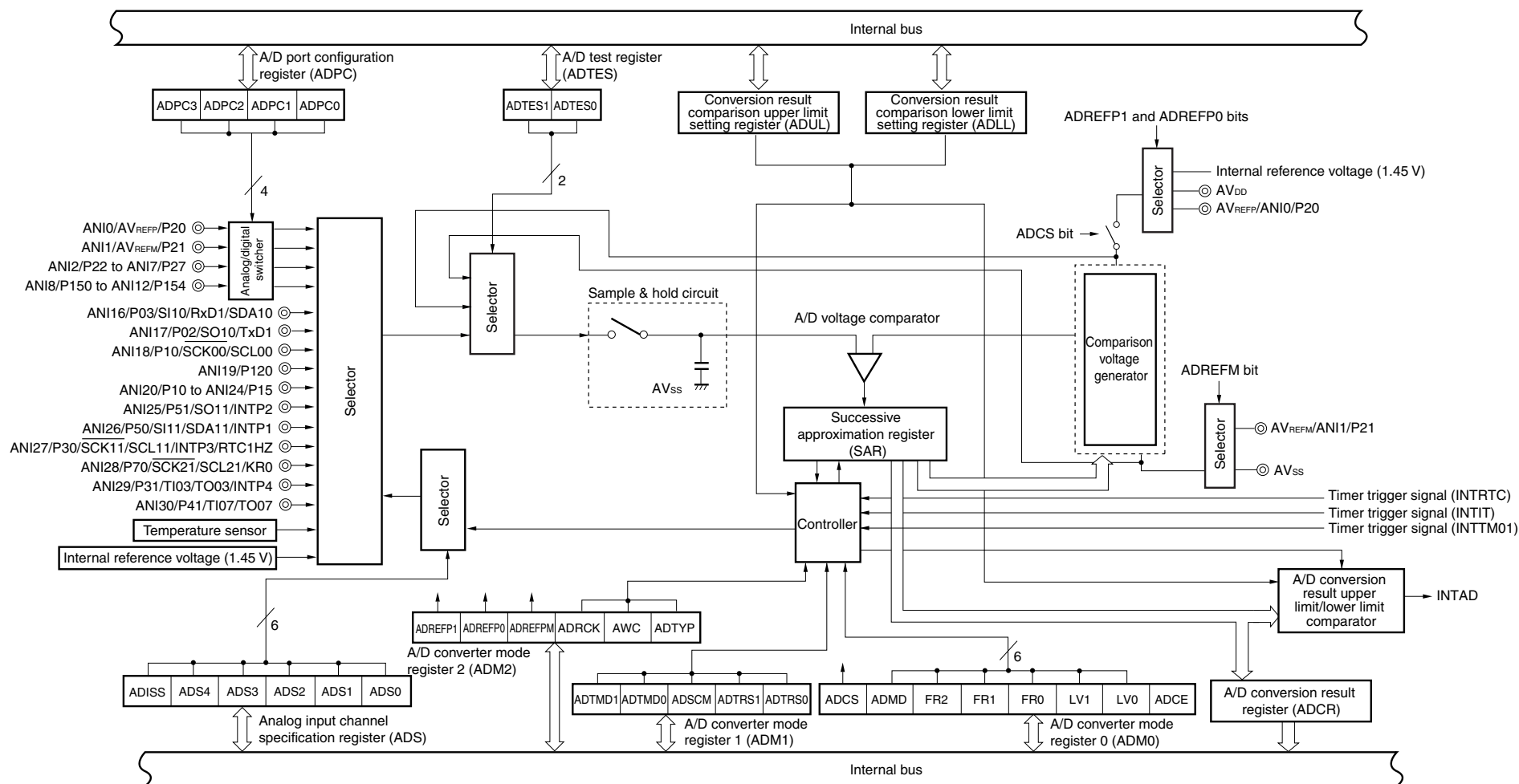
A/D conversion is carried out repeatedly for one analog input channel selected from ANI0 to ANI12 and ANI16 to ANI30. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated (when in the select mode).

Various A/D conversion modes can be specified by using the mode combinations below.

Trigger Mode	Channel Selection Mode	Conversion Operation Mode
- Software trigger Conversion is started by specifying a software trigger. - Hardware trigger no-wait mode Conversion is started by detecting a hardware trigger. - Hardware trigger wait mode The power is turned on by detecting a hardware trigger while the power is off and in the conversion standby state, and conversion is then started automatically after the stabilization wait time passes.	- Select mode A/D conversion is performed on the analog input of one channel. - Scan mode A/D conversion is performed on the analog input of four channels in order.	- One-shot conversion mode A/D conversion is performed on the selected channel once. - Sequential conversion mode A/D conversion is sequentially performed on the selected channels until it is stopped by software.

<R>

Figure 11-1. Block Diagram of A/D Converter



Remark Analog input pins in figure 11-1 when a 64-pin product is used.

11.2 Configuration of A/D Converter

The A/D converter includes the following hardware.

(1) ANI0 to ANI12 and ANI16 to ANI30 pins

These are the analog input pins of the 28 channels of the A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

(2) Sample & hold circuit

The sample & hold circuit samples each of the analog input voltages sequentially sent from the input circuit, and sends them to the A/D voltage comparator. This circuit also holds the sampled analog input voltage during A/D conversion.

(3) A/D voltage comparator

This A/D voltage comparator compares output from the voltage tap of the comparison voltage generator with the sampled voltage value.

If the analog input voltage is found to be greater than the reference voltage ($1/2 AV_{REF}$) as a result of the comparison, the most significant bit (MSB) of the successive approximation register (SAR) is set. If the analog input voltage is less than the reference voltage ($1/2 AV_{REF}$), the MSB bit of the SAR is reset.

After that, bit 10 of the SAR register is automatically set, and the next comparison is made. The voltage tap of the comparison voltage generator is selected by the value of bit 11, to which the result has been already set.

Bit 11 = 0: ($1/4 AV_{REF}$)

Bit 11 = 1: ($3/4 AV_{REF}$)

The voltage tap of the comparison voltage generator and the analog input voltage are compared and bit 10 of the SAR register is manipulated according to the result of the comparison.

Analog input voltage $\geq$ Voltage tap of comparison voltage generator: Bit 10 = 1

Analog input voltage $\leq$ Voltage tap of comparison voltage generator: Bit 10 = 0

Comparison is continued like this to bit 0 of the SAR register.

When performing A/D conversion at a resolution of 8 bits, the comparison continues until bit 4 of the SAR register.

Remark AV_{REF} : The + side reference voltage of the A/D converter.

(This can be selected from AV_{REFP} , the internal reference voltage (1.45 V), and AV_{DD} .)

(4) Comparison voltage generator

The comparison voltage generator generates the comparison voltage input from an analog input pin.

(5) Successive approximation register (SAR)

The SAR register is a register that sets voltage tap data whose values from the comparison voltage generator match the voltage values of the analog input pins, 1 bit at a time starting from the most significant bit (MSB).

If data is set in the SAR register all the way to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register (conversion results) are held in the A/D conversion result register (ADCR). When all the specified A/D conversion operations have ended, an A/D conversion end interrupt request signal (INTAD) is generated.

(6) 12-bit A/D conversion result register (ADCR)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the A/D conversion result in its lower 12 bits (the higher 4 bits are fixed to 0).

(7) 8-bit A/D conversion result register (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

(8) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD.

(9) AV_{REFP} pin

This pin inputs an external reference voltage (AV_{REFP}).

If using AV_{REFP} as the + side reference voltage of the A/D converter, set the ADREFP1 and ADREFP0 bits of A/D converter mode register 2 (ADM2) to 1.

The analog signals input to ANI0 to ANI12 and ANI16 to ANI30 are converted to digital signals based on the voltage applied between AV_{REFP} and the – side reference voltage (AV_{REFM}/AV_{SS}).

In addition to AV_{REFP}, it is possible to select AV_{DD}, or the internal reference voltage (1.45 V) as the + side reference voltage of the A/D converter.

(10) AV_{REFM} pin

This pin inputs an external reference voltage (AV_{REFM}). If using AV_{REFM} as the – side reference voltage of the A/D converter, set the ADREFM bit of the ADM2 register to 1.

In addition to AV_{REFM}, it is possible to select AV_{SS} as the – side reference voltage of the A/D converter.

11.3 Registers Used in A/D Converter

The A/D converter is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- A/D converter mode register 0 (ADM0)
- A/D converter mode register 1 (ADM1)
- A/D converter mode register 2 (ADM2)
- 12-bit A/D conversion result register (ADCR)
- 8-bit A/D conversion result register (ADCRH)
- Analog input channel specification register (ADS)
- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)
- A/D test register (ADTES)
- A/D port configuration register (ADPC)
- Port mode control registers 0, 1, 3 to 5, 7, and 12 (PMC0, PMC1, PMC3 to PMC5, PMC7, PMC12)
- Port mode registers 0 to 5, 7, 12, and 15 (PM0 to PM5, PM7, PM12, PM15)

11.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the A/D converter is used, be sure to set bit 5 (ADCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-2. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	IICA0EN	SAU1EN ^{Note}	SAU0EN	0	TAU0EN

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. - SFR used by the A/D converter cannot be written. - The A/D converter is in the reset status.
1	Enables input clock supply. SFR used by the A/D converter can be read/written.

Note 32-, 48-, 64-pin products only

Cautions 1. When setting the A/D converter, be sure to set the ADCEN bit to 1 first. If ADCEN = 0, writing to a control register of the A/D converter is ignored, and, even if the register is read, only the default value is read (except for port mode registers 0 to 5, 7, 12, and 15 (PM0 to PM5, PM7, PM12, PM15), port mode control registers 0, 1, 3 to 5, 7, and 12 (PMC0, PMC1, PMC3 to PMC5, PMC7, PMC12), and A/D port configuration register (ADPC)).

2. Be sure to clear the following bits to 0.

25-pin products: bits 1, 3, 6

32, 48, 64-pin products: bits 1, 6

11.3.2 A/D converter mode register 0 (ADM0)

This register sets the conversion time for analog input to be A/D converted, and starts/stops conversion.

The ADM0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-3. Format of A/D Converter Mode Register 0 (ADM0)

Address: FFF30H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
ADM0	ADCS	ADMD	FR2 ^{Note 1}	FR1 ^{Note 1}	FR0 ^{Note 1}	LV1 ^{Note 1}	LV0 ^{Note 1}	ADCE

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	Enables conversion operation [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: Stabilization wait status + conversion operation status

ADMD	Specification of the A/D conversion channel selection mode
0	Select mode
1	Scan mode

ADCE	A/D voltage comparator operation control ^{Note 2}
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Notes 1. For details of the FR2 to FR0, LV1, LV0 bits, and A/D conversion, see **Table 11-3 A/D Conversion Time Selection**.

- 2.** While in the software trigger mode or hardware trigger no-wait mode, the operation of the A/D voltage comparator is controlled by the ADCS and ADCE bits, and it takes stabilization wait status from the start of operation for the operation to stabilize. Therefore, when the ADCS bit is set to 1 after stabilization wait status or more has elapsed from the time ADCE bit is set to 1, the conversion result at that time has priority over the first conversion result. If the ADCS bit was set to 1 before the stabilization time elapsed, ignore the first conversion data.

[Stabilization wait status]

If a high-accuracy channel is selected as the analog input channel: 0.5 μ s

If a test mode setting (ADTES1 bit of ADTES register = 1) is selected: 0.5 μ s

If a standard channel is selected as the analog input channel: 2 μ s

If a temperature sensor output/internal reference voltage output are selected as the analog input channel: (ADISS bit of ADS register = 1): 2 μ s

Cautions 1. Change the ADMD, FR2 to FR0, LV1, and LV0 bits while in the conversion stopped status (ADCS = 0, ADCE = 0).

2. Setting ADCS = 1, ADCE = 0 is prohibited.

- 3.** Do not change the ADCE and ADCS bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to set these bits in the order described in **11.7 A/D Converter Setup Flowchart**.

Table 11-1. Settings of ADCS and ADCE Bits

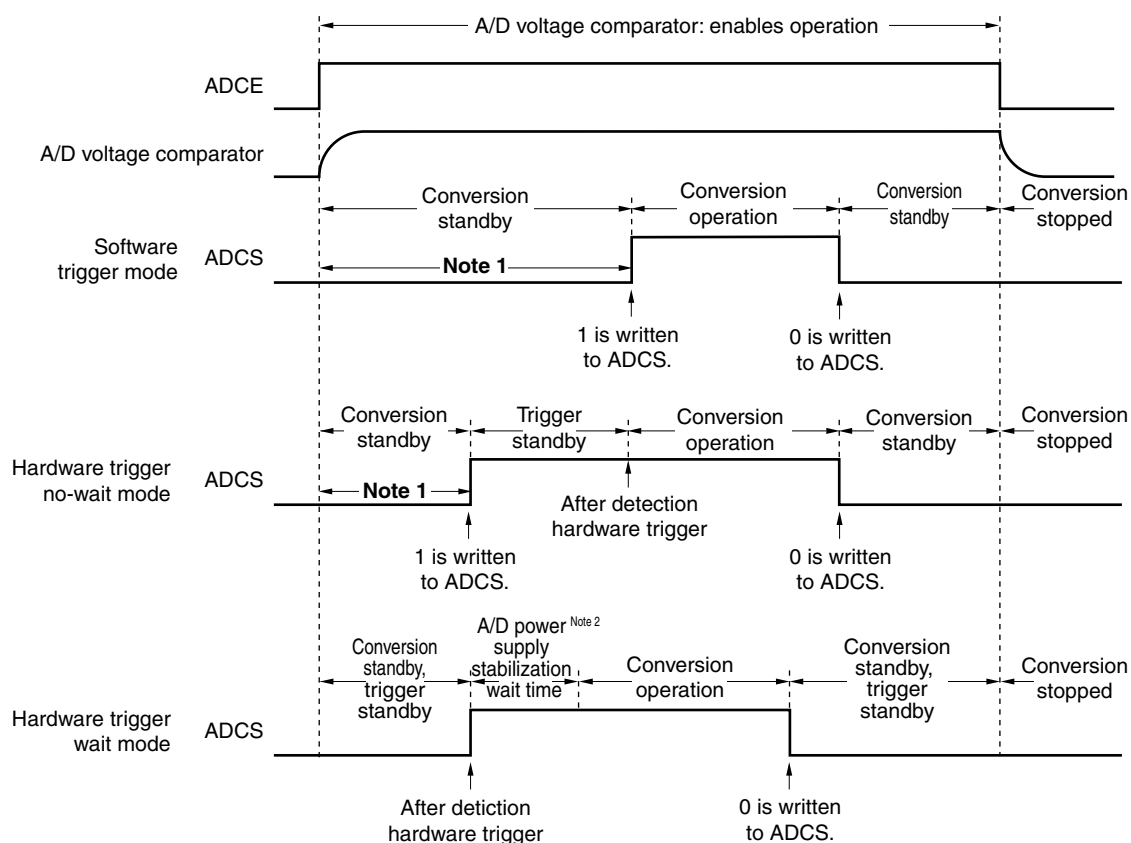
ADCS	ADCE	A/D Conversion Operation
0	0	Stop status (DC power consumption path does not exist)
0	1	Conversion standby mode (only A/D voltage comparator consumes power ^{Note})
1	0	Setting prohibited
1	1	Conversion mode (A/D voltage comparator: enables operation)

Note In hardware trigger wait mode, there is no DC power consumption path even during conversion standby mode.

Table 11-2. Setting and Clearing Conditions for ADCS Bit

A/D Conversion Mode			Set Conditions	Clear Conditions
Software trigger	Select mode	Sequential conversion mode	When 1 is written to ADCE and ADCS	When 0 is written to ADCS
		One-shot conversion mode		- When 0 is written to ADCS - The bit is automatically cleared to 0 when A/D conversion ends.
	Scan mode	Sequential conversion mode		When 0 is written to ADCS
		One-shot conversion mode		- When 0 is written to ADCS - The bit is automatically cleared to 0 when conversion ends on the specified four channels.
Hardware trigger no-wait mode	Select mode	Sequential conversion mode		When 0 is written to ADCS
		One-shot conversion mode		When 0 is written to ADCS
	Scan mode	Sequential conversion mode		When 0 is written to ADCS
		One-shot conversion mode		When 0 is written to ADCS
Hardware trigger wait mode	Select mode	Sequential conversion mode	When 1 is written to ADCE and a hardware trigger is input	When 0 is written to ADCS
		One-shot conversion mode		- When 0 is written to ADCS - The bit is automatically cleared to 0 when A/D conversion ends.
	Scan mode	Sequential conversion mode		When 0 is written to ADCS
		One-shot conversion mode		- When 0 is written to ADCS - The bit is automatically cleared to 0 when conversion ends on the specified four channels.

Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used



Notes 1. While in the software trigger mode or hardware trigger no-wait mode, the time from the rising of the ADCE bit to the falling of the ADCS bit must be following time or longer to stabilize the internal circuit.

[Stabilization wait status]

If a high-accuracy channel is selected as the analog input channel: $0.5 \mu s$

If a test mode setting (ADTES1 bit of ADTES register = 1) is selected: $0.5 \mu s$

If a standard channel is selected as the analog input channel: $2 \mu s$

If a temperature sensor output/internal reference voltage output are selected as the analog input channel: (ADISS bit of ADS register = 1): $2 \mu s$

- 2.** For the second and subsequent conversion in sequential conversion mode and for conversion of the channel specified by scan 1, 2, and 3 in scan mode, the A/D power supply stabilization wait time do not occur after a hardware trigger is detected.

Cautions 1. If using the hardware trigger wait mode, setting the ADCS bit to 1 is prohibited (but the bit is automatically switched to 1 when the hardware trigger signal is detected). However, it is possible to clear the ADCS bit to 0 to specify the A/D conversion standby status.

2. While in the one-shot conversion mode of the hardware trigger no-wait mode, the ADCS flag is not automatically cleared to 0 when A/D conversion ends. Instead, 1 is retained.

3 Only rewrite the value of the ADCE bit when $ADCS = 0$ (while in the conversion stopped/conversion standby status).

4. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no wait mode: $2 f_{CLK}$ clock + conversion operation status

Hardware trigger wait mode: $2 f_{CLK}$ clock + stabilization wait status + conversion operation status

Remark f_{CLK} : CPU/peripheral hardware clock frequency

<R>

Table 11-3. A/D Conversion Time Selection (1/4)

(1) 12 bit A/D Converter When there is no stabilization wait time (software trigger mode/hardware trigger no-wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f _{AD})	Number of Conversion Clock	Conversion Time	Conversion Time Selection				
FR2	FR1	FR0	LV1	LV0					AV _{DD} = 1.6 to 3.6 V f _{CLK} = 1 MHz	AV _{DD} = 1.6 to 3.6 V f _{CLK} = 4 MHz	AV _{DD} = 1.8 to 3.6 V f _{CLK} = 8 MHz	AV _{DD} = 2.4 to 3.6 V f _{CLK} = 16 MHz	AV _{DD} = 2.7 to 3.6 V f _{CLK} = 32 MHz
0	0	0	0	0	Normal 1	f _{CLK} /32	54 f _{AD} (number of sampling clock: 11 f _{AD})	1728/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs
0	0	1				f _{CLK} /16		864/f _{CLK}				54 μs	27 μs
0	1	0				f _{CLK} /8		432/f _{CLK}			54 μs	27 μs	13.5 μs
0	1	1				f _{CLK} /6		324/f _{CLK}			40.5 μs	20.25 μs	10.125 μs
1	0	0				f _{CLK} /5		270/f _{CLK}			33.75 μs	16.875 μs	8.4375 μs
1	0	1				f _{CLK} /4		216/f _{CLK}		54 μs	27 μs	13.5 μs	6.75 μs
1	1	0				f _{CLK} /2		108/f _{CLK}		27 μs	13.5 μs	6.75 μs	3.375 μs
1	1	1				f _{CLK} /1		54/f _{CLK}	54 μs	13.5 μs	6.75 μs	3.375 μs	Setting prohibited
0	0	0	0	1	Normal 2	f _{CLK} /32	66 f _{AD} (number of sampling clock: 23 f _{AD})	2112/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	66 μs
0	0	1				f _{CLK} /16		1056/f _{CLK}				66 μs	33 μs
0	1	0				f _{CLK} /8		528/f _{CLK}			66 μs ^{Note}	33 μs	16.5 μs
0	1	1				f _{CLK} /6		396/f _{CLK}			49.5 μs ^{Note}	24.75 μs	12.375 μs
1	0	0				f _{CLK} /5		330/f _{CLK}			41.25 μs ^{Note}	20.625 μs	10.3125 μs
1	0	1				f _{CLK} /4		264/f _{CLK}		66 μs ^{Note}	33 μs ^{Note}	16.5 μs	8.25 μs
1	1	0				f _{CLK} /2		132/f _{CLK}		33 μs ^{Note}	16.5 μs ^{Note}	8.25 μs	4.125 μs
1	1	1				f _{CLK} /1		66/f _{CLK}	66 μs ^{Note}	16.5 μs ^{Note}	8.25 μs ^{Note}	4.125 μs	Setting prohibited
0	0	0	1	0	Normal 1	f _{CLK} /32	76 f _{AD} (number of sampling clock: 33 f _{AD})	2432/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	76 μs
0	0	1				f _{CLK} /16		1216/f _{CLK}				76 μs	38 μs
0	1	0				f _{CLK} /8		608/f _{CLK}			76 μs	38 μs	19 μs
0	1	1				f _{CLK} /6		456/f _{CLK}			57 μs	28.5 μs	14.25 μs
1	0	0				f _{CLK} /5		380/f _{CLK}			47.5 μs	23.75 μs	11.875 μs
1	0	1				f _{CLK} /4		304/f _{CLK}		76 μs ^{Note}	38 μs	19 μs	9.5 μs
1	1	0				f _{CLK} /2		152/f _{CLK}		38 μs ^{Note}	19 μs	9.5 μs	4.75 μs
1	1	1				f _{CLK} /1		76/f _{CLK}	76 μs ^{Note}	19 μs ^{Note}	9.5 μs	4.75 μs	Setting prohibited
0	0	0	1	1	Normal 2	f _{CLK} /32	230 f _{AD} (number of sampling clock: 187 f _{AD})	7360/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	230 μs
0	0	1				f _{CLK} /16		3680/f _{CLK}				230 μs	115 μs
0	1	0				f _{CLK} /8		1840/f _{CLK}			230 μs	115 μs	57.5 μs
0	1	1				f _{CLK} /6		1380/f _{CLK}			172.5 μs	86.25 μs	43.125 μs
1	0	0				f _{CLK} /5		1150/f _{CLK}			143.75 μs	71.875 μs	35.9375 μs
1	0	1				f _{CLK} /4		920/f _{CLK}		230 μs	115 μs	57.5 μs	28.75 μs
1	1	0				f _{CLK} /2		460/f _{CLK}		115 μs	57.5 μs	28.75 μs	14.375 μs
1	1	1				f _{CLK} /1		230/f _{CLK}	230 μs	57.5 μs	28.75 μs	14.375 μs	Setting prohibited

Note When using ANI16 to ANI30, setting this value is prohibited.

(Cautions and Remark are listed on the next page.)

- <R> **Cautions**
1. When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, while in the conversion stopped (ADCS = 0, ADCE = 0).
 2. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.
 3. When software trigger mode/hardware trigger no-wait mode, specify the conversion time so that the following conditions are satisfied:
 - f_{AD} is used within a range of 1 to 16 MHz.
 - When using ANI16 to ANI30, the A/D converter is used in the following range of AV_{DD} , in accordance with the settings of the LV1 and LV0 bits:

When LV1 = 0, LV0 = 0: Setting prohibit

When LV1 = 0, LV0 = 1: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$

When LV1 = 1, LV0 = 0: $1.8\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$

When LV1 = 1, LV0 = 1: $1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$
 - If temperature sensor output or internal reference voltage output (ADISS bit of ADS register = 1) is specified for the analog input channel, the A/D converter is used in the following range of AV_{DD} :

When LV1 = 0, LV0 = 0: Setting prohibit

When other than LV1 = 0, LV0 = 0: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$

Remark f_{CLK} : CPU/peripheral hardware clock frequency

<R>

Table 11-3. A/D Conversion Time Selection (2/4)

(2) 12 bit A/D Converter When there is stabilization wait time(hardware trigger wait mode (except second and subsequent conversion in sequential conversion mode and conversion of channel specified by scan 1, 2, and 3 in scan mode^{Note 1)}))

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f _{CLK})	Number of Stabilization Wait Clock	Number of Conversion Clock	Stabilization Wait Time + Conversion Time	Conversion Time Selection							
FR2	FR1	FR0	LV1	LV0						AV _{DD} = 1.6 to 3.6 V	AV _{DD} = 1.6 to 3.6 V	AV _{DD} = 1.8 to 3.6 V	AV _{DD} = 2.4 to 3.6 V	AV _{DD} = 2.7 to 3.6 V			
										f _{CLK} = 1 MHz	f _{CLK} = 4 MHz	f _{CLK} = 8 MHz	f _{CLK} = 16 MHz	f _{CLK} = 32 MHz			
0	0	0	1	0	Low-voltage 1	f _{CLK} /32	4 f _{CLK}	54 f _{AD} (number of sampling clock: 11 f _{AD})	1732/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54.125 μs			
0	0	1				f _{CLK} /16			868/f _{CLK}						54.25 μs	27.125 μs	
0	1	0				f _{CLK} /8			436/f _{CLK}						54.5 μs	27.25 μs	13.625 μs
0	1	1				f _{CLK} /6			328/f _{CLK}						41 μs	20.5 μs	10.25 μs
1	0	0				f _{CLK} /5			274/f _{CLK}						34.25 μs	17.125 μs	8.5625 μs
1	0	1				f _{CLK} /4			220/f _{CLK}					55 μs	27.5 μs	13.75 μs	6.875 μs
1	1	0				f _{CLK} /2			112/f _{CLK}						28 μs	14 μs	7 μs
1	1	1				f _{CLK} /1			56/f _{CLK}					56 μs	14 μs	7 μs	3.5 μs
0	0	0	1	1	Low-voltage 2	f _{CLK} /32	58 f _{CLK}	66 f _{AD} (number of sampling clock: 23 f _{AD})	2170/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	67.8125 μs			
0	0	1				f _{CLK} /16			1114/f _{CLK}						69.625 μs	34.8125 μs	
0	1	0				f _{CLK} /8			586/f _{CLK}						73.25 μs ^{Note 2}	36.625 μs	18.3125 μs
0	1	1				f _{CLK} /6			454/f _{CLK}						56.75 μs ^{Note 2}	28.375 μs	14.1875 μs
1	0	0				f _{CLK} /5			388/f _{CLK}						48.5 μs ^{Note 2}	24.25 μs	12.125 μs
1	0	1				f _{CLK} /4			322/f _{CLK}					80.5 μs ^{Note 2}	40.25 μs ^{Note 2}	20.125 μs	10.0625 μs
1	1	0				f _{CLK} /2			190/f _{CLK}						47.5 μs ^{Note 2}	23.75 μs ^{Note 2}	11.875 μs
1	1	1				f _{CLK} /1			95/f _{CLK}					95 μs ^{Note 2}	23.75 μs ^{Note 2}	11.875 μs ^{Note 2}	5.9375 μs
0	0	0	1	0	Low-voltage 1	f _{CLK} /32	15 f _{CLK}	76 f _{AD} (number of sampling clock: 33 f _{AD})	2447/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	76.46875 μs ^{Note 2}			
0	0	1				f _{CLK} /16			1231/f _{CLK}						76.9375 μs ^{Note 2}	38.46875 μs ^{Note 2}	
0	1	0				f _{CLK} /8			623/f _{CLK}						77.875 μs	38.9375 μs ^{Note 2}	19.46875 μs ^{Note 2}
0	1	1				f _{CLK} /6			471/f _{CLK}						58.875 μs	29.4375 μs ^{Note 2}	14.71875 μs ^{Note 2}
1	0	0				f _{CLK} /5			395/f _{CLK}						49.375 μs	24.6875 μs ^{Note 2}	12.34375 μs ^{Note 2}
1	0	1				f _{CLK} /4			319/f _{CLK}					79.75 μs ^{Note 2}	39.875 μs	19.9375 μs ^{Note 2}	9.96875 μs ^{Note 2}
1	1	0				f _{CLK} /2			167/f _{CLK}						41.75 μs ^{Note 2}	20.875 μs	10.4375 μs ^{Note 2}
1	1	1				f _{CLK} /1			91/f _{CLK}					91 μs ^{Note 2}	22.75 μs ^{Note 2}	11.375 μs	5.6875 μs ^{Note}
0	0	0	1	1	Low-voltage 2	f _{CLK} /32	8 f _{CLK}	230 f _{AD} (number of sampling clock: 187 f _{AD})	7368/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	230.25 μs ^{Note 2}			
0	0	1				f _{CLK} /16			3688/f _{CLK}						230.5 μs ^{Note 2}	115.25 μs ^{Note 2}	
0	1	0				f _{CLK} /8			1848/f _{CLK}						231 μs ^{Note 2}	115.5 μs ^{Note 2}	57.75 μs ^{Note 2}
0	1	1				f _{CLK} /6			1388/f _{CLK}						173.5 μs ^{Note 2}	86.75 μs ^{Note 2}	43.375 μs ^{Note 2}
1	0	0				f _{CLK} /5			1158/f _{CLK}						144.75 μs ^{Note 2}	72.375 μs ^{Note 2}	36.1875 μs ^{Note 2}
1	0	1				f _{CLK} /4			928/f _{CLK}					232 μs	116 μs	58 μs	29 μs ^{Note 2}
1	1	0				f _{CLK} /2			468/f _{CLK}						117 μs	58.5 μs ^{Note 2}	29.25 μs ^{Note 2}
1	1	1				f _{CLK} /1			238/f _{CLK}					238 μs	59.5 μs	29.75 μs ^{Note 2}	14.875 μs ^{Note 2}

(Notes, Cautions and Remark are listed on the next page.)

- <R> **Notes** 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channel specified by scan 1, 2, and 3 in scan mode, the conversion start time and stabilization wait time for A/D power supply do not occur after a hardware trigger is detected (see **table 11-3 (1/4)**).
2. When using ANI16 to ANI30, setting this value is prohibited.

- <R> **Cautions** 1. When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, while in the conversion stopped (ADCS = 0, ADCE = 0).
2. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.
3. When hardware trigger wait mode, specify the conversion time so that the following conditions are satisfied:
- f_{AD} is used within a range of 1 to 16 MHz.
 - When using ANI16 to ANI30, the A/D converter is used in the following conditions:
 - When LV1 = 0, LV0 = 0: Setting prohibit
 - When LV1 = 0, LV0 = 1: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$
 - When LV1 = 1, LV0 = 0: $1.8\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $1\text{ MHz} \leq f_{CLK} \leq 8\text{ MHz}$
 - When LV1 = 1, LV0 = 1: $1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $1\text{ MHz} \leq f_{CLK} \leq 4\text{ MHz}$
 - If temperature sensor output or internal reference voltage output (ADISS bit of ADS register = 1) is specified for the analog input channel, the A/D converter is used in the following conditions:
 - When LV1 = 0, LV0 = 0: Setting prohibit
 - When LV1 = 0, LV0 = 1: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$
 - When LV1 = 1, LV0 = 0: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $1\text{ MHz} \leq f_{CLK} \leq 8\text{ MHz}$
 - When LV1 = 1, LV0 = 1: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $1\text{ MHz} \leq f_{CLK} \leq 4\text{ MHz}$

Remark f_{CLK} : CPU/peripheral hardware clock frequency

<R>

Table 11-3. A/D Conversion Time Selection (3/4)

(3) 8 bit A/D Converter When there is no stabilization wait time (software trigger mode/hardware trigger no-wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f _{AD})	Number of Conversion Clock	Conversion Time	Conversion Time Selection				
FR2	FR1	FR0	LV1	LV0					AV _{DD} = 1.6 to 3.6 V f _{CLK} = 1 MHz	AV _{DD} = 1.6 to 3.6 V f _{CLK} = 4 MHz	AV _{DD} = 1.8 to 3.6 V f _{CLK} = 8 MHz	AV _{DD} = 2.4 to 3.6 V f _{CLK} = 16 MHz	AV _{DD} = 2.7 to 3.6 V f _{CLK} = 32 MHz
0	0	0	0	0	Normal 1	f _{CLK} /32	41 f _{AD} (number of sampling clock: 11 f _{AD})	1312/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	41 μs
0	0	1				f _{CLK} /16		656/f _{CLK}					41 μs
0	1	0				f _{CLK} /8		328/f _{CLK}					20.5 μs
0	1	1				f _{CLK} /6		246/f _{CLK}					10.25 μs
1	0	0				f _{CLK} /5		205/f _{CLK}					7.6875 μs
1	0	1				f _{CLK} /4		164/f _{CLK}					6.40625 μs
1	1	0				f _{CLK} /2		82/f _{CLK}					5.125 μs
1	1	1				f _{CLK} /1		41/f _{CLK}	41 μs	10.25 μs	5.125 μs	2.5625 μs	Setting prohibited
0	0	0	0	1	Normal 2	f _{CLK} /32	53 f _{AD} (number of sampling clock: 23 f _{AD})	1696/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	53 μs
0	0	1				f _{CLK} /16		848/f _{CLK}					26.5 μs
0	1	0				f _{CLK} /8		424/f _{CLK}					13.25 μs
0	1	1				f _{CLK} /6		318/f _{CLK}					9.9375 μs
1	0	0				f _{CLK} /5		265/f _{CLK}					8.28125 μs
1	0	1				f _{CLK} /4		212/f _{CLK}					6.625 μs
1	1	0				f _{CLK} /2		106/f _{CLK}					3.3125 μs
1	1	1				f _{CLK} /1		53/f _{CLK}	53 μs ^{Note}	13.25 μs ^{Note}	6.625 μs ^{Note}	3.3125 μs	Setting prohibited
0	0	0	1	0	Normal 1	f _{CLK} /32	63 f _{AD} (number of sampling clock: 33 f _{AD})	2016/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	63 μs
0	0	1				f _{CLK} /16		1008/f _{CLK}					31.5 μs
0	1	0				f _{CLK} /8		504/f _{CLK}					15.75 μs
0	1	1				f _{CLK} /6		378/f _{CLK}					11.8125 μs
1	0	0				f _{CLK} /5		315/f _{CLK}					9.84375 μs
1	0	1				f _{CLK} /4		252/f _{CLK}					7.875 μs
1	1	0				f _{CLK} /2		126/f _{CLK}					3.9375 μs
1	1	1				f _{CLK} /1		63/f _{CLK}	63 μs ^{Note}	15.75 μs ^{Note}	7.875 μs	3.9375 μs	Setting prohibited
0	0	0	1	1	Normal 2	f _{CLK} /32	217 f _{AD} (number of sampling clock: 187 f _{AD})	6944/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	217 μs
0	0	1				f _{CLK} /16		3472/f _{CLK}					108.5 μs
0	1	0				f _{CLK} /8		1736/f _{CLK}					54.25 μs
0	1	1				f _{CLK} /6		1302/f _{CLK}					40.6875 μs
1	0	0				f _{CLK} /5		1085/f _{CLK}					33.90625 μs
1	0	1				f _{CLK} /4		868/f _{CLK}					27.125 μs
1	1	0				f _{CLK} /2		434/f _{CLK}					13.5625 μs
1	1	1				f _{CLK} /1		217/f _{CLK}	217 μs	54.25 μs	27.125 μs	13.5625 μs	Setting prohibited

Note When using ANI16 to ANI30, setting this value is prohibited.

(Cautions and Remark are listed on the next page.)

- <R> **Cautions**
1. When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, while in the conversion stopped (ADCS = 0, ADCE = 0).
 2. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.
 3. When software trigger mode/hardware trigger no-wait mode, specify the conversion time so that the following conditions are satisfied:
 - f_{AD} is used within a range of 1 to 16 MHz.
 - When using ANI16 to ANI30, the A/D converter is used in the following range of AV_{DD} , in accordance with the settings of the LV1 and LV0 bits:

When LV1 = 0, LV0 = 0: Setting prohibit

When LV1 = 0, LV0 = 1: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$

When LV1 = 1, LV0 = 0: $1.8\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$

When LV1 = 1, LV0 = 1: $1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$
 - If temperature sensor output or internal reference voltage output (ADISS bit of ADS register = 1) is specified for the analog input channel, the A/D converter is used in the following range of AV_{DD} :

When LV1 = 0, LV0 = 0: Setting prohibit

When other than LV1 = 0, LV0 = 0: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$

Remark f_{CLK} : CPU/peripheral hardware clock frequency

<R>

Table 11-3. A/D Conversion Time Selection (4/4)

(4) 8 bit A/D Converter When there is stabilization wait time(hardware trigger wait mode (except second and subsequent conversion in sequential conversion mode and conversion of channel specified by scan 1, 2, and 3 in scan mode^{Note 1)}))

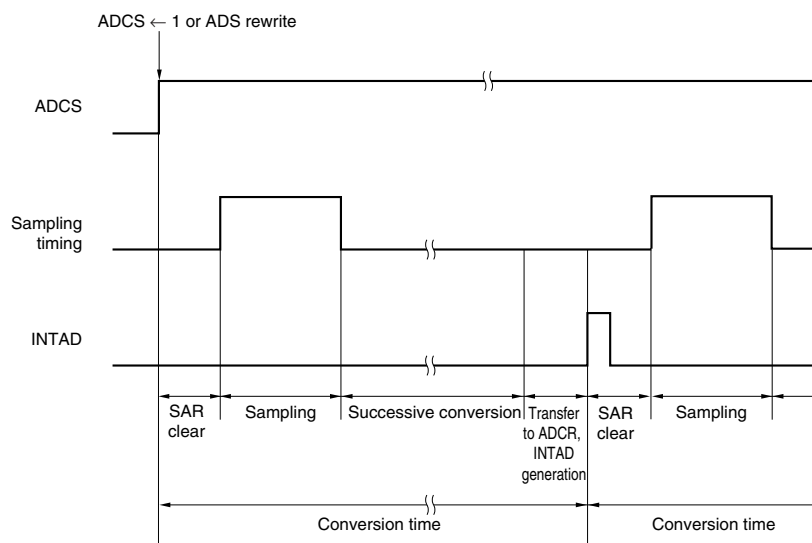
A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f _{CLK})	Number of Stabilization Wait Clock	Number of Conversion Clock	Stabilization Wait Time +Conversion Time	Conversion Time Selection							
										AV _{DD} = 1.6 to 3.6 V f _{CLK} = 1 MHz	AV _{DD} = 1.6 to 3.6 V f _{CLK} = 4 MHz	AV _{DD} = 1.8 to 3.6 V f _{CLK} = 8 MHz	AV _{DD} = 2.4 to 3.6 V f _{CLK} = 16 MHz	AV _{DD} = 2.7 to 3.6 V f _{CLK} = 32 MHz			
FR2	FR1	FR0	LV1	LV0	Low-voltage 1	f _{CLK} /32	4 f _{CLK}	41 f _{AD} (number of sampling clock: 11 f _{AD})	1316/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	41.125 μs			
0	0	1				f _{CLK} /16			660/f _{CLK}					41.25 μs	20.625 μs		
0	1	0				f _{CLK} /8			332/f _{CLK}					41.5 μs	20.75 μs	10.375 μs	
0	1	1				f _{CLK} /6			250/f _{CLK}					31.25 μs	15.625 μs	7.8125 μs	
1	0	0				f _{CLK} /5			209/f _{CLK}					25.125 μs	13.0625 μs	6.53125 μs	
1	0	1				f _{CLK} /4			168/f _{CLK}					42 μs	21 μs	10.5 μs	5.25 μs
1	1	0				f _{CLK} /2			86/f _{CLK}					21.5 μs	10.75 μs	5.375 μs	2.6875 μs
1	1	1				f _{CLK} /1	2 f _{CLK}	43/f _{CLK}	43 μs	10.75 μs	5.375 μs	2.6875 μs	Setting prohibited				
0	0	0	1	1	Low-voltage 2	f _{CLK} /32	58 f _{CLK}	53 f _{AD} (number of sampling clock: 23 f _{AD})	1754/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54.8125 μs			
0	0	1				f _{CLK} /16			906/f _{CLK}					56.625 μs	28.3125 μs		
0	1	0				f _{CLK} /8			482/f _{CLK}					60.25 μs ^{Note 2}	30.125 μs	15.0625 μs	
0	1	1				f _{CLK} /6			376/f _{CLK}					47 μs ^{Note 2}	23.5 μs	11.75 μs	
1	0	0				f _{CLK} /5			323/f _{CLK}					40.375 μs ^{Note 2}	20.1875 μs	10.09375 μs	
1	0	1				f _{CLK} /4			270/f _{CLK}					67.5 μs ^{Note 2}	33.75 μs ^{Note 2}	16.875 μs	8.4375 μs
1	1	0				f _{CLK} /2			164/f _{CLK}					41 μs ^{Note 2}	20.5 μs ^{Note 2}	10.25 μs	5.125 μs
1	1	1				f _{CLK} /1	29 f _{CLK}	82/f _{CLK}	82 μs ^{Note 2}	20.5 μs ^{Note 2}	10.25 μs ^{Note 2}	5.125 μs	Setting prohibited				
0	0	0	1	0	Low-voltage 1	f _{CLK} /32	15 f _{CLK}	63 f _{AD} (number of sampling clock: 33 f _{AD})	2031/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	63.46875 μs ^{Note 2}			
0	0	1				f _{CLK} /16			1023/f _{CLK}					63.9375 μs ^{Note 2}	31.96875 μs ^{Note 2}		
0	1	0				f _{CLK} /8			519/f _{CLK}					64.875 μs	32.4375 μs ^{Note 2}	16.21875 μs ^{Note 2}	
0	1	1				f _{CLK} /6			393/f _{CLK}					49.125 μs	24.5625 μs ^{Note 2}	12.28125 μs ^{Note 2}	
1	0	0				f _{CLK} /5			330/f _{CLK}					41.25 μs	20.625 μs ^{Note 2}	10.3125 μs ^{Note 2}	
1	0	1				f _{CLK} /4			267/f _{CLK}					66.75 μs ^{Note 2}	33.375 μs	16.6875 μs ^{Note 2}	8.34375 μs ^{Note 2}
1	1	0				f _{CLK} /2			141/f _{CLK}					35.25 μs ^{Note 2}	17.625 μs	8.8125 μs ^{Note 2}	4.40625 μs ^{Note 2}
1	1	1				f _{CLK} /1	78/f _{CLK}	78 μs ^{Note 2}	19.5 μs ^{Note 2}	9.75 μs	4.875 μs ^{Note 2}	Setting prohibited					
0	0	0	1	1	Low-voltage 2	f _{CLK} /32	8 f _{CLK}	217 f _{AD} (number of sampling clock: 187 f _{AD})	6952/f _{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	217.25 μs ^{Note 2}			
0	0	1				f _{CLK} /16			3480/f _{CLK}					217.5 μs ^{Note 2}	108.75 μs ^{Note 2}		
0	1	0				f _{CLK} /8			1744/f _{CLK}					218 μs	109 μs ^{Note 2}	54.5 μs ^{Note 2}	
0	1	1				f _{CLK} /6			1310/f _{CLK}					163.75 μs ^{Note 2}	81.875 μs ^{Note 2}	40.9375 μs ^{Note 2}	
1	0	0				f _{CLK} /5			1093/f _{CLK}					136.625 μs ^{Note 2}	68.3125 μs ^{Note 2}	34.15625 μs ^{Note 2}	
1	0	1				f _{CLK} /4			876/f _{CLK}					219 μs ^{Note 2}	109.5 μs ^{Note 2}	54.75 μs ^{Note 2}	27.375 μs ^{Note 2}
1	1	0				f _{CLK} /2			442/f _{CLK}					110.5 μs	55.25 μs ^{Note 2}	27.625 μs ^{Note 2}	13.8125 μs ^{Note 2}
1	1	1				f _{CLK} /1	225/f _{CLK}	225 μs	56.25 μs	28.125 μs ^{Note 2}	14.0625 μs ^{Note 2}	Setting prohibited					

(Notes, Cautions and Remark are listed on the next page.)

- <R> **Notes** 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channel specified by scan 1, 2, and 3 in scan mode, the conversion start time and stabilization wait time for A/D power supply do not occur after a hardware trigger is detected (see **table 11-3 (3/4)**).
2. When using ANI16 to ANI30, setting this value is prohibited.

- <R> **Cautions** 1. When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, while in the conversion stopped (ADCS = 0, ADCE = 0).
2. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.
3. When hardware trigger wait mode, specify the conversion time so that the following conditions are satisfied:
- f_{AD} is used within a range of 1 to 16 MHz.
 - When using ANI16 to ANI30, the A/D converter is used in the following conditions:
 - When LV1 = 0, LV0 = 0: Setting prohibit
 - When LV1 = 0, LV0 = 1: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$
 - When LV1 = 1, LV0 = 0: $1.8\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $1\text{ MHz} \leq f_{CLK} \leq 8\text{ MHz}$
 - When LV1 = 1, LV0 = 1: $1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $1\text{ MHz} \leq f_{CLK} \leq 4\text{ MHz}$
 - If temperature sensor output or internal reference voltage output (ADISS bit of ADS register = 1) is specified for the analog input channel, the A/D converter is used in the following conditions:
 - When LV1 = 0, LV0 = 0: Setting prohibit
 - When LV1 = 0, LV0 = 1: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$
 - When LV1 = 1, LV0 = 0: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $1\text{ MHz} \leq f_{CLK} \leq 8\text{ MHz}$
 - When LV1 = 1, LV0 = 1: $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $1\text{ MHz} \leq f_{CLK} \leq 4\text{ MHz}$

Remark f_{CLK} : CPU/peripheral hardware clock frequency

Figure 11-5. A/D Converter Sampling and A/D Conversion Timing (Example for Software Trigger Mode)

11.3.3 A/D converter mode register 1 (ADM1)

This register is used to specify the A/D conversion trigger, conversion mode, and hardware trigger signal.

The ADM1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-6. Format of A/D Converter Mode Register 1 (ADM1)

Address: FFF32H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	×	Software trigger mode
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	One-shot conversion mode

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 01 count or capture interrupt signal (INTTM01)
0	1	Setting prohibited
1	0	Real-time clock interrupt signal (INTRTC)
1	1	Interval timer interrupt signal (INTIT)

Cautions 1. Only rewrite the value of the ADM1 register while conversion is stopped (ADCE bit of A/D converter mode register 0 (ADM0) being 0).

2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no wait mode: $2 f_{CLK}$ clock + conversion operation status

Hardware trigger wait mode: $2 f_{CLK}$ clock + stabilization wait status + conversion operation status

3. In modes other than SNOOZE mode, input of the next INTRTC or INTIT will not be recognized as a valid hardware trigger for up to four f_{CLK} cycles after the first INTRTC or INTIT is input.

Remarks 1. ×: don't care

2. f_{CLK} : CPU/peripheral hardware clock frequency

11.3.4 A/D converter mode register 2 (ADM2)

This register is used to select the A/D converter reference voltage, check the upper limit and lower limit A/D conversion result values, select the resolution, and specify whether to use the SNOOZE mode.

The ADM2 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-7. Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	1	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from AV _{DD}
0	1	Supplied from P20/AV _{REFP} /ANI0
1	0	Supplied from the internal reference voltage (1.45 V) ^{Note}
1	1	Setting prohibited

- When ADREFP1 or ADREFP0 bit is rewritten, this must be configured in accordance with the following procedures.
 - Set ADCE = 0
 - Change the values of ADREFP1 and ADREFP0
 - Stabilization wait time (A)
 - Set ADCE = 1
 - Stabilization wait time (B)

The stabilization wait time indicated by (3) is required when the value of the ADREFP1 and ADREFP0 bits is changed.

When ADREFP1 and ADREFP0 are changed to 1 and 0: $A = 10 \mu s$

When ADREFP1 and ADREFP0 are changed to 0 and 0 or 0 and 1: $A = 1 \mu s$

The stabilization wait time indicated by (5) is required when the value of the ADCE bit is changed to 1.

If a high-accuracy channel is selected as the analog input channel: $0.5 \mu s$

If a test mode setting (ADTES1 bit of ADTES register = 1) is selected: $0.5 \mu s$

If a standard channel is selected as the analog input channel: $2 \mu s$

If a temperature sensor output/internal reference voltage output are selected as the analog input channel: (ADISS bit of ADS register = 1): $2 \mu s$

After (5) stabilization time, start the A/D conversion.
- When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output and internal reference voltage output.
Be sure to perform A/D conversion while ADISS = 0.

<R> **Note** This setting can be used only in HS (high-speed main) mode. For detail, refer to **Figure 24-3. Format of User Option Byte (000C2H/010C2H).**

- Cautions**
- Only rewrite the value of the ADM2 register while conversion is stopped (which is indicated by the ADCE bit of A/D converter mode register 0 (ADM0) being 0).
 - Do not set the ADREFP1 bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. Also, if the ADREFP1 bit is set to 1, the A/D converter reference voltage current (I_{ADREF}) indicated in 29.3.2 and 30.3.2 Supply current characteristics will be added to the current consumption when shifting to HALT mode while the CPU is operating on the main system clock.
 - When using AV_{REFP} and AV_{REFM}, specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.

Figure 11-7. Format of A/D Converter Mode Register 2 (ADM2) (2/2)

Address: F0010H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	1	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP

ADREFM	Selection of the – side reference voltage source of the A/D converter
0	Supplied from AV _{SS}
1	Supplied from P21/AV _{REFM} /ANI1

ADRCK	Checking the upper limit and lower limit conversion result values
0	The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register (<1>).
1	The interrupt signal (INTAD) is output when the ADCR register < the ADLL register (<2>) or the ADUL register < the ADCR register (<3>).

Figure 11-8 shows the generation range of the interrupt signal (INTAD) for <1> to <3>.

AWC	Specification of the SNOOZE mode
0	Do not use the SNOOZE mode function.
1	Use the SNOOZE mode function.

When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).

- The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (f_{CLK}). If any other clock is selected, specifying this mode is prohibited.
- Using the SNOOZE mode function in the software trigger mode or hardware trigger no-wait mode is prohibited.
- Using the SNOOZE mode function in the sequential conversion mode is prohibited.
- When using the SNOOZE mode function, specify a hardware trigger interval of at least “shift time to SNOOZE mode^{Note} + A/D power supply stabilization wait time + A/D conversion time + 2 f_{CLK} clock”
- Even when using SNOOZE mode, be sure to set the AWC bit to 0 in normal operation mode and change it to 1 just before shifting to STOP mode.

Also, be sure to change the AWC bit to 0 after returning from STOP mode to normal operation mode.

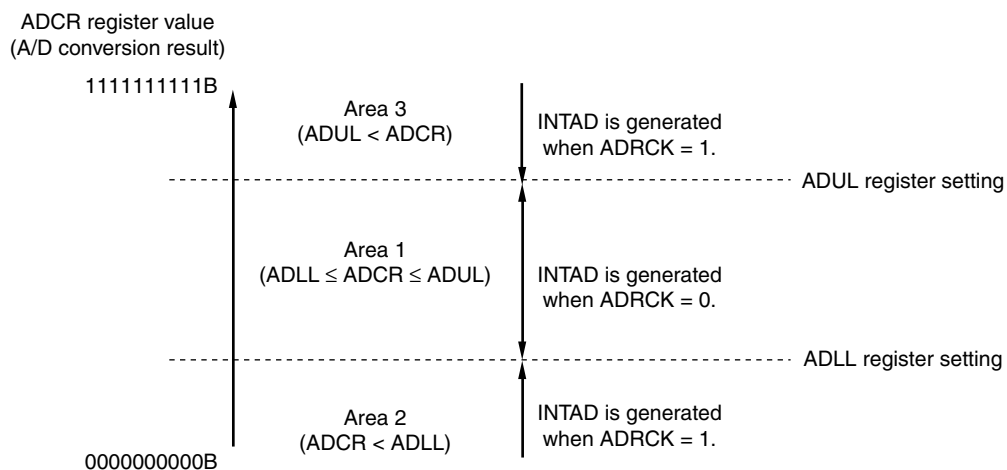
If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE or normal operation mode.

ADTYP	Selection of the A/D conversion resolution
0	12-bit resolution
1	8-bit resolution

<R>

<R> **Note** Refer to “From STOP to SNOOZE” in **18.3.3 SNOOZE mode**

Caution Only rewrite the value of the ADM2 register while conversion operation is stopped (which is indicated by the ADCE bit of A/D converter mode register 0 (ADM0) being 0).

Figure 11-8. ADRCK Bit Interrupt Signal Generation Range

Remark If INTAD does not occur, the A/D conversion result is not stored in the ADCR or ADCRH register.

11.3.5 12-bit A/D conversion result register (ADCR)

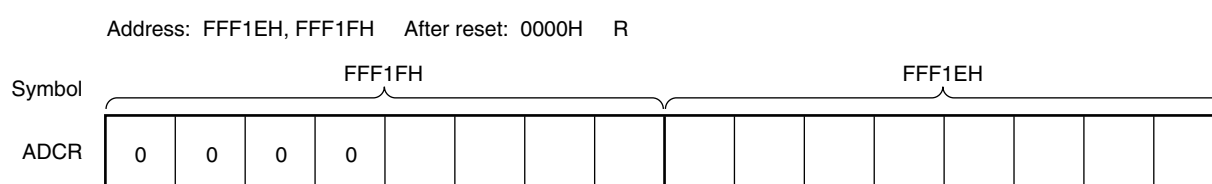
This register is a 16-bit register that stores the A/D conversion result in the select mode. The higher 4 bits are fixed to 0. Each time A/D conversion ends, the value of ADSAR [11:0] is stored in the A/D conversion result register (note that whether to store this value is determined by the setting of the ADRCK bit of the ADM2 register and by the settings of the ADUL and ADLL registers). The higher 4 bits of the conversion result are stored in FFF1FH and the lower 8 bits are stored in the lower 4 bits of FFF1EH^{Note}.

The ADCR register can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

<R> **Note** If the A/D conversion result is outside the range specified by using the A/D conversion comparison function (the value specified by the ADRCK bit of the ADM2 register and ADUL/ADLL registers; see Figure 11-8), the result is not stored.

Figure 11-9. Format of 12-bit A/D Conversion Result Register (ADCR)



- Cautions 1.** When writing to the A/D converter mode register 0 (ADM0), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of the ADCR register may become undefined. Read the conversion result following conversion completion before writing to the ADM0, ADS, and ADPC registers. Using timing other than the above may cause an incorrect conversion result to be read.
- 2.** If INTAD does not occur, the A/D conversion result is not stored in the ADCR register.

11.3.6 8-bit A/D conversion result register (ADCRH)

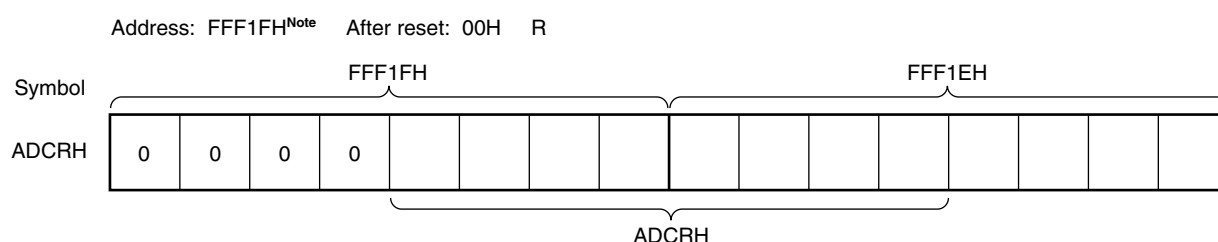
This register is an 8-bit register that indicate [11:4] bits of ADCR register. The higher 8 bits of 12-bit resolution are stored^{Note}.

The ADCRH register can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

<R> **Note** If the A/D conversion result is outside the range specified by using the A/D conversion comparison function (the value specified by the ADRCK bit of the ADM2 register and ADUL/ADLL registers; see Figure 11-8), the result is not stored.

Figure 11-10. Format of 8-bit A/D Conversion Result Register (ADCRH)



Note The ADCRH data (the lower 4 bits of FFF1FH + the higher 4 bits of FFF1EH) is to be read as a FFF1FH address.

- Cautions 1.** When writing to the A/D converter mode register 0 (ADM0), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of the ADCRH register may become undefined. Read the conversion result following conversion completion before writing to the ADM0, ADS, and ADPC registers. Using timing other than the above may cause an incorrect conversion result to be read.
- 2.** If INTAD does not occur, the A/D conversion result is not stored in the ADCRH register.

11.3.7 Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

The ADS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (1/2)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

○ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV _{REFF} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV _{REFM} pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	0	1	0	1	ANI5	P25/ANI5 pin
0	0	0	1	1	0	ANI6	P26/ANI6 pin
0	0	0	1	1	1	ANI7	P27/ANI7 pin
0	0	1	0	0	0	ANI8	P150/ANI8 pin
0	0	1	0	0	1	ANI9	P151/ANI9 pin
0	0	1	0	1	0	ANI10	P152/ANI10 pin
0	0	1	0	1	1	ANI11	P153/ANI11 pin
0	0	1	1	0	0	ANI12	P154/ANI12 pin
0	0	1	1	0	1	Setting prohibited	
0	0	1	1	1	0	Setting prohibited	
0	0	1	1	1	1	Setting prohibited	
0	1	0	0	0	0	ANI16	P03/ANI16 pin
0	1	0	0	0	1	ANI17	P02/ANI17 pin
0	1	0	0	1	0	ANI18	P10/ANI18 pin
0	1	0	0	1	1	ANI19	P120/ANI19 pin
0	1	0	1	0	0	ANI20	P11/ANI20 pin
0	1	0	1	0	1	ANI21	P12/ANI21 pin
0	1	0	1	1	0	ANI22	P13/ANI22 pin
0	1	0	1	1	1	ANI23	P14/ANI23 pin
0	1	1	0	0	0	ANI24	P15/ANI24 pin
0	1	1	0	0	1	ANI25	P51/ANI25 pin
0	1	1	0	1	0	ANI26	P50/ANI26 pin
0	1	1	0	1	1	ANI27	P30/ANI27 pin
0	1	1	1	0	0	ANI28	P70/ANI28 pin
0	1	1	1	0	1	ANI29	P31/ANI29 pin
0	1	1	1	1	0	ANI30	P41/ANI30 pin
0	1	1	1	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output Note
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V) Note
Other than the above						Setting prohibited	

<R>

Note This setting can be used only in HS (high-speed main) mode. For detail, refer to **Figure 24-3. Format of User Option Byte (000C2H/010C2H).**

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (2/2)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

○ Scan mode (ADMD = 1)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel			
						Scan 0	Scan 1	Scan 2	Scan 3
0	0	0	0	0	0	ANI0	ANI1	ANI2	ANI3
0	0	0	0	0	1	ANI1	ANI2	ANI3	ANI4
0	0	0	0	1	0	ANI2	ANI3	ANI4	ANI5
0	0	0	0	1	1	ANI3	ANI4	ANI5	ANI6
0	0	0	1	0	0	ANI4	ANI5	ANI6	ANI7
0	0	0	0	0	0	ANI5	ANI6	ANI7	ANI8
0	0	0	0	0	1	ANI6	ANI7	ANI8	ANI9
0	0	0	0	1	0	ANI7	ANI8	ANI9	ANI10
0	0	0	0	1	1	ANI8	ANI9	ANI10	ANI11
0	0	0	0	1	0	ANI9	ANI10	ANI11	ANI12
0	1	0	0	0	0	ANI16	ANI17	ANI18	ANI19
0	1	0	0	0	1	ANI17	ANI18	ANI19	ANI20
0	1	0	0	1	0	ANI18	ANI19	ANI20	ANI21
0	1	0	0	1	1	ANI19	ANI20	ANI21	ANI22
0	1	0	1	0	0	ANI20	ANI21	ANI22	ANI23
0	1	0	1	0	1	ANI21	ANI22	ANI23	ANI24
0	1	0	1	1	0	ANI22	ANI23	ANI24	ANI25
0	1	0	1	1	1	ANI23	ANI24	ANI25	ANI26
0	1	1	0	0	0	ANI24	ANI25	ANI26	ANI27
0	1	1	0	0	1	ANI25	ANI26	ANI27	ANI28
0	1	1	0	1	0	ANI26	ANI27	ANI28	ANI29
0	1	1	0	1	1	ANI27	ANI28	ANI29	ANI30
Other than the above						Setting prohibited			

- Cautions**
1. Be sure to clear bits 5 and 6 to 0.
 2. Set a channel to be set the analog input by ADPC and PMC registers in the input mode by using port mode registers0 to 5, 7, 12, or 15 (PM0 to PM5, PM7, PM12, PM15).
 3. Do not set the pin that is set by the A/D port configuration register (ADPC) as digital I/O by the ADS register.
 4. Do not set the pin that is set by port mode control register 0, 1, 3 to 5, 7, or 12 (PMC0, PMC1, PMC3 to PMC5, PMC7, PMC12) as digital I/O by the ADS register.
 5. Only rewrite the value of the ADISS bit while conversion operation is stopped (which is indicated by the ADCE bit of A/D voltage cooperator mode register 0 (ADM0) being 0).
 6. If using AV_{REFP} as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.
 7. If using AV_{REFM} as the – side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.
 8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source. Also, after setting the ADISS to 1, the result of the first conversion cannot be used. For details about the setting flow, refer to 11.7.4 Setup when using temperature sensor/internal reference voltage (ADISS = 1).
 9. Do not set the ADREFP1 bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. Also, if the ADREFP1 bit is set to 1, the temperature sensor operating current (I_{TMPs}) and A/D converter reference voltage current (I_{ADREF}) indicated in 29.3.2 and 30.3.2 Supply current characteristics will be added to the current consumption when shifting to HALT mode while the CPU is operating on the main system clock.
 10. Ignore the conversion result if the corresponding ANI pin does not exist in the product used.

11.3.8 Conversion result comparison upper limit setting register (ADUL)

This register is used to specify the setting for checking the upper limit of the A/D conversion results.

The A/D conversion results and ADUL register value are compared, and interrupt signal (INTAD) generation is controlled in the range specified for the ADRCK bit of A/D converter mode register 2 (ADM2) (shown in **Figure 11-8**).

The ADUL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

- Cautions**
1. When 12-bit resolution A/D conversion is selected, the higher eight bits of the 12-bit A/D conversion result register (ADCR) are compared with the ADUL register.
 2. Only rewrite the value of the ADUL register and ADLL register while conversion operation is stopped (which is indicated by the ADCE bit of A/D converter mode register 0 (ADM0) being 0).
 3. Make sure that ADUL > ADLL when setting these registers.

Figure 11-12. Format of Conversion Result Comparison Upper Limit Setting Register (ADUL)

Address: F0011H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
ADUL	ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0

11.3.9 Conversion result comparison lower limit setting register (ADLL)

This register is used to specify the setting for checking the lower limit of the A/D conversion results.

The A/D conversion results and ADLL register value are compared, and interrupt signal (INTAD) generation is controlled in the range specified for the ADRCK bit of A/D converter mode register 2 (ADM2) (shown in **Figure 11-8**).

The ADLL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-13. Format of Conversion Result Comparison Lower Limit Setting Register (ADLL)

Address: F0012H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADLL	ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0

- Cautions**
1. When 12-bit resolution A/D conversion is selected, the higher eight bits of the 12-bit A/D conversion result register (ADCR) are compared with the ADLL register.
 2. Only rewrite the value of the ADUL register and ADLL register while conversion operation is stopped (which is indicated by the ADCE bit of A/D converter mode register 0 (ADM0) being 0).
 3. Make sure that ADUL > ADLL when setting these registers.

11.3.10 A/D test register (ADTES)

This register is used to select the + side reference voltage or – side reference voltage of the A/D converter, or the analog input channel (ANLxx) as the A/D conversion target for the A/D test function.

The ADTES register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-14. Format of A/D Test Register (ADTES)

Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

<R>

ADTES1	ADTES0	A/D conversion target
0	0	ANLxx/temperature sensor output ^{Note} /internal reference voltage output (1.45 V) ^{Note} (This is specified using the analog input channel specification register (ADS).)
1	0	– side reference voltage (Setting at ADREFM bit of ADM2 register)
1	1	+ side reference voltage (Setting at ADREFP1, ADREFP0 bits of ADM2 register)
Other than the above		Setting prohibited

<R>

Note Temperature sensor output/internal reference voltage (1.45 V) can be used only in HS (high-speed main) mode. For detail, refer to **Figure 24-3. Format of User Option Byte (000C2H/010C2H)**.

<R>

Caution For details of the A/D test function, see CHAPTER 22 SAFETY FUNCTIONS.

11.3.11 A/D port configuration register (ADPC)

This register switches the ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI12/P154 pins to analog input of A/D converter or digital I/O of port.

The ADPC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-15. Format of A/D Port Configuration Register (ADPC)

Address: F0076H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching												
				ANI12/P154	ANI11/P153	ANI10/P152	ANI9/P151	ANI8/P150	ANI7/P27	ANI6/P26	ANI5/P25	ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	1	0	D	D	D	D	D	D	D	D	D	D	D	D	A
0	0	1	1	D	D	D	D	D	D	D	D	D	D	D	A	A
0	1	0	0	D	D	D	D	D	D	D	D	D	D	A	A	A
0	1	0	1	D	D	D	D	D	D	D	D	D	A	A	A	A
0	1	1	0	D	D	D	D	D	D	D	D	A	A	A	A	A
0	1	1	1	D	D	D	D	D	D	D	A	A	A	A	A	A
1	0	0	0	D	D	D	D	D	D	A	A	A	A	A	A	A
1	0	0	1	D	D	D	D	D	A	A	A	A	A	A	A	A
1	0	1	0	D	D	D	D	A	A	A	A	A	A	A	A	A
1	0	1	1	D	D	D	A	A	A	A	A	A	A	A	A	A
1	1	0	0	D	D	A	A	A	A	A	A	A	A	A	A	A
1	1	0	1	D	A	A	A	A	A	A	A	A	A	A	A	A
1	1	1	0	A	A	A	A	A	A	A	A	A	A	A	A	A
1	1	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A

- Cautions**
1. Set the port to analog input by ADPC register to the input mode by using port mode registers 2, 15 (PM2, PM15).
 2. Do not set the pin set by the ADPC register as digital I/O by the analog input channel specification register (ADS).
 3. When using AV_{REFP} and AV_{REFM} , specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.

11.3.12 Port mode control registers 0, 1, 3 to 5, 7, 12 (PMC0, PMC1, PMC3 to PMC5, PMC7, PMC12)

This register switches the ANI16 to ANI30 pins to digital I/O of port or analog input of A/D converter.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to FFH.

Figure 11-16. Format of Port Mode Control Register (64-pin products)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC1	1	1	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC3	1	1	1	1	1	1	PMC31	PMC30	F0063H	FFH	R/W

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC5	1	1	1	1	1	1	PMC51	PMC50	F0065H	FFH	R/W

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC12	1	1	1	1	1	1	1	PMC120	F006CH	FFH	R/W

PMCmn	Pmn pin digital I/O/analog input selection (m = 0, 1, 3 to 5, 7, 12; n = 0 to 5)
0	Digital I/O (alternate function other than analog input)
1	Analog input

<R> **Caution** When using AV_{REFP} and AV_{REFM}, specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.

11.3.13 Port mode register 0 to 5, 7, 12, 15 (PM0 to PM5, PM7, PM12, PM15)

When using the ANI0 to ANI12 or ANI16 to ANI30 pin for an analog input port, set the PMmn bit to 1. The output latches of Pnm at this time may be 0 or 1.

If the PMmn bits are set to 0, they cannot be used as analog input port pins.

The PMmn registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Caution If a pin is set as an analog input port, not the pin level but “0” is always read.

Remark m = 0 to 5, 7, 12, 15, n = 0 to 7

**Figure 11-17. Formats of Port Mode Registers 0 to 5, 7, 12, and 15 (PM0 to PM5, PM7, PM12, PM15)
(64-pin products)**

Address: FFF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

Address: FFF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

Address: FFF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	1	1	PM31	PM30

Address: FFF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	1	1	1	1	PM43	PM42	PM41	PM40

Address: FFF25H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM5	1	1	1	1	1	1	PM51	PM50

Address: FFF27H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70

Address: FFF2CH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM12	1	1	1	1	1	1	1	PM120

Address: FFF2FH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150

PMmn	Pmn pin I/O mode selection (m = 0 to 5, 7, 12, 15 ; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution When using AV_{REFP} and AV_{REFM}, specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register (PM20, PM21).

Remark For details of the port mode register other than 64-pin products, see **4.3 Registers Controlling Port Function**.

The ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI12/P154 pins are as shown below depending on the settings of the A/D port configuration register (ADPC), analog input channel specification register (ADS), PM2 and PM15 registers.

Table 11-4. Setting Functions of ANI0/P20 to ANI7/P27, ANI8/P150 to ANI12/P154 Pins

ADPC	PM2, PM15	ADS	ANI0/P20 to ANI7/P27, ANI8/P150 to ANI12/P154 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

The ANI16 to ANI30 pins are as shown below depending on the settings of port mode control registers 0, 1, 3 to 5, 7, and 12 (PMC0, PMC1, PMC3 to PMC5, PMC7, PMC12), analog input channel specification register (ADS), PM0, PM1, PM3, PM4, PM5, PM7, PM12, and PM15 registers.

Table 11-5. Setting Functions of ANI16 to ANI30 Pins

PMC0, PMC1, PMC3 to PMC5, PMC7, and PMC12	PM0, PM1, PM3, PM4, PM5, PM7, PM12, and PM15	ADS	ANI16 to ANI30 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

11.4 A/D Converter Conversion Operations

The A/D converter conversion operations are described below.

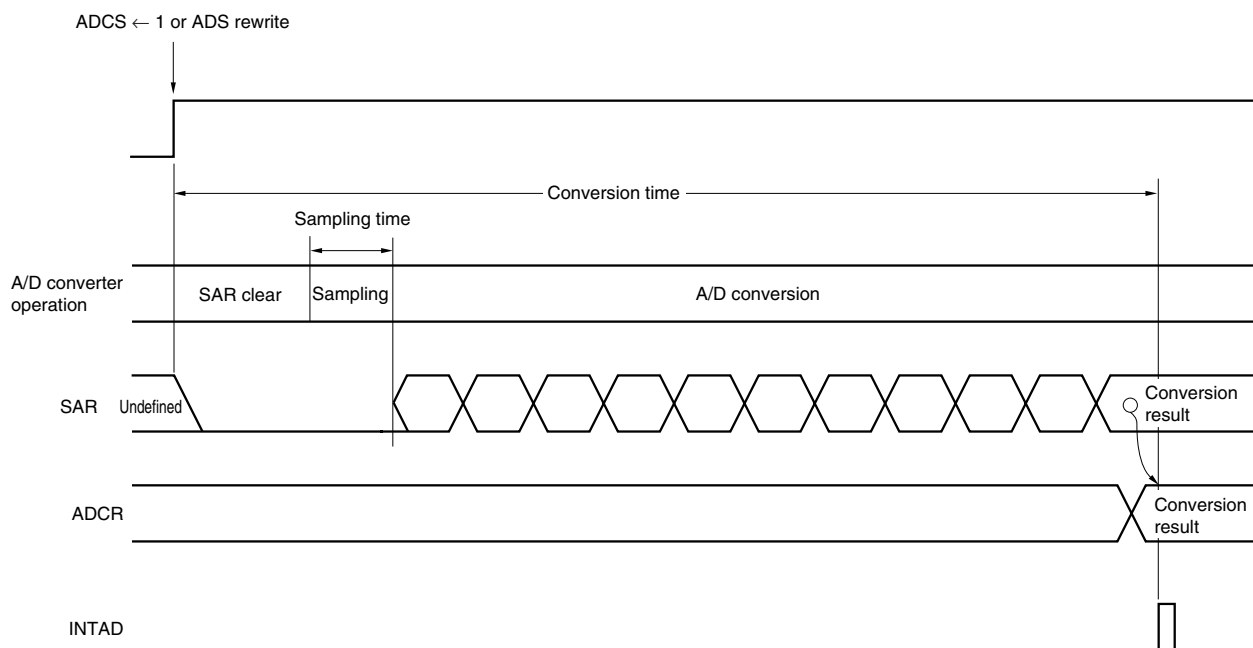
- <1> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.
- <2> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.
- <3> Bit 11 of the successive approximation register (SAR) is set. The series resistor string voltage tap is set to $(1/2) AV_{REF}$ by the tap selector.
- <4> The voltage difference between the series resistor string voltage tap and sampled voltage is compared by the voltage comparator. If the analog input is greater than $(1/2) AV_{REF}$, the MSB bit of the SAR register remains set to 1. If the analog input is smaller than $(1/2) AV_{REF}$, the MSB bit is reset to 0.
- <5> Next, bit 10 of the SAR register is automatically set to 1, and the operation proceeds to the next comparison. The series resistor string voltage tap is selected according to the preset value of bit 11, as described below.
 - Bit 11 = 1: $(3/4) AV_{REF}$
 - Bit 11 = 0: $(1/4) AV_{REF}$

The voltage tap and sampled voltage are compared and bit 10 of the SAR register is manipulated as follows.

- Sampled voltage $\geq$ Voltage tap: Bit 10 = 1
- Sampled voltage $<$ Voltage tap: Bit 10 = 0
- <6> Comparison is continued in this way up to bit 0 of the SAR register.
- <7> Upon completion of the comparison of 12 bits, an effective digital result value remains in the SAR register, and the result value is transferred to the A/D conversion result register (ADCR, ADCRH) and then latched^{Note 1}.
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated^{Note 1}.
- <8> Repeat steps <1> to <7>, until the ADCS bit is cleared to 0^{Note 2}.
To stop the A/D converter, clear the ADCS bit to 0.

- <R> **Notes**
1. If the A/D conversion result is outside the A/D conversion result range specified by the ADRCK bit and the ADUL and ADLL registers (see Figure 11-8), the A/D conversion result interrupt request signal is not generated and no A/D conversion results are stored in the ADCR and ADCRH registers.
 2. While in the sequential conversion mode, the ADCS flag is not automatically cleared to 0. This flag is not automatically cleared to 0 while in the one-shot conversion mode of the hardware trigger no-wait mode, either. Instead, 1 is retained.

- Remarks**
1. Two types of the A/D conversion result registers are available.
 - ADCR register (16 bits): Store 12-bit A/D conversion value
 - ADCRH register (8 bits): Store 8-bit A/D conversion value
 2. AV_{REF} : The + side reference voltage of the A/D converter. This can be selected from AV_{REFP} , the internal reference voltage (1.45 V), and AV_{DD} .

Figure 11-18. Conversion Operation of A/D Converter (Software Trigger Mode)

A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register (ADM) is reset (0) by software.

If a write operation is performed to the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH) to 0000H or 00H.

11.5 Input Voltage and Conversion Results

The relationship between the analog input voltage input to the analog input pins (ANI0 to ANI12, ANI16 to ANI30) and the theoretical A/D conversion result (stored in the 12-bit A/D conversion result register (ADCR)) is shown by the following expression.

$$\text{ADCR} = \text{INT} \left(\frac{V_{\text{AIN}}}{V_{\text{REF}}} \times 4096 + 0.5 \right)$$

or

$$(\text{ADCR} - 0.5) \times \frac{V_{\text{REF}}}{4096} \leq V_{\text{AIN}} < (\text{ADCR} + 0.5) \times \frac{V_{\text{REF}}}{4096}$$

where, INT(): Function which returns integer part of value in parentheses

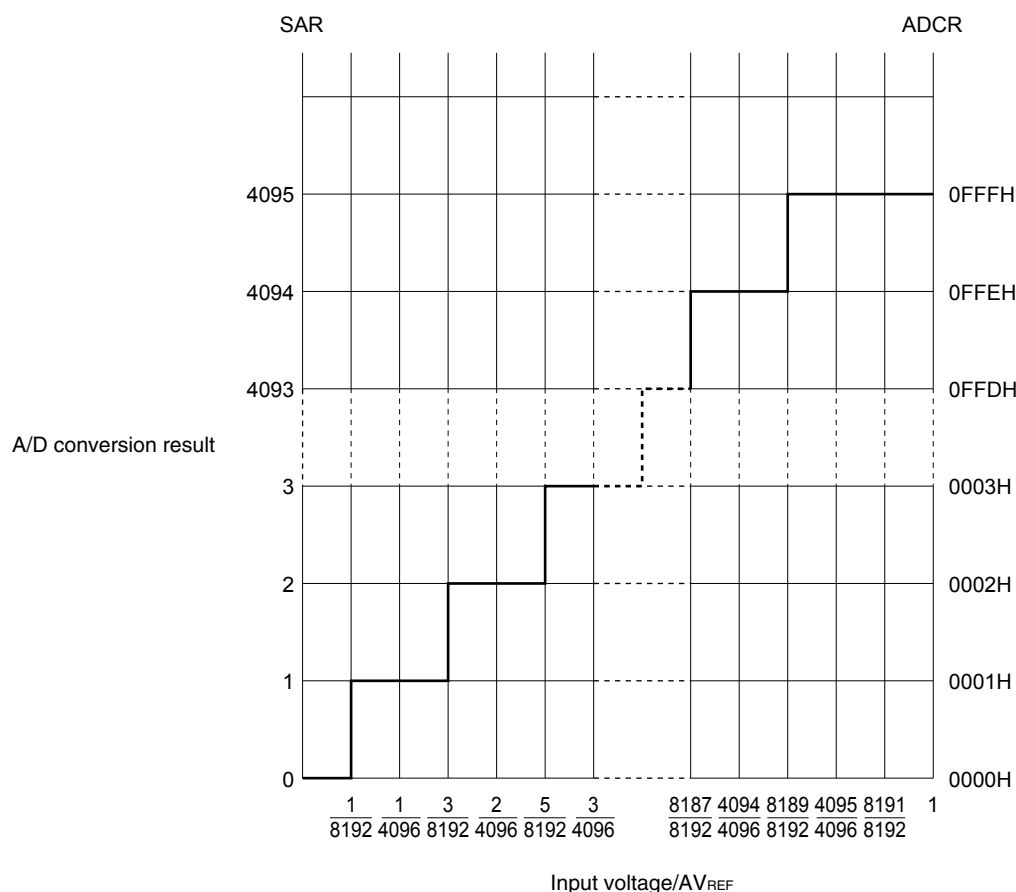
V_{AIN} : Analog input voltage

V_{REF} : V_{REF} pin voltage

ADCR: A/D conversion result register (ADCR) value

Figure 11-19 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 11-19. Relationship Between Analog Input Voltage and A/D Conversion Result



Remark V_{REF} : The + side reference voltage of the A/D converter. This can be selected from V_{REFP} , the internal reference voltage (1.45 V), and V_{DD} .

11.6 A/D Converter Operation Modes

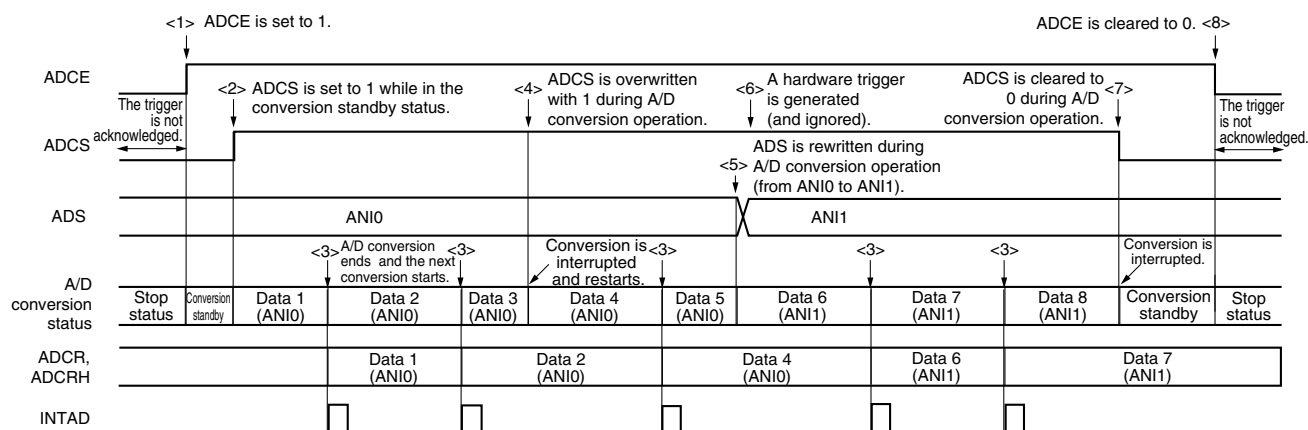
The operation of each A/D converter mode is described below. In addition, the procedure for specifying each mode is described in **11.7 A/D Converter Setup Flowchart**.

11.6.1 Software trigger mode (select mode, sequential conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time^{Note}, the ADCS bit of the ADM0 register is set to 1 to perform the A/D conversion of the analog input specified by the analog input channel specification register (ADS).
- <3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion ends, the next A/D conversion immediately starts.
- <4> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <5> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <6> Even if a hardware trigger is input during conversion operation, A/D conversion does not start.
- <7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status.
- <8> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start.

Note If a high-accuracy channel is selected as the analog input channel: Stabilization wait time = 0.5 μ s
 If a standard channel is selected as the analog input channel: Stabilization wait time = 2 μ s

Figure 11-20. Example of Software Trigger Mode (Select Mode, Sequential Conversion Mode) Operation Timing

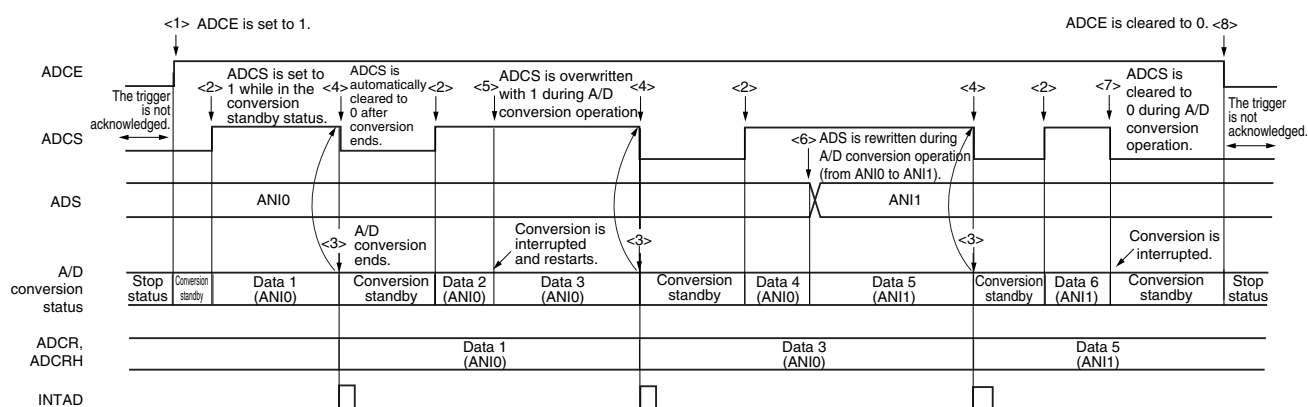


11.6.2 Software trigger mode (select mode, one-shot conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time^{Note}, the ADCS bit of the ADM0 register is set to 1 to perform the A/D conversion of the analog input specified by the analog input channel specification register (ADS).
- <3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated.
- <4> After A/D conversion ends, the ADCS bit is automatically cleared to 0, and the system enters the A/D conversion standby status.
- <5> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status.
- <8> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start. In addition, A/D conversion does not start even if a hardware trigger is input while in the A/D conversion standby status.

Note If a high-accuracy channel is selected as the analog input channel: Stabilization wait time = 0.5 μ s
 If a standard channel is selected as the analog input channel: Stabilization wait time = 2 μ s

Figure 11-21. Example of Software Trigger Mode (Select Mode, One-Shot Conversion Mode) Operation Timing



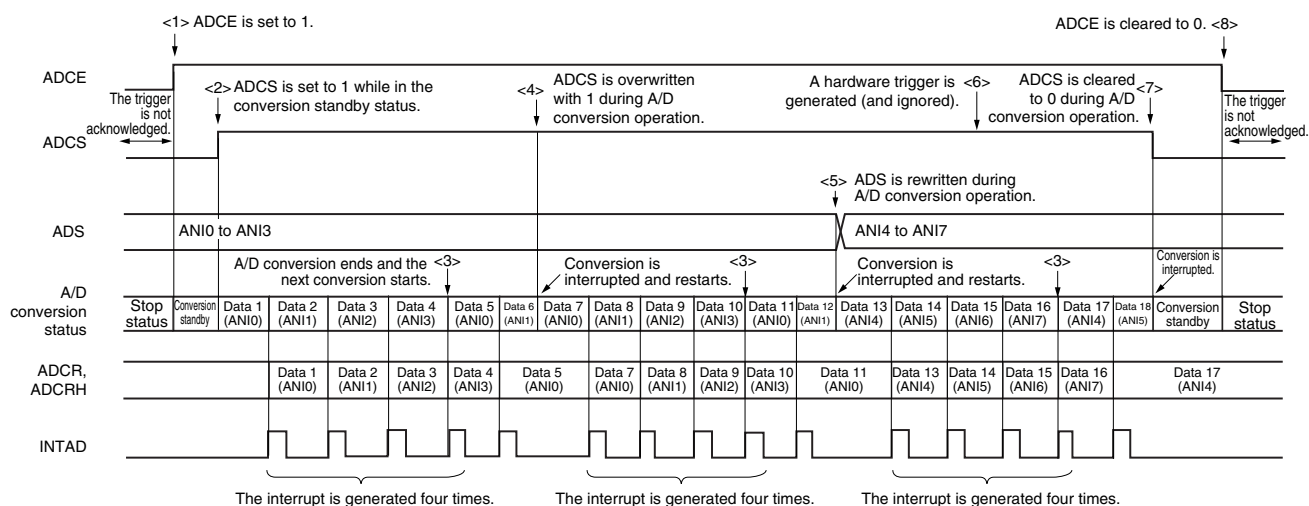
11.6.3 Software trigger mode (scan mode, sequential conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time^{Note}, the ADCS bit of the ADM0 register is set to 1 to perform A/D conversion on the four analog input channels specified by scan 0 to scan 3, which are specified by the analog input channel specification register (ADS). A/D conversion is performed on the analog input channels in order, starting with that specified by scan 0.
- <3> A/D conversion is sequentially performed on the four analog input channels, the conversion results are stored in the A/D conversion result register (ADCR, ADCRH) each time conversion ends, and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion of the four channels ends, the A/D conversion of the channel following the specified channel automatically starts (until all four channels are finished).
- <4> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.
- <5> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the first channel respecified by the ADS register. The partially converted data is discarded.
- <6> Even if a hardware trigger is input during conversion operation, A/D conversion does not start.
- <7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status.
- <8> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start.

Note If a high-accuracy channel is selected as the analog input channel: Stabilization wait time = 0.5 μ s

If a standard channel is selected as the analog input channel: Stabilization wait time = 2 μ s

Figure 11-22. Example of Software Trigger Mode (Scan Mode, Sequential Conversion Mode) Operation Timing

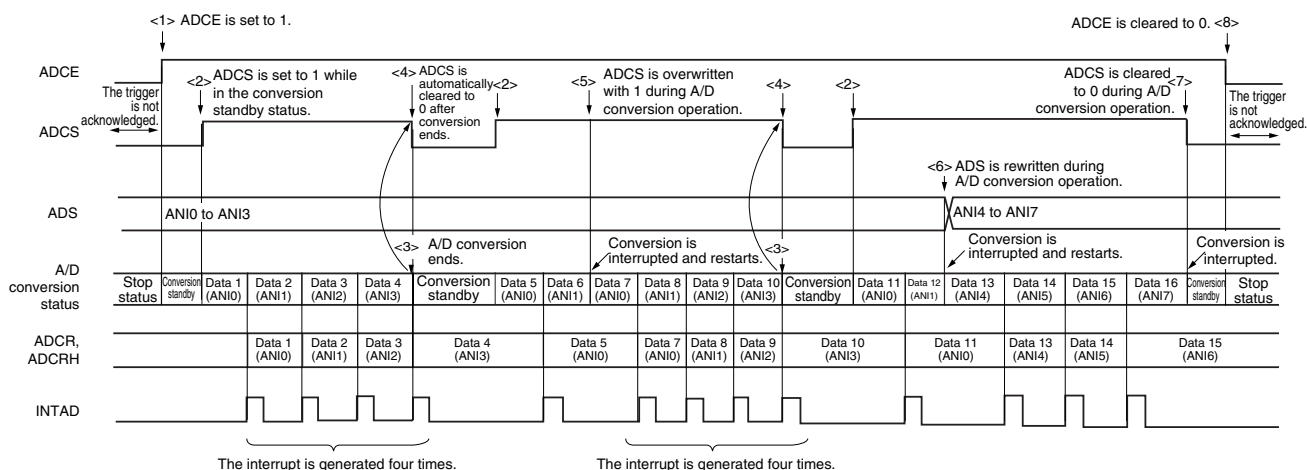


11.6.4 Software trigger mode (scan mode, one-shot conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time^{Note}, the ADCS bit of the ADM0 register is set to 1 to perform A/D conversion on the four analog input channels specified by scan 0 to scan 3, which are specified by the analog input channel specification register (ADS). A/D conversion is performed on the analog input channels in order, starting with that specified by scan 0.
- <3> A/D conversion is sequentially performed on the four analog input channels, the conversion results are stored in the A/D conversion result register (ADCR, ADCRH) each time conversion ends, and the A/D conversion end interrupt request signal (INTAD) is generated.
- <4> After A/D conversion of the four channels ends, the ADCS bit is automatically cleared to 0, and the system enters the A/D conversion standby status.
- <5> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.
- <6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the first channel respecified by the ADS register. The partially converted data is discarded.
- <7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status.
- <8> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start. In addition, A/D conversion does not start even if a hardware trigger is input while in the A/D conversion standby status.

Note If a high-accuracy channel is selected as the analog input channel: Stabilization wait time = 0.5 μ s
 If a standard channel is selected as the analog input channel: Stabilization wait time = 2 μ s

Figure 11-23. Example of Software Trigger Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing

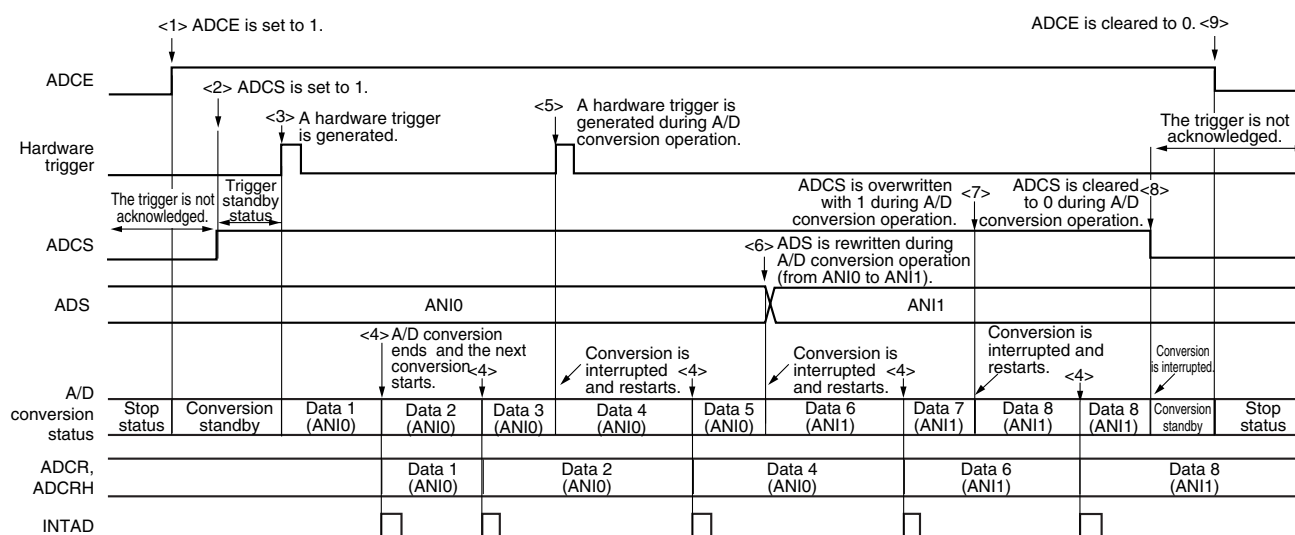


11.6.5 Hardware trigger no-wait mode (select mode, sequential conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time^{Note}, the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.
- <3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS).
- <4> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion ends, the next A/D conversion immediately starts.
- <5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not stop in this status.
- <9> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCS = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Note If a high-accuracy channel is selected as the analog input channel: Stabilization wait time = 0.5 μ s
 If a standard channel is selected as the analog input channel: Stabilization wait time = 2 μ s

Figure 11-24. Example of Hardware Trigger No-Wait Mode (Select Mode, Sequential Conversion Mode) Operation Timing

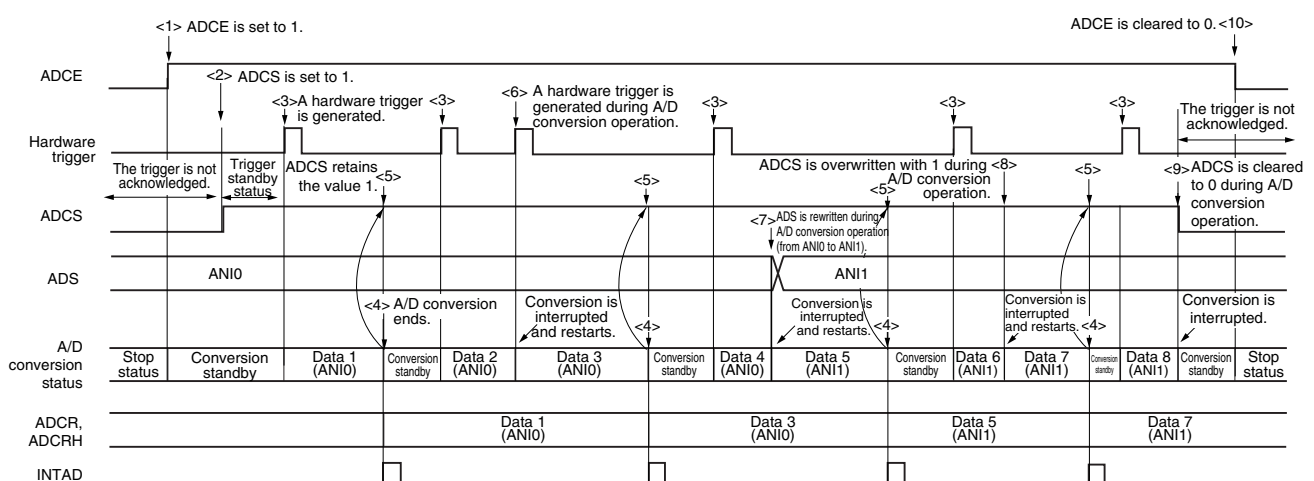


11.6.6 Hardware trigger no-wait mode (select mode, one-shot conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time^{Note}, the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.
- <3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS).
- <4> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated.
- <5> After A/D conversion ends, the ADCS bit remains set to 1, and the system enters the A/D conversion standby status.
- <6> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <7> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <8> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <9> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not stop in this status.
- <10> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCS = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Note If a high-accuracy channel is selected as the analog input channel: Stabilization wait time = 0.5 μ s
 If a standard channel is selected as the analog input channel: Stabilization wait time = 2 μ s

Figure 11-25. Example of Hardware Trigger No-Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing

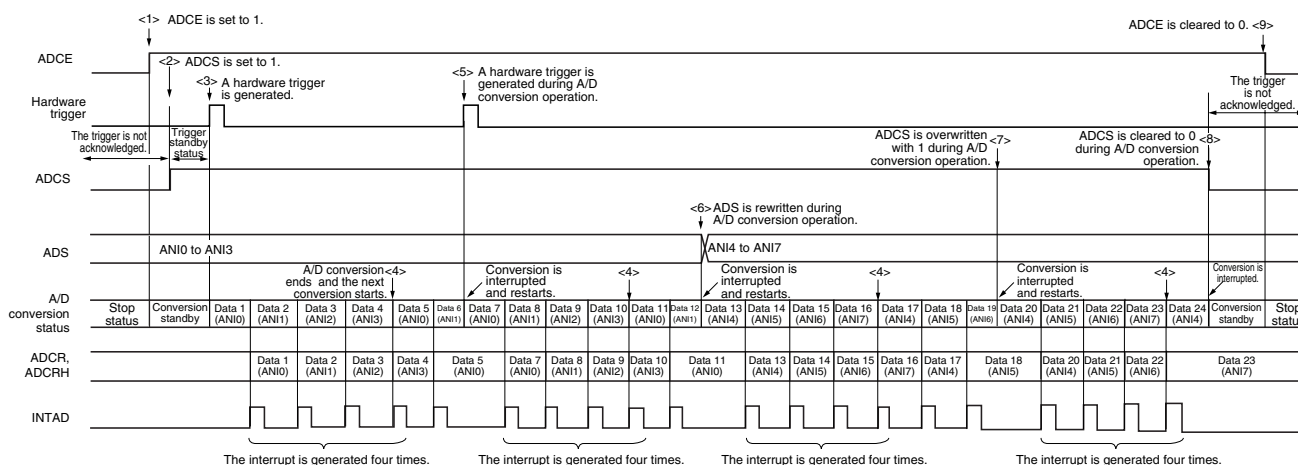


11.6.7 Hardware trigger no-wait mode (scan mode, sequential conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time^{Note}, the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.
- <3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the four analog input channels specified by scan 0 to scan 3, which are specified by the analog input channel specification register (ADS). A/D conversion is performed on the analog input channels in order, starting with that specified by scan 0.
- <4> A/D conversion is sequentially performed on the four analog input channels, the conversion results are stored in the A/D conversion result register (ADCR, ADCRH) each time conversion ends, and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion of the four channels ends, the A/D conversion of the channel following the specified channel automatically starts.
- <5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.
- <6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the first channel respecified by the ADS register. The partially converted data is discarded.
- <7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.
- <8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not stop in this status.
- <9> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start.

Note If a high-accuracy channel is selected as the analog input channel: Stabilization wait time = $0.5 \mu\text{s}$
 If a standard channel is selected as the analog input channel: Stabilization wait time = $2 \mu\text{s}$

Figure 11-26. Example of Hardware Trigger No-Wait Mode (Scan Mode, Sequential Conversion Mode) Operation Timing

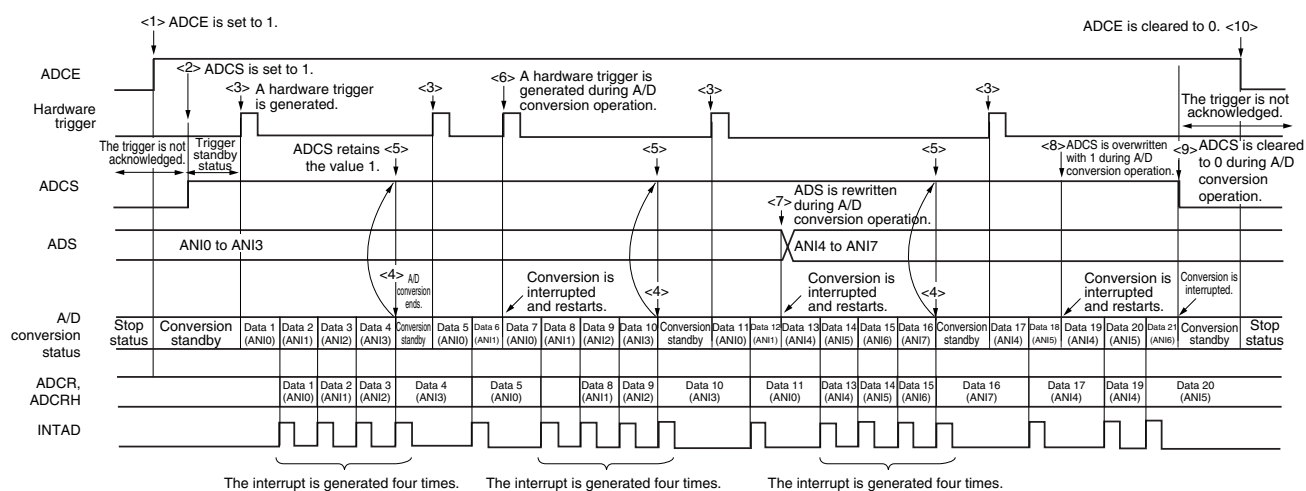


11.6.8 Hardware trigger no-wait mode (scan mode, one-shot conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time^{Note}, the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.
- <3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the four analog input channels specified by scan 0 to scan 3, which are specified by the analog input channel specification register (ADS). A/D conversion is performed on the analog input channels in order, starting with that specified by scan 0.
- <4> A/D conversion is sequentially performed on the four analog input channels, the conversion results are stored in the A/D conversion result register (ADCR, ADCRH) each time conversion ends, and the A/D conversion end interrupt request signal (INTAD) is generated.
- <5> After A/D conversion of the four channels ends, the ADCS bit remains set to 1, and the system enters the A/D conversion standby status.
- <6> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.
- <7> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the first channel respecified by the ADS register. The partially converted data is discarded.
- <8> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.
- <9> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not stop in this status.
- <10> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCS = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Note If a high-accuracy channel is selected as the analog input channel: Stabilization wait time = 0.5 μ s
 If a standard channel is selected as the analog input channel: Stabilization wait time = 2 μ s

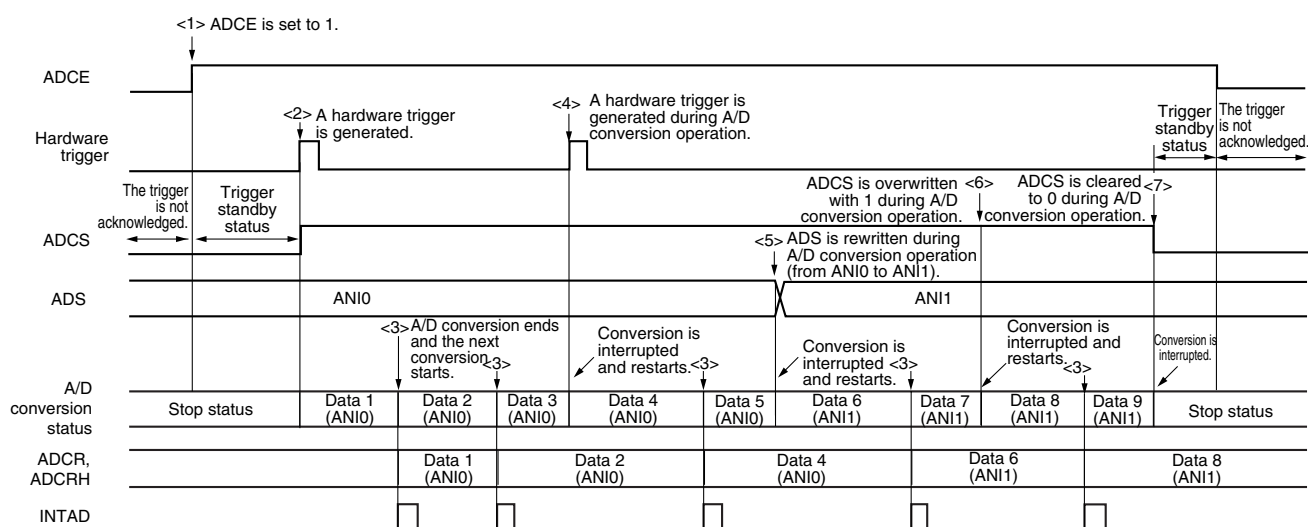
Figure 11-27. Example of Hardware Trigger No-Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing



11.6.9 Hardware trigger wait mode (select mode, sequential conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the hardware trigger standby status.
- <2> If a hardware trigger is input while in the hardware trigger standby status, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS). The ADCS bit of the ADM0 register is automatically set to 1 according to the hardware trigger input.
- <3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion ends, the next A/D conversion immediately starts. (At this time, no hardware trigger is necessary.)
- <4> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <5> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <6> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the system enters the hardware trigger standby status, and the A/D converter enters the stop status. When ADCE = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

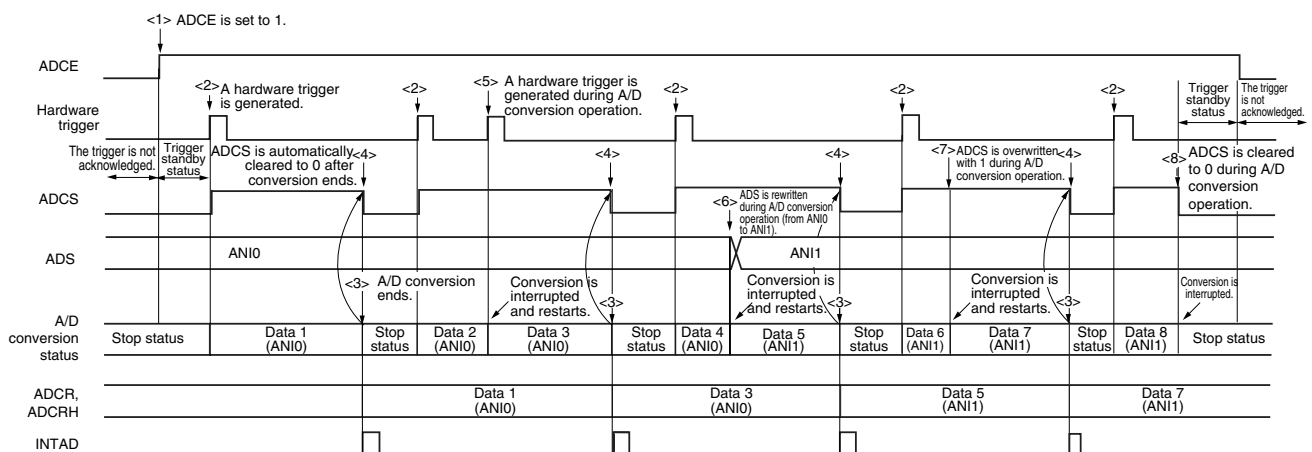
Figure 11-28. Example of Hardware Trigger Wait Mode (Select Mode, Sequential Conversion Mode) Operation Timing



11.6.10 Hardware trigger wait mode (select mode, one-shot conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the hardware trigger standby status.
- <2> If a hardware trigger is input while in the hardware trigger standby status, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS). The ADCS bit of the ADM0 register is automatically set to 1 according to the hardware trigger input.
- <3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated.
- <4> After A/D conversion ends, the ADCS bit is automatically cleared to 0, and the A/D converter enters the stop status.
- <5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is initialized.
- <8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the system enters the hardware trigger standby status, and the A/D converter enters the stop status. When ADCE = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

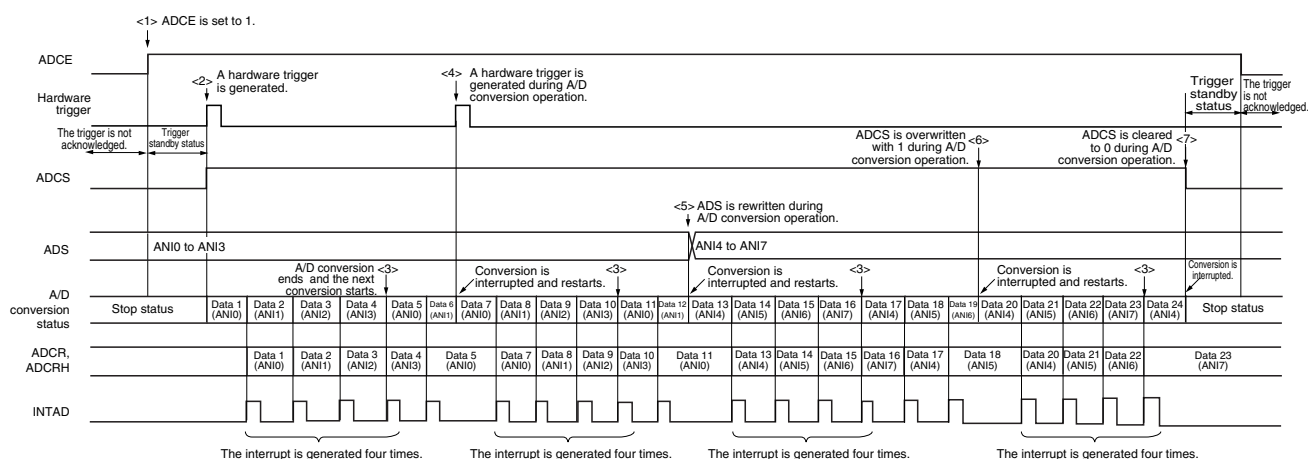
Figure 11-29. Example of Hardware Trigger Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing



11.6.11 Hardware trigger wait mode (scan mode, sequential conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> If a hardware trigger is input while in the hardware trigger standby status, A/D conversion is performed on the four analog input channels specified by scan 0 to scan 3, which are specified by the analog input channel specification register (ADS). The ADCS bit of the ADM0 register is automatically set to 1 according to the hardware trigger input. A/D conversion is performed on the analog input channels in order, starting with that specified by scan 0.
- <3> A/D conversion is sequentially performed on the four analog input channels, the conversion results are stored in the A/D conversion result register (ADCR, ADCRH) each time conversion ends, and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion of the four channels ends, the A/D conversion of the channel following the specified channel automatically starts.
- <4> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.
- <5> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the first channel respecified by the ADS register. The partially converted data is discarded.
- <6> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.
- <7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the system enters the hardware trigger standby status, and the A/D converter enters the stop status. When ADCE = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

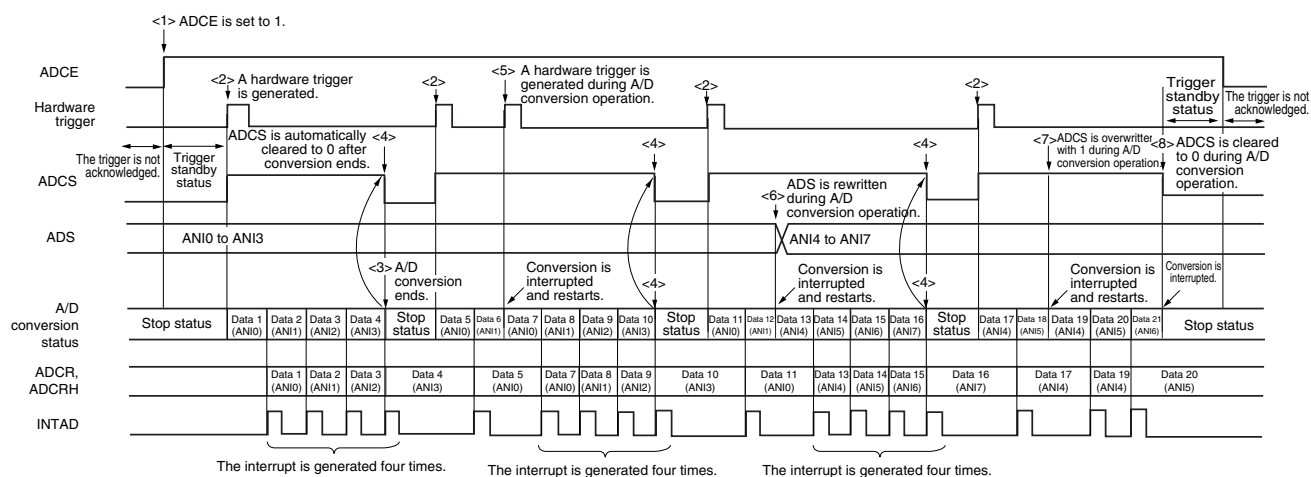
Figure 11-30. Example of Hardware Trigger Wait Mode (Scan Mode, Sequential Conversion Mode) Operation Timing



11.6.12 Hardware trigger wait mode (scan mode, one-shot conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> If a hardware trigger is input while in the hardware trigger standby status, A/D conversion is performed on the four analog input channels specified by scan 0 to scan 3, which are specified by the analog input channel specification register (ADS). The ADCS bit of the ADM0 register is automatically set to 1 according to the hardware trigger input. A/D conversion is performed on the analog input channels in order, starting with that specified by scan 0.
- <3> A/D conversion is sequentially performed on the four analog input channels, the conversion results are stored in the A/D conversion result register (ADCR, ADCRH) each time conversion ends, and the A/D conversion end interrupt request signal (INTAD) is generated.
- <4> After A/D conversion ends, the ADCS bit is automatically cleared to 0, and the A/D converter enters the stop status.
- <5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.
- <6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the first channel respecified by the ADS register. The partially converted data is discarded.
- <7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.
- <8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the system enters the hardware trigger standby status, and the A/D converter enters the stop status. When ADCE = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Figure 11-31. Example of Hardware Trigger Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing

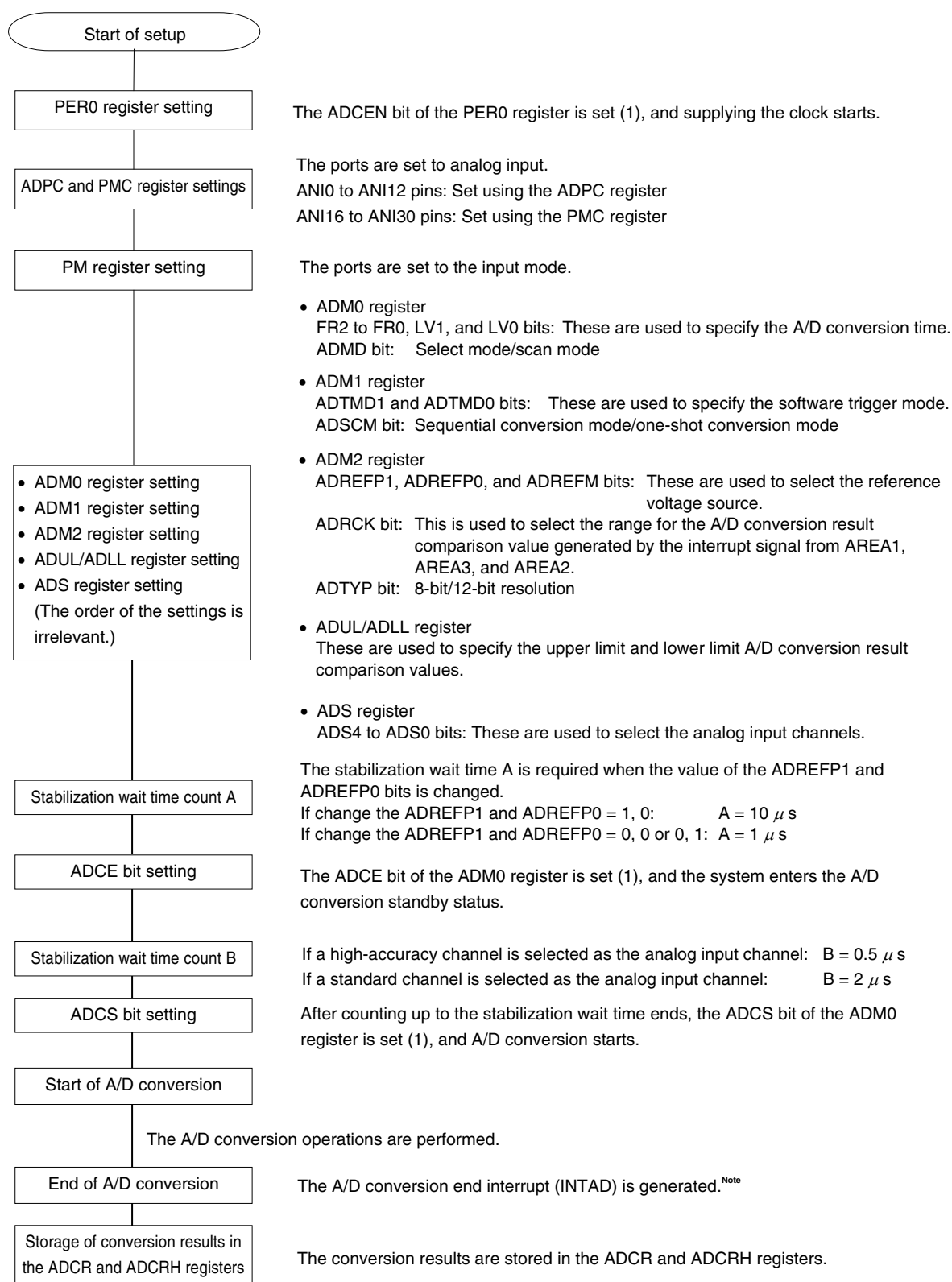


11.7 A/D Converter Setup Flowchart

The A/D converter setup flowchart in each operation mode is described below.

11.7.1 Setting up software trigger mode

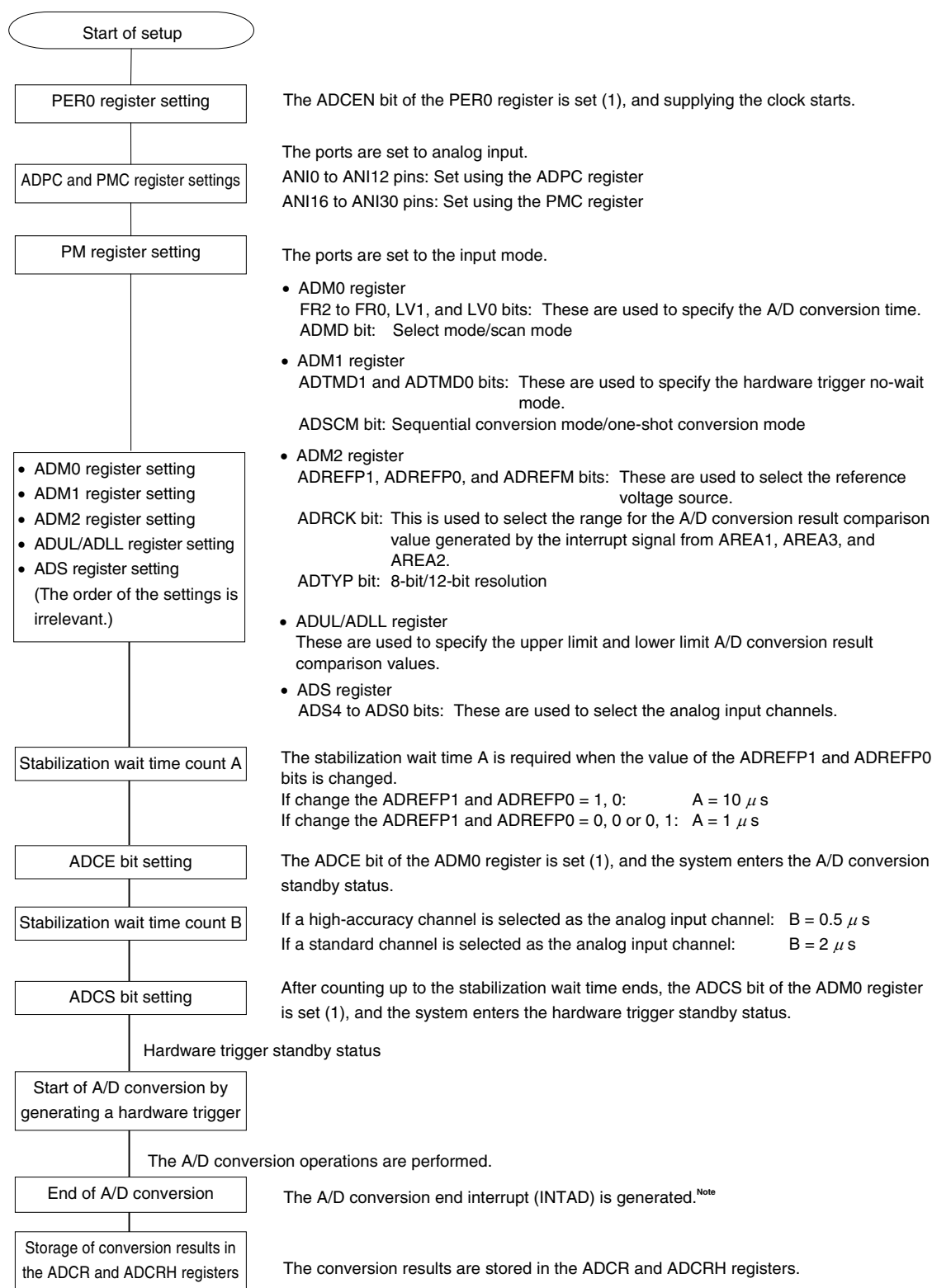
Figure 11-32. Setting up Software Trigger Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

11.7.2 Setting up hardware trigger no-wait mode

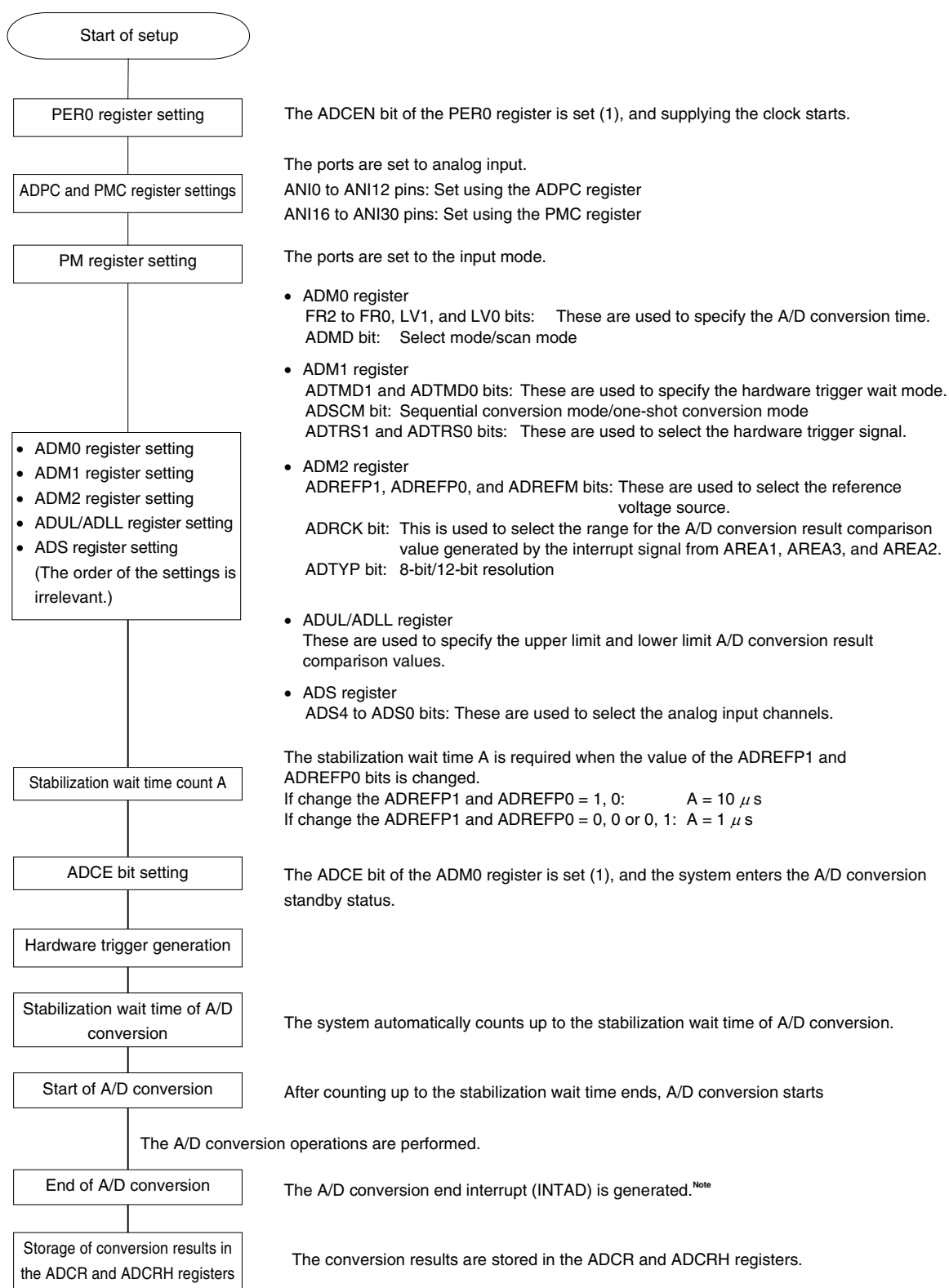
Figure 11-33. Setting up Hardware Trigger No-Wait Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

11.7.3 Setting up hardware trigger wait mode

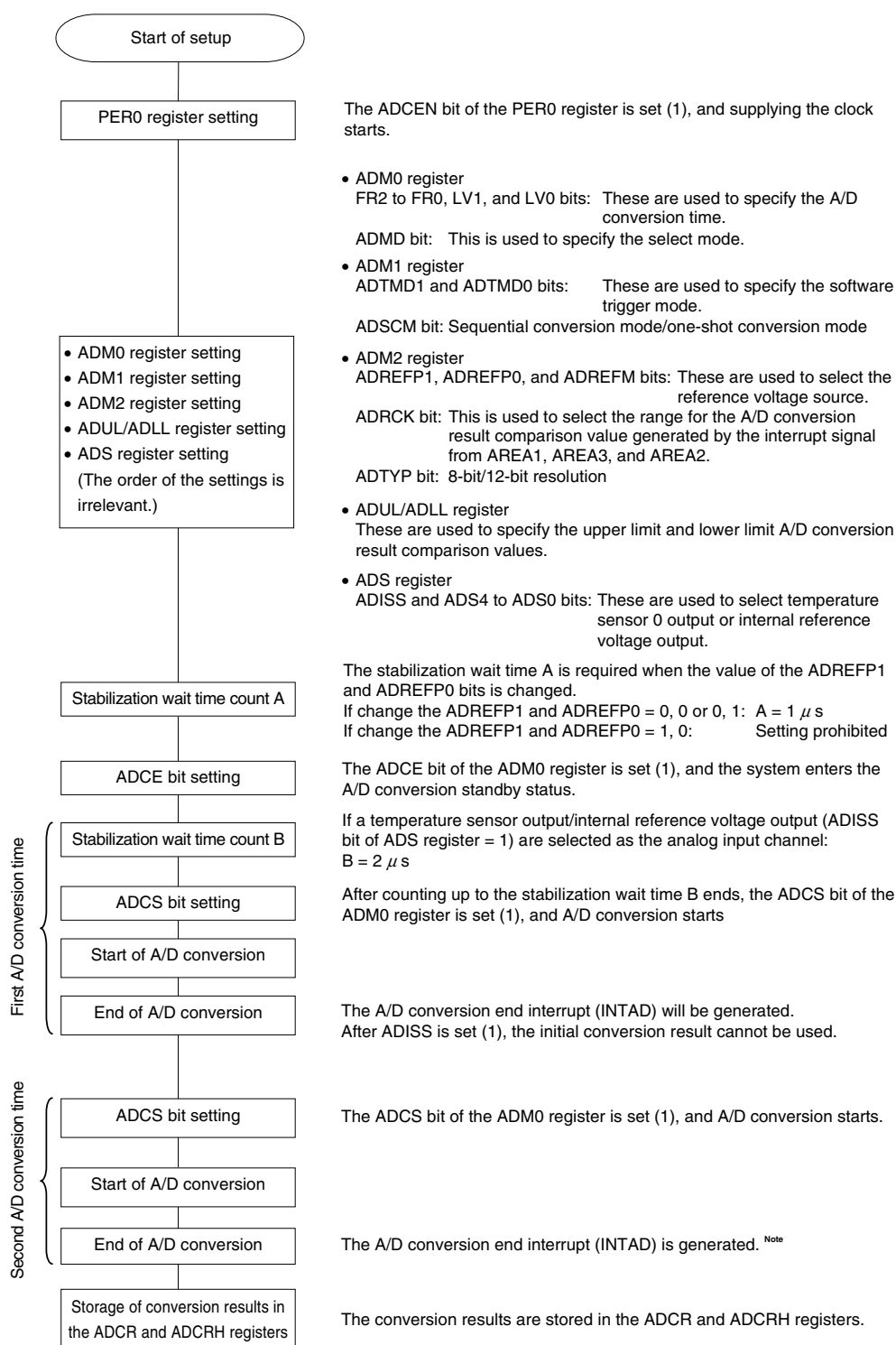
Figure 11-34. Setting up Hardware Trigger Wait Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

11.7.4 Setup when using temperature sensor/internal reference voltage (ADISS = 1) (example for software trigger mode and one-shot conversion mode)

Figure 11-35. Setup when using temperature sensor/internal reference voltage (ADISS = 1)

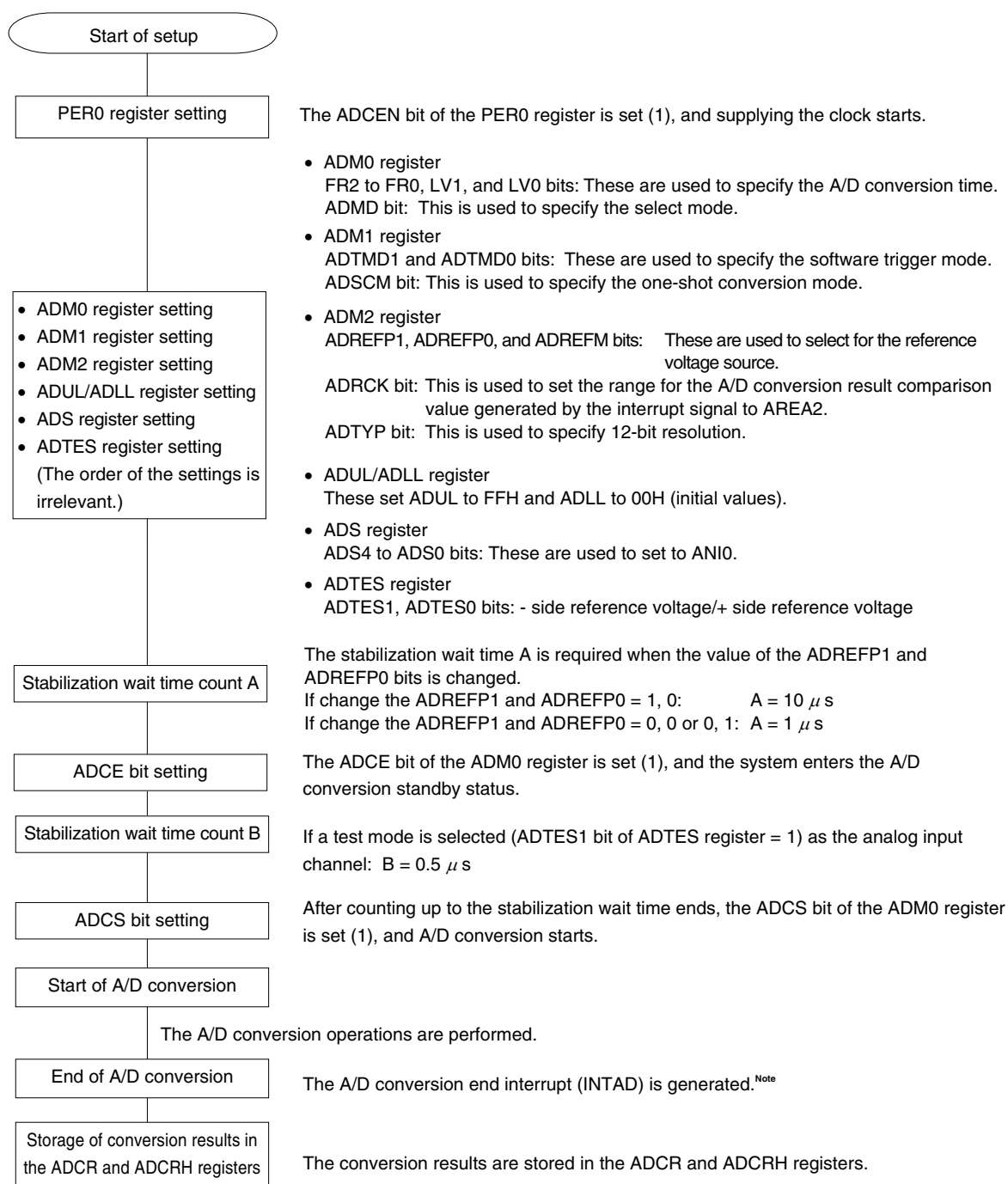


Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

<R> **Caution** This setting can be used only in HS (high-speed main) mode. For detail, refer to Figure 24-3. Format of User Option Byte (000C2H/010C2H).

11.7.5 Setting up test mode

Figure 11-36. Setting up Test Trigger Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

11.8 SNOOZE Mode Function

In the SNOOZE mode, A/D conversion is triggered by inputting a hardware trigger in the STOP mode. Normally, A/D conversion is stopped while in the STOP mode, but, by using the SNOOZE mode, A/D conversion can be performed without operating the CPU by inputting a hardware trigger. This is effective for reducing the operation current.

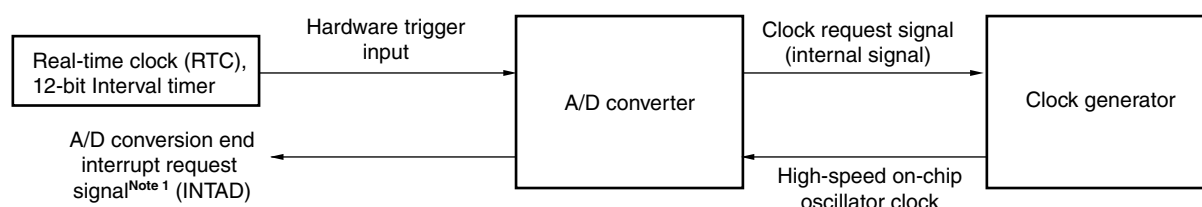
<R> If the A/D conversion result range is specified using the ADUL and ADLL registers, A/D conversion results can be judged at a certain interval of time in SNOOZE mode. Using this function enables power supply voltage monitoring and input key judgment based on A/D inputs.

In the SNOOZE mode, only the following two conversion modes can be used:

- Hardware trigger wait mode (select mode, one-shot conversion mode)
- Hardware trigger wait mode (scan mode, one-shot conversion mode)

Caution The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for f_{CLK} .

Figure 11-37. Block Diagram When Using SNOOZE Mode Function



When using the SNOOZE mode function, the initial setting of each register is specified before switching to the STOP mode. (For details about these settings, see 11.7.3 **Setting up hardware trigger wait mode**^{Note 2}.) Just before move to STOP mode, bit 2 (AWC) of A/D converter mode register 2 (ADM2) is set to 1. After the initial settings are specified, bit 0 (ADCE) of A/D converter mode register 0 (ADM0) is set to 1.

If a hardware trigger is input after switching to the STOP mode, the high-speed on-chip oscillator clock is supplied to the A/D converter. After supplying this clock, the system automatically counts up to the stabilization wait time, and then A/D conversion starts.

The SNOOZE mode operation after A/D conversion ends differs depending on whether an interrupt signal is generated^{Note 1}.

- Notes**
1. Depending on the setting of the A/D conversion result comparison function (ADRCK bit, ADUL/ADLL register), there is a possibility of no interrupt signal being generated.
 2. Be sure to set the ADM1 register to E2H or E3H.

Remark The hardware trigger is INTRTC or INTIT.

Specify the hardware trigger by using the A/D Converter Mode Register 1 (ADM1).

(1) If an interrupt is generated after A/D conversion ends

If the A/D conversion result value is inside the range of values specified by the A/D conversion result comparison function (which is set up by using the ADRCK bit and ADUL/ADLL register), the A/D conversion end interrupt request signal (INTAD) is generated.

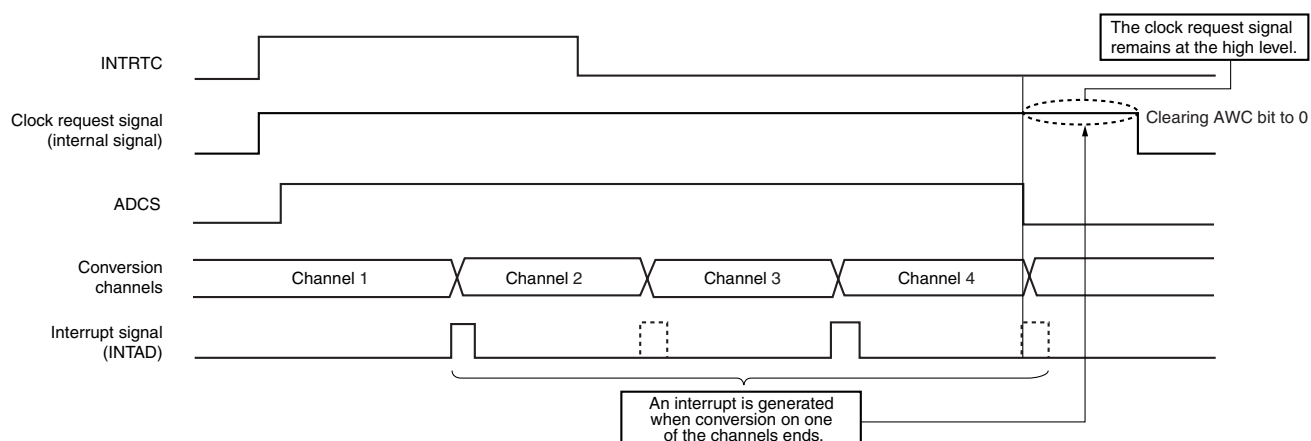
- While in the select mode

<R> When A/D conversion ends and an A/D conversion end interrupt request signal (INTAD) is generated, the A/D converter returns to normal operation mode from SNOOZE mode. At this time, be sure to clear bit 2 (AWC = 0: SNOOZE mode release) of the A/D converter mode register 2 (ADM2). If the AWC bit is left set to 1, A/D conversion will not start normally in the subsequent SNOOZE or normal operation mode.

- While in the scan mode

<R> If even one A/D conversion end interrupt request signal (INTAD) is generated during A/D conversion of the four channels, the clock request signal remains at the high level, and the A/D converter switches from the SNOOZE mode to the normal operation mode. At this time, be sure to clear bit 2 (AWC = 0: SNOOZE mode release) of A/D converter mode register 2 (ADM2) to 0. If the AWC bit is left set to 1, A/D conversion will not start normally in the subsequent SNOOZE or normal operation mode.

Figure 11-38. Operation Example When Interrupt Is Generated After A/D Conversion Ends (While in Scan Mode)



(2) If no interrupt is generated after A/D conversion ends

If the A/D conversion result value is outside the range of values specified by the A/D conversion result comparison function (which is set up by using the ADRCK bit and ADUL/ADLL register), the A/D conversion end interrupt request signal (INTAD) is not generated.

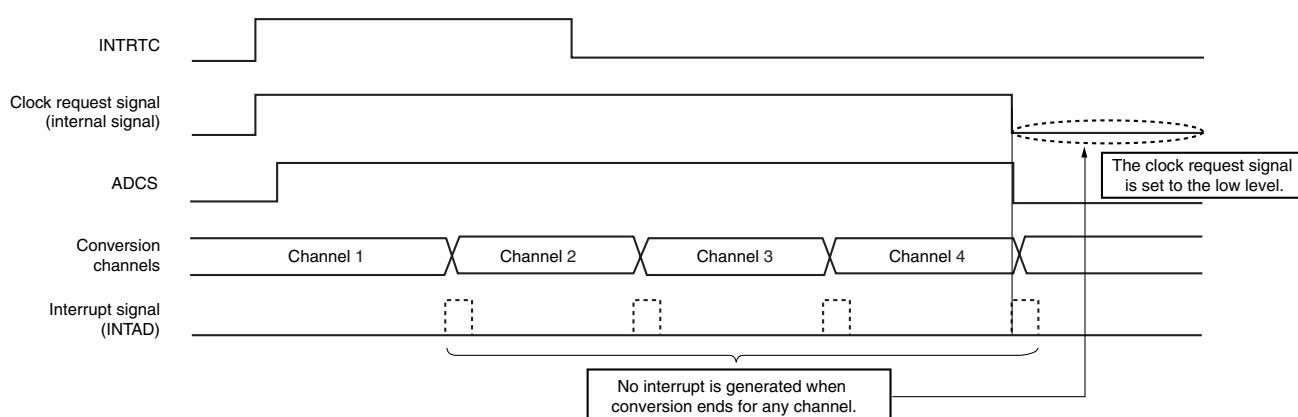
- While in the select mode

If the A/D conversion end interrupt request signal (INTAD) is not generated after A/D conversion ends, the clock request signal (an internal signal) is automatically set to the low level, and supplying the high-speed on-chip oscillator clock stops. If a hardware trigger is input later, A/D conversion work is again performed in the SNOOZE mode.

- While in the scan mode

If the A/D conversion end interrupt request signal (INTAD) is not generated even once during A/D conversion of the four channels, the clock request signal (an internal signal) is automatically set to the low level after A/D conversion of the four channels ends, and supplying the high-speed on-chip oscillator clock stops. If a hardware trigger is input later, A/D conversion work is again performed in the SNOOZE mode.

Figure 11-39. Operation Example When No Interrupt Is Generated After A/D Conversion Ends (While in Scan Mode)



11.9 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 12 bits.

$$1\text{LSB} = 1/2^{12} = 1/4096$$

$$\approx 0.024\%\text{FSR}$$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.

Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.

Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a $\pm 1/2\text{LSB}$ error naturally occurs. In an A/D converter, an analog input voltage in a range of $\pm 1/2\text{LSB}$ is converted to the same digital code, so a quantization error cannot be avoided.

Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 11-40. Overall Error

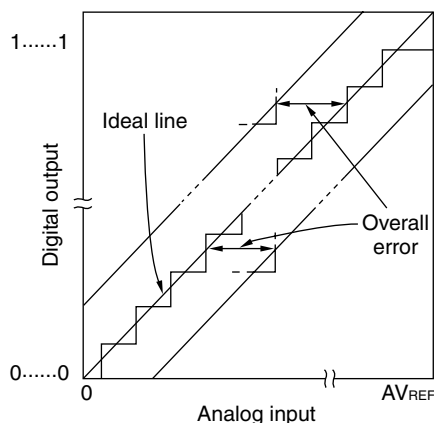
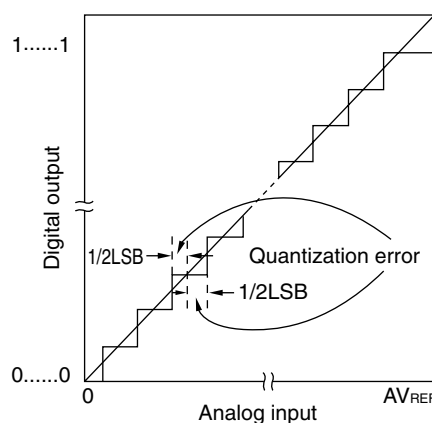


Figure 11-41. Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value ($1/2\text{LSB}$) when the digital output changes from 0.....000 to 0.....001.

If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value ($3/2\text{LSB}$) when the digital output changes from 0.....001 to 0.....010.

(5) Full-scale error

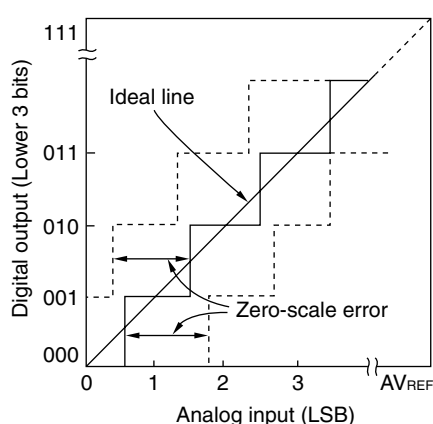
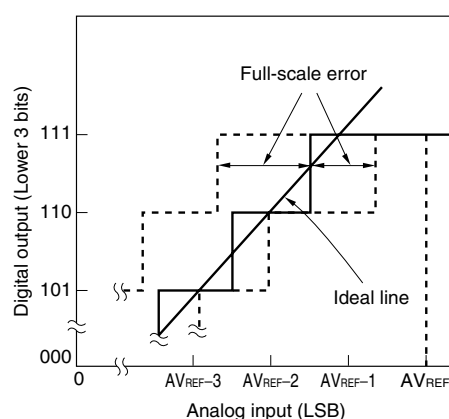
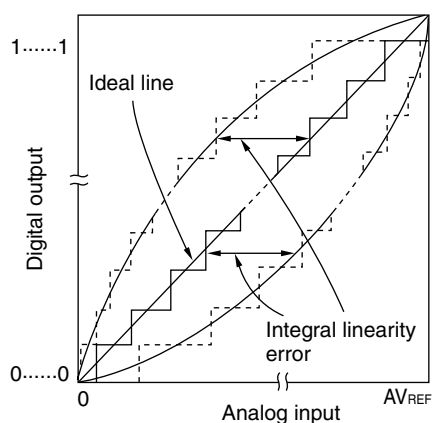
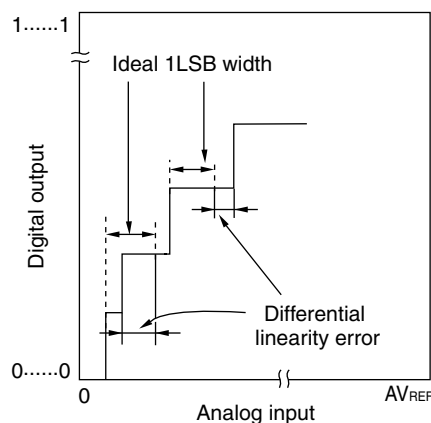
This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale – 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

(7) Differential linearity error

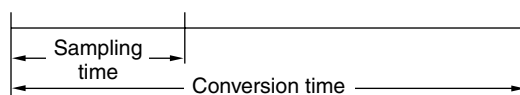
While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

Figure 11-42. Zero-Scale Error**Figure 11-43. Full-Scale Error****Figure 11-44. Integral Linearity Error****Figure 11-45. Differential Linearity Error****(8) Conversion time**

This expresses the time from the start of sampling to when the digital output is obtained. The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.



11.10 Cautions for A/D Converter

(1) Operating current in STOP mode

Shift to STOP mode after stopping the A/D converter (by setting bit 7 (ADCS) of A/D converter mode register 0 (ADM0) to 0). The operating current can be reduced by setting bit 0 (ADCE) of the ADM0 register to 0 at the same time.

To restart from the standby status, clear bit 0 (ADIF) of interrupt request flag register 1H (IF1H) to 0 and start operation.

(2) Input range of ANI0 to ANI12 and ANI16 to ANI30 pins

Observe the rated range of the ANI0 to ANI12 and ANI16 to ANI30 pins input voltage. If a voltage of AV_{DD} , and AV_{REFP} or higher and AV_{SS} , and AV_{REFM} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When internal reference voltage (1.45 V) is selected reference voltage source for the + side of the A/D converter, do not input internal reference voltage or higher voltage to a pin selected by the ADS register. However, it is no problem that a pin not selected by the ADS register is input voltage greater than the internal reference voltage.

<R> **Caution** Internal reference voltage (1.45 V) can be used only in HS (high-speed main) mode. For detail, refer to Figure 24-3. Format of User Option Byte (000C2H/010C2H).

(3) Conflicting operations

<1> Conflict between the A/D conversion result register (ADCR, ADCRH) write and the ADCR or ADCRH register read by instruction upon the end of conversion

The ADCR or ADCRH register read has priority. After the read operation, the new conversion result is written to the ADCR or ADCRH registers.

<2> Conflict between the ADCR or ADCRH register write and the A/D converter mode register 0 (ADM0) write, the analog input channel specification register (ADS), or A/D port configuration register (ADPC) write upon the end of conversion

The ADM0, ADS, or ADPC registers write has priority. The ADCR or ADCRH register write is not performed, nor is the conversion end interrupt signal (INTAD) generated.

(4) Noise countermeasures

To maintain the 12-bit resolution, attention must be paid to noise input to the AV_{REFP} , AV_{DD} , ANI0 to ANI12, and ANI16 to ANI30 pins.

<1> Be sure to separate AV_{DD} and AV_{SS} from other power supplies and connect a capacitor with low equivalent resistance and good frequency response characteristics (a capacitance of about $0.01\ \mu\text{F}$ is recommended) between AV_{DD} and AV_{SS} .

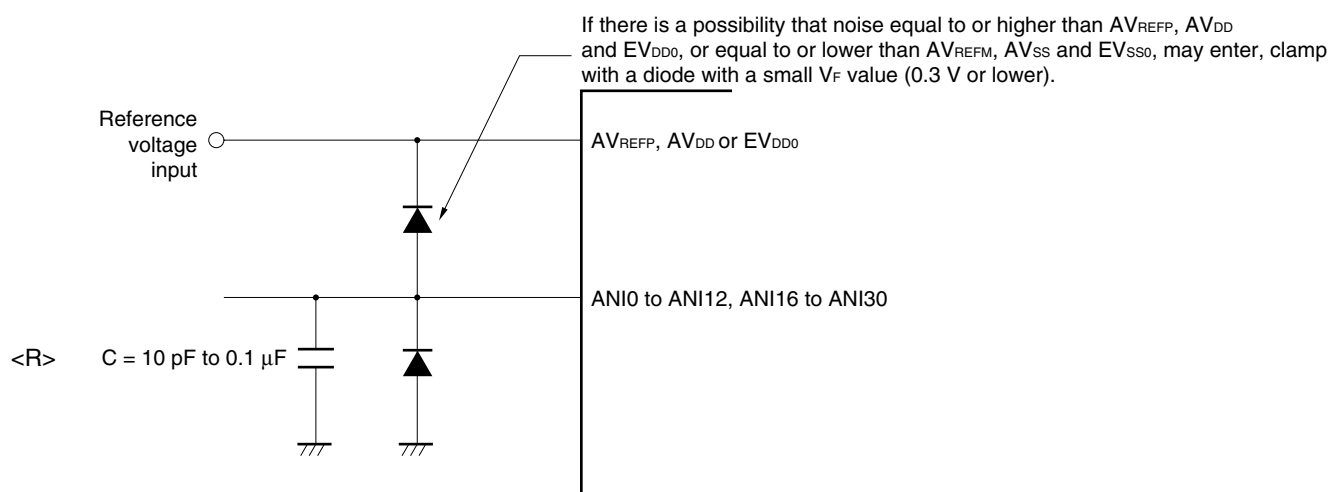
<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external C as shown in Figure 11-46 is recommended.

<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

<5> Separate digital and analog signals so that they do not cross or approach each other.

Figure 11-46. Analog Input Pin Connection



(5) Analog input (ANIn) pins

- <R> <1> ANI0 to ANI12 pins (high-accuracy channel) are also used as P20 to P27, and P150 to P154 pins. When A/D conversion is performed with any of the high-accuracy channel (ANI0 to ANI12) pins selected, do not change the output value P20 to P27, and P150 to P154 while conversion is in progress; otherwise the conversion accuracy may be degraded.
- <R> <2> If a pin adjacent to the pin whose value is being A/D converted is used as a digital I/O port pin, the A/D conversion value might differ from the expected value due to coupling noise. To prevent coupling noise, make sure that pulses whose voltage suddenly change, such as digital pulses, are not input or output to a pin adjacent to the pin whose value is being A/D converted.

(6) Input impedance of analog input (ANIn) pins

This A/D converter charges a sampling capacitor for sampling during sampling time.

Therefore, only a leakage current flows when sampling is not in progress, and a current that charges the capacitor flows during sampling. Consequently, the input impedance fluctuates depending on whether sampling is in progress, and on the other states.

- <R> However, in order to perform sampling accurately, the output impedance of the analog input source should be 1 k Ω or lower. If it is not possible to keep the output impedance below this level, it is recommended to either extend the sampling time or connect a capacitor of about 0.1 μ F to the ANI0 to ANI12 and ANI16 to ANI30 pins. (See **Figure 11-46** for details.)

Also, if the ADCS bit is set to 0 or a reconversion is started during A/D conversion, the sampling capacitor will be insufficiently charged. This means that charging will start with an undefined conversion voltage from the next conversion in the case of setting the ADCS bit to 0, or from the current conversion in the case of starting a reconversion.

To ensure that the capacitor is fully charged, therefore, either reduce the output impedance of the analog input source or specify a sufficiently long sampling time, irrespective of the analog signal voltage variation.

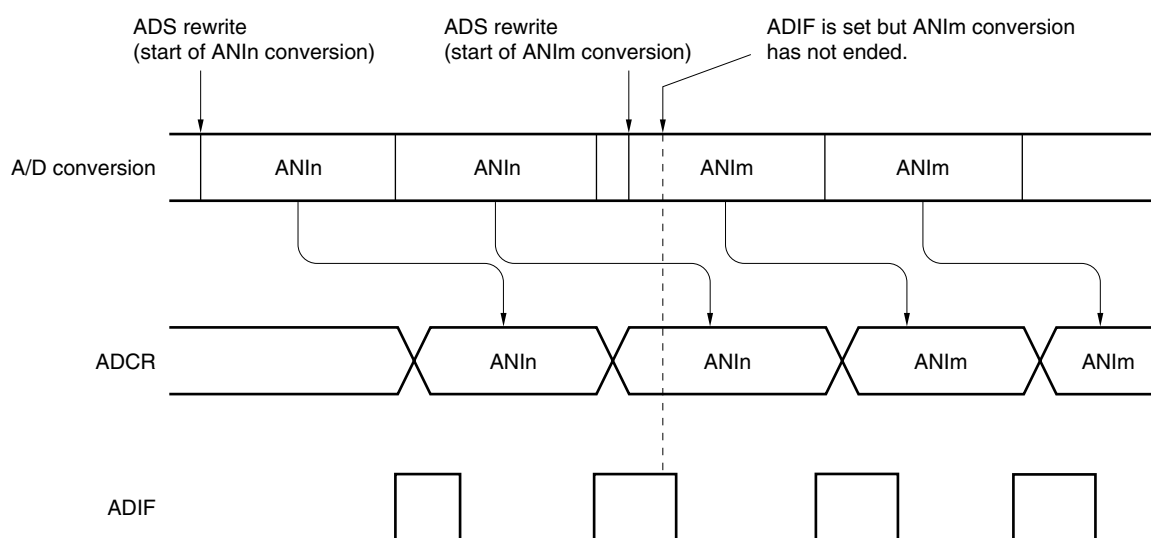
(7) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.

Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF flag for the pre-change analog input may be set just before the ADS register rewrite. Caution is therefore required since, at this time, when ADIF flag is read immediately after the ADS register rewrite, ADIF flag is set despite the fact A/D conversion for the post-change analog input has not ended.

When A/D conversion is stopped and then resumed, clear ADIF flag before the A/D conversion operation is resumed.

Figure 11-47. Timing of A/D Conversion End Interrupt Request Generation

**(8) Conversion results just after A/D conversion start**

While in the software trigger mode or hardware trigger no-wait mode, the first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μ s after the ADCE bit was set to 1. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.

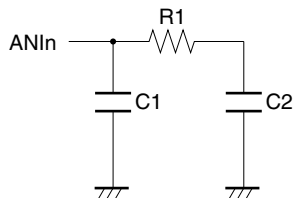
(9) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to A/D converter mode register 0 (ADM0), analog input channel specification register (ADS), A/D port configuration register (ADPC), and port mode control register (PMC), the contents of the ADCR and ADCRH registers may become undefined. Read the conversion result following conversion completion before writing to the ADM0, ADS, ADPC, or PMC register. Using a timing other than the above may cause an incorrect conversion result to be read.

(10) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 11-48. Internal Equivalent Circuit of ANIn Pin



<R>

Table 11-6. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AV_{DD}	ANIn pin	$R1[k\Omega]$	$C1[pF]$	$C2[pF]$
$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	ANI0 to ANI12	7.4	8	6.3
	ANI16 to ANI30	12.3	8	7.4
$1.8\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	ANI0 to ANI12	11	8	6.3
	ANI16 to ANI30	41	8	7.4
$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	ANI0 to ANI12	510	8	6.3
	ANI16 to ANI30	650	8	7.4

Remark The resistance and capacitance values shown in Table 11-6 are not guaranteed values.

(11) Starting the A/D converter

Start the A/D converter after the AV_{REFP} and AV_{DD} voltages stabilize.

CHAPTER 12 SERIAL ARRAY UNIT

Serial array unit 0 has four serial channels, and serial array unit 1 has two. Each channel can achieve 3-wire serial (CSI), UART, and simplified I²C communication.

Function assignment of each channel supported by the RL78/G1A is as shown below.

- 25-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	–		–
	2	–	UART1	–
	3	CSI11		IIC11

- 32-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	–		–
	2	–	UART1	–
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	–		–

- 48-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	CSI01		IIC01
	2	–	UART1	–
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	CSI21		IIC21

- 64-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	CSI01		IIC01
	2	CSI10	UART1	IIC10
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	CSI21		IIC21

When “UART0” is used for channels 0 and 1 of the unit 0, CSI00 and CSI01 cannot be used, but CSI10, UART1, or IIC10 can be used.

Caution Most of the following descriptions in this chapter use the units and channels of the 64-pin products as an example.

12.1 Functions of Serial Array Unit

Each serial interface supported by the RL78/G1A has the following features.

12.1.1 3-wire serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21)

Data is transmitted or received in synchronization with the serial clock ($\overline{\text{SCK}}$) output from the master channel.

3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock ($\overline{\text{SCK}}$), one for transmitting serial data (SO), one for receiving serial data (SI).

For details about the settings, see **12.5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) Communication.**

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

During master communication (CSI00): Max. $f_{\text{CLK}}/2$ ^{Notes 1, 2}

During master communication (other than CSI00): Max. $f_{\text{CLK}}/4$ ^{Note 2}

During slave communication: Max. $f_{\text{MCK}}/6$ ^{Note 2}

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

In addition, CSI00 of following channels supports the SNOOZE mode. When $\overline{\text{SCK}}$ input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only CSI00 can be specified for asynchronous reception.

<R> **Notes 1.** In master communication (CSI00), maximum transfer rate become $f_{\text{CLK}}/2$ when the following conditions.

- $2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq V_{\text{DD}} \leq 3.6\text{ V}$
- $f_{\text{MCK}} \leq 24\text{ MHz}$

Other cases, maximum transfer rate become $f_{\text{CLK}}/4$.

2. Use the clocks within a range satisfying the $\overline{\text{SCK}}$ cycle time (t_{KCY}) characteristics (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS ($T_{\text{A}} = -40$ to $+85^{\circ}\text{C}$) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_{\text{A}} = -40$ to $+105^{\circ}\text{C}$) (TARGET)**).

12.1.2 UART (UART0 to UART2)

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using timer array unit with an external interrupt (INTP0).

For details about the settings, see **12.6 Operation of UART (UART0 to UART2) Communication**.

[Data transmission/reception]

- Data length of 7, 8, or 9 bits^{Note}
- Select the MSB/LSB first
- Level setting of transmit/receive data and select of reverse
- Parity bit appending and parity check functions
- Stop bit appending

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

In addition, UARTs of following channels supports the SNOOZE mode. When RxD input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only UART0 can be specified for asynchronous reception.

The LIN-bus is accepted in UART2 (0 and 1 channels of unit 1) (32, 48, and 64-pin products only).

[LIN-bus functions]

- Wakeup signal detection
- Break field (BF) detection
- Sync field measurement, baud rate calculation

} Using the external interrupt (INTP0) and timer array unit

<R> **Note** Only UART0 can be specified for the 9-bit data length.

12.1.3 Simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21)

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I²C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master.

Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

For details about the settings, see **12.8 Operation of Simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21)**

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function^{Note} and ACK detection function
- Data length of 8 bits (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- ACK error, or overrun error

* [Functions not supported by simplified I²C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

Note When receiving the last data, ACK will not be output if 0 is written to the SOEmn bit (serial output enable register m (SOEm)) and serial communication data output is stopped. See the processing flow in **12.8.3 (2)** for details.

Remarks 1. To use an I²C bus of full function, see **CHAPTER 13 SERIAL INTERFACE IICA**.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

12.2 Configuration of Serial Array Unit

The serial array unit includes the following hardware.

Table 12-1. Configuration of Serial Array Unit

Item	Configuration
Shift register	8 bits or 9 bits ^{Note 1}
Buffer register	Lower 8 bits or 9 bits of serial data register mn (SDRmn) ^{Notes 1, 2}
Serial clock I/O	$\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK10}}$, $\overline{\text{SCK11}}$, $\overline{\text{SCK20}}$, $\overline{\text{SCK21}}$ pins (for 3-wire serial I/O), SCL00, SCL01, SCL10, SCL11, SCL20, SCL21 pins (for simplified I ² C)
Serial data input	SI00, SI01, SI10, SI11, SI20, SI21 pins (for 3-wire serial I/O), RxD0, RxD1 pins (for UART), RxD2 pin (for UART supporting LIN-bus)
Serial data output	SO00, SO01, SO10, SO11, SO20, SO21 pins (for 3-wire serial I/O), TxD0, TxD1 pins (for UART), TxD2 pin (for UART supporting LIN-bus), output controller
Serial data I/O	SDA00, SDA01, SDA10, SDA11, SDA20, SDA21 pins (for simplified I ² C)
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Serial clock select register m (SPSm) • Serial channel enable status register m (SEm) • Serial channel start register m (SSm) • Serial channel stop register m (STm) • Serial output enable register m (SOEm) • Serial output register m (SOM) • Serial output level register m (SOLm) • Serial standby control register m (SSCm) • Input switch control register (ISC) • Noise filter enable register 0 (NFEN0) <Registers of each channel> • Serial data register mn (SDRmn) • Serial mode register mn (SMRmn) • Serial communication operation setting register mn (SCRmn) • Serial status register mn (SSRmn) • Serial flag clear trigger register mn (SIRmn) • Port input mode registers 0, 1 (PIM0, PIM1) • Port output mode registers 0, 1, 5, 7 (POM0, POM1, POM5, POM7) • Port mode control registers 0, 1, 3, 5, 7 (PMC0, PMC1, PMC3, PMC5, PMC7) • Port mode registers 0, 1, 3, 5, 7 (PM0, PM1, PM3, PM5, PM7) • Port registers 0, 1, 3, 5, 7 (P0, P1, P3, P5, P7)

Notes 1. The number of bits used as the shift register and buffer register differs depending on the unit and channel.

- mn = 00, 01: lower 9 bits
- Other than above: lower 8 bits

2. The lower 8 bits of serial data register mn (SDRmn) can be read or written as the following SFR, depending on the communication mode.

- CSIp communication ... SIOp (CSIp data register)
- UARTq reception ... RXDq (UARTq receive data register)
- UARTq transmission ... TXDq (UARTq transmit data register)
- IICr communication ... SIOr (IICr data register)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), q: UART number (q = 0 to 2), r: IIC number (r = 00, 01, 10, 11, 20, 21)

Figure 12-1 shows the block diagram of the serial array unit 0.

Figure 12-1. Block Diagram of Serial Array Unit 0

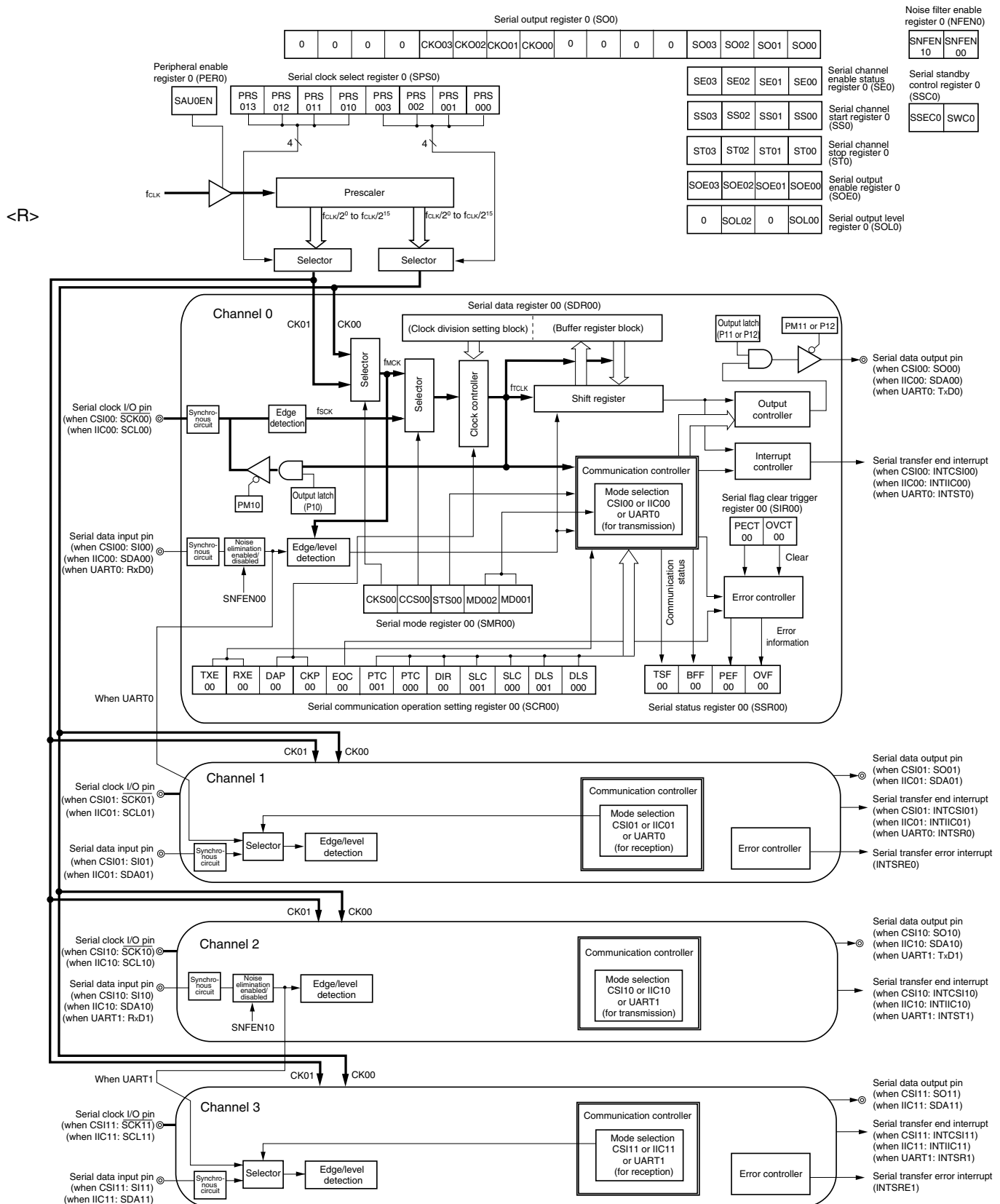
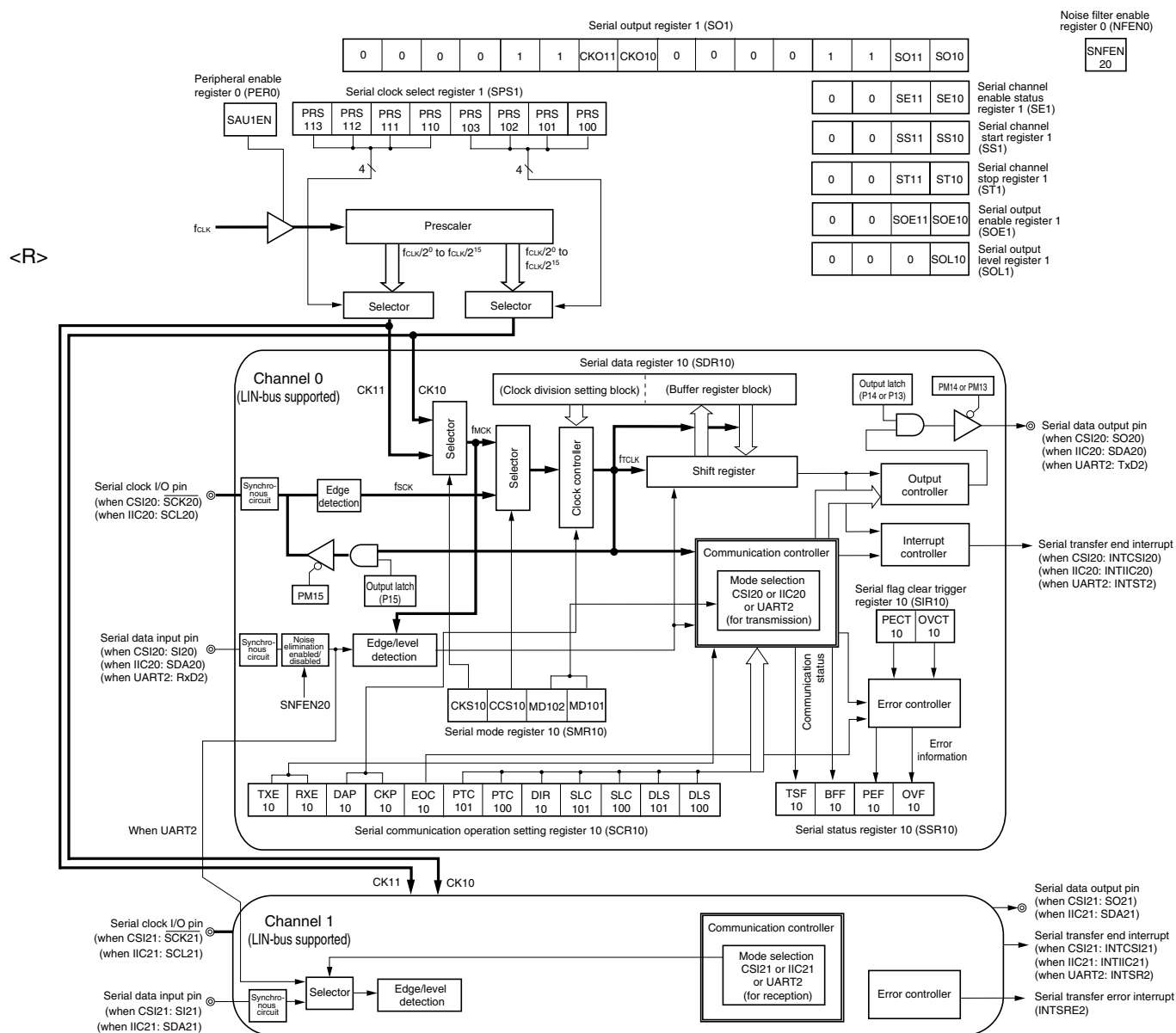


Figure 12-2 shows the block diagram of the serial array unit 1.

Figure 12-2. Block Diagram of Serial Array Unit 1



12.2.1 Shift register

This is a 9-bit register that converts parallel data into serial data or vice versa.

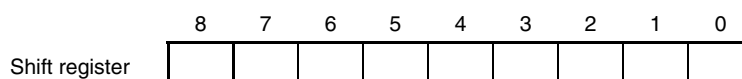
In case of the UART communication of nine bits of data, nine bits (bits 0 to 8) are used ^{Note 1}.

During reception, it converts data input to the serial pin into parallel data.

When data is transmitted, the value set to this register is output as serial data from the serial output pin.

The shift register cannot be directly manipulated by program.

To read or write the shift register, use the lower 8/9 bits of serial data register mn (SDRmn).



12.2.2 Lower 8/9 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 (lower 9 bits) ^{Note 1} or bits 7 to 0 (lower 8 bits) function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock (f_{MCK}).

When data is received, parallel data converted by the shift register is stored in the lower 8/9 bits. When data is to be transmitted, set transmit to be transferred to the shift register to the lower 8/9 bits.

The data stored in the lower 8/9 bits of this register is as follows, depending on the setting of bits 0 and 1 (DLSmn0, DLSmn1) of serial communication operation setting register mn (SCRmn), regardless of the output sequence of the data.

- 7-bit data length (stored in bits 0 to 6 of SDRmn register)
- 8-bit data length (stored in bits 0 to 7 of SDRmn register)
- 9-bit data length (stored in bits 0 to 8 of SDRmn register) ^{Note 1}

The SDRmn register can be read or written in 16-bit units.

The lower 8/9 bits of the SDRmn register can be read or written ^{Note 2} as the following SFR, depending on the communication mode.

- CSIp communication ... SIOP (CSIp data register)
- UARTq reception ... RXDq (UARTq receive data register)
- UARTq transmission ... TXDq (UARTq transmit data register)
- IICr communication ... SIOr (IICr data register)

Reset signal generation clears the SDRmn register to 0000H.

Notes 1. Only following UART0 can be specified for the 9-bit data length.

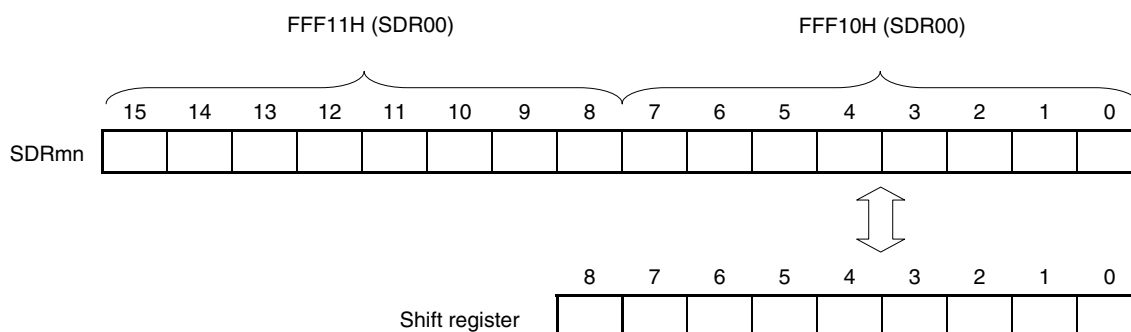
2. Writing in 8-bit units is prohibited when the operation is stopped ($SEmn = 0$).

Remarks 1. After data is received, "0" is stored in bits 0 to 8 in bit portions that exceed the data length.

2. m: Unit number ($m = 0, 1$), n: Channel number ($n = 0$ to 3), p: CSI number ($p = 00, 01, 10, 11, 20, 21$),
q: UART number ($q = 0$ to 2), r: IIC number ($r = 00, 01, 10, 11, 20, 21$)

Figure 12-3. Format of Serial Data Register mn (SDRmn) (mn = 00, 01, 10, 11)

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01) After reset: 0000H R/W
 FFF48H, FFF49H (SDR10) ^{Note}, FFF4AH, FFF4BH (SDR11) ^{Note}

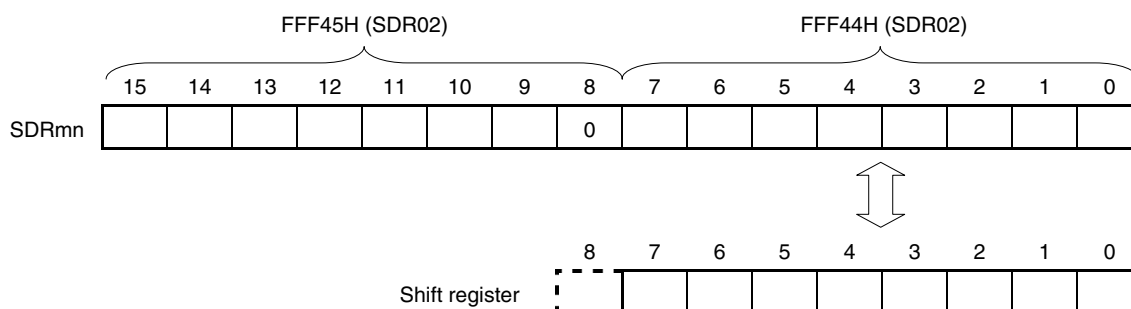


Note 32, 48, 64-pin products only

Remark For the function of the higher 7 bits of the SDRmn register, see **12.3 Registers Controlling Serial Array Unit**.

Figure 12-4. Format of Serial Data Register mn (SDRmn) (mn = 02, 03, 10, 11, 12, 13)

Address: FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03), After reset: 0000H R/W
 FFF48H, FFF49H (SDR10) ^{Note}, FFF4AH, FFF4BH (SDR11) ^{Note}



Note 32, 48, 64-pin products only

Caution Be sure to clear bit 8 to “0”.

Remark For the function of the higher 7 bits of the SDRmn register, see **12.3 Registers Controlling Serial Array Unit**.

12.3 Registers Controlling Serial Array Unit

Serial array unit is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Serial clock select register m (SPSm)
- Serial mode register mn (SMRmn)
- Serial communication operation setting register mn (SCRmn)
- Serial data register mn (SDRmn)
- Serial flag clear trigger register mn (SIRmn)
- Serial status register mn (SSRmn)
- Serial channel start register m (SSm)
- Serial channel stop register m (STm)
- Serial channel enable status register m (SEm)
- Serial output enable register m (SOEm)
- Serial output level register m (SOLm)
- Serial output register m (SOM)
- Serial standby control register 0 (SSC0)
- Input switch control register (ISC)
- Noise filter enable register 0 (NFEN0)
- Port input mode registers 0, 1 (PIM0, PIM1)
- Port output mode registers 0, 1, 5, 7 (POM0, POM1, POM5, POM7)
- Port mode control registers 0, 1, 3, 5, 7 (PMC0, PMC1, PMC3, PMC5, PMC7)
- Port mode registers 0, 1, 3, 5, 7 (PM0, PM1, PM3, PM5, PM7)
- Port registers 0, 1, 3, 5, 7 (P0, P1, P3, P5, P7)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

12.3.1 Peripheral enable register 0 (PER0)

PER0 is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When serial array unit 0 is used, be sure to set bit 2 (SAU0EN) of this register to 1.

When serial array unit 1 is used, be sure to set bit 3 (SAU1EN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the PER0 register to 00H.

Figure 12-5. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN	0	ADCEN	IICA0EN	SAU1EN ^{Note}	SAU0EN	0	TAU0EN

SAUmEN	Control of serial array unit m input clock supply
0	Stops supply of input clock. - SFR used by serial array unit m cannot be written. - Serial array unit m is in the reset status.
1	Enables input clock supply. SFR used by serial array unit m can be read/written.

Note 32, 48, and 64-pin products only.

Cautions 1. When setting serial array unit m, be sure to set the SAUmEN bit to 1 first. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read (except for the input switch control register (ISC), noise filter enable register 0 (NFEN0), port input mode registers 0, 1 (PIM0, PIM1), port output mode registers 0, 1, 5, 7 (POM0, POM1, POM5, POM7), Port mode control registers 0, 1, 3, 5, 7 (PMC0, PMC1, PMC3, PMC5, PMC7), port mode registers 0, 1, 3, 5, 7 (PM0, PM1, PM3, PM5, PM7), and port registers 0, 1, 3, 5, 7 (P0, P1, P3, P5, P7)).

2. Be sure to clear the following bits to 0.

25-pin products: bits 1, 3, 6

32, 48, 64-pin products: bits 1, 6

12.3.2 Serial clock select register m (SPSm)

The SPSm register is a 16-bit register that is used to select two types of operation clocks (CKm0, CKm1) that are commonly supplied to each channel. CKm1 is selected by bits 7 to 4 of the SPSm register, and CKm0 is selected by bits 3 to 0.

Rewriting the SPSm register is prohibited when the register is in operation (when SEMn = 1).

The SPSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SPSm register can be set with an 8-bit memory manipulation instruction with SPSmL.

Reset signal generation clears the SPSm register to 0000H.

Figure 12-6. Format of Serial Clock Select Register m (SPSm)

Address: F0126H, F0127H (SPS0), F0166H, F0167H (SPS1) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPSm	0	0	0	0	0	0	0	0	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00

PRS mk3	PRS mk2	PRS mk1	PRS mk0		Section of operation clock (CKmk) ^{Note 1}				
					f _{CLK} = 2 MHz	f _{CLK} = 5 MHz	f _{CLK} = 10 MHz	f _{CLK} = 20 MHz	f _{CLK} = 32 MHz
0	0	0	0	f _{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	32 MHz
0	0	0	1	f _{CLK} /2	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	f _{CLK} /2 ²	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	f _{CLK} /2 ³	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	f _{CLK} /2 ⁴	125 kHz	313 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	f _{CLK} /2 ⁵	62.5 kHz	156 kHz	313 kHz	625 kHz	1 MHz
0	1	1	0	f _{CLK} /2 ⁶	31.3 kHz	78.1 kHz	156 kHz	313 kHz	500 kHz
0	1	1	1	f _{CLK} /2 ⁷	15.6 kHz	39.1 kHz	78.1 kHz	156 kHz	250 kHz
1	0	0	0	f _{CLK} /2 ⁸	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	f _{CLK} /2 ⁹	3.91 kHz	9.77 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	f _{CLK} /2 ¹⁰	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	31.3 kHz
1	0	1	1	f _{CLK} /2 ¹¹	977 Hz	2.44 kHz	4.88 kHz	9.77 kHz	15.6 kHz
1	1	0	0	f _{CLK} /2 ¹²	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	f _{CLK} /2 ¹³	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	f _{CLK} /2 ¹⁴	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	f _{CLK} /2 ¹⁵	61 Hz	153 kHz	305 Hz	610 Hz	977 Hz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

Caution Be sure to clear bits 15 to 8 to “0”.

- Remarks**
1. f_{CLK}: CPU/peripheral hardware clock frequency
 2. m: Unit number (m = 0, 1)
 3. k = 0, 1

12.3.3 Serial mode register mn (SMRmn)

The SMRmn register is a register that sets an operation mode of channel n. It is also used to select an operation clock (f_{MCK}), specify whether the serial clock (f_{SCK}) may be input or not, set a start trigger, an operation mode (CSI, UART, or simplified I²C), and an interrupt source. This register is also used to invert the level of the receive data only in the UART mode.

Rewriting the SMRmn register is prohibited when the register is in operation (when $SE_{mn} = 1$). However, the MDmn0 bit can be rewritten during operation.

The SMRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets the SMRmn register to 0020H.

Figure 12-7. Format of Serial Mode Register mn (SMRmn) (1/2)

Address: F0110H, F0111H (SMR00) to F0116H, F0117H (SMR03), After reset: 0020H R/W
F0150H, F0151H (SMR10), F0152H, F0153H (SMR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKS mn	CCS mn	0	0	0	0	0	STS mn ^{Note}	0	SIS mn0 ^{Note}	1	0	0	MD mn2	MD mn1	MD mn0

CKS mn	Selection of operation clock (f_{MCK}) of channel n
0	Operation clock CKm0 set by the SPSm register
1	Operation clock CKm1 set by the SPSm register
Operation clock (f_{MCK}) is used by the edge detector. In addition, depending on the setting of the CCSmn bit and the higher 7 bits of the SDRmn register, a transfer clock (f_{TCLK}) is generated.	

CCS mn	Selection of transfer clock (f_{TCLK}) of channel n
0	Divided operation clock f_{MCK} specified by the CKSmn bit
1	Clock input f_{SCK} from the $\overline{SCKp}$ pin (slave transfer in CSI mode)
Transfer clock f_{TCLK} is used for the shift register, communication controller, output controller, interrupt controller, and error controller. When CCSmn = 0, the division ratio of operation clock (f_{MCK}) is set by the higher 7 bits of the SDRmn register.	

STS mn	Selection of start trigger source
0	Only software trigger is valid (selected for CSI, UART transmission, and simplified I ² C).
1	Valid edge of the RxDq pin (selected for UART reception)
Transfer is started when the above source is satisfied after 1 is set to the SSm register.	

Note The SMR01, SMR03, and SMR11 registers only.

Caution Be sure to clear bits 13 to 9, 7, 4, and 3 (or bits 13 to 6, 4, and 3 for the SMR00, SMR02, or SMR10 register) to “0”. Be sure to set bit 5 to “1”.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21),
q: UART number (q = 0 to 2), r: IIC number (r = 00, 01, 10, 11, 20, 21)

Figure 12-7. Format of Serial Mode Register mn (SMRmn) (2/2)

Address: F0110H, F0111H (SMR00) to F0116H, F0117H (SMR03), After reset: 0020H R/W
 F0150H, F0151H (SMR10), F0152H, F0153H (SMR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKS mn	CCS mn	0	0	0	0	0	STS mn ^{Note}	0	SIS mn0 ^{Note}	1	0	0	MD mn2	MD mn1	MD mn0

SIS mn0	Controls inversion of level of receive data of channel n in UART mode
0	Falling edge is detected as the start bit. The input communication data is captured as is.
1	Rising edge is detected as the start bit. The input communication data is inverted and captured.

MD mn2	MD mn1	Setting of operation mode of channel n
0	0	CSI mode
0	1	UART mode
1	0	Simplified I ² C mode
1	1	Setting prohibited

MD mn0	Selection of interrupt source of channel n
0	Transfer end interrupt
1	Buffer empty interrupt (Occurs when data is transferred from the SDRmn register to the shift register.)
For successive transmission, the next transmit data is written by setting the MDmn0 bit to 1 when SDRmn data has run out.	

Note The SMR01, SMR03, and SMR11 registers only.

Caution Be sure to clear bits 13 to 9, 7, 4, and 3 (or bits 13 to 6, 4, and 3 for the SMR00, SMR02, or SMR10 register) to “0”. Be sure to set bit 5 to “1”.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21),
 q: UART number (q = 0 to 2), r: IIC number (r = 00, 01, 10, 11, 20, 21)

12.3.4 Serial communication operation setting register mn (SCRmn)

The SCRmn register is a communication operation setting register of channel n. It is used to set a data transmission/reception mode, phase of data and clock, whether an error signal is to be masked or not, parity bit, start bit, stop bit, and data length.

Rewriting the SCRmn register is prohibited when the register is in operation (when SEMn = 1).

The SCRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets the SCRmn register to 0087H.

Figure 12-8. Format of Serial Communication Operation Setting Register mn (SCRmn) (1/2)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), After reset: 0087H R/W
 F0158H, F0159H (SCR10), F015AH, F015BH (SCR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLCm n1 ^{Note 1}	SLC mn0	0	1	DLSm n1 ^{Note 2}	DLS mn0

TXE mn	RXE mn	Setting of operation mode of channel n
0	0	Disable communication.
0	1	Reception only
1	0	Transmission only
1	1	Transmission/reception

DAP mn	CKP mn	Selection of data and clock phase in CSI mode	Type
0	0		1
0	1		2
1	0		3
1	1		4
Be sure to set DAPmn, CKPmn = 0, 0 in the UART mode and simplified I ² C mode.			

EOC mn	Selection of masking of error interrupt signal (INTSREx (x = 0 to 2))
0	Masks error interrupt INTSREx (INTSRx is not masked).
1	Enables generation of error interrupt INTSREx (INTSRx is masked if an error occurs).
Set EOCmn = 0 in the CSI mode, simplified I ² C mode, and during UART transmission ^{Note 3} . Can select EOCmn = 1 during UART reception ^{Note 3} .	

<R>

- Notes**
1. The SCR00, SCR02, and SCR10 registers only.
 2. The SCR00 and SCR01 registers only. Others are fixed to 1.
 3. When using CSImn not with EOCmn = 0, error interrupt INTSREn may be generated.

Caution Be sure to clear bits 3, 6, and 11 to “0” (Also clear bit 5 of the SCR01, SCR03, or SCR11 register to 0). Be sure to set bit 2 to “1”.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21)

Figure 12-8. Format of Serial Communication Operation Setting Register mn (SCRmn) (2/2)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), After reset: 0087H R/W
 F0158H, F0159H (SCR10), F015AH, F015BH (SCR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLCm n1 ^{Note 1}	SLC mn0	0	1	DLSm n1 ^{Note 2}	DLS mn0

PTC mn1	PTC mn0	Setting of parity bit in UART mode	
		Transmission	Reception
0	0	Does not output the parity bit.	Receives without parity
0	1	Outputs 0 parity ^{Note 3} .	No parity judgment
1	0	Outputs even parity.	Judged as even parity.
1	1	Outputs odd parity.	Judges as odd parity.
Be sure to set PTCmn1, PTCmn0 = 0, 0 in the CSI mode and simplified I ² C mode.			

DIRmn	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	Inputs/outputs data with LSB first.
Be sure to clear DIRmn = 0 in the simplified I ² C mode.	

SLCmn1 ^{Note 1}	SLCmn0	Setting of stop bit in UART mode
0	0	No stop bit
0	1	Stop bit length = 1 bit
1	0	Stop bit length = 2 bits (mn = 00, 02, 10 only)
1	1	Setting prohibited

When the transfer end interrupt is selected, the interrupt is generated when all stop bits have been completely transferred.

Set 1 bit (SLCmn1, SLCmn0 = 0, 1) during UART reception and in the simplified I²C mode.

Set no stop bit (SLCmn1, SLCmn0 = 0, 0) in the CSI mode.

DLSm n1 ^{Note 2}	DLS mn0	Setting of data length in CSI and UART modes
0	1	9-bit data length (stored in bits 0 to 8 of the SDRmn register) (settable in UART mode only)
1	0	7-bit data length (stored in bits 0 to 6 of the SDRmn register)
1	1	8-bit data length (stored in bits 0 to 7 of the SDRmn register)
Other than above		Setting prohibited
Be sure to set DLSmn1, DLSmn0 = 1, 1 in the simplified I ² C mode.		

- Notes**
1. The SCR00, SCR02, and SCR10 registers only.
 2. The SCR00 and SCR01 registers only. Others are fixed to 1.
 3. 0 is always added regardless of the data contents.

Caution Be sure to clear bits 3, 6, and 11 to “0”. (Also clear bit 5 of the SCR01, SCR03, or SCR11 register to 0). Be sure to set bit 2 to “1”.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21)

12.3.5 Higher 7 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 (lower 9 bits) of SDR00, SDR01, SDR10, SDR11 or bits 7 to 0 (lower 8 bits) of SDR02, SDR03, SDR10, and SDR11 function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock (f_{MCK}).

<R> If the CCSmn bit of serial mode register mn (SMRmn) is cleared to 0, the clock set by dividing the operating clock by the higher 7 bits of the SDRmn register is used as the transfer clock. If the CCSmn bit of serial mode register mn (SMRmn) is cleared to 1, bits 15 to 9 of SDR01, SDR00 (higher 7 bits) are set to "0000000B". f_{SCK} of input clock from the SCKp pin (slave transfer of CSI mode) is the transfer clock.

The lower 8/9 bits of the SDRmn register function as a transmit/receive buffer register. During reception, the parallel data converted by the shift register is stored in the lower 8/9 bits, and during transmission, the data to be transmitted to the shift register is set to the lower 8/9 bits.

The SDRmn register can be read or written in 16-bit units.

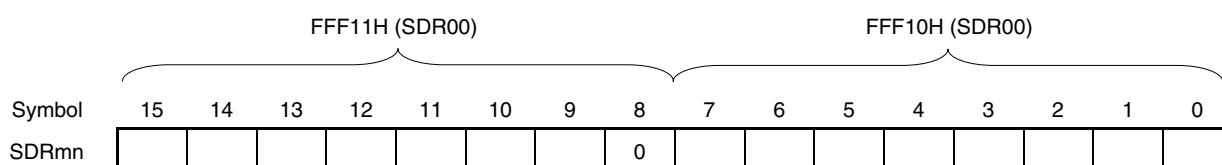
However, the higher 7 bits can be written or read only when the operation is stopped ($SEmn = 0$). During operation ($SEmn = 1$), a value is written only to the lower 8/9 bits of the SDRmn register. When the SDRmn register is read during operation, 0 is always read.

Reset signal generation clears the SDRmn register to 0000H.

Figure 12-9. Format of Serial Data Register mn (SDRmn)

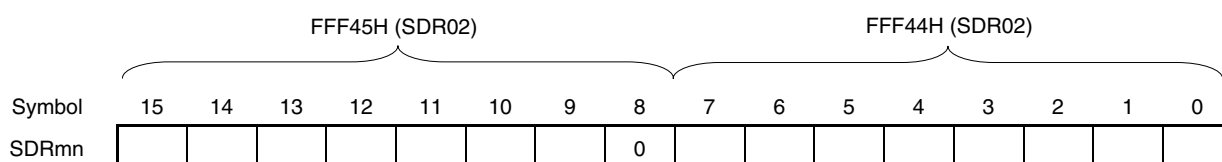
Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01)

After reset: 0000H R/W



Address: FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03),
FFF48H, FFF49H (SDR10), FFF4AH, FFF4BH (SDR11)

After reset: 0000H R/W



SDRmn[15:9]							Transfer clock setting by dividing the operating clock (f_{MCK})
0	0	0	0	0	0	0	$f_{MCK}/2$
0	0	0	0	0	0	1	$f_{MCK}/4$
0	0	0	0	0	1	0	$f_{MCK}/6$
0	0	0	0	0	1	1	$f_{MCK}/8$
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	$f_{MCK}/254$
1	1	1	1	1	1	1	$f_{MCK}/256$

(Cautions and remarks are listed on the next page.)

- Cautions**
1. Be sure to clear bit 8 of the SDR02, SDR03, SDR10, and SDR11 to “0”.
 2. Setting SDRmn[15:9] = (0000000B, 0000001B) is prohibited when UART is used.
 3. Setting SDRmn[15:9] = 0000000B is prohibited when simplified I²C is used. Set SDRmn[15:9] to 0000001B or greater.
 4. Do not write eight bits to the lower eight bits if operation is stopped (SEmn = 0). (If these bits are written to, the higher seven bits are cleared to 0.)

- Remarks**
1. For the function of the lower 8/9 bits of the SDRmn register, see **12.2 Configuration of Serial Array Unit**.
 2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

12.3.6 Serial flag clear trigger register mn (SIRmn)

The SIRmn register is a trigger register that is used to clear each error flag of channel n.

When each bit (FECTmn, PECTmn, OVCTmn) of this register is set to 1, the corresponding bit (FEFmn, PEFmn, OVFMn) of serial status register mn (SSRmn) is cleared to 0. Because the SIRmn register is a trigger register, it is cleared immediately when the corresponding bit of the SSRmn register is cleared.

The SIRmn register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SIRmn register can be set with an 8-bit memory manipulation instruction with SIRmnL.

Reset signal generation clears the SIRmn register to 0000H.

Figure 12-10. Format of Serial Flag Clear Trigger Register mn (SIRmn)

Address: F0108H, F0109H (SIR00) to F010EH, F010FH (SIR03), After reset: 0000H R/W
F0148H, F0149H (SIR10), F014AH, F014BH (SIR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIRmn	0	0	0	0	0	0	0	0	0	0	0	0	0	FECT mn ^{Note}	PEC Tmn	OVC Tmn

FEC Tmn	Clear trigger of framing error of channel n														
0	Not cleared														
1	Clears the FEFmn bit of the SSRmn register to 0.														

PEC Tmn	Clear trigger of parity error flag of channel n														
0	Not cleared														
1	Clears the PEFmn bit of the SSRmn register to 0.														

OVC Tmn	Clear trigger of overrun error flag of channel n														
0	Not cleared														
1	Clears the OVFMn bit of the SSRmn register to 0.														

Note The SIR01, SIR03, and SIR11 registers only.

Caution Be sure to clear bits 15 to 3 (or bits 15 to 2 for the SIR00, SIR02, or SIR10 register) to “0”.

- Remarks**
1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)
 2. When the SIRmn register is read, 0000H is always read.

12.3.7 Serial status register mn (SSRmn)

The SSRmn register is a register that indicates the communication status and error occurrence status of channel n. The errors indicated by this register are a framing error, parity error, and overrun error.

The SSRmn register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSRmn register can be set with an 8-bit memory manipulation instruction with SSRmnL.

Reset signal generation clears the SSRmn register to 0000H.

Figure 12-11. Format of Serial Status Register mn (SSRmn) (1/2)

Address: F0100H, F0101H (SSR00) to F0106H, F0107H (SSR03), After reset: 0000H R
F0140H, F0141H (SSR10), F0142H, F0143H (SSR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSRmn	0	0	0	0	0	0	0	0	0	TSF mn	BFF mn	0	0	FEFm n ^{Note}	PEF mn	OVF mn

TSF mn	Communication status indication flag of channel n
0	Communication is stopped or suspended.
1	Communication is in progress.
<Clear conditions> • The STmn bit of the STm register is set to 1 (communication is stopped) or the SSmn bit of the SSm register is set to 1 (communication is suspended). • Communication ends. <Set condition> • Communication starts.	

BFF mn	Buffer register status indication flag of channel n
0	Valid data is not stored in the SDRmn register.
1	Valid data is stored in the SDRmn register.
<Clear conditions> • Transferring transmit data from the SDRmn register to the shift register ends during transmission. • Reading receive data from the SDRmn register ends during reception. • The STmn bit of the STm register is set to 1 (communication is stopped) or the SSmn bit of the SSm register is set to 1 (communication is enabled). <Set conditions> • Transmit data is written to the SDRmn register while the TXEmn bit of the SCRmn register is set to 1 (transmission or transmission and reception mode in each communication mode). • Receive data is stored in the SDRmn register while the RXEmn bit of the SCRmn register is set to 1 (reception or transmission and reception mode in each communication mode). • A reception error occurs.	

Note The SSR01, SSR03, and SSR11 registers only.

Caution If data is written to the SDRmn register when BFFmn = 1, the transmit/receive data stored in the register is discarded and an overrun error (OVEmn = 1) is detected.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Figure 12-11. Format of Serial Status Register mn (SSRmn) (2/2)

Address: F0100H, F0101H (SSR00) to F0106H, F0107H (SSR03), After reset: 0000H R
 F0140H, F0141H (SSR10), F0142H, F0143H (SSR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSRmn	0	0	0	0	0	0	0	0	0	TSF mn	BFF mn	0	0	FEF mn ^{Note}	PEF mn	OVF mn

FEF mn ^{Note}	Framing error detection flag of channel n
0	No error occurs.
1	An error occurs (during UART reception).
<Clear condition> 1 is written to the FECTmn bit of the SIRmn register. <Set condition> - A stop bit is not detected when UART reception ends.	

PEF mn	Parity/ACK error detection flag of channel n
0	No error occurs.
1	Parity error occurs (during UART reception) or ACK is not detected (during I ² C transmission).
<Clear condition> 1 is written to the PECTmn bit of the SIRmn register. <Set condition> - The parity of the transmit data and the parity bit do not match when UART reception ends (parity error). - No ACK signal is returned from the slave channel at the ACK reception timing during I²C transmission (ACK is not detected).	

OVF mn	Overflow error detection flag of channel n
0	No error occurs.
1	An error occurs
<Clear condition> 1 is written to the OVCTmn bit of the SIRmn register. <Set condition> - Even though receive data is stored in the SDRmn register, that data is not read and transmit data or the next receive data is written while the RXEmn bit of the SCRmn register is set to 1 (reception or transmission and reception mode in each communication mode). - Transmit data is not ready for slave transmission or transmission and reception in CSI mode.	

Note The SSR01, SSR03, and SSR11 registers only.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

12.3.8 Serial channel start register m (SSm)

The SSm register is a trigger register that is used to enable starting communication/count by each channel.

When 1 is written a bit of this register (SSmn), the corresponding bit (SEmn) of serial channel enable status register m (SEm) is set to 1 (Operation is enabled). Because the SSmn bit is a trigger bit, it is cleared immediately when SEMn = 1.

The SSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSm register can be set with an 1-bit or 8-bit memory manipulation instruction with SSmL.

Reset signal generation clears the SSm register to 0000H.

Figure 12-12. Format of Serial Channel Start Register m (SSm)

Address: F0122H, F0123H (SS0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS0	0	0	0	0	0	0	0	0	0	0	0	0	SS03	SS02	SS01	SS00

Address: F0162H, F0163H (SS1)^{Note 1} After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SS11	SS10

SSmn	Operation start trigger of channel n
0	No trigger operation
1	Sets the SEMn bit to 1 and enters the communication wait status ^{Note 2} .

Notes 1. 32, 48, 64-pin products only

<R> **2.** If set the SSmn = 1 to during a communication operation, will wait status to stop the communication. At this time, holding status value of control register and shift register, $\overline{\text{SCKmn}}$ and SOMn pins, and FEFmn, PEFmn, OVFmn flags.

Cautions 1. Be sure to clear bits 15 to 4 of the SS0 register and bits 15 to 2 of the SS1 register to "0".

<R> **2.** For the UART reception, set the RXEmn bit of SCRmn register to 1, and then be sure to set SSmn to 1 after 4 or more f_{MCK} clocks have elapsed.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

2. When the SSm register is read, 0000H is always read.

12.3.9 Serial channel stop register m (STm)

The STm register is a trigger register that is used to enable stopping communication/count by each channel.

When 1 is written a bit of this register (STmn), the corresponding bit (SEmn) of serial channel enable status register m (SEm) is cleared to 0 (operation is stopped). Because the STmn bit is a trigger bit, it is cleared immediately when SEmn = 0.

The STm register can set written by a 16-bit memory manipulation instruction.

The lower 8 bits of the STm register can be set with a 1-bit or 8-bit memory manipulation instruction with STmL.

Reset signal generation clears the STm register to 0000H.

Figure 12-13. Format of Serial Channel Stop Register m (STm)

Address: F0124H, F0125H (ST0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST0	0	0	0	0	0	0	0	0	0	0	0	0	ST03	ST02	ST01	ST00

Address: F0164H, F0165H (ST1) ^{Note 1} After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ST11	ST10

STm n	Operation stop trigger of channel n
0	No trigger operation
1	Clears the SEmn bit to 0 and stops the communication operation ^{Note 2} .

Notes 1. 32, 48, 64-pin products only

2. Holding status value of the control register and shift register, the $\overline{\text{SCKmn}}$ and SOMn pins, and FEFmn, PEFmn, OVFMn flags.

Caution Be sure to clear bits 15 to 4 of the ST0 register and bits 15 to 2 of the ST1 register to “0”.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

2. When the STm register is read, 0000H is always read.

12.3.10 Serial channel enable status register m (SEm)

The SEm register indicates whether data transmission/reception operation of each channel is enabled or stopped.

When 1 is written a bit of serial channel start register m (SSm), the corresponding bit of this register is set to 1. When 1 is written a bit of serial channel stop register m (STm), the corresponding bit is cleared to 0.

Channel n that is enabled to operate cannot rewrite by software the value of the CKOm_n bit (serial clock output of channel n) of serial output register m (SOM) to be described below, and a value reflected by a communication operation is output from the serial clock pin.

Channel n that stops operation can set the value of the CKOm_n bit of the SOM register by software and output its value from the serial clock pin. In this way, any waveform, such as that of a start condition/stop condition, can be created by software.

The SEm register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the SEm register can be set with a 1-bit or 8-bit memory manipulation instruction with SEmL.

Reset signal generation clears the SEm register to 0000H.

Figure 12-14. Format of Serial Channel Enable Status Register m (SEm)

Address: F0120H, F0121H (SE0) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SE0	0	0	0	0	0	0	0	0	0	0	0	0	SE03	SE02	SE01	SE00

Address: F0160H, F0161H (SE1)^{Note} After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SE1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SE11	SE10

SEm _n	Indication of operation enable/stop status of channel n
0	Operation stops
1	Operation is enabled.

Note 32, 48, 64-pin products only

Caution Be sure to clear bits 15 to 4 of the SE0 register and bits 15 to 2 of the SE1 register to “0”.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

12.3.11 Serial output enable register m (SOEm)

The SOEm register is a register that is used to enable or stop output of the serial communication operation of each channel.

Channel n that enables serial output cannot rewrite by software the value of the SOMn bit of serial output register m (SOM) to be described below, and a value reflected by a communication operation is output from the serial data output pin.

For channel n, whose serial output is stopped, the SOMn bit value of the SOM register can be set by software, and that value can be output from the serial data output pin. In this way, any waveform of the start condition and stop condition can be created by software.

The SOEm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SOEm register can be set with a 1-bit or 8-bit memory manipulation instruction with SOEmL.

Reset signal generation clears the SOEm register to 0000H.

Figure 12-15. Format of Serial Output Enable Register m (SOEm)

Address: F012AH, F012BH (SOE0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE0	0	0	0	0	0	0	0	0	0	0	0	0	SOE 03	SOE 02	SOE 01	SOE 00

Address: F016AH, F016BH^{Note} (SOE1) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE 11	SOE 10

SOE mn	Serial output enable/stop of channel n
0	Stops output by serial communication operation.
1	Enables output by serial communication operation.

Note 32, 48, 64-pin products only

Caution Be sure to clear bits 15 to 4 of the SOE0 register, and bits 15 to 2 of the SOE1 register to “0”.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

12.3.12 Serial output register m (SOM)

The SOM register is a buffer register for serial output of each channel.

The value of the SOMn bit of this register is output from the serial data output pin of channel n.

The value of the CKOm bit of this register is output from the serial clock output pin of channel n.

The SOMn bit of this register can be rewritten by software only when serial output is disabled (SOEmn = 0). When serial output is enabled (SOEmn = 1), rewriting by software is ignored, and the value of the register can be changed only by a serial communication operation.

The CKOm bit of this register can be rewritten by software only when the channel operation is stopped (SEmn = 0). While channel operation is enabled (SEmn = 1), rewriting by software is ignored, and the value of the CKOm bit can be changed only by a serial communication operation.

To use the pin for serial interface as a port function pin, set the corresponding CKOm and SOMn bits to "1".

The SOM register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears the SOM register to 0F0FH.

Figure 12-16. Format of Serial Output Register m (SOM)

Address: F0128H, F0129H (SO0) After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO 03	CKO 02	CKO 01	CKO 00	0	0	0	0	SO 03	SO 02	SO 01	SO 00

Address: F0168H, F0169H^{Note} (SO1) After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	0	0	CKO 11	CKO 10	0	0	0	0	0	0	SO 11	SO 10

CKO mn	Serial clock output of channel n
0	Serial clock output value is "0".
1	Serial clock output value is "1".

SO mn	Serial data output of channel n
0	Serial data output value is "0".
1	Serial data output value is "1".

Note 32, 48, 64-pin products only

Caution Be sure to clear bits 15 to 12, 7 to 4 of the SO0 register, and bits 15 to 10, 7 to 2 of the SO1 register to "0".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

12.3.13 Serial output level register m (SOLm)

The SOLm register is a register that is used to set inversion of the data output level of each channel.

This register can be set only in the UART mode. Be sure to set 0 for corresponding bit in the CSI mode and simplifies I²C mode.

Inverting channel n by using this register is reflected on pin output only when serial output is enabled (SOEmn = 1). When serial output is disabled (SOEmn = 0), the value of the SOMn bit is output as is.

Rewriting the SOLm register is prohibited when the register is in operation (when SEMn = 1).

The SOLm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SOLm register can be set with an 8-bit memory manipulation instruction with SOLmL.

Reset signal generation clears the SOLm register to 0000H.

Figure 12-17. Format of Serial Output Level Register m (SOLm)

Address: F0134H, F0135H (SOL0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOL0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOL02	0	SOL00

Address: F0174H, F0175H (SOL1)^{Note} After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOL1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOL10

SOLmn	Selects inversion of the level of the transmit data of channel n in UART mode
0	Communication data is output as is.
1	Communication data is inverted and output.

Note 32, 48, 64-pin products only

Caution Be sure to clear bits 15 to 3, and 1 of the SOL0 register and bits 15 to 1, and 1 of the SOL1 register to “0”.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

12.3.14 Serial standby control register m (SSCm)

The SSC0 register is used to control the startup of reception (the SNOOZE mode) while in the STOP mode when receiving CSI00 or UART0 serial data.

The SSC1^{Note} register is used to control the startup of reception (the SNOOZE mode) while in the STOP mode when receiving CSI20 or UART2 serial data.

The SSCm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSCm register can be set with an 8-bit memory manipulation instruction with SSCmL.

Reset signal generation clears the SSCm register to 0000H.

Note The SSC1 register is provided in the 32, 48, 64-pin products only.

Caution The maximum transfer rate in the SNOOZE mode is as follows.

- When using CSI00, CSI20 : 1 Mbps
- When using UART0, UART2 : 9600 bps

Figure 12-18. Format of Serial Standby Control Register m (SSCm)

Address: F0138H (SSC0), F0178H (SSC1) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSCm	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SSEC m	SWC m

SSEC m	Selection of whether to enable or stop the generation of transfer end interrupts
0	Enable the generation of error interrupts (INTSRE0/INTSRE2). In the following cases, the clock request signal (an internal signal) to the clock generator is also cleared: • When the SWC bit is cleared to 0 • When the UART reception start bit is mistakenly detected
1	Stop the generation of error interrupts (INTSRE0/INTSRE2). In the following cases, the clock request signal (an internal signal) to the clock generator is also cleared: • When the SWCm bit is cleared to 0 • When the UART reception start bit is mistakenly detected • When the transfer end interrupt generation timing is based on a parity error or framing error

SWC m	Setting of the SNOOZE mode
0	Do not use the SNOOZE mode function.
1	Use the SNOOZE mode function.
• When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode). • The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (f_{CLK}). If any other clock is selected, specifying this mode is prohibited. • Even when using SNOOZE mode, be sure to set the AWC bit to 0 in normal operation mode and change it to 1 just before shifting to STOP mode. Also, be sure to change the SWC bit to 0 after returning from STOP mode to normal operation mode.	

Caution Setting SSECm, SWCm = 1, 0 is prohibited.

12.3.15 Input switch control register (ISC)

The ISC1 and ISC0 bits of the ISC register are used to realize a LIN-bus communication operation by UART2 in coordination with an external interrupt and the timer array unit.

When bit 0 is set to 1, the input signal of the serial data input (RxD2) pin is selected as an external interrupt (INTP0) that can be used to detect a wakeup signal.

When bit 1 is set to 1, the input signal of the serial data input (RxD2) pin is selected as a timer input, so that wake up signal can be detected, the low width of the break field, and the pulse width of the sync field can be measured by the timer.

The ISC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the ISC register to 00H.

Figure 12-19. Format of Input Switch Control Register (ISC)

Address: F0073H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	0	0	0	0	0	0	ISC1	ISC0

ISC1	Switching channel 7 input of timer array unit
0	32, 48, and 64-pin products: Uses the input signal of the TI07 pin as a timer input (normal operation). 25-pin products: Do not use a timer input signal for channel 7.
1	Input signal of the RxD2 pin is used as timer input (detects the wakeup signal and measures the low width of the break field and the pulse width of the sync field). Setting is prohibited in the 25-pin products.

ISC0	Switching external interrupt (INTP0) input
0	Uses the input signal of the INTP0 pin as an external interrupt (normal operation).
1	Uses the input signal of the RxD2 pin as an external interrupt (wakeup signal detection).

Caution Be sure to clear bits 7 to 2 to “0”.

12.3.16 Noise filter enable register 0 (NFEN0)

The NFEN0 register is used to set whether the noise filter can be used for the input signal from the serial data input pin to each channel.

Disable the noise filter of the pin used for CSI or simplified I²C communication, by clearing the corresponding bit of this register to 0.

Enable the noise filter of the pin used for UART communication, by setting the corresponding bit of this register to 1.

When the noise filter is enabled, CPU/peripheral hardware clock (f_{CLK}) is synchronized with 2-clock match detection. When the noise filter is OFF, only synchronization is performed with the CPU/peripheral hardware clock (f_{MCK}).

The NFEN0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the NFEN0 register to 00H.

Figure 12-20. Format of Noise Filter Enable Register 0 (NFEN0)

Address: F0070H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN0	0	0	0	SNFEN20	0	SNFEN10	0	SNFEN00

SNFEN20	Use of noise filter of RxD2 pin (RxD2/SDA20/SI20/P14)
0	Noise filter OFF
1	Noise filter ON
Set SNFEN20 to 1 to use the RxD2 pin. Clear SNFEN20 to 0 to use the other than RxD2 pin.	

SNFEN10	Use of noise filter of RxD1 pin (RXD1/ANI16/SI10/SDA10/P03)
0	Noise filter OFF
1	Noise filter ON
Set the SNFEN10 bit to 1 to use the RxD1 pin. Clear the SNFEN10 bit to 0 to use the other than RxD1 pin.	

SNFEN00	Use of noise filter of RxD0 pin (RXD0/TOOLRXD/SDA00/SI00/P11)
0	Noise filter OFF
1	Noise filter ON
Set the SNFEN00 bit to 1 to use the RxD0 pin. Clear the SNFEN00 bit to 0 to use the other than RxD0 pin.	

Caution Be sure to clear bits 7 to 5, 3, and 1 to “0”.

12.3.17 Port input mode registers 0, 1 (PIM0, PIM1)

These registers set the input buffer of ports 0 and 1 in 1-bit units.

The PIM0 and PIM1 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the PIM0 and PIM1 registers to 00H.

Refer to Table 4-16 to see which PIMxx registers are provided for each product.

Figure 12-21. Format of Port Input Mode Registers 0 and 1 (PIM0, PIM1) (64-pin products)

Address F0040H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM0	0	0	0	PIM04	PIM03	0	PIM01	PIM00

Address F0041H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM1	0	PIM16	PIM15	PIM14	PIM13	0	PIM11	PIM10

PIMmn	Pmn pin input buffer selection (m = 0, 1; n = 0, 1, 3 to 6)
0	Normal input buffer
1	TTL input buffer

12.3.18 Port output mode registers 0, 1, 5, 7 (POM0, POM1, POM5, POM7)

These registers set the output mode of ports 0, 1, 5, and 7 in 1-bit units.

The POM0, POM1, POM5, and POM7 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

<R> In addition, POM0, POM1, POM5, and POM7 register is set with PUxx register, whether or not to use the on-chip pull-up resistor.

Reset signal generation clears the POM0, POM1, POM5, and POM7 registers to 00H.

Refer to Tables 4-16 to see which POMxx registers are provided for each product.

Figure 12-22. Format of Port Output Mode Registers 0, 1, 5, 7 (POM0, POM1, POM5, POM7) (64-pin products)

Address F0050H	After reset: 00H	R/W						
Symbol	7	6	5	4	3	2	1	0
POM0	0	0	0	POM04	POM03	POM02	0	0

Address F0051H	After reset: 00H	R/W						
Symbol	7	6	5	4	3	2	1	0
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10

Address F0055H	After reset: 00H	R/W						
Symbol	7	6	5	4	3	2	1	0
POM5	0	0	0	0	0	0	0	POM50

Address F0057H	After reset: 00H	R/W						
Symbol	7	6	5	4	3	2	1	0
POM7	0	0	0	POM74	0	0	POM71	0

POMmn	Pmn pin output buffer selection (m = 0, 1, 5, 7; n = 0 to 5)
0	Normal output mode Enable to the PUmn bit (when the input mode)
1	N-ch open-drain output (V_{DD} tolerance ^{Note 1} / EV_{DD} tolerance ^{Note 2}) mode Disable to the PUmn bit

Notes 1. 25 to 48-pin products

2. 64 -pin products

12.3.19 Port mode registers 0, 1, 3, 5, 7 (PM0, PM1, PM3, PM5, PM7)

These registers set input/output of ports 0, 1, 3, 5, 7 in 1-bit units.

When using the ports (such as P02/ANI17/SO10/TXD1, P04/SCK10/SCL10) to be shared with the serial data output pin or serial clock output pin for serial data output or serial clock output, set the port mode register (PMxx) bit and port <R> mode control register (PMCxx) bit corresponding to each port to 0. And set the port register (Pxx) bit corresponding to each port to 1

Example: When using P02/ANI17/SO10/TXD1 for serial data output

<R> Set the PMC02 bit of the port mode control register 0 to 0.
 Set the PM02 bit of the port mode register 0 to 0.
 Set the P02 bit of the port register 0 to 1.

When using the ports (such as P04/SCK10/SCL10, P50/ANI26/INTP1/SI11/SDA11) to be shared with the serial data input pin or serial clock input pin for serial data input or serial clock input, set the port mode register (PMxx) bit <R> corresponding to each port to 1. And set the port mode control register (PMCxx) bit to 0. At this time, the port register (Pxx) bit may be 0 or 1.

Example: When using P50/INTP1/SI11/SDA11 for serial data input

<R> Set the PMC50 bit of port mode control register 5 to 0.
 Set the PM50 bit of port mode register 5 to 1.
 Set the P50 bit of port register 5 to 0 or 1.

The PM0, PM1, PM3, PM5, PM7 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the PM0, PM1, PM3, PM5, PM7 registers to FFH.

Refer to Table 4-16 to see which PMxx registers are provided for each product.

Figure 12-23. Format of Port Mode Registers 0, 1, 3, 5, and 7 (PM0, PM1, PM3, PM5, and PM7) (64-pin products)

Address: FFF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

Address: FFF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	1	1	PM31	PM30

Address: FFF25H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM5	1	1	1	1	PM53	PM52	PM51	PM50

Address: FFF27H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70

PMmn	Pmn pin I/O mode selection (m = 0, 1, 3, 5, 7; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

12.4 Operation stop mode

Each serial interface of serial array unit has the operation stop mode.

In this mode, serial communication cannot be executed, thus reducing the power consumption.

In addition, the pin for serial interface can be used as port function pins in this mode.

12.4.1 Stopping the operation by units

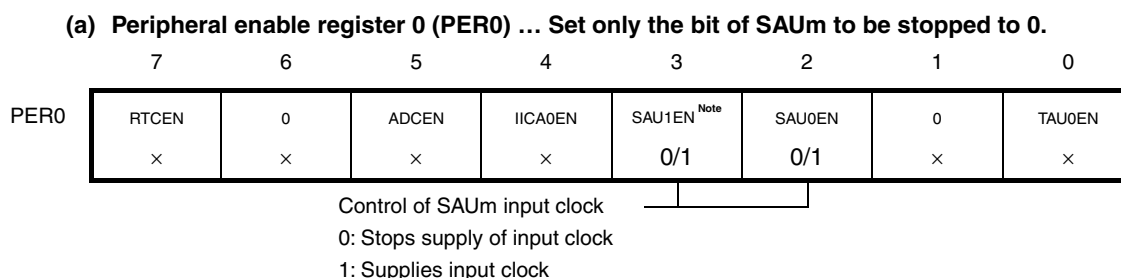
The stopping of the operation by units is set by using peripheral enable register 0 (PER0).

The PER0 register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

To stop the operation of serial array unit 0, set bit 2 (SAU0EN) to 0.

To stop the operation of serial array unit 1, set bit 3 (SAU1EN) to 0.

Figure 12-24. Peripheral Enable Register 0 (PER0) Setting When Stopping the Operation by Units



Note 32, 48, and 64-pin products only.

Cautions 1. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read

Note that this does not apply to the following registers.

- Input switch control register (ISC)
- Noise filter enable register 0 (NFEN0)
- Port input mode registers 0, 1 (PIM0, PIM1)
- Port output mode registers 0, 1, 5, 7 (POM0, POM1, POM5, POM7)
- Port mode control registers 0, 1, 3, 5, 7 (PMC0, PMC1, PMC3, PMC5, PMC7)
- Port mode registers 0, 1, 3, 5, 7 (PM0, PM1, PM3, PM5, PM7)
- Port registers 0, 1, 3, 5, 7 (P0, P1, P3, P5, P7)

2. Be sure to clear the following bits to 0.

25-pin products: bits 1, 3, 6

32, 48, 64-pin products: bits 1, 6

Remark ×: Bits not used with serial array units (depending on the settings of other peripheral functions)

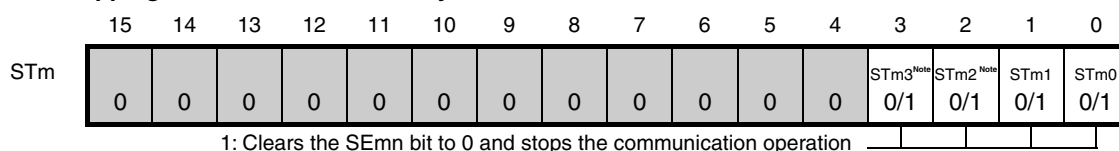
0/1: Set to 0 or 1 depending on the usage of the user

12.4.2 Stopping the operation by channels

The stopping of the operation by channels is set using each of the following registers.

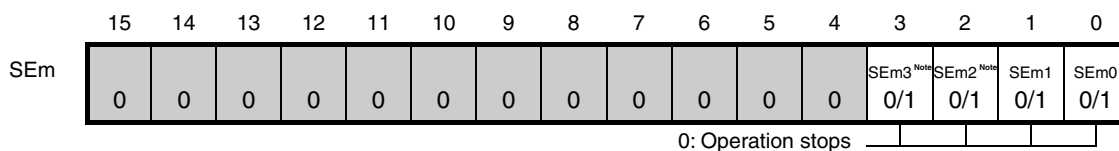
Figure 12-25. Each Register Setting When Stopping the Operation by Channels

- (a) **Serial channel stop register m (STm) ... This register is a trigger register that is used to enable stopping communication/count by each channel.**



* Because the ST_{mn} bit is a trigger bit, it is cleared immediately when SE_{mn} = 0.

- (b) **Serial Channel Enable Status Register m (SEm) ... This register indicates whether data transmission/reception operation of each channel is enabled or stopped.**



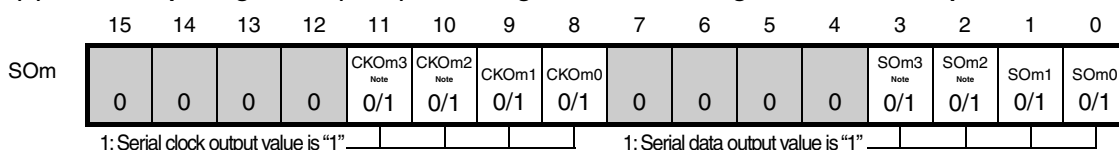
* The SEm register is a read-only status register, whose operation is stopped by using the STm register. With a channel whose operation is stopped, the value of the CKOm_n bit of the SOm register can be set by software.

- (c) **Serial output enable register m (SOEm) ... This register is a register that is used to enable or stop output of the serial communication operation of each channel.**



* For channel n, whose serial output is stopped, the SO_{mn} bit value of the SOm register can be set by software.

- (d) **Serial output register m (SOm) ... This register is a buffer register for serial output of each channel.**



* When using pins corresponding to each channel as port function pins, set the corresponding CKOm_n, SOm_n bits to "1".

Note Serial array unit 0 only.

- Remarks 1.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 10 to 13, 10, 11
2.  : Setting disabled (fixed by hardware), 0/1: Set to 0 or 1 depending on the usage of the user

12.5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) Communication

This is a clocked communication function that uses three lines: serial clock ($\overline{\text{SCK}}$) and serial data (SI and SO) lines.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

During master communication (CSI00): Max. $f_{\text{CLK}}/2$ ^{Notes 1, 2}

During master communication (other than CSI00): Max. $f_{\text{CLK}}/4$ ^{Note 2}

During slave communication: Max. $f_{\text{MCK}}/6$ ^{Note 2}

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

In addition, CSI00 of following channels supports the SNOOZE mode. When $\overline{\text{SCK}}$ input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only following CSIs can be specified.

- <R> **Notes 1.** In master communication (CSI00), maximum transfer rate become $f_{\text{CLK}}/2$ when the following conditions.
- $2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6 \text{ V}$
 - $f_{\text{MCK}} \leq 24 \text{ MHz}$
- Other cases, maximum transfer rate become $f_{\text{CLK}}/4$.
- 2.** Use the clocks within a range satisfying the $\overline{\text{SCK}}$ cycle time (t_{KCY}) characteristics (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = -40 to +105°C) (TARGET)**).

The channels supporting 3-wire serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) are channels 0 to 3 of SAU0 and channels 0 to 3 of SAU1.

- 25-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	–		–
	2	–	UART1	–
	3	CSI11		IIC11

- 32-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	–		–
	2	–	UART1	–
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	–		–

- 48-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	CSI01		IIC01
	2	–	UART1	–
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	CSI21		IIC21

- 64-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	CSI01		IIC01
	2	CSI10	UART1	IIC10
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	CSI21		IIC21

3-wire serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) performs the following seven types of communication operations.

- Master transmission (See **12.5.1.**)
- Master reception (See **12.5.2.**)
- Master transmission/reception (See **12.5.3.**)
- Slave transmission (See **12.5.4.**)
- Slave reception (See **12.5.5.**)
- Slave transmission/reception (See **12.5.6.**)
- SNOOZE mode function (See **12.5.7.**)

12.5.1 Master transmission

Master transmission is that the RL78/G1A outputs a transfer clock and transmits data to another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI11	CSI20	CSI21
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1	Channel 1 of SAU1
Pins used	$\overline{\text{SCK00}}$, SO00	$\overline{\text{SCK01}}$, SO01	$\overline{\text{SCK10}}$, SO10	$\overline{\text{SCK11}}$, SO11	$\overline{\text{SCK20}}$, SO20	$\overline{\text{SCK21}}$, SO21
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI11	INTCSI20	INTCSI21
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.					
Error detection flag	None					
Transfer data length	7 or 8 bits					
Transfer rate	Max. $f_{\text{CLK}}/2$ [Hz] (CSI00), $f_{\text{CLK}}/4$ [Hz] (other than CSI00) Min. $f_{\text{CLK}}/(2 \times 2^{15} \times 128)$ [Hz] ^{Note} f_{CLK} : System clock frequency					
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data output starts from the start of the operation of the serial clock. • DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristic in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = -40 to +105°C) (TARGET)**).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

(1) Register setting

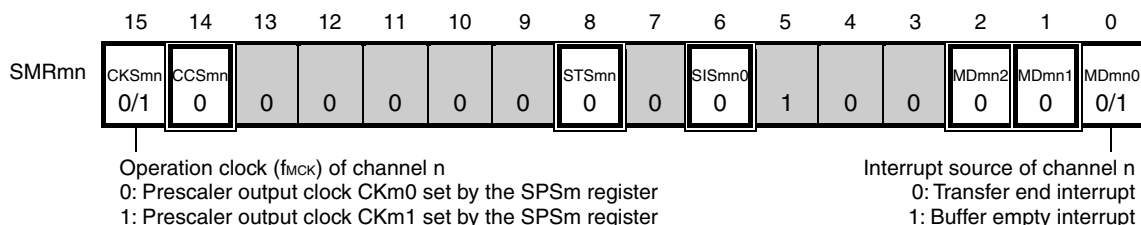
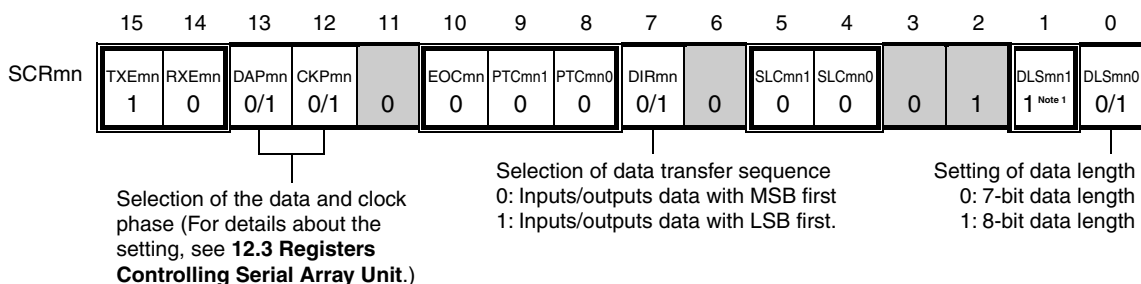
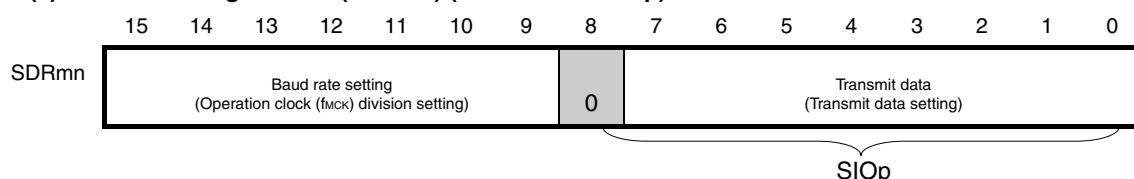
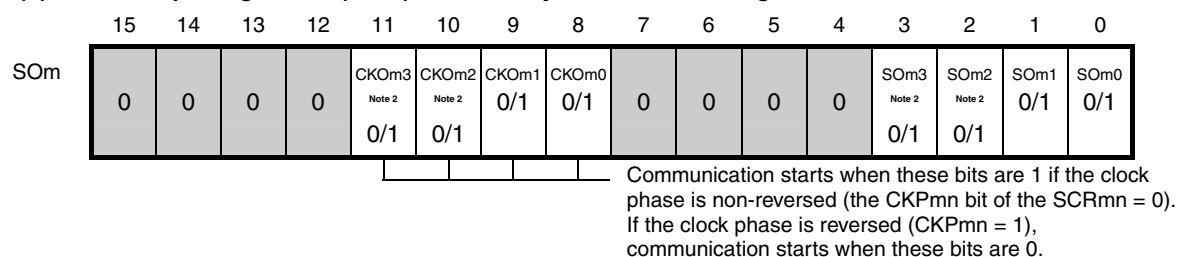
Figure 12-26. Example of Contents of Registers for Master Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) (1/2)**(a) Serial mode register mn (SMRmn)****(b) Serial communication operation setting register mn (SCRmn)****(c) Serial data register mn (SDRmn) (lower 8 bits: SIOP)****(d) Serial output register m (SOM) ... Sets only the bits of the target channel.****Notes 1.** Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.**2.** Unit 0 only**Remarks 1.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
 p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11**2.** : Setting is fixed in the CSI master transmission mode, : Setting disabled (set to the initial value)
 0/1: Set to 0 or 1 depending on the usage of the user

Figure 12-26. Example of Contents of Registers for Master Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) (2/2)

(e) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOEm3 Note 0/1	SOEm2 Note 0/1	SOEm1 0/1	SOEm0 0/1

(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 0/1	SSm2 Note 0/1	SSm1 0/1	SSm0 0/1

Note Unit 0 only

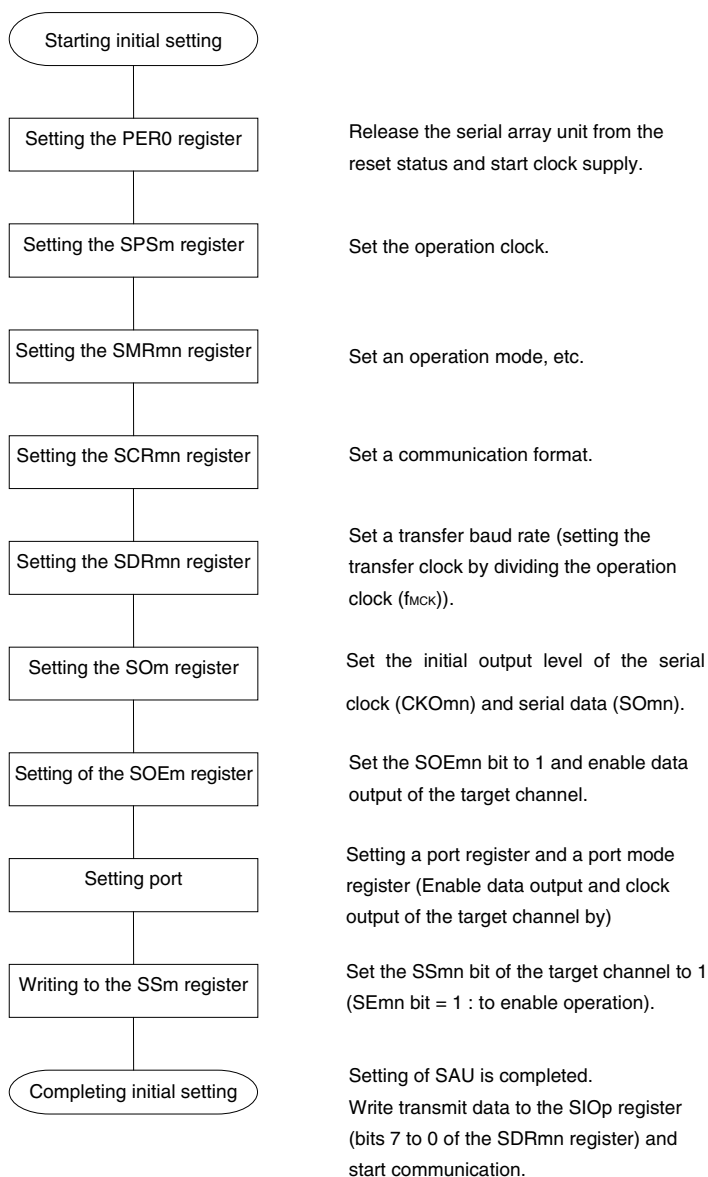
Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

2. : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

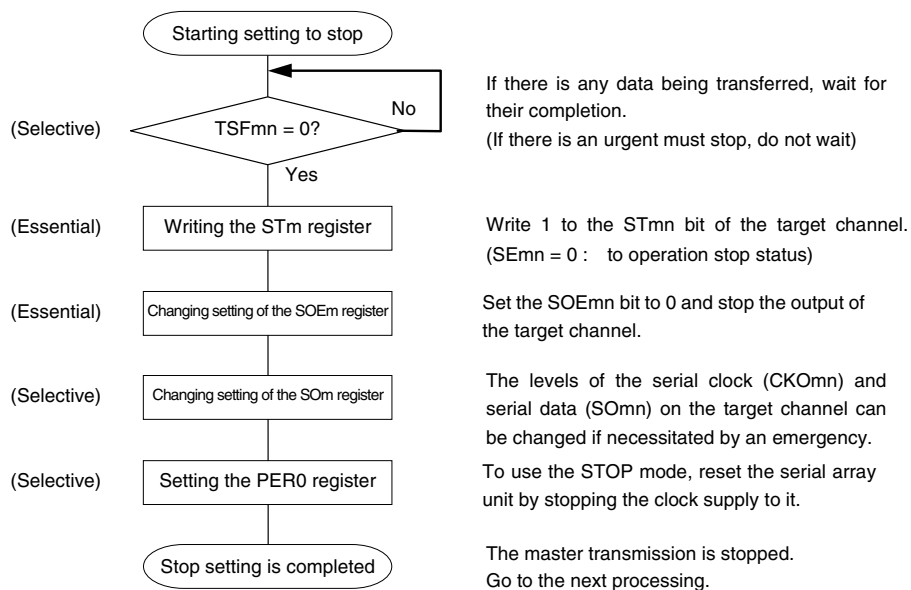
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 12-27. Initial Setting Procedure for Master Transmission

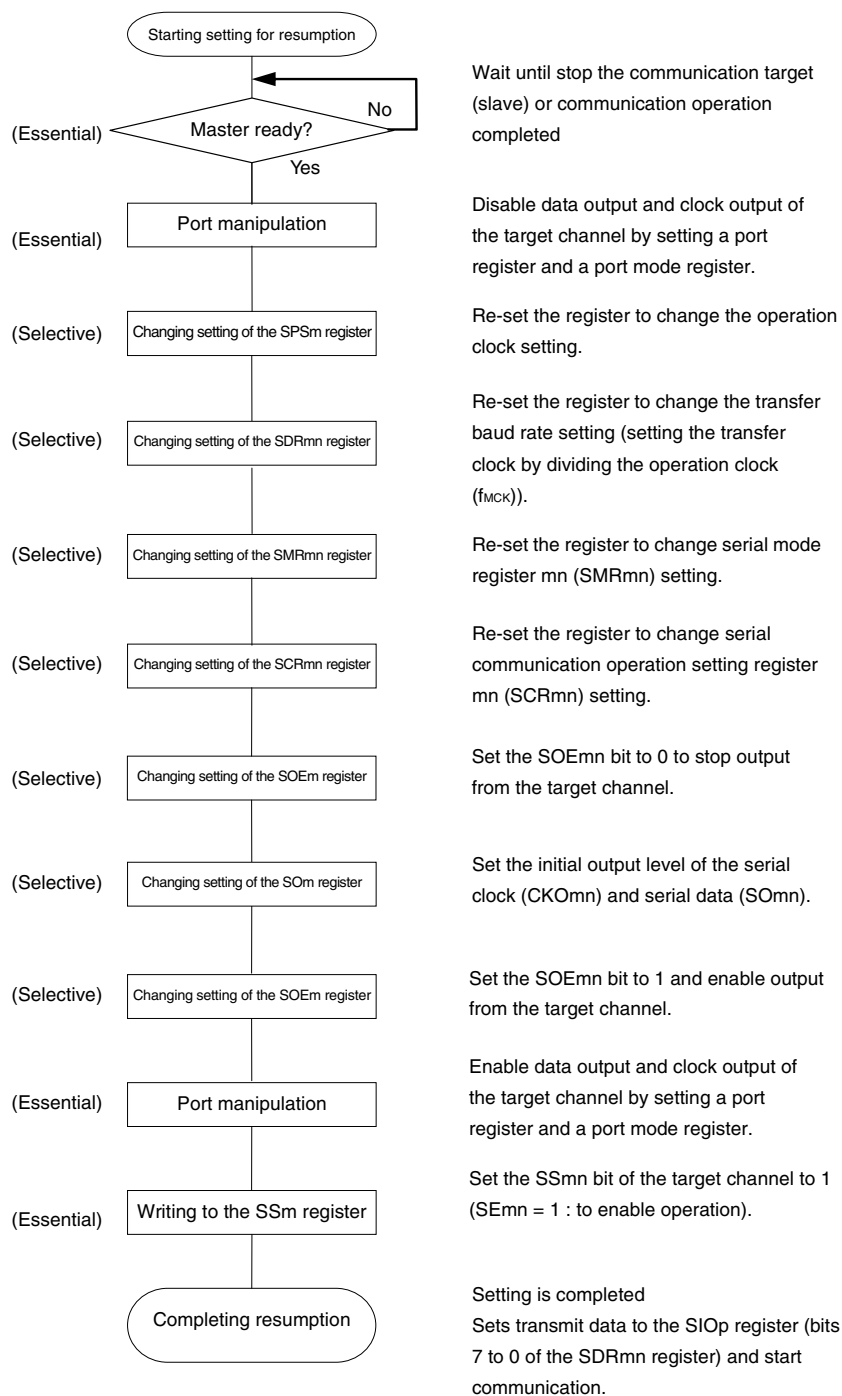
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

<R>

Figure 12-28. Procedure for Stopping Master Transmission

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

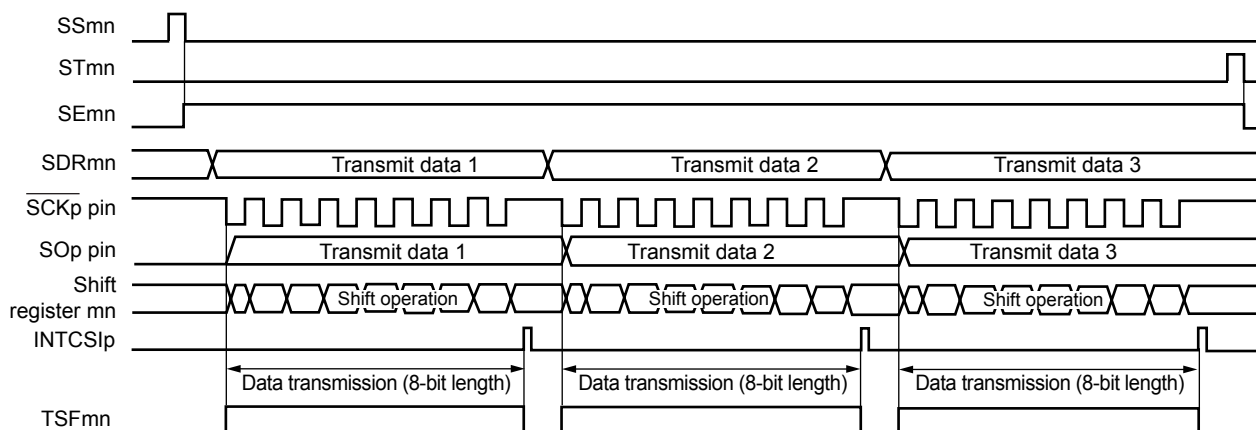
<R>

Figure 12-29. Procedure for Resuming Master Transmission

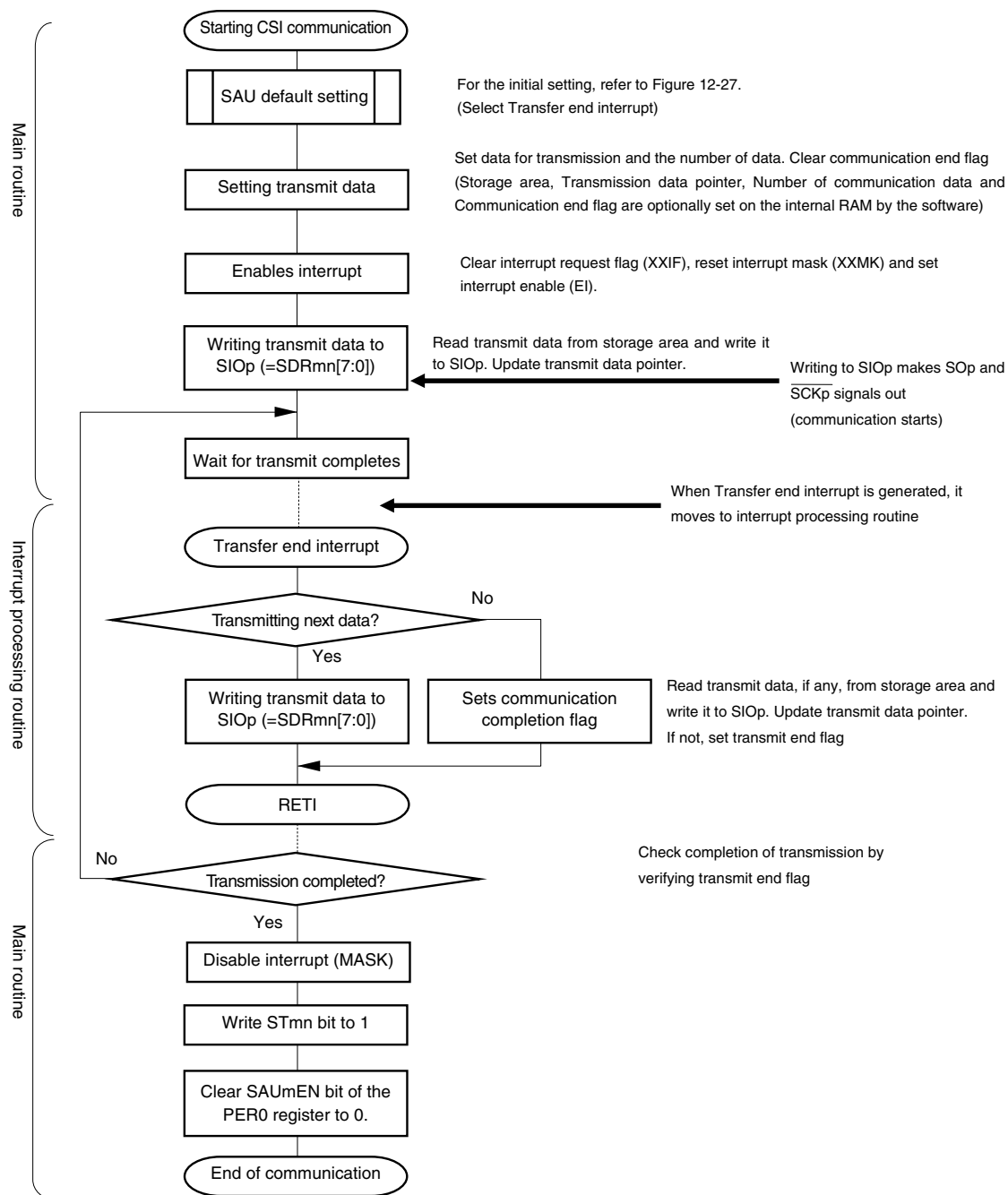
- Remarks 1.** If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (slave) stops or transmission finishes, and then perform initialization instead of restarting the transmission.
- 2.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

(3) Processing flow (in single-transmission mode)

Figure 12-30. Timing Chart of Master Transmission (in Single-Transmission Mode)
 (Type 1: DAPmn = 0, CKPmn = 0)



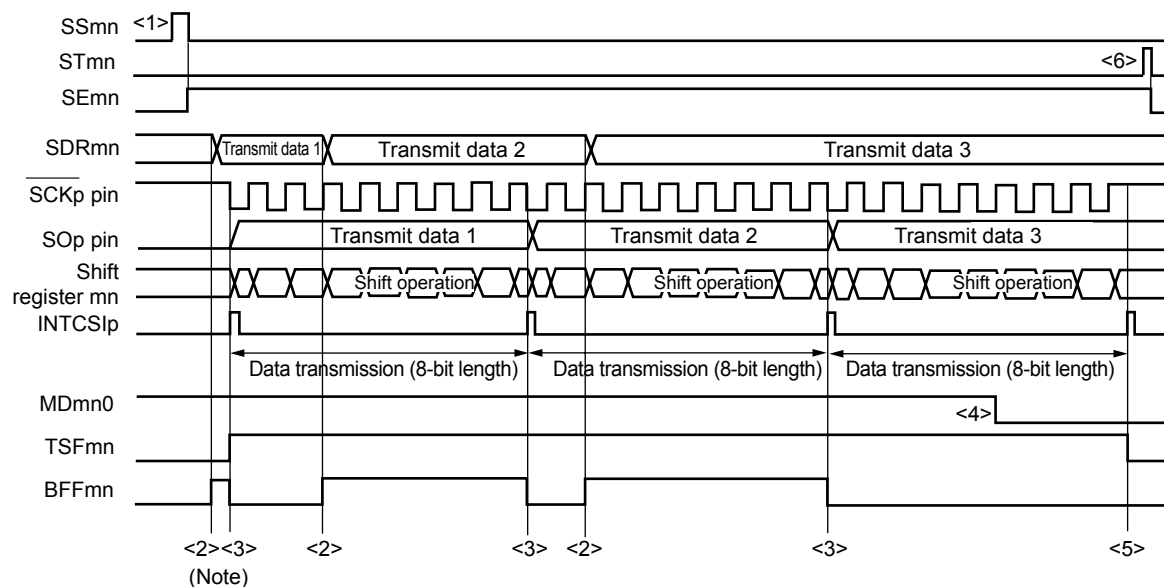
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21),
 mn = 00 to 03, 10, 11

Figure 12-31. Flowchart of Master Transmission (in Single-Transmission Mode)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21),
mn = 00 to 03, 10, 11

(4) Processing flow (in continuous transmission mode)

Figure 12-32. Timing Chart of Master Transmission (in Continuous Transmission Mode)
 (Type 1: DAPmn = 0, CKPmn = 0)

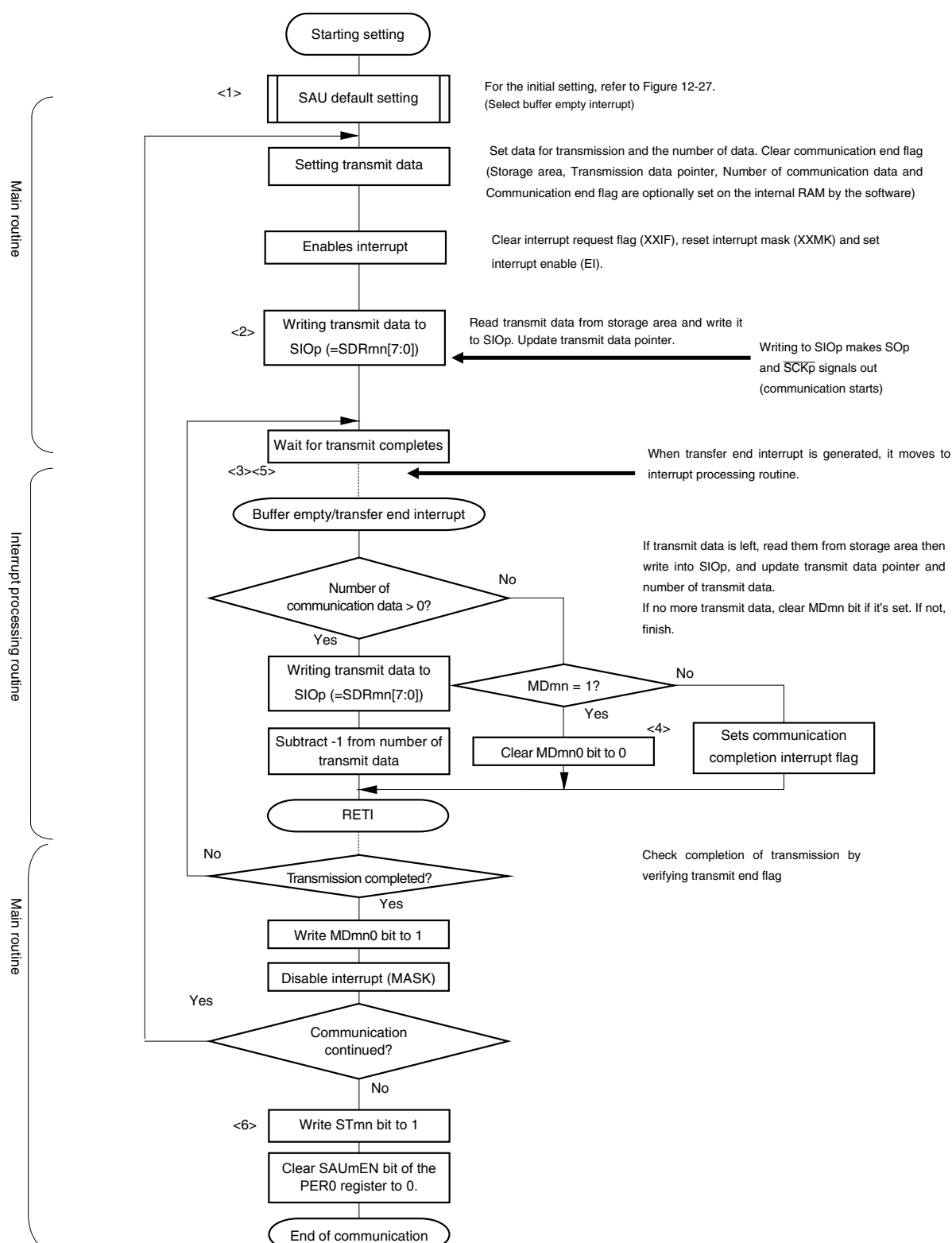


Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

Figure 12-33. Flowchart of Master Transmission (in Continuous Transmission Mode)



Remarks 1. <1> to <6> in the figure correspond to <1> to <6> in **Figure 12-32 Timing Chart of Master Transmission (in Continuous Transmission Mode).**

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

12.5.2 Master reception

Master reception is that the RL78/G1A outputs a transfer clock and receives data from other device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI11	CSI20	CSI21
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1	Channel 1 of SAU1
Pins used	$\overline{\text{SCK00}}$, SI00	$\overline{\text{SCK01}}$, SI01	$\overline{\text{SCK10}}$, SI10	$\overline{\text{SCK11}}$, SI11	$\overline{\text{SCK20}}$, SI20	$\overline{\text{SCK21}}$, SI21
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI11	INTCSI20	INTCSI21
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.					
Error detection flag	Overflow error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. $f_{\text{CLK}}/2$ [Hz] (CSI00), $f_{\text{CLK}}/4$ [Hz] (other than CSI00) Min. $f_{\text{CLK}}/(2 \times 2^{15} \times 128)$ [Hz] ^{Note} f_{CLK} : System clock frequency					
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data input starts from the start of the operation of the serial clock. • DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

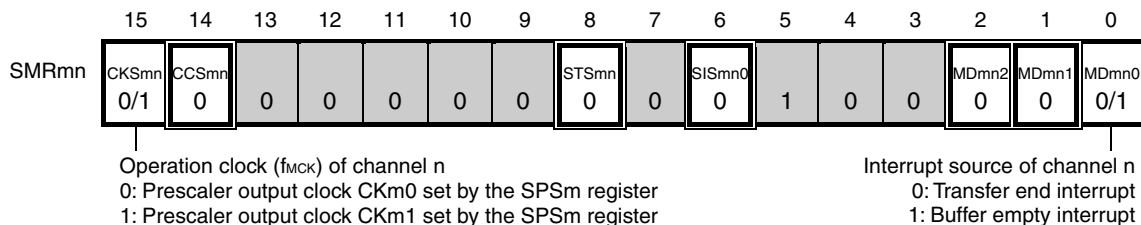
Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristic in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = -40 to +105°C) (TARGET)**).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

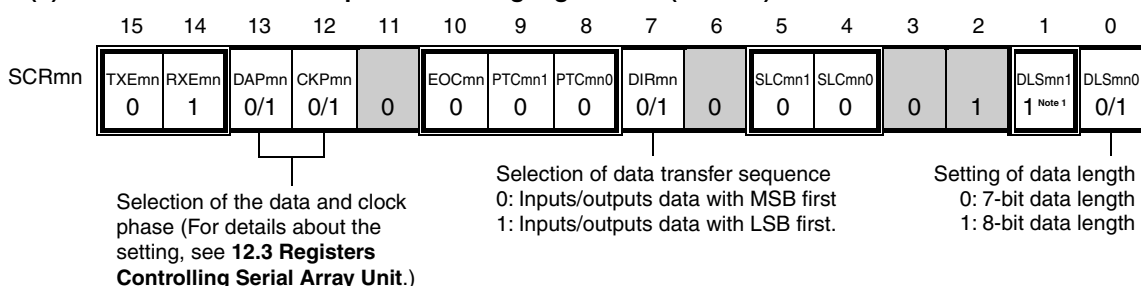
(1) Register setting

**Figure 12-34. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O
(CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) (1/2)**

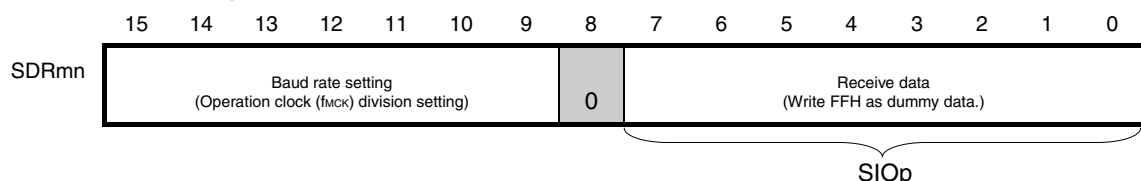
(a) Serial mode register mn (SMRmn)



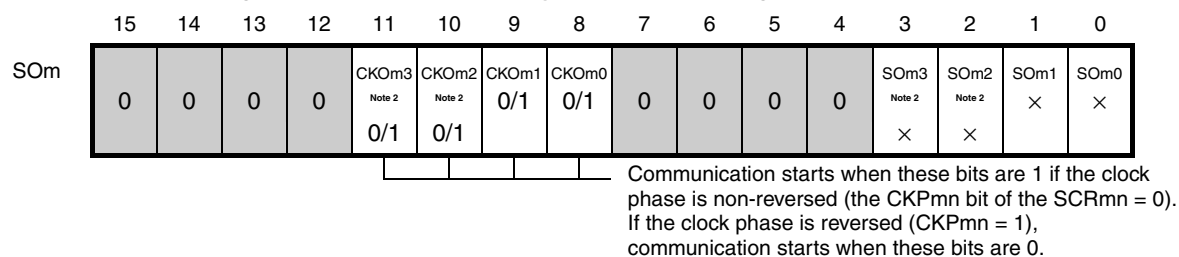
(b) Serial communication operation setting register mn (SCRmn)



(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOM) ... Sets only the bits of the target channel.



Notes 1. Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.

2. Unit 0 only

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

2. : Setting is fixed in the CSI master reception mode, : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-34. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O
(CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, CSI30, CSI31) (2/2)**

(e) Serial output enable register m (SOEm) ...The register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOEm3 Note ×	SOEm2 Note ×	SOEm1 ×	SOEm0 ×

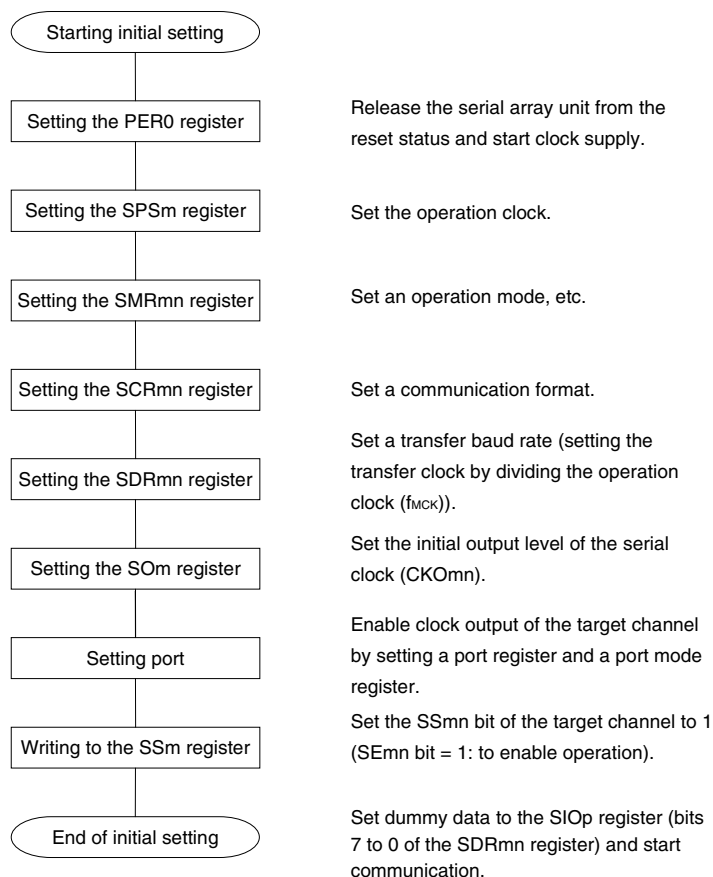
(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 0/1	SSm2 Note 0/1	SSm1 0/1	SSm0 0/1

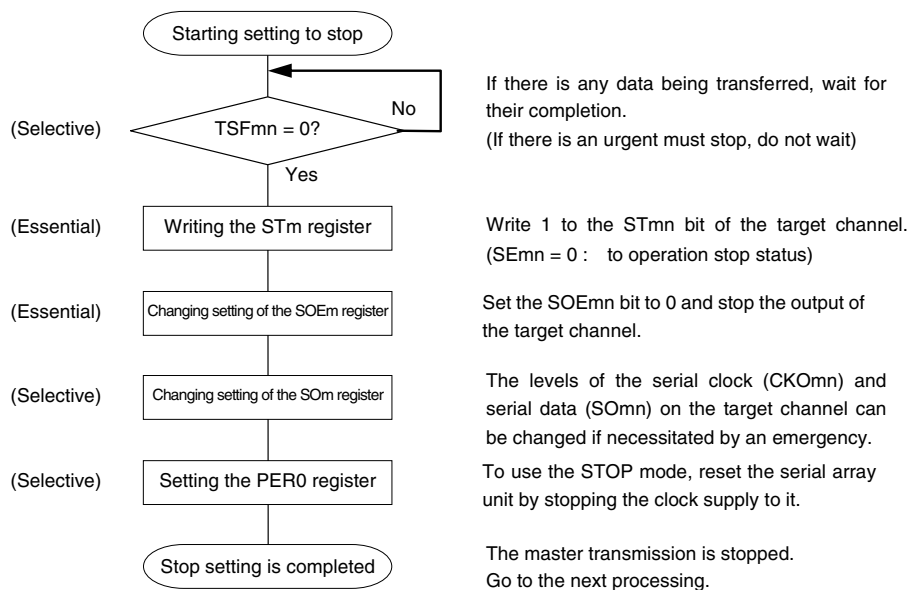
Note Unit 0 only

- Remarks** 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21),
mn = 00 to 03, 10, 11
2.  : Setting disabled (set to the initial value)
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
 0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

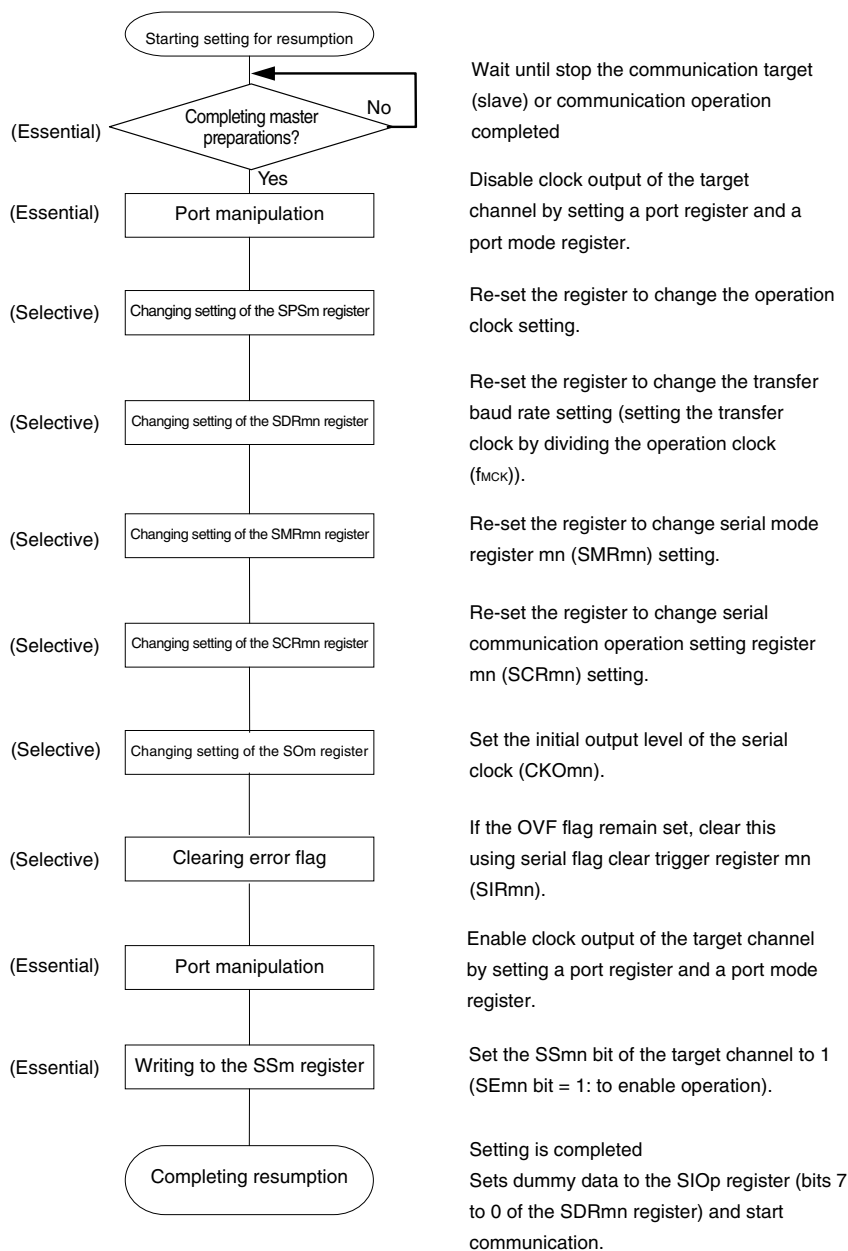
Figure 12-35. Initial Setting Procedure for Master Reception

<R>

Figure 12-36. Procedure for Stopping Master Reception

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

<R>

Figure 12-37. Procedure for Resuming Master Reception

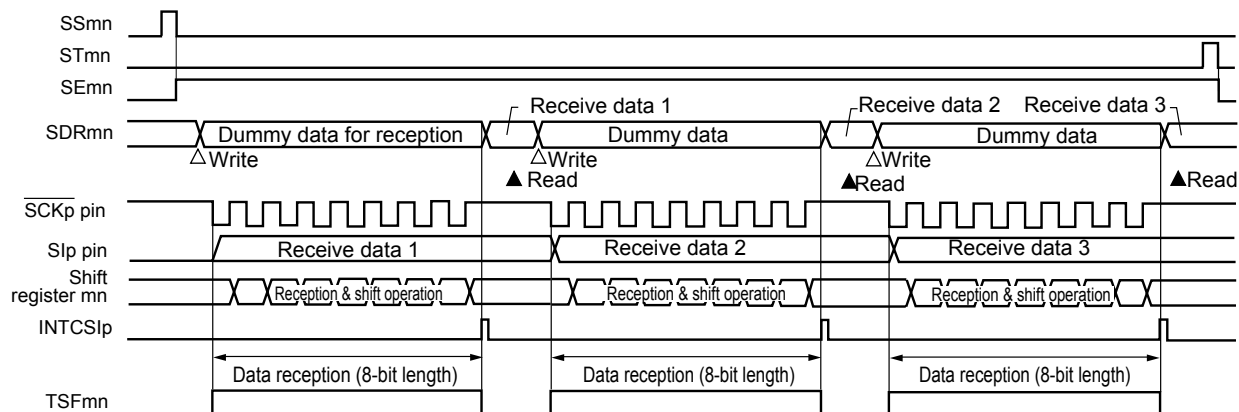
Remarks 1. If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (slave) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

- 2.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

(3) Processing flow (in single-reception mode)

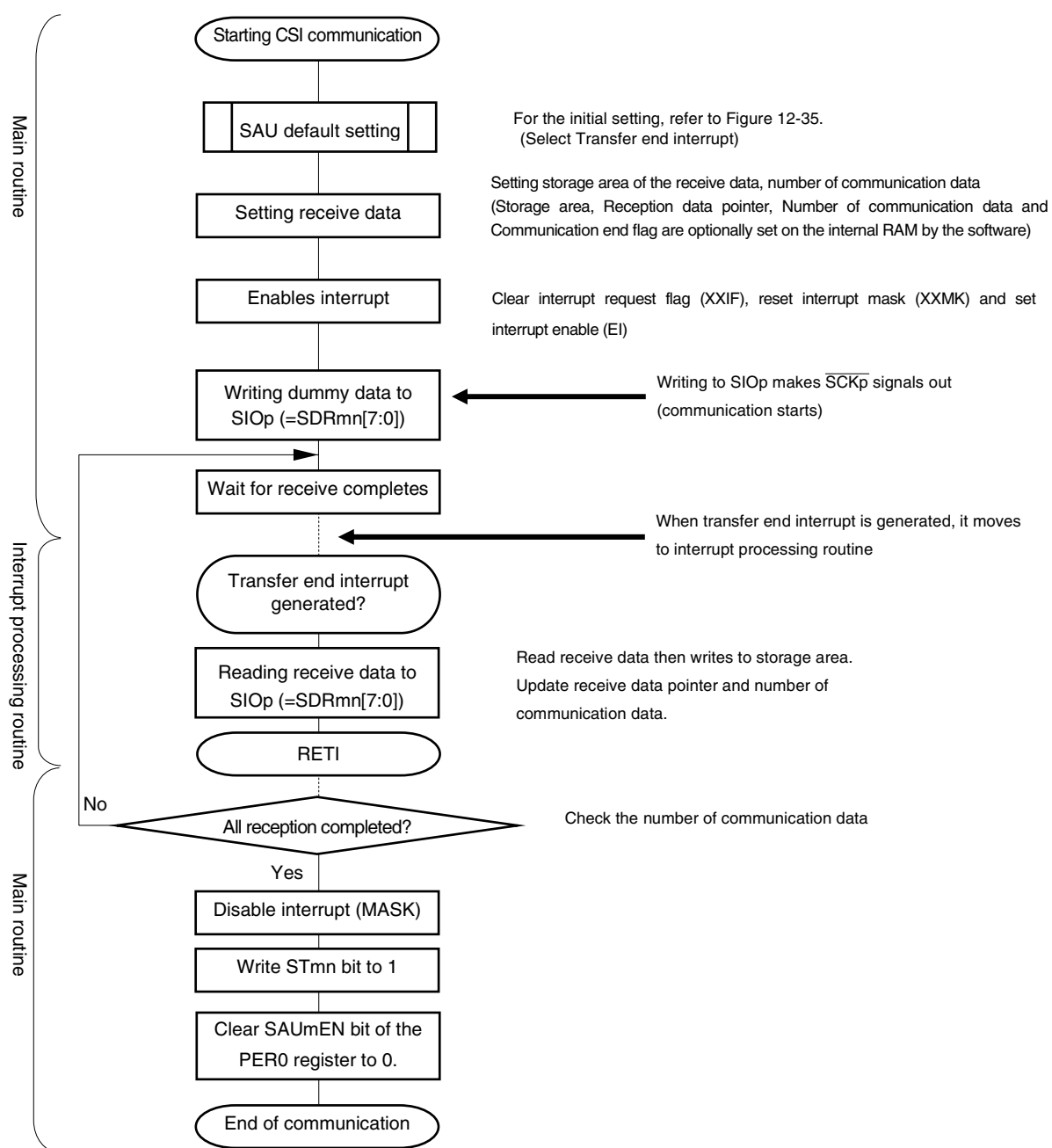
Figure 12-38. Timing Chart of Master Reception (in Single-Reception Mode)

(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21),
mn = 00 to 03, 10, 11

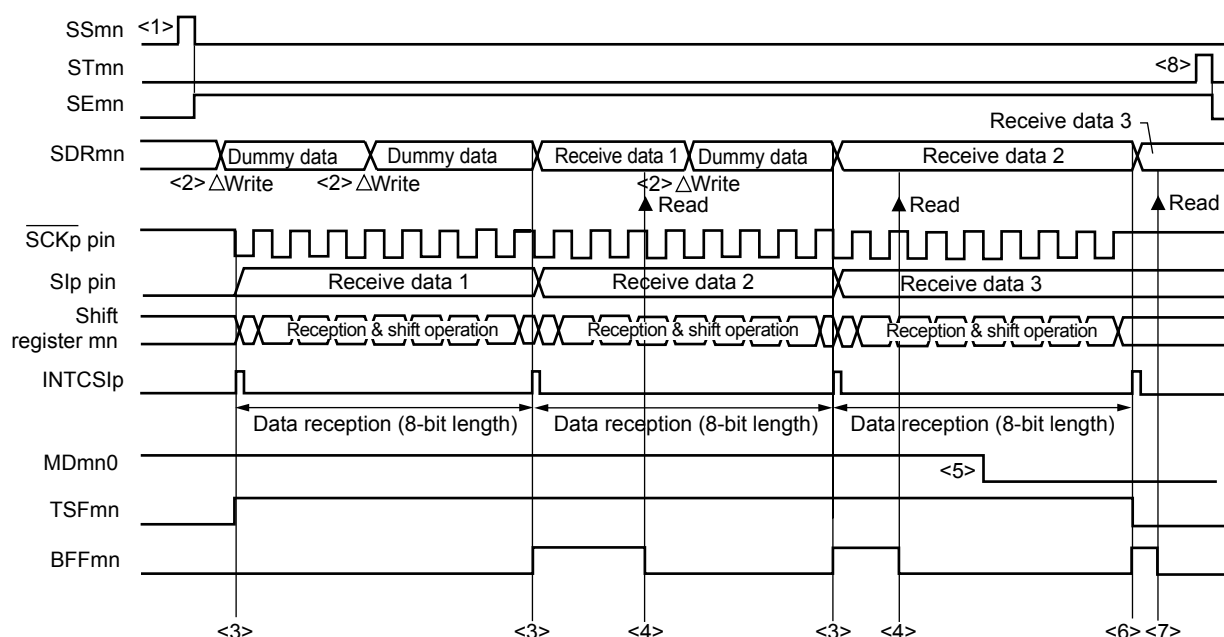
Figure 12-39. Flowchart of Master Reception (in Single-Reception Mode)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

(4) Processing flow (in continuous reception mode)

Figure 12-40. Timing Chart of Master Reception (in Continuous Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



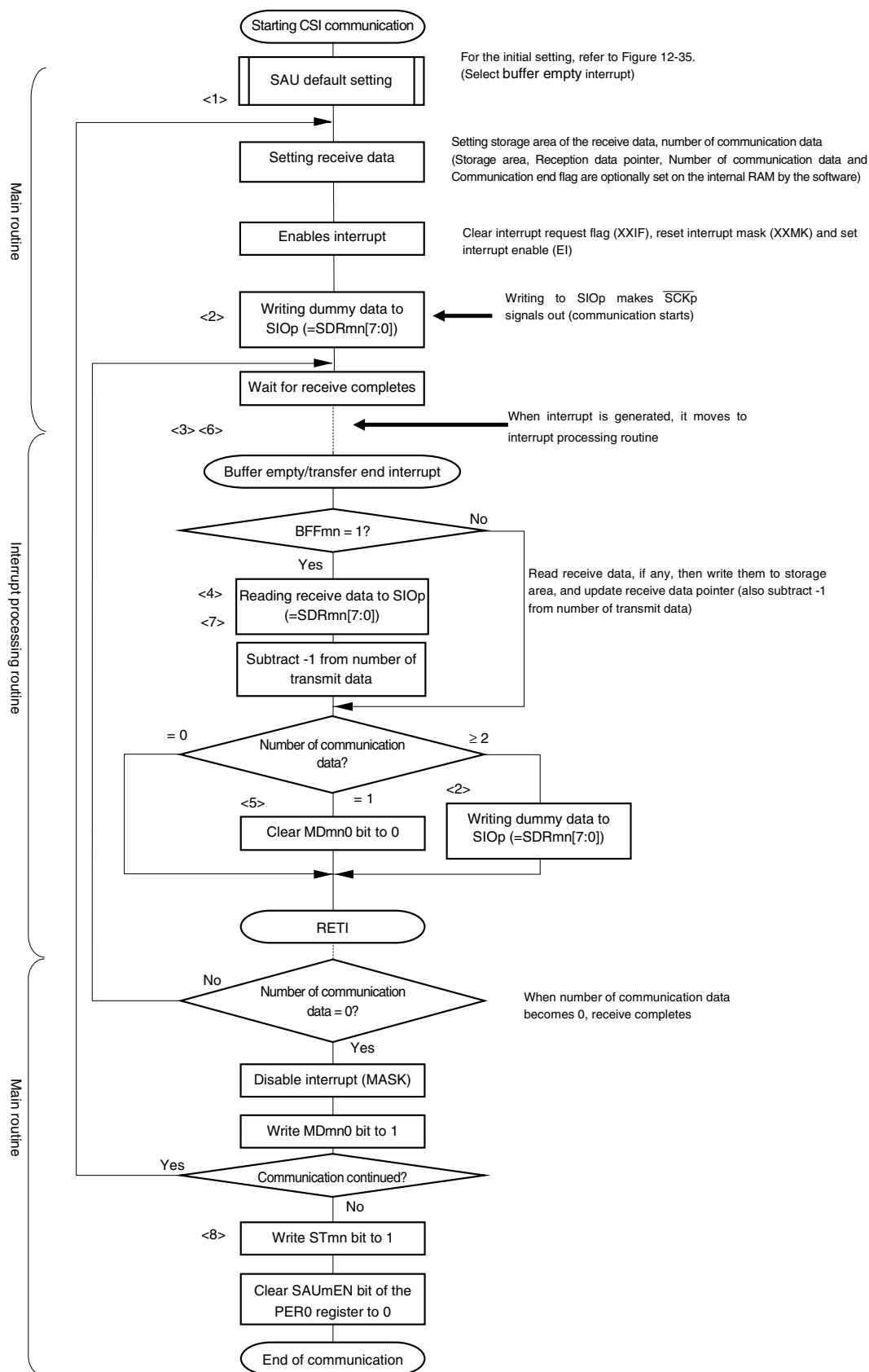
Caution The MDmn0 bit can be rewritten even during operation.

However, rewrite it before receive of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last receive data.

Remarks 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 12-41 Flowchart of Master Reception (in Continuous Reception Mode)**.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

Figure 12-41. Flowchart of Master Reception (in Continuous Reception Mode)



Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 12-40 Timing Chart of Master Reception (in Continuous Reception Mode)**.

12.5.3 Master transmission/reception

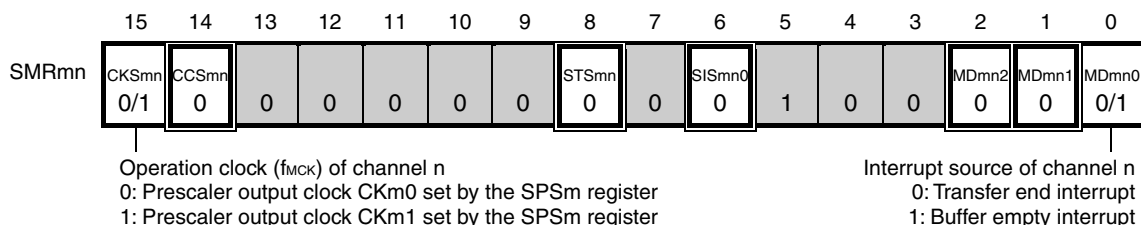
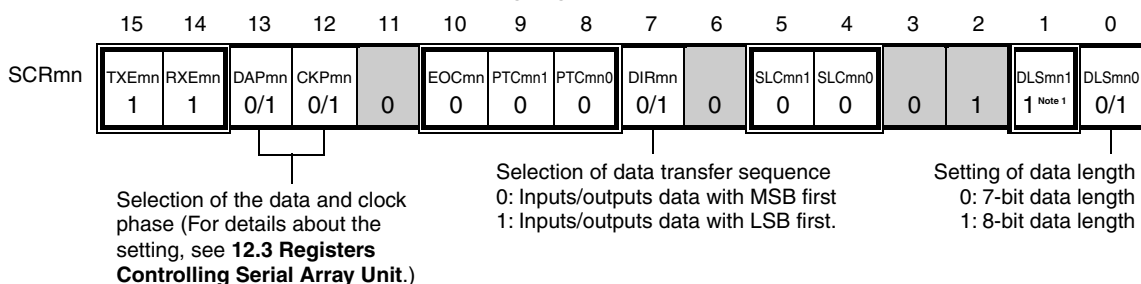
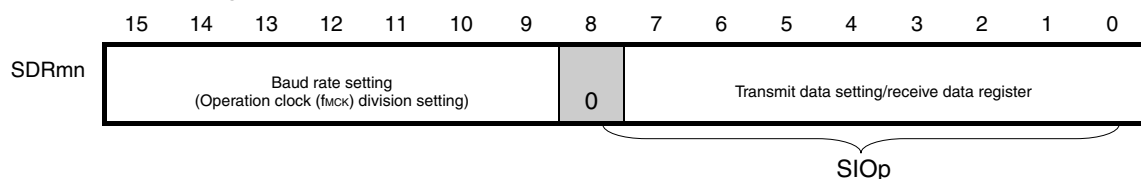
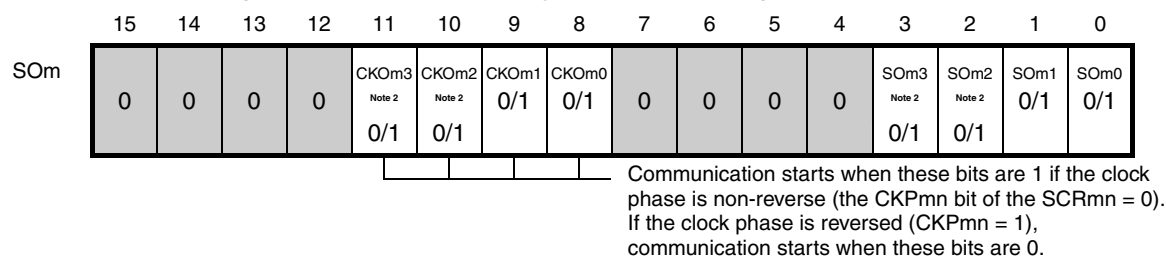
Master transmission/reception is that the RL78/G1A outputs a transfer clock and transmits/receives data to/from other device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI11	CSI20	CSI21
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1	Channel 1 of SAU1
Pins used	$\overline{\text{SCK00}}$, SI00, SO00	$\overline{\text{SCK01}}$, SI01, SO01	$\overline{\text{SCK10}}$, SI10, SO10	$\overline{\text{SCK11}}$, SI11, SO11	$\overline{\text{SCK20}}$, SI20, SO20	$\overline{\text{SCK21}}$, SI21, SO21
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI11	INTCSI20	INTCSI21
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. $f_{\text{CLK}}/2$ [Hz] (CSI00), $f_{\text{CLK}}/4$ [Hz] (other than CSI00) Min. $f_{\text{CLK}}/(2 \times 2^{15} \times 128)$ [Hz] ^{Note} f_{CLK} : System clock frequency					
Data phase	Selectable by the DAPmn bit of the SCRmn register - DAPmn = 0: Data I/O starts at the start of the operation of the serial clock. - DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register - CKPmn = 0: Non-reverse - CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristic in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = -40 to +105°C) (TARGET)**).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

(1) Register setting

Figure 12-42. Example of Contents of Registers for Master Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, CSI30, CSI31) (1/2)**(a) Serial mode register mn (SMRmn)****(b) Serial communication operation setting register mn (SCRmn)****(c) Serial data register mn (SDRmn) (lower 8 bits: SIOP)****(d) Serial output register m (SOM) ... Sets only the bits of the target channel.**

- Notes 1.** Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.
2. Unit 0 only

- Remarks 1.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11
2. ☐: Setting is fixed in the CSI master transmission/reception mode
☐: Setting disabled (set to the initial value)
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
 0/1: Set to 0 or 1 depending on the usage of the user

Figure 12-42. Example of Contents of Registers for Master Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, CSI30, CSI31) (2/2)

(e) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOEm3 Note 0/1	SOEm2 Note 0/1	SOEm1 0/1	SOEm0 0/1

(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 0/1	SSm2 Note 0/1	SSm1 0/1	SSm0 0/1

Note Serial array unit 0 only.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

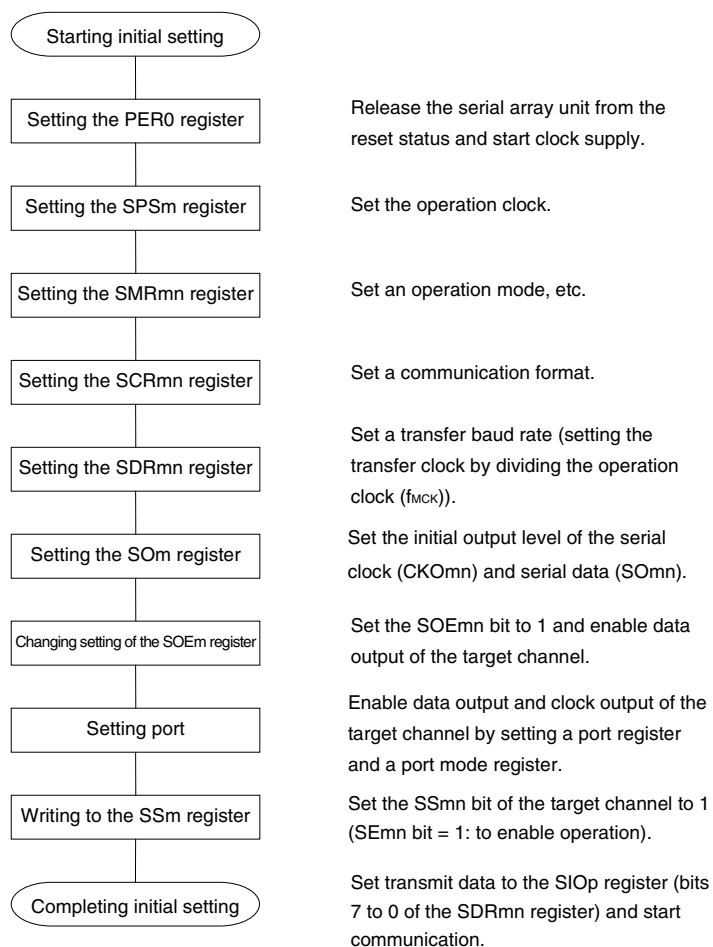
2.  : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

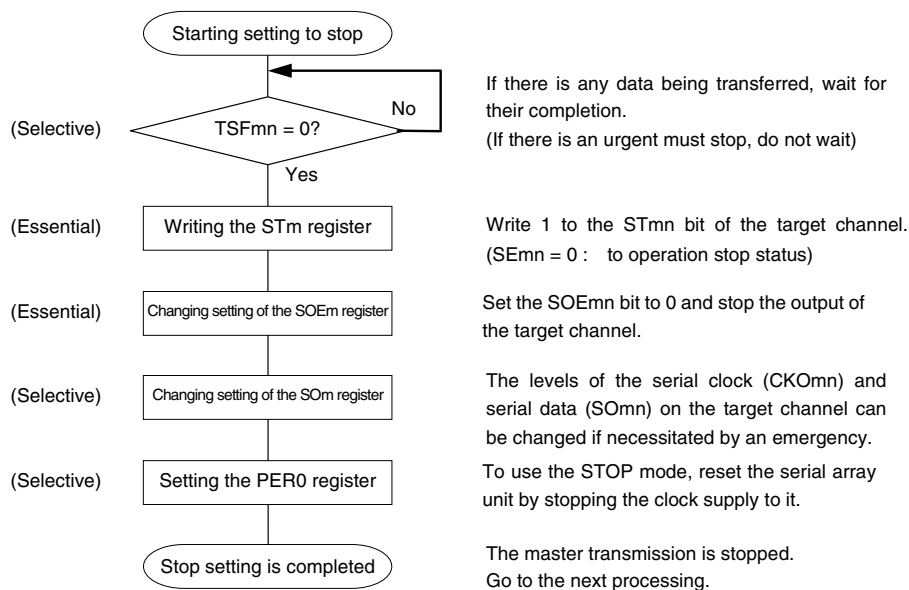
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 12-43. Initial Setting Procedure for Master Transmission/Reception

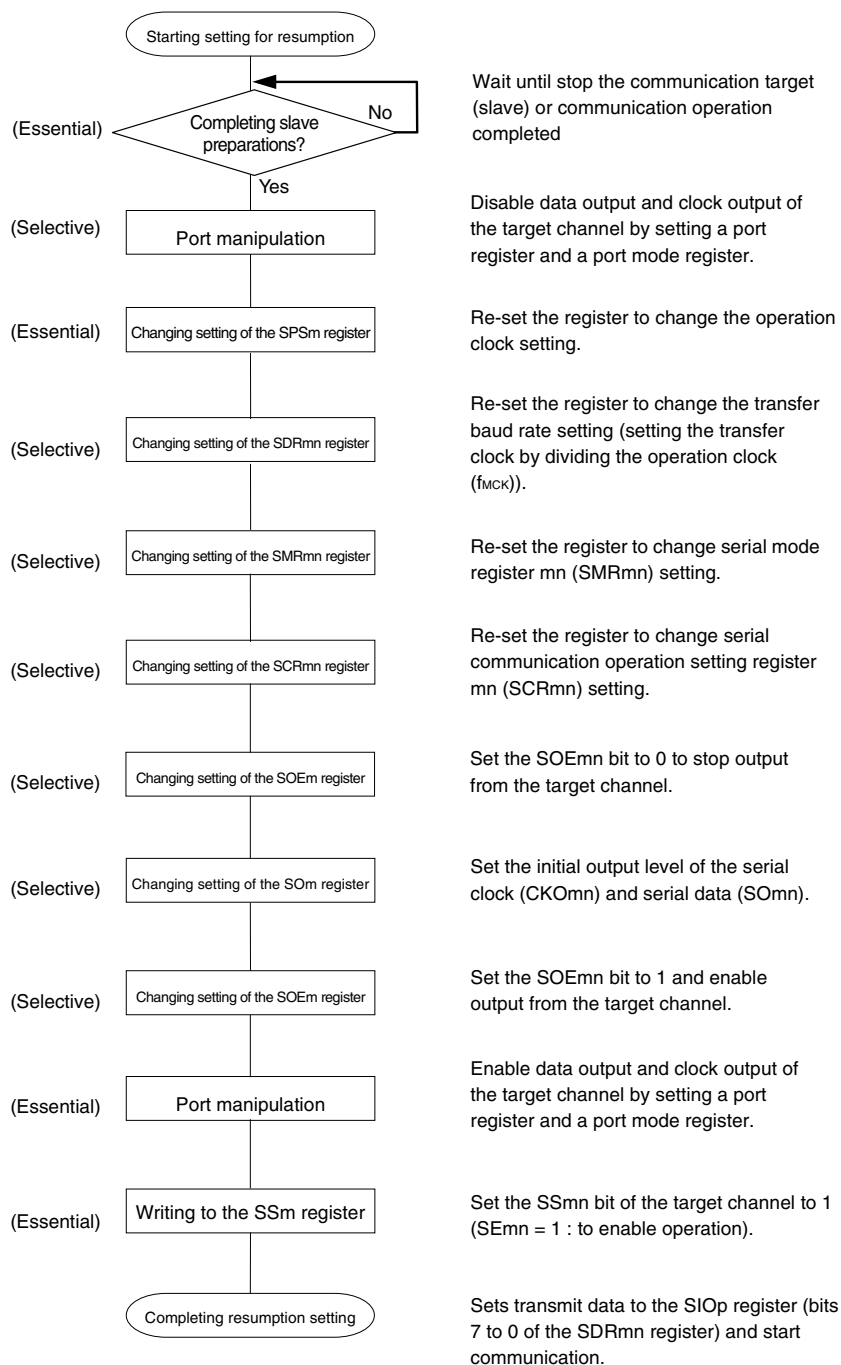


<R>

Figure 12-44. Procedure for Stopping Master Transmission/Reception

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

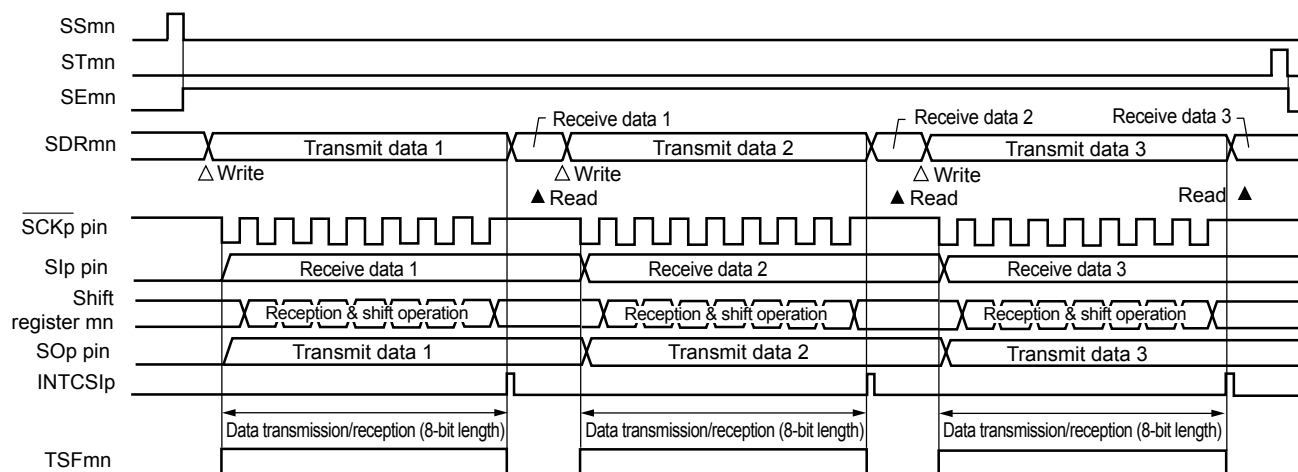
<R>

Figure 12-45. Procedure for Resuming Master Transmission/Reception

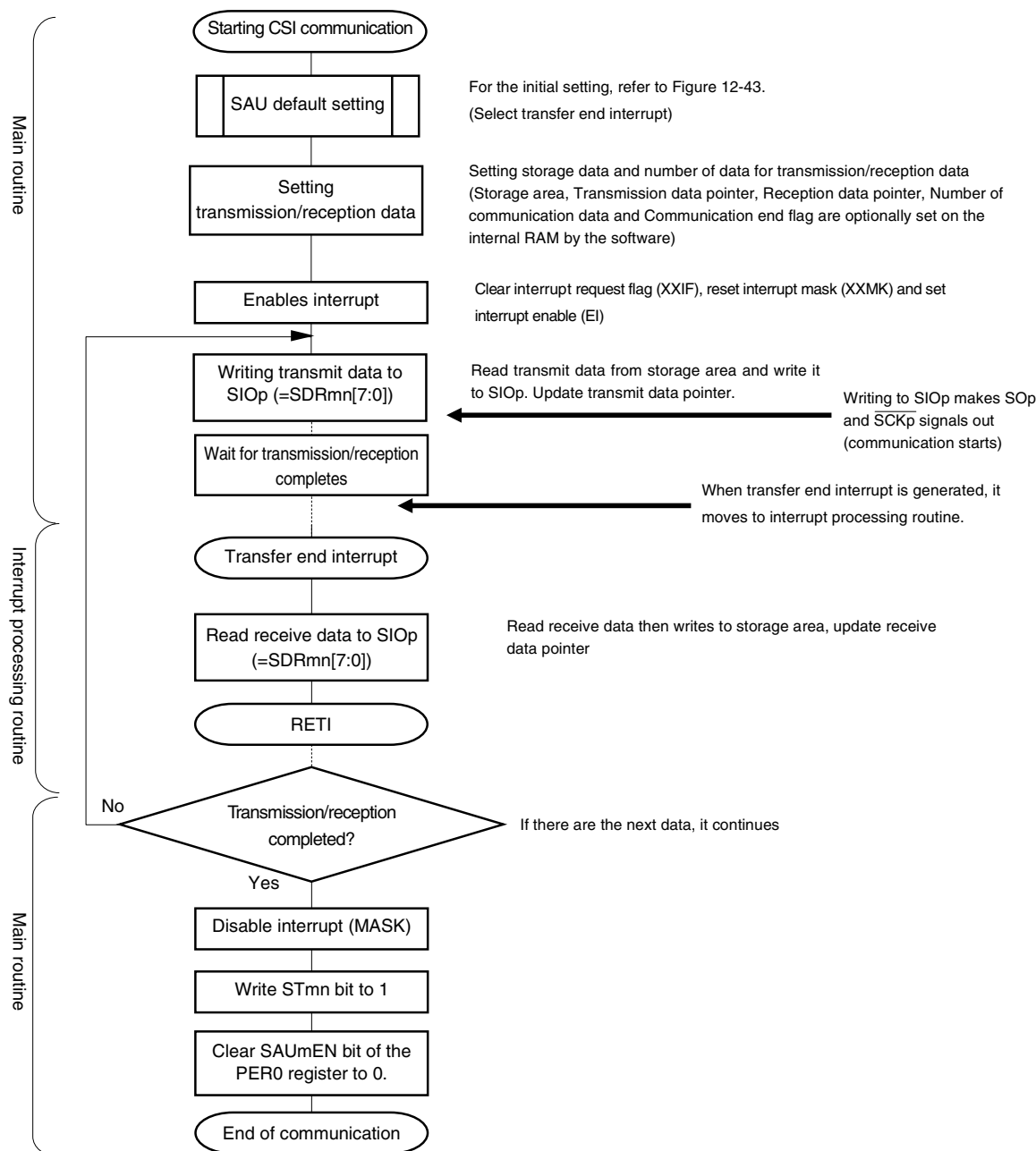
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

(3) Processing flow (in single-transmission/reception mode)

Figure 12-46. Timing Chart of Master Transmission/Reception (in Single-Transmission/Reception Mode)
 (Type 1: DAPmn = 0, CKPmn = 0)



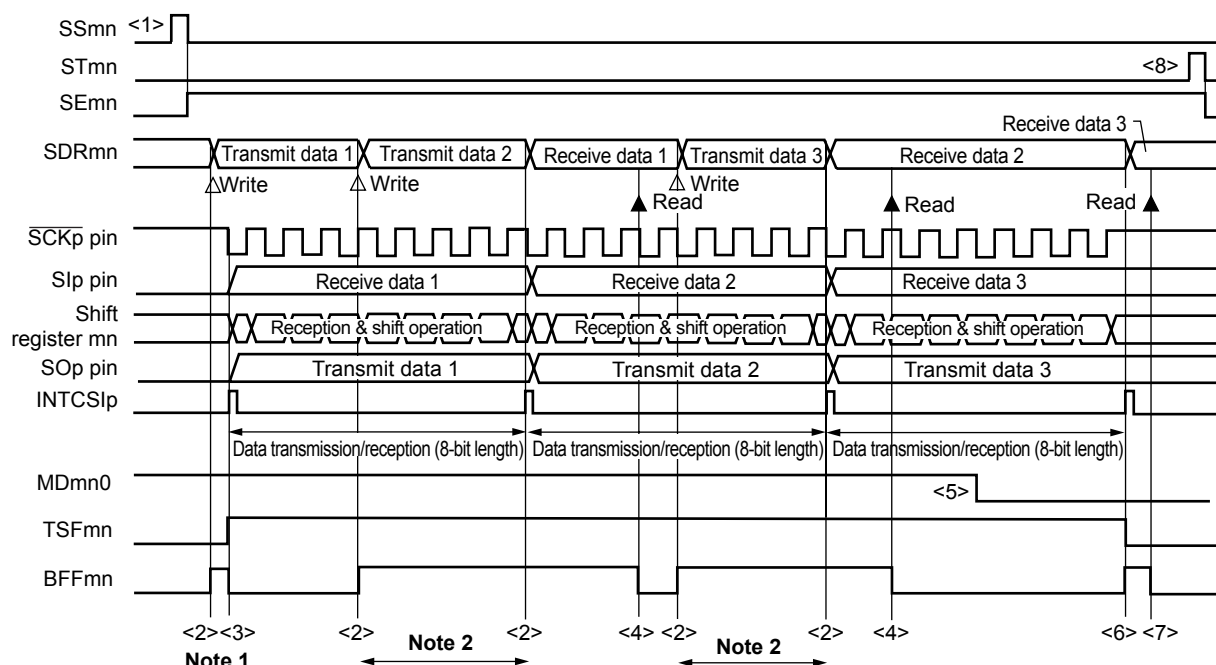
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21),
 mn = 00 to 03, 10, 11

Figure 12-47. Flowchart of Master Transmission/Reception (in Single- Transmission/Reception Mode)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

(4) Processing flow (in continuous transmission/reception mode)

Figure 12-48. Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)
 (Type 1: DAPmn = 0, CKPmn = 0)



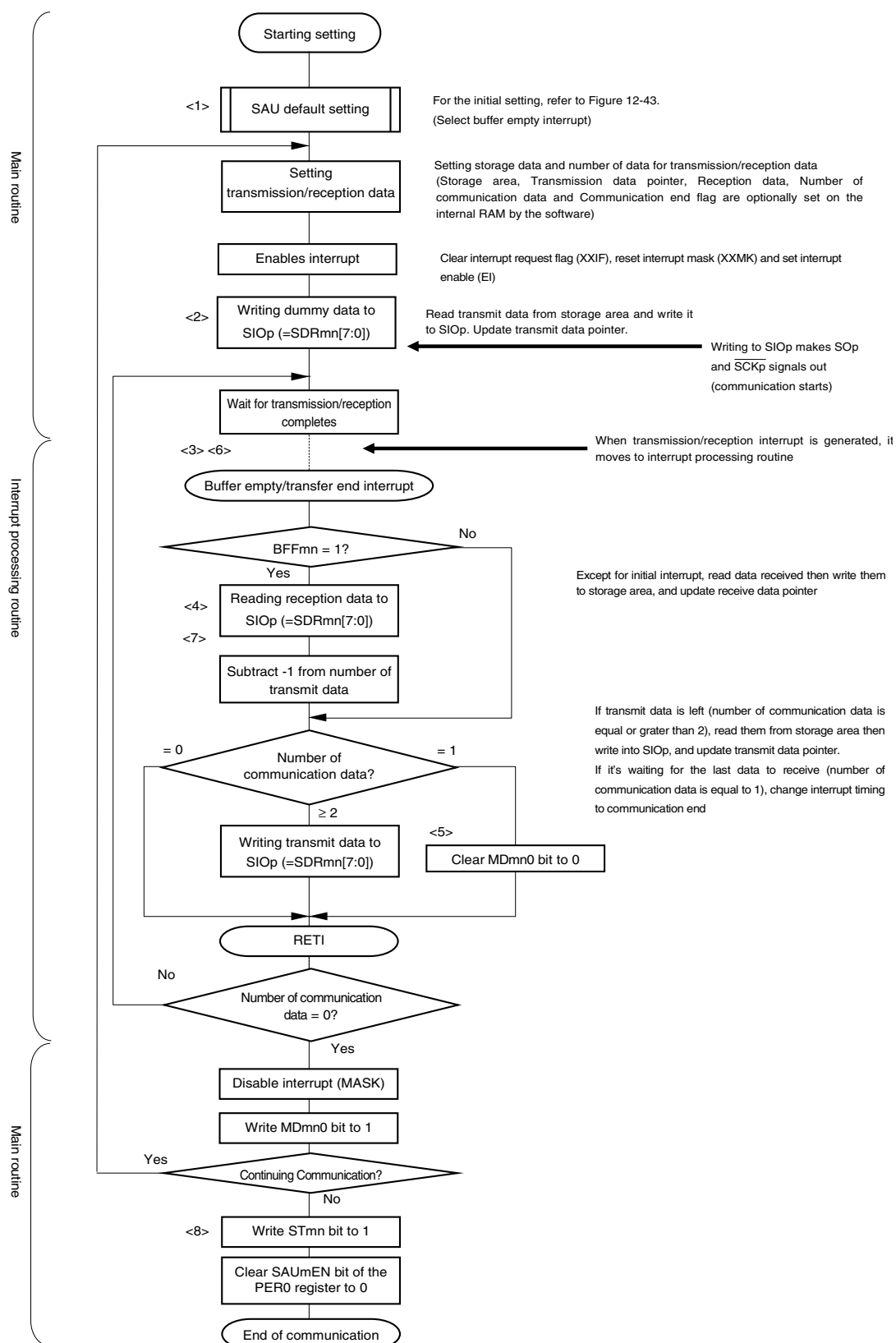
- Notes**
1. If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.
 2. The transmit data can be read by reading the SDRmn register during this period. At this time, the transfer operation is not affected.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last transmit data.

Remarks 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 12-49 Flowchart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)**.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

Figure 12-49. Flowchart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)



Remarks 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 12-48 Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)**.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

12.5.4 Slave transmission

Slave transmission is that the RL78/G1A transmits data to another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI11	CSI20	CSI21
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1	Channel 1 of SAU1
Pins used	$\overline{\text{SCK00}}$, SO00	$\overline{\text{SCK01}}$, SO01	$\overline{\text{SCK10}}$, SO10	$\overline{\text{SCK11}}$, SO11	$\overline{\text{SCK20}}$, SO20	$\overline{\text{SCK21}}$, SO21
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI11	INTCSI20	INTCSI21
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. $f_{\text{MCK}}/6$ [Hz] ^{Notes 1, 2}					
Data phase	Selectable by the DAPmn bit of the SCRMn register • DAPmn = 0: Data output starts from the start of the operation of the serial clock. • DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRMn register • CKPmn = 0: Forward • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Notes 1. Because the external serial clock input to the $\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK10}}$, $\overline{\text{SCK11}}$, $\overline{\text{SCK20}}$, and $\overline{\text{SCK21}}$ pins is sampled internally and used, the fastest transfer rate is $f_{\text{MCK}}/6$ [Hz].

2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristic in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = -40 to +105°C) (TARGET)**).

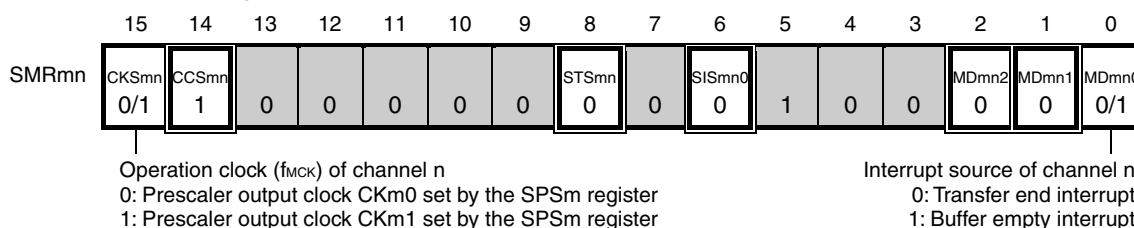
Remarks 1. f_{MCK} : Operation clock frequency of target channel

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

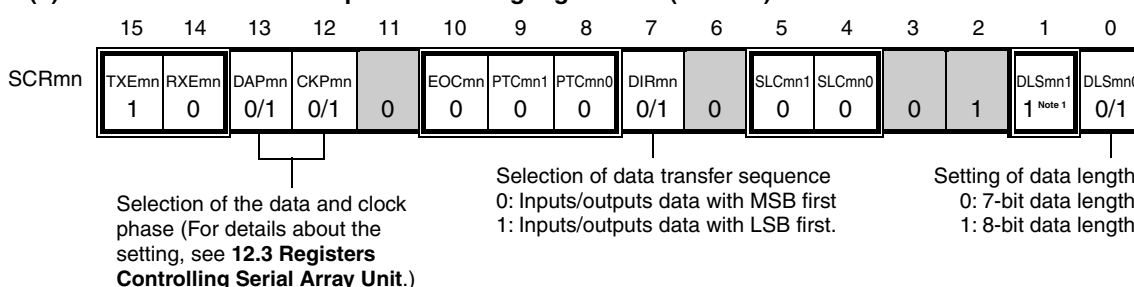
(1) Register setting

Figure 12-50. Example of Contents of Registers for Slave Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) (1/2)

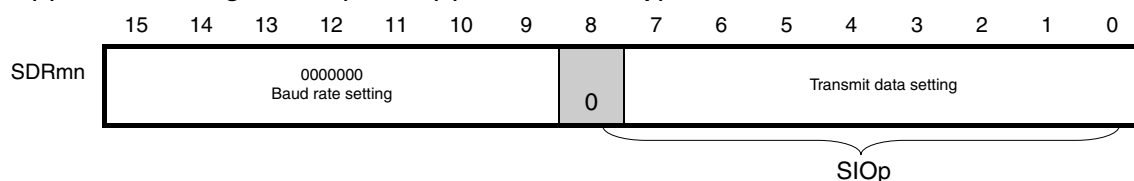
(a) Serial mode register mn (SMRmn)



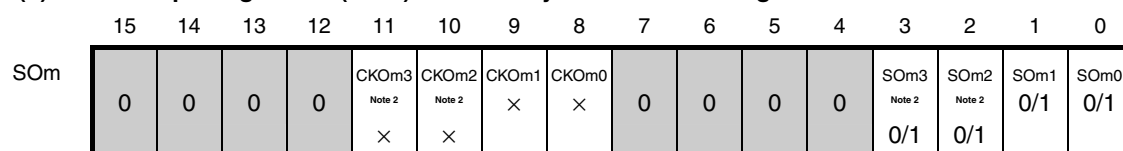
(b) Serial communication operation setting register mn (SCRmn)



(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOM) ... Sets only the bits of the target channel.



Notes 1. Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.

2. Unit 0 only

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

2. : Setting is fixed in the CSI slave transmission mode, : Setting disabled (set to the initial value)
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
 0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-50. Example of Contents of Registers for Slave Transmission of 3-Wire Serial I/O
(CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) (2/2)**

(e) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOEm3 Note 0/1	SOEm2 Note 0/1	SOEm1 0/1	SOEm0 0/1

(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.

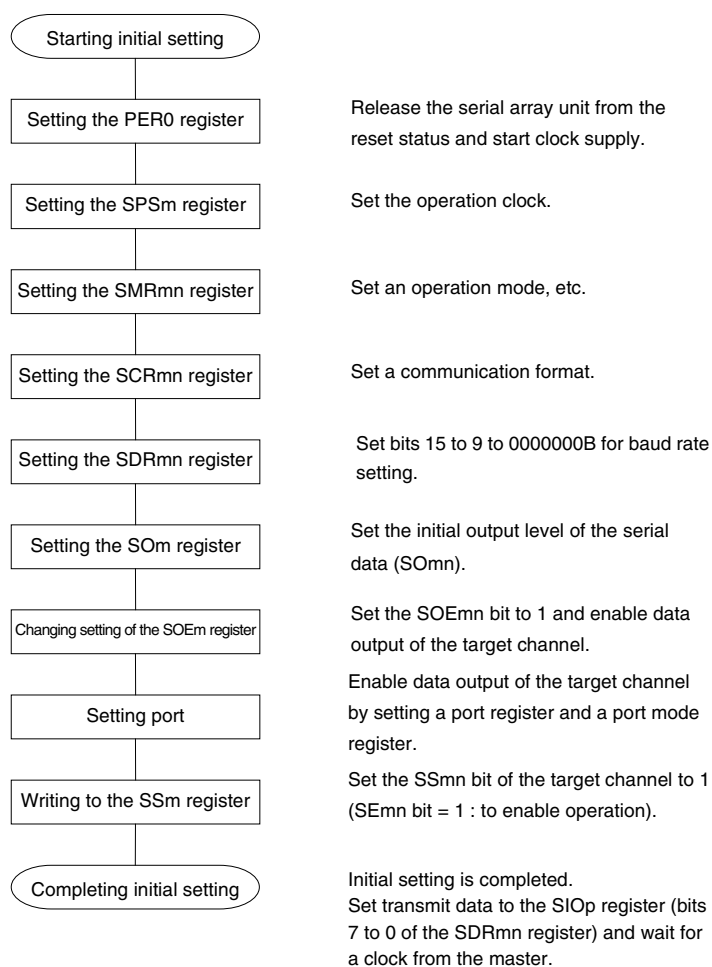
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 0/1	SSm2 Note 0/1	SSm1 0/1	SSm0 0/1

Note Unit 0 only

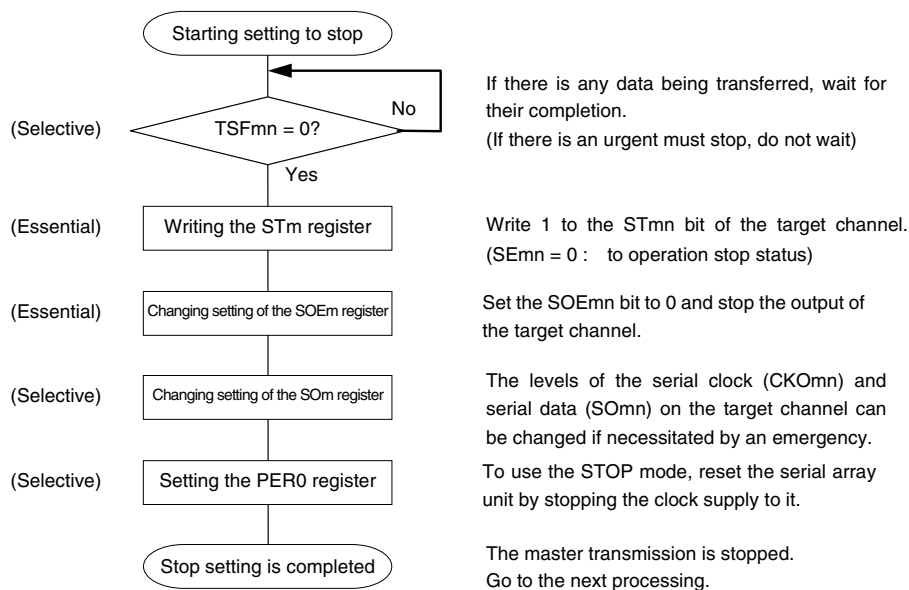
- Remarks**
1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11
 2. : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 12-51. Initial Setting Procedure for Slave Transmission

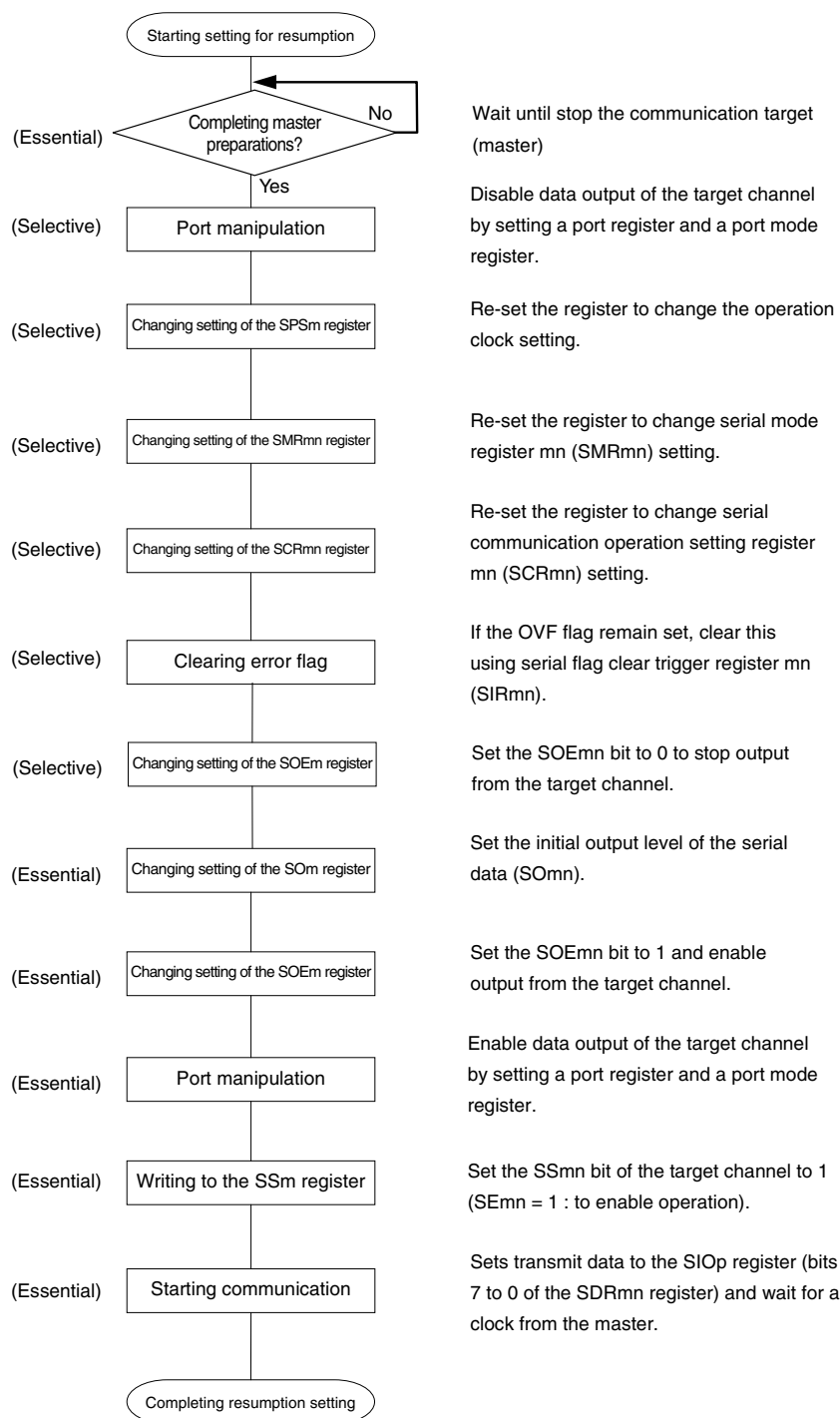


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Figure 12-52. Procedure for Stopping Slave Transmission

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

<R>

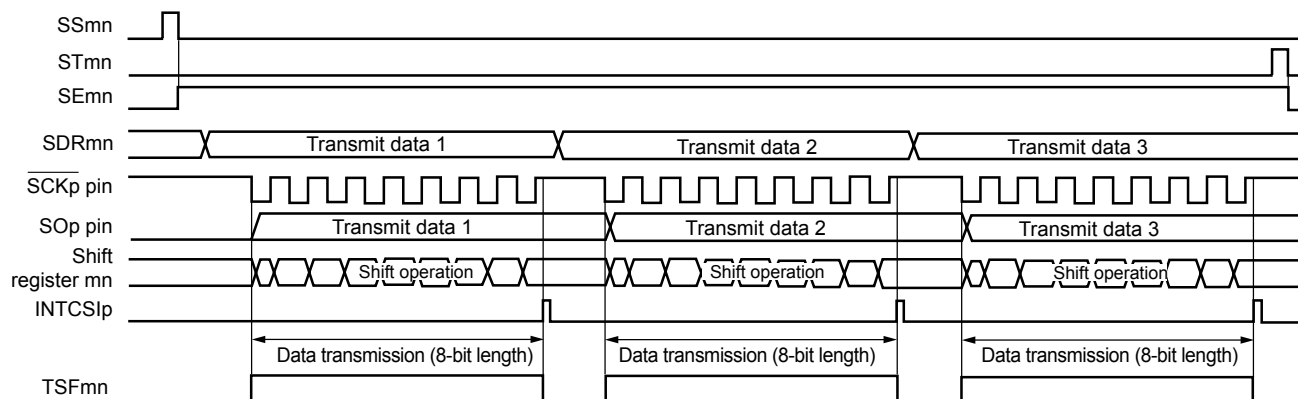
Figure 12-53. Procedure for Resuming Slave Transmission

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

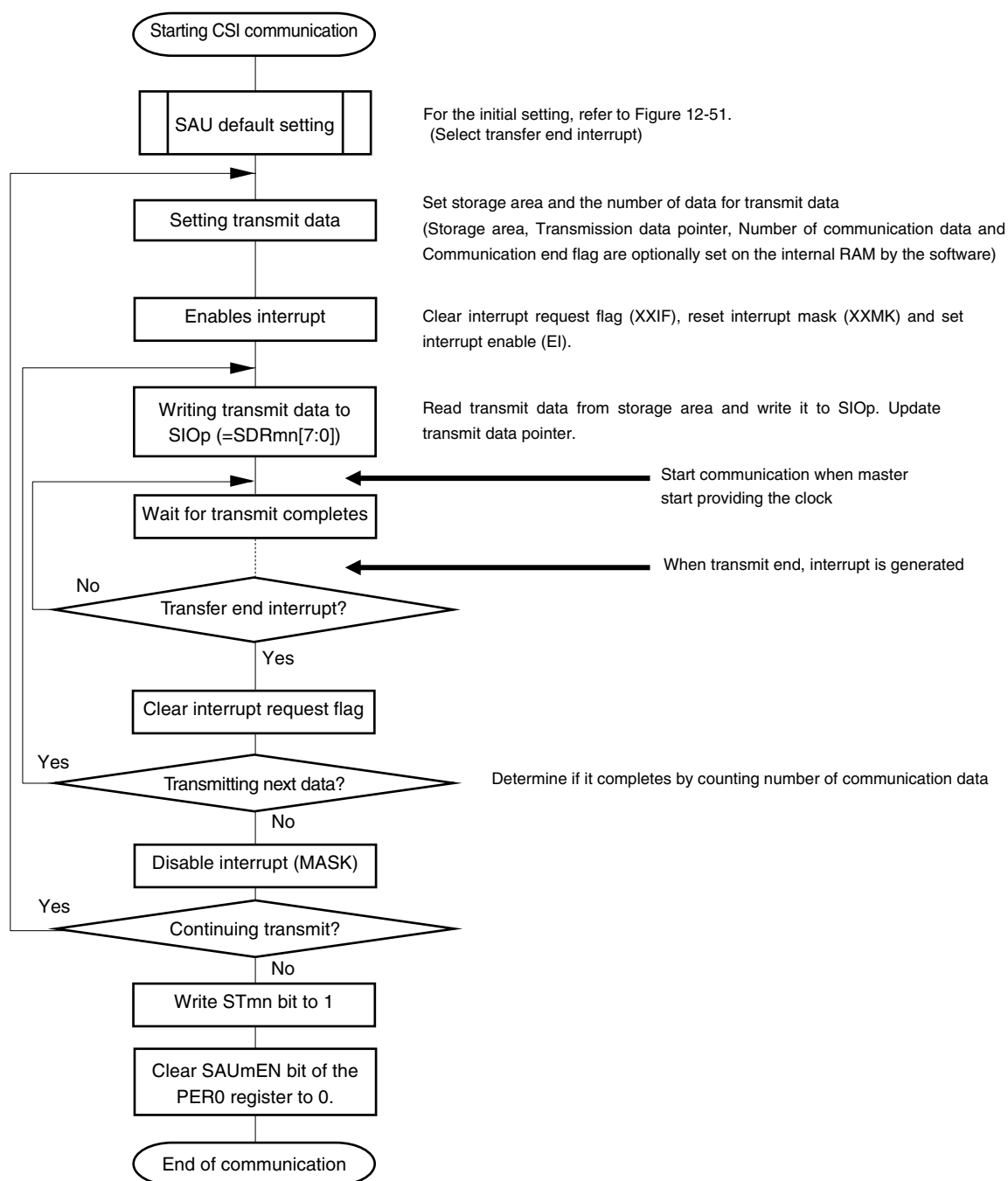
(3) Processing flow (in single-transmission mode)

Figure 12-54. Timing Chart of Slave Transmission (in Single-Transmission Mode)

(Type 1: DAPmn = 0, CKPmn = 0)



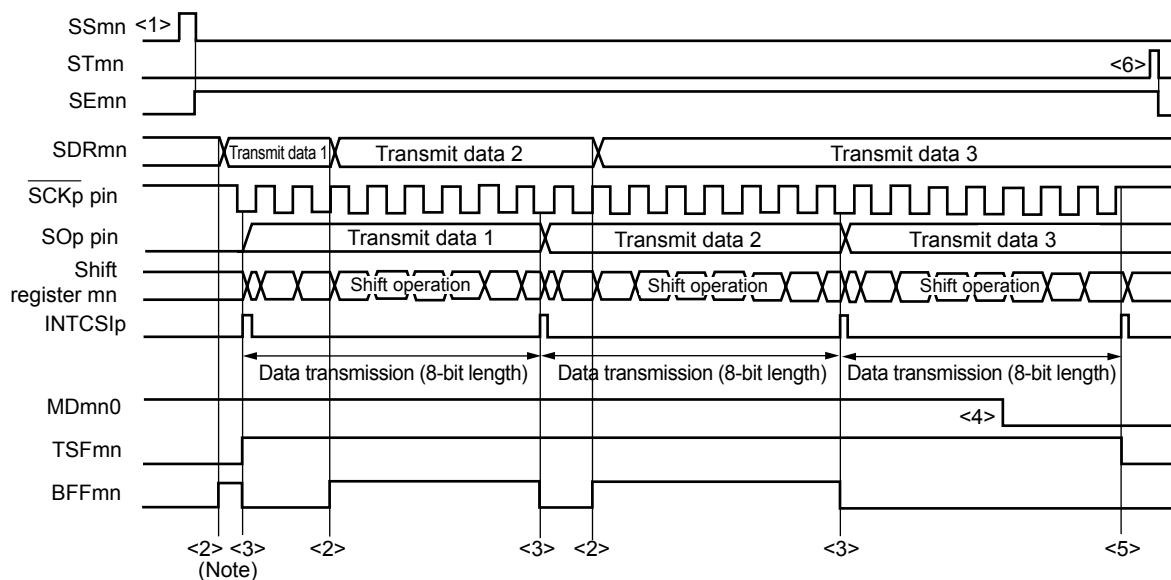
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

Figure 12-55. Flowchart of Slave Transmission (in Single-Transmission Mode)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

(4) Processing flow (in continuous transmission mode)

Figure 12-56. Timing Chart of Slave Transmission (in Continuous Transmission Mode)
 (Type 1: DAPmn = 0, CKPmn = 0)

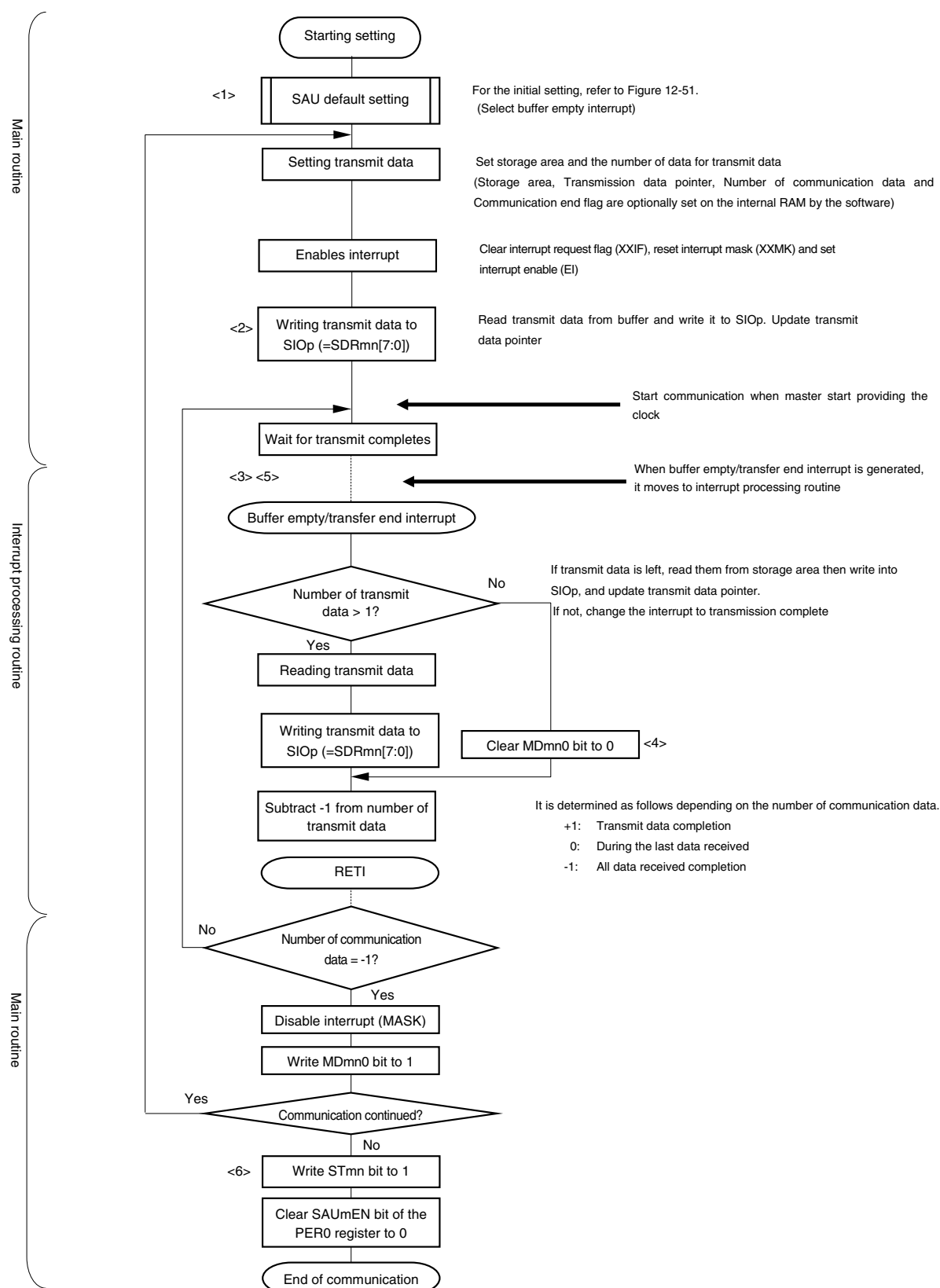


Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

Figure 12-57. Flowchart of Slave Transmission (in Continuous Transmission Mode)



Remarks 1. <1> to <6> in the figure correspond to <1> to <6> in Figure 12-56 Timing Chart of Slave Transmission (in Continuous Transmission Mode).

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

12.5.5 Slave reception

Slave reception is that the RL78/G1A receives data from another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI11	CSI20	CSI21
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1	Channel 1 of SAU1
Pins used	$\overline{\text{SCK00}}$, SI00	$\overline{\text{SCK01}}$, SI01	$\overline{\text{SCK10}}$, SI10	$\overline{\text{SCK11}}$, SI11	$\overline{\text{SCK20}}$, SI20	$\overline{\text{SCK21}}$, SI21
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI11	INTCSI20	INTCSI21
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. $f_{\text{MCK}}/6$ [Hz] ^{Notes 1, 2}					
Data phase	Selectable by the DAPmn bit of the SCRMn register • DAPmn = 0: Data input starts from the start of the operation of the serial clock. • DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRMn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Notes 1. Because the external serial clock input to the $\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK10}}$, $\overline{\text{SCK11}}$, $\overline{\text{SCK20}}$, and $\overline{\text{SCK21}}$ pins is sampled internally and used, the fastest transfer rate is $f_{\text{MCK}}/6$ [Hz].

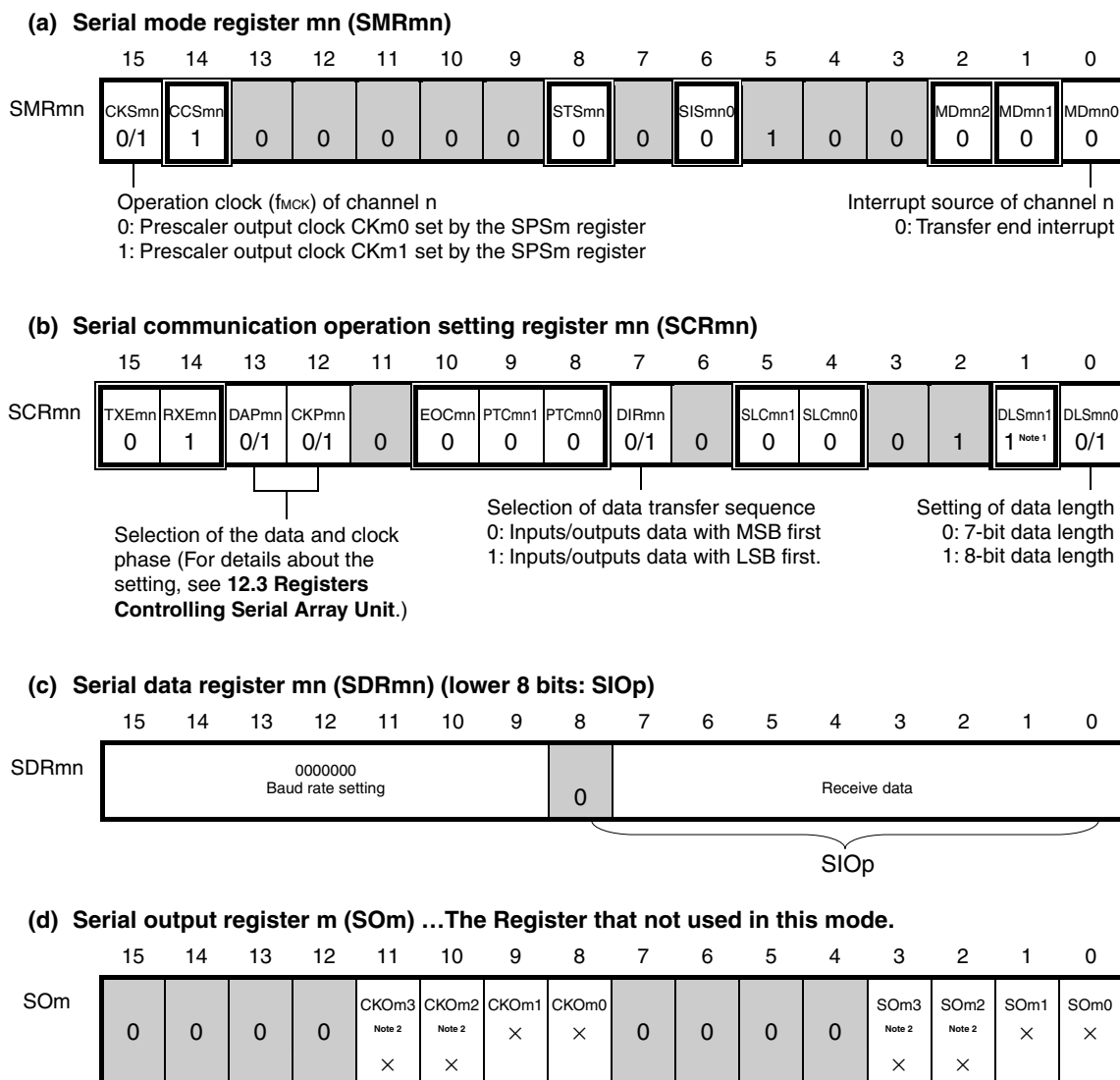
2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristic in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = -40 to +105°C) (TARGET)**).

Remarks 1. f_{MCK} : Operation clock frequency of target channel

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

(1) Register setting

**Figure 12-58. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O
(CSI00, CSI01, CSI10, CSI11, CSI20, CSI21)**



Notes 1. Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.

2. Unit 0 only

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),

p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

2. : Setting is fixed in the CSI slave transmission mode, : Setting disabled (set to the initial value)
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
 0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-58. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O
(CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) (2/2)**

(e) Serial output enable register m (SOEm) ...The Register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOEm3 Note ×	SOEm2 Note ×	SOEm1 ×	SOEm0 ×

(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.

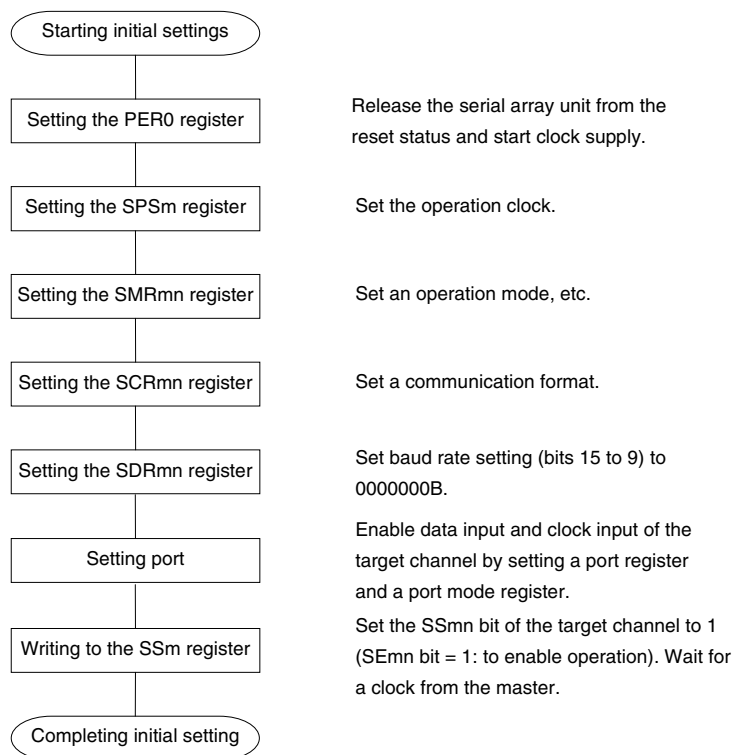
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 0/1	SSm2 Note 0/1	SSm1 0/1	SSm0 0/1

Note Unit 0 only

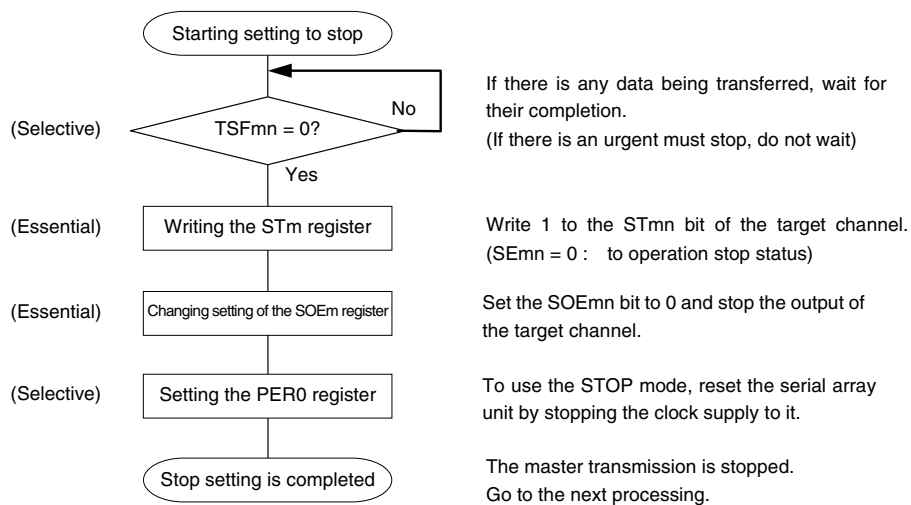
- Remarks** 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21),
mn = 00 to 03, 10, 11
2. : Setting disabled (set to the initial value)
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
 0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 12-59. Initial Setting Procedure for Slave Reception

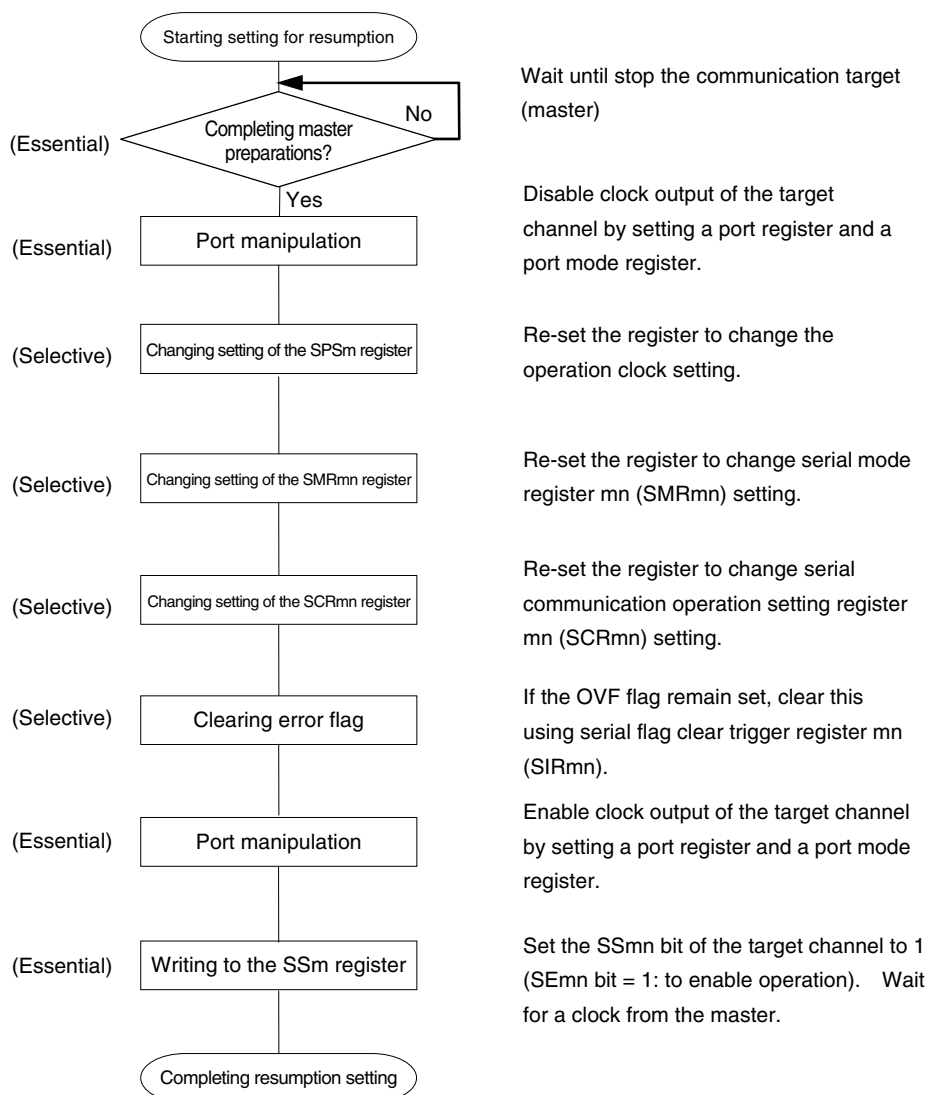


<R>

Figure 12-60. Procedure for Stopping Slave Reception

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

<R>

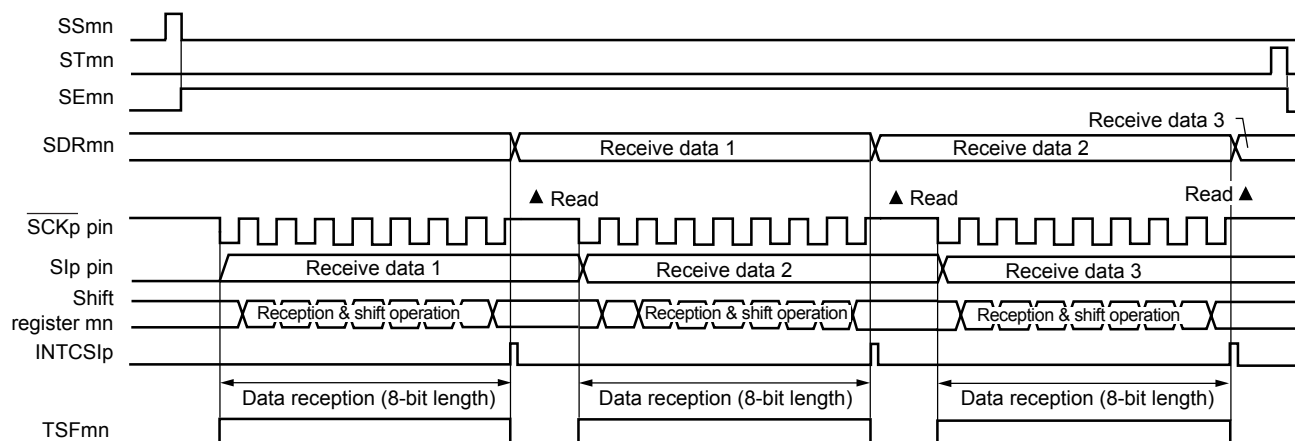
Figure 12-61. Procedure for Resuming Slave Reception

- Remarks 1.** If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.
- 2.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

(3) Processing flow (in single-reception mode)

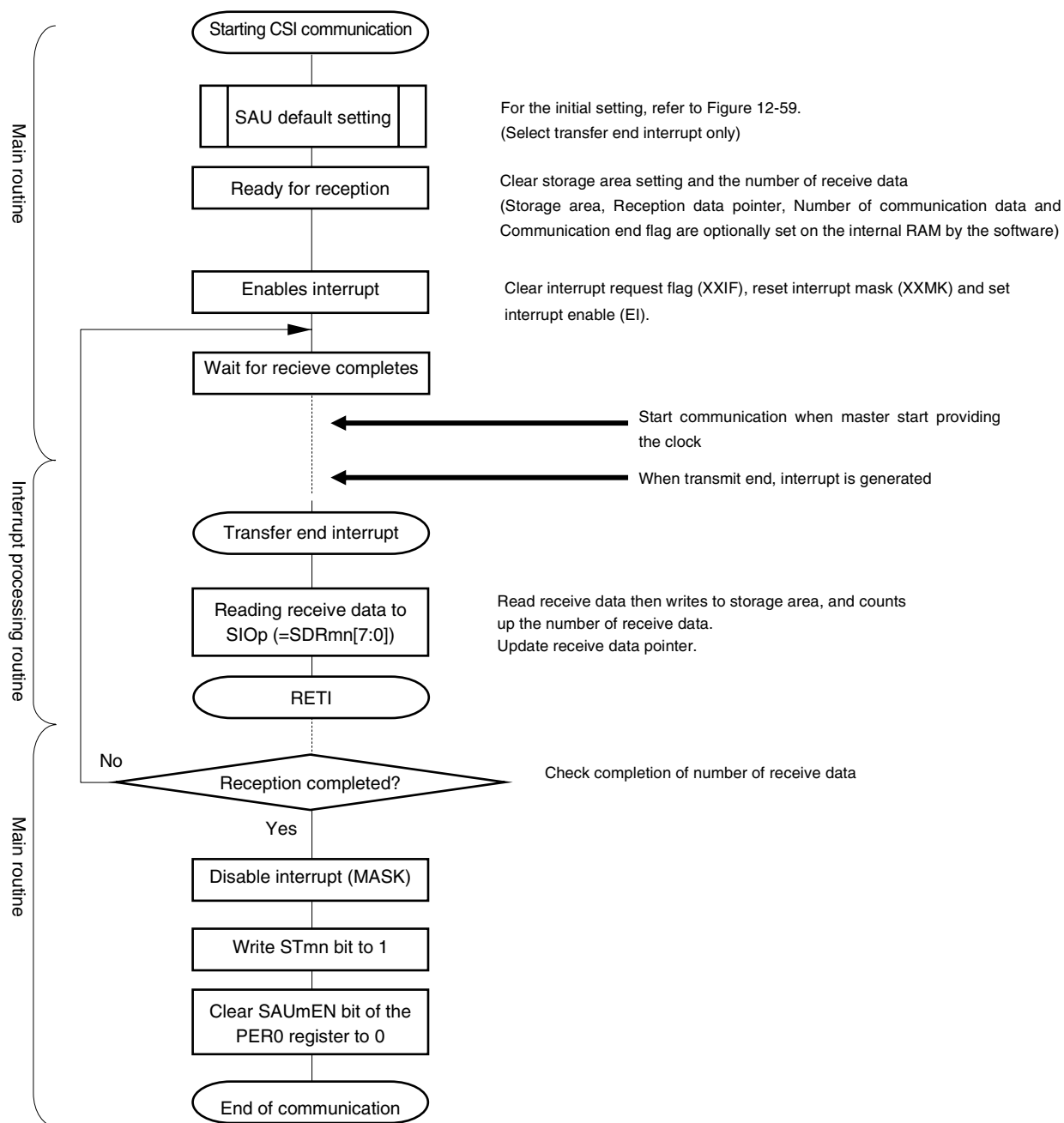
Figure 12-62. Timing Chart of Slave Reception (in Single-Reception Mode)

(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21),
mn = 00 to 03, 10, 11

Figure 12-63. Flowchart of Slave Reception (in Single-Reception Mode)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

12.5.6 Slave transmission/reception

Slave transmission/reception is that the RL78/G1A transmits/receives data to/from another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI11	CSI20	CSI21
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1	Channel 1 of SAU1
Pins used	$\overline{\text{SCK00}}$, SI00, SO00	$\overline{\text{SCK01}}$, SI01, SO01	$\overline{\text{SCK10}}$, SI10, SO10	$\overline{\text{SCK11}}$, SI11, SO11	$\overline{\text{SCK20}}$, SI20, SO20	$\overline{\text{SCK21}}$, SI21, SO21
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI11	INTCSI20	INTCSI21
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. $f_{\text{MCK}}/6$ [Hz] ^{Notes 1, 2}					
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data I/O starts from the start of the operation of the serial clock. • DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

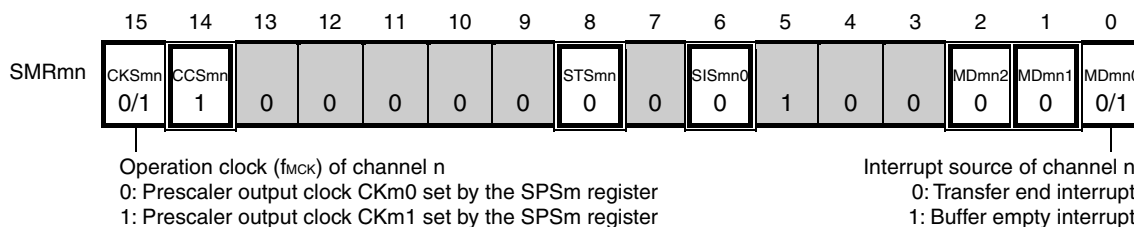
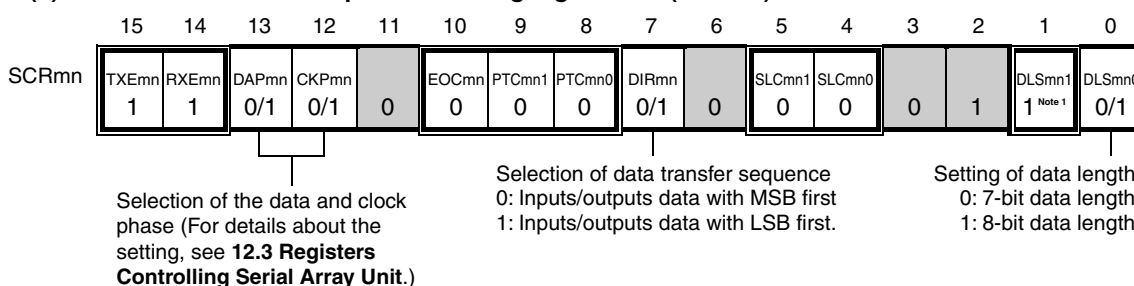
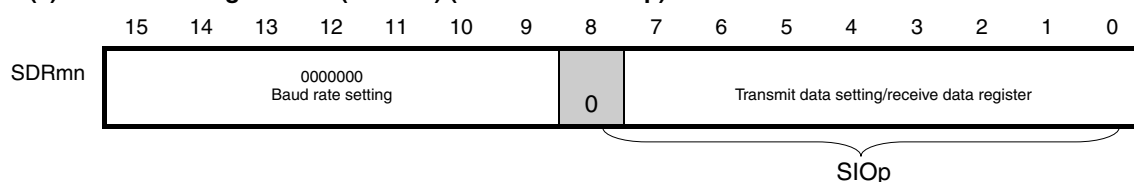
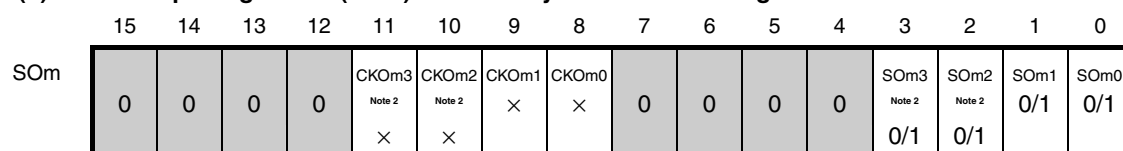
Notes 1. Because the external serial clock input to the $\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK10}}$, $\overline{\text{SCK11}}$, $\overline{\text{SCK20}}$, and $\overline{\text{SCK21}}$ pins is sampled internally and used, the fastest transfer rate is $f_{\text{MCK}}/6$ [Hz].

2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristic in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = -40 to +105°C) (TARGET)**).

Remarks 1. f_{MCK} : Operation clock frequency of target channel

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

(1) Register setting

Figure 12-64. Example of Contents of Registers for Slave Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) (1/2)**(a) Serial mode register mn (SMRmn)****(b) Serial communication operation setting register mn (SCRmn)****(c) Serial data register mn (SDRmn) (lower 8 bits: SIOP)****(d) Serial output register m (SOM) ... Sets only the bits of the target channel.****Notes 1.** Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.**2.** Unit 0 only**Caution** Be sure to set transmit data to the SIOP register before the clock from the master is started.**Remarks 1.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11**2.**

: Setting is fixed in the CSI slave transmission/reception mode,

: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

Figure 12-64. Example of Contents of Registers for Slave Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, CSI30, CSI31) (2/2)

(e) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOEm3 Note 0/1	SOEm2 Note 0/1	SOEm1 0/1	SOEm0 0/1

(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.

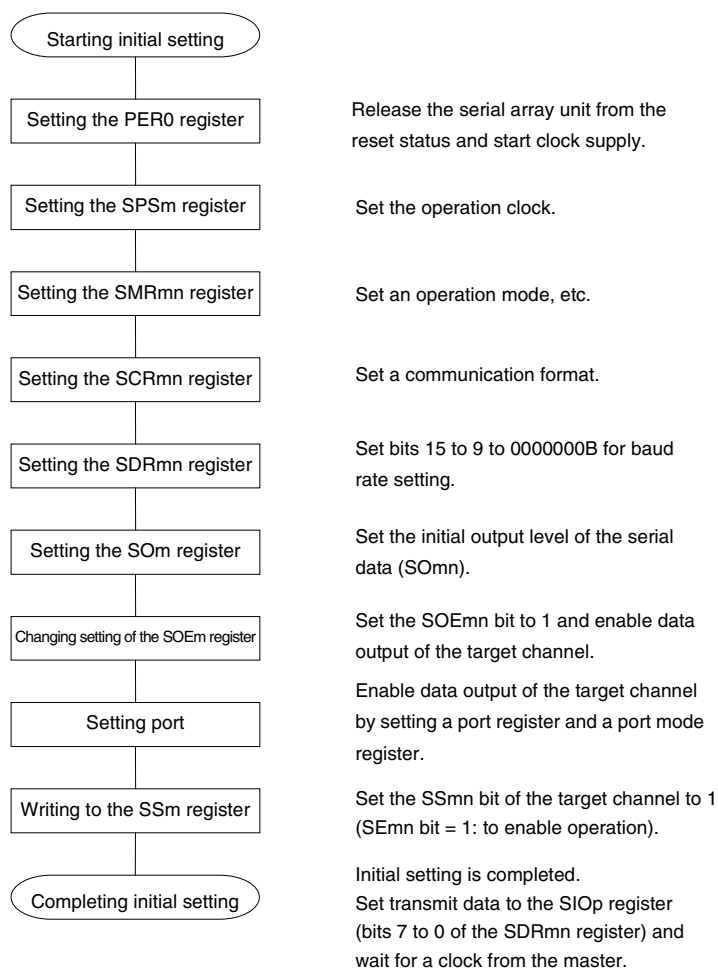
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 0/1	SSm2 Note 0/1	SSm1 0/1	SSm0 0/1

Note Unit 0 only

- Remarks**
1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11
 2.  : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

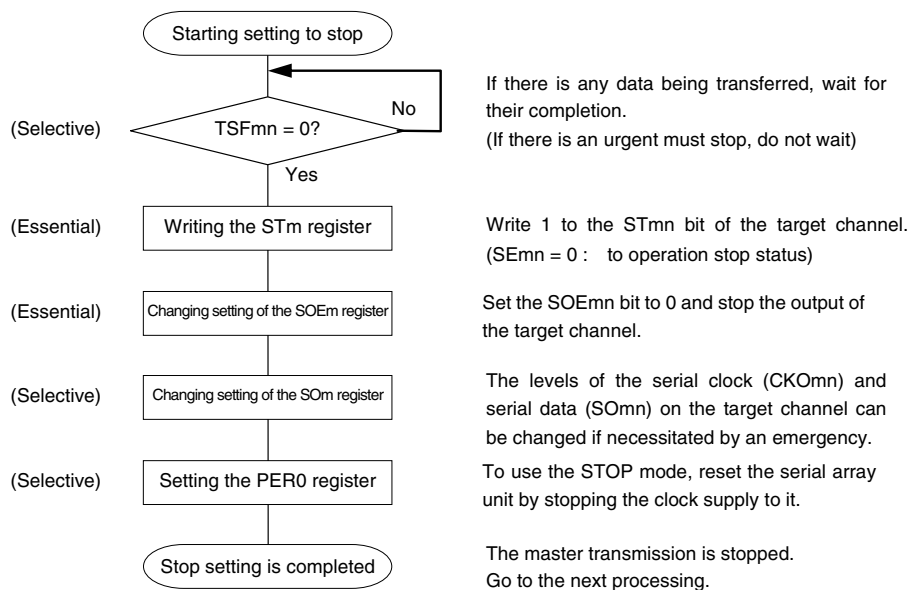
(2) Operation procedure

Figure 12-65. Initial Setting Procedure for Slave Transmission/Reception



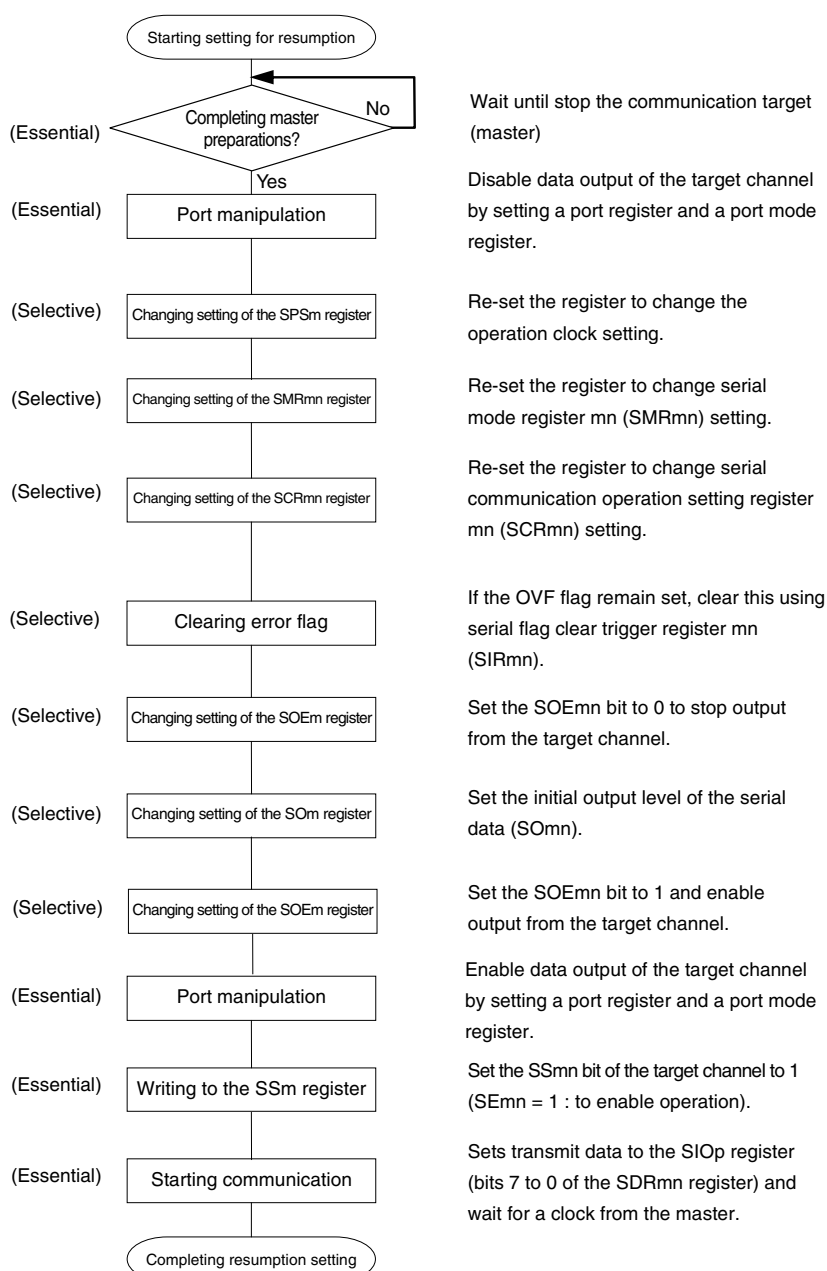
Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

Figure 12-66. Procedure for Stopping Slave Transmission/Reception

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

<R>

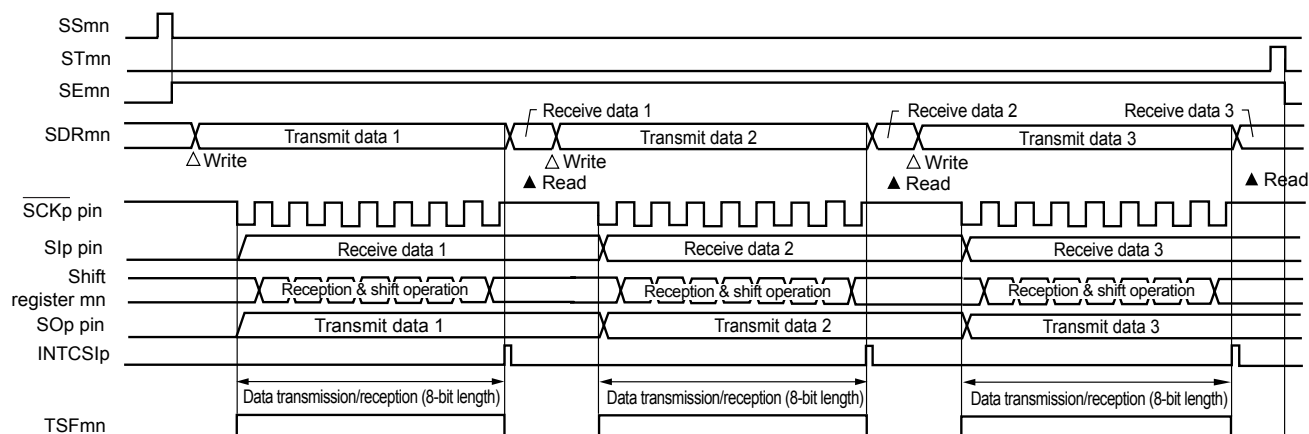
Figure 12-67. Procedure for Resuming Slave Transmission/Reception

- Cautions**
1. Be sure to set transmit data to the SIOp register before the clock from the master is started.
 2. If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

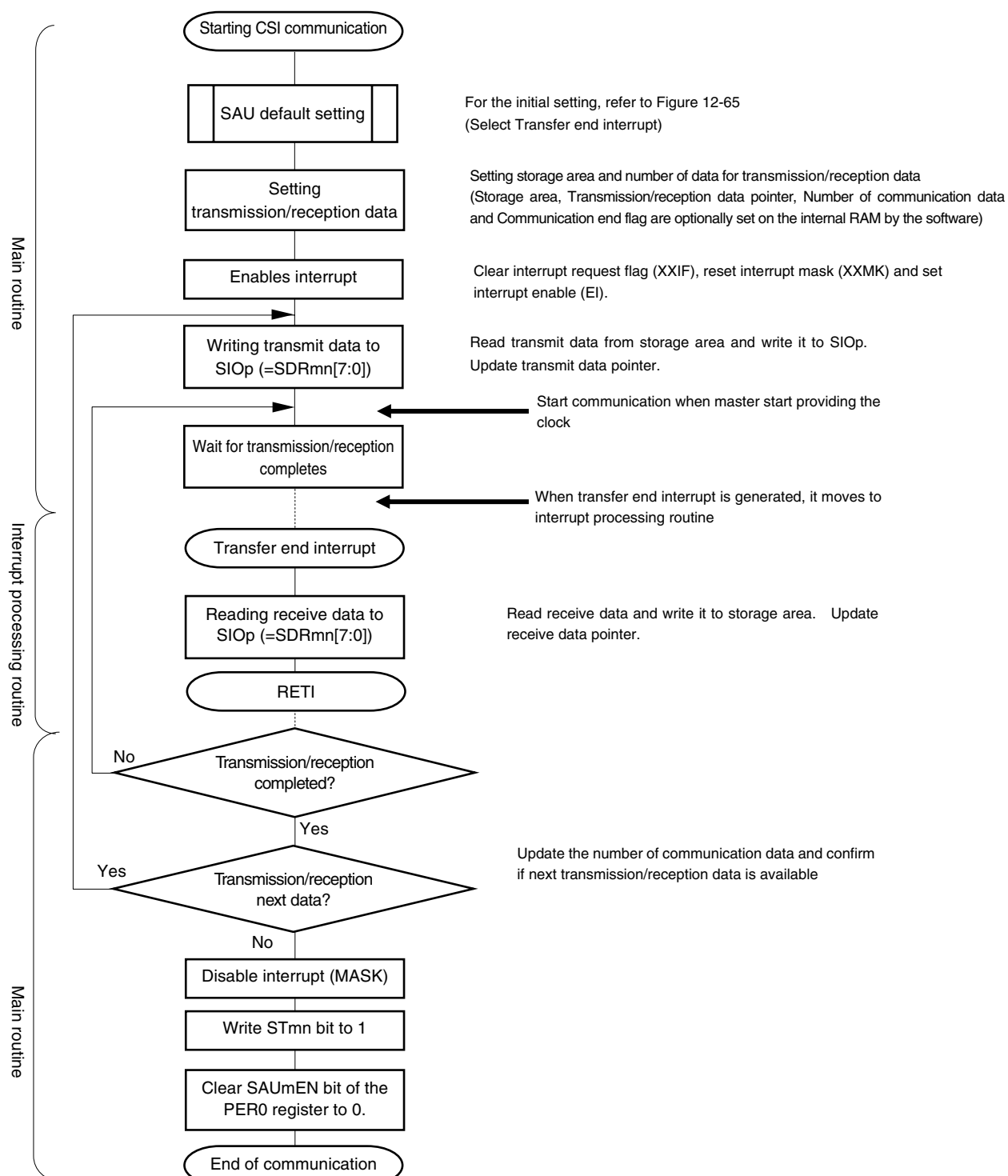
(3) Processing flow (in single-transmission/reception mode)

Figure 12-68. Timing Chart of Slave Transmission/Reception (in Single-Transmission/Reception Mode)
 (Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21),
 mn = 00 to 03, 10, 11

Figure 12-69. Flowchart of Slave Transmission/Reception (in Single- Transmission/Reception Mode)

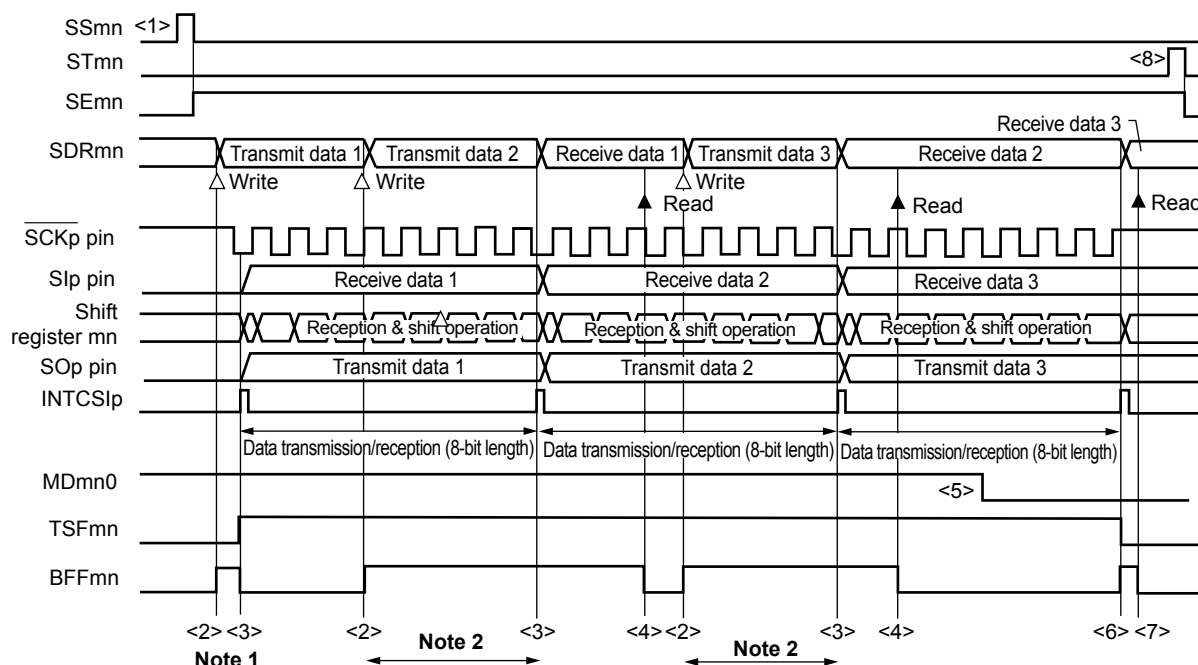


Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

(4) Processing flow (in continuous transmission/reception mode)

Figure 12-70. Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)
(Type 1: DAPmn = 0, CKPmn = 0)

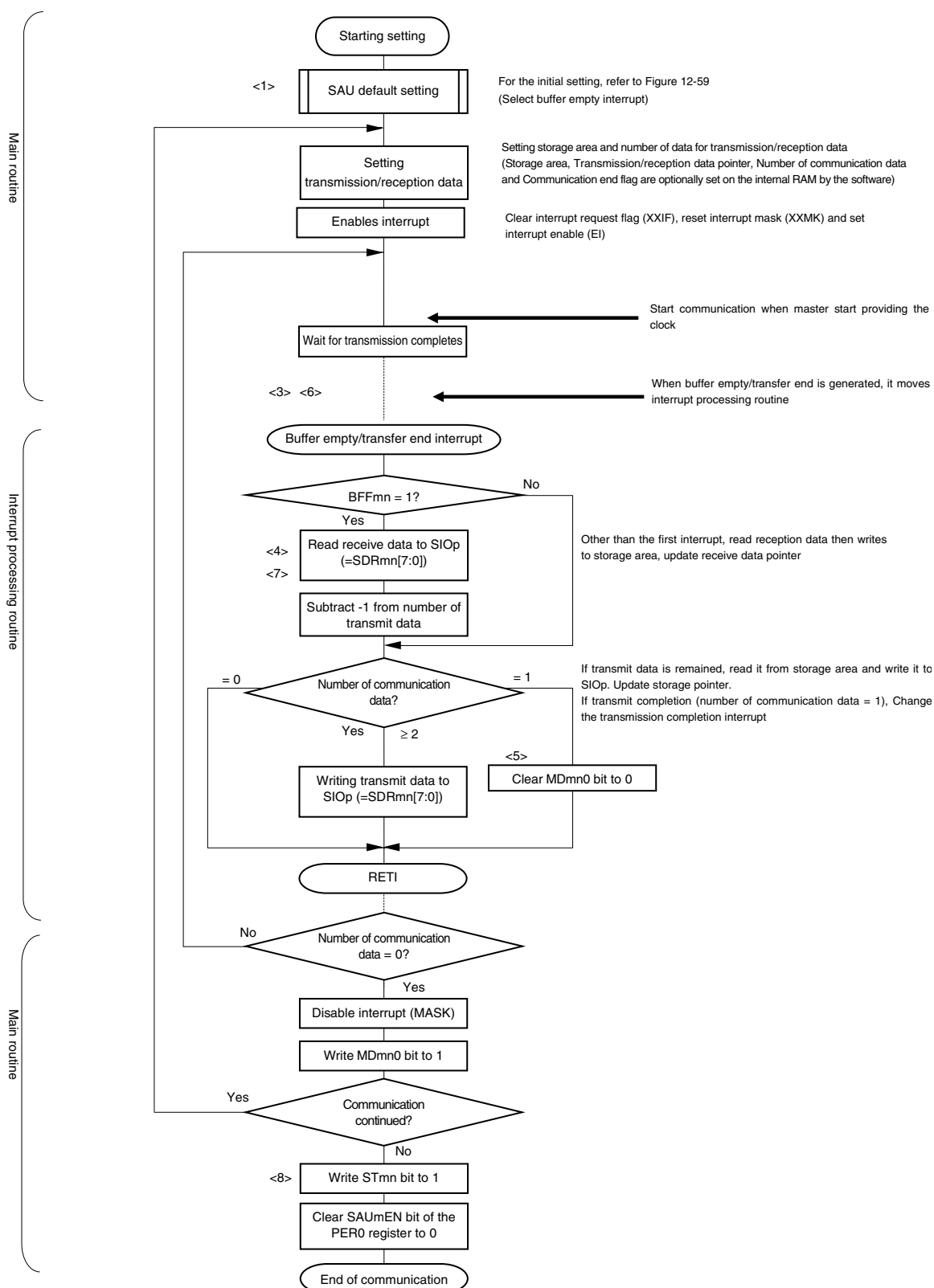


- Notes**
1. If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.
 2. The transmit data can be read by reading the SDRmn register during this period. At this time, the transfer operation is not affected.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last transmit data.

- Remarks**
1. <1> to <8> in the figure correspond to <1> to <8> in Figure 12-71 Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode).
 2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

Figure 12-71. Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)



Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

Remarks 1. <1> to <8> in the figure correspond to <1> to <8> in Figure 12-70 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode).

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

12.5.7 SNOOZE mode function

<R> SNOOZE mode makes CSI operate reception by $\overline{\text{SCKp}}$ pin input detection while the STOP mode. Normally CSI stops communication in the STOP mode. But, using the SNOOZE mode makes reception CSI operate unless the CPU operation by detecting $\overline{\text{SCKp}}$ pin input. Only CSIs00 can be specified for asynchronous reception.

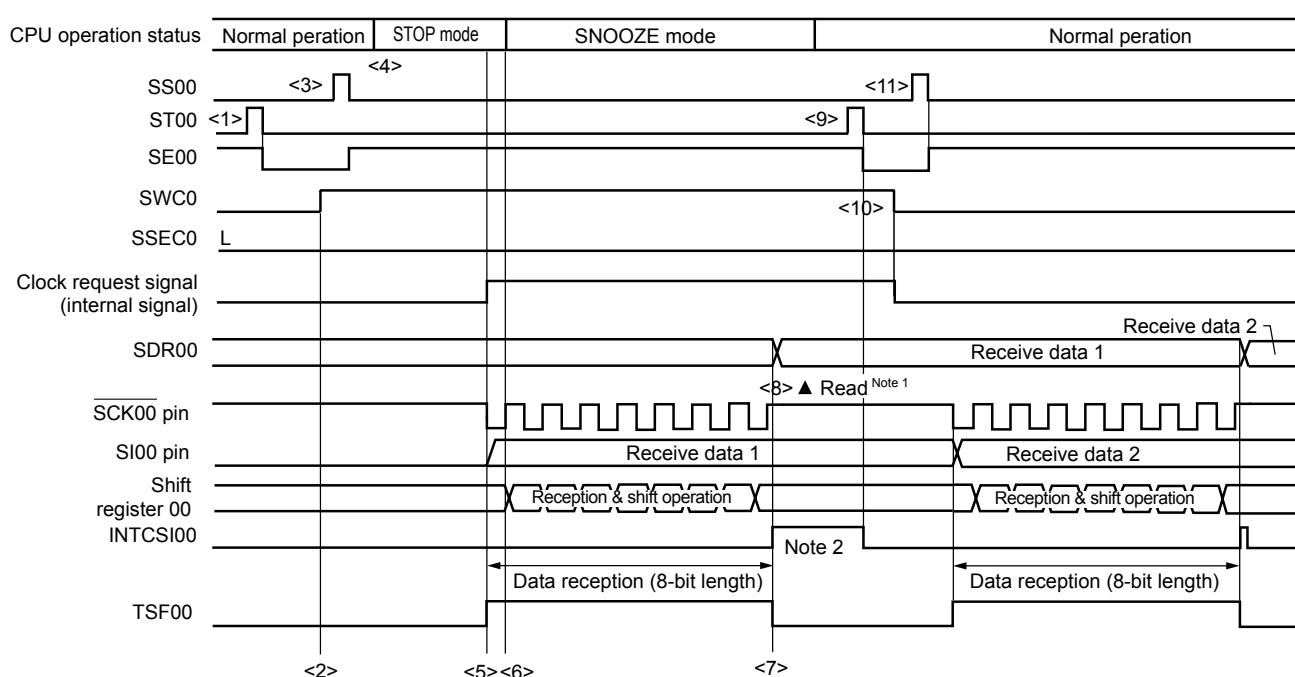
When using the SNOOZE mode function, set the SWCm bit of serial standby control register m (SSCm) to 1 before switching to the STOP mode.

Cautions 1. The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for fCLK.

2. The maximum transfer rate when using CSIp in the SNOOZE mode is 1 Mbps.

(1) SNOOZE mode operation (once startup)

Figure 12-72. Timing Chart of SNOOZE Mode Operation (once startup) (Type 1: DAPmn = 0, CKPmn = 0)



Notes 1. Only read received data while SWCm = 1 and before the next edge of the $\overline{\text{SCKp}}$ pin input is detected.

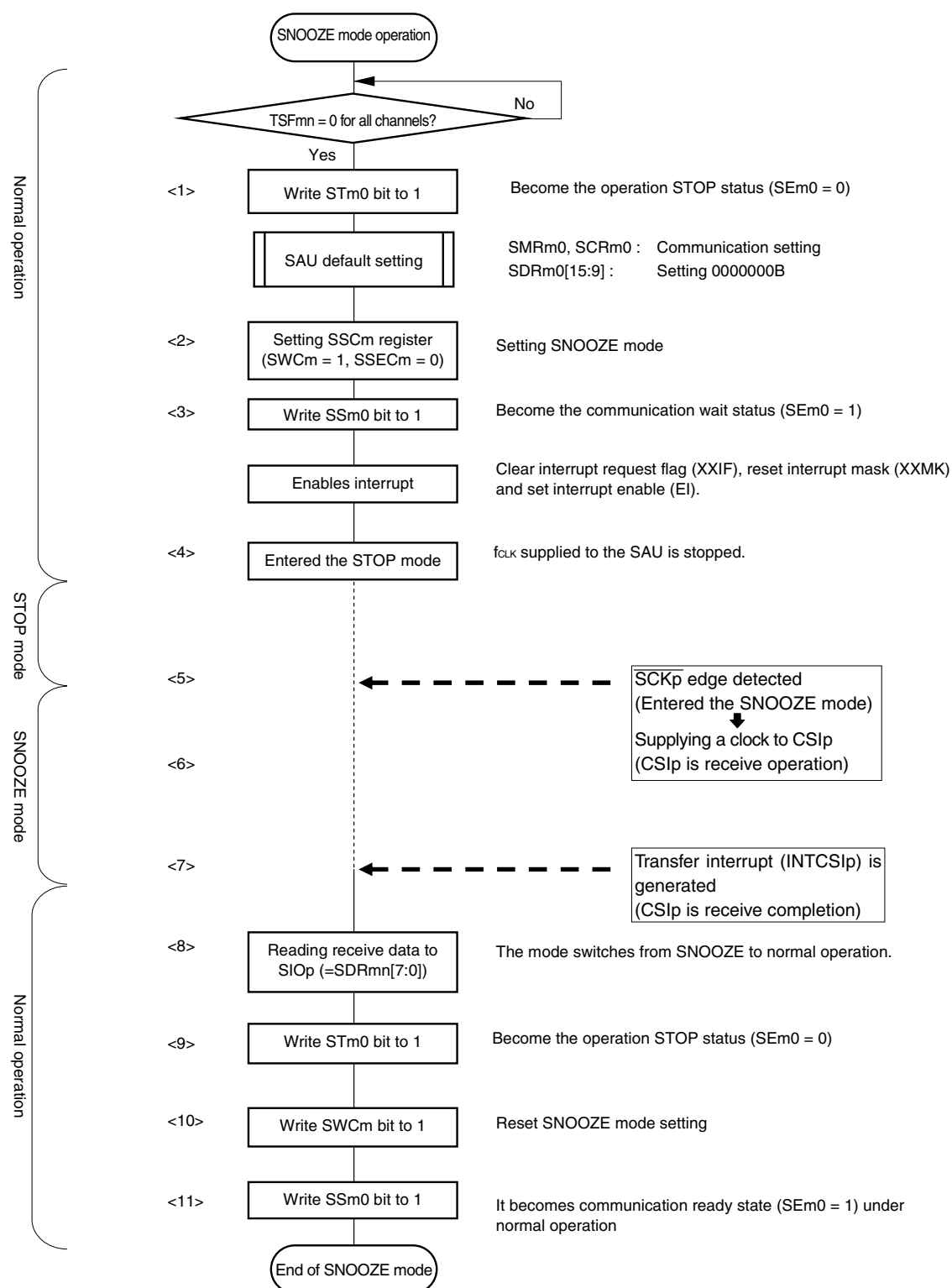
2. The transfer end interrupt (INTCSIp) is cleared either when SWCm is cleared to 0 or when the next edge of the $\overline{\text{SCKp}}$ pin input is detected.

<R> **Caution** Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm0 bit to 1 (clear the SEm0 bit, and stop the operation). And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE mode release).

Remarks 1. <1> to <11> in the figure correspond to <1> to <11> in Figure 12-73. Flowchart of SNOOZE Mode Operation (once startup).

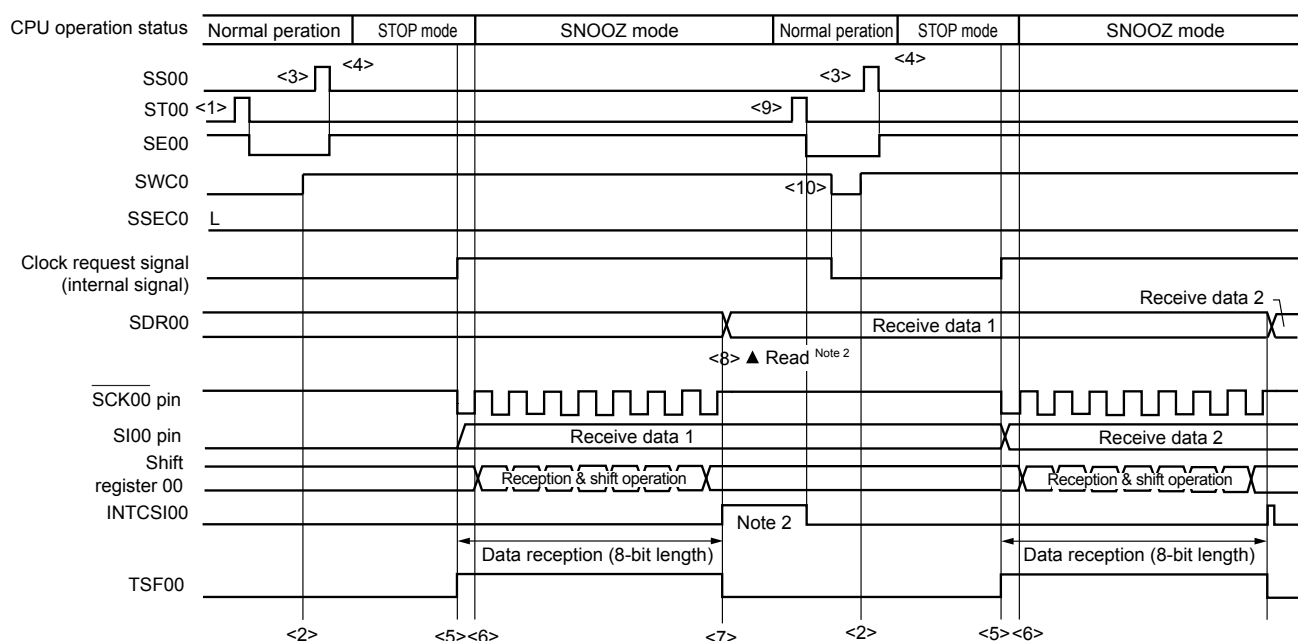
2. m = 0; p = 00

Figure 12-73. Flowchart of SNOOZE Mode Operation (once startup)



(2) SNOOZE mode operation (continuous startup)

Figure 12-74. Timing Chart of SNOOZE Mode Operation (continuous startup) (Type 1: DAPmn = 0, CKPmn = 0)

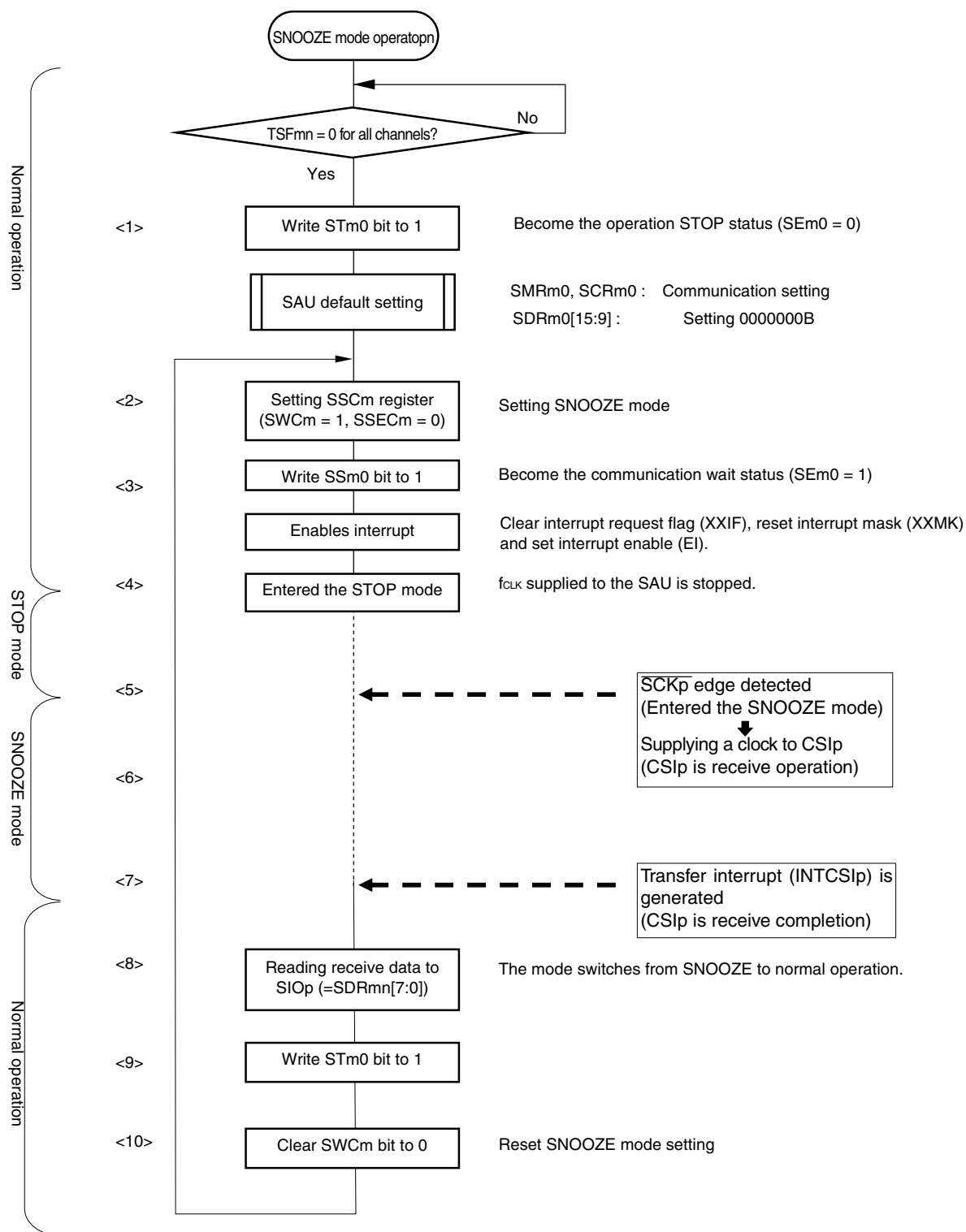


- Notes**
1. Only read received data while SWCm = 1 and before the next edge of the $\overline{\text{SCKp}}$ pin input is detected.
 2. The transfer end interrupt (INTCSIp) is cleared either when SWCm is cleared to 0 or when the next edge of the $\overline{\text{SCKp}}$ pin input is detected.

<R> Caution Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm0 bit to 1 (clear the SEM0 bit, and stop the operation).
And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE release).

- Remarks 1.** <1> to <10> in the figure correspond to <1> to <10> in **Figure 12-75. Flowchart of SNOOZE Mode Operation (continuous startup).**
- 2.** $m = 0$; $p = 00$

Figure 12-75. Flowchart of SNOOZE Mode Operation (continuous startup)



Remarks 1. <1> to <10> in the figure correspond to <1> to <10> in **Figure 12-74. Timing Chart of SNOOZE Mode Operation (continuous startup).**

2. m = 0; p = 00

12.5.8 Calculating transfer clock frequency

The transfer clock frequency for 3-wire serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) communication can be calculated by the following expressions.

(1) Master

$(\text{Transfer clock frequency}) = \{ \text{Operation clock (f}_{\text{MCK}}) \text{ frequency of target channel} \} \div (\text{SDRmn}[15:9] + 1) \div 2 \text{ [Hz]}$

(2) Slave

$(\text{Transfer clock frequency}) = \{ \text{Frequency of serial clock (SCK) supplied by master} \}^{\text{Note}} \text{ [Hz]}$

Note The permissible maximum transfer clock frequency is $f_{\text{MCK}}/6$.

Remark The value of SDRmn[15:9] is the value of bits 15 to 9 of serial data register mn (SDRmn) (0000000B to 1111111B) and therefore is 0 to 127.

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 12-2. Selection of Operation Clock For 3-Wire Serial I/O

SMRmn Register	SPSm Register								Operation Clock (f _{CLK}) ^{Note}	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		f _{CLK} = 32 MHz
0	X	X	X	X	0	0	0	0	f _{CLK}	32 MHz
	X	X	X	X	0	0	0	1	f _{CLK} /2	16 MHz
	X	X	X	X	0	0	1	0	f _{CLK} /2 ²	8 MHz
	X	X	X	X	0	0	1	1	f _{CLK} /2 ³	4 MHz
	X	X	X	X	0	1	0	0	f _{CLK} /2 ⁴	2 MHz
	X	X	X	X	0	1	0	1	f _{CLK} /2 ⁵	1 MHz
	X	X	X	X	0	1	1	0	f _{CLK} /2 ⁶	500 kHz
	X	X	X	X	0	1	1	1	f _{CLK} /2 ⁷	250 kHz
	X	X	X	X	1	0	0	0	f _{CLK} /2 ⁸	125 kHz
	X	X	X	X	1	0	0	1	f _{CLK} /2 ⁹	62.5 kHz
	X	X	X	X	1	0	1	0	f _{CLK} /2 ¹⁰	31.25 kHz
	X	X	X	X	1	0	1	1	f _{CLK} /2 ¹¹	15.63 kHz
	X	X	X	X	1	1	0	0	f _{CLK} /2 ¹²	7.81 kHz
	X	X	X	X	1	1	0	1	f _{CLK} /2 ¹³	3.91 kHz
	X	X	X	X	1	1	1	0	f _{CLK} /2 ¹⁴	1.95 kHz
	X	X	X	X	1	1	1	1	f _{CLK} /2 ¹⁵	977 Hz
1	0	0	0	0	X	X	X	X	f _{CLK}	32 MHz
	0	0	0	1	X	X	X	X	f _{CLK} /2	16 MHz
	0	0	1	0	X	X	X	X	f _{CLK} /2 ²	8 MHz
	0	0	1	1	X	X	X	X	f _{CLK} /2 ³	4 MHz
	0	1	0	0	X	X	X	X	f _{CLK} /2 ⁴	2 MHz
	0	1	0	1	X	X	X	X	f _{CLK} /2 ⁵	1 MHz
	0	1	1	0	X	X	X	X	f _{CLK} /2 ⁶	500 kHz
	0	1	1	1	X	X	X	X	f _{CLK} /2 ⁷	250 kHz
	1	0	0	0	X	X	X	X	f _{CLK} /2 ⁸	125 kHz
	1	0	0	1	X	X	X	X	f _{CLK} /2 ⁹	62.5 kHz
	1	0	1	0	X	X	X	X	f _{CLK} /2 ¹⁰	31.25 kHz
	1	0	1	1	X	X	X	X	f _{CLK} /2 ¹¹	15.63 kHz
	1	1	0	0	X	X	X	X	f _{CLK} /2 ¹²	7.81 kHz
	1	1	0	1	X	X	X	X	f _{CLK} /2 ¹³	3.91 kHz
	1	1	1	0	X	X	X	X	f _{CLK} /2 ¹⁴	1.95 kHz
	1	1	1	1	X	X	X	X	f _{CLK} /2 ¹⁵	977 Hz
Other than above									Setting prohibited	

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

Remarks 1. X: Don't care

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

12.5.9 Procedure for processing errors that occurred during 3-wire serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) communication

The procedure for processing errors that occurred during 3-wire serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) communication is described in Figure 12-76.

Figure 12-76. Processing Procedure in Case of Overrun Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn).	→ The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn).	→ Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

12.6 Operation of UART (UART0 to UART2) Communication

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using UART2, timer array unit 0 (channel 0) with an external interrupt (INTP0).

[Data transmission/reception]

- Data length of 7, 8, or 9 bits ^{Note}
- Select the MSB/LSB first
- Level setting of transmit/receive data (selecting whether to reverse the level)
- Parity bit appending and parity check functions
- Stop bit appending, stop bit check function

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

In addition, UART0 reception (channel 1 of unit 0) supports the SNOOZE mode. When RxD0 pin input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only following UART0 can be specified for the reception baud rate adjustment function.

The LIN-bus is accepted in UART2 (channels 0 and 1 of unit 1) (32, 48, and 64-pin products only).

[LIN-bus functions]

- Wakeup signal detection
- Break field (BF) detection
- Sync field measurement, baud rate calculation

Using the external interrupt (INTP0) and timer array unit 0

Note Only following UART0 can be specified for the 9-bit data length.

UART0 uses channels 0 and 1 of SAU0.

UART1 uses channels 2 and 3 of SAU0.

UART2 uses channels 0 and 1 of SAU1.

- 25-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	—		—
	2	—	UART1	—
	3	CSI11		IIC11

- 32-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	—		—
	2	—	UART1	—
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	CSI21		IIC21

- 48-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	CSI01		IIC01
	2	—	UART1	—
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	CSI21		IIC21

- 64-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	CSI01		IIC01
	2	CSI10	UART1	IIC10
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	CSI21		IIC21

<R> Select any function for each channel. Only the selected function is possible. If UART0 is selected for channels 0 and 1 of unit 0, for example, these channels cannot be used for CSI00 and CSI01. At this time, however, channel 2, 3, or other channels of the same unit can be used for a function other than UART0, such as CSI10, UART1, and IIC10.

Caution When using a serial array unit for UART, both the transmitter side (even-numbered channel) and the receiver side (odd-numbered channel) can only be used for UART.

UART performs the following four types of communication operations.

- UART transmission (See 12.6.1.)
- UART reception (See 12.6.2.)
- LIN transmission (UART2 only) (See 12.7.1.)
- LIN reception (UART2 only) (See 12.7.2.)

12.6.1 UART transmission

UART transmission is an operation to transmit data from the RL78/G1A to another device asynchronously (start-stop synchronization).

Of two channels used for UART, the even channel is used for UART transmission.

<R>

UART	UART0	UART1	UART2
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	TxD0	TxD1	TxD2
Interrupt	INTST0	INTST1	INTST2
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.		
Error detection flag	None		
Transfer data length	7, 8, or 9 bits ^{Note 1}		
Transfer rate	Max. $f_{MCK}/6$ [bps] (SDRmn [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps] ^{Note 2}		
Data phase	Non-reverse output (default: high level) Reverse output (default: low level)		
Parity bit	The following selectable • No parity bit • Appending 0 parity • Appending even parity • Appending odd parity		
Stop bit	The following selectable • Appending 1 bit • Appending 2 bits		
Data direction	MSB or LSB first		

Notes 1. Only following UART0 can be specified for the 9-bit data length.

2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = -40 to +105°C) (TARGET)**).

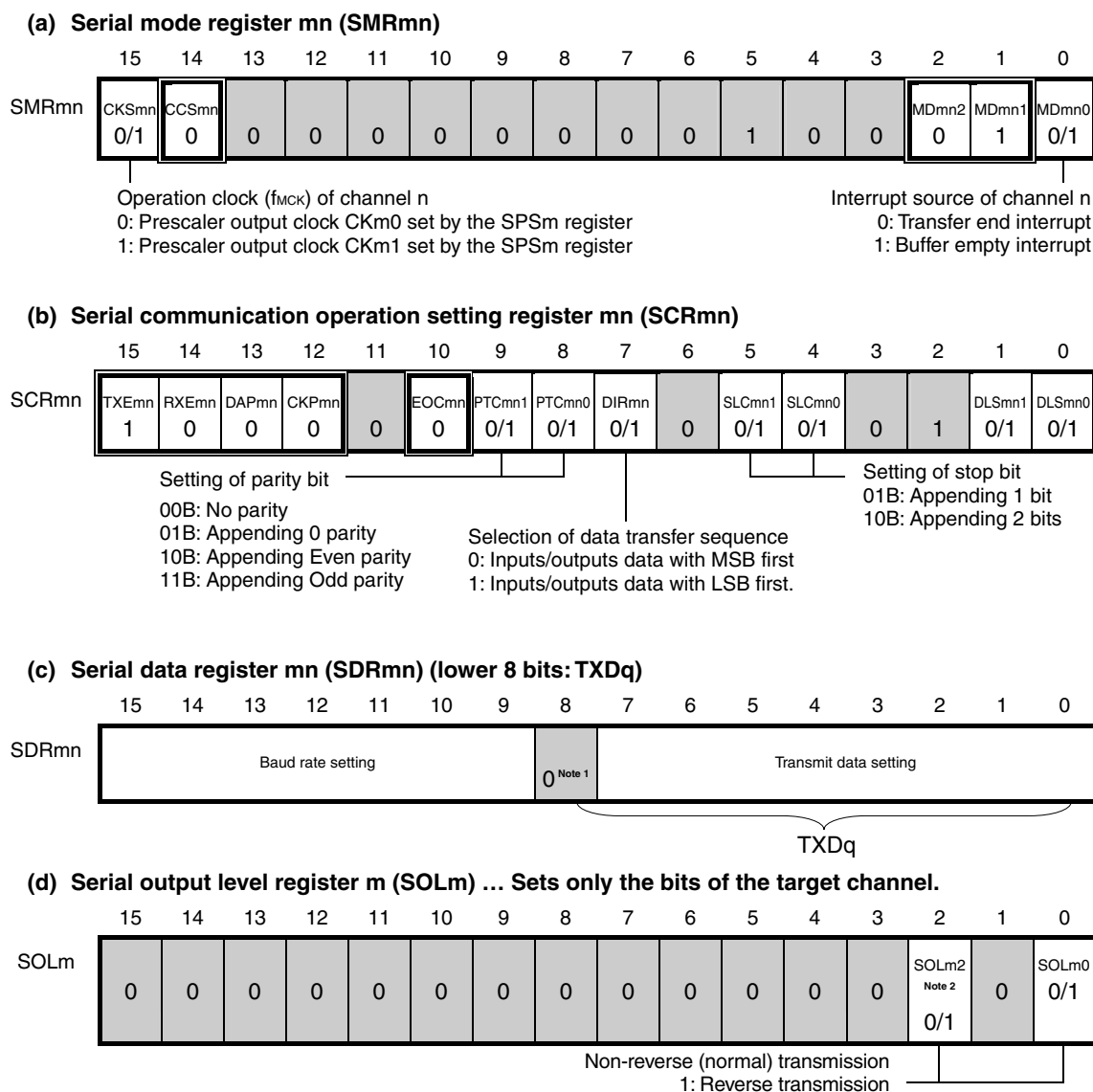
Remarks 1. f_{MCK} : Operation clock frequency of target channel

f_{CLK} : System clock frequency

2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

(1) Register setting

Figure 12-77. Example of Contents of Registers for UART Transmission of UART (UART0 to UART2) (1/2)



- Notes**
1. Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.
 2. When UART0 performs 9-bit communication (by setting the DLS001 and DLS000 bits of the SCR00 register to 1), bits 0 to 8 of the SDR00 register are used as the transmission data specification area. Only following UART0 can be specified for the 9-bit data length.
 3. Unit 0 only

- Remarks**
1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2), mn = 00, 02, 10
 2. : Setting is fixed in the UART transmission mode, : Setting disabled (set to the initial value)
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
 0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-77. Example of Contents of Registers for UART Transmission of UART
(UART0 to UART2) (2/2)**

(e) Serial output register m (SOM) ... Sets only the bits of the target channel.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOM	0	0	0	0	CKOm3 Note 1	CKOm2 Note 1	CKOm1	CKOm0	0	0	0	0	Som3 Note 1	SOM2 Notes 1,2	SOM1	SOM0 Note 2
					×	×	×	×					×	0/1	×	0/1

0: Serial data output value is "0"
1: Serial data output value is "1"

(f) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOEm3 Note 1	SOEm2 Note 1	SOEm1	SOEm0
													×	0/1	×	0/1

(g) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 1	SSm2 Note 1	SSm1	SSm0
													×	0/1	×	0/1

Notes 1. Before transmission is started, be sure to set to 1 when the SOLmn bit of the target channel is set to 0, and set to 0 when the SOLmn bit of the target channel is set to 1. The value varies depending on the communication data during communication operation.

2. Unit 0 only

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2)
mn = 00, 02, 10

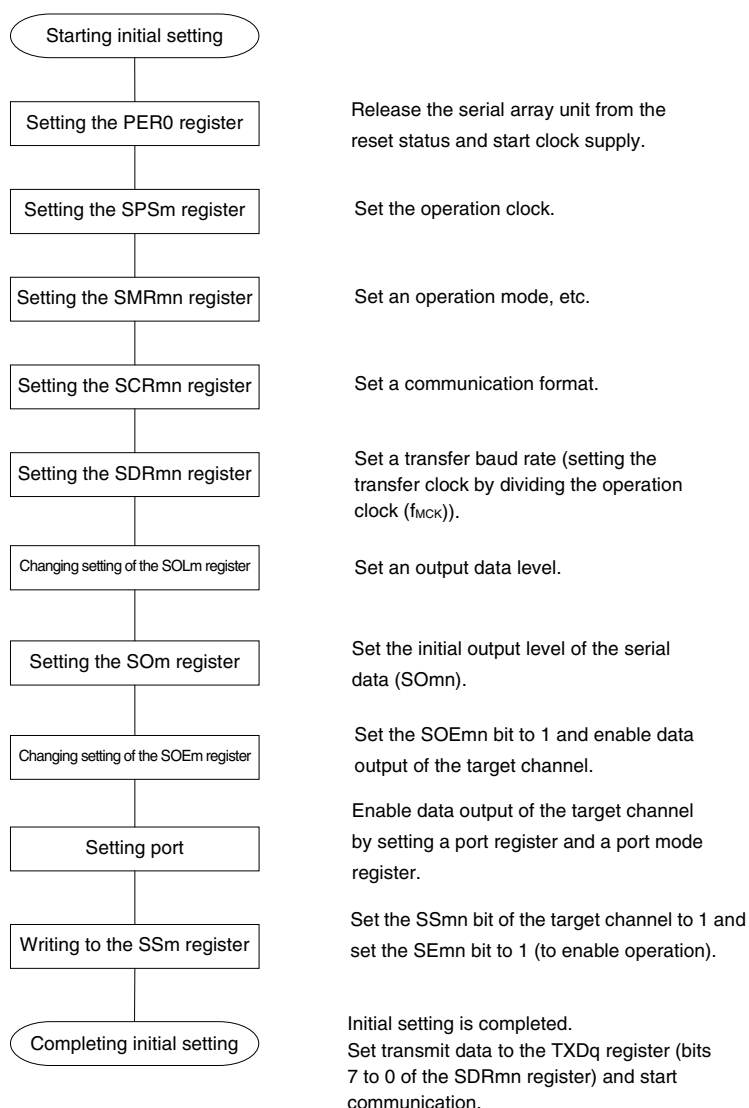
2. : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

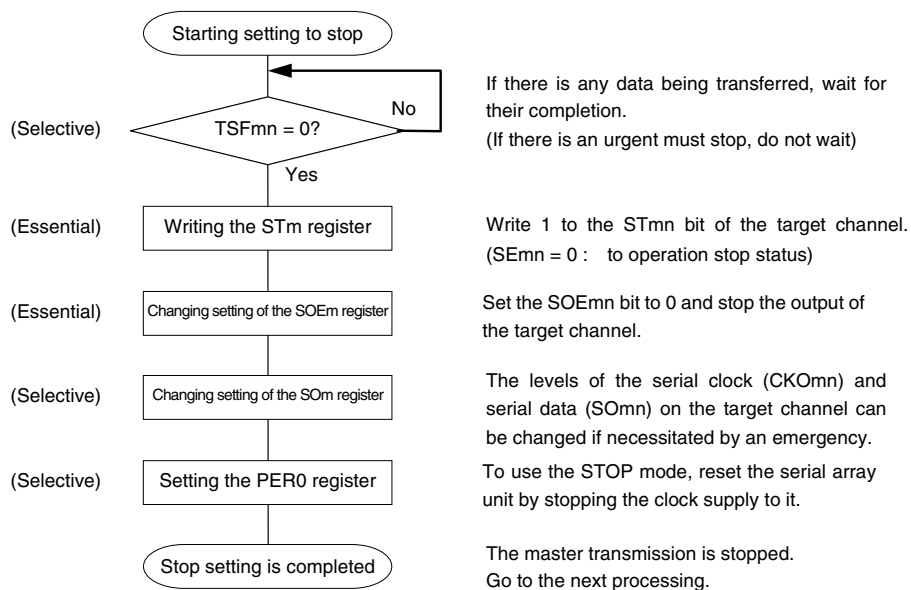
(2) Operation procedure

Figure 12-78. Initial Setting Procedure for UART Transmission



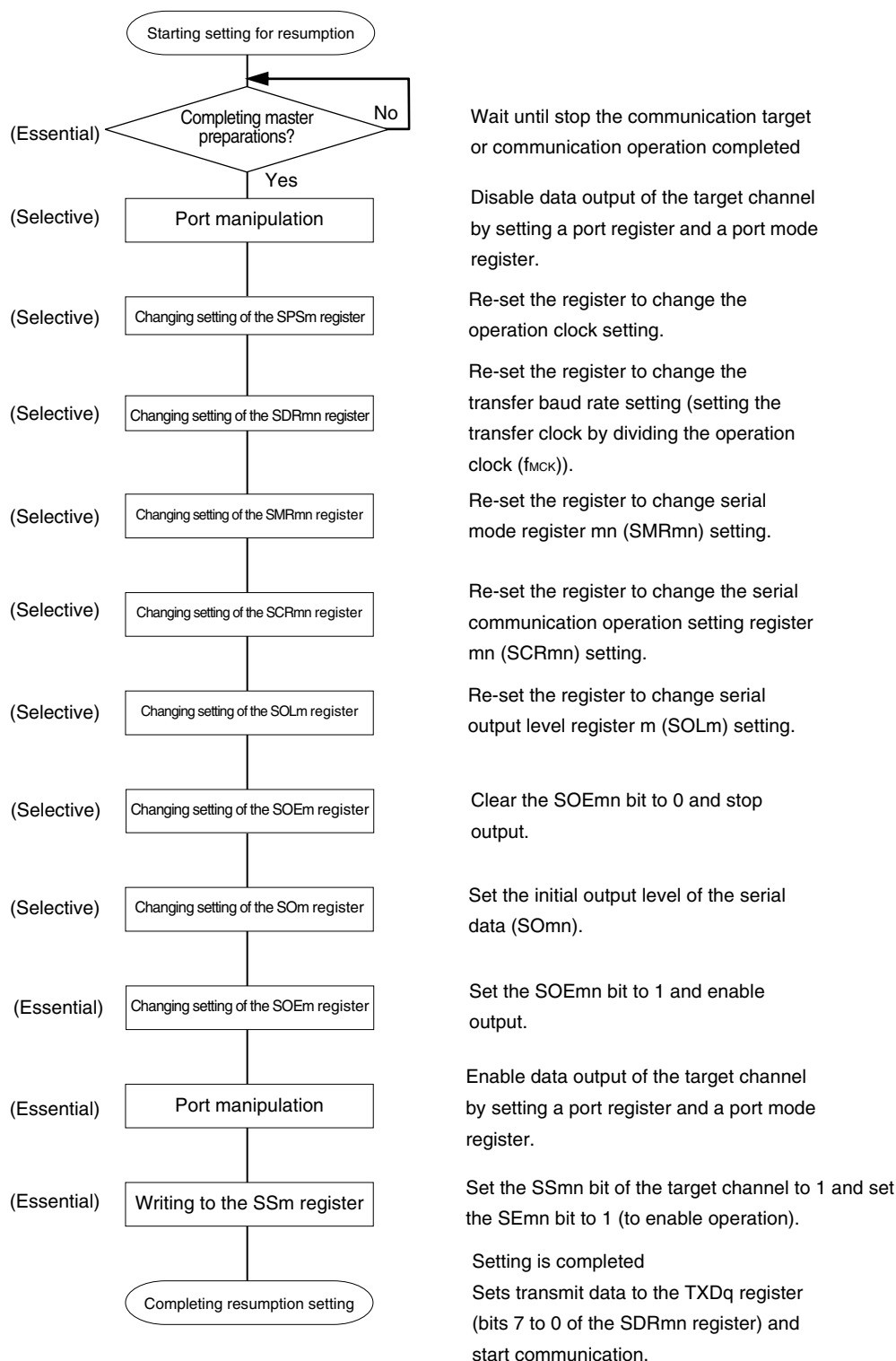
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2)
mn = 00, 02, 10

<R>

Figure 12-79. Procedure for Stopping UART Transmission

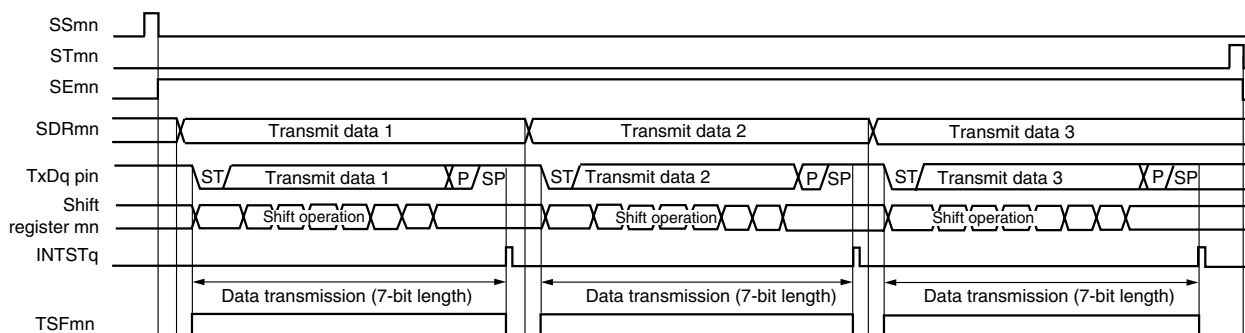
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2)
mn = 00, 02, 10

<R>

Figure 12-80. Procedure for Resuming UART Transmission

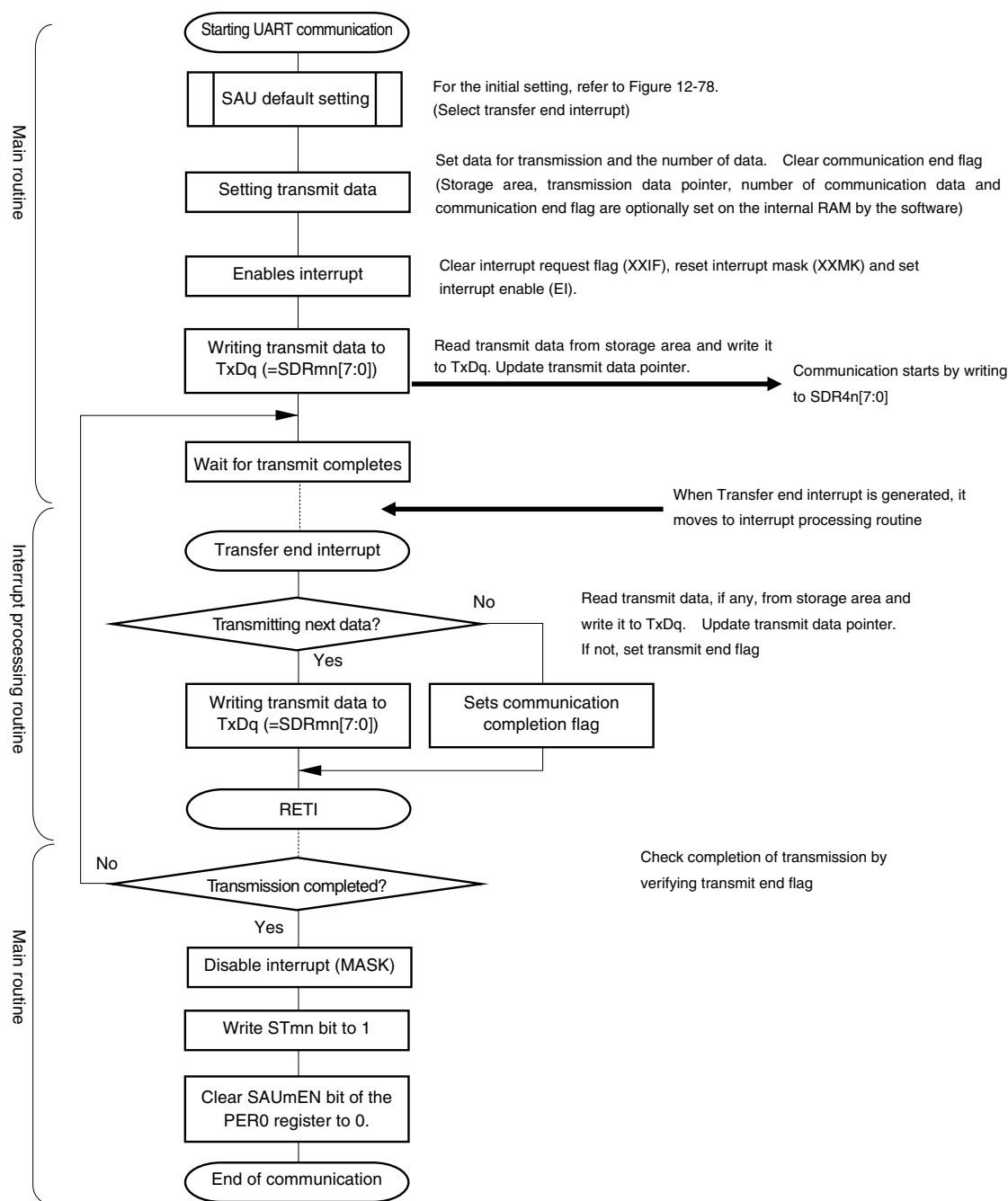
Remarks 1. If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target stops or transmission finishes, and then perform initialization instead of restarting the transmission.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2), mn = 00, 02, 10

(3) Processing flow (in single-transmission mode)**Figure 12-81. Timing Chart of UART Transmission (in Single-Transmission Mode)**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2)
 mn = 00, 02, 10

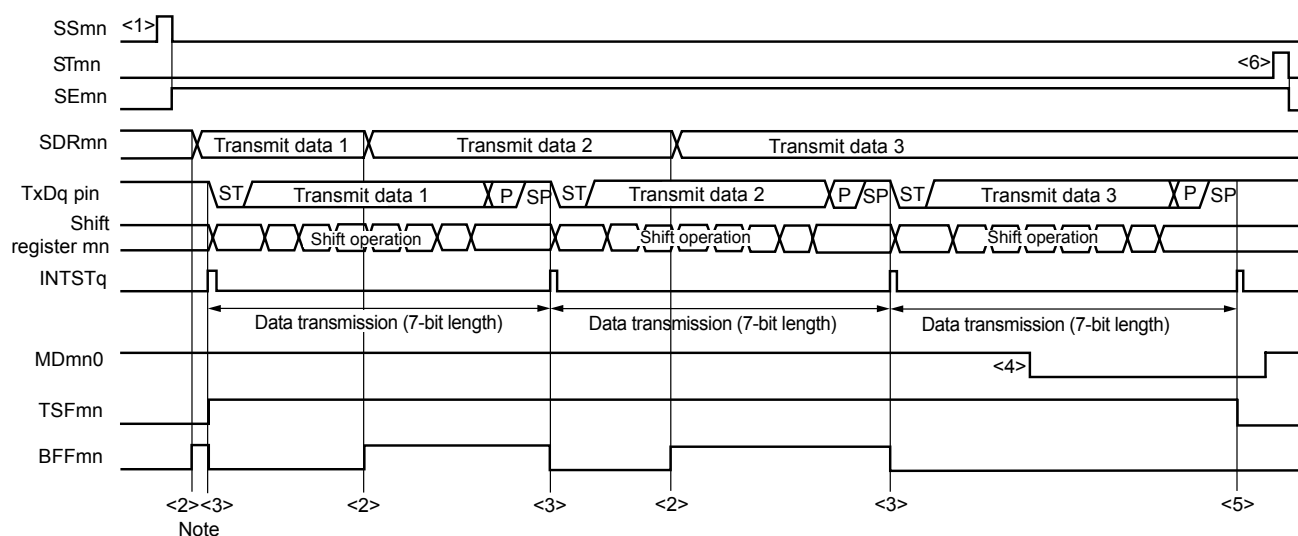
<R>

Figure 12-82. Flowchart of UART Transmission (in Single-Transmission Mode)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2)
mn = 00, 02, 10

(4) Processing flow (in continuous transmission mode)

Figure 12-83. Timing Chart of UART Transmission (in Continuous Transmission Mode)

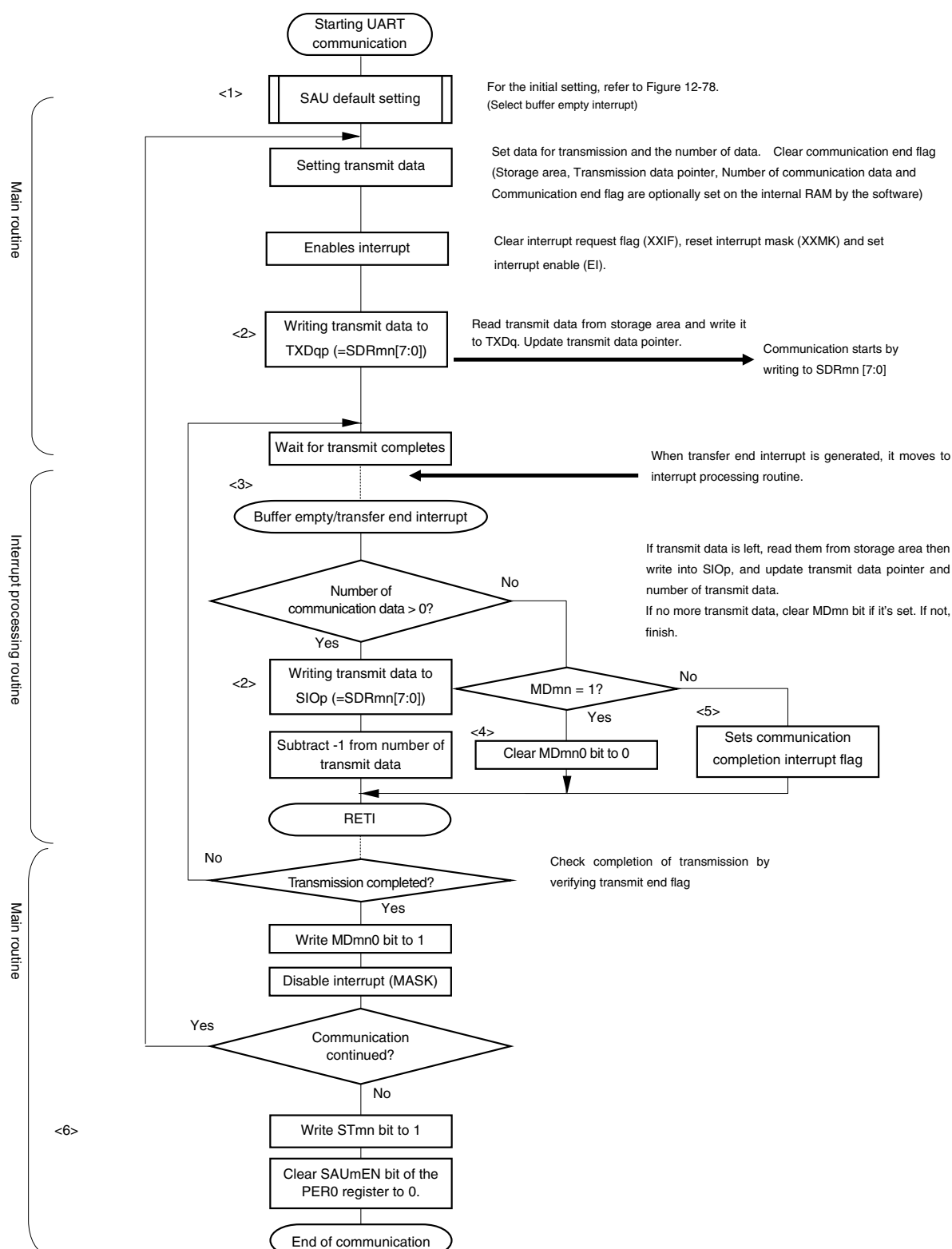


Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution The MDmn0 bit of serial mode register mn (SSRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2)
mn = 00, 02, 10

<R>

Figure 12-84. Flowchart of UART Transmission (in Continuous Transmission Mode)

Remarks 1. <1> to <6> in the figure correspond to <1> to <6> in **Figure 12-83 Timing Chart of UART Transmission (in Continuous Transmission Mode).**

- 2.** m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2)
mn = 00, 02, 10

12.6.2 UART reception

UART reception is an operation wherein the RL78/G1A asynchronously receives data from another device (start-stop synchronization).

For UART reception, the odd-number channel of the two channels used for UART is used. The SMR register of both the odd- and even-numbered channels must be set.

<R>

UART	UART0	UART1	UART2
Target channel	Channel 1 of SAU0	Channel 3 of SAU0	Channel 1 of SAU1
Pins used	RxD0	RxD1	RxD2
Interrupt	INTSR0	INTSR1	INTSR2
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)		
Error interrupt	INTSRE0	INTSRE1	INTSRE2
Error detection flag	- Framing error detection flag (FEFmn) - Parity error detection flag (PEFmn) - Overrun error detection flag (OVFmn)		
Transfer data length	7, 8 or 9 bits ^{Note 1}		
Transfer rate	Max. $f_{MCK}/6$ [bps] (SDRmn [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps] ^{Note 2}		
Data phase	Non-reverse output (default: high level) Reverse output (default: low level)		
Parity bit	The following selectable - No parity bit (no parity check) - No parity judgment (0 parity) - Appending even parity - Appending odd parity		
Stop bit	1 bit check		
Data direction	MSB or LSB first		

Notes 1. Only following UART0 can be specified for the 8-bit data length.

2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = -40 to +105°C) (TARGET)**).

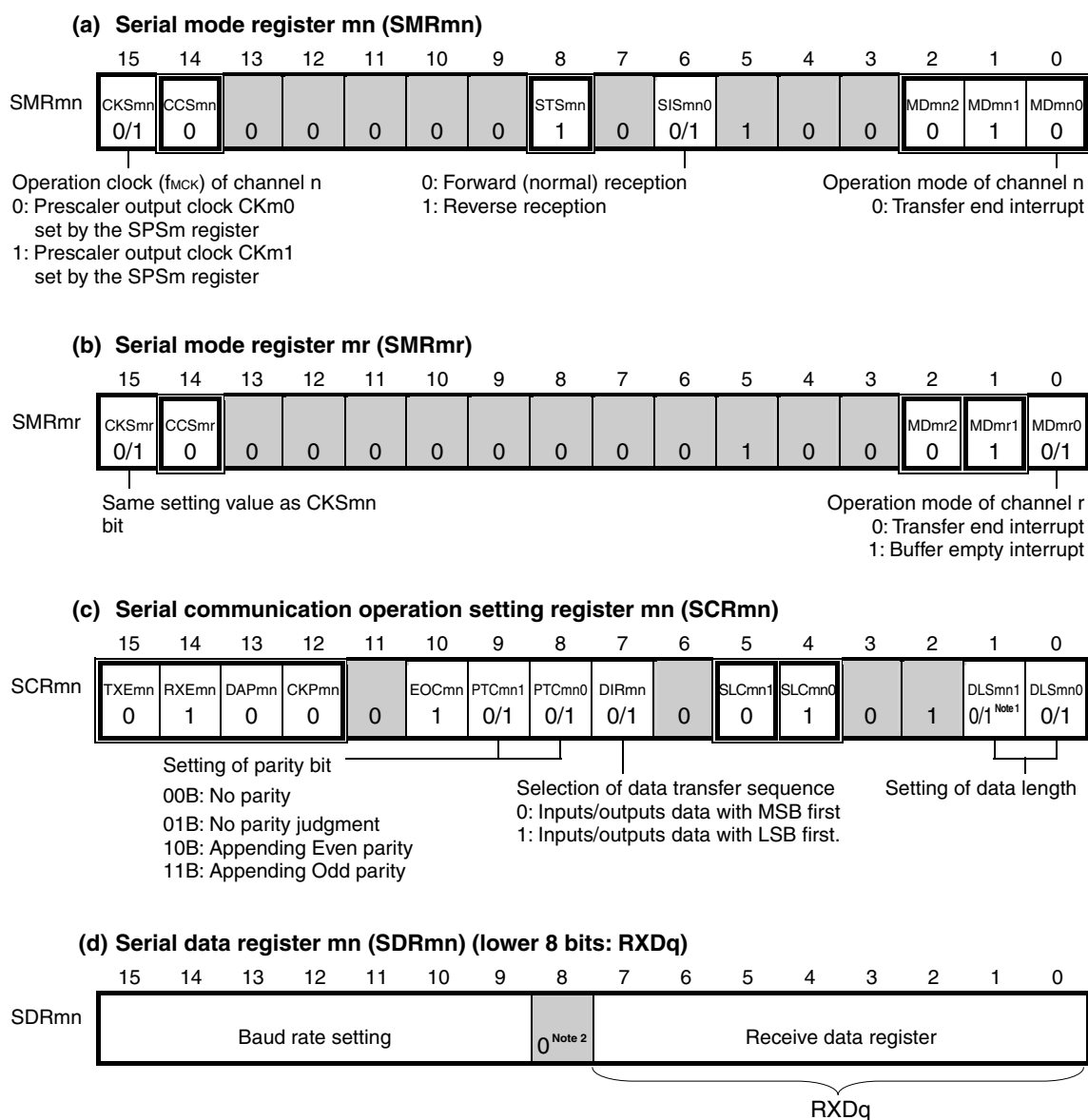
Remarks 1. f_{MCK} : Operation clock frequency of target channel

f_{CLK} : System clock frequency

2. m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11

(1) Register setting

<R>

Figure 12-85. Example of Contents of Registers for UART Reception of UART (UART0 to UART2) (1/2)

Notes 1. Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.

2. When UART performs 9-bit communication, bits 0 to 8 of the SDRm1 register are used as the transmission data specification area. Only following UART0 can be specified for the 8-bit data length.

Caution For the UART reception, be sure to set the SMRmr register of channel r to UART transmission mode that is to be paired with channel n.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11

r: Channel number (r = n - 1), q: UART number (q = 0 to 2)

2. : Setting is fixed in the UART reception mode, : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

Figure 12-85. Example of Contents of Registers for UART Reception of UART (UART0 to UART2) (2/2)

(e) Serial output register m (SOM) ... The register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOM	0	0	0	0	CKOm3 Note ×	CKOm2 Note ×	CKOm1 ×	CKOm0 ×	0	0	0	0	SOM3 Note ×	SOM2 Note ×	SOM1 ×	SOM0 ×

(f) Serial output enable register m (SOEm) ...The register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOEm3 Note ×	SOEm2 Note ×	SOEm1 ×	SOEm0 ×

(g) Serial channel start register m (SSm) ... Sets only the bits of the target channel is 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 0/1	SSm2 Note ×	SSm1 0/1	SSm0 ×

Note Unit 0 only

Caution For the UART reception, be sure to set the SMRmr register of channel r to UART Transmission mode that is to be paired with channel n.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11

r: Channel number (r = n – 1), q: UART number (q = 0 to 2)

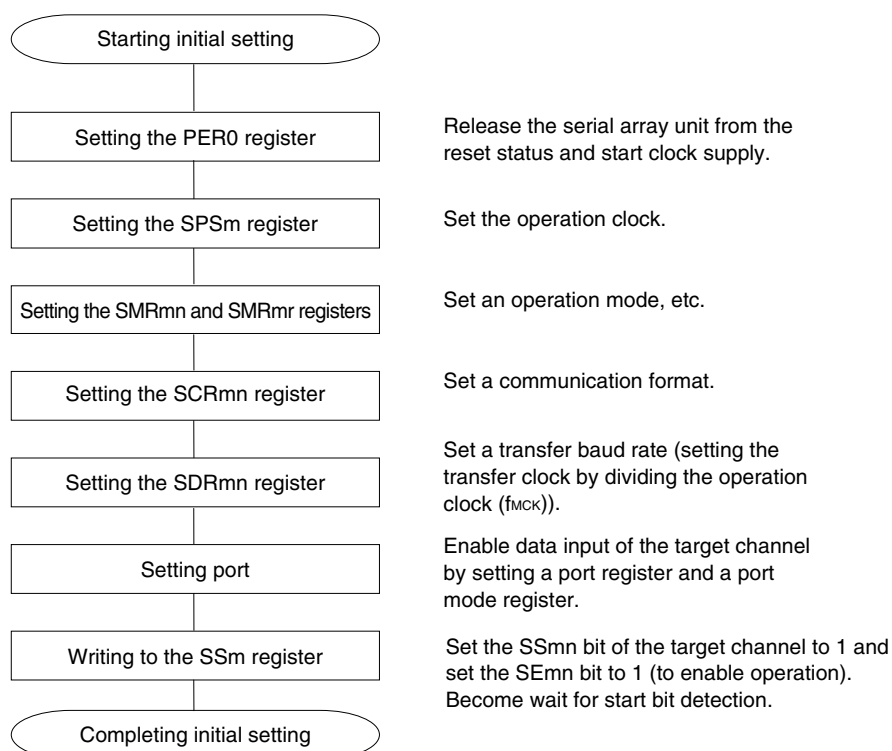
2. ☐: Setting is fixed in the UART reception mode, ☐: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

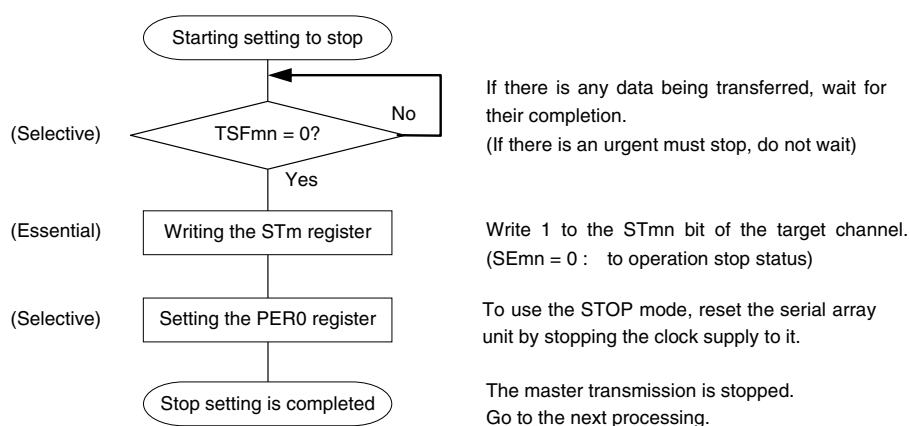
(2) Operation procedure

Figure 12-86. Initial Setting Procedure for UART Reception



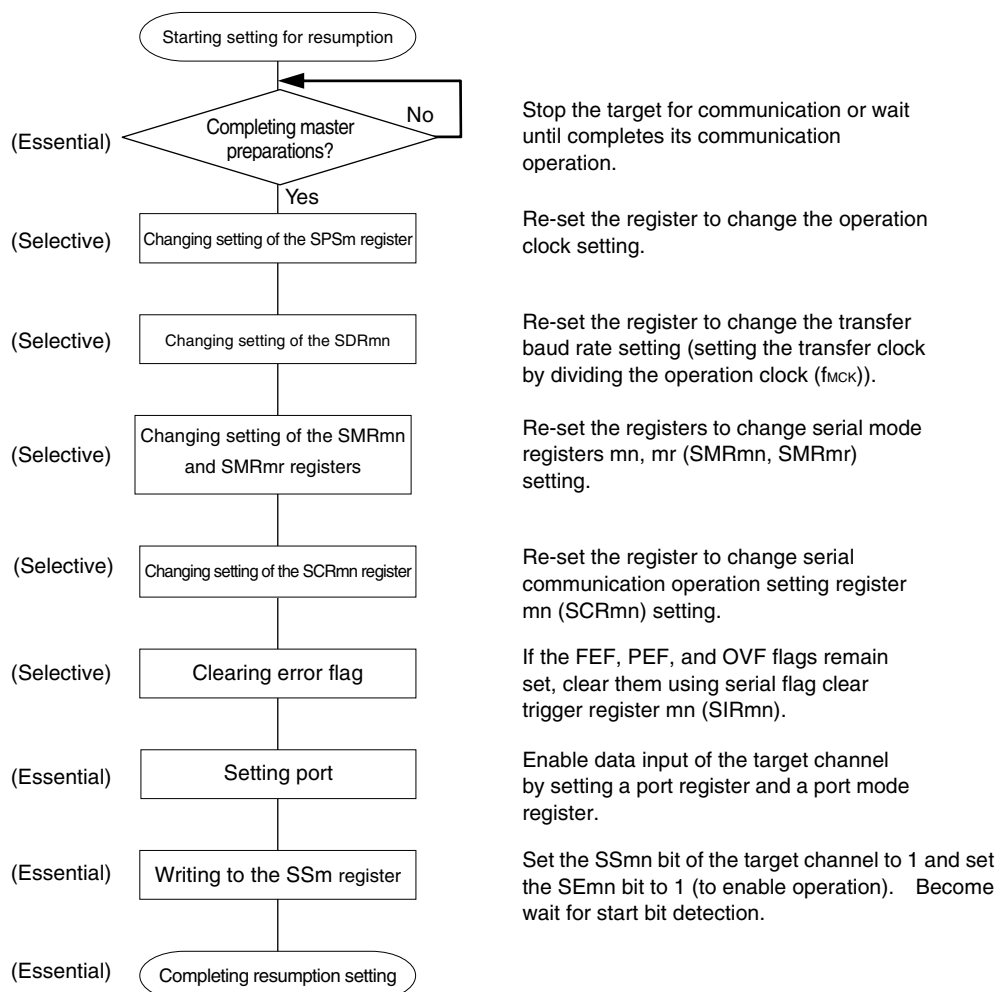
<R> **Caution** Set the RXEmn bit of SCRmn register to 1, and then be sure to set SSmn to 1 after 4 or more f_{MCK} clocks have elapsed.

<R> Figure 12-87. Procedure for Stopping UART Reception



Remark m: Unit number ($m = 0, 1$), n: Channel number ($n = 1, 3$), mn = 01, 03, 11
r: Channel number ($r = n - 1$), q: UART number ($q = 0$ to 2)

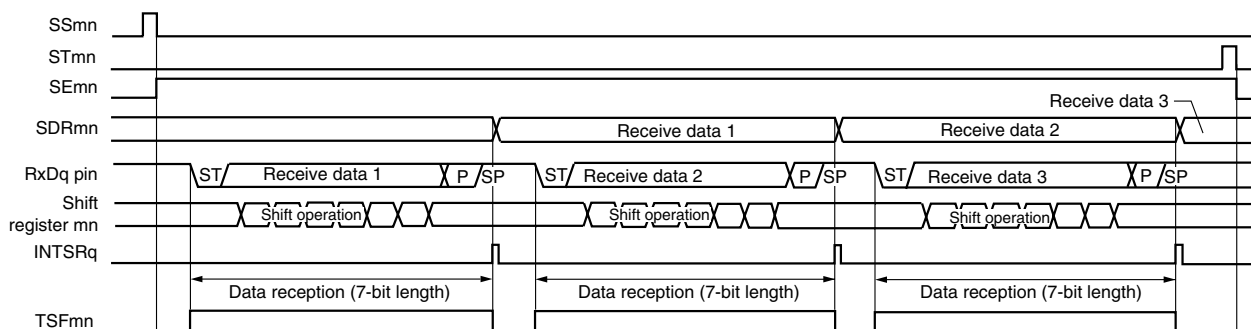
<R>

Figure 12-88. Procedure for Resuming UART Reception

<R>

Caution After is set RXEmn bit to 1 of SCRmn register, set the SSmn = 1 from an interval of at least four clocks of f_{MCK} .

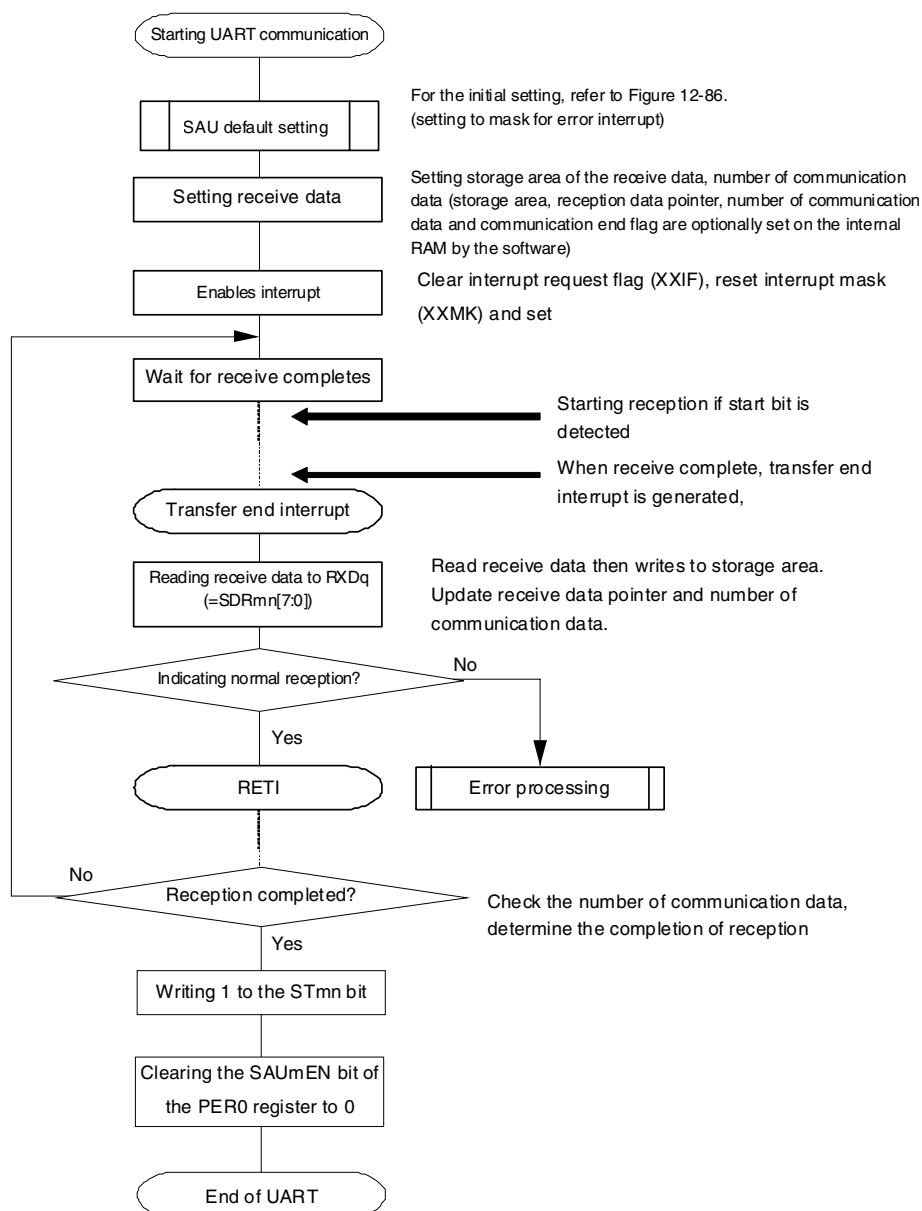
- Remarks**
1. If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (slave) stops or transmission finishes, and then perform initialization instead of restarting the transmission.
 2. m: Unit number ($m = 0, 1$), n: Channel number ($n = 1, 3$), mn = 01, 03, 11
r: Channel number ($r = n - 1$), q: UART number ($q = 0$ to 2)

(3) Processing flow**Figure 12-89. Timing Chart of UART Reception**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11
 r: Channel number (r = n - 1), q: UART number (q = 0 to 2)

<R>

Figure 12-90. Flowchart of UART Reception



Remark m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11
 r: Channel number (r = n - 1), q: UART number (q = 0 to 2)

12.6.3 SNOOZE mode function

<R> SNOOZE mode makes UART operate reception by RxDq pin input detection while the STOP mode. Normally UART stops communication in the STOP mode. But, using the SNOOZE mode makes reception UART operate unless the CPU operation by detecting RxDq pin input. Only following channels can be set to the SNOOZE mode.

When RxDq pin input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only UART0 can be specified for the reception baud rate adjustment function.

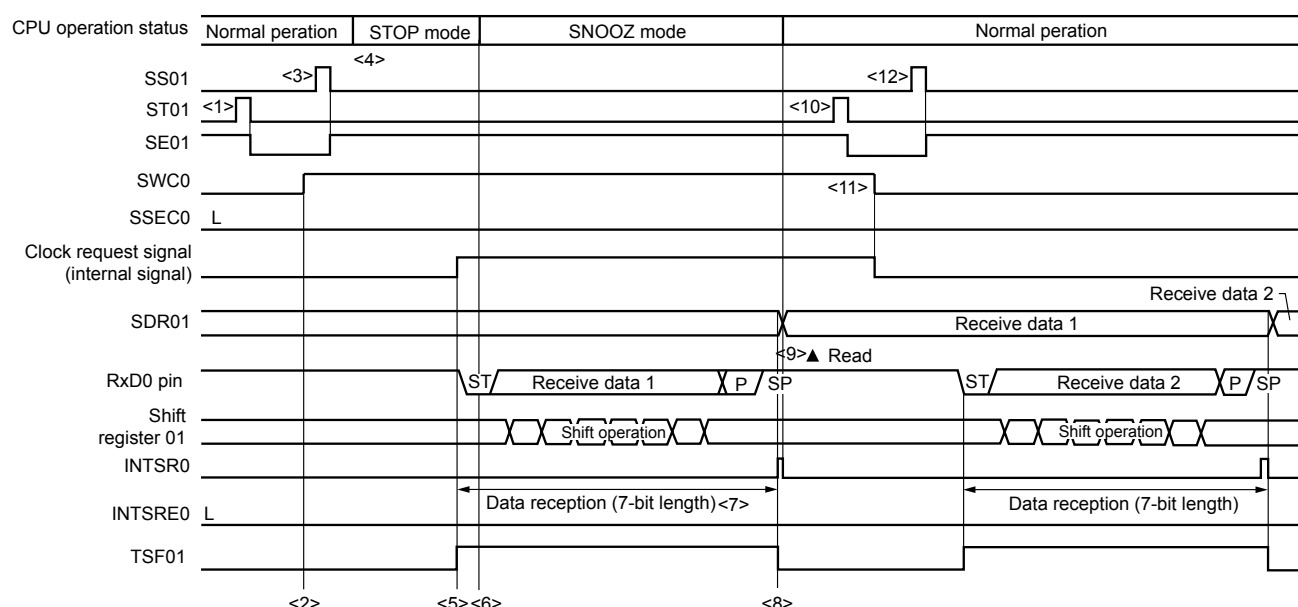
When using the SNOOZE mode function, set the SWCm bit of serial standby control register m (SSCm) to 1 before switching to the STOP mode.

Cautions 1. The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for f_{CLK}.

2. The maximum transfer rate when using UARTq in the SNOOZE mode is 9600 bps.

(1) SNOOZE mode operation (Normal operation)

Figure 12-91. Timing Chart of SNOOZE Mode Operation (Normal operation mode)



<R> **Note** Read the received data when SWCm is 1

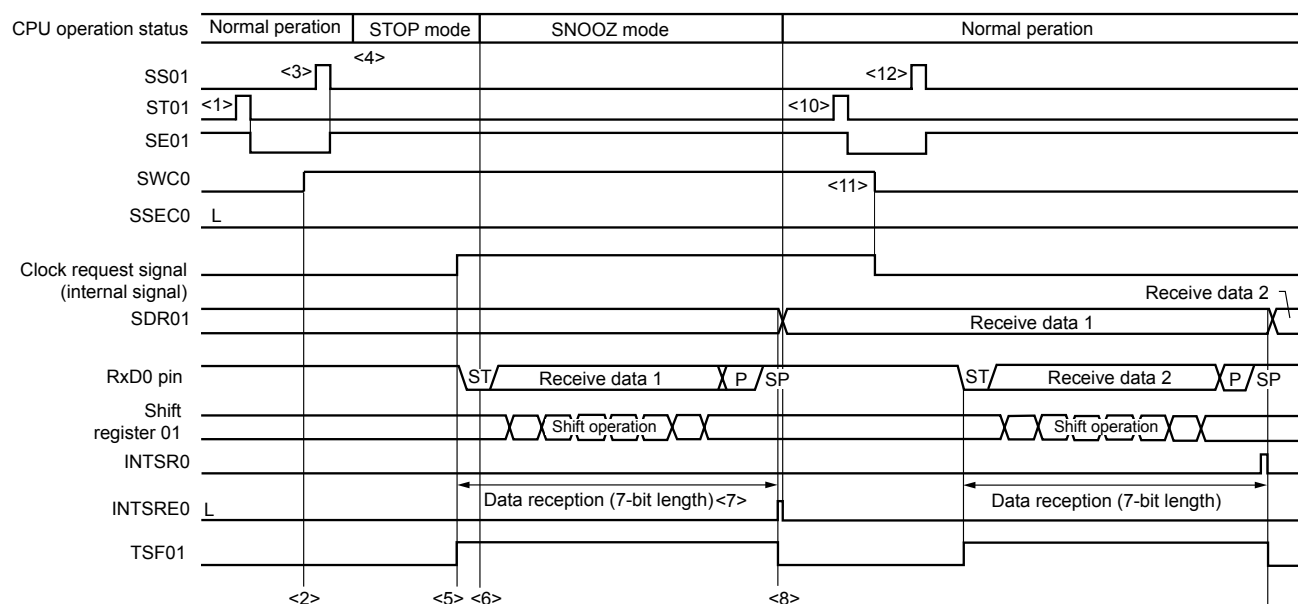
<R> **Caution** Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm1 bit to 1 (clear the SEM1 bit, and stop the operation). And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE mode release).

Remarks 1. <1> to <11> in the figure correspond to <1> to <11> in Figure 12-93. Flowchart of SNOOZE Mode Operation (Normal Operation/Abnormal Operation <1>).

2. m = 0; q = 0

(2) SNOOZE mode operation (Abnormal Operation <1>)

Abnormal operation <1> is the operation performed when a communication error occurs while SSECm = 0.
Because SSECm = 0, an error interrupt (INTSREq) is generated when a communication error occurs.

Figure 12-92. Timing Chart of SNOOZE Mode Operation (Abnormal Operation <1>)

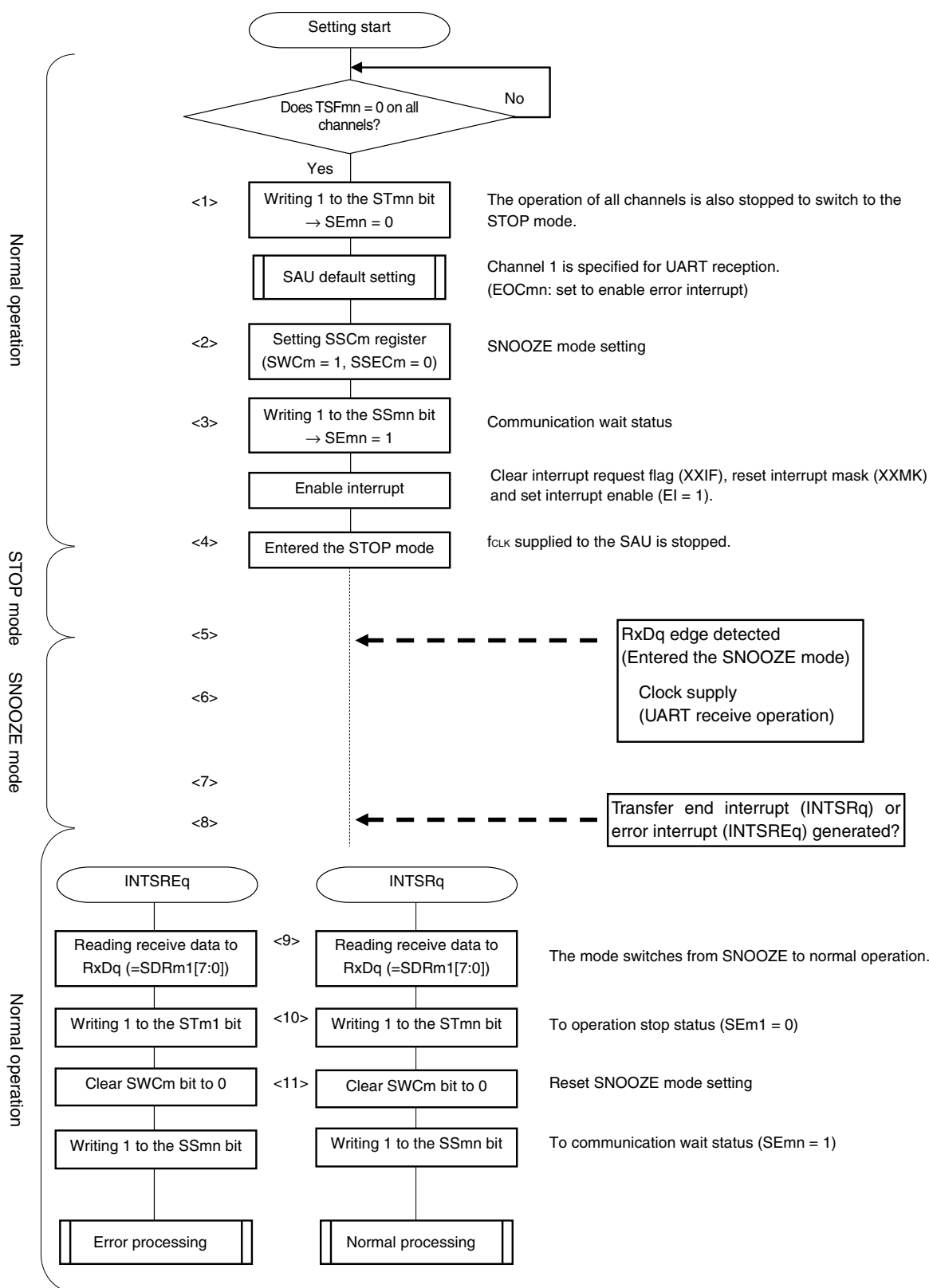
<R>

Caution Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm1 bit to 1 (clear the SEM1 bit, and stop the operation).
And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE mode release).

Remarks 1. <1> to <11> in the figure correspond to <1> to <11> in Figure 12-93. Flowchart of SNOOZE Mode Operation (Normal Operation/Abnormal Operation <1>).

2. m = 0

<R> **Figure 12-93. Flowchart of SNOOZE Mode Operation (Normal Operation/Abnormal Operation <1>)**

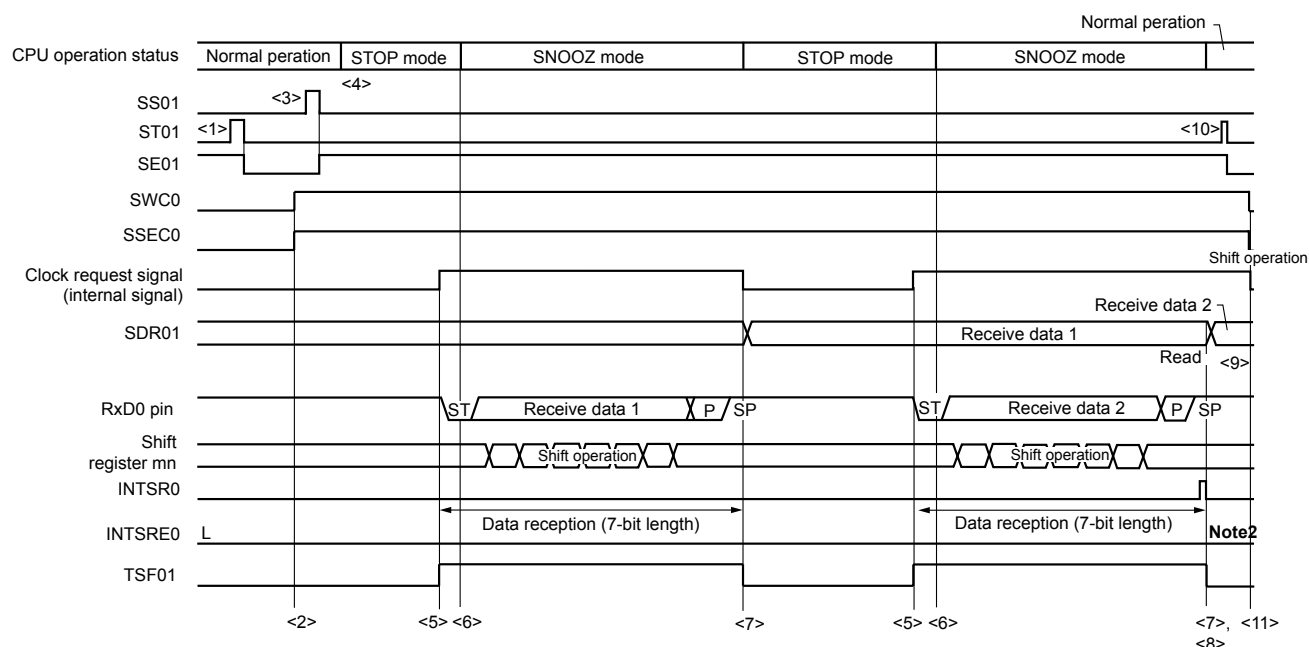


Remarks 1. <1> to <11> in the figure correspond to <1> to <11> in **Figure 12-91. Timing Chart of SNOOZE Mode Operation (Normal operation mode)** and **Figure 12-92. Timing Chart of SNOOZE Mode Operation (Abnormal Operation <1>).**

2. m = 0; q = 0

(3) SNOOZE mode operation (Abnormal Operation <2>)

Abnormal operation <2> is the operation performed when a communication error occurs while $SSECm = 1$. Because $SSECm = 1$, an error interrupt (INTSREq) is not generated when a communication error occurs.

Figure 12-94. Timing Chart of SNOOZE Mode Operation (Abnormal Operation <2>)

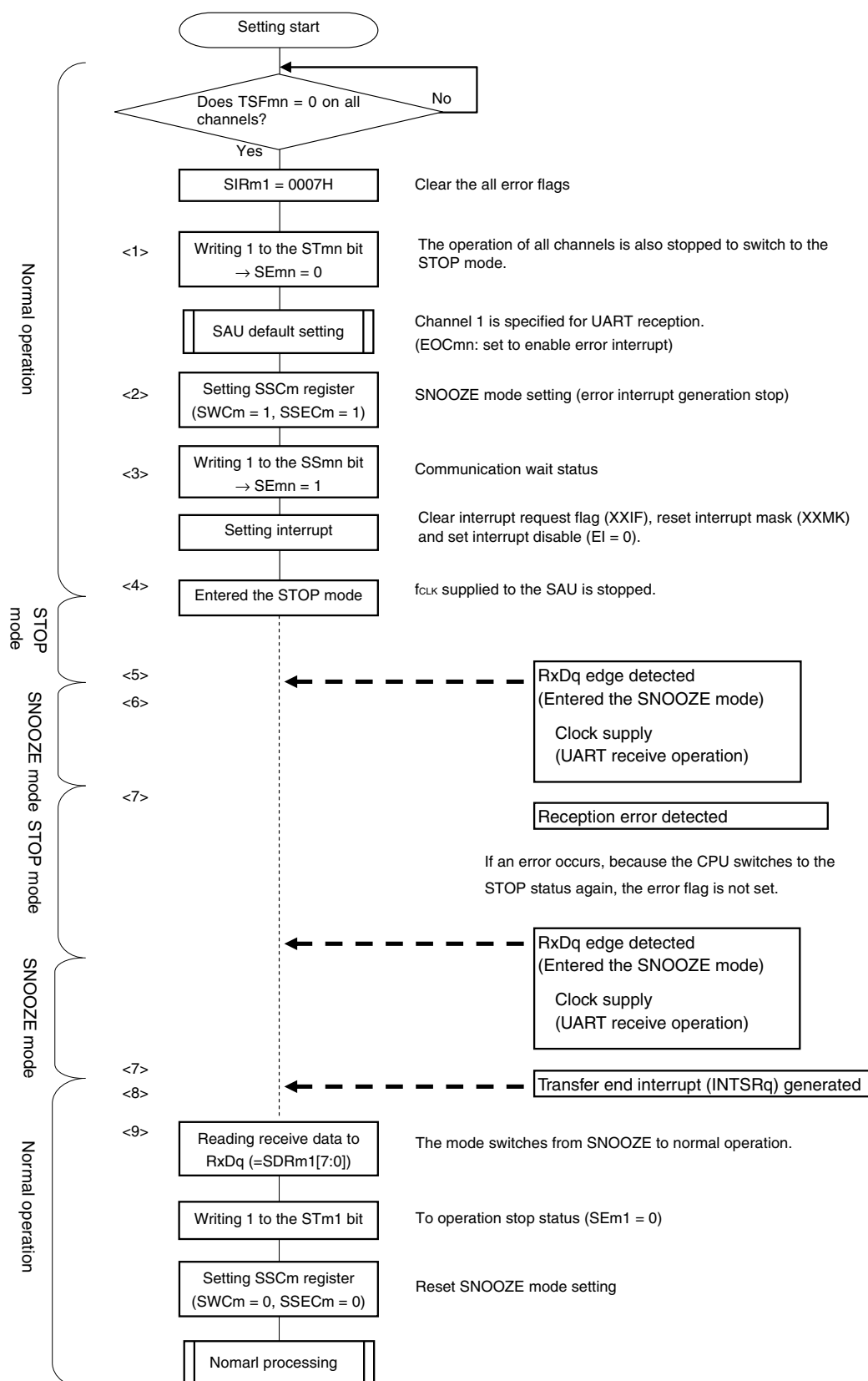
- <R> **Notes**
1. Only read received data while $SWCm = 1$.
 2. After UARTq successfully finishes reception in the SNOOZE mode, it is possible to continue to perform normal reception operations without changing the settings, but, because $SSECm = 1$, the $PEFm1$ and $FEFm1$ bits are not set even if a framing error or parity error occurs. In addition, no error interrupt (INTSREq) is generated.

- <R> **Cautions**
1. Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the $STm1$ bit to 1 (clear the $SEm1$ bit, and stop the operation). And after completion the receive operation, also clearing $SWCm$ bit to 0 (SNOOZE mode release).
 2. When using the SNOOZE mode while $SSECm$ is set to 1, no overrun errors occur. Therefore, when using the SNOOZE mode, read bits 7 to 0 ($RxDq$) of the $SDRm1$ register before switching to the STOP mode.

- Remarks**
1. <1> to <9> in the figure correspond to <1> to <9> in **Figure 12-95. Flowchart of SNOOZE Mode Operation (Abnormal Operation <2>)**.
 2. $m = 0$; $q = 0$

$\langle R \rangle$

Figure 12-95. Flowchart of SNOOZE Mode Operation (Abnormal Operation <2>)



Caution When using the SNOOZE mode while SSECm is set to 1, no overrun errors occur. Therefore, when using the SNOOZE mode, read bits 7 to 0 (RxDq) of the SDRm1 register before switching to the STOP mode.

Remarks 1. <1> to <9> in the figure correspond to <1> to <9> in **Figure 12-94. Timing Chart of SNOOZE Mode Operation (Abnormal Operation <2>).**

2. m = 0; q = 0

12.6.4 Calculating baud rate

(1) Baud rate calculation expression

The baud rate for UART (UART0 to UART2) communication can be calculated by the following expressions.

$$(\text{Baud rate}) = \{\text{Operation clock (f}_{\text{MCK}}\text{) frequency of target channel}\} \div (\text{SDRmn}[15:9] + 1) \div 2 \text{ [bps]}$$

Caution Setting serial data register mn (SDRmn) SDRmn[15:9] = (0000000B, 0000001B) is prohibited.

Remarks 1. When UART is used, the value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000010B to 1111111B) and therefore is 2 to 127.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 12-3. Selection of Operation Clock For UART

SMRmn Register	SPSm Register								Operation Clock (f _{CLK}) ^{Note}	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		f _{CLK} = 32 MHz
0	X	X	X	X	0	0	0	0	f _{CLK}	32 MHz
	X	X	X	X	0	0	0	1	f _{CLK} /2	16 MHz
	X	X	X	X	0	0	1	0	f _{CLK} /2 ²	8 MHz
	X	X	X	X	0	0	1	1	f _{CLK} /2 ³	4 MHz
	X	X	X	X	0	1	0	0	f _{CLK} /2 ⁴	2 MHz
	X	X	X	X	0	1	0	1	f _{CLK} /2 ⁵	1 MHz
	X	X	X	X	0	1	1	0	f _{CLK} /2 ⁶	500 kHz
	X	X	X	X	0	1	1	1	f _{CLK} /2 ⁷	250 kHz
	X	X	X	X	1	0	0	0	f _{CLK} /2 ⁸	125 kHz
	X	X	X	X	1	0	0	1	f _{CLK} /2 ⁹	62.5 kHz
	X	X	X	X	1	0	1	0	f _{CLK} /2 ¹⁰	31.25 kHz
	X	X	X	X	1	0	1	1	f _{CLK} /2 ¹¹	15.63 kHz
	X	X	X	X	1	1	0	0	f _{CLK} /2 ¹²	7.81 kHz
	X	X	X	X	1	1	0	1	f _{CLK} /2 ¹³	3.91 kHz
	X	X	X	X	1	1	1	0	f _{CLK} /2 ¹⁴	1.95 kHz
	X	X	X	X	1	1	1	1	f _{CLK} /2 ¹⁵	977 Hz
1	0	0	0	0	X	X	X	X	f _{CLK}	32 MHz
	0	0	0	1	X	X	X	X	f _{CLK} /2	16 MHz
	0	0	1	0	X	X	X	X	f _{CLK} /2 ²	8 MHz
	0	0	1	1	X	X	X	X	f _{CLK} /2 ³	4 MHz
	0	1	0	0	X	X	X	X	f _{CLK} /2 ⁴	2 MHz
	0	1	0	1	X	X	X	X	f _{CLK} /2 ⁵	1 MHz
	0	1	1	0	X	X	X	X	f _{CLK} /2 ⁶	500 kHz
	0	1	1	1	X	X	X	X	f _{CLK} /2 ⁷	250 kHz
	1	0	0	0	X	X	X	X	f _{CLK} /2 ⁸	125 kHz
	1	0	0	1	X	X	X	X	f _{CLK} /2 ⁹	62.5 kHz
	1	0	1	0	X	X	X	X	f _{CLK} /2 ¹⁰	31.25 kHz
	1	0	1	1	X	X	X	X	f _{CLK} /2 ¹¹	15.63 kHz
	1	1	0	0	X	X	X	X	f _{CLK} /2 ¹²	7.81 kHz
	1	1	0	1	X	X	X	X	f _{CLK} /2 ¹³	3.91 kHz
	1	1	1	0	X	X	X	X	f _{CLK} /2 ¹⁴	1.95 kHz
	1	1	1	1	X	X	X	X	f _{CLK} /2 ¹⁵	977 Hz
Other than above									Setting prohibited	

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

Remarks 1. X: Don't care

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

(2) Baud rate error during transmission

The baud rate error of UART (UART0 to UART2) communication during transmission can be calculated by the following expression. Make sure that the baud rate at the transmission side is within the permissible baud rate range at the reception side.

$$(\text{Baud rate error}) = (\text{Calculated baud rate value}) \div (\text{Target baud rate}) \times 100 - 100 [\%]$$

Here is an example of setting a UART baud rate at $f_{\text{CLK}} = 32 \text{ MHz}$.

UART Baud Rate (Target Baud Rate)	$f_{\text{CLK}} = 32 \text{ MHz}$			
	Operation Clock (f_{MCK})	SDRmn[15:9]	Calculated Baud Rate	Error from Target Baud Rate
300 bps	$f_{\text{CLK}}/2^9$	103	300.48 bps	+0.16 %
600 bps	$f_{\text{CLK}}/2^8$	103	600.96 bps	+0.16 %
1200 bps	$f_{\text{CLK}}/2^7$	103	1201.92 bps	+0.16 %
2400 bps	$f_{\text{CLK}}/2^6$	103	2403.85 bps	+0.16 %
4800 bps	$f_{\text{CLK}}/2^5$	103	4807.69 bps	+0.16 %
9600 bps	$f_{\text{CLK}}/2^4$	103	9615.38 bps	+0.16 %
19200 bps	$f_{\text{CLK}}/2^3$	103	19230.8 bps	+0.16 %
31250 bps	$f_{\text{CLK}}/2^3$	63	31250.0 bps	$\pm 0.0 \%$
38400 bps	$f_{\text{CLK}}/2^2$	103	38461.5 bps	+0.16 %
76800 bps	$f_{\text{CLK}}/2$	103	76923.1 bps	+0.16 %
153600 bps	f_{CLK}	103	153846 bps	+0.16 %
312500 bps	f_{CLK}	50	312500 bps	$\pm 0.39 \%$

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

(3) Permissible baud rate range for reception

The permissible baud rate range for reception during UART (UART0 to UART2) communication can be calculated by the following expression. Make sure that the baud rate at the transmission side is within the permissible baud rate range at the reception side.

$$(\text{Maximum receivable baud rate}) = \frac{2 \times k \times \text{Nfr}}{2 \times k \times \text{Nfr} - k + 2} \times \text{Brate}$$

$$(\text{Minimum receivable baud rate}) = \frac{2 \times k \times (\text{Nfr} - 1)}{2 \times k \times \text{Nfr} - k - 2} \times \text{Brate}$$

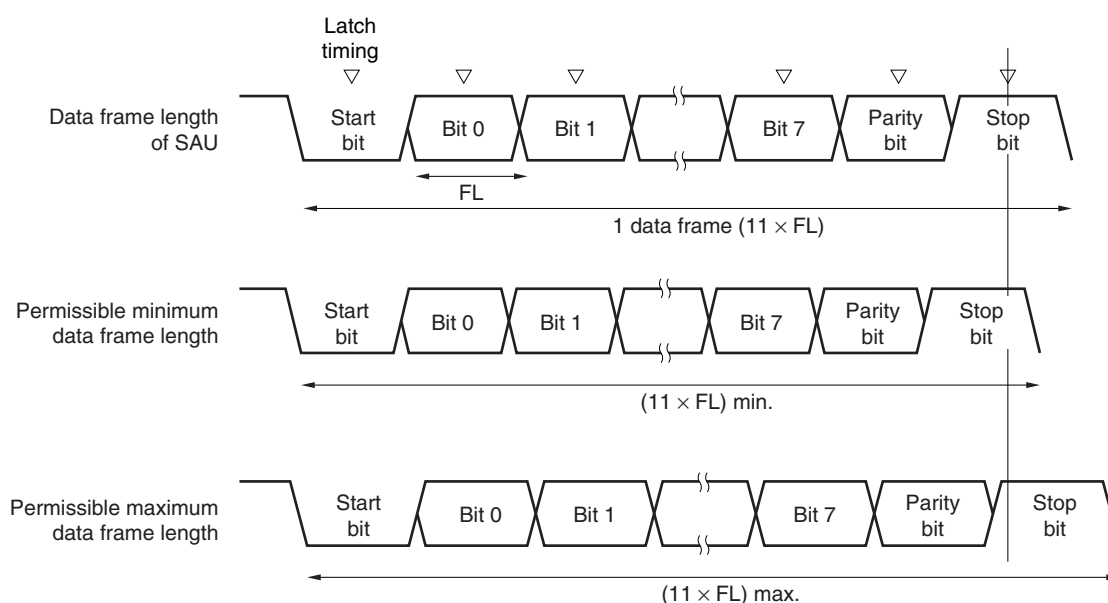
Brate: Calculated baud rate value at the reception side (See **12.6.4 (1) Baud rate calculation expression.**)

k: $\text{SDRmn}[15:9] + 1$

Nfr: 1 data frame length [bits]
 = (Start bit) + (Data length) + (Parity bit) + (Stop bit)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11

Figure 12-96. Permissible Baud Rate Range for Reception (1 Data Frame Length = 11 Bits)



As shown in Figure 12-96, the timing of latching receive data is determined by the division ratio set by bits 15 to 9 of serial data register mn (SDRmn) after the start bit is detected. If the last data (stop bit) is received before this latch timing, the data can be correctly received.

12.6.5 Procedure for processing errors that occurred during UART (UART0 to UART2) communication

The procedure for processing errors that occurred during UART (UART0 to UART2) communication is described in Figures 12-97 and 12-98.

Figure 12-97. Processing Procedure in Case of Parity Error or Overrun Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

Figure 12-98. Processing Procedure in Case of Framing Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.
Sets the STmn bit of serial channel stop register m (STm) to 1. →	The SEMn bit of serial channel enable status register m (SEm) is set to 0 and channel n stops operating.	
Synchronization with other party of communication		Synchronization with the other party of communication is re-established and communication is resumed because it is considered that a framing error has occurred because the start bit has been shifted.
Sets the SSmn bit of serial channel start register m (SSm) to 1. →	The SEMn bit of serial channel enable status register m (SEm) is set to 1 and channel n is enabled to operate.	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

12.7 LIN Communication Operation

12.7.1 LIN transmission

Of UART transmission, UART2 of the 32, 48, and 64-pin products support LIN communication.

For LIN transmission, channel 0 of unit 1 is used.

UART	UART0	UART1	UART2
Support of LIN communication	Not supported	Not supported	Supported
Target channel	–	–	Channel 0 of SAU1
Pins used	–	–	TxD2
Interrupt	–	–	INTST2
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.		
Error detection flag	None		
Transfer data length	8 bits		
<R> Transfer rate	Max. $f_{MCK}/6$ [bps] (SDR10 [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps] ^{Note}		
Data phase	Non-reverse output (default: high level) Reverse output (default: low level)		
<R> Parity bit	No parity bit		
<R> Stop bit	Appending 1 bit		
<R> Data direction	LSB first		

Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in <R> the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (TA = –40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS TA = –40 to +105°C) (TARGET)**). In addition, LIN communication is usually 2.4/9.6/19.2 kbps is often used.

Remark f_{MCK} : Operation clock frequency of target channel
 f_{CLK} : System clock frequency

LIN stands for Local Interconnect Network and is a low-speed (1 to 20 kbps) serial communication protocol designed to reduce the cost of an automobile network.

Communication of LIN is single-master communication and up to 15 slaves can be connected to one master.

The slaves are used to control switches, actuators, and sensors, which are connected to the master via LIN.

Usually, the master is connected to a network such as CAN (Controller Area Network).

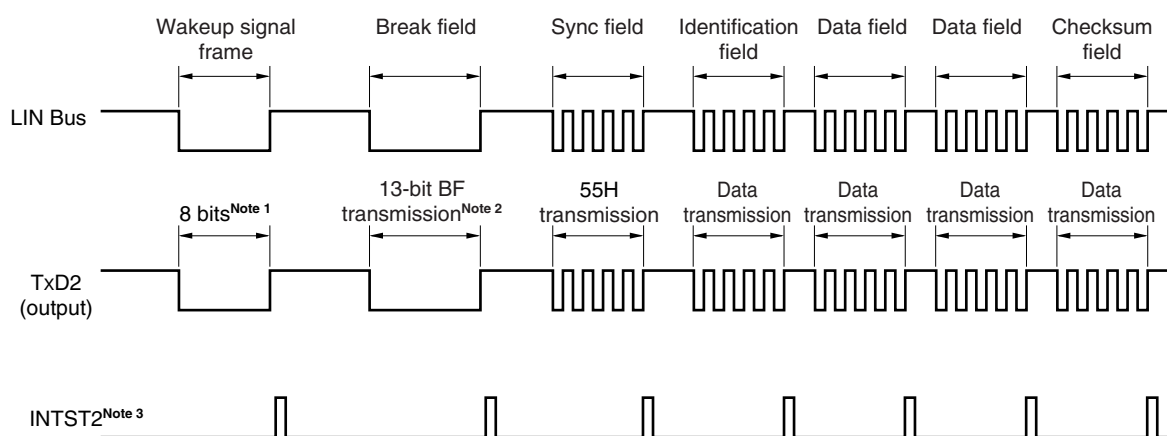
A LIN bus is a single-wire bus to which nodes are connected via transceiver conforming to ISO9141.

According to the protocol of LIN, the master transmits a frame by attaching baud rate information to it. A slave receives this frame and corrects a baud rate error from the master. If the baud rate error of a slave is within $\pm 15\%$, communication can be established.

Figure 12-99 outlines a master transmission operation of LIN.

<R>

Figure 12-99. Master Transmission Operation of LIN



Notes 1. Data of 80H is transmitted.

2. A break field is defined to have a width of 13 bits and output a low level. Where the baud rate for main transfer is N [bps], therefore, the baud rate of the break field is calculated as follows.

$$(\text{Baud rate of break field}) = 9/13 \times N$$

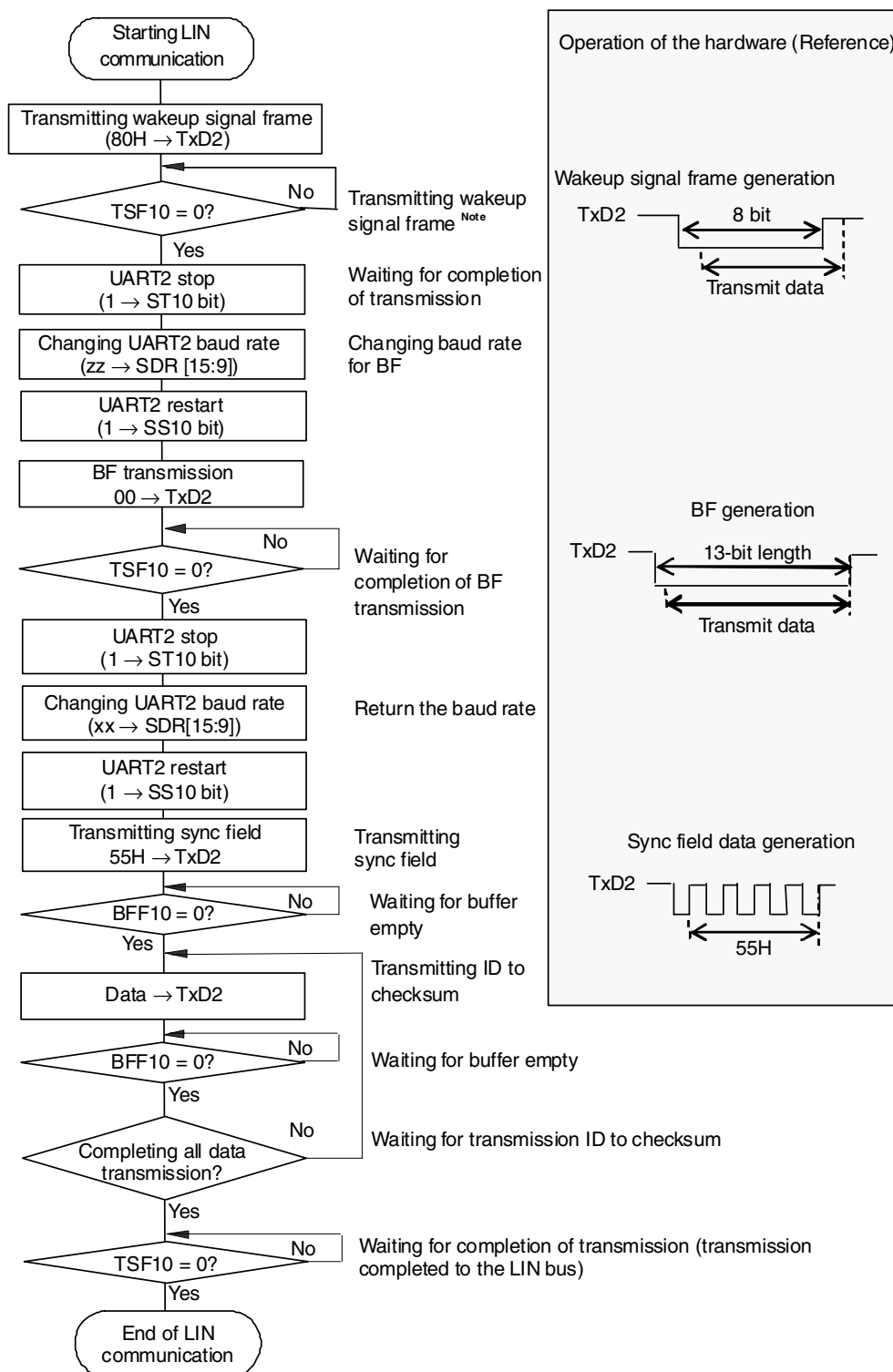
By transmitting data of 00H at this baud rate, a break field is generated.

3. INTST2 is output upon completion of transmission.

Remark The interval between fields is controlled by software.

<R>

Figure 12-100. Flowchart for LIN Transmission



Note When LIN-bus start from sleep status only

Remark Default setting of the UART is complete, and the flow from the transmission enable status.

12.7.2 LIN reception

Of UART reception, UART2 of the 32, 48, and 64-pin products support LIN communication.

For LIN reception, channel 1 of unit 1 is used.

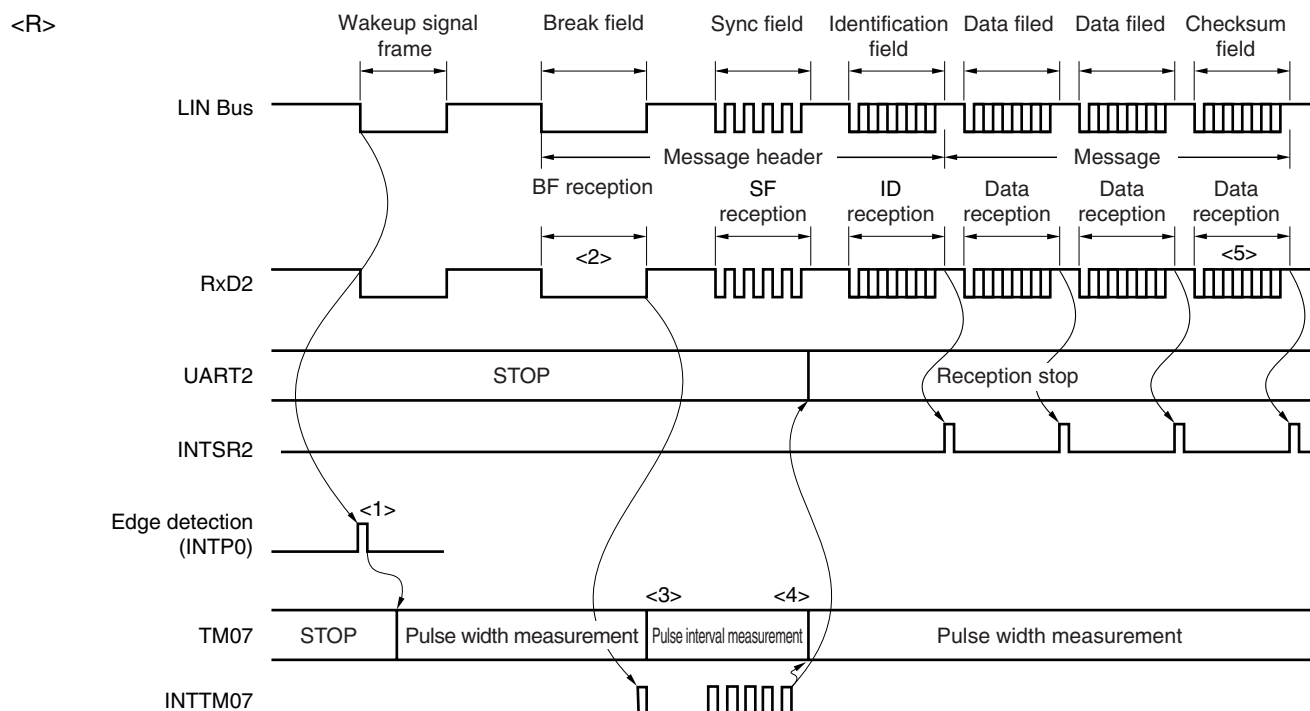
UART	UART0	UART1	UART2
Support of LIN communication	Not supported	Not supported	Supported
Target channel	–	–	Channel 1 of SAU1
Pins used	–	–	RxD2
Interrupt	–	–	INTSR2
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)		
Error interrupt	–	–	INTSRE2
Error detection flag	• Framing error detection flag (FEF11) • Parity error detection flag (PEF11) • Overrun error detection flag (OVF11)		
Transfer data length	8 bits		
<R> Transfer rate	Max. $f_{MCK}/6$ [bps] (SDR11 [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps] ^{Note}		
Data phase	Non-reverse output (default: high level) Reverse output (default: low level)		
<R> Parity bit	No parity bit (The parity bit is not checked.)		
<R> Stop bit	Check the first bit		
<R> Data direction	LSB first		

Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (T_A = –40 to +85°C) (TARGET)**, **CHAPTER 30 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = –40 to +105°C) (TARGET)**).

Remark f_{MCK} : Operation clock frequency of target channel
 f_{CLK} : System clock frequency

Figure 12-101 outlines a reception operation of LIN.

Figure 12-101. Reception Operation of LIN



Here is the flow of signal processing.

- <R>
- <1> The wakeup signal is detected by detecting an interrupt edge (INTP0) on a pin. When the wakeup signal is detected, change TM07 to pulse width measurement upon detection of the wakeup signal to measure the low-level width of the BF signal. Then wait for BF signal reception.
 - <2> TM07 starts measuring the low-level width upon detection of the falling edge of the BF signal, and then captures the data upon detection of the rising edge of the BF signal. The captured data is used to judge whether it is the BF signal.
 - <R>
 - <3> When the BF signal has been received normally, change TM07 to pulse interval measurement and measure the interval between the falling edges of the RxD2 signal in the sync field four times (see **6.7.4 Operation as input pulse interval measurement**).
 - <4> Calculate a baud rate error from the bit interval of sync field (SF). Stop UART2 once and adjust (re-set) the baud rate.
 - <5> The checksum field should be distinguished by software. In addition, processing to initialize UART2 after the checksum field is received and to wait for reception of BF should also be performed by software.

<R>

Figure 12-102. Flowchart for LIN Reception

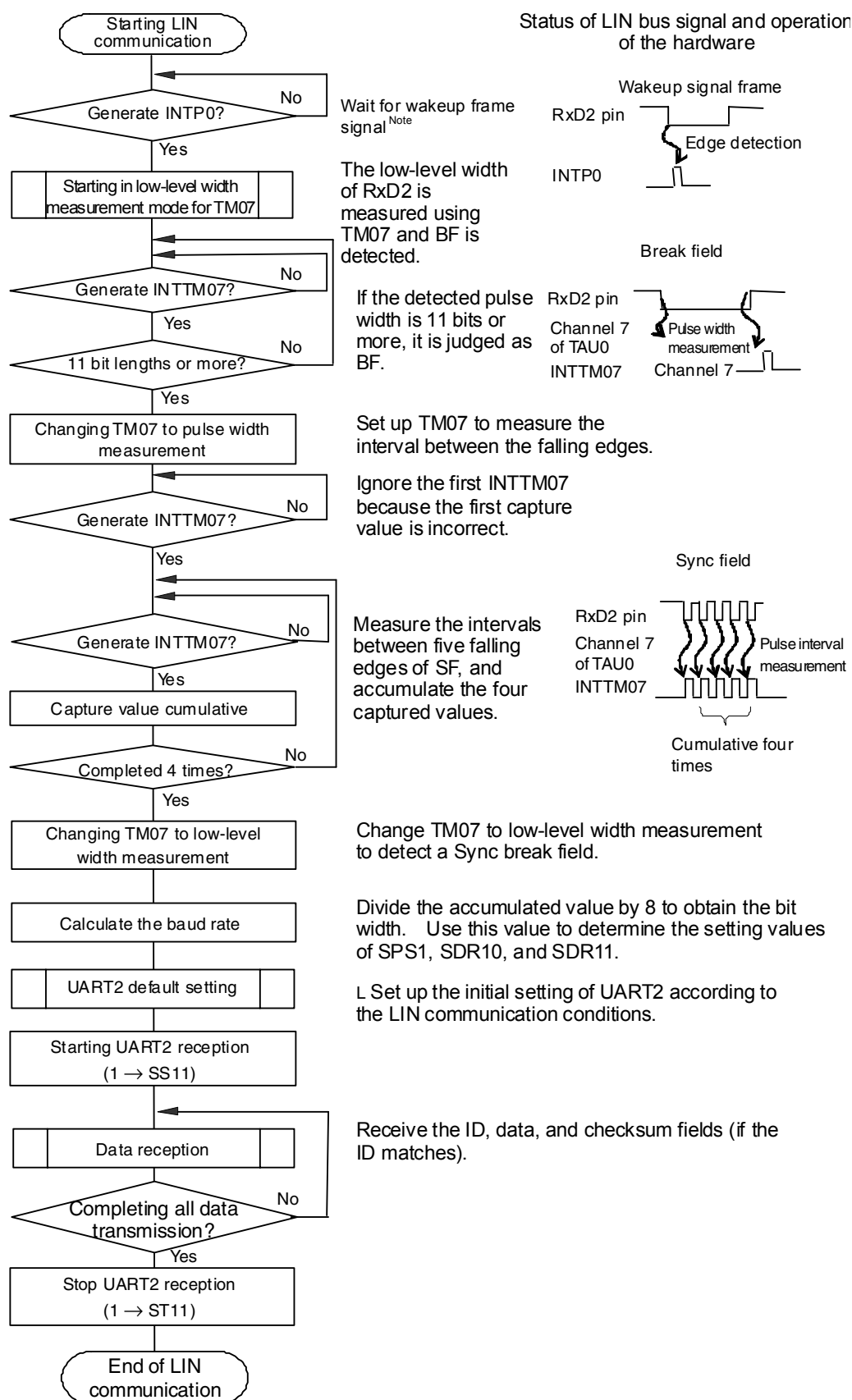
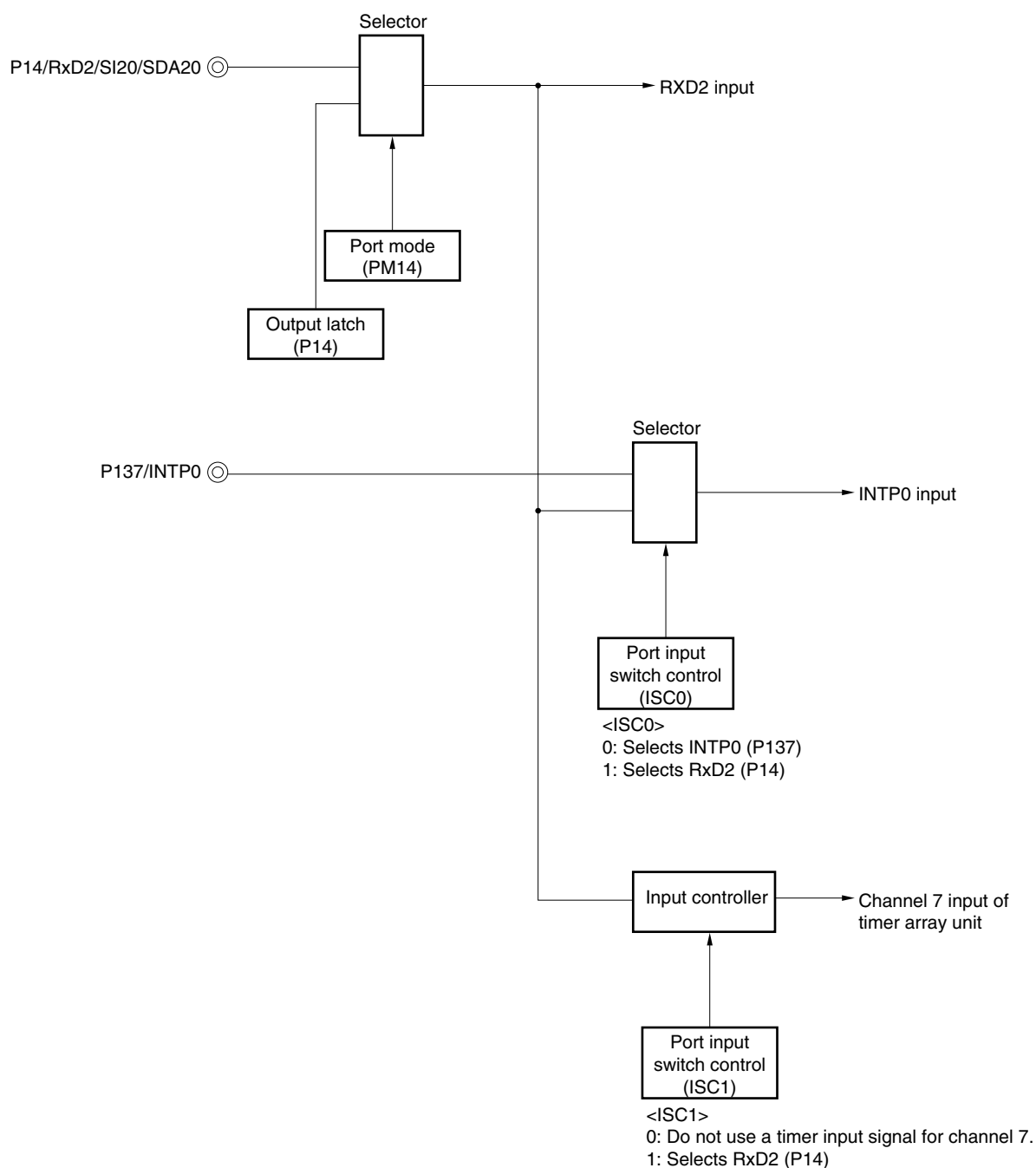
**Note** Required in the sleep status only.

Figure 12-103 and figure 12-104 show the configuration of a port that manipulates reception of LIN.

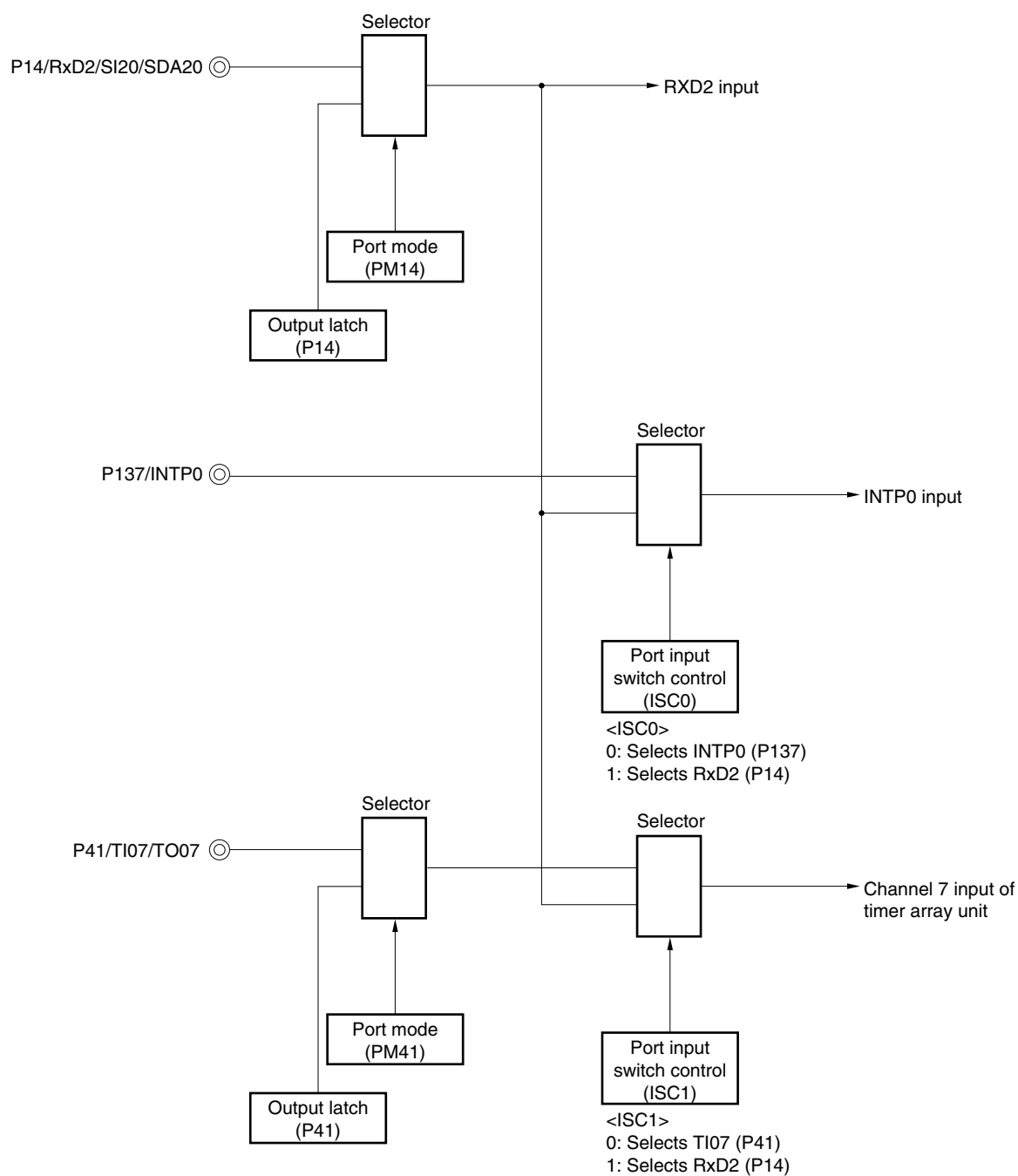
The wakeup signal transmitted from the master of LIN is received by detecting an edge of an external interrupt (INTP0). The length of the sync field transmitted from the master can be measured by using the external event capture operation of the timer array unit 0 to calculate a baud-rate error.

By controlling switch of port input (ISC0/ISC1), the input source of port input (RxD2) for reception can be input to the external interrupt pin (INTP0) and timer array unit

Figure 12-103. Port Configuration for Manipulating Reception of LIN (32-pin)



Remark ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (See **Figure 12-19**.)

Figure 12-104. Port Configuration for Manipulating Reception of LIN (48, 64-pin)

Remark ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (See **Figure 12-19**.)

The peripheral functions used for the LIN communication operation are as follows.

<Peripheral functions used>

- External interrupt (INTP0); Wakeup signal detection

Usage: To detect an edge of the wakeup signal and the start of communication

<R>

- Channel 7 of timer array unit; Baud rate error detection, break field detection.

Usage: To detect the length of the sync field (SF) and divide it by the number of bits in order to detect an error (The interval of the edge input to RxD2 is measured in the capture mode.)

Measured the low-level width, determine whether break field (BF).

- Channels 0 and 1 (UART2) of serial array unit 1 (SAU1)

12.8 Operation of Simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) Communication

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This communication function is designed to execute single communication with devices such as EEPROM, flash memory, and A/D converter, and therefore, can be used only by the master.

Operate the control registers by software for setting the start and stop conditions while observing the specifications of the I²C bus line

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function^{Note} and ACK detection function
- Data length of 8 bits
(When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Generation of start condition and stop condition for software

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- Overrun error
- ACK error

* [Functions not supported by simplified I²C]

- Slave transmission, slave reception
- Multi-master function (arbitration loss detection function)
- Wait detection function

Note When receiving the last data, ACK will not be output if 0 is written to the SOEmn (SOEm register) bit and serial communication data output is stopped. See the processing flow in **12.8.3 (2)** for details.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

The channel supporting simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) is channels 0 to 3 of SAU0 and channel 0 and 1 of SAU1.

- 25-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	–		–
	2	–	UART1	–
	3	CSI11		IIC11

- 32-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	–		–
	2	–	UART1	–
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	–		–

- 48-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	CSI01		IIC01
	2	–	UART1	–
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	CSI21		IIC21

- 64-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I ² C
0	0	CSI00	UART0	IIC00
	1	CSI01		IIC01
	2	CSI10	UART1	IIC10
	3	CSI11		IIC11
1	0	CSI20	UART2 (supporting LIN-bus)	IIC20
	1	CSI21		IIC21

Simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) performs the following four types of communication operations.

- Address field transmission (See **12.8.1.**)
- Data transmission (See **12.8.2.**)
- Data reception (See **12.8.3.**)
- Stop condition generation (See **12.8.4.**)

12.8.1 Address field transmission

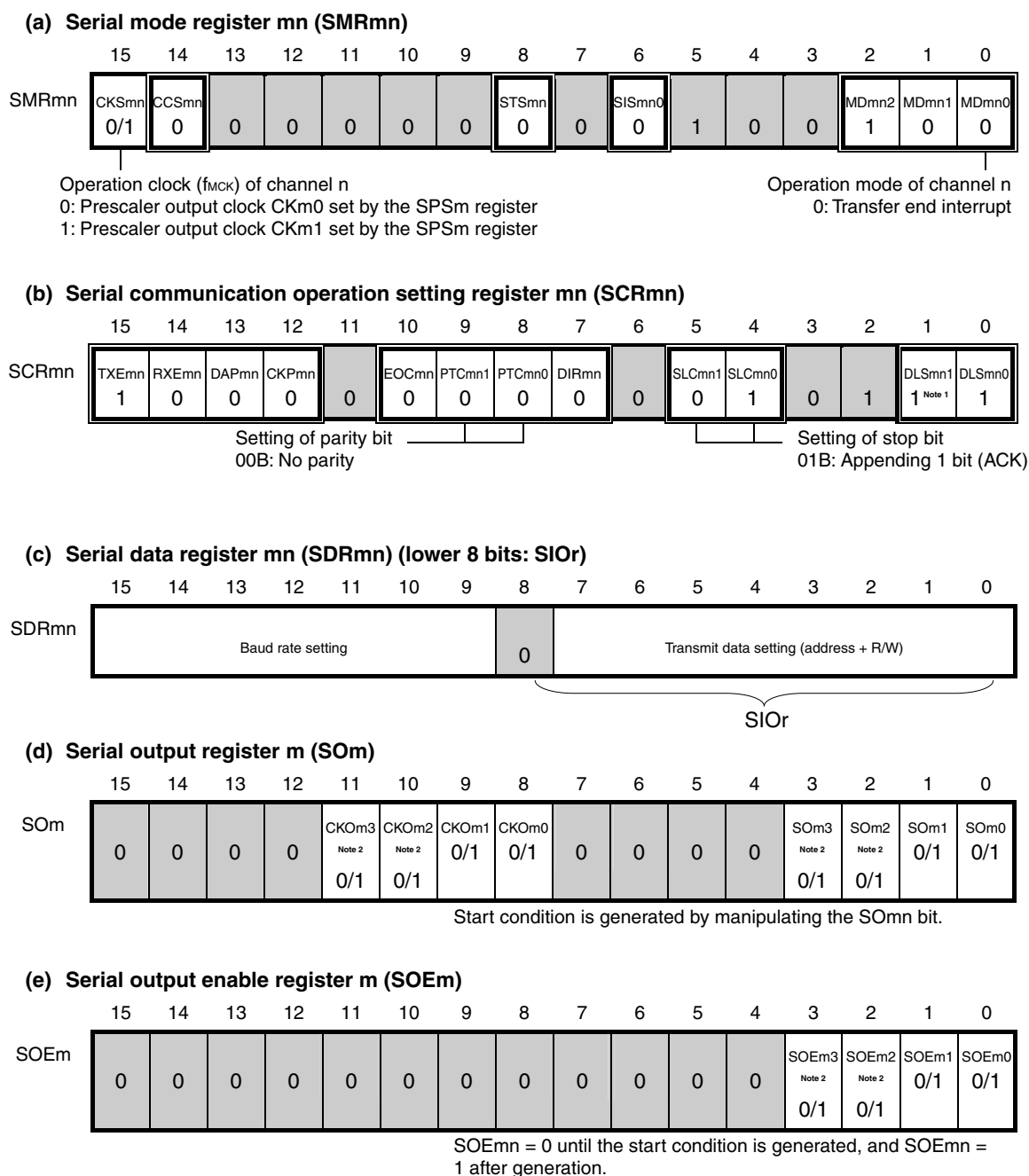
Address field transmission is a transmission operation that first executes in I²C communication to identify the target for transfer (slave). After a start condition is generated, an address (7 bits) and a transfer direction (1 bit) are transmitted in one frame.

Simplified I ² C	IIC00	IIC01	IIC10	IIC11	IIC20	IIC21
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1	Channel 1 of SAU1
Pins used	SCL00, SDA00 ^{Note}	SCL01, SDA01 ^{Note}	SCL10, SDA10 ^{Note}	SCL11, SDA11 ^{Note}	SCL20, SDA20 ^{Note}	SCL21, SDA21 ^{Note}
Interrupt	INTIIC00	INTIIC01	INTIIC10	INTIIC11	INTIIC20	INTIIC21
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)					
Error detection flag	ACK error detection flag (PEFmn)					
Transfer data length	8 bits (transmitted with specifying the higher 7 bits as address and the least significant bit as R/W control)					
<R> Transfer rate	Max. $f_{MCK}/4$ [Hz] ($SDRmn[15:9] = 1$ or more) f_{MCK} : Operation clock frequency of target channel However, the following condition must be satisfied in each mode of I ² C. • Max. 1 MHz (first mode plus) • Max. 400 kHz (first mode) • Max. 100 kHz (standard mode)					
Data level	Non-reversed output (default: high level)					
Parity bit	No parity bit					
Stop bit	Appending 1 bit (or ACK reception timing)					
Data direction	MSB first					

Note To perform communication via simplified I²C, set the N-ch open-drain output (V_{DD} tolerance (25 to 48-pin products/ EV_{DD} tolerance (64-pin products)) mode (POM03, POM11, POM14 = 1) for the port output mode registers (POM0, POM1) (see **4.3 Registers Controlling Port Function** for details). When IIC00, IIC10, IIC20 communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance (25 to 48-pin products/ EV_{DD} tolerance (64-pin products)) mode (POM04, POM10, POM15 = 1) also for the clock input/output pins (SCL00, SCL10, SCL20) (see **4.4.4 Connecting to external device with different potential (1.8 V, 2.5 V)** for details).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

(1) Register setting

Figure 12-105. Example of Contents of Registers for Address Field Transmission of Simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) (1/2)

Notes 1. Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.

2. Unit 0 only

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

2. : Setting is fixed in the IIC mode, : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

Figure 12-105. Example of Contents of Registers for Address Field Transmission of Simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) (2/2)

(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel is 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 0/1	SSm2 Note 0/1	SSm1 0/1	SSm0 0/1

Note Unit 0 only

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21),
mn = 00 to 03, 10, 11

2.  : Setting disabled (set to the initial value)

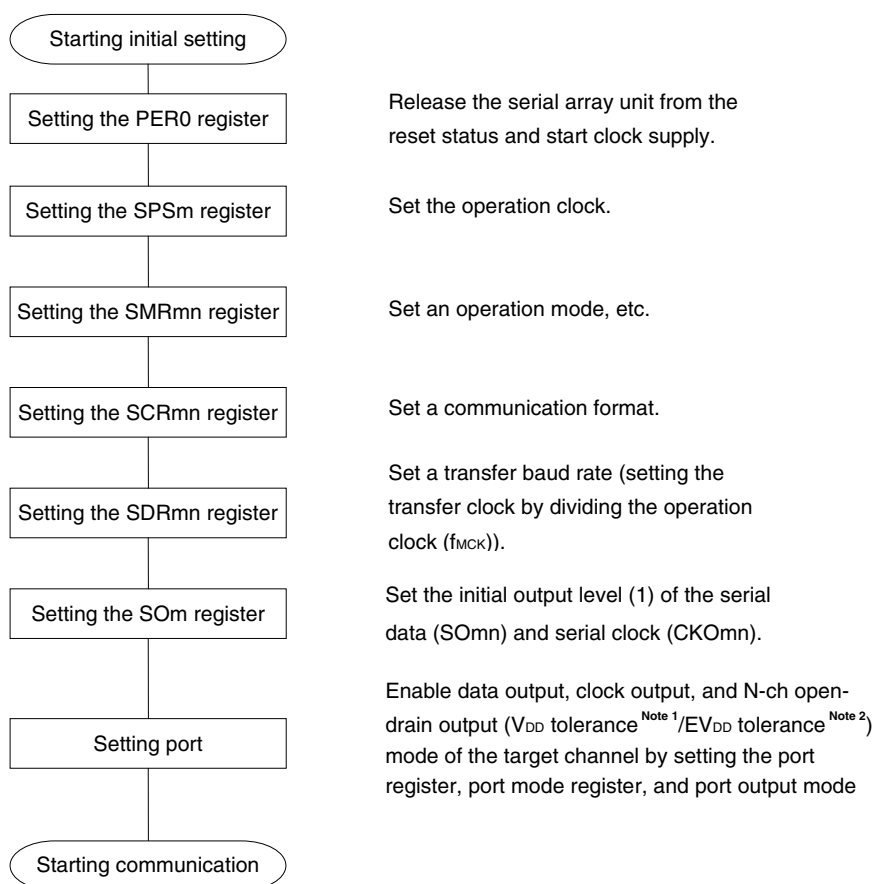
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

<R>

Figure 12-106. Initial Setting Procedure for Address Field Transmission

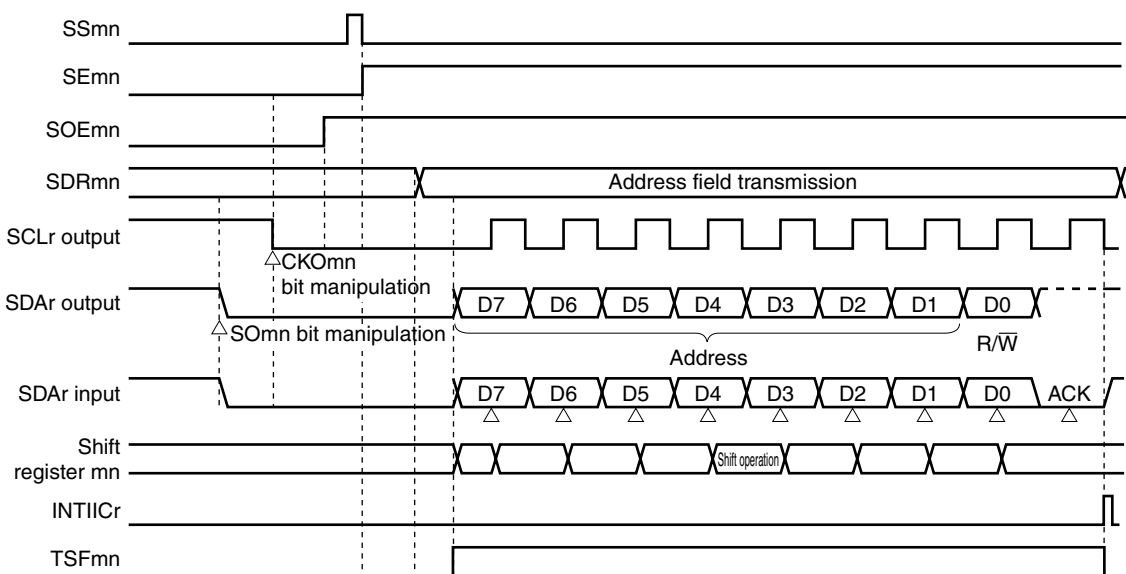
**Notes** 1. 25 to 48pin products

2. 64-pin products

Remarks 1. At the end of the initial setting, the simplified I2C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) must be set so that output is disabled and operations are stopped.2. m: Unit number ($m = 0, 1$), n: Channel number ($n = 0$ to 3), mn = 00 to 03, 10, 11

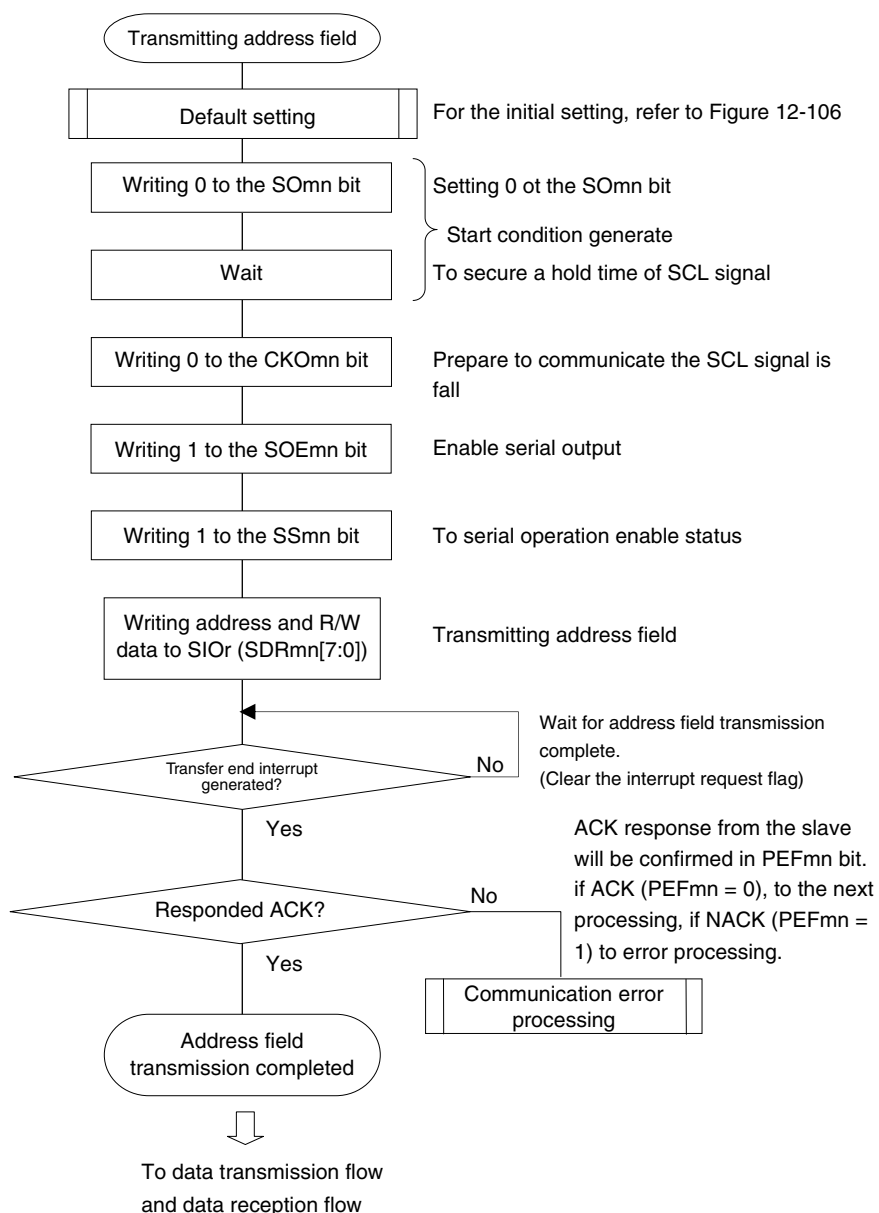
(3) Processing flow

Figure 12-107. Timing Chart of Address Field Transmission



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

<R>

Figure 12-108. Flowchart of Address Field Transmission

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

12.8.2 Data transmission

Data transmission is an operation to transmit data to the target for transfer (slave) after transmission of an address field. After all data are transmitted to the slave, a stop condition is generated and the bus is released.

<R>

Simplified I ² C	IIC00	IIC01	IIC10	IIC11	IIC20	IIC21
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1	Channel 1 of SAU1
Pins used	SCL00, SDA00 ^{Note}	SCL01, SDA01 ^{Note}	SCL10, SDA10 ^{Note}	SCL11, SDA11 ^{Note}	SCL20, SDA20 ^{Note}	SCL21, SDA21 ^{Note}
Interrupt	INTIIC00	INTIIC01	INTIIC10	INTIIC11	INTIIC20	INTIIC21
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)					
Error detection flag	ACK error detection flag (PEFmn)					
Transfer data length	8 bits					
Transfer rate	Max. $f_{MCK}/4$ [Hz] ($SDRmn[15:9] = 1$ or more) f_{MCK} : Operation clock frequency of target channel However, the following condition must be satisfied in each mode of I ² C. • Max. 1 MHz (first mode plus) • Max. 400 kHz (first mode) • Max. 100 kHz (standard mode)					
Data level	Forward output (default: high level)					
Parity bit	No parity bit					
Stop bit	Appending 1 bit (for ACK reception timing)					
Data direction	MSB first					

Note To perform communication via simplified I²C, set the N-ch open-drain output (V_{DD} tolerance (25 to 48-pin products/ EV_{DD} tolerance (64-pin products)) mode (POM03, POM11, POM14 = 1) for the port output mode registers (POM0, POM1) (see **4.3 Registers Controlling Port Function** for details). When IIC00, IIC10, IIC20 communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance (25 to 48-pin products/ EV_{DD} tolerance (64-pin products)) mode (POM04, POM10, POM15 = 1) also for the clock input/output pins (SCL00, SCL10, SCL20) (see **4.4.4 Connecting to external device with different potential (1.8 V, 2.5 V)** for details).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

(1) Register setting

<R>

Figure 12-109. Example of Contents of Registers for Data Transmission of Simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) (1/2)

(a) Serial mode register mn (SMRmn) ... Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn 0/1	CCSmn 0	0	0	0	0	0	STSmn 0	0	SISmn0 0	1	0	0	MDmn2 1	MDmn1 0	MDmn0 0

(b) Serial communication operation setting register mn (SCRmn) ... Do not manipulate the bits of this register, except the TXEmn and RXEmn bits, during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn 1	RXEmn 0	DAPmn 0	CKPmn 0	0	EOCmn 0	PTCmn1 0	PTCmn0 0	DIRmn 0	0	SLCmn1 0	SLCmn0 1	0	1	DLSmn1 1 Note 1	DLSmn0 1

(c) Serial data register mn (SDRmn) (lower 8 bits: SIOr) ... During data transmission/reception, valid only lower 8-bits (SIOr)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	Baud rate setting ^{Note 2}							0	Transmit data setting							
SIOr																

(d) Serial output register m (SOM) ... Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOM	0	0	0	0	CKOm3 Note 3 0/1 Note 4	CKOm2 Note 3 0/1 Note 4	CKOm1 0/1 Note 4	CKOm0 0/1 Note 4	0	0	0	0	SOM3 Note 3 0/1 Note 4	SOM2 Note 3 0/1 Note 4	SOM1 0/1 Note 4	SOM0 0/1 Note 4

- Notes**
1. Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.
 2. Because the setting is completed by address field transmission, setting is not required.
 3. Unit 0 only.
 4. The value varies depending on the communication data during communication operation.

- Remarks**
1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11
 2. : Setting is fixed in the IIC mode, : Setting disabled (set to the initial value)
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
 0/1: Set to 0 or 1 depending on the usage of the user

Figure 12-109. Example of Contents of Registers for Data Transmission of Simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) (2/2)

(e) Serial output enable register m (SOEm) ... Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOEm3 Note 1	SOEm2 Note 1	SOEm1 1	SOEm0 1

(f) Serial channel start register m (SSm) ... Do not manipulate this register during data transmission/reception.

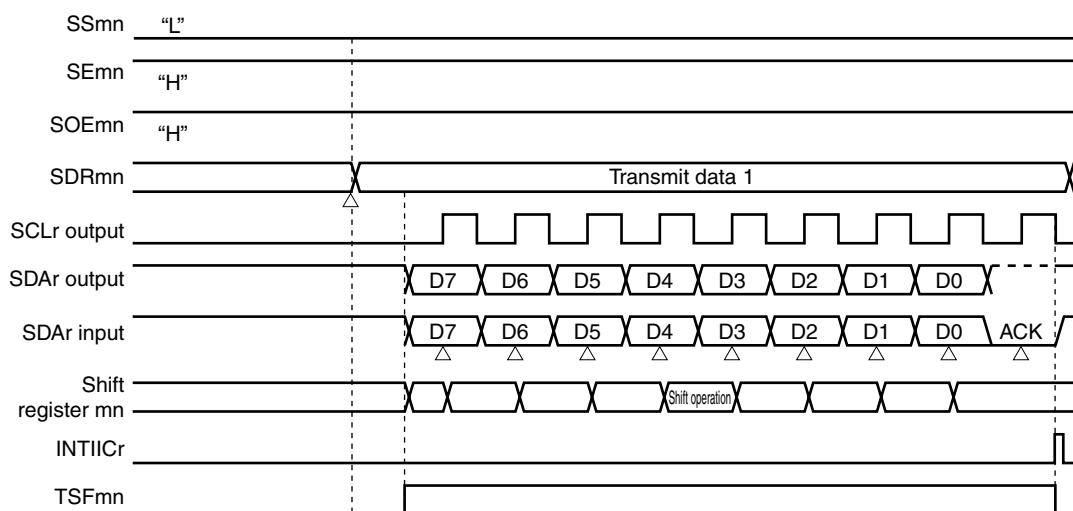
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 0/1	SSm2 Note 0/1	SSm1 0/1	SSm0 0/1

Note Unit 0 only.

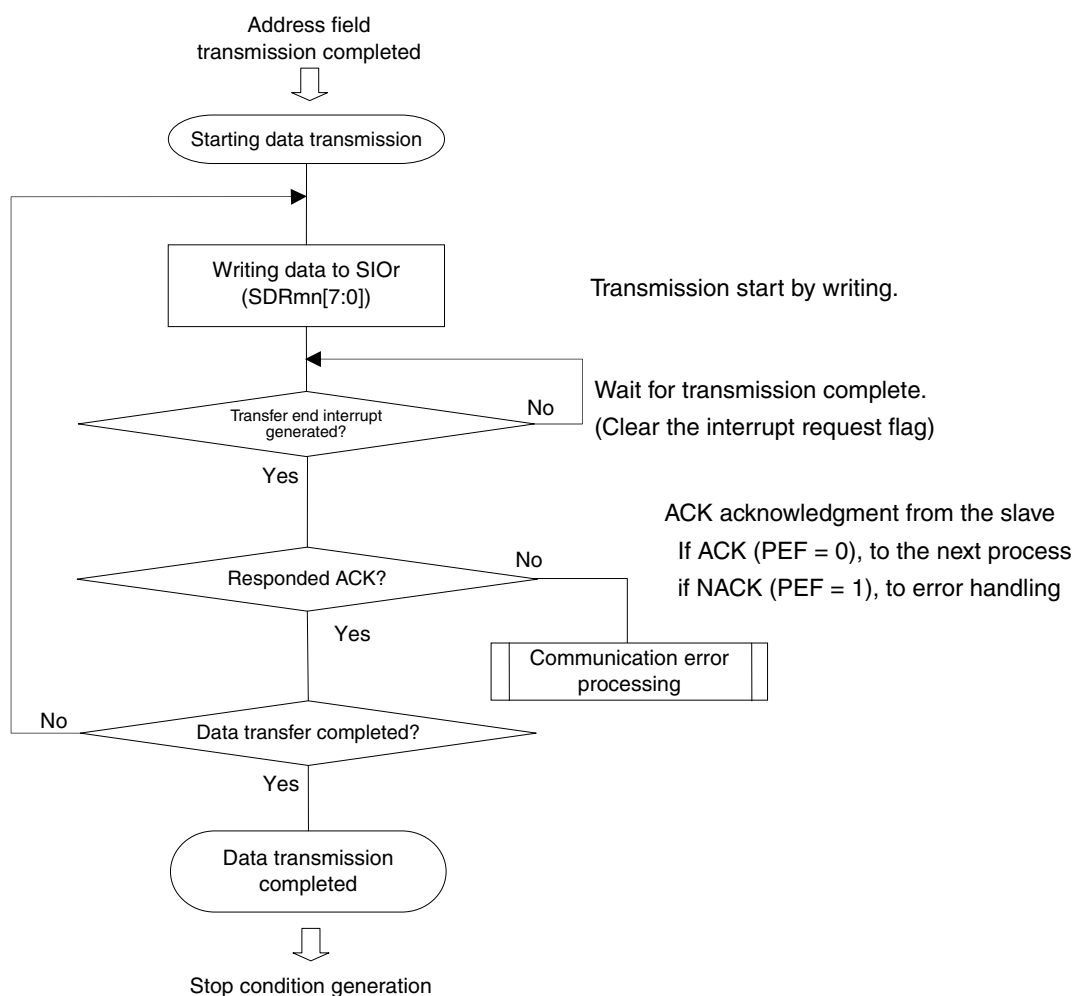
- Remarks**
- m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11
 - : Setting disabled (set to the initial value)
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
 0/1: Set to 0 or 1 depending on the usage of the user

(2) Processing flow

Figure 12-110. Timing Chart of Data Transmission



<R>

Figure 12-111. Flowchart of Simplified I²C Data Transmission

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

12.8.3 Data reception

Data reception is an operation to receive data to the target for transfer (slave) after transmission of an address field. After all data are received to the slave, a stop condition is generated and the bus is released.

<R>

Simplified I ² C	IIC00	IIC01	IIC10	IIC11	IIC20	IIC21
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1	Channel 1 of SAU1
Pins used	SCL00, SDA00 ^{Note}	SCL01, SDA01 ^{Note}	SCL10, SDA10 ^{Note}	SCL11, SDA11 ^{Note}	SCL20, SDA20 ^{Note}	SCL21, SDA21 ^{Note}
Interrupt	INTIIC00	INTIIC01	INTIIC10	INTIIC11	INTIIC20	INTIIC21
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	8 bits					
Transfer rate	Max. $f_{MCK}/4$ [Hz] ($SDRmn[15:9] = 1$ or more) f_{MCK} : Operation clock frequency of target channel However, the following condition must be satisfied in each mode of I ² C. • Max. 1 MHz (first mode plus) • Max. 400 kHz (first mode) • Max. 100 kHz (standard mode)					
Data level	Non-reversed output (default: high level)					
Parity bit	No parity bit					
Stop bit	Appending 1 bit (ACK transmission)					
Data direction	MSB first					

Note To perform communication via simplified I²C, set the N-ch open-drain output (V_{DD} tolerance (25 to 48-pin products/ EV_{DD} tolerance (64-pin products)) mode (POM03, POM11, POM14 = 1) for the port output mode registers (POM0, POM1) (see **4.3 Registers Controlling Port Function** for details). When IIC00, IIC10, IIC20 communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance (25 to 48-pin products/ EV_{DD} tolerance (64-pin products)) mode (POM04, POM10, POM15 = 1) also for the clock input/output pins (SCL00, SCL10, SCL20) (see **4.4.4 Connecting to external device with different potential (1.8 V, 2.5 V)** for details).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

(1) Register setting

Figure 12-112. Example of Contents of Registers for Data Reception of Simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) (1/2)

(a) Serial mode register mn (SMRmn) ... Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn 0/1	CCSmn 0	0	0	0	0	0	STSmn 0	0	SISmn0 0	1	0	0	MDmn2 1	MDmn1 0	MDmn0 0

(b) Serial communication operation setting register mn (SCRmn) ... Do not manipulate the bits of this register, except the TXEmn and RXEmn bits, during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn 0	RXEmn 1	DAPmn 0	CKPmn 0	0	EOCmn 0	PTCmn1 0	PTCmn0 0	DIRmn 0	0	SLCmn1 0	SLCmn0 1	0	1	DLSmn1 1	DLSmn0 1

(c) Serial data register mn (SDRmn) (lower 8 bits: SIO_r)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	Baud rate setting ^{Note 2}							0	Dummy transmit data setting (FFH)							
									SIO _r							

(d) Serial output register m (SOM) ... Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOM	0	0	0	0	CKOm3 Note 3 0/1 Note 4	CKOm2 Note 3 0/1 Note 4	CKOm1 0/1 Note 4	CKOm0 0/1 Note 4	0	0	0	0	SOM3 Note 3 0/1 Note 4	SOM2 Note 3 0/1 Note 4	SOM1 0/1 Note 4	SOM0 0/1 Note 4

- Notes**
1. Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.
 2. The baud rate setting is not required because the baud rate has already been set when the address field was transmitted.
 3. Unit 0 only.
 4. The value varies depending on the communication data during communication operation.

- Remarks**
1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11
 2. ☐: Setting is fixed in the IIC mode, ☐: Setting disabled (set to the initial value)
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
 0/1: Set to 0 or 1 depending on the usage of the user

Figure 12-112. Example of Contents of Registers for Data Reception of Simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) (2/2)

(e) Serial output enable register m (SOEm) ... Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOEm3 Note 0/1	SOEm2 Note 0/1	SOEm1 0/1	SOEm0 0/1

(f) Serial channel start register m (SSm) ... Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 Note 0/1	SSm2 Note 0/1	SSm1 0/1	SSm0 0/1

Note Unit 0 only

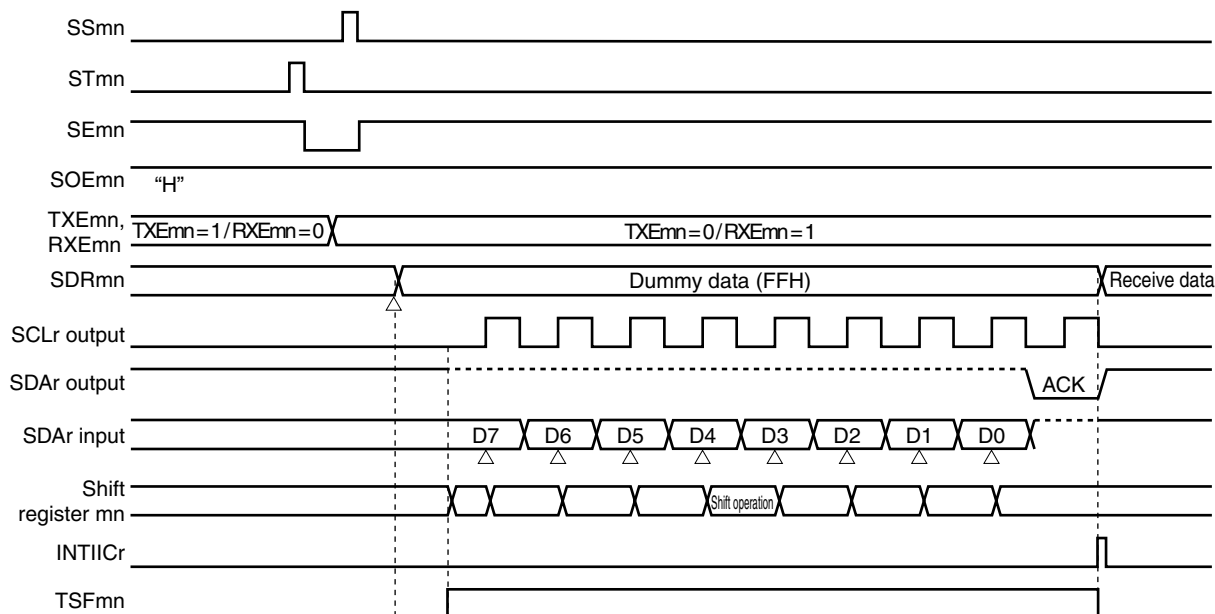
Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

2. ☐: Setting is fixed in the CSI master transmission mode, ☐: Setting disabled (set to the initial value)
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
 0/1: Set to 0 or 1 depending on the usage of the user

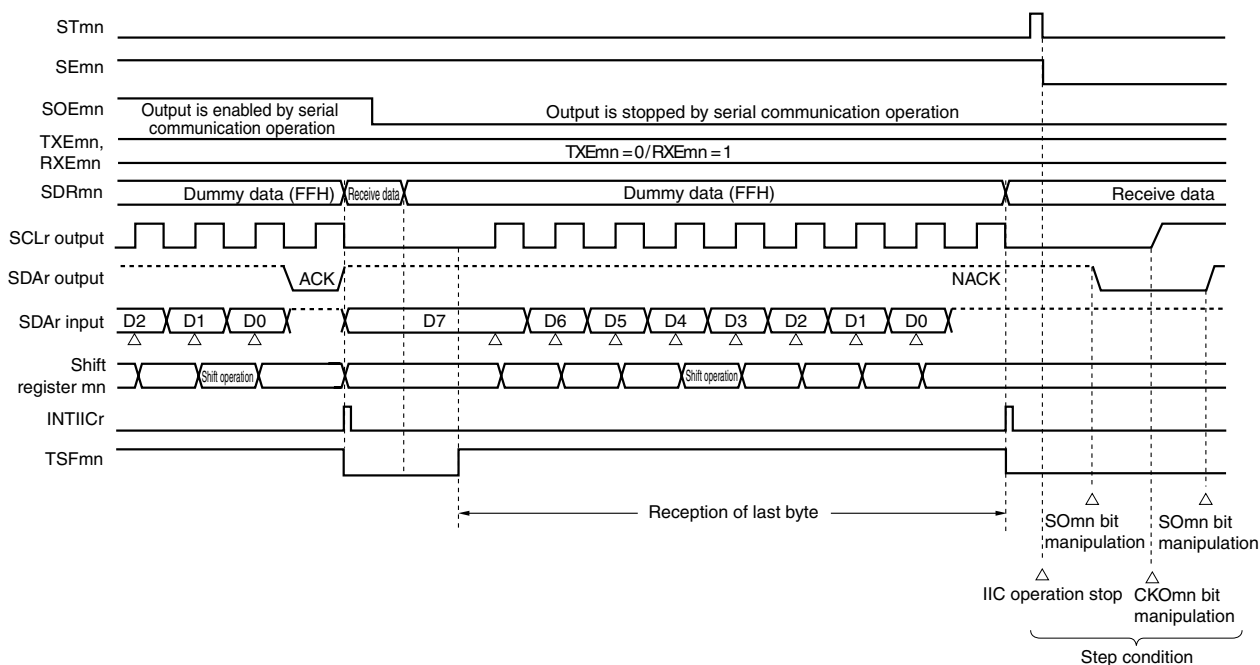
(2) Processing flow

Figure 12-113. Timing Chart of Data Reception

(a) When starting data reception

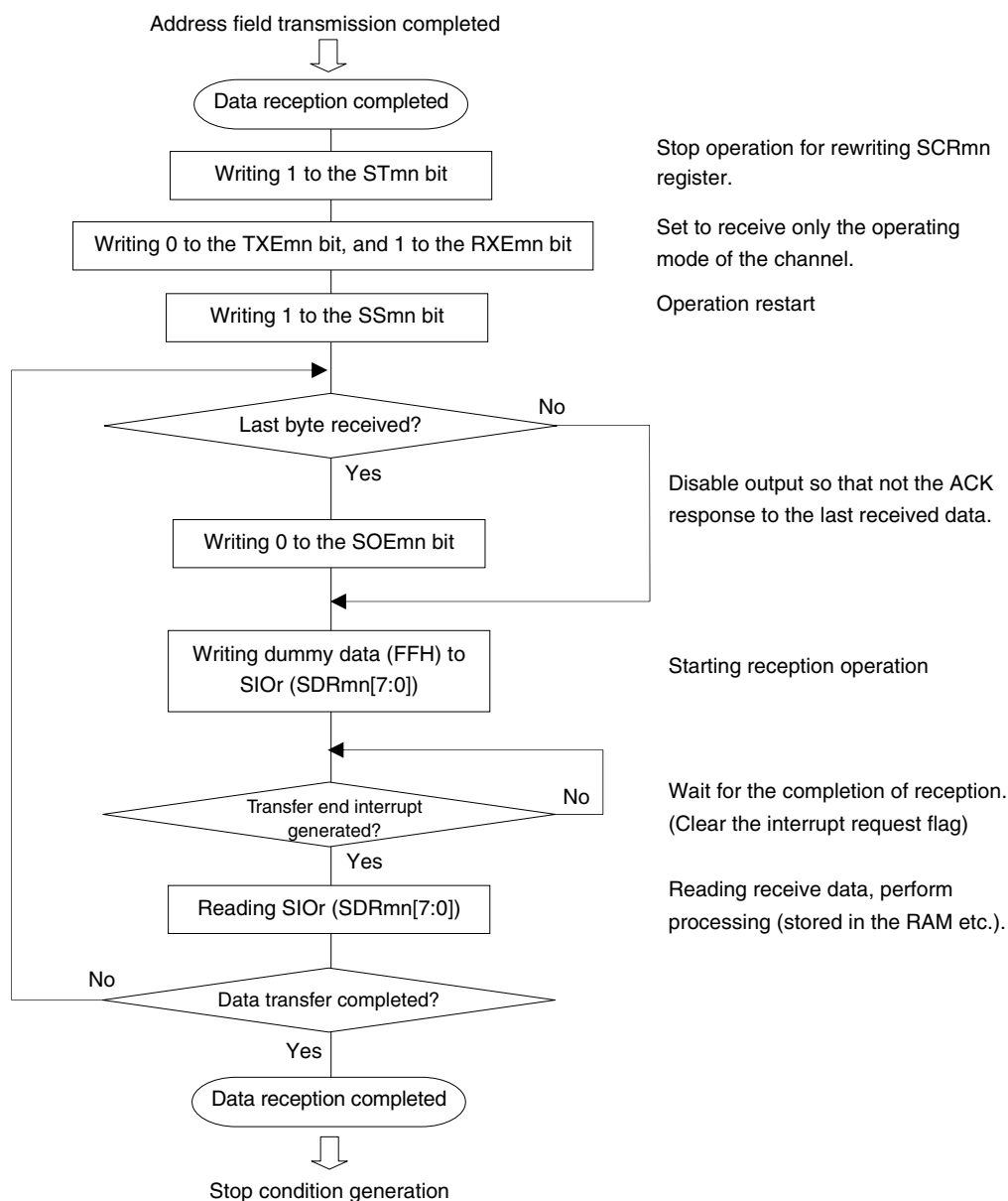


(b) When receiving last data



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

<R>

Figure 12-114. Flowchart of Data Reception

Caution ACK is not output when the last data is received (NACK). Communication is then completed by setting “1” to the STmn bit of serial channel stop register m (STm) to stop operation and generating a stop condition.

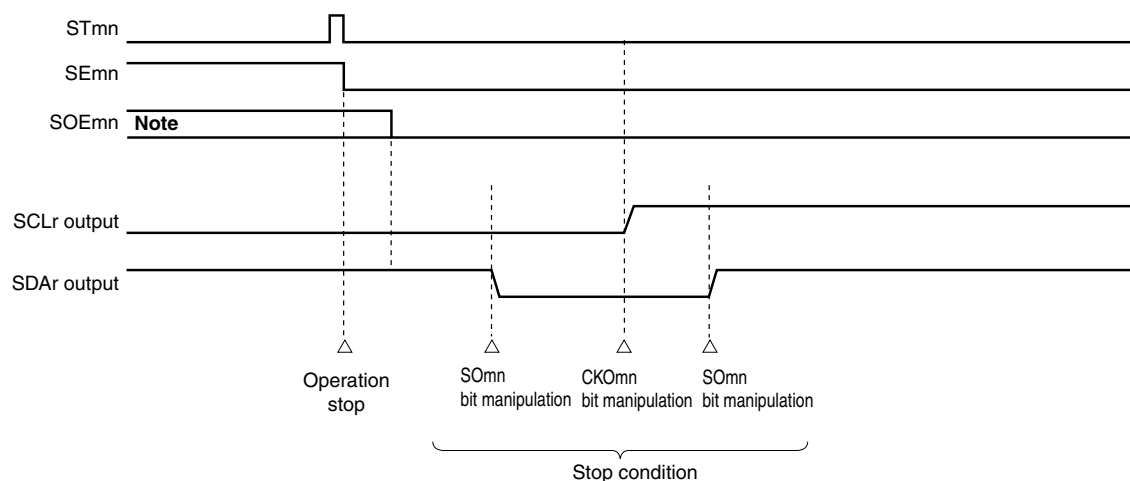
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

12.8.4 Stop condition generation

After all data are transmitted to or received from the target slave, a stop condition is generated and the bus is released.

(1) Processing flow

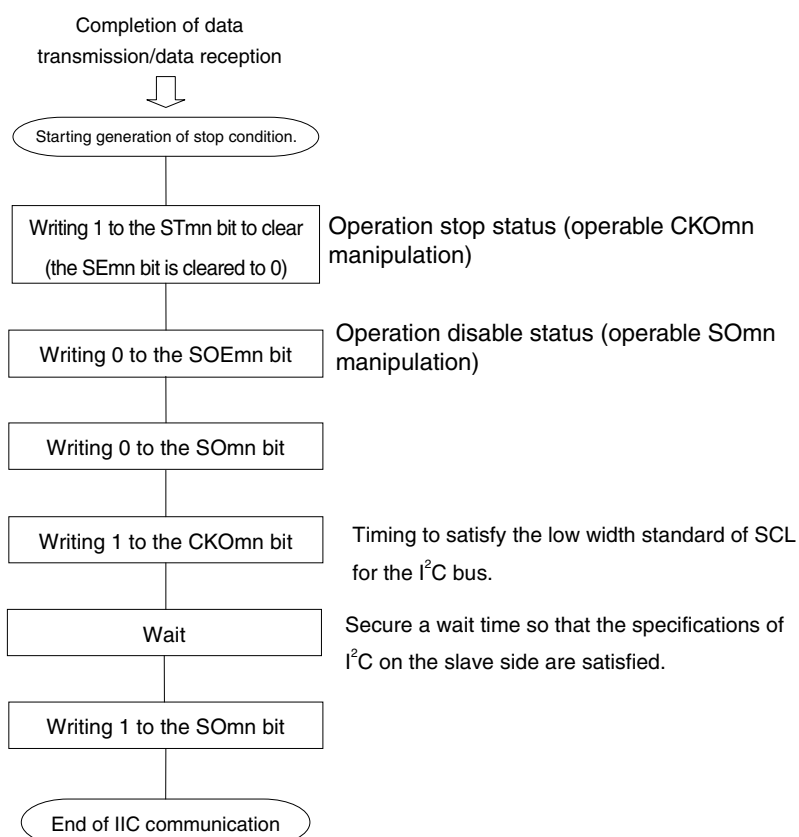
Figure 12-115. Timing Chart of Stop Condition Generation



Note During a receive operation, the SOEmn bit of serial output enable register m (SOEm) is cleared to 0 before receiving the last data.

<R>

Figure 12-116. Flowchart of Stop Condition Generation



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21), mn = 00 to 03, 10, 11

12.8.5 Calculating transfer rate

The transfer rate for simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) communication can be calculated by the following expressions.

$$(\text{Transfer rate}) = \{\text{Operation clock (f}_{\text{MCK}}) \text{ frequency of target channel}\} \div (\text{SDRmn}[15:9] + 1) \div 2$$

<R>

Caution SDRmn[15:9] must not be set to 00000000B. Be sure to set a value of 00000001B or greater for SDRmn[15:9]. The duty ratio of the SCL signal output by the simplified I2C is 50%. The I2C bus specifications define that the low-level width of the SCL signal is longer than the high-level width. If 400 kbps (fast mode) or 1 Mbps (fast mode plus) is specified, therefore, the low-level width of the SCL output signal becomes shorter than the value specified in the I2C bus specifications. Make sure that the SDRmn[15:9] value satisfies the I2C bus specifications.

- Remarks**
1. The value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000001B to 1111111B) and therefore is 1 to 127.
 2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 12-4. Selection of Operation Clock For Simplified I²C

SMRmn Register	SPSm Register								Operation Clock (fMCK) ^{Note}	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		fCLK = 32 MHz
0	X	X	X	X	0	0	0	0	fCLK	32 MHz
	X	X	X	X	0	0	0	1	fCLK/2	16 MHz
	X	X	X	X	0	0	1	0	fCLK/2 ²	8 MHz
	X	X	X	X	0	0	1	1	fCLK/2 ³	4 MHz
	X	X	X	X	0	1	0	0	fCLK/2 ⁴	2 MHz
	X	X	X	X	0	1	0	1	fCLK/2 ⁵	1 MHz
	X	X	X	X	0	1	1	0	fCLK/2 ⁶	500 kHz
	X	X	X	X	0	1	1	1	fCLK/2 ⁷	250 kHz
	X	X	X	X	1	0	0	0	fCLK/2 ⁸	125 kHz
	X	X	X	X	1	0	0	1	fCLK/2 ⁹	62.5 kHz
	X	X	X	X	1	0	1	0	fCLK/2 ¹⁰	31.25 kHz
	X	X	X	X	1	0	1	1	fCLK/2 ¹¹	15.63 kHz
1	0	0	0	0	X	X	X	X	fCLK	32 MHz
	0	0	0	1	X	X	X	X	fCLK/2	16 MHz
	0	0	1	0	X	X	X	X	fCLK/2 ²	8 MHz
	0	0	1	1	X	X	X	X	fCLK/2 ³	4 MHz
	0	1	0	0	X	X	X	X	fCLK/2 ⁴	2 MHz
	0	1	0	1	X	X	X	X	fCLK/2 ⁵	1 MHz
	0	1	1	0	X	X	X	X	fCLK/2 ⁶	500 kHz
	0	1	1	1	X	X	X	X	fCLK/2 ⁷	250 kHz
	1	0	0	0	X	X	X	X	fCLK/2 ⁸	125 kHz
	1	0	0	1	X	X	X	X	fCLK/2 ⁹	62.5 kHz
	1	0	1	0	X	X	X	X	fCLK/2 ¹⁰	31.25 kHz
	1	0	1	1	X	X	X	X	fCLK/2 ¹¹	15.63 kHz
Other than above									Setting prohibited	

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

Remarks 1. X: Don't care

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

Here is an example of setting an I²C transfer rate where f_{MCK} = f_{CLK} = 32 MHz.

I ² C Transfer Mode (Desired Transfer Rate)	f _{CLK} = 32 MHz			
	Operation Clock (f _{MCK})	SDRmn[15:9]	Calculated Transfer Rate	Error from Desired Transfer Rate
100 kHz	f _{CLK} /2	79	100 kHz	0.0%
400 kHz	f _{CLK}	41	380 kHz	5.0% ^{Note}
1 MHz	f _{CLK} /2	18	0.84 MHz	16.0% ^{Note}

Note The error cannot be set to about 0% because the duty ratio of the SCL signal is 50%.

12.8.6 Procedure for processing errors that occurred during simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) communication

The procedure for processing errors that occurred during simplified I²C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) communication is described in Figure 12-117 and 12-118.

Figure 12-117. Processing Procedure in Case of Overrun Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

Figure 12-118. Processing Procedure in Case of Parity Error (ACK error) in Simplified I²C Mode

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.
Sets the STmn bit of serial channel stop register m (STm) to 1. →	The SEMn bit of serial channel enable status register m (SEm) is set to 0 and channel n stops operation.	Slave is not ready for reception because ACK is not returned. Therefore, a stop condition is created, the bus is released, and communication is started again from the start condition. Or, a restart condition is generated and transmission can be redone from address transmission.
Creates stop condition.		
Creates start condition.		
Sets the SSmn bit of serial channel start register m (SSm) to 1. →	The SEMn bit of serial channel enable status register m (SEm) is set to 1 and channel n is enabled to operate.	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), r: IIC number (r = 00, 01, 10, 11, 20, 21)
mn = 00 to 03, 10, 11

CHAPTER 13 SERIAL INTERFACE IICA

13.1 Functions of Serial Interface IICA

Serial interface IICA has the following three modes.

(1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

(2) I²C bus mode (multimaster supported)

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLA0) line and a serial data bus (SDAA0) line.

This mode complies with the I²C bus format and the master device can generate “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I²C bus.

Since the SCLA0 and SDAA0 pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.

(3) Wakeup mode

The STOP mode can be released by generating an interrupt request signal (INTIICA0) when an extension code from the master device or a local address has been received while in STOP mode. This can be set by using the WUP0 bit of IICA control register 01 (IICCTL01).

Figure 13-1 shows a block diagram of serial interface IICA.

Figure 13-1. Block Diagram of Serial Interface IICA

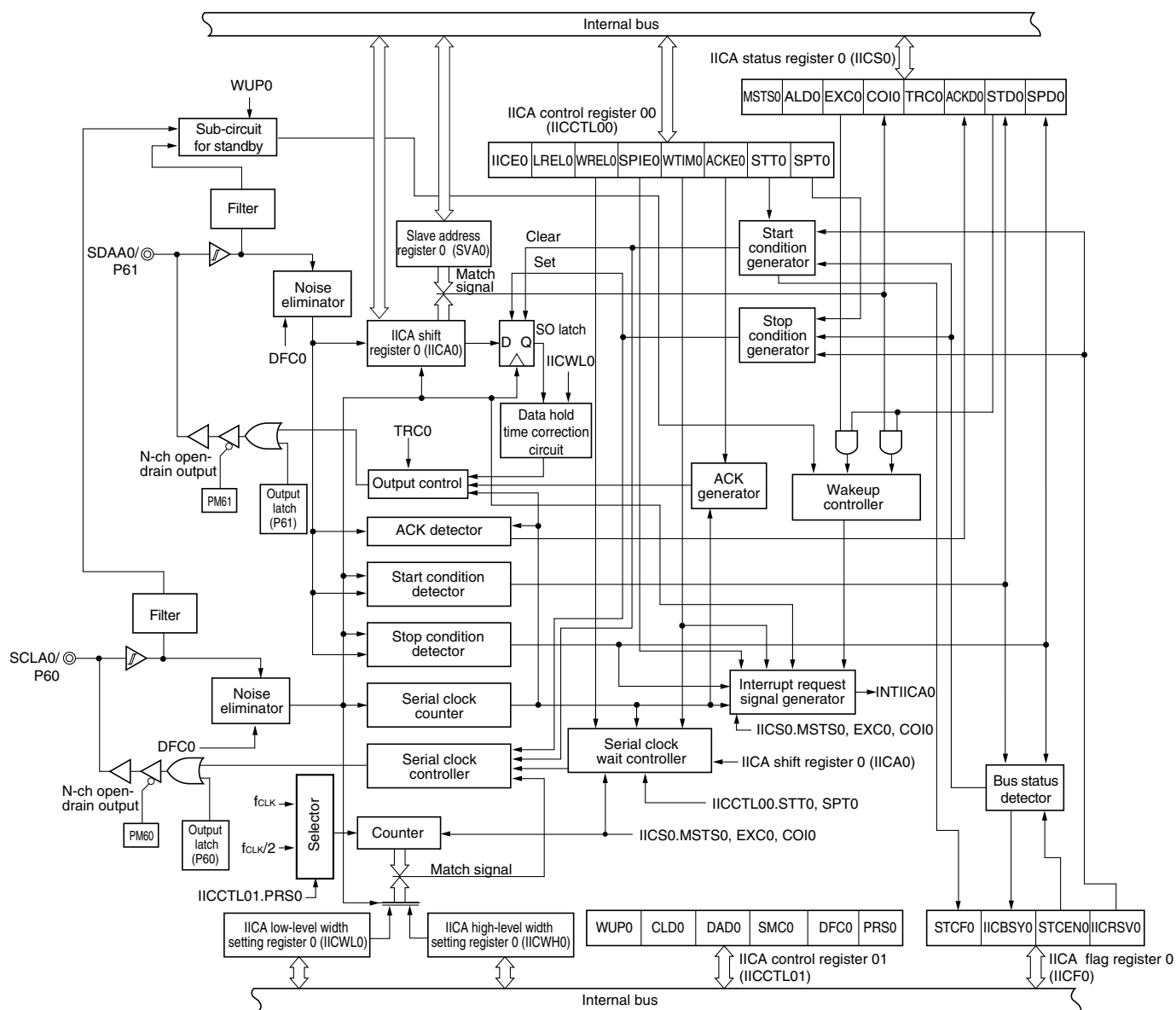
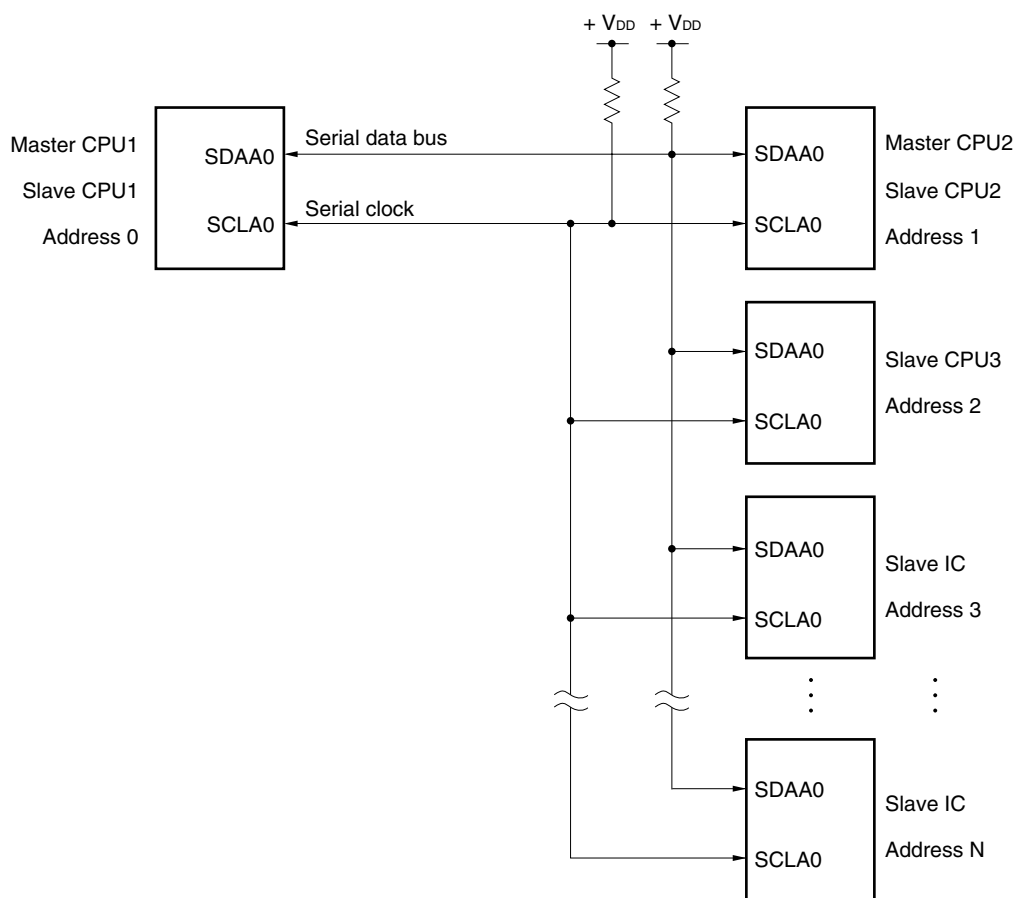


Figure 13-2 shows a serial bus configuration example.

Figure 13-2. Serial Bus Configuration Example Using I²C Bus



13.2 Configuration of Serial Interface IICA

Serial interface IICA includes the following hardware.

Table 13-1. Configuration of Serial Interface IICA

Item	Configuration
Registers	IICA shift register 0 (IICA0) Slave address register 0 (SVA0)
Control registers	Peripheral enable register 0 (PER0) IICA control register 00 (IICCTL00) IICA status register 0 (IICS0) IICA flag register 0 (IICF0) IICA control register 01 (IICCTL01) IICA low-level width setting register 0 (IICWL0) IICA high-level width setting register 0 (IICWH0) Port mode register 6 (PM6) Port register 6 (P6)

(1) IICA shift register 0 (IICA0)

The IICA0 register is used to convert 8-bit serial data to 8-bit parallel data and vice versa in synchronization with the serial clock. The IICA0 register can be used for both transmission and reception.

The actual transmit and receive operations can be controlled by writing and reading operations to the IICA0 register. Cancel the wait state and start data transfer by writing data to the IICA0 register during the wait period.

The IICA0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears IICA0 to 00H.

Figure 13-3. Format of IICA Shift Register 0 (IICA0)

Address: FFF50H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IICA0								

Cautions 1. Do not write data to the IICA0 register during data transfer.

2. Write or read the IICA0 register only during the wait period. Accessing the IICA0 register in a communication state other than during the wait period is prohibited. When the device serves as the master, however, the IICA0 register can be written only once after the communication trigger bit (STT0) is set to 1.

3. When communication is reserved, write data to the IICA0 register after the interrupt triggered by a stop condition is detected.

(2) Slave address register 0 (SVA0)

This register stores seven bits of local addresses {A6, A5, A4, A3, A2, A1, A0} when in slave mode.

The SVA0 register can be set by an 8-bit memory manipulation instruction.

However, rewriting to this register is prohibited while STD0 = 1 (while the start condition is detected).

Reset signal generation clears the SVA0 register to 00H.

Figure 13-4. Format of Slave Address Register 0 (SVA0)

Address: F0234H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SVA0	A6	A5	A4	A3	A2	A1	A0	0 ^{Note}

Note Bit 0 is fixed to 0.**(3) SO latch**

The SO latch is used to retain the SDAA0 pin's output level.

(4) Wakeup controller

This circuit generates an interrupt request (INTIICA0) when the address received by this register matches the address value set to the slave address register 0 (SVA0) or when an extension code is received.

(5) Serial clock counter

This counter counts the serial clocks that are output or input during transmit/receive operations and is used to verify that 8-bit data was transmitted or received.

(6) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIICA0).

An I²C interrupt request is generated by the following two triggers.

- Falling edge of eighth or ninth clock of the serial clock (set by the WTIM0 bit)
- Interrupt request generated when a stop condition is detected (set by the SPIE0 bit)

Remark WTIM0 bit: Bit 3 of IICA control register 00 (IICCTL00)

SPIE0 bit: Bit 4 of IICA control register 00 (IICCTL00)

(7) Serial clock controller

In master mode, this circuit generates the clock output via the SCLA0 pin from a sampling clock.

(8) Serial clock wait controller

This circuit controls the wait timing.

(9) ACK generator, stop condition detector, start condition detector, and ACK detector

These circuits generate and detect each status.

(10) Data hold time correction circuit

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

(11) Start condition generator

This circuit generates a start condition when the STT0 bit is set to 1.

However, in the communication reservation disabled status (IICRSV bit = 1), when the bus is not released (IICBSY bit = 1), start condition requests are ignored and the STCF bit is set to 1.

(12) Stop condition generator

This circuit generates a stop condition when the SPT0 bit is set to 1.

(13) Bus status detector

This circuit detects whether or not the bus is released by detecting start conditions and stop conditions.

However, as the bus status cannot be detected immediately following operation, the initial status is set by the STCEN bit.

Remark	STT0 bit:	Bit 1 of IICA control register 00 (IICCTL00)
	SPT0 bit:	Bit 0 of IICA control register 00 (IICCTL00)
	IICRSV bit:	Bit 0 of IICA flag register 0 (IICF0)
	IICBSY bit:	Bit 6 of IICA flag register 0 (IICF0)
	STCF bit:	Bit 7 of IICA flag register 0 (IICF0)
	STCEN bit:	Bit 1 of IICA flag register 0 (IICF0)

13.3 Registers Controlling Serial Interface IICA

Serial interface IICA is controlled by the following eight registers.

- Peripheral enable register 0 (PER0)
- IICA control register 00 (IICCTL00)
- IICA flag register 0 (IICF0)
- IICA status register 0 (IICS0)
- IICA control register 01 (IICCTL01)
- IICA low-level width setting register 0 (IICWL0)
- IICA high-level width setting register 0 (IICWH0)
- Port mode register 6 (PM6)
- Port register 6 (P6)

13.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When serial interface IICAm is used, be sure to set bit 4 (IICA0EN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 13-5. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN	0	ADCEN	IICA0EN	SAU1EN ^{Note}	SAU0EN	0	TAU0EN

IICA0EN	Control of serial interface IICA0 input clock supply
0	Stops input clock supply. • SFR used by serial interface IICA0 cannot be written. • Serial interface IICA0 is in the reset status.
1	Enables input clock supply. • SFR used by serial interface IICA0 can be read/written.

Note 32, 48, and 64-pin products only.

Cautions 1. When setting serial interface IICAm, be sure to set the IICAmEN bit to 1 first. If IICAmEN = 0, writing to a control register of serial interface IICAm is ignored, and, even if the register is read, only the default value is read (except for port mode register 6 (PM6) and port register 6 (P6)).

2. Be sure to clear the following bits to 0.

25-pin products: bits 1, 3, 6

32, 48, 64-pin products: bits 1, 6

Remark m = 0

13.3.2 IICA control register 00 (IICCTL00)

This register is used to enable/stop I²C operations, set wait timing, and set other I²C operations.

The IICCTL00 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, set the SPIE0, WTIM0, and ACKE0 bits while IICE0 = 0 or during the wait period. These bits can be set at the same time when the IICE0 bit is set from “0” to “1”.

Reset signal generation clears this register to 00H.

Figure 13-6. Format of IICA Control Register 00 (IICCTL00) (1/4)

Address: F0230H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICCTL00	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

IICE0	I ² C operation enable
0	Stop operation. Reset the IICA status register 0 (IICS0) ^{Note 1} . Stop internal operation.
1	Enable operation.
Be sure to set this bit (1) while the SCLA0 and SDAA0 lines are at high level.	
Condition for clearing (IICE0 = 0)	
• Cleared by instruction • Reset	
Condition for setting (IICE0 = 1)	
• Set by instruction	

LREL0 ^{Notes 2,3}	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCLA0 and SDAA0 lines are set to high impedance. The following flags of IICA control register 00 (IICCTL00) and the IICA status register 0 (IICS0) are cleared to 0. • STT0 • SPT0 • MSTS0 • EXC0 • COI0 • TRC0 • ACKD0 • STD0
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL0 = 0)	
• Automatically cleared after execution • Reset	
Condition for setting (LREL0 = 1)	
• Set by instruction	

WREL0 ^{Notes 2,3}	Wait cancellation
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared after wait is canceled.
When the WREL0 bit is set (wait canceled) during the wait period at the ninth clock pulse in the transmission status (TRC0 = 1), the SDAA0 line goes into the high impedance state (TRC0 = 0).	
Condition for clearing (WREL0 = 0)	
• Automatically cleared after execution • Reset	
Condition for setting (WREL0 = 1)	
• Set by instruction	

Notes 1. The IICA status register 0 (IICS0), the STCF and IICBSY bits of the IICA flag register 0 (IICF0), and the CLD0 and DAD0 bits of IICA control register 01 (IICCTL01) are reset.

2. The signal of this bit is invalid while IICE0 is 0.

3. When the LREL0 and WREL0 bits are read, 0 is always read.

Caution If the operation of I²C is enabled (IICE0 = 1) when the SCLA0 line is high level, the SDAA0 line is low level, and the digital filter is turned on (DFC0 bit of IICCTL01 register = 1), a start condition will be inadvertently detected immediately. In this case, set (1) the LREL0 bit by using a 1-bit memory manipulation instruction immediately after enabling operation of I²C (IICE0 = 1).

Figure 13-6. Format of IICA Control Register 00 (IICCTL00) (2/4)

SPIE0 ^{Note 1}	Enable/disable generation of interrupt request when stop condition is detected
0	Disable
1	Enable
If the WUP0 bit of IICA control register 01 (IICCTL01) is 1, no stop condition interrupt will be generated even if SPIE0 = 1.	
Condition for clearing (SPIE0 = 0)	
• Cleared by instruction • Reset	
Condition for setting (SPIE0 = 1)	
• Set by instruction	

WTIM0 ^{Note 1}	Control of wait and interrupt request generation
0	Interrupt request is generated at the eighth clock's falling edge. Master mode: After output of eight clocks, clock output is set to low level and wait is set. Slave mode: After input of eight clocks, the clock is set to low level and wait is set for master device.
1	Interrupt request is generated at the ninth clock's falling edge. Master mode: After output of nine clocks, clock output is set to low level and wait is set. Slave mode: After input of nine clocks, the clock is set to low level and wait is set for master device.
An interrupt is generated at the falling edge of the ninth clock during address transfer independently of the setting of this bit. The setting of this bit is valid when the address transfer is completed. When in master mode, a wait is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a wait is inserted at the falling edge of the ninth clock after an acknowledge ($\overline{ACK}$) is issued. However, when the slave device has received an extension code, a wait is inserted at the falling edge of the eighth clock.	
Condition for clearing (WTIM0 = 0)	
• Cleared by instruction • Reset	
Condition for setting (WTIM0 = 1)	
• Set by instruction	

ACKE0 ^{Notes 1, 2}	Acknowledgment control
0	Disable acknowledgment.
1	Enable acknowledgment. During the ninth clock period, the SDAA0 line is set to low level.
Condition for clearing (ACKE0 = 0)	
• Cleared by instruction • Reset	
Condition for setting (ACKE0 = 1)	
• Set by instruction	

- Notes**
1. The signal of this bit is invalid while IICE0 is 0. Set this bit during that period.
 2. The set value is invalid during address transfer and if the code is not an extension code.
When the device serves as a slave and the addresses match, an acknowledgment is generated regardless of the set value.

Figure 13-6. Format of IICA Control Register 00 (IICCTL00) (3/4)

STT0 ^{Note}	Start condition trigger
0	Do not generate a start condition.
1	When bus is released (in standby state, when IICBSY = 0): If this bit is set (1), a start condition is generated (startup as the master). When a third party is communicating: - When communication reservation function is enabled (IICRSV = 0) Functions as the start condition reservation flag. When set to 1, automatically generates a start condition after the bus is released. - When communication reservation function is disabled (IICRSV = 1) Even if this bit is set (1), the STT0 bit is cleared and the STT0 clear flag (STCF) is set (1). No start condition is generated. In the wait state (when master device): Generates a restart condition after releasing the wait.
Cautions concerning set timing - For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the waiting period when the ACKEO bit has been cleared to 0 and slave has been notified of final reception. - For master transmission: A start condition cannot be generated normally during the acknowledge period. Set to 1 during the wait period that follows output of the ninth clock. - Cannot be set to 1 at the same time as stop condition trigger (SPT0). - Once STT0 is set (1), setting it again (1) before the clear condition is met is not allowed.	
Condition for clearing (STT0 = 0)	Condition for setting (STT0 = 1)
- Cleared by setting the STT0 bit to 1 while communication reservation is prohibited. - Cleared by loss in arbitration - Cleared after start condition is generated by master device - Cleared by LREL0 = 1 (exit from communications) - When IICE0 = 0 (operation stop) - Reset	Set by instruction

Note The signal of this bit is invalid while IICE0 is 0.

Remarks

- Bit 1 (STT0) becomes 0 when it is read after data setting.
- IICRSV: Bit 0 of IIC flag register 0 (IICF0)
STCF: Bit 7 of IIC flag register 0 (IICF0)

Figure 13-6. Format of IICA Control Register 00 (IICCTL00) (4/4)

SPT0	Stop condition trigger
0	Stop condition is not generated.
1	Stop condition is generated (termination of master device's transfer).
Cautions concerning set timing - For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the waiting period when the ACKE0 bit has been cleared to 0 and slave has been notified of final reception. - For master transmission: A stop condition cannot be generated normally during the acknowledge period. Therefore, set it during the wait period that follows output of the ninth clock. - Cannot be set to 1 at the same time as start condition trigger (STT0). - The SPT0 bit can be set to 1 only when in master mode. - When the WTIM0 bit has been cleared to 0, if the SPT0 bit is set to 1 during the wait period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock. The WTIM0 bit should be changed from 0 to 1 during the wait period following the output of eight clocks, and the SPT0 bit should be set to 1 during the wait period that follows the output of the ninth clock. - Once STT0 is set (1), setting it again (1) before the clear condition is met is not allowed.	
Condition for clearing (SPT0 = 0)	Condition for setting (SPT0 = 1)
- Cleared by loss in arbitration - Automatically cleared after stop condition is detected - Cleared by LREL0 = 1 (exit from communications) - When IICE0 = 0 (operation stop) - Reset	Set by instruction

Caution When bit 3 (TRC0) of the IICA status register 0 (IICS0) is set to 1 (transmission status), bit 5 (WREL0) of IICA control register 00 (IICCTL00) is set to 1 during the ninth clock and wait is canceled, after which the TRC0 bit is cleared (reception status) and the SDAA0 line is set to high impedance. Release the wait performed while the TRC0 bit is 1 (transmission status) by writing to the IICA shift register 0.

Remark Bit 0 (SPT0) becomes 0 when it is read after data setting.

13.3.3 IICA status register 0 (IICS0)

This register indicates the status of I²C.

The IICS0 register is read by a 1-bit or 8-bit memory manipulation instruction only when STT0 = 1 and during the wait period.

Reset signal generation clears this register to 00H.

Caution Reading the IICS0 register while the address match wakeup function is enabled (WUP0 = 1) in STOP mode is prohibited. When the WUP0 bit is changed from 1 to 0 (wakeup operation is stopped), regardless of the INTIICA0 interrupt request, the change in status is not reflected until the next start condition or stop condition is detected. To use the wakeup function, therefore, enable (SPIE0 = 1) the interrupt generated by detecting a stop condition and read the IICS0 register after the interrupt has been detected.

Remark STT0: bit 1 of IICA control register 00 (IICCTL00)
WUP0: bit 7 of IICA control register 01 (IICCTL01)

Figure 13-7. Format of IICA Status Register 0 (IICS0) (1/3)

Address: FFF51H After reset: 00H R

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICS0	MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0

MSTS0	Master status check flag	
0	Slave device status or communication standby status	
1	Master device communication status	
Condition for clearing (MSTS0 = 0)		Condition for setting (MSTS0 = 1)
- When a stop condition is detected - When ALD0 = 1 (arbitration loss) - Cleared by LREL0 = 1 (exit from communications) - When the IICE0 bit changes from 1 to 0 (operation stop) - Reset		When a start condition is generated

ALD0	Detection of arbitration loss	
0	This status means either that there was no arbitration or that the arbitration result was a "win".	
1	This status indicates the arbitration result was a "loss". The MSTS0 bit is cleared.	
Condition for clearing (ALD0 = 0)		Condition for setting (ALD0 = 1)
- Automatically cleared after the IICS0 register is read^{Note} - When the IICE0 bit changes from 1 to 0 (operation stop) - Reset		When the arbitration result is a "loss".

Note This register is also cleared when a 1-bit memory manipulation instruction is executed for bits other than the IICS0 register. Therefore, when using the ALD0 bit, read the data of this bit before the data of the other bits.

Remark LREL0: Bit 6 of IICA control register 00 (IICCTL00)
IICE0: Bit 7 of IICA control register 00 (IICCTL00)

Figure 13-7. Format of IICA Status Register 0 (IICS0) (2/3)

EXC0	Detection of extension code reception	
0	Extension code was not received.	
1	Extension code was received.	
Condition for clearing (EXC0 = 0)		Condition for setting (EXC0 = 1)
- When a start condition is detected - When a stop condition is detected - Cleared by LREL0 = 1 (exit from communications) - When the IICE0 bit changes from 1 to 0 (operation stop) - Reset		When the higher four bits of the received address data is either "0000" or "1111" (set at the rising edge of the eighth clock).

COI0	Detection of matching addresses	
0	Addresses do not match.	
1	Addresses match.	
Condition for clearing (COI0 = 0)		Condition for setting (COI0 = 1)
- When a start condition is detected - When a stop condition is detected - Cleared by LREL0 = 1 (exit from communications) - When the IICE0 bit changes from 1 to 0 (operation stop) - Reset		When the received address matches the local address (slave address register 0 (SVA0)) (set at the rising edge of the eighth clock).

TRC0	Detection of transmit/receive status	
0	Receive status (other than transmit status). The SDAA0 line is set for high impedance.	
1	Transmit status. The value in the SO0 latch is enabled for output to the SDAA0 line (valid starting at the falling edge of the first byte's ninth clock).	
Condition for clearing (TRC0 = 0)		Condition for setting (TRC0 = 1)
<Both master and slave> - When a stop condition is detected - Cleared by LREL0 = 1 (exit from communications) - When the IICE0 bit changes from 1 to 0 (operation stop) - Cleared by WREL0 = 1^{Note} (wait cancel) - When the ALD0 bit changes from 0 to 1 (arbitration loss) - Reset - When not used for communication (MSTS0, EXC0, COI0 = 0) <Master> - When "1" is output to the first byte's LSB (transfer direction specification bit) <Slave> - When a start condition is detected - When "0" is input to the first byte's LSB (transfer direction specification bit)		<Master> - When a start condition is generated - When 0 (master transmission) is output to the LSB (transfer direction specification bit) of the first byte (during address transfer) <Slave> - When 1 (slave transmission) is input to the LSB (transfer direction specification bit) of the first byte from the master (during address transfer)

Note When bit 3 (TRC0) of the IICA status register 0 (IICS0) is set to 1 (transmission status), bit 5 (WREL0) of IICA control register 00 (IICCTL00) is set to 1 during the ninth clock and wait is canceled, after which the TRC0 bit is cleared (reception status) and the SDAA0 line is set to high impedance. Release the wait performed while the TRC0 bit is 1 (transmission status) by writing to the IICA shift register 0.

Remark LREL0: Bit 6 of IICA control register 00 (IICCTL00)
IICE0: Bit 7 of IICA control register 00 (IICCTL00)

Figure 13-7. Format of IICA Status Register 0 (IICS0) (3/3)

ACKD0	Detection of acknowledge ($\overline{\text{ACK}}$)	
0	Acknowledge was not detected.	
1	Acknowledge was detected.	
Condition for clearing (ACKD0 = 0)		Condition for setting (ACKD0 = 1)
- When a stop condition is detected - At the rising edge of the next byte's first clock - Cleared by LREL0 = 1 (exit from communications) - When the IICE0 bit changes from 1 to 0 (operation stop) - Reset		After the SDAA0 line is set to low level at the rising edge of SCLA0 line's ninth clock

STD0	Detection of start condition	
0	Start condition was not detected.	
1	Start condition was detected. This indicates that the address transfer period is in effect.	
Condition for clearing (STD0 = 0)		Condition for setting (STD0 = 1)
- When a stop condition is detected - At the rising edge of the next byte's first clock following address transfer - Cleared by LREL0 = 1 (exit from communications) - When the IICE0 bit changes from 1 to 0 (operation stop) - Reset		When a start condition is detected

SPD0	Detection of stop condition	
0	Stop condition was not detected.	
1	Stop condition was detected. The master device's communication is terminated and the bus is released.	
Condition for clearing (SPD0 = 0)		Condition for setting (SPD0 = 1)
- At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition - When the WUP0 bit changes from 1 to 0 - When the IICE0 bit changes from 1 to 0 (operation stop) - Reset		When a stop condition is detected

Remark LREL0: Bit 6 of IICA control register 00 (IICCTL00)

IICE0: Bit 7 of IICA control register 00 (IICCTL00)

13.3.4 IICA flag register 0 (IICF0)

This register sets the operation mode of I²C and indicates the status of the I²C bus.

The IICF0 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the STT0 clear flag (STCF) and I²C bus status flag (IICBSY) bits are read-only.

The IICRSV bit can be used to enable/disable the communication reservation function.

The STCEN bit can be used to set the initial value of the IICBSY bit.

The IICRSV and STCEN bits can be written only when the operation of I²C is disabled (bit 7 (IICE0) of IICA control register 00 (IICCTL00) = 0). When operation is enabled, the IICF0 register can be read.

Reset signal generation clears this register to 00H.

Figure 13-8. Format of IICA Flag Register 0 (IICF0)

Address: FFF52H	After reset: 00H	R/W ^{Note}						
Symbol	<7>	<6>	5	4	3	2	<1>	<0>
IICF0	STCF0	IICBSY0	0	0	0	0	STCEN0	IICRSV0

STCF0	STT0 clear flag
0	Generate start condition
1	Start condition generation unsuccessful: clear the STT0 flag
Condition for clearing (STCF0 = 0)	
- Cleared by STT0 = 1 - When IICE0 = 0 (operation stop) - Reset	
Condition for setting (STCF0 = 1)	
Generating start condition unsuccessful and the STT0 bit cleared to 0 when communication reservation is disabled (IICRSV0 = 1).	

IICBSY0	I ² C bus status flag
0	Bus release status (communication initial status when STCEN0 = 1)
1	Bus communication status (communication initial status when STCEN0 = 0)
Condition for clearing (IICBSY0 = 0)	
- Detection of stop condition - When IICE0 = 0 (operation stop) - Reset	
Condition for setting (IICBSY0 = 1)	
- Detection of start condition - Setting of the IICE0 bit when STCEN0 = 0	

STCEN0	Initial start enable trigger
0	After operation is enabled (IICE0 = 1), enable generation of a start condition upon detection of a stop condition.
1	After operation is enabled (IICE0 = 1), enable generation of a start condition without detecting a stop condition.
Condition for clearing (STCEN0 = 0)	
- Cleared by instruction - Detection of start condition - Reset	
Condition for setting (STCEN0 = 1)	
Set by instruction	

IICRSV0	Communication reservation function disable bit
0	Enable communication reservation
1	Disable communication reservation
Condition for clearing (IICRSV0 = 0)	
- Cleared by instruction - Reset	
Condition for setting (IICRSV0 = 1)	
Set by instruction	

Note Bits 6 and 7 are read-only.

- Cautions**
1. Write to the STCEN bit only when the operation is stopped (IICE0 = 0).
 2. As the bus release status (IICBSY = 0) is recognized regardless of the actual bus status when STCEN = 1, when generating the first start condition (STT0 = 1), it is necessary to verify that no third party communications are in progress in order to prevent such communications from being destroyed.
 3. Write to IICRSV only when the operation is stopped (IICE0 = 0).

Remark STT0: Bit 1 of IICA control register 00 (IICCTL00)
IICE0: Bit 7 of IICA control register 00 (IICCTL00)

13.3.5 IICA control register 01 (IICCTL01)

This register is used to set the operation mode of I²C and detect the statuses of the SCLA0 and SDAA0 pins.

The IICCTL01 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the CLD0 and DAD0 bits are read-only.

Set the IICCTL01 register, except the WUP0 bit, while operation of I²C is disabled (bit 7 (IICE0) of IICA control register 00 (IICCTL00) is 0).

Reset signal generation clears this register to 00H.

Figure 13-9. Format of IICA Control Register 01 (IICCTL01) (1/2)

Address: F0231H After reset: 00H R/W^{Note 1}

Symbol	7	6	<5>	<4>	<3>	<2>	1	<0>
IICCTL01	WUP0	0	CLD0	DAD0	SMC0	DFC0	0	PRS0

WUP0	Control of address match wakeup
0	Stops operation of address match wakeup function in STOP mode.
1	Enables operation of address match wakeup function in STOP mode.
To shift to STOP mode when WUP0 = 1, execute the STOP instruction at least three clocks after setting (1) the WUP0 bit (see Figure 13-22 Flow When Setting WUP0 = 1). Clear (0) the WUP0 bit after the address has matched or an extension code has been received. The subsequent communication can be entered by the clearing (0) WUP0 bit. (The wait must be released and transmit data must be written after the WUP0 bit has been cleared (0).) The interrupt timing when the address has matched or when an extension code has been received, while WUP0 = 1, is identical to the interrupt timing when WUP0 = 0. (A delay of the difference of sampling by the clock will occur.) Furthermore, when WUP0 = 1, a stop condition interrupt is not generated even if the SPIE0 bit is set to 1. When WUP0 = 0 is set by a source other than an interrupt from serial interface IICA, operation as the master device cannot be performed until the subsequent start condition or stop condition is detected. Do not output a start condition by setting (1) the STT0 bit, without waiting for the detection of the subsequent start condition or stop condition.	
Condition for clearing (WUP0 = 0)	
• Cleared by instruction (after address match or extension code reception)	
Condition for setting (WUP0 = 1)	
• Set by instruction (when the MST0, EXC0, and COI0 bits are "0", and the STD0 bit also "0" (communication not entered))^{Note 2}	

Notes 1. Bits 4 and 5 are read-only.

- The status of the IICA status register 0 (IICS0) must be checked and the WUP0 bit must be set during the period shown below.

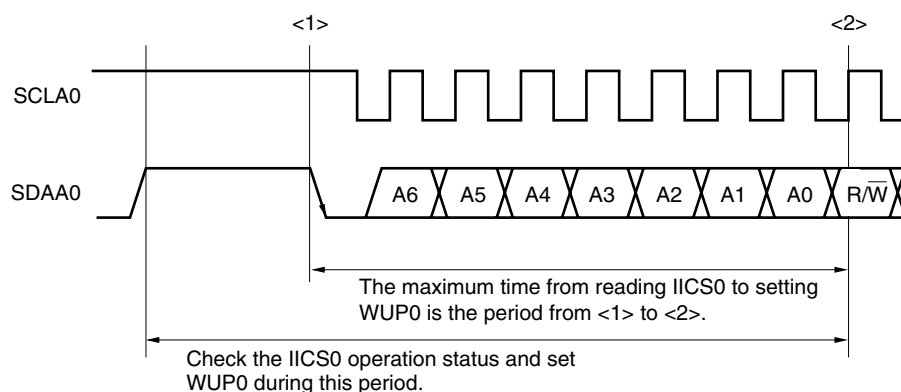


Figure 13-9. Format of IICA Control Register 01 (IICCTL01) (2/2)

CLD0	Detection of SCLA0 pin level (valid only when IICE0 = 1)	
0	The SCLA0 pin was detected at low level.	
1	The SCLA0 pin was detected at high level.	
Condition for clearing (CLD0 = 0)		Condition for setting (CLD0 = 1)
- When the SCLA0 pin is at low level - When IICE0 = 0 (operation stop) - Reset		When the SCLA0 pin is at high level

DAD0	Detection of SDAA0 pin level (valid only when IICE0 = 1)	
0	The SDAA0 pin was detected at low level.	
1	The SDAA0 pin was detected at high level.	
Condition for clearing (DAD0 = 0)		Condition for setting (DAD0 = 1)
- When the SDAA0 pin is at low level - When IICE0 = 0 (operation stop) - Reset		When the SDAA0 pin is at high level

SMC0	Operation mode switching	
0	Operates in standard mode (fastest transfer rate: 100 kbps).	
1	Operates in fast mode (fastest transfer rate: 400 kbps) or fast mode plus (fastest transfer rate: 1 Mbps).	

DFC0	Digital filter operation control
0	Digital filter off.
1	Digital filter on.

Digital filter can be used only in fast mode.

In fast mode, the transfer clock does not vary, regardless of the DFC0 bit being set (1) or cleared (0).

The digital filter is used for noise elimination in fast mode.

PRS0	Division of the operation clock	
0	Selects f_{CLK} as operation clock.	
1	Selects $f_{CLK}/2$ as operation clock.	

Caution The fastest operation frequency of the operation clock of the serial interface IICA is 20 MHz (Max.). If the f_{CLK} exceeds 20 MHz, set the clock to $f_{CLK}/2$ by setting the PRS0 bit to 1.

Remark IICE0: Bit 7 of IICA control register 00 (IICCTL00)

13.3.6 IICA low-level width setting register 0 (IICWL0)

This register is used to set the low-level width (t_{LOW}) and data hold time ($t_{HD:DAT}$) of the SCLA0 pin signal that is output by serial interface IICA. The data hold time is decided by value the higher 6 bits of IICWL register.

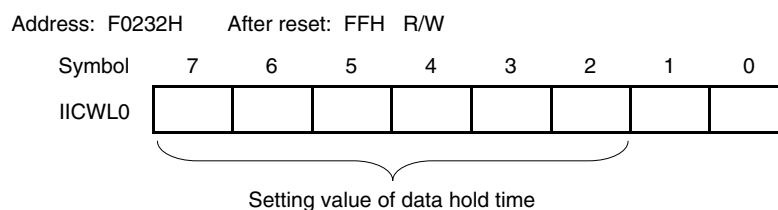
The IICWL0 register can be set by an 8-bit memory manipulation instruction.

Set the IICWL0 register while operation of I²C is disabled (bit 7 (IICE0) of IICA control register 00 (IICCTL00) is 0).

Reset signal generation sets this register to FFH.

For details about setting the IICWL0 register, see 13.4.2 Setting transfer clock by using IICWL0 and IICWH0 registers.

Figure 13-10. Format of IICA Low-Level Width Setting Register 0 (IICWL0)



13.3.7 IICA high-level width setting register 0 (IICWH0)

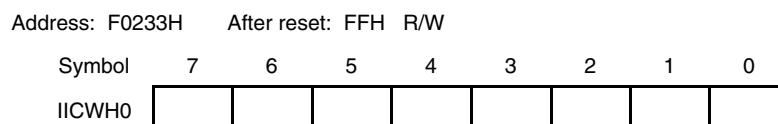
This register is used to set the high-level width of the SCLA0 pin signal that is output by serial interface IICA.

The IICWH0 register can be set by an 8-bit memory manipulation instruction.

Set the IICWH0 register while operation of I²C is disabled (bit 7 (IICE0) of IICA control register 00 (IICCTL00) is 0).

Reset signal generation sets this register to FFH.

Figure 13-11. Format of IICA High-Level Width Setting Register 0 (IICWH0)



Remark For how to set the transfer clock by using the IICWL0 and IICWH0 registers, see **13.4.2 Setting transfer clock by using IICWL0 and IICWH0 registers.**

13.3.8 Port mode register 6 (PM6)

This register sets the input/output of port 6 in 1-bit units.

When using the P60/SCLA0 pin as clock I/O and the P61/SDAA0 pin as serial data I/O, clear PM60 and PM61, and the output latches of P60 and P61 to 0.

Set the IICE0 bit (bit 7 of IICA control register 00 (IICCTL00)) to 1 before setting the output mode because the P60/SCLA0 and P61/SDAA0 pins output a low level (fixed) when the IICE0 bit is 0.

The PM6 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 13-12. Format of Port Mode Register 6 (PM6)(in case of 64-pin products)

Address: FFF26H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM6	1	1	1	1	PM63	PM62	PM61	PM60

PM6n	P6n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

13.4 I²C Bus Mode Functions

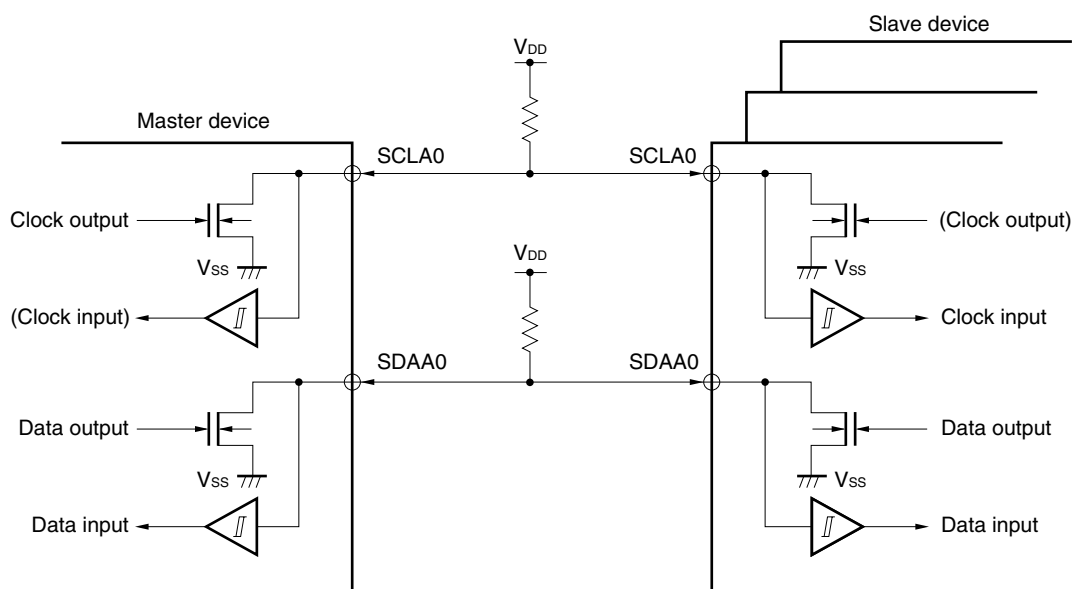
13.4.1 Pin configuration

The serial clock pin (SCLA0) and the serial data bus pin (SDAA0) are configured as follows.

- (1) SCLA0 This pin is used for serial clock input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.
- (2) SDAA0 This pin is used for serial data input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

Since outputs from the serial clock line and the serial data bus line are N-ch open-drain outputs, an external pull-up resistor is required.

Figure 13-13. Pin Configuration Diagram



13.4.2 Setting transfer clock by using IICWL0 and IICWH0 registers

(1) Setting transfer clock on master side

$$\text{Transfer clock} = \frac{f_{\text{CLK}}}{\text{IICWL0} + \text{IICWH0} + f_{\text{CLK}}(t_{\text{R}} + t_{\text{F}})}$$

At this time, the optimal setting values of the IICWL0 and IICWH0 registers are as follows.

(The fractional parts of all setting values are rounded up.)

- When the fast mode

$$\begin{aligned}\text{IICWL0} &= \frac{0.52}{\text{Transfer clock}} \times f_{\text{CLK}} \\ \text{IICWH0} &= \left(\frac{0.48}{\text{Transfer clock}} - t_{\text{R}} - t_{\text{F}} \right) \times f_{\text{CLK}}\end{aligned}$$

- When the normal mode

$$\begin{aligned}\text{IICWL0} &= \frac{0.47}{\text{Transfer clock}} \times f_{\text{CLK}} \\ \text{IICWH0} &= \left(\frac{0.53}{\text{Transfer clock}} - t_{\text{R}} - t_{\text{F}} \right) \times f_{\text{CLK}}\end{aligned}$$

- When the fast mode plus

$$\begin{aligned}\text{IICWL0} &= \frac{0.50}{\text{Transfer clock}} \times f_{\text{CLK}} \\ \text{IICWH0} &= \left(\frac{0.50}{\text{Transfer clock}} - t_{\text{R}} - t_{\text{F}} \right) \times f_{\text{CLK}}\end{aligned}$$

(2) Setting IICWL0 and IICWH0 registers on slave side

(The fractional parts of all setting values are truncated.)

- When the fast mode

$$\begin{aligned}\text{IICWL0} &= 1.3 \mu\text{s} \times f_{\text{CLK}} \\ \text{IICWH0} &= (1.2 \mu\text{s} - t_{\text{R}} - t_{\text{F}}) \times f_{\text{CLK}}\end{aligned}$$

- When the normal mode

$$\begin{aligned}\text{IICWL0} &= 4.7 \mu\text{s} \times f_{\text{CLK}} \\ \text{IICWH0} &= (5.3 \mu\text{s} - t_{\text{R}} - t_{\text{F}}) \times f_{\text{CLK}}\end{aligned}$$

- When the fast mode plus

$$\begin{aligned}\text{IICWL0} &= 0.50 \mu\text{s} \times f_{\text{CLK}} \\ \text{IICWH0} &= (0.50 \mu\text{s} - t_{\text{R}} - t_{\text{F}}) \times f_{\text{CLK}}\end{aligned}$$

(**Caution** and **Remarks** are listed on the next page.)

Caution Note the minimum f_{CLK} operation frequency when setting the transfer clock. The minimum f_{CLK} operation frequency for serial interface IICA is determined according to the mode.

Fast mode: $f_{CLK} = 3.5 \text{ MHz (MIN.)}$

Fast mode plus: $f_{CLK} = 10 \text{ MHz (MIN.)}$

Normal mode: $f_{CLK} = 1 \text{ MHz (MIN.)}$

In addition, the fastest operation frequency of the operation clock of the serial interface IICA is 20 MHz (Max.). If the f_{CLK} exceeds 20 MHz, set the clock to $f_{CLK}/2$ by setting the PRS0 bit of IICCTL01 register to 1.

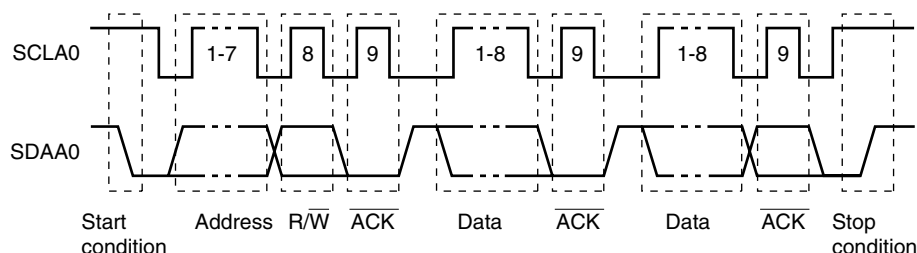
Remarks 1. Calculate the rise time (t_R) and fall time (t_F) of the SDAA0 and SCLA0 signals separately, because they differ depending on the pull-up resistance and wire load.

- 2.**
- | | |
|-------------|--|
| IICWL0: | IICA low-level width setting register 0 |
| IICWH0: | IICA high-level width setting register 0 |
| t_F : | SDAA0 and SCLA0 signal falling times |
| t_R : | SDAA0 and SCLA0 signal rising times |
| f_{CLK} : | CPU/peripheral hardware clock frequency |

13.5 I²C Bus Definitions and Control Methods

The following section describes the I²C bus's serial data communication format and the signals used by the I²C bus. Figure 13-14 shows the transfer timing for the "start condition", "address", "data", and "stop condition" output via the I²C bus's serial data bus.

Figure 13-14. I²C Bus Serial Data Transfer Timing



The master device generates the start condition, slave address, and stop condition.

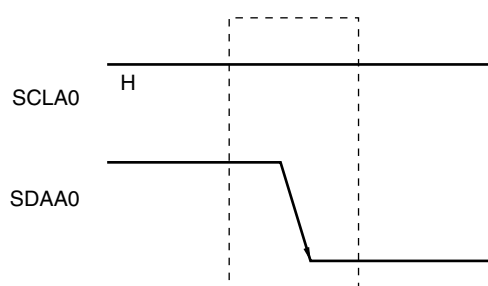
The acknowledge ($\overline{\text{ACK}}$) can be generated by either the master or slave device (normally, it is output by the device that receives 8-bit data).

The serial clock (SCLA0) is continuously output by the master device. However, in the slave device, the SCLA0 pin low level period can be extended and a wait can be inserted.

13.5.1 Start conditions

A start condition is met when the SCLA0 pin is at high level and the SDAA0 pin changes from high level to low level. The start conditions for the SCLA0 pin and SDAA0 pin are signals that the master device generates to the slave device when starting a serial transfer. When the device is used as a slave, start conditions can be detected.

Figure 13-15. Start Conditions



A start condition is output when bit 1 (STT0) of IICA control register 00 (IICCTL00) is set (1) after a stop condition has been detected (SPD0: Bit 0 of the IICA status register 0 (IICCS0) = 1). When a start condition is detected, bit 1 (STD0) of the IICCS0 register is set (1).

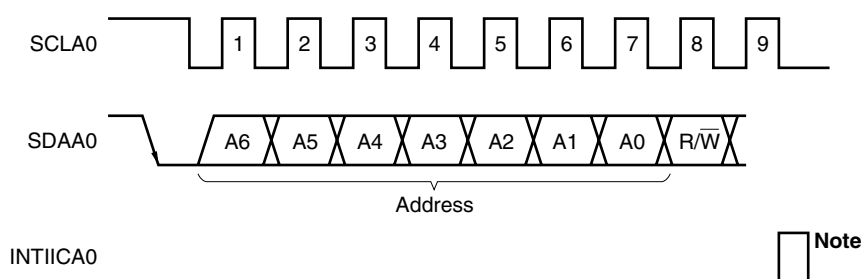
13.5.2 Addresses

The address is defined by the 7 bits of data that follow the start condition.

An address is a 7-bit data segment that is output in order to select one of the slave devices that are connected to the master device via the bus lines. Therefore, each slave device connected via the bus lines must have a unique address.

The slave devices include hardware that detects the start condition and checks whether or not the 7-bit address data matches the data values stored in the slave address register 0 (SVA0). If the address data matches the SVA0 register values, the slave device is selected and communicates with the master device until the master device generates a start condition or stop condition.

Figure 13-16. Address



Note INTIICA0 is not issued if data other than a local address or extension code is received during slave device operation.

Addresses are output when a total of 8 bits consisting of the slave address and the transfer direction described in **13.5.3 Transfer direction specification** are written to the IICA shift register 0 (IICA0). The received addresses are written to the IICA0 register.

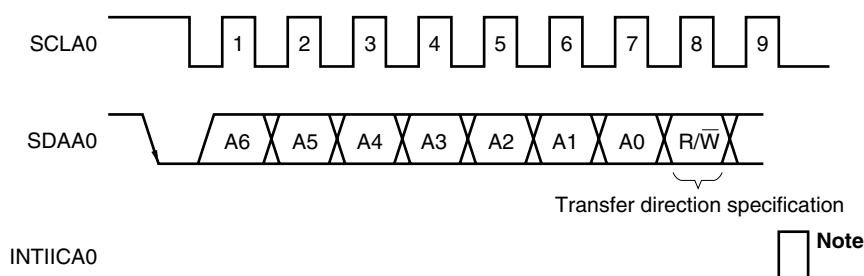
The slave address is assigned to the higher 7 bits of the IICA0 register.

13.5.3 Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction.

When this transfer direction specification bit has a value of "0", it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of "1", it indicates that the master device is receiving data from a slave device.

Figure 13-17. Transfer Direction Specification



Note INTIICA0 is not issued if data other than a local address or extension code is received during slave device operation.

13.5.4 Acknowledge ($\overline{\text{ACK}}$)

$\overline{\text{ACK}}$ is used to check the status of serial data at the transmission and reception sides.

The reception side returns $\overline{\text{ACK}}$ each time it has received 8-bit data.

The transmission side usually receives $\overline{\text{ACK}}$ after transmitting 8-bit data. When $\overline{\text{ACK}}$ is returned from the reception side, it is assumed that reception has been correctly performed and processing is continued. Whether $\overline{\text{ACK}}$ has been detected can be checked by using bit 2 (ACKD0) of the IICA status register 0 (IICS0).

When the master receives the last data item, it does not return $\overline{\text{ACK}}$ and instead generates a stop condition. If a slave does not return $\overline{\text{ACK}}$ after receiving data, the master outputs a stop condition or restart condition and stops transmission. If $\overline{\text{ACK}}$ is not returned, the possible causes are as follows.

- <1> Reception was not performed normally.
- <2> The final data item was received.
- <3> The reception side specified by the address does not exist.

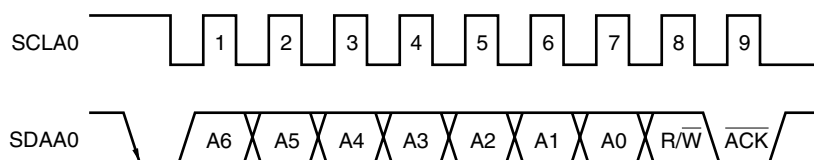
To generate $\overline{\text{ACK}}$, the reception side makes the SDAA0 line low at the ninth clock (indicating normal reception).

Automatic generation of $\overline{\text{ACK}}$ is enabled by setting bit 2 (ACKE0) of IICA control register 00 (IICCTL00) to 1. Bit 3 (TRC0) of the IICS0 register is set by the data of the eighth bit that follows 7-bit address information. Usually, set the ACKE0 bit to 1 for reception (TRC0 = 0).

If a slave can receive no more data during reception (TRC0 = 0) or does not require the next data item, then the slave must inform the master, by clearing the ACKE0 bit to 0, that it will not receive any more data.

When the master does not require the next data item during reception (TRC0 = 0), it must clear the ACKE0 bit to 0 so that $\overline{\text{ACK}}$ is not generated. In this way, the master informs a slave at the transmission side that it does not require any more data (transmission will be stopped).

Figure 13-18. $\overline{\text{ACK}}$



When the local address is received, $\overline{\text{ACK}}$ is automatically generated, regardless of the value of the ACKE0 bit. When an address other than that of the local address is received, $\overline{\text{ACK}}$ is not generated (NACK).

When an extension code is received, $\overline{\text{ACK}}$ is generated if the ACKE0 bit is set to 1 in advance.

How $\overline{\text{ACK}}$ is generated when data is received differs as follows depending on the setting of the wait timing.

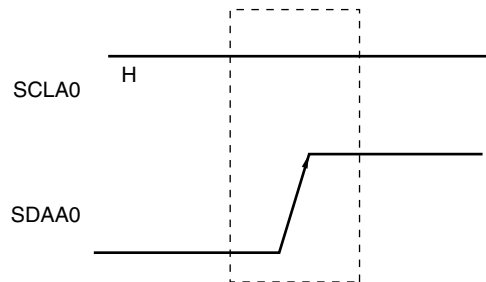
- When 8-clock wait state is selected (bit 3 (WTIM0) of IICCTL00 register = 0):
By setting the ACKE0 bit to 1 before releasing the wait state, $\overline{\text{ACK}}$ is generated at the falling edge of the eighth clock of the SCL A0 pin.
- When 9-clock wait state is selected (bit 3 (WTIM0) of IICCTL00 register = 1):
 $\overline{\text{ACK}}$ is generated by setting the ACKE0 bit to 1 in advance.

13.5.5 Stop condition

When the SCLA0 pin is at high level, changing the SDAA0 pin from low level to high level generates a stop condition.

A stop condition is a signal that the master device generates to the slave device when serial transfer has been completed. When the device is used as a slave, stop conditions can be detected.

Figure 13-19. Stop Condition



A stop condition is generated when bit 0 (SPT0) of IICA control register 00 (IICCTL00) is set to 1. When the stop condition is detected, bit 0 (SPD0) of the IICA status register 0 (IICS0) is set to 1 and INTIICA0 is generated when bit 4 (SPIE0) of the IICCTL00 register is set to 1.

13.5.6 Wait

The wait is used to notify the communication partner that a device (master or slave) is preparing to transmit or receive data (i.e., is in a wait state).

Setting the SCLA0 pin to low level notifies the communication partner of the wait state. When wait state has been canceled for both the master and slave devices, the next data transfer can begin.

Figure 13-20. Wait (1/2)

- (1) When master device has a nine-clock wait and slave device has an eight-clock wait
(master transmits, slave receives, and ACKE0 = 1)**

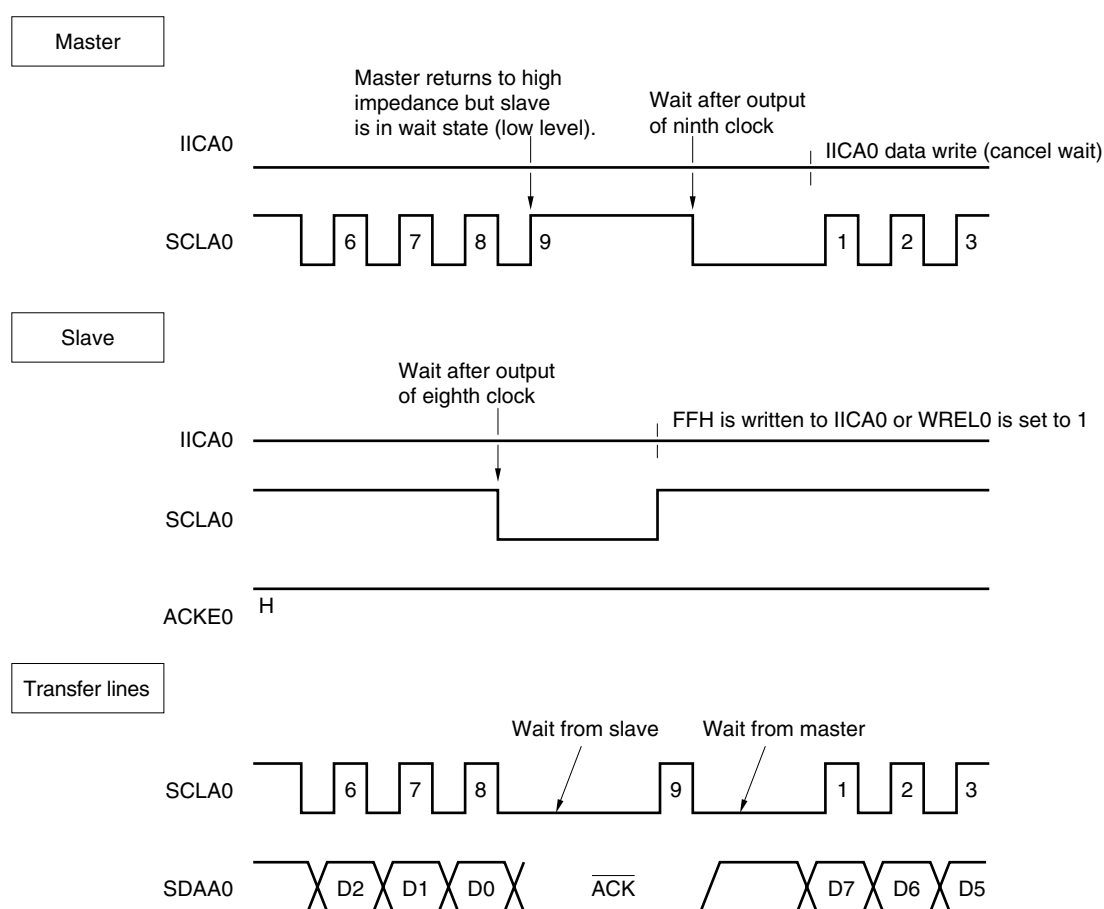
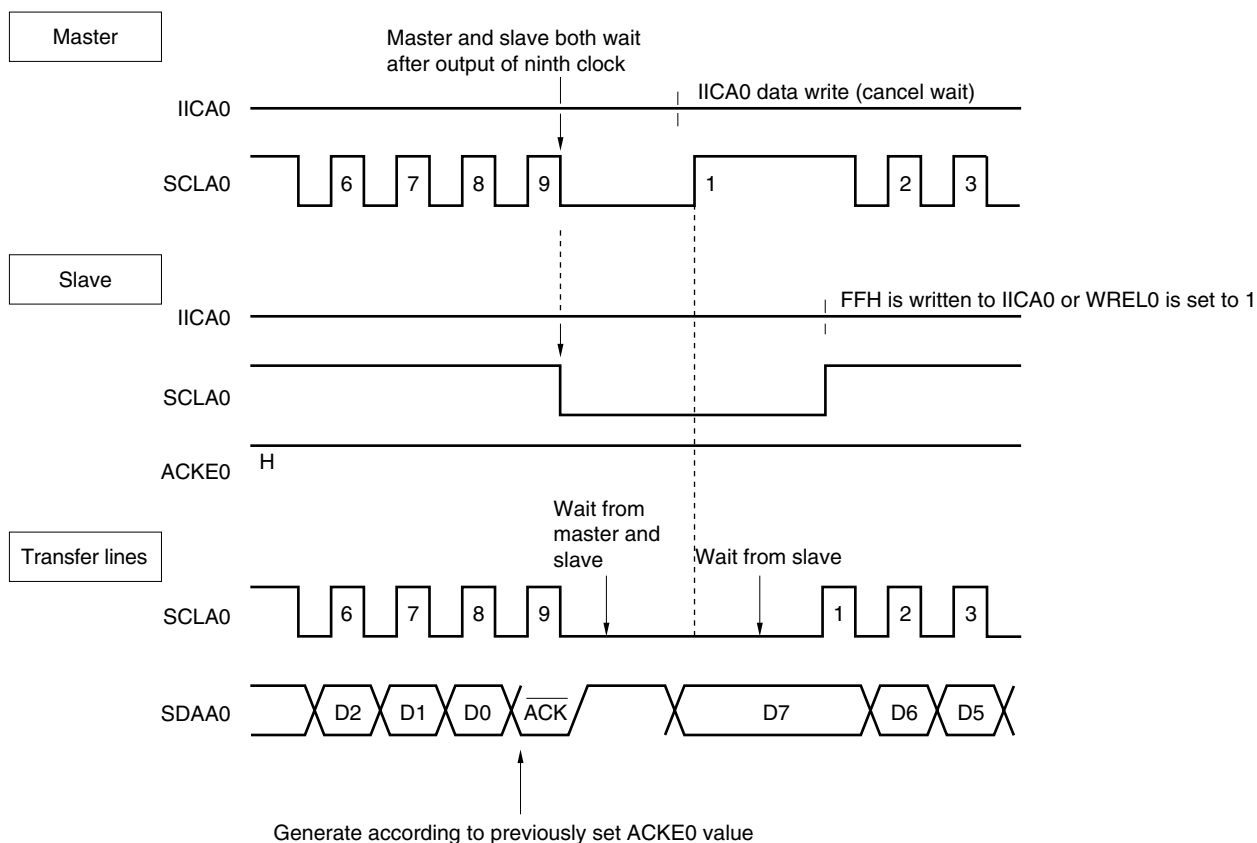


Figure 13-20. Wait (2/2)

**(2) When master and slave devices both have a nine-clock wait
(master transmits, slave receives, and ACKE0 = 1)**



Remark ACKE0: Bit 2 of IICA control register 00 (IICCTL00)

WREL0: Bit 5 of IICA control register 00 (IICCTL00)

A wait may be automatically generated depending on the setting of bit 3 (WTIM0) of IICA control register 00 (IICCTL00).

Normally, the receiving side cancels the wait state when bit 5 (WREL0) of the IICCTL00 register is set to 1 or when FFH is written to the IICA shift register 0 (IICA0), and the transmitting side cancels the wait state when data is written to the IICA0 register.

The master device can also cancel the wait state via either of the following methods.

- By setting bit 1 (STT0) of the IICCTL00 register to 1
- By setting bit 0 (SPT0) of the IICCTL00 register to 1

13.5.7 Canceling wait

The I²C usually cancels a wait state by the following processing.

- Writing data to the IICA shift register 0 (IICA0)
- Setting bit 5 (WRELO) of IICA control register 00 (IICCTL00) (canceling wait)
- Setting bit 1 (STT0) of the IICCTL00 register (generating start condition)^{Note}
- Setting bit 0 (SPT0) of the IICCTL00 register (generating stop condition)^{Note}

Note Master only

When the above wait canceling processing is executed, the I²C cancels the wait state and communication is resumed.

To cancel a wait state and transmit data (including addresses), write the data to the IICA0 register.

To receive data after canceling a wait state, or to complete data transmission, set bit 5 (WRELO) of the IICCTL00 register to 1.

To generate a restart condition after canceling a wait state, set bit 1 (STT0) of the IICCTL00 register to 1.

To generate a stop condition after canceling a wait state, set bit 0 (SPT0) of the IICCTL00 register to 1.

Execute the canceling processing only once for one wait state.

If, for example, data is written to the IICA0 register after canceling a wait state by setting the WRELO bit to 1, an incorrect value may be output to SDAA0 line because the timing for changing the SDAA0 line conflicts with the timing for writing the IICA0 register.

In addition to the above, communication is stopped if the IICE0 bit is cleared to 0 when communication has been aborted, so that the wait state can be canceled.

If the I²C bus has deadlocked due to noise, processing is saved from communication by setting bit 6 (LRELO) of the IICCTL00 register, so that the wait state can be canceled.

Caution If a processing to cancel a wait state is executed when WUP0 = 1, the wait state will not be canceled.

13.5.8 Interrupt request (INTIICA0) generation timing and wait control

The setting of bit 3 (WTIM0) of IICA control register 00 (IICCTL00) determines the timing by which INTIICA0 is generated and the corresponding wait control, as shown in Table 13-2.

Table 13-2. INTIICA0 Generation Timing and Wait Control

WTIM0	During Slave Device Operation			During Master Device Operation		
	Address	Data Reception	Data Transmission	Address	Data Reception	Data Transmission
0	9 ^{Notes 1, 2}	8 ^{Note 2}	8 ^{Note 2}	9	8	8
1	9 ^{Notes 1, 2}	9 ^{Note 2}	9 ^{Note 2}	9	9	9

Notes 1. The slave device's INTIICA0 signal and wait period occurs at the falling edge of the ninth clock only when there is a match with the address set to the slave address register 0 (SVA0).

At this point, $\overline{ACK}$ is generated regardless of the value set to the IICCTL00 register's bit 2 (ACKE0). For a slave device that has received an extension code, INTIICA0 occurs at the falling edge of the eighth clock.

However, if the address does not match after restart, INTIICA0 is generated at the falling edge of the 9th clock, but wait does not occur.

- 2.** If the received address does not match the contents of the slave address register 0 (SVA0) and extension code is not received, neither INTIICA0 nor a wait occurs.

Remark The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and wait control are both synchronized with the falling edge of these clock signals.

(1) During address transmission/reception

- Slave device operation: Interrupt and wait timing are determined depending on the conditions described in Notes 1 and 2 above, regardless of the WTIM0 bit.
- Master device operation: Interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIM0 bit.

(2) During data reception

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

(3) During data transmission

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

(4) Wait cancellation method

The four wait cancellation methods are as follows.

- Writing data to the IICA shift register 0 (IICA0)
- Setting bit 5 (WRELO) of IICA control register 00 (IICCTL00) (canceling wait)
- Setting bit 1 (STT0) of IICCTL00 register (generating start condition)^{Note}
- Setting bit 0 (SPT0) of IICCTL00 register (generating stop condition)^{Note}

Note Master only.

When an 8-clock wait has been selected (WTIM0 = 0), the presence/absence of $\overline{ACK}$ generation must be determined prior to wait cancellation.

(5) Stop condition detection

INTIICA0 is generated when a stop condition is detected (only when SPIE0 = 1).

13.5.9 Address match detection method

In I²C bus mode, the master device can select a particular slave device by transmitting the corresponding slave address.

Address match can be detected automatically by hardware. An interrupt request (INTIICA0) occurs when the address set to the slave address register 0 (SVA0) matches the slave address sent by the master device, or when an extension code has been received.

13.5.10 Error detection

In I²C bus mode, the status of the serial data bus (SDAA0) during data transmission is captured by the IICA shift register 0 (IICA0) of the transmitting device, so the IICA data prior to transmission can be compared with the transmitted IICA data to enable detection of transmission errors. A transmission error is judged as having occurred when the compared data values do not match.

13.5.11 Extension code

- (1) When the higher 4 bits of the receive address are either "0000" or "1111", the extension code reception flag (EXC0) is set to 1 for extension code reception and an interrupt request (INTIICA0) is issued at the falling edge of the eighth clock. The local address stored in the slave address register 0 (SVA0) is not affected.
- (2) The settings below are specified if 11110xx0 is transferred from the master by using a 10-bit address transfer when the SVA0 register is set to 11110xx0. Note that INTIICA0 occurs at the falling edge of the eighth clock.
 - Higher four bits of data match: EXC0 = 1
 - Seven bits of data match: COI0 = 1

Remark EXC0: Bit 5 of IICA status register 0 (IICS0)

COI0: Bit 4 of IICA status register 0 (IICS0)

- (3) Since the processing after the interrupt request occurs differs according to the data that follows the extension code, such processing is performed by software.

If the extension code is received while a slave device is operating, then the slave device is participating in communication even if its address does not match.

For example, after the extension code is received, if you do not wish to operate the target device as a slave device, set bit 6 (LREL0) of IICA control register 00 (IICCTL00) to 1 to set the standby mode for the next communication operation.

Table 13-3. Bit Definitions of Major Extension Codes

Slave Address	R/W Bit	Description
0 0 0 0 0 0 0	0	General call address
1 1 1 1 0 x x	0	10-bit slave address specification (during address authentication)
1 1 1 1 0 x x	1	10-bit slave address specification (after address match, when read command is issued)

Remark See the I²C bus specifications issued by NXP Semiconductors for details of extension codes other than those described above.

13.5.12 Arbitration

When several master devices simultaneously generate a start condition (when the STT0 bit is set to 1 before the STD0 bit is set to 1), communication among the master devices is performed as the number of clocks are adjusted until the data differs. This kind of operation is called arbitration.

When one of the master devices loses in arbitration, an arbitration loss flag (ALD0) in the IICA status register 0 (IICS0) is set (1) via the timing by which the arbitration loss occurred, and the SCLA0 and SDAA0 lines are both set to high impedance, which releases the bus.

The arbitration loss is detected based on the timing of the next interrupt request (the eighth or ninth clock, when a stop condition is detected, etc.) and the ALD0 = 1 setting that has been made by software.

For details of interrupt request timing, see **13.5.8 Interrupt request (INTIICA0) generation timing and wait control**.

Remark STD0: Bit 1 of IICA status register 0 (IICS0)
STT0: Bit 1 of IICA control register 00 (IICCTL00)

Figure 13-21. Arbitration Timing Example

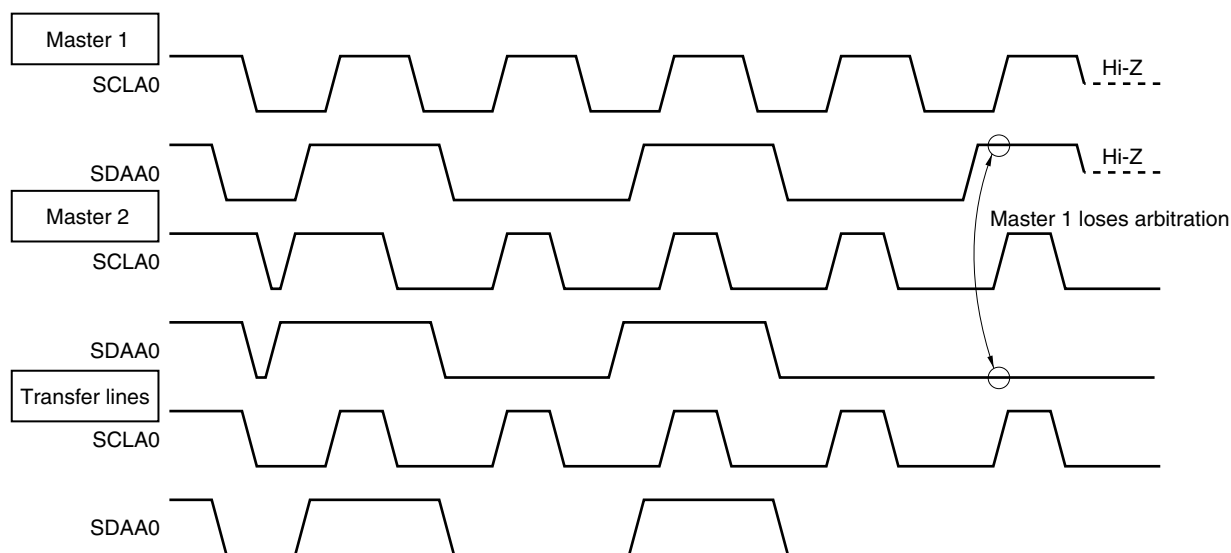


Table 13-4. Status During Arbitration and Interrupt Request Generation Timing

Status During Arbitration	Interrupt Request Generation Timing
During address transmission	At falling edge of eighth or ninth clock following byte transfer ^{Note 1}
Read/write data after address transmission	
During extension code transmission	
Read/write data after extension code transmission	
During data transmission	
During $\overline{\text{ACK}}$ transfer period after data transmission	
When restart condition is detected during data transfer	
When stop condition is detected during data transfer	When stop condition is generated (when SPIE0 = 1) ^{Note 2}
When data is at low level while attempting to generate a restart condition	At falling edge of eighth or ninth clock following byte transfer ^{Note 1}
When stop condition is detected while attempting to generate a restart condition	When stop condition is generated (when SPIE0 = 1) ^{Note 2}
When data is at low level while attempting to generate a stop condition	At falling edge of eighth or ninth clock following byte transfer ^{Note 1}
When SCLA0 is at low level while attempting to generate a restart condition	

- Notes 1.** When the WTIM0 bit (bit 3 of IICA control register 00 (IICCTL00)) = 1, an interrupt request occurs at the falling edge of the ninth clock. When WTIM0 = 0 and the extension code's slave address is received, an interrupt request occurs at the falling edge of the eighth clock.
- 2.** When there is a chance that arbitration will occur, set SPIE0 = 1 for master device operation.

Remark SPIE0: Bit 4 of IICA control register 00 (IICCTL00)

13.5.13 Wakeup function

The I²C bus slave function is a function that generates an interrupt request signal (INTIICA0) when a local address and extension code have been received.

This function makes processing more efficient by preventing unnecessary INTIICA0 signal from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has generated a start condition) to a slave device.

However, when a stop condition is detected, bit 4 (SPIE0) of IICA control register 00 (IICCTL00) is set regardless of the wakeup function, and this determines whether interrupt requests are enabled or disabled.

To use the wakeup function in the STOP mode, set the WUP0 bit to 1. Addresses can be received regardless of the operation clock. An interrupt request signal (INTIICA0) is also generated when a local address and extension code have been received. Operation returns to normal operation by using an instruction to clear (0) the WUP0 bit after this interrupt has been generated.

Figure 13-22 shows the flow for setting WUP0 = 1 and Figure 13-23 shows the flow for setting WUP0 = 0 upon an address match.

Figure 13-22. Flow When Setting WUP0 = 1

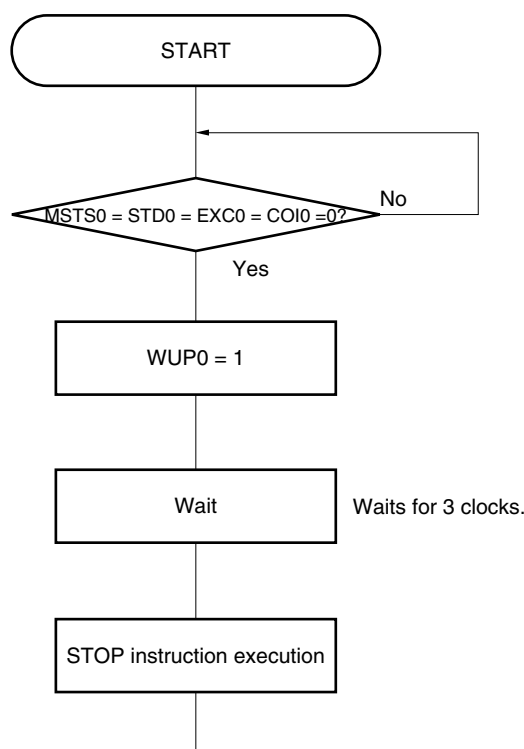
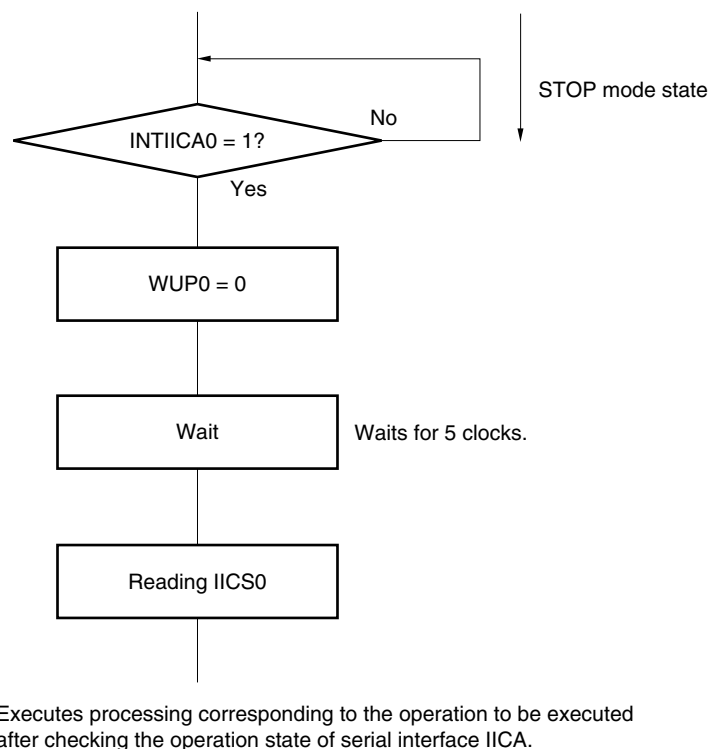
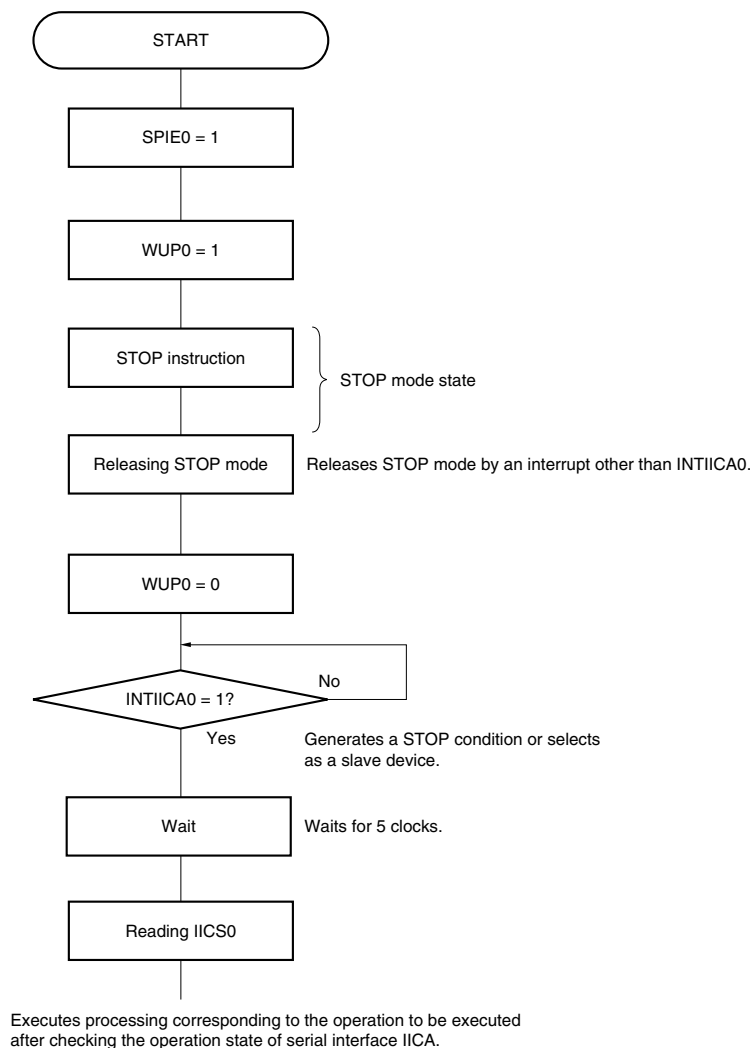


Figure 13-23. Flow When Setting WUP0 = 0 upon Address Match (Including Extension Code Reception)

Use the following flows to perform the processing to release the STOP mode other than by an interrupt request (INTIICA0) generated from serial interface IICA.

- Master device operation: Flow shown in Figure 13-24
- Slave device operation: Same as the flow in Figure 13-23

Figure 13-24. When Operating as Master Device after Releasing STOP Mode other than by INTIICA0

13.5.14 Communication reservation

(1) When communication reservation function is enabled (bit 0 (IICRSV) of IICA flag register 0 (IICF0) = 0)

To start master device communications when not currently using a bus, a communication reservation can be made to enable transmission of a start condition when the bus is released. There are two modes under which the bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ is not returned and the bus was released by setting bit 6 (LREL0) of IICA control register 00 (IICCTL00) to 1 and saving communication).

If bit 1 (STT0) of the IICCTL00 register is set to 1 while the bus is not used (after a stop condition is detected), a start condition is automatically generated and wait state is set.

If an address is written to the IICA shift register 0 (IICA0) after bit 4 (SPIE0) of the IICCTL00 register was set to 1, and it was detected by generation of an interrupt request signal (INTIICA0) that the bus was released (detection of the stop condition), then the device automatically starts communication as the master. Data written to the IICA0 register before the stop condition is detected is invalid.

When the STT0 bit has been set to 1, the operation mode (as start condition or as communication reservation) is determined according to the bus status.

- If the bus has been released a start condition is generated
- If the bus has not been released (standby mode) communication reservation

Check whether the communication reservation operates or not by using the MSTS0 bit (bit 7 of the IICA status register 0 (IICS0)) after the STT0 bit is set to 1 and the wait time elapses.

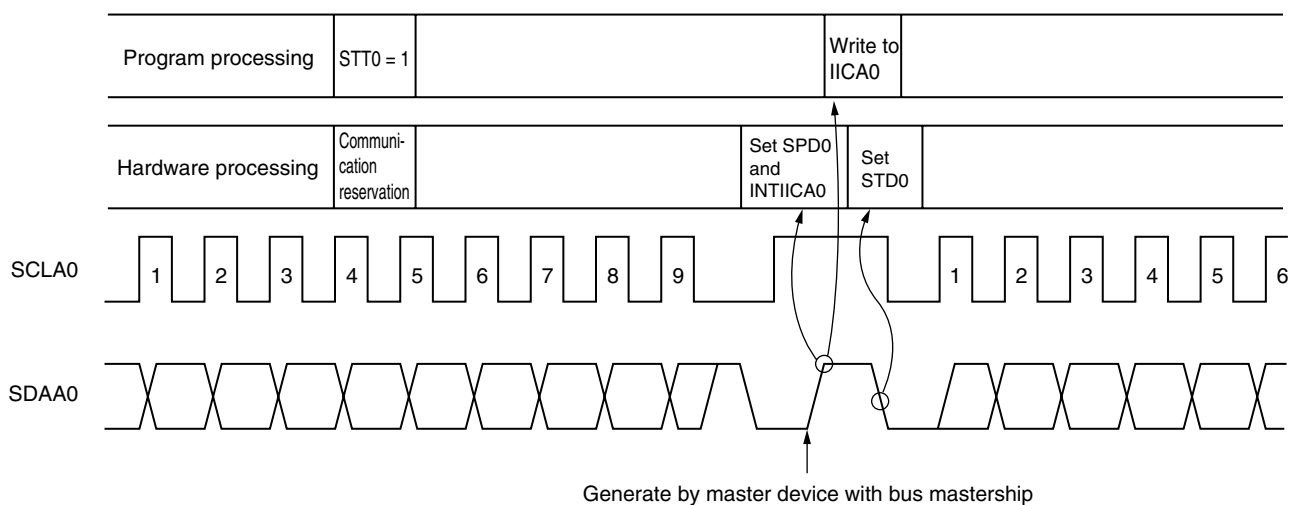
Use software to secure the wait time calculated by the following expression.

Wait time from setting STT0 = 1 to checking the MSTS0 flag:
 $(IICWL0 \text{ setting value} + IICWH0 \text{ setting value} + 4) + t_F \times 2 \times f_{CLK} [\text{clocks}]$

Remark IICWL0: IICA low-level width setting register 0
 IICWH0: IICA high-level width setting register 0
 t_F : SDAA0 and SCLA0 signal falling times
 f_{CLK} : CPU/peripheral hardware clock frequency

Figure 13-25 shows the communication reservation timing.

Figure 13-25. Communication Reservation Timing



Remark IICA0: IICA shift register 0
 STT0: Bit 1 of IICA control register 00 (IICCTL00)
 STD0: Bit 1 of IICA status register 0 (IICS0)
 SPD0: Bit 0 of IICA status register 0 (IICS0)

Communication reservations are accepted via the timing shown in Figure 13-26. After bit 1 (STD0) of the IICA status register 0 (IICS0) is set to 1, a communication reservation can be made by setting bit 1 (STT0) of IICA control register 00 (IICCTL00) to 1 before a stop condition is detected.

Figure 13-26. Timing for Accepting Communication Reservations

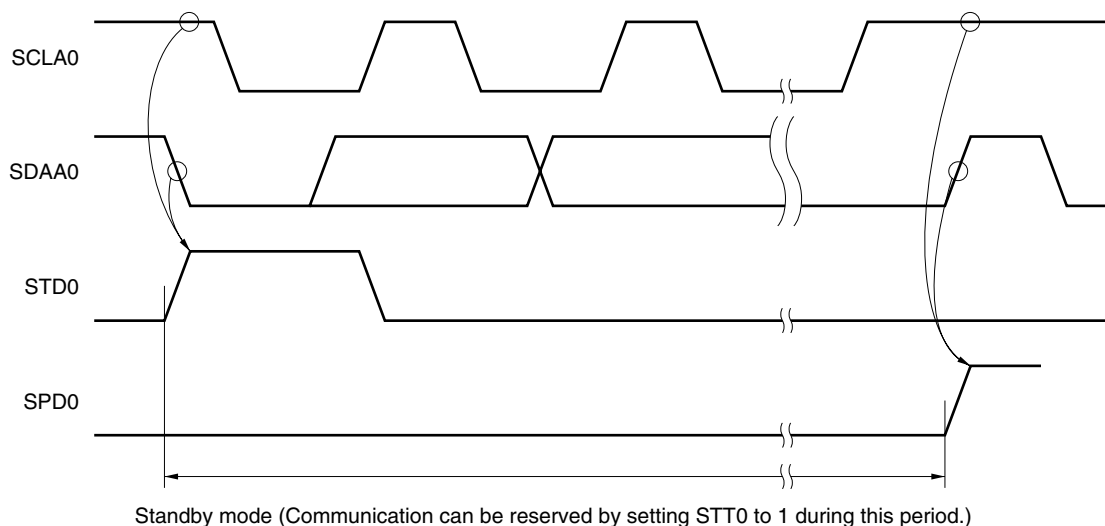
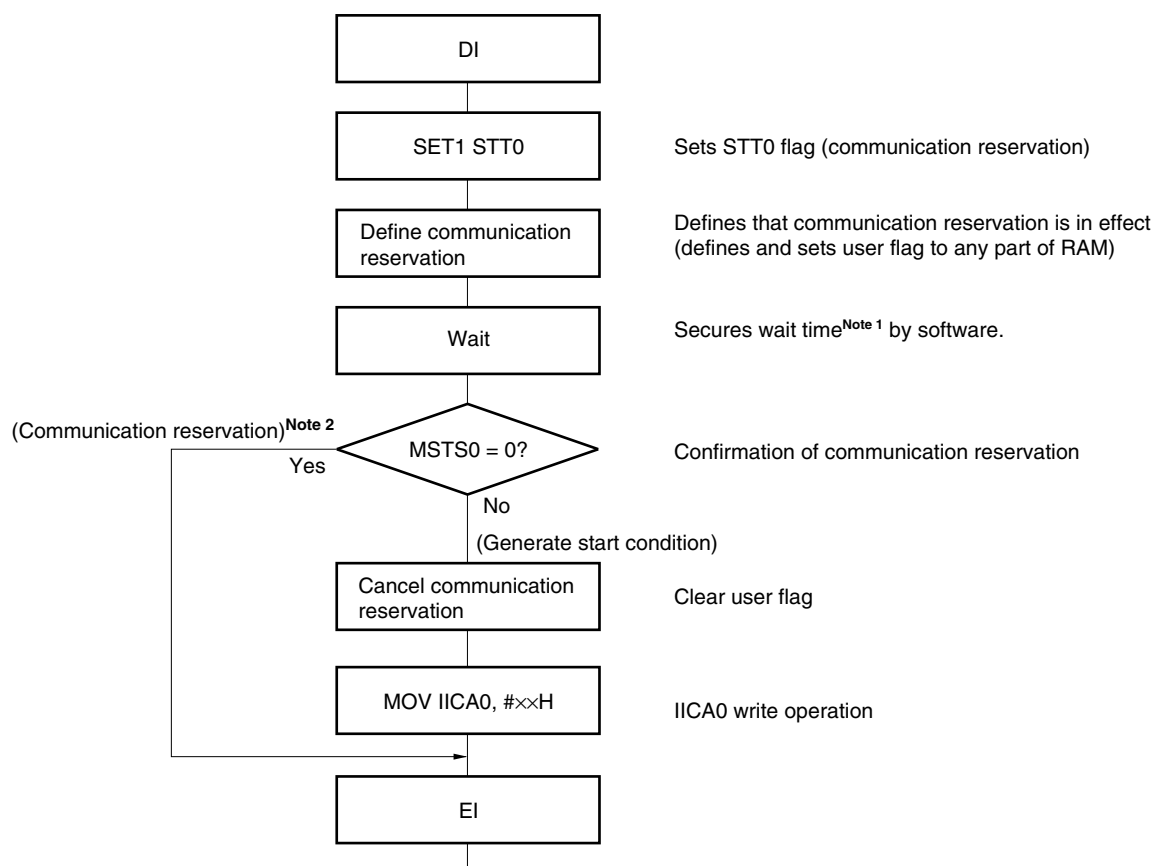


Figure 13-27 shows the communication reservation protocol.

Figure 13-27. Communication Reservation Protocol

Notes 1. The wait time is calculated as follows.

$(\text{IICWL0 setting value} + \text{IICWH0 setting value} + 4) + t_F \times 2 \times f_{\text{CLK}} [\text{clocks}]$

- 2.** The communication reservation operation executes a write to the IICA shift register 0 (IICA0) when a stop condition interrupt request occurs.

Remark STT0: Bit 1 of IICA control register 00 (IICCTL00)

MSTS0: Bit 7 of IICA status register 0 (IICS0)

IICA0: IICA shift register 0

IICWL0: IICA low-level width setting register 0

IICWH0: IICA high-level width setting register 0

t_F : SDAA0 and SCLA0 signal falling times

f_{CLK} : CPU/peripheral hardware clock frequency

(2) When communication reservation function is disabled (bit 0 (IICRSV) of IICA flag register 0 (IICF0) = 1)

When bit 1 (STT0) of IICA control register 00 (IICCTL00) is set to 1 when the bus is not used in a communication during bus communication, this request is rejected and a start condition is not generated. The following two statuses are included in the status where bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{\text{ACK}}$ is not returned and the bus was released by setting bit 6 (LREL0) of the IICCTL00 register to 1 and saving communication)

To confirm whether the start condition was generated or request was rejected, check STCF (bit 7 of the IICF0 register). It takes up to 5 clocks until the STCF bit is set to 1 after setting STT0 = 1. Therefore, secure the time by software.

13.5.15 Cautions

(1) When STCEN = 0

Immediately after I²C operation is enabled (IICE0 = 1), the bus communication status (IICBSY = 1) is recognized regardless of the actual bus status. When changing from a mode in which no stop condition has been detected to a master device communication mode, first generate a stop condition to release the bus, then perform master device communication.

When using multiple masters, it is not possible to perform master device communication when the bus has not been released (when a stop condition has not been detected).

Use the following sequence for generating a stop condition.

<1> Set IICA control register 01 (IICCTL01).

<2> Set bit 7 (IICE0) of IICA control register 00 (IICCTL00) to 1.

<3> Set bit 0 (SPT0) of the IICCTL00 register to 1.

(2) When STCEN = 1

Immediately after I²C operation is enabled (IICE0 = 1), the bus released status (IICBSY = 0) is recognized regardless of the actual bus status. To generate the first start condition (STT0 = 1), it is necessary to confirm that the bus has been released, so as to not disturb other communications.

(3) If other I²C communications are already in progress

If I²C operation is enabled and the device participates in communication already in progress when the SDAA0 pin is low and the SCLA0 pin is high, the macro of I²C recognizes that the SDAA0 pin has gone low (detects a start condition). If the value on the bus at this time can be recognized as an extension code, $\overline{ACK}$ is returned, but this interferes with other I²C communications. To avoid this, start I²C in the following sequence.

<1> Clear bit 4 (SPIE0) of the IICCTL00 register to 0 to disable generation of an interrupt request signal (INTIICA0) when the stop condition is detected.

<2> Set bit 7 (IICE0) of the IICCTL00 register to 1 to enable the operation of I²C.

<3> Wait for detection of the start condition.

<4> Set bit 6 (LREL0) of the IICCTL00 register to 1 before $\overline{ACK}$ is returned (4 to 80 clocks after setting the IICE0 bit to 1), to forcibly disable detection.

(4) Setting the STT0 and SPT0 bits (bits 1 and 0 of the IICCTL00 register) again after they are set and before they are cleared to 0 is prohibited.

(5) When transmission is reserved, set the SPIE0 bit (bit 4 of the IICCTL0 register) to 1 so that an interrupt request is generated when the stop condition is detected. Transfer is started when communication data is written to the IICA shift register 0 (IICA0) after the interrupt request is generated. Unless the interrupt is generated when the stop condition is detected, the device stops in the wait state because the interrupt request is not generated when communication is started. However, it is not necessary to set the SPIE0 bit to 1 when the MST0 bit (bit 7 of the IICA status register 0 (IICS0)) is detected by software.

13.5.16 Communication operations

The following shows three operation procedures with the flowchart.

(1) Master operation in single master system

The flowchart when using the RL78/G1A as the master in a single master system is shown below.

This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

(2) Master operation in multimaster system

In the I²C bus multimaster system, whether the bus is released or used cannot be judged by the I²C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the RL78/G1A takes part in a communication with bus released state.

This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the RL78/G1A loses in arbitration and is specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

(3) Slave operation

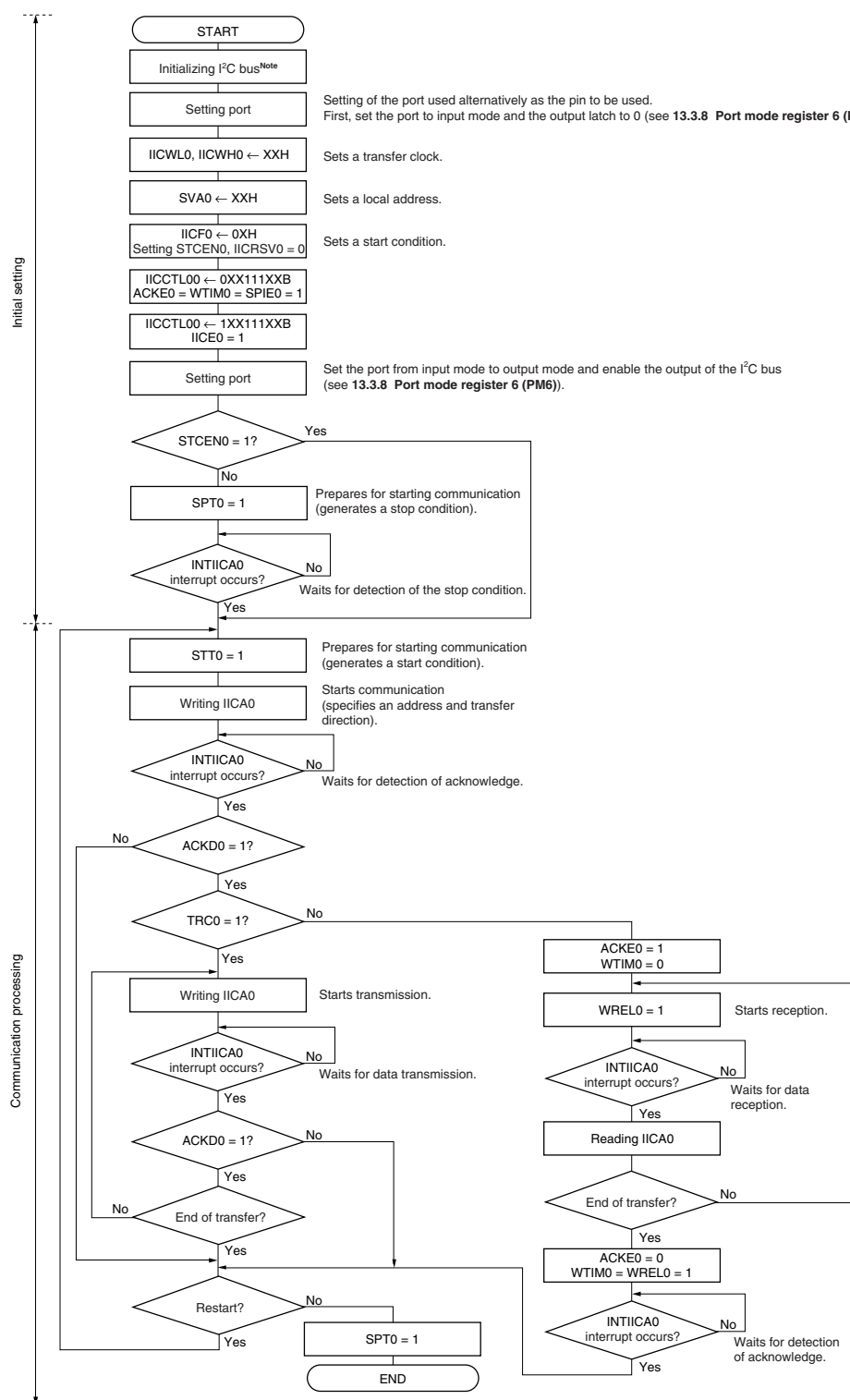
An example of when the RL78/G1A is used as the I²C bus slave is shown below.

When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIICA0 interrupt occurrence (communication waiting). When an INTIICA0 interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.

By checking the flags, necessary communication processing is performed.

(1) Master operation in single-master system

Figure 13-28. Master Operation in Single-Master System

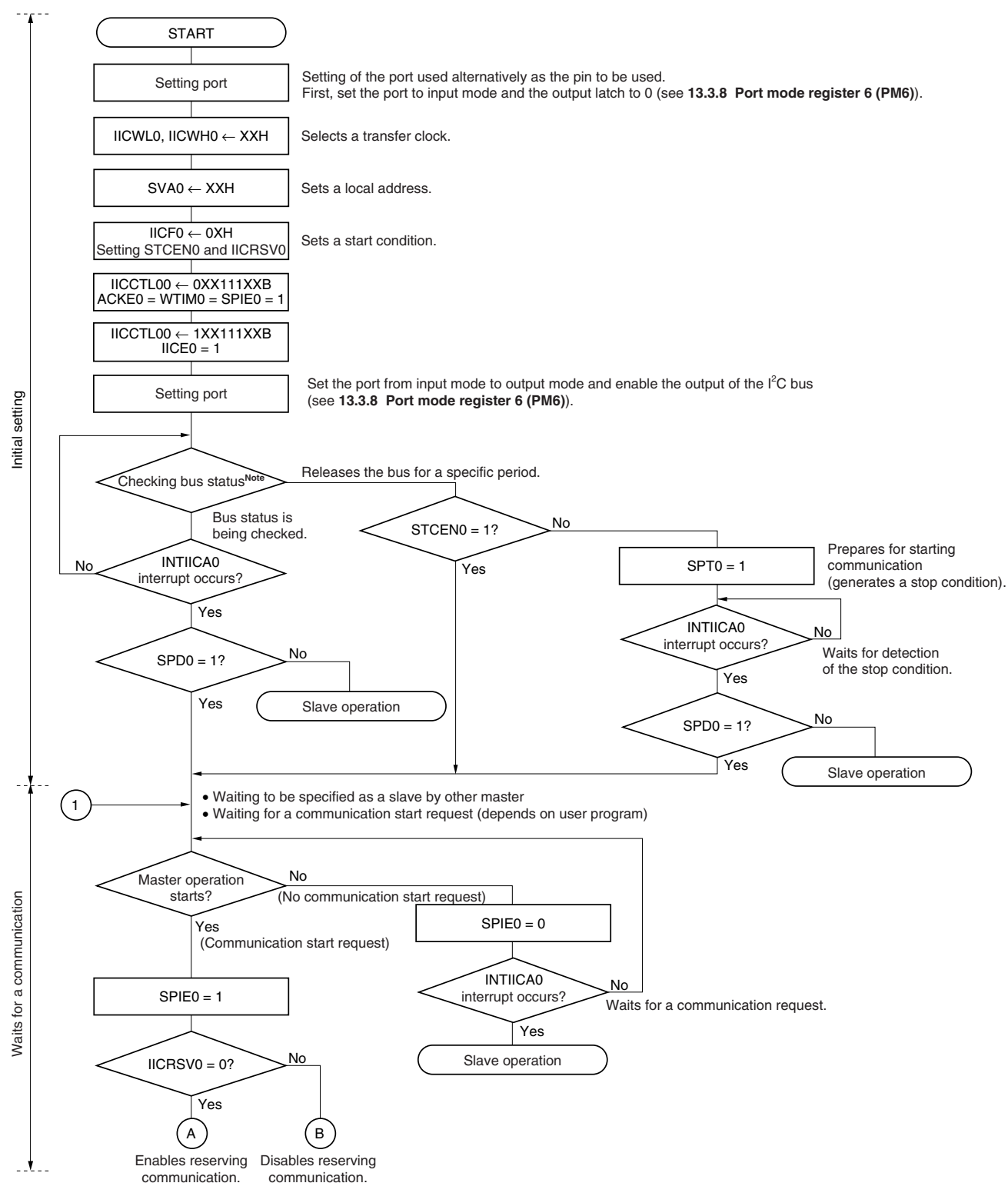


Note Release (SCLA0 and SDAA0 pins = high level) the I²C bus in conformance with the specifications of the product that is communicating. If EEPROM is outputting a low level to the SDAA0 pin, for example, set the SCLA0 pin in the output port mode, and output a clock pulse from the output port until the SDAA0 pin is constantly at high level.

Remark Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

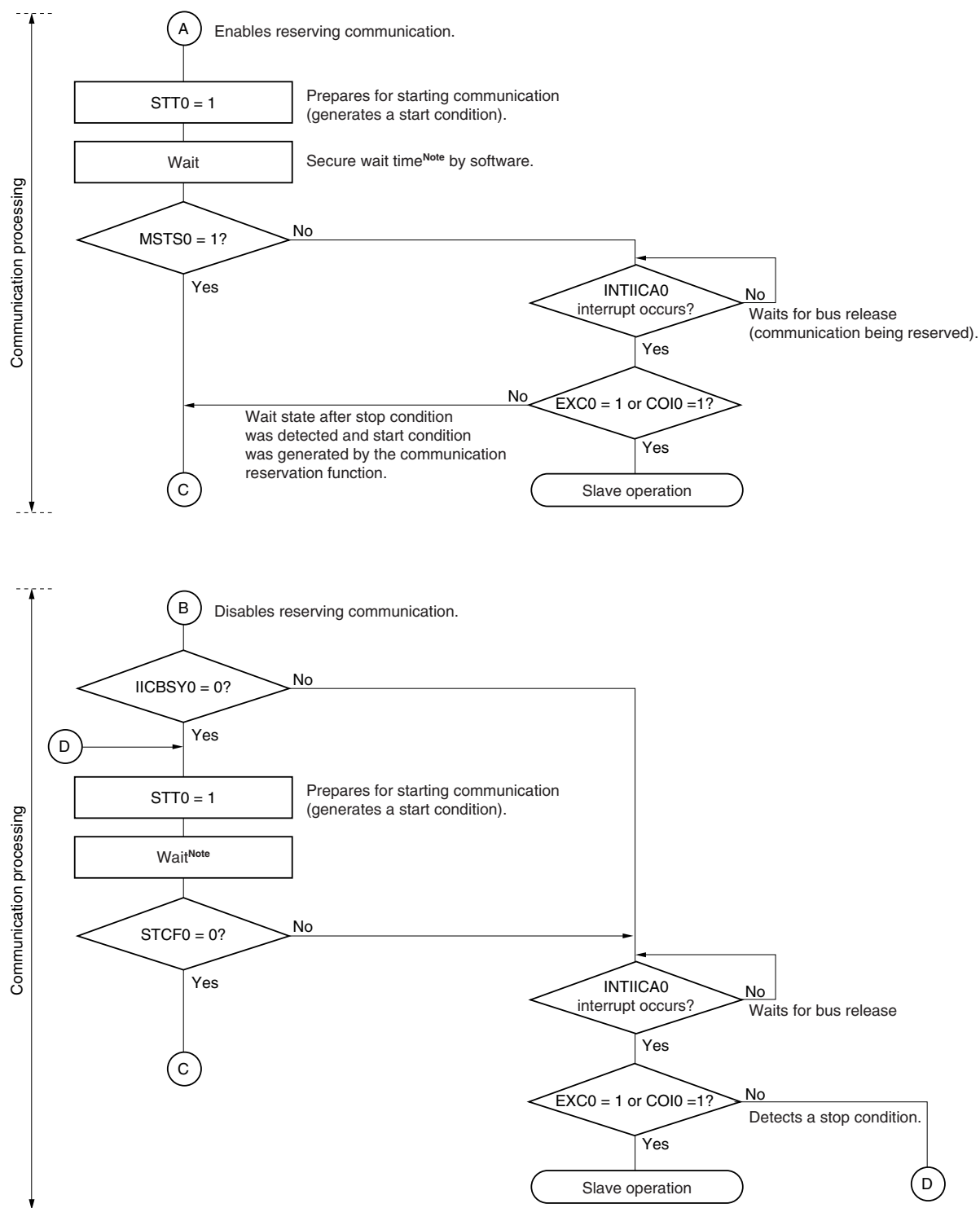
(2) Master operation in multi-master system

Figure 13-29. Master Operation in Multi-Master System (1/3)



Note Confirm that the bus is released (CLD0 bit = 1, DAD0 bit = 1) for a specific period (for example, for a period of one frame). If the SDAA0 pin is constantly at low level, decide whether to release the I²C bus (SCLA0 and SDAA0 pins = high level) in conformance with the specifications of the product that is communicating.

Figure 13-29. Master Operation in Multi-Master System (2/3)

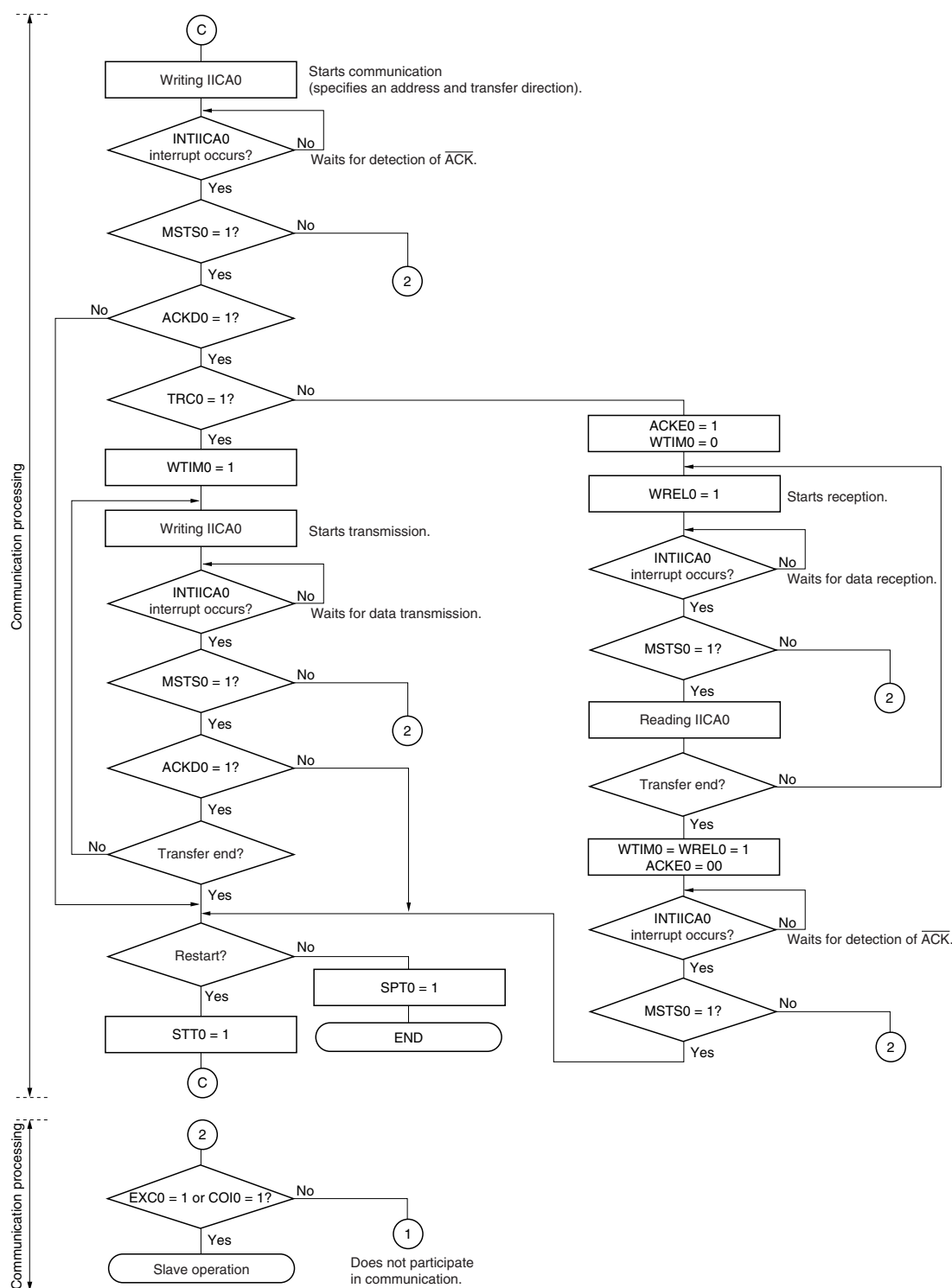


Note The wait time is calculated as follows.

$$(\text{IICWL0 setting value} + \text{IICWH0 setting value} + 4) \times f_{\text{CLK}} + t_{\text{F}} \times 2 \text{ [clocks]}$$

Remark IICWL0: IICA low-level width setting register 0
 IICWH0: IICA high-level width setting register 0
 t_{F} : SDAA0 and SCLA0 signal falling times
 f_{CLK} : CPU/peripheral hardware clock frequency

Figure 13-29. Master Operation in Multi-Master System (3/3)



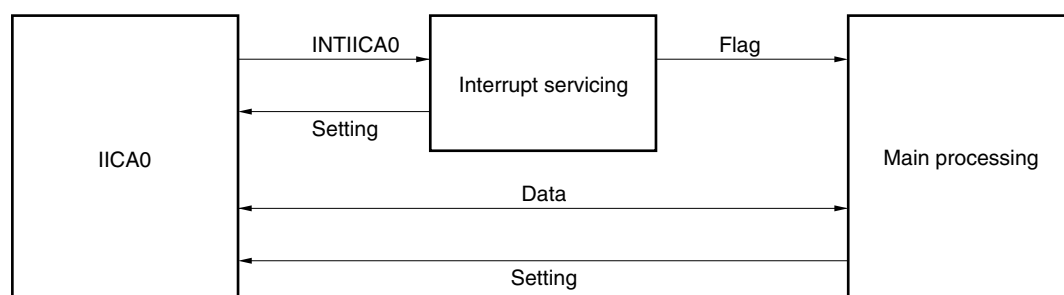
- Remarks**
1. Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.
 2. To use the device as a master in a multi-master system, read the MST0 bit each time interrupt INTIICA0 has occurred to check the arbitration result.
 3. To use the device as a slave in a multi-master system, check the status by using the IICA status register 0 (IICS0) and IICA flag register 0 (IICF0) each time interrupt INTIICA0 has occurred, and determine the processing to be performed next.

(3) Slave operation

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIICA0 interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICA0 interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICA0.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

<2> Ready flag

This flag indicates that data communication is enabled. Its function is the same as the INTIICA0 interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as the TRC0 bit.

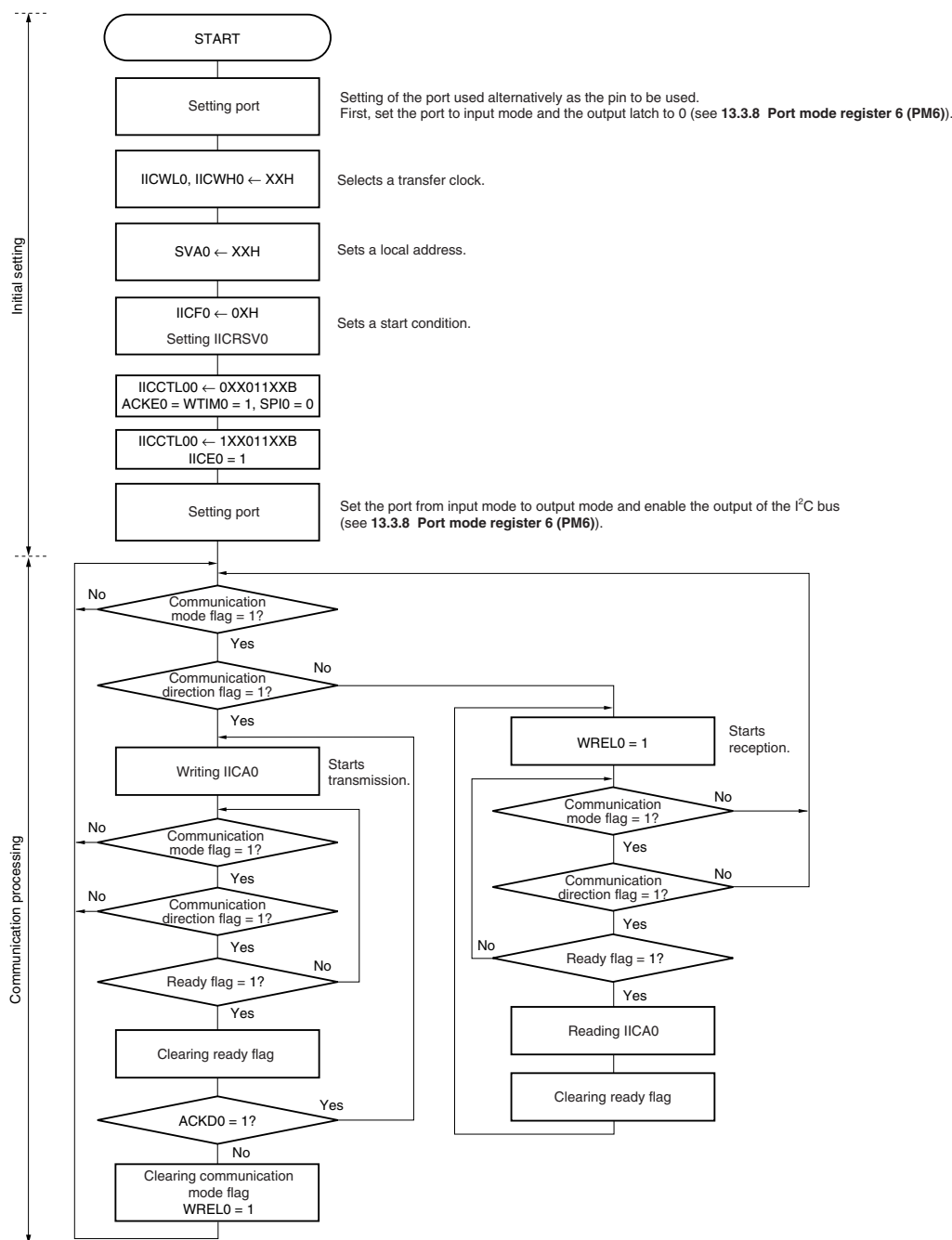
The main processing of the slave operation is explained next.

Start serial interface IICA and wait until communication is enabled. When communication is enabled, execute communication by using the communication mode flag and ready flag (processing of the stop condition and start condition is performed by an interrupt. Here, check the status by using the flags).

The transmission operation is repeated until the master no longer returns $\overline{\text{ACK}}$. If $\overline{\text{ACK}}$ is not returned from the master, communication is completed.

For reception, the necessary amount of data is received. When communication is completed, $\overline{\text{ACK}}$ is not returned as the next data. After that, the master generates a stop condition or restart condition. Exit from the communication status occurs in this way.

Figure 13-30. Slave Operation Flowchart (1)



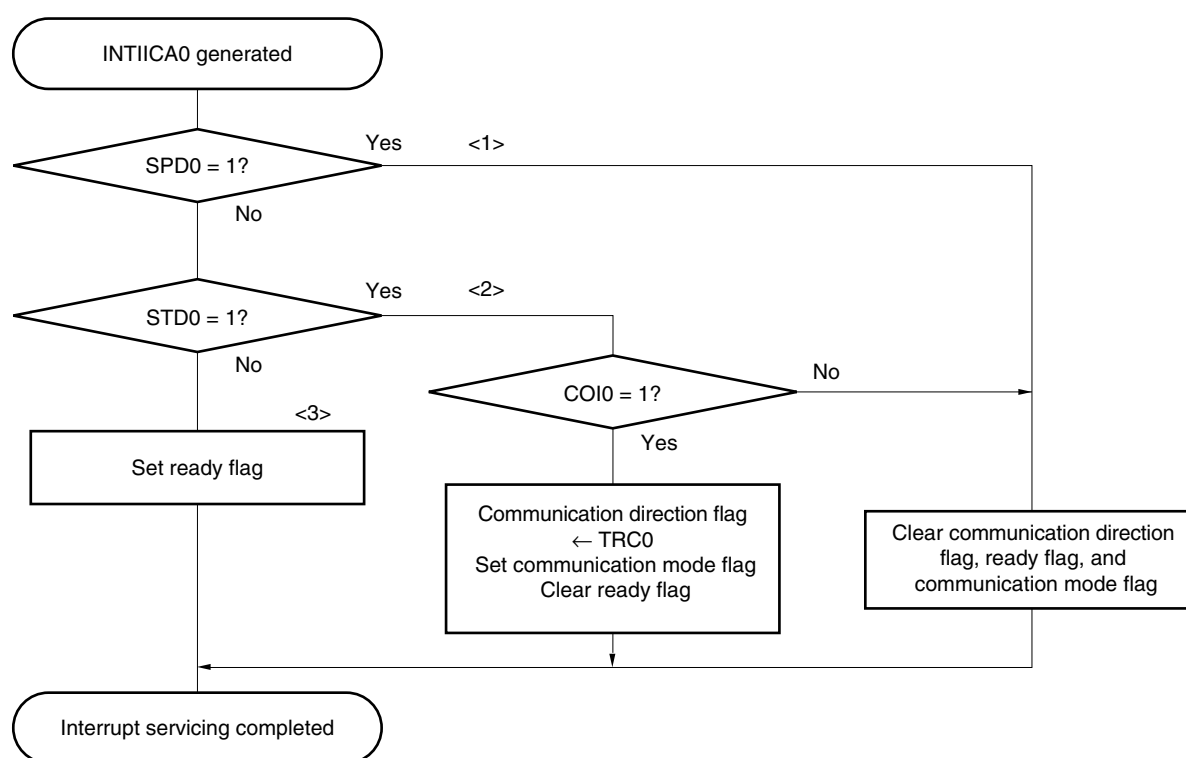
Remark Conform to the specifications of the product that is in communication, regarding the transmission and reception formats.

An example of the processing procedure of the slave with the INTIICA0 interrupt is explained below (processing is performed assuming that no extension code is used). The INTIICA0 interrupt checks the status, and the following operations are performed.

- <1> Communication is stopped if the stop condition is issued.
- <2> If the start condition is issued, the address is checked and communication is completed if the address does not match. If the address matches, the communication mode is set, wait is cancelled, and processing returns from the interrupt (the ready flag is cleared).
- <3> For data transmit/receive, only the ready flag is set. Processing returns from the interrupt with the I²C bus remaining in the wait state.

Remark <1> to <3> above correspond to <1> to <3> in Figure 13-31 Slave Operation Flowchart (2).

Figure 13-31. Slave Operation Flowchart (2)



13.5.17 Timing of I²C interrupt request (INTIICA0) occurrence

The timing of transmitting or receiving data and generation of interrupt request signal INTIICA0, and the value of the IICA status register 0 (IICS0) when the INTIICA0 signal is generated are shown below.

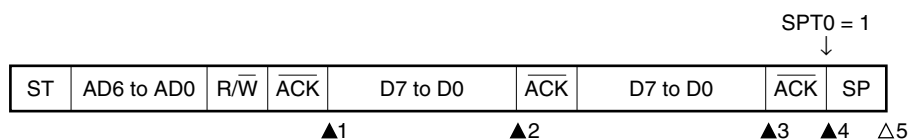
Remark

ST:	Start condition
AD6 to AD0:	Address
R/ $\overline{W}$:	Transfer direction specification
ACK:	Acknowledge
D7 to D0:	Data
SP:	Stop condition

(1) Master device operation

(a) Start ~ Address ~ Data ~ Data ~ Stop (transmission/reception)

(i) When WTIM0 = 0



▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000×000B

▲3: IICS0 = 1000×000B (Sets the WTIM0 bit to 1)^{Note}▲4: IICS0 = 1000××00B (Sets the SPT0 bit to 1)^{Note}

△5: IICS0 = 00000001B

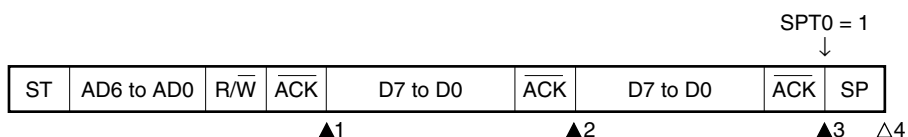
Note To generate a stop condition, set the WTIM0 bit to 1 and change the timing for generating the INTIICA0 interrupt request signal.

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(ii) When WTIM0 = 1



▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000×100B

▲3: IICS0 = 1000××00B (Sets the SPT0 bit to 1)

△4: IICS0 = 00000001B

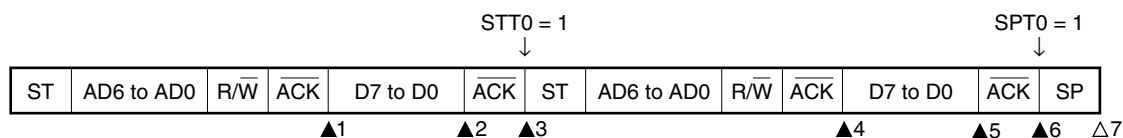
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

(i) When WTIM0 = 0



▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000×000B (Sets the WTIM0 bit to 1)^{Note 1}▲3: IICS0 = 1000××00B (Clears the WTIM0 bit to 0^{Note 2}, sets the STT0 bit to 1)

▲4: IICS0 = 1000×110B

▲5: IICS0 = 1000×000B (Sets the WTIM0 bit to 1)^{Note 3}

▲6: IICS0 = 1000××00B (Sets the SPT0 bit to 1)

Δ7: IICS0 = 00000001B

Notes 1. To generate a start condition, set the WTIM0 bit to 1 and change the timing for generating the INTIICA0 interrupt request signal.

2. Clear the WTIM0 bit to 0 to restore the original setting.

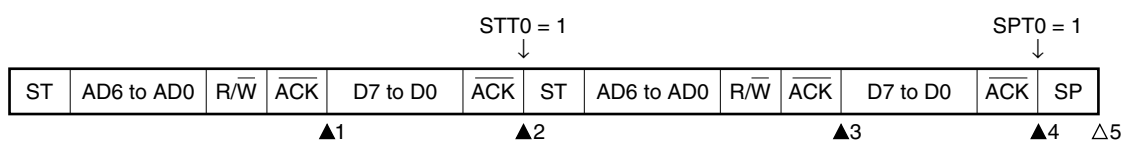
3. To generate a stop condition, set the WTIM0 bit to 1 and change the timing for generating the INTIICA0 interrupt request signal.

Remark ▲: Always generated

Δ: Generated only when SPIE0 = 1

×: Don't care

(ii) When WTIM0 = 1



▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000××00B (Sets the STT0 bit to 1)

▲3: IICS0 = 1000×110B

▲4: IICS0 = 1000××00B (Sets the SPT0 bit to 1)

Δ5: IICS0 = 00000001B

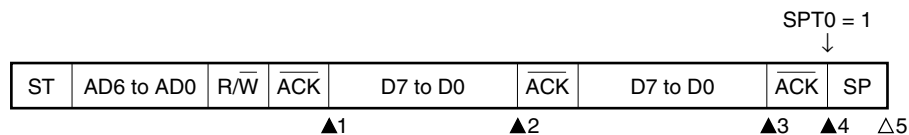
Remark ▲: Always generated

Δ: Generated only when SPIE0 = 1

×: Don't care

(c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

(i) When WTIM0 = 0



▲1: IICS0 = 1010×110B

▲2: IICS0 = 1010×000B

▲3: IICS0 = 1010×000B (Sets the WTIM0 bit to 1)^{Note}

▲4: IICS0 = 1010××00B (Sets the SPT0 bit to 1)

Δ5: IICS0 = 00000001B

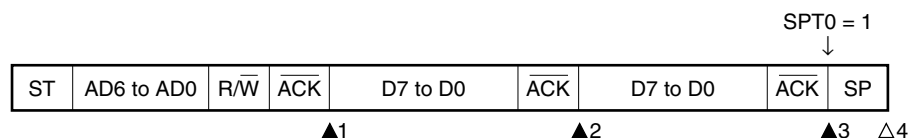
Note To generate a stop condition, set the WTIM0 bit to 1 and change the timing for generating the INTIICA0 interrupt request signal.

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(ii) When WTIM0 = 1



▲1: IICS0 = 1010×110B

▲2: IICS0 = 1010×100B

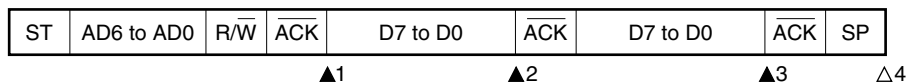
▲3: IICS0 = 1010××00B (Sets the SPT0 bit to 1)

Δ4: IICS0 = 00001001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(2) Slave device operation (slave address data reception)**(a) Start ~ Address ~ Data ~ Data ~ Stop****(i) When WTIM0 = 0**

▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001×000B

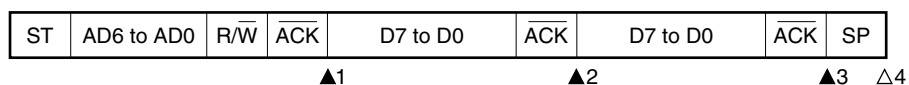
▲3: IICS0 = 0001×000B

△4: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(ii) When WTIM0 = 1

▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001×100B

▲3: IICS0 = 0001××00B

△4: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop**(i) When WTIM0 = 0 (after restart, matches with SVA0)**

▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001×000B

▲3: IICS0 = 0001×110B

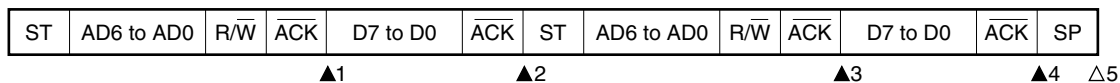
▲4: IICS0 = 0001×000B

△5: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(ii) When WTIM0 = 1 (after restart, matches with SVA0)

▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001××00B

▲3: IICS0 = 0001×110B

▲4: IICS0 = 0001××00B

△5: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(c) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, does not match address (= extension code))



▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001×000B

▲3: IICS0 = 0010×010B

▲4: IICS0 = 0010×000B

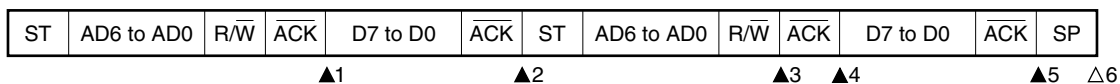
△5: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

(ii) When WTIM0 = 1 (after restart, does not match address (= extension code))



▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001××00B

▲3: IICS0 = 0010×010B

▲4: IICS0 = 0010×110B

▲5: IICS0 = 0010××00B

△6: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

(d) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop**(i) When WTIM0 = 0 (after restart, does not match address (= not extension code))**

<R>



▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001×000B

▲3: IICS_n = 00000×10B

△4: IICS0 = 00000001B

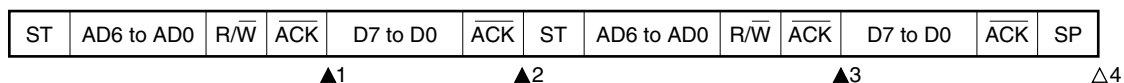
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

(ii) When WTIM0 = 1 (after restart, does not match address (= not extension code))

<R>



▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001××00B

▲3: IICS_n = 00000×10B

△4: IICS0 = 00000001B

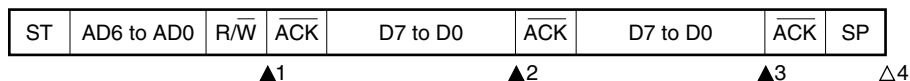
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

(3) Slave device operation (when receiving extension code)

The device is always participating in communication when it receives an extension code.

(a) Start ~ Code ~ Data ~ Data ~ Stop**(i) When WTIM0 = 0**

▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×000B

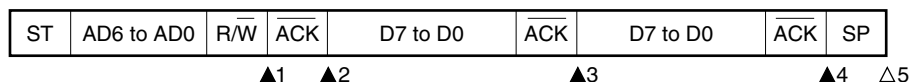
▲3: IICS0 = 0010×000B

△4: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(ii) When WTIM0 = 1

▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×110B

▲3: IICS0 = 0010×100B

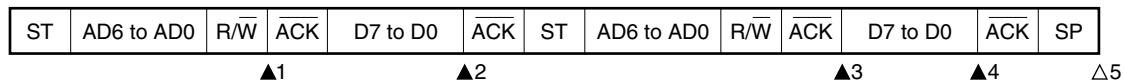
▲4: IICS0 = 0010××00B

△5: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(b) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop**(i) When WTIM0 = 0 (after restart, matches SVA0)**

▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×000B

▲3: IICS0 = 0001×110B

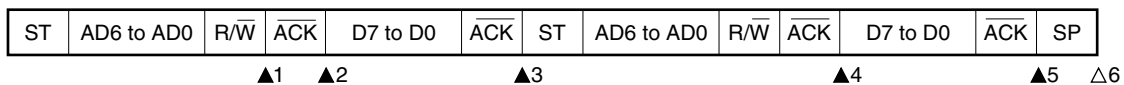
▲4: IICS0 = 0001×000B

△5: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(ii) When WTIM0 = 1 (after restart, matches SVA0)

▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×110B

▲3: IICS0 = 0010××00B

▲4: IICS0 = 0001×110B

▲5: IICS0 = 0001××00B

△6: IICS0 = 00000001B

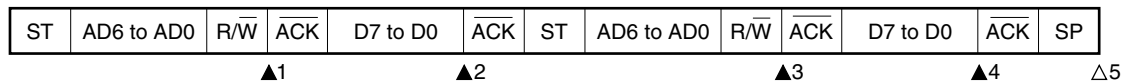
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(c) Start ~ Code ~ Data ~ Start ~ Code ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, extension code reception)



▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×000B

▲3: IICS0 = 0010×010B

▲4: IICS0 = 0010×000B

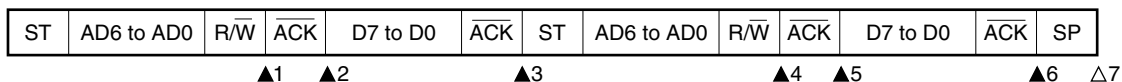
△5: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(ii) When WTIM0 = 1 (after restart, extension code reception)



▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×110B

▲3: IICS0 = 0010××00B

▲4: IICS0 = 0010×010B

▲5: IICS0 = 0010×110B

▲6: IICS0 = 0010××00B

△7: IICS0 = 00000001B

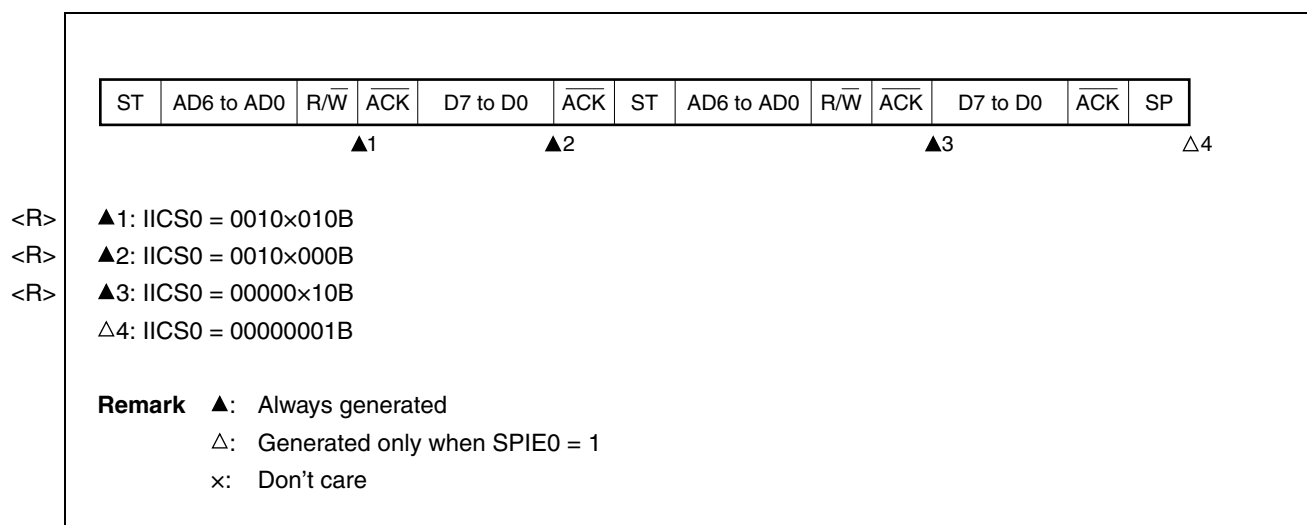
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

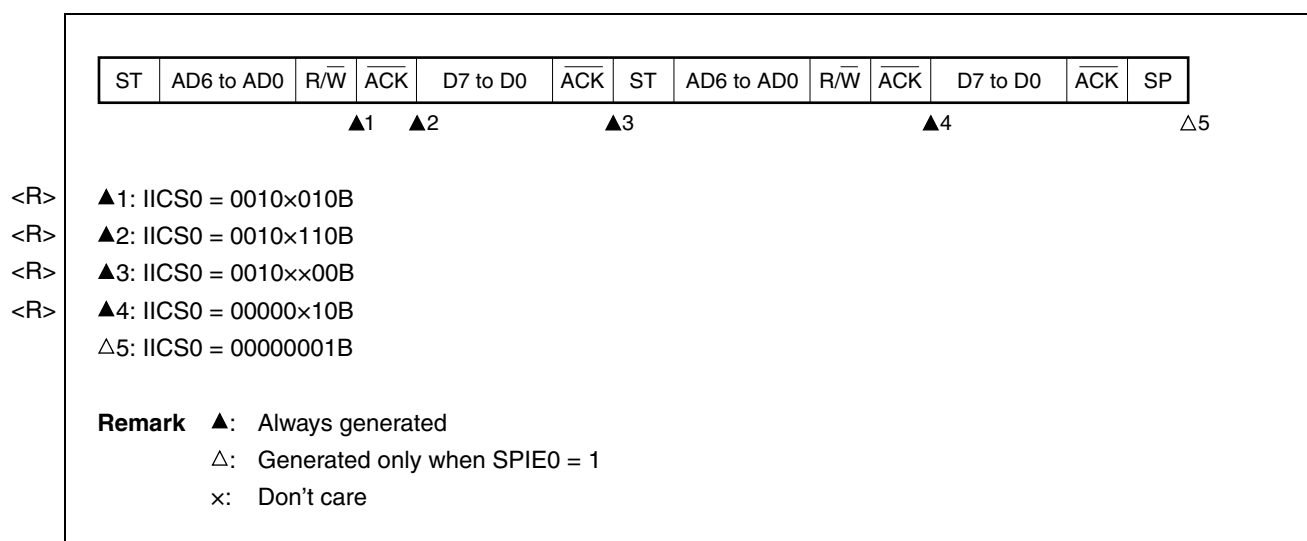
×: Don't care

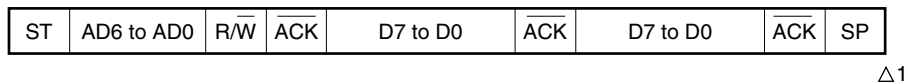
(d) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, does not match address (= not extension code))



(ii) When WTIM0 = 1 (after restart, does not match address (= not extension code))



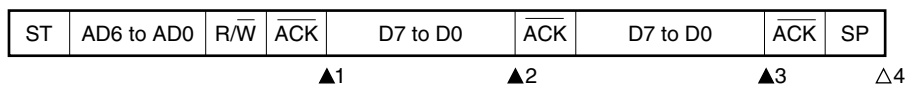
(4) Operation without communication**(a) Start ~ Code ~ Data ~ Data ~ Stop**

△1: IICS0 = 00000001B

Remark △: Generated only when SPIE0 = 1

(5) Arbitration loss operation (operation as slave after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTSO bit each time interrupt request signal INTIICA0 has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data**(i) When WTIM0 = 0**

▲1: IICS0 = 0101×110B

▲2: IICS0 = 0001×000B

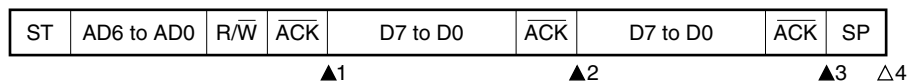
▲3: IICS0 = 0001×000B

△4: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(ii) When $WTIM0 = 1$ 

▲1: IICS0 = 0101×110B

▲2: IICS0 = 0001×100B

▲3: IICS0 = 0001××00B

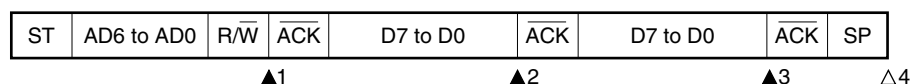
△4: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(b) When arbitration loss occurs during transmission of extension code

(i) When $WTIM0 = 0$ 

▲1: IICS0 = 0110×010B

▲2: IICS0 = 0010×000B

▲3: IICS0 = 0010×000B

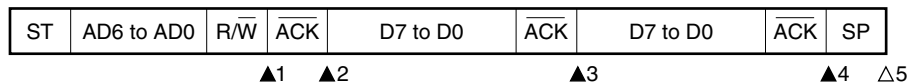
△4: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

(ii) When WTIM0 = 1



▲1: IICS0 = 0110x010B

▲2: IICS0 = 0010x110B

▲3: IICS0 = 0010x100B

▲4: IICS0 = 0010xx00B

△5: IICS0 = 00000001B

Remark ▲: Always generated

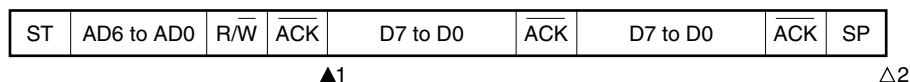
△: Generated only when SPIE0 = 1

x: Don't care

(6) Operation when arbitration loss occurs (no communication after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTS0 bit each time interrupt request signal INTIICA0 has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data (when WTIM0 = 1)

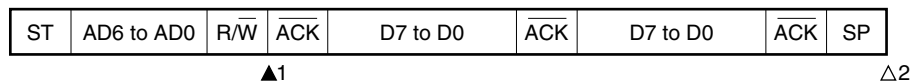


▲1: IICS0 = 01000110B

△2: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

(b) When arbitration loss occurs during transmission of extension code

▲1: IICS0 = 0110x010B

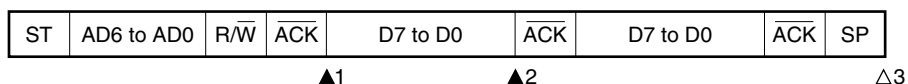
Sets LREL0 = 1 by software

△2: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

(c) When arbitration loss occurs during transmission of data**(i) When WTIM0 = 0**

▲1: IICS0 = 10001110B

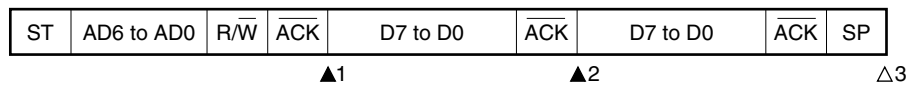
▲2: IICS0 = 01000000B

△3: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

(ii) When WTIM0 = 1



▲1: IICS0 = 10001110B

▲2: IICS0 = 01000100B

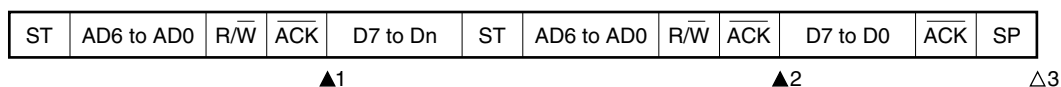
△3: IICS0 = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

(d) When loss occurs due to restart condition during data transfer

(i) Not extension code (Example: unmatched with SVA0)



▲1: IICS0 = 1000×110B

▲2: IICS0 = 01000110B

△3: IICS0 = 00000001B

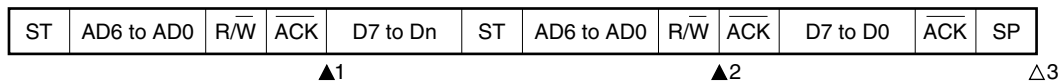
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

n = 6 to 0

(ii) Extension code



▲1: IICS0 = 1000×110B

▲2: IICS0 = 01100010B

Sets LREL0 = 1 by software

△3: IICS0 = 00000001B

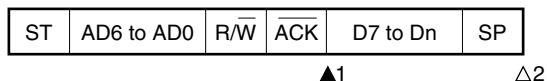
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

n = 6 to 0

(e) When loss occurs due to stop condition during data transfer



▲1: IICS0 = 10000110B

△2: IICS0 = 01000001B

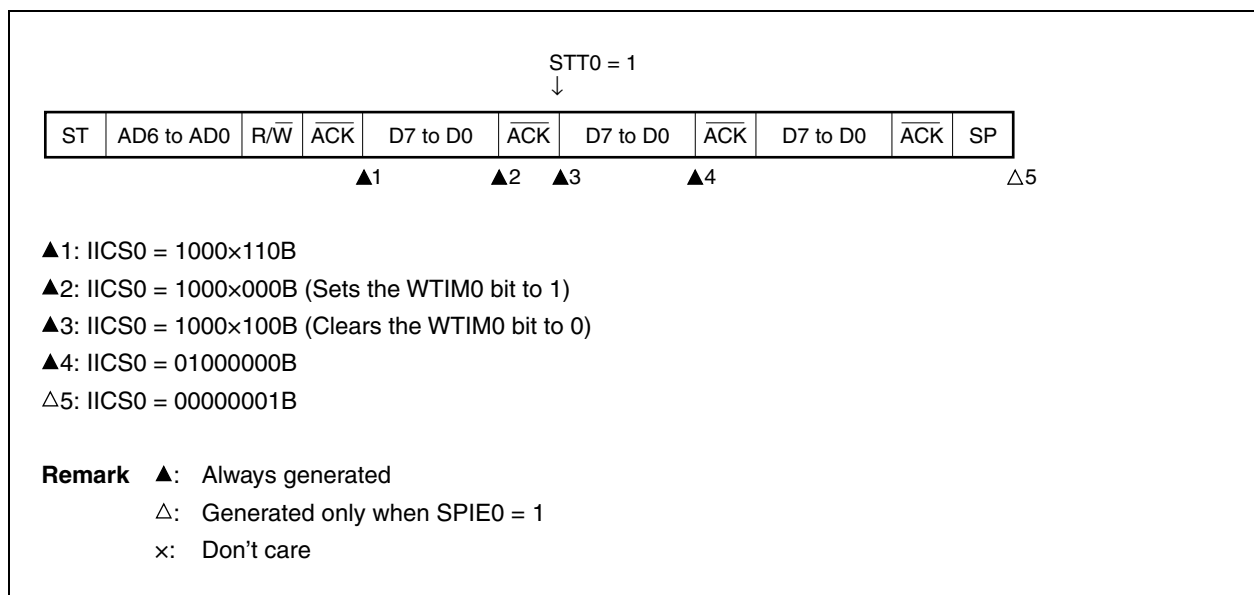
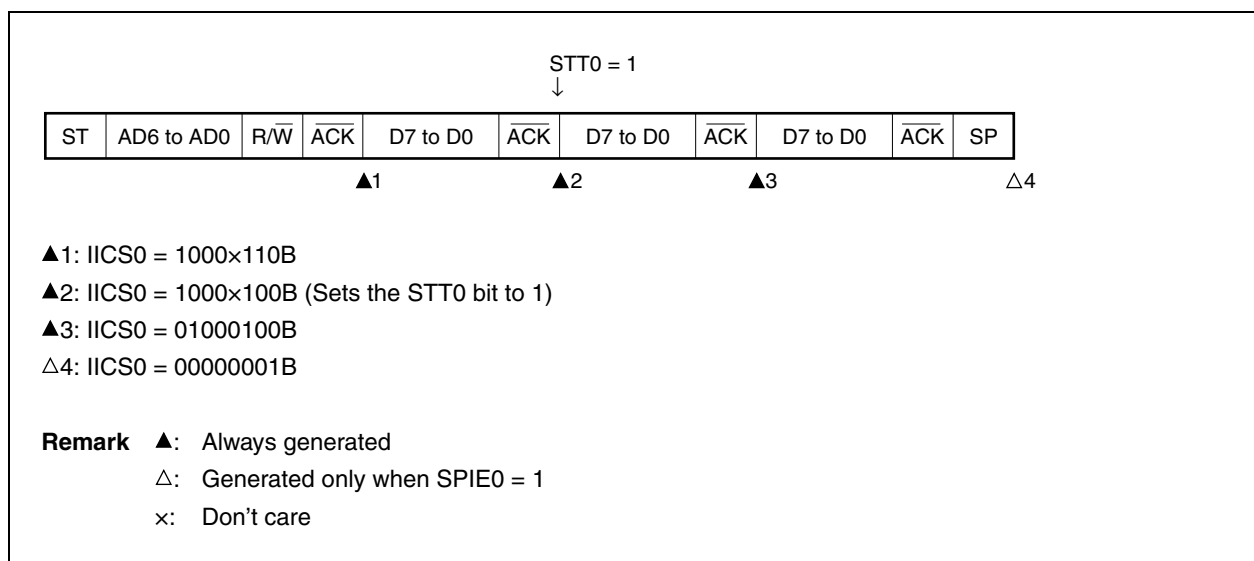
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

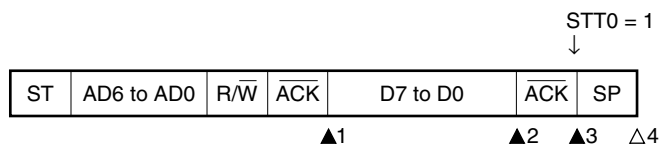
x: Don't care

n = 6 to 0

(f) When arbitration loss occurs due to low-level data when attempting to generate a restart condition

(i) When $WTIM0 = 0$ (ii) When $WTIM0 = 1$ 

(g) When arbitration loss occurs due to a stop condition when attempting to generate a restart condition

(i) When $WTIM0 = 0$ 

▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000×000B (Sets the WTIM0 bit to 1)

▲3: IICS0 = 1000××00B (Sets the STT0 bit to 1)

△4: IICS0 = 01000001B

Remark ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

(ii) When $WTIM0 = 1$ 

▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000××00B (Sets the STT0 bit to 1)

△3: IICS0 = 01000001B

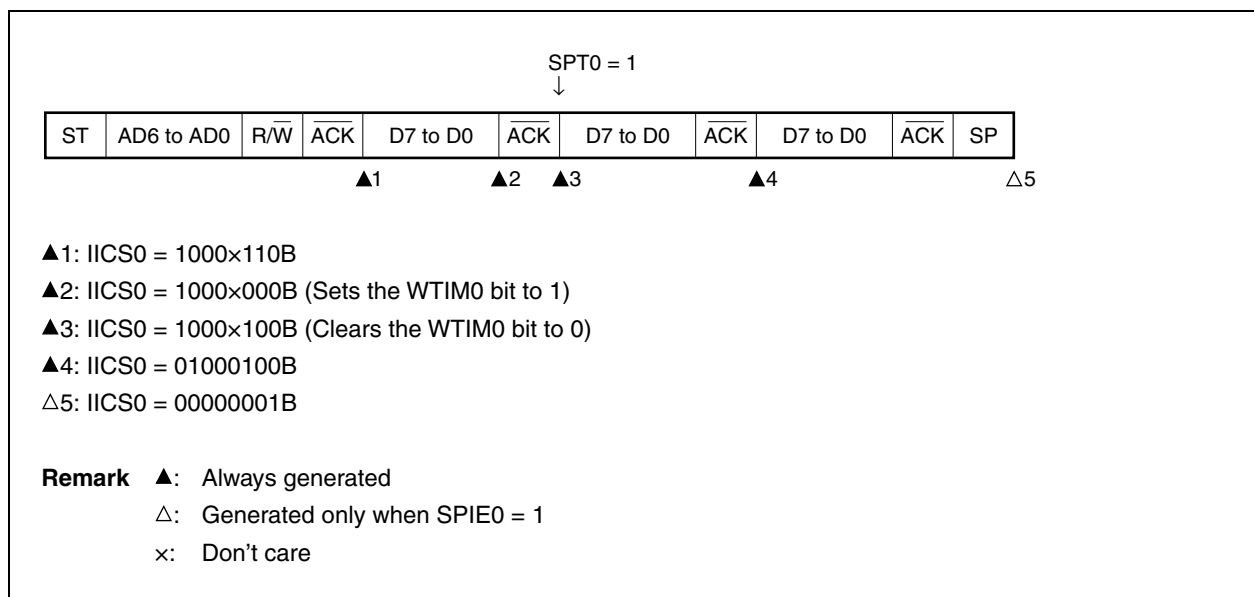
Remark ▲: Always generated

△: Generated only when SPIE0 = 1

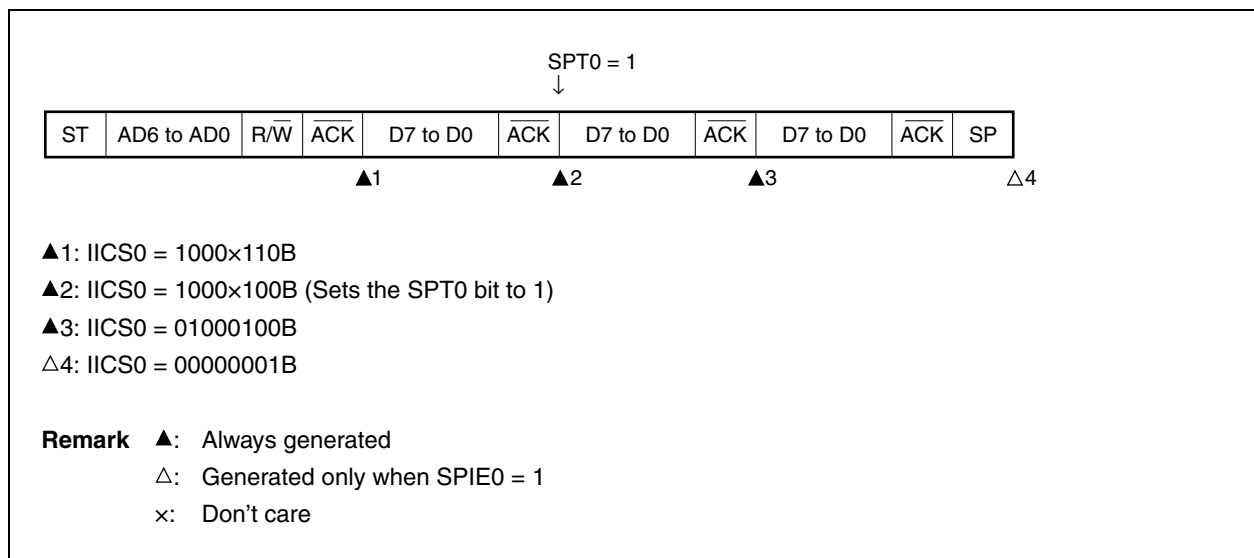
x: Don't care

(h) When arbitration loss occurs due to low-level data when attempting to generate a stop condition

(i) When $WTIM0 = 0$



(ii) When $WTIM0 = 1$



13.6 Timing Charts

When using the I²C bus mode, the master device outputs an address via the serial bus to select one of several slave devices as its communication partner.

After outputting the slave address, the master device transmits the TRC0 bit (bit 3 of the IICA status register 0 (IICS0)), which specifies the data transfer direction, and then starts serial communication with the slave device.

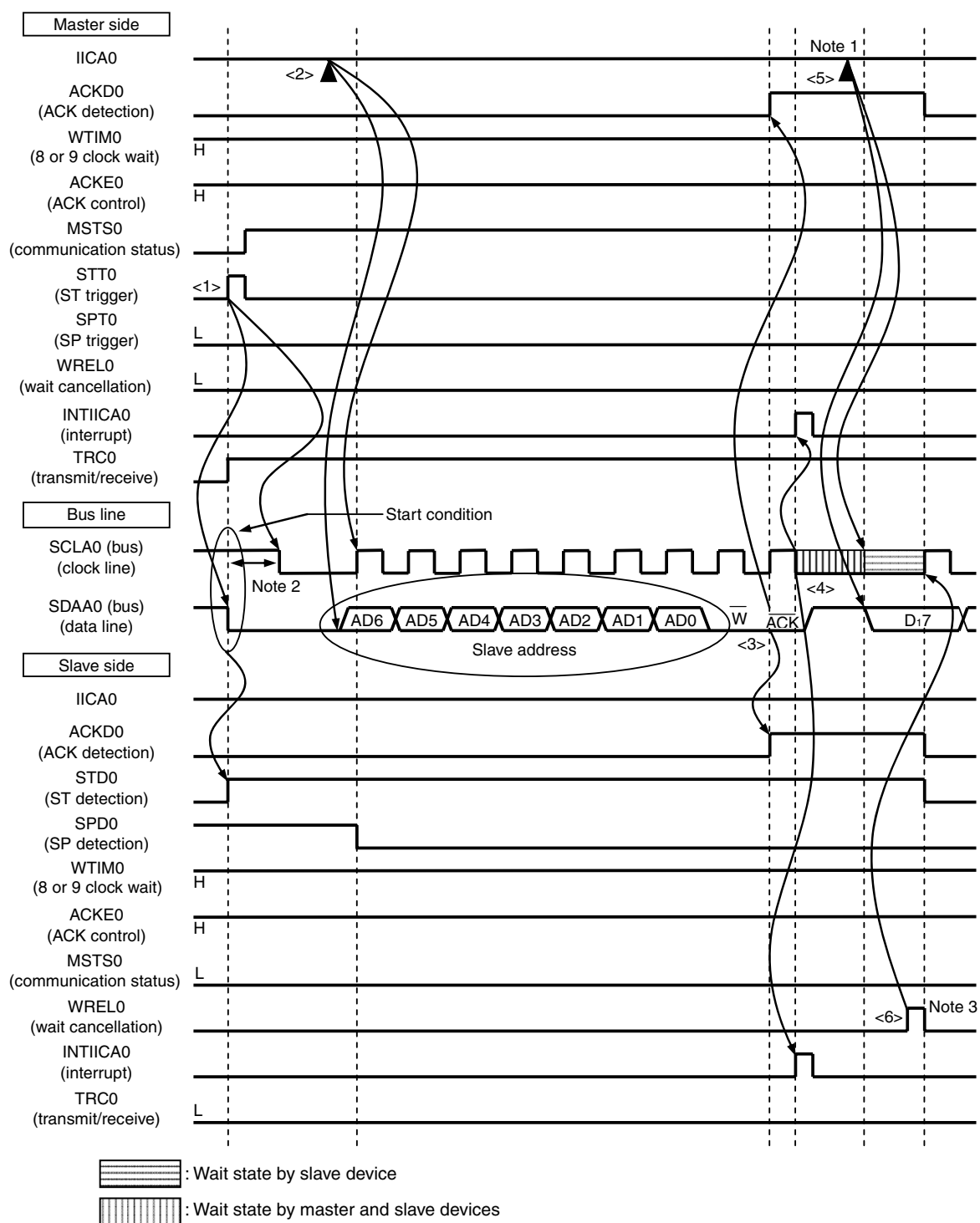
Figures 13-32 and 13-33 show timing charts of the data communication.

The IICA shift register 0 (IICA0)'s shift operation is synchronized with the falling edge of the serial clock (SCLA0). The transmit data is transferred to the SO latch and is output (MSB first) via the SDAA0 pin.

Data input via the SDAA0 pin is captured into IICA0 at the rising edge of SCLA0.

Figure 13-32. Example of Master to Slave Communication
(9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/4)

(1) Start condition ~ address ~ data



- Notes**
1. Write data to IICA0, not setting the WREL0 bit, in order to cancel a wait state during transmission by a master device.
 2. Make sure that the time between the fall of the SDAA0 pin signal and the fall of the SCLA0 pin signal is at least 4.0 μ s when specifying standard mode and at least 0.6 μ s when specifying fast mode.
 3. For releasing wait state during reception of a slave device, write "FFH" to IICA0 or set the WREL0 bit.

The meanings of <1> to <6> in (1) Start condition ~ address ~ data in Figure 13-32 are explained below.

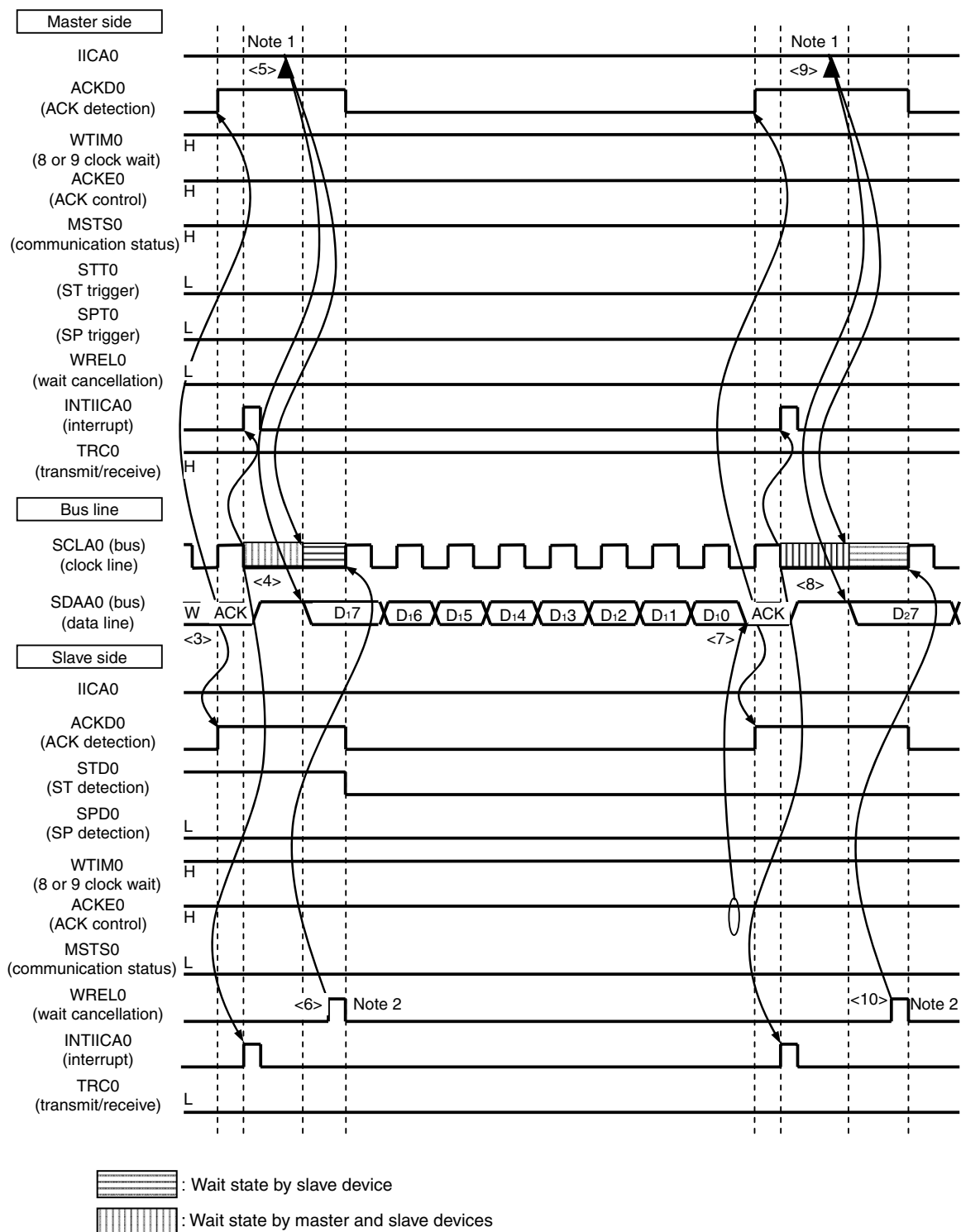
- <1> The start condition trigger is set by the master device (STT0 = 1) and a start condition (i.e. SCLA0 = 1 changes SDAA0 from 1 to 0) is generated once the bus data line goes low (SDAA0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS0 = 1). The master device is ready to communicate once the bus clock line goes low (SCLA0 = 0) after the hold time has elapsed.
- <2> The master device writes the address + W (transmission) to the IICA shift register 0 (IICA0) and transmits the slave address.
- <3> In the slave device if the address received matches the address (SVA0 value) of a slave device^{Note}, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)^{Note}.
- <5> The master device writes the data to transmit to the IICA0 register and releases the wait status that it set by the master device.
- <6> If the slave device releases the wait status (WREL0 = 1), the master device starts transferring data to the slave device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <15> in Figure 13-32 represent the entire procedure for communicating data using the I²C bus. Figure 13-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 13-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 13-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

Figure 13-32. Example of Master to Slave Communication
(9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/4)

(2) Address ~ data ~ data



Notes 1. Write data to IICA0, not setting the WREL0 bit, in order to cancel a wait state during transmission by a master device.

2. For releasing wait state during reception of a slave device, write "FFH" to IICA0 or set the WREL0 bit.

The meanings of <3> to <10> in (2) Address ~ data ~ data in Figure 13-32 are explained below.

- <3> In the slave device if the address received matches the address (SVA0 value) of a slave device^{Note}, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)^{Note}.
- <5> The master device writes the data to transmit to the IICA shift register 0 (IICA0) and releases the wait status that it set by the master device.
- <6> If the slave device releases the wait status (WREL0 = 1), the master device starts transferring data to the slave device.
- <7> After data transfer is completed, because of ACKE0 = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <8> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).
- <9> The master device writes the data to transmit to the IICA0 register and releases the wait status that it set by the master device.
- <10> The slave device reads the received data and releases the wait status (WREL0 = 1). The master device then starts transferring data to the slave device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <15> in Figure 13-32 represent the entire procedure for communicating data using the I²C bus. Figure 13-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 13-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 13-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

**Figure 13-32. Example of Master to Slave Communication
(9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/4)**

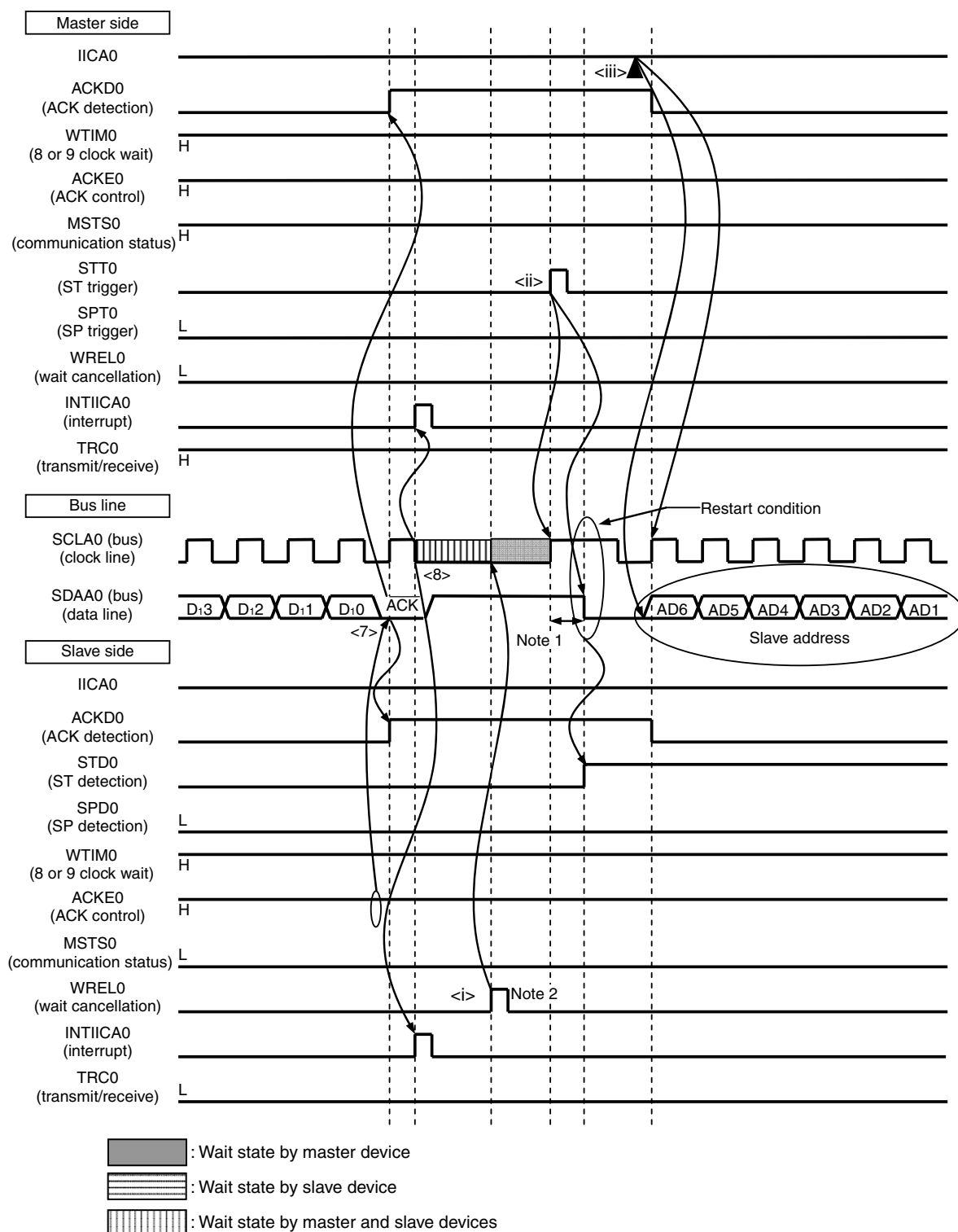
The meanings of <7> to <15> in (3) Data ~ data ~ stop condition in Figure 13-32 are explained below.

- <7> After data transfer is completed, because of ACKE0 = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <8> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).
- <9> The master device writes the data to transmit to the IICA shift register 0 (IICA0) and releases the wait status that it set by the master device.
- <10> The slave device reads the received data and releases the wait status (WREL0 = 1). The master device then starts transferring data to the slave device.
- <11> When data transfer is complete, the slave device (ACKE0 = 1) sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <12> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).
- <13> The slave device reads the received data and releases the wait status (WREL0 = 1).
- <14> By the master device setting a stop condition trigger (SPT0 = 1), the bus data line is cleared (SDAA0 = 0) and the bus clock line is set (SCLA0 = 1). After the stop condition setup time has elapsed, by setting the bus data line (SDAA0 = 1), the stop condition is then generated (i.e. SCLA0 = 1 changes SDAA0 from 0 to 1).
- <15> When a stop condition is generated, the slave device detects the stop condition and issues an interrupt (INTIICA0: stop condition).

Remark <1> to <15> in Figure 13-32 represent the entire procedure for communicating data using the I²C bus. Figure 13-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 13-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 13-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

Figure 13-32. Example of Master to Slave Communication
(9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (4/4)

(4) Data ~ restart condition ~ address



Notes 1. Make sure that the time between the rise of the SCLA0 pin signal and the generation of the start condition after a restart condition has been issued is at least 4.7 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

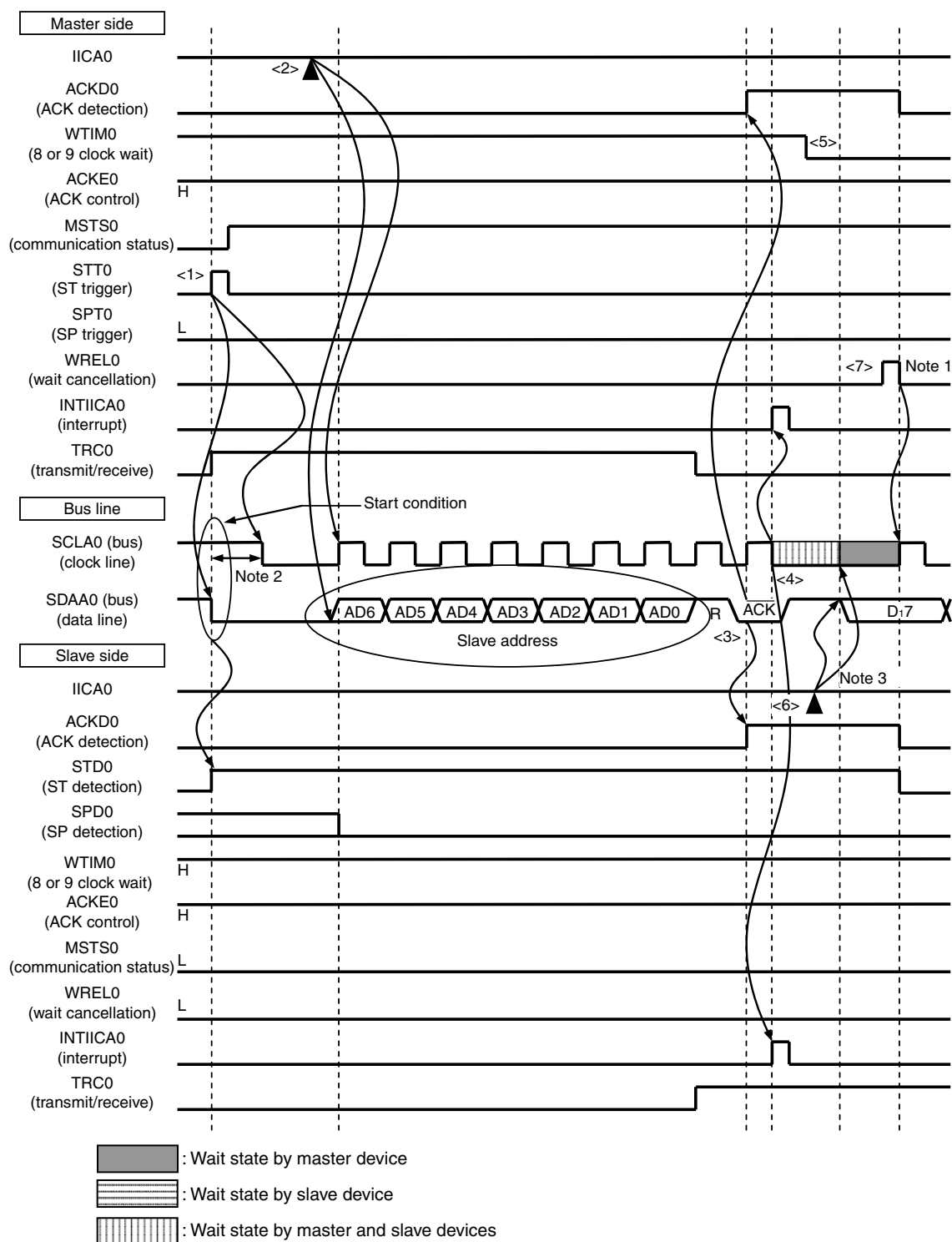
2. For releasing wait state during reception of a slave device, write "FFH" to IICA0 or set the WREL0 bit.

The following describes the operations in Figure 13-32 (4) Data ~ restart condition ~ address. After the operations in steps <7> and <8>, the operations in steps <i> to <iii> are performed. These steps return the processing to step <iii>, the data transmission step.

- <7> After data transfer is completed, because of $ACKEO = 1$, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device ($ACKD0 = 1$) at the rising edge of the 9th clock.
- <8> The master device and slave device set a wait status ($SCLA0 = 0$) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).
- <i> The slave device reads the received data and releases the wait status ($WREL0 = 1$).
- <ii> The start condition trigger is set again by the master device ($STT0 = 1$) and a start condition (i.e. $SCLA0 = 1$ changes $SDAA0$ from 1 to 0) is generated once the bus clock line goes high ($SCLA0 = 1$) and the bus data line goes low ($SDAA0 = 0$) after the restart condition setup time has elapsed. When the start condition is subsequently detected, the master device is ready to communicate once the bus clock line goes low ($SCLA0 = 0$) after the hold time has elapsed.
- <iii> The master device writing the address + R/W (transmission) to the IICA shift register (IICA0) enables the slave address to be transmitted.

Figure 13-33. Example of Slave to Master Communication
(8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)

(1) Start condition ~ address ~ data



- Notes**
- For releasing wait state during reception of a master device, write "FFH" to IICA0 or set the WRELO bit.
 - Make sure that the time between the fall of the SDAA0 pin signal and the fall of the SCLA0 pin signal is at least $4.0 \mu\text{s}$ when specifying standard mode and at least $0.6 \mu\text{s}$ when specifying fast mode.
 - Write data to IICA0, not setting the WRELO bit, in order to cancel a wait state during transmission by a slave device.

The meanings of <1> to <7> in (1) Start condition ~ address ~ data in Figure 13-33 are explained below.

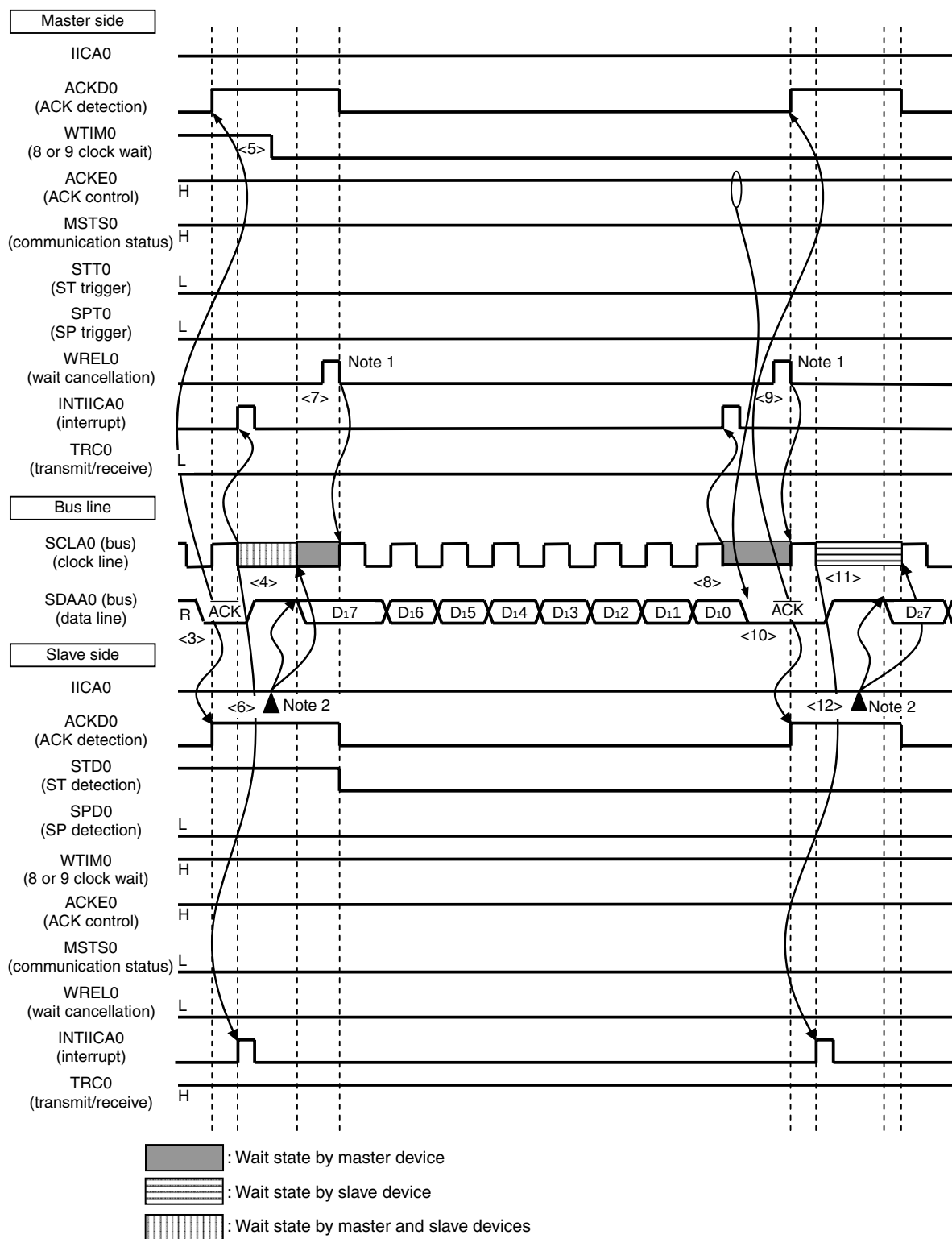
- <1> The start condition trigger is set by the master device (STT0 = 1) and a start condition (i.e. SCLA0 = 1 changes SDAA0 from 1 to 0) is generated once the bus data line goes low (SDAA0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS0 = 1). The master device is ready to communicate once the bus clock line goes low (SCLA0 = 0) after the hold time has elapsed.
- <2> The master device writes the address + R (reception) to the IICA shift register 0 (IICA0) and transmits the slave address.
- <3> In the slave device if the address received matches the address (SVA0 value) of a slave device^{Note}, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)^{Note}.
- <5> The timing at which the master device sets the wait status changes to the 8th clock (WTIM0 = 0).
- <6> The slave device writes the data to transmit to the IICA0 register and releases the wait status that it set by the slave device.
- <7> The master device releases the wait status (WREL0 = 1) and starts transferring data from the slave device to the master device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <19> in Figure 13-33 represent the entire procedure for communicating data using the I²C bus. Figure 13-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 13-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 13-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

Figure 13-33. Example of Slave to Master Communication
(8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/3)

(2) Address ~ data ~ data



- Notes**
- For releasing wait state during reception of a master device, write "FFH" to IICA0 or set the WREL0 bit.
 - Write data to IICA0, not setting the WREL0 bit, in order to cancel a wait state during transmission by a slave device.

The meanings of <3> to <12> in (2) Address ~ data ~ data in Figure 13-33 are explained below.

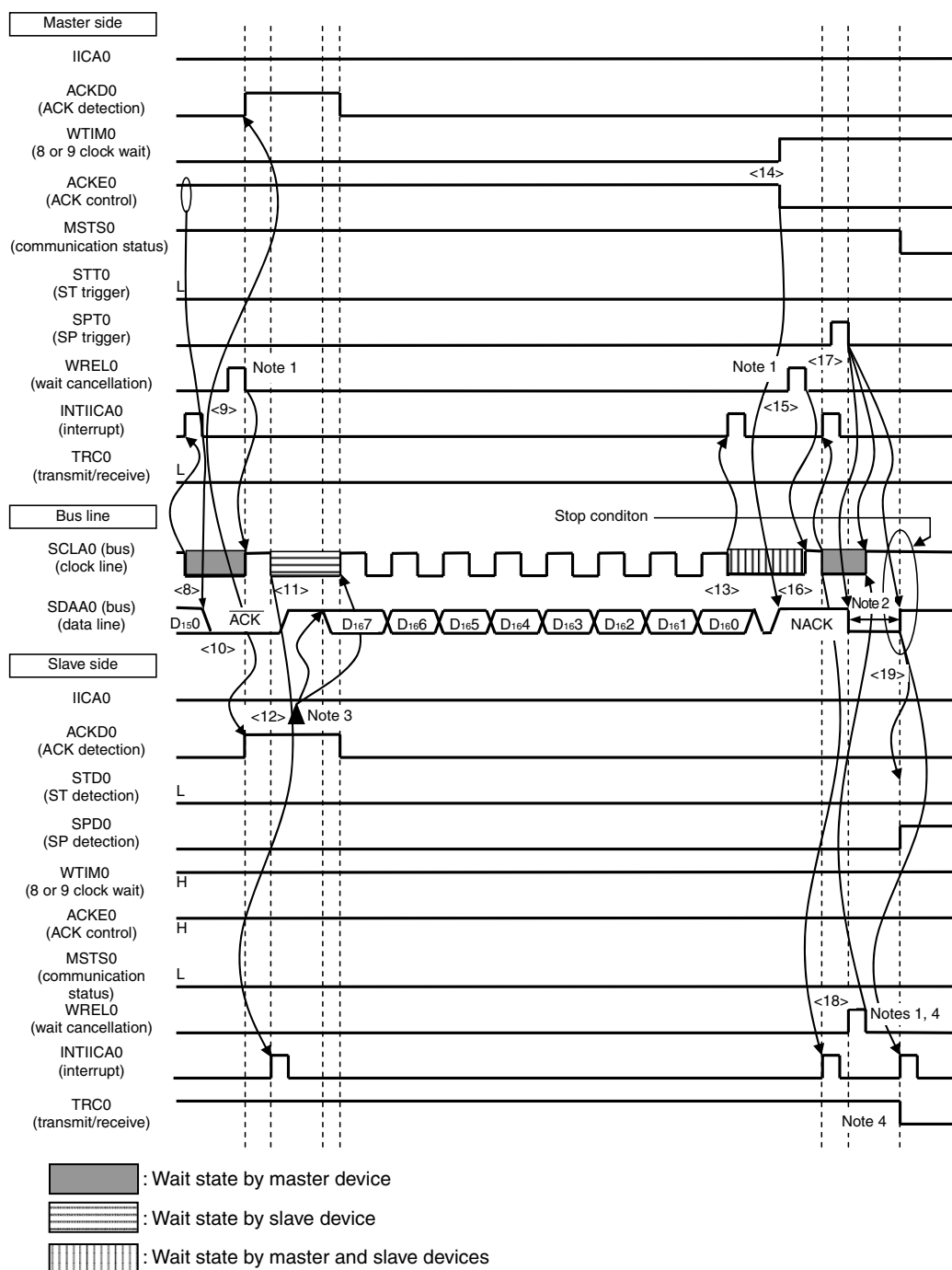
- <3> In the slave device if the address received matches the address (SVA0 value) of a slave device^{Note}, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)^{Note}.
- <5> The master device changes the timing of the wait status to the 8th clock (WTIM0 = 0).
- <6> The slave device writes the data to transmit to the IICA shift register 0 (IICA0) and releases the wait status that it set by the slave device.
- <7> The master device releases the wait status (WREL0 = 1) and starts transferring data from the slave device to the master device.
- <8> The master device sets a wait status (SCLA0 = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICA0: end of transfer). Because of ACKE0 = 1 in the master device, the master device then sends an ACK by hardware to the slave device.
- <9> The master device reads the received data and releases the wait status (WREL0 = 1).
- <10> The ACK is detected by the slave device (ACKD0 = 1) at the rising edge of the 9th clock.
- <11> The slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and the slave device issue an interrupt (INTIICA0: end of transfer).
- <12> By the slave device writing the data to transmit to the IICA0 register, the wait status set by the slave device is released. The slave device then starts transferring data to the master device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <19> in Figure 13-33 represent the entire procedure for communicating data using the I²C bus. Figure 13-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 13-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 13-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

Figure 13-33. Example of Slave to Master Communication
(8-Clock and 9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/3)

(3) Data ~ data ~ stop condition



The meanings of <8> to <19> in (3) Data ~ data ~ stop condition in Figure 13-33 are explained below.

- <8> The master device sets a wait status (SCLA0 = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICA0: end of transfer). Because of ACKE0 = 0 in the master device, the master device then sends an ACK by hardware to the slave device.
- <9> The master device reads the received data and releases the wait status (WREL0 = 1).
- <10> The ACK is detected by the slave device (ACKD0 = 1) at the rising edge of the 9th clock.
- <11> The slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and the slave device issue an interrupt (INTIICA0: end of transfer).
- <12> By the slave device writing the data to transmit to the IICA register, the wait status set by the slave device is released. The slave device then starts transferring data to the master device.
- <13> The master device issues an interrupt (INTIICA0: end of transfer) at the falling edge of the 8th clock, and sets a wait status (SCLA0 = 0). Because ACK control (ACKE0 = 1) is performed, the bus data line is at the low level (SDAA0 = 0) at this stage.
- <14> The master device sets NACK as the response (ACKE0 = 0) and changes the timing at which it sets the wait status to the 9th clock (WTIM0 = 1).
- <15> If the master device releases the wait status (WREL0 = 1), the slave device detects the NACK (ACK = 0) at the rising edge of the 9th clock.
- <16> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).
- <17> When the master device issues a stop condition (SPT0 = 1), the bus data line is cleared (SDAA0 = 0) and the master device releases the wait status. The master device then waits until the bus clock line is set (SCLA0 = 1).
- <18> The slave device acknowledges the NACK, halts transmission, and releases the wait status (WREL0 = 1) to end communication. Once the slave device releases the wait status, the bus clock line is set (SCLA0 = 1).
- <19> Once the master device recognizes that the bus clock line is set (SCLA0 = 1) and after the stop condition setup time has elapsed, the master device sets the bus data line (SDAA0 = 1) and issues a stop condition (i.e. SCLA0 =1 changes SDAA0 from 0 to 1). The slave device detects the generated stop condition and slave device issue an interrupt (INTIICA0: stop condition).

Remark <1> to <19> in Figure 13-33 represent the entire procedure for communicating data using the I²C bus. Figure 13-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 13-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 13-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

CHAPTER 14 MULTIPLIER AND DIVIDER/MULTIPLY-ACCUMULATOR

14.1 Functions of Multiplier and Divider/Multiply-Accumulator

The multiplier and divider/multiply-accumulator has the following functions.

- $16 \text{ bits} \times 16 \text{ bits} = 32 \text{ bits}$ (Unsigned)
- $16 \text{ bits} \times 16 \text{ bits} = 32 \text{ bits}$ (Signed)
- $16 \text{ bits} \times 16 \text{ bits} + 32 \text{ bits} = 32 \text{ bits}$ (Unsigned)
- $16 \text{ bits} \times 16 \text{ bits} + 32 \text{ bits} = 32 \text{ bits}$ (Signed)
- $32 \text{ bits} \div 32 \text{ bits} = 32 \text{ bits}$, 32-bits remainder (Unsigned)

14.2 Configuration of Multiplier and Divider/Multiply-Accumulator

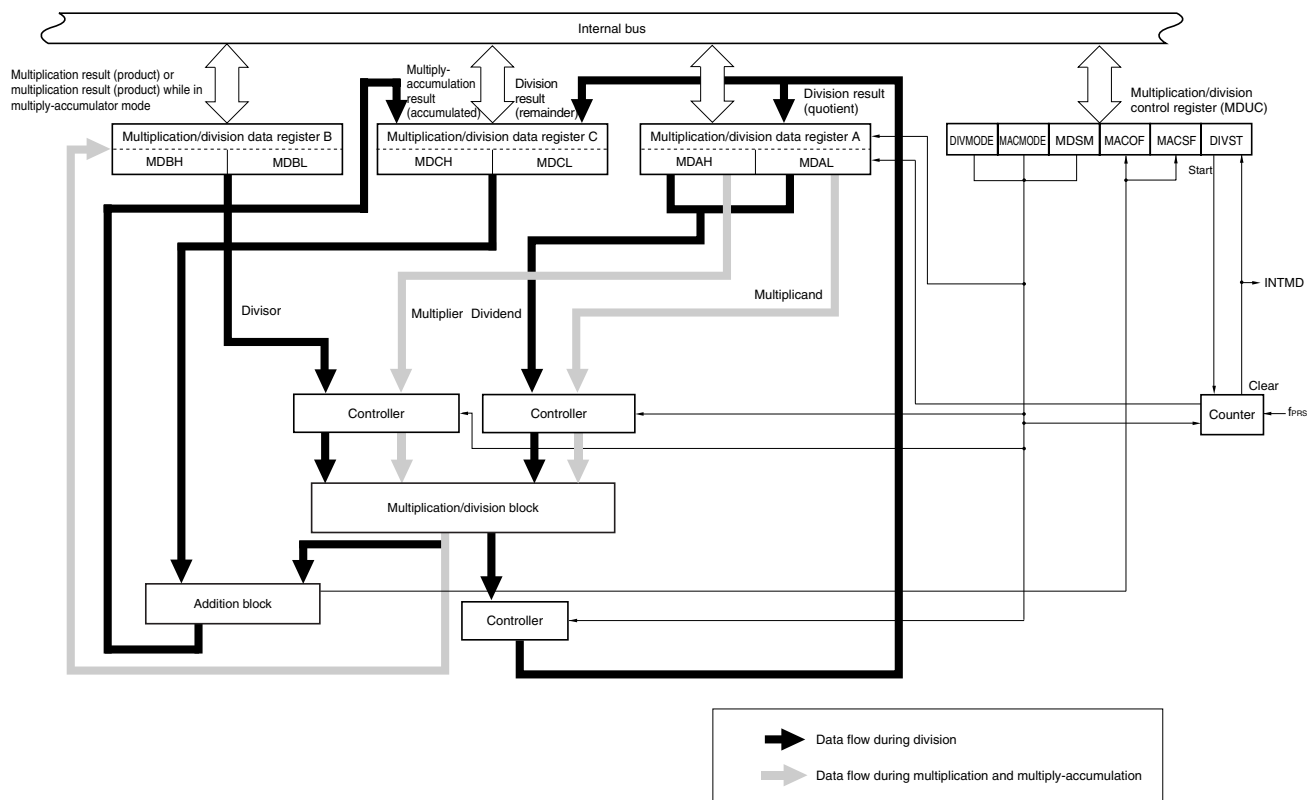
The multiplier and divider/multiply-accumulator consists of the following hardware.

Table 14-1. Configuration of Multiplier and Divider/Multiply-Accumulator

Item	Configuration
Registers	Multiplication/division data register A (L) (MDAL) Multiplication/division data register A (H) (MDAH) Multiplication/division data register B (L) (MDBL) Multiplication/division data register B (H) (MDBH) Multiplication/division data register C (L) (MDCL) Multiplication/division data register C (H) (MDCH)
Control register	Multiplication/division control register (MDUC)

Figure 14-1 shows a block diagram of the multiplier and divider/multiply-accumulator.

<R>

Figure 14-1. Block Diagram of Multiplier and Divider/Multiply-Accumulator

14.2.1 Multiplication/division data register A (MDAH, MDAL)

The MDAH and MDAL registers set the values that are used for a multiplication or division operation and store the operation result. They set the multiplier and multiplicand data in the multiplication mode or multiply-accumulator mode, and set the dividend data in the division mode. Furthermore, the operation result (quotient) is stored in the MDAH and MDAL registers in the division mode.

The MDAH and MDAL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 14-2. Format of Multiplication/Division Data Register A (MDAH, MDAL)

Address: FFFF0H, FFFF1H, FFFF2H, FFFF3H After reset: 0000H, 0000H R/W



- Cautions**
1. Do not rewrite the MDAH and MDAL registers values during division operation processing (when the multiplication/division control register (MDUC) value is 81H or C1H). The operation will be executed in this case, but the operation result will be an undefined value.
 2. The MDAH and MDAL registers values read during division operation processing (when the MDUC register value is 81H or C1H) will not be guaranteed.
 3. The data is in the two's complement format in either the multiplication mode (signed) or multiply-accumulator mode (signed).

The following table shows the functions of the MDAH and MDAL registers during operation execution.

Table 14-2. Functions of MDAH and MDAL Registers During Operation Execution

Operation Mode	Setting	Operation Result
Multiplication mode (unsigned) Multiply-accumulator mode (unsigned)	MDAH: Multiplier (unsigned) MDAL: Multiplicand (unsigned)	—
Multiplication mode (signed) Multiply-accumulator mode (signed)	MDAH: Multiplier (signed) MDAL: Multiplicand (signed)	—
Division mode (unsigned)	MDAH: Dividend (unsigned) (higher 16 bits) MDAL: Dividend (unsigned) (lower 16 bits)	MDAH: Division result (quotient) (unsigned) Higher 16 bits MDAL: Division result (quotient) (unsigned) Lower 16 bits

14.2.2 Multiplication/division data register B (MDBL, MDBH)

The MDBH and MDBL registers set the values that are used for multiplication or division operation and store the operation result. They store the operation result (product) in the multiplication mode and multiply-accumulator mode, and set the divisor data in the division mode.

The MDBH and MDBL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 14-3. Format of Multiplication/Division Data Register B (MDBH, MDBL)

Address: FFFF4H, FFFF5H, FFFF6H, FFFF7H After reset: 0000H, 0000H R/W



- Cautions**
1. Do not rewrite the MDBH and MDBL registers values during division operation processing (when the multiplication/division control register (MDUC) value is 81H or C1H) or multiply-accumulation operation processing. The operation result will be an undefined value.
 2. Do not set the MDBH and MDBL registers to 0000H in the division mode. If they are set, the operation result will be an undefined value.
 3. The data is in the two's complement format in either the multiplication mode (signed) or multiply-accumulator mode (signed).

The following table shows the functions of the MDBH and MDBL registers during operation execution.

Table 14-3. Functions of MDBH and MDBL Registers During Operation Execution

Operation Mode	Setting	Operation Result
Multiplication mode (unsigned) Multiply-accumulator mode (unsigned)	—	MDBH: Multiplication result (product) (unsigned) Higher 16 bits MDBL: Multiplication result (product) (unsigned) Lower 16 bits
Multiplication mode (signed) Multiply-accumulator mode (signed)	—	MDBH: Multiplication result (product) (signed) Higher 16 bits MDBL: Multiplication result (product) (signed) Lower 16 bits
Division mode (unsigned)	MDBH: Divisor (unsigned) (higher 16 bits) MDBL: Divisor (unsigned) (lower 16 bits)	—

14.2.3 Multiplication/division data register C (MDCL, MDCH)

The MDCH and MDCL registers are used to store the accumulated result while in the multiply-accumulator mode or the remainder of the operation result while in the division mode. These registers are not used while in the multiplication mode.

The MDCH and MDCL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 14-4. Format of Multiplication/Division Data Register C (MDCH, MDCL)

Address: F00E0H, F00E1H, F00E2H, F00E3H After reset: 0000H, 0000H R/W

The diagram illustrates the bit fields for the MDCH and MDCL registers. The MDCH register (bits 15-0) is divided into two 8-bit fields: F00E3H (bits 15-8) and F00E2H (bits 7-0). The MDCL register (bits 15-0) is divided into two 8-bit fields: F00E1H (bits 15-8) and F00E0H (bits 7-0).

Cautions

1. The MDCH and MDCL registers values read during division operation processing (when the multiplication/division control register (MDUC) value is 81H or C1H) will not be guaranteed.
2. During multiply-accumulator processing, do not use software to rewrite the values of the MDCH and MDCL registers. If this is done, the operation result will be undefined.
3. The data is in the two's complement format in the multiply-accumulator mode (signed).

Table 14-4. Functions of MDCH and MDCL Registers During Operation Execution

Operation Mode	Setting	Operation Result
Multiplication mode (unsigned or signed)	–	–
Multiply-accumulator mode (unsigned)	MDCH: Initial accumulated value (unsigned) (higher 16 bits) MDCL: Initial accumulated value (unsigned) (lower 16 bits)	MDCH: accumulated value (unsigned) (higher 16 bits) MDCL: accumulated value (unsigned) (lower 16 bits)
Multiply-accumulator mode (signed)	MDCH: Initial accumulated value (signed) (higher 16 bits) MDCL: Initial accumulated value (signed) (lower 16 bits)	MDCH: accumulated value (signed) (higher 16 bits) MDCL: accumulated value (signed) (lower 16 bits)
Division mode (unsigned)	–	MDCH: Remainder (unsigned) (higher 16 bits) MDCL: Remainder (unsigned) (lower 16 bits)

The register configuration differs between when multiplication is executed and when division is executed, as follows.

- Register configuration during multiplication

$$\begin{array}{ccc} \text{<Multiplier A>} & \text{<Multiplier B>} & \text{<Product>} \\ \text{MDAL (bits 15 to 0)} \times \text{MDAH (bits 15 to 0)} & = & [\text{MDBH (bits 15 to 0)}, \text{MDBL (bits 15 to 0)}] \end{array}$$

- Register configuration during multiply-accumulation

$$\begin{array}{cccc} \text{<Multiplier A>} & \text{<Multiplier B>} & \text{< accumulated value >} & \text{< accumulated result >} \\ \text{MDAL (bits 15 to 0)} \times \text{MDAH (bits 15 to 0)} + \text{MDC (bits 31 to 0)} & = & [\text{MDCH (bits 15 to 0)}, \text{MDCL (bits 15 to 0)}] \end{array}$$
 (The multiplication result is stored in the MDBH (bits 15 to 0) and MDBL (bits 15 to 0).)

- Register configuration during division

$$\begin{array}{ccc} \text{<Dividend>} & & \text{<Divisor>} \\ [\text{MDAH (bits 15 to 0)}, \text{MDAL (bits 15 to 0)}] \div [\text{MDBH (bits 15 to 0)}, \text{MDBL (bits 15 to 0)}] & = & \\ \text{<Quotient>} & & \text{<Remainder>} \\ [\text{MDAH (bits 15 to 0)}, \text{MDAL (bits 15 to 0)}] \dots [\text{MDCH (bits 15 to 0)}, \text{MDCL (bits 15 to 0)}] \end{array}$$

14.3 Register Controlling Multiplier and Divider/Multiply-Accumulator

The multiplier and divider/multiply-accumulator is controlled by using the multiplication/division control register (MDUC).

14.3.1 Multiplication/division control register (MDUC)

The MDUC register is an 8-bit register that controls the operation of the multiplier and divider/multiply-accumulator.

The MDUC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 14-5. Format of Multiplication/Division Control Register (MDUC)

Address: F00E8H After reset: 00H R/W

Symbol	<7>	<6>	5	4	<3>	<2>	<1>	<0>
MDUC	DIVMODE	MACMODE	0	0	MDSM	MACOF	MACSF	DIVST

DIVMODE	MACMODE	MDSM	Operation mode selection
0	0	0	Multiplication mode (unsigned) (default)
0	0	1	Multiplication mode (signed)
0	1	0	Multiply-accumulator mode (unsigned)
0	1	1	Multiply-accumulator mode (signed)
1	0	0	Division mode (unsigned), generation generation of a division completion interrupt (INTMD)
1	1	0	Division mode (unsigned), not generation of a division completion interrupt (INTMD)
Other than above			Setting prohibited

MACOF	Overflow flag of multiply-accumulation result (accumulated value)
0	No overflow
1	With over flow
<Set condition> - For the multiply-accumulator mode (unsigned) The bit is set when the accumulated value goes outside the range from 00000000h to FFFFFFFFh. - For the multiply-accumulator mode (signed) The bit is set when the result of adding a positive product to a positive accumulated value exceeds 7FFFFFFFh and is negative, or when the result of adding a negative product to a negative accumulated value exceeds 80000000h and is positive.	

MACSF	Sign flag of multiply-accumulation result (accumulated value)
0	The accumulated value is positive.
1	The accumulated value is negative.
Multiply-accumulator mode (unsigned): The bit is always 0. Multiply-accumulator mode (signed): The bit indicates the sign bit of the accumulated value.	

DIVST ^{Note}	Division operation start/stop
0	Division operation processing complete
1	Starts division operation/division operation processing in progress

(Note and Cautions are listed on the next page.)

Note The DIVST bit can only be set (1) in the division mode. In the division mode, division operation is started by setting (1) the DIVST bit. The DIVST bit is automatically cleared (0) when the operation ends. In the multiplication mode, operation is automatically started by setting the multiplier and multiplicand to multiplication/division data register A (MDAH, MDAL), respectively.

Cautions

1. Do not rewrite the DIVMODE, MDSM bits during operation processing (while the DIVST bit is 1). If it is rewritten, the operation result will be an undefined value.
2. The DIVST bit cannot be cleared (0) by using software during division operation processing (while the DIVST bit is 1).

14.4 Operations of Multiplier and Divider/Multiply-Accumulator

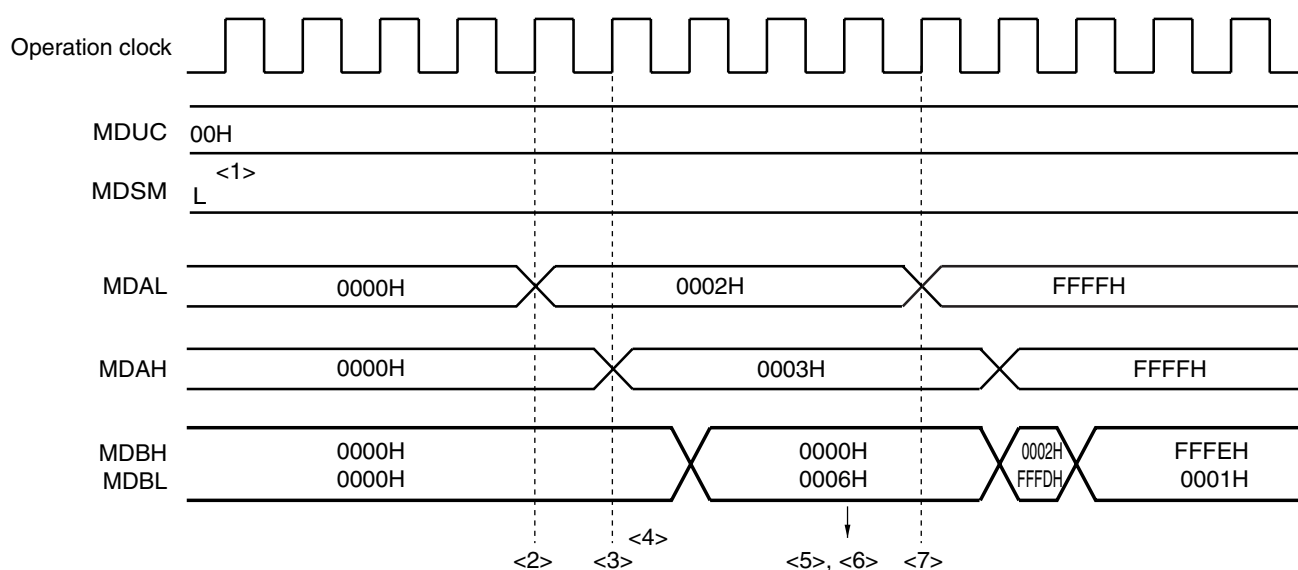
14.4.1 Multiplication (unsigned) operation

- Initial setting
 - <1> Set the multiplication/division control register (MDUC) to 00H.
 - <2> Set the multiplicand to multiplication/division data register A (L) (MDAL).
 - <3> Set the multiplier to multiplication/division data register A (H) (MDAH).
(There is no preference in the order of executing steps <2> and <3>. Multiplication operation is automatically started when the multiplier and multiplicand are set to the MDAH and MDAL registers, respectively.)
- During operation processing
 - <4> Wait for at least one clock. The operation will end when one clock has been issued.
- Operation end
 - <5> Read the product (lower 16 bits) from multiplication/division data register B (L) (MDBL).
 - <6> Read the product (higher 16 bits) from multiplication/division data register B (H) (MDBH).
(There is no preference in the order of executing steps <5> and <6>.)
- Next operation

<R> <7> The next time multiplication, division, or multiply-accumulation is performed, start with the initial settings of each step.

Remark Steps <1> to <7> correspond to <1> to <7> in Figure 14-6.

<R> **Figure 14-6. Timing Diagram of Multiplication (Unsigned) Operation ($2 \times 3 = 6$)**



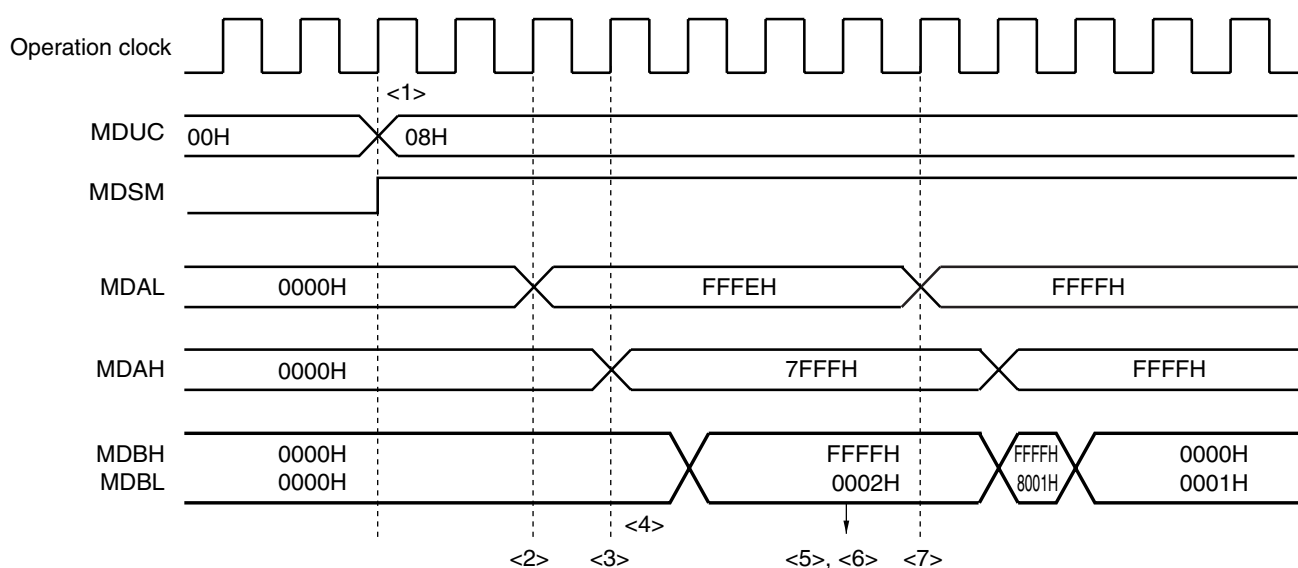
14.4.2 Multiplication (signed) operation

- Initial setting
 - <1> Set the multiplication/division control register (MDUC) to 08H.
 - <2> Set the multiplicand to multiplication/division data register A (L) (MDAL).
 - <3> Set the multiplier to multiplication/division data register A (H) (MDAH).
 - (There is no preference in the order of executing steps <2> and <3>. Multiplication operation is automatically started when the multiplier and multiplicand are set to the MDAH and MDAL registers, respectively.)
- During operation processing
 - <4> Wait for at least one clock. The operation will end when one clock has been issued.
- Operation end
 - <5> Read the product (lower 16 bits) from multiplication/division data register B (L) (MDBL).
 - <6> Read the product (higher 16 bits) from multiplication/division data register B (H) (MDBH).
 - (There is no preference in the order of executing steps <5> and <6>.)
- Next operation
 - <7> The next time multiplication, division, or multiply-accumulation is performed, start with the initial settings of each step.

Caution The data is in the two's complement format in multiplication mode (signed).

Remark Steps <1> to <7> correspond to <1> to <7> in Figure 14-7.

<R> **Figure 14-7. Timing Diagram of Multiplication (Signed) Operation ($-2 \times 32767 = -65534$)**



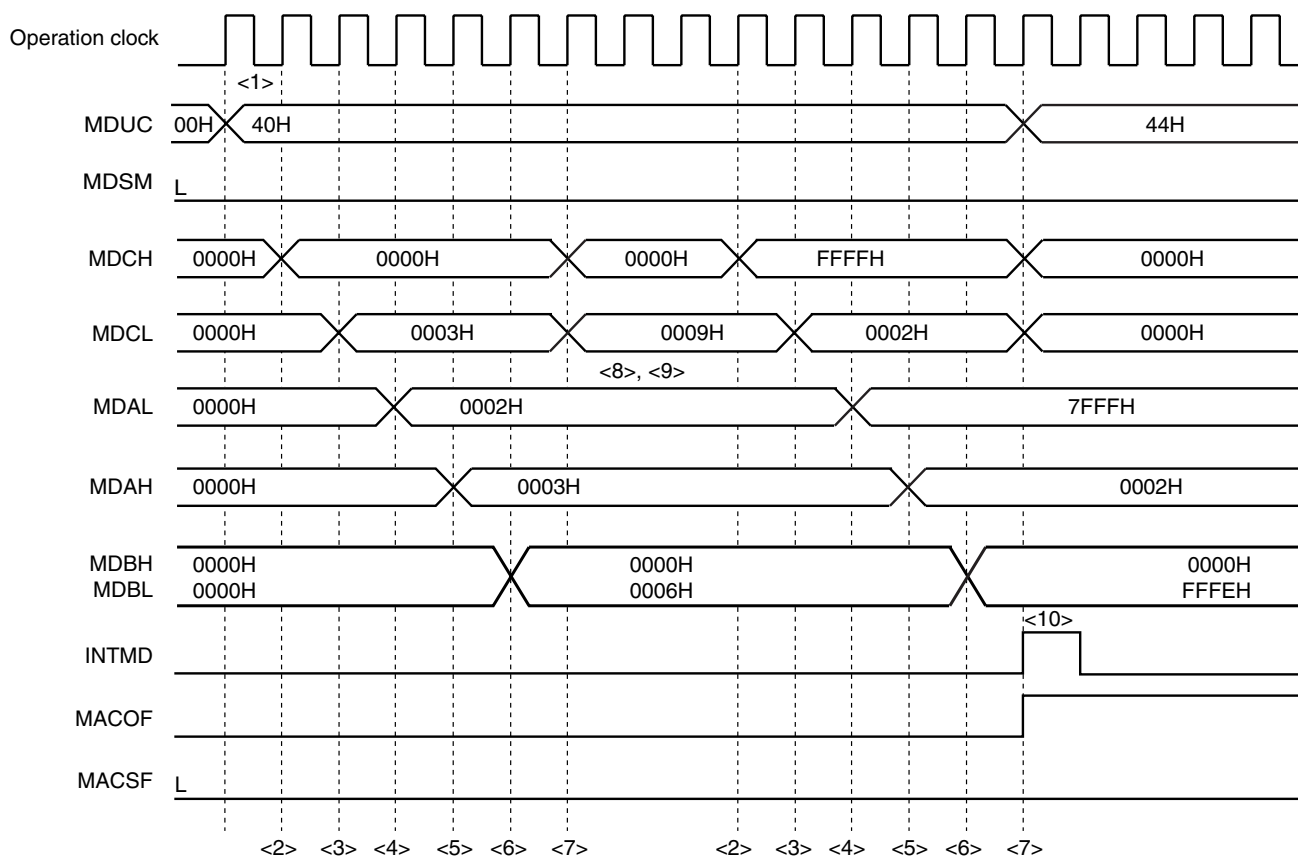
14.4.3 Multiply-accumulation (unsigned) operation

- Initial setting
 - <1> Set the multiplication/division control register (MDUC) to 40H.
 - <2> Set the initial accumulated value of higher 16 bits to multiplication/division data register C (L) (MDCL).
 - <3> Set the initial accumulated value of lower 16 bits to multiplication/division data register C (H) (MDCH).
 - <4> Set the multiplicand to multiplication/division data register A (L) (MDAL).
 - <5> Set the multiplier to multiplication/division data register A (H) (MDAH).
(There is no preference in the order of executing steps <2>, <3>, and <4>. Multiplication operation is automatically started when the multiplier is set to the MDAH register, respectively.)
 - During operation processing
 - <6> The multiplication operation finishes in one clock cycle.
(The multiplication result is stored in multiplication/division data register B (L) (MDBL) and multiplication/division data register B (H) (MDBH).)
 - <7> After <6>, the multiply-accumulation operation finishes in one additional clock cycle. (There is a wait of at least two clock cycles after specifying the initial settings is finished (<5>).)
 - Operation end
 - <8> Read the accumulated value (lower 16 bits) from the MDCL register.
 - <9> Read the accumulated value (higher 16 bits) from the MDCH register.
(There is no preference in the order of executing steps <8> and <9>.)
 - (<10> If the result of the multiply-accumulation operation causes an overflow, the MACOF bit is set to 1, INTMD signal is occurred.)
 - Next operation
 - <11> The next time multiplication, division, or multiply-accumulation is performed, start with the initial settings of each step.
- <R>

Remark Steps <1> to <10> correspond to <1> to <10> in Figure 14-8.

<R>

Figure 14-8. Timing Diagram of Multiply-Accumulation (Unsigned) Operation
 $(2 \times 3 + 3 = 9 \rightarrow 32767 \times 2 + 4294901762 = 0 \text{ (over flow generated)})$



14.4.4 Multiply-accumulation (signed) operation

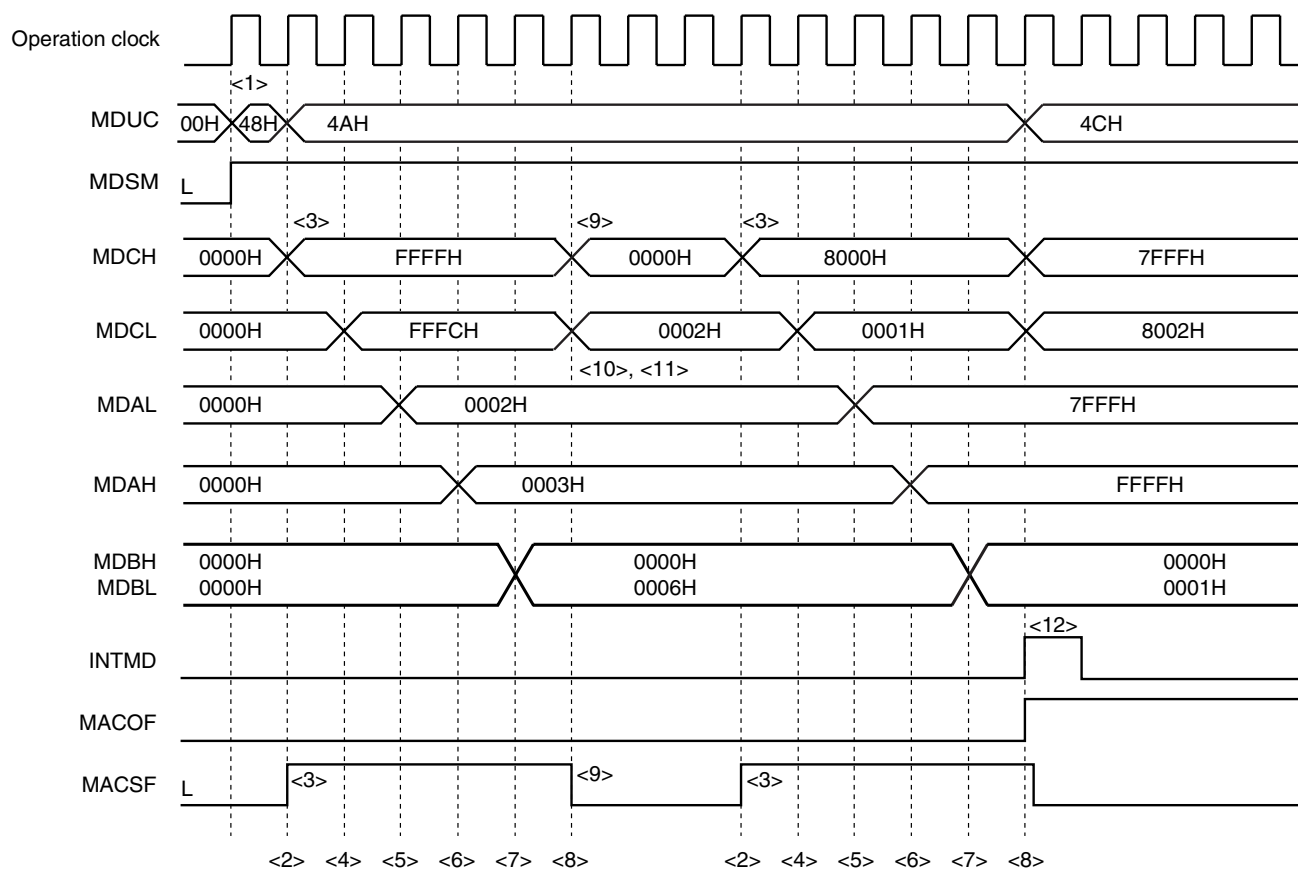
- Initial setting
 - <1> Set the multiplication/division control register (MDUC) to 48H.
 - <2> Set the initial accumulated value of higher 16 bits to multiplication/division data register C (H) (MDCH).
(<3> If the accumulated value in the MDCH register is negative, the MACSF bit is set to 1.)
 - <4> Set the initial accumulated value of lower 16 bits to multiplication/division data register C (L) (MDCL).
 - <5> Set the multiplicand to multiplication/division data register A (L) (MDAL).
 - <6> Set the multiplier to multiplication/division data register A (H) (MDAH).
(There is no preference in the order of executing steps <2>, <4>, and <5>. Multiplication operation is automatically started when the multiplier is set to the MDAH register, respectively.)
- During operation processing
 - <7> The multiplication operation finishes in one clock cycle.
(The multiplication result is stored in multiplication/division data register B (L) (MDBL) and multiplication/division data register B (H) (MDBH).)
 - <8> After <7>, the multiply-accumulation operation finishes in one additional clock cycle. (There is a wait of at least two clock cycles after specifying the initial settings is finished (<6>).)
- Operation end
 - <9> If the accumulated value stored in the MDCL and MDCH registers is positive, the MACSF bit is cleared to 0.
 - <10> Read the accumulated value (lower 16 bits) from the MDCL register.
 - <11> Read the accumulated value (higher 16 bits) from the MDCH register.
(There is no preference in the order of executing steps <10> and <11>.)
 - (<12> If the result of the multiply-accumulation operation causes an overflow, the MACOF bit is set to 1, INTMD signal is occurred.)
- Next operation
 - <R> <13> The next time multiplication, division, or multiply-accumulation is performed, start with the initial settings of each step.

Caution The data is in the two's complement format in multiply-accumulation (signed) operation.

Remark Steps <1> to <12> correspond to <1> to <12> in Figure 14-9.

<R>

Figure 14-9. Timing Diagram of Multiply-Accumulation (signed) Operation
 $(2 \times 3 + (-4) = 2 \rightarrow 32767 \times (-1) + (-2147483647) = -2147450882 \text{ (overflow occurs.)})$



14.4.5 Division operation

- Initial setting
 - <1> Set the multiplication/division control register (MDUC) to 80H.
 - <2> Set the dividend (higher 16 bits) to multiplication/division data register A (H) (MDAH).
 - <3> Set the dividend (lower 16 bits) to multiplication/division data register A (L) (MDAL).
 - <4> Set the divisor (higher 16 bits) to multiplication/division data register B (H) (MDBH).
 - <5> Set the divisor (lower 16 bits) to multiplication/division data register B (L) (MDBL).
 - <6> Set bit 0 (DIVST) of the MDUC register to 1.

(There is no preference in the order of executing steps <2> to <5>.)
- During operation processing
 - <7> The operation will end when one of the following processing is completed.
 - A wait of at least 16 clocks (The operation will end when 16 clocks have been issued.)
 - A check whether the DIVST bit has been cleared

(The read values of the MDBL, MDBH, MDCL, and MDCH registers during operation processing are not guaranteed.)
- Operation end
 - <8> The DIVST bit is cleared and the operation ends. At this time, an interrupt request signal (INTMD) is generated if the operation was performed with MACMODE = 0.
 - <9> Read the quotient (lower 16 bits) from the MDAL register.
 - <10> Read the quotient (higher 16 bits) from the MDAH register.
 - <11> Read the remainder (lower 16 bits) from multiplication/division data register C (L) (MDCL).
 - <12> Read the remainder (higher 16 bits) from multiplication/division data register C (H) (MDCH).

(There is no preference in the order of executing steps <9> to <12>.)
- Next operation
 - <13> The next time multiplication, division, or multiply-accumulation is performed, start with the initial settings of each step.

Remark Steps <1> to <12> correspond to <1> to <12> in Figure 14-10.

CHAPTER 15 DMA CONTROLLER

The RL78/G1A has an internal DMA (Direct Memory Access) controller.

Data can be automatically transferred between the peripheral hardware supporting DMA, SFRs, and internal RAM without via CPU.

As a result, the normal internal operation of the CPU and data transfer can be executed in parallel with transfer between the SFR and internal RAM, and therefore, a large capacity of data can be processed. In addition, real-time control using communication, timer, and A/D can also be realized.

15.1 Functions of DMA Controller

- Number of DMA channels: 2 channels
- Transfer unit: 8 or 16 bits
- Maximum transfer unit: 1024 times
- Transfer type: 2-cycle transfer (One transfer is processed in 2 clocks and the CPU stops during that processing.)
- Transfer mode: Single-transfer mode
- Transfer request: Selectable from the following peripheral hardware interrupts
 - A/D converter
 - Serial interface
(CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, UART0 to UART2)
 - Timer (channel 0, 1, 2, or 3)
- Transfer target: Between SFR and internal RAM

Here are examples of functions using DMA.

- Successive transfer of serial interface
- Batch transfer of analog data
- Capturing A/D conversion result at fixed interval
- Capturing port value at fixed interval

15.2 Configuration of DMA Controller

The DMA controller includes the following hardware.

Table 15-1. Configuration of DMA Controller

Item	Configuration
Address registers	• DMA SFR address registers 0, 1 (DSA0, DSA1) • DMA RAM address registers 0, 1 (DRA0, DRA1)
Count register	• DMA byte count registers 0, 1 (DBC0, DBC1)
Control registers	• DMA mode control registers 0, 1 (DMC0, DMC1) • DMA operation control register 0, 1 (DRC0, DRC1)

15.2.1 DMA SFR address register n (DSAn)

This is an 8-bit register that is used to set an SFR address that is the transfer source or destination of DMA channel n. Set the lower 8 bits of the SFR addresses FFF00H to FFFFH.

This register is not automatically incremented but fixed to a specific value.

In the 16-bit transfer mode, the least significant bit is ignored and is treated as an even address.

The DSAn register can be read or written in 8-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 00H.

Figure 15-1. Format of DMA SFR Address Register n (DSAn)

Address: FFFB0H (DSA0), FFFB1H (DSA1) After reset: 00H R/W

	7	6	5	4	3	2	1	0
DSAn								

Remark n: DMA channel number (n = 0, 1)

15.2.2 DMA RAM address register n (DRAn)

This is a 16-bit register that is used to set a RAM address that is the transfer source or destination of DMA channel n.

Addresses of the internal RAM area other than the general-purpose registers (see table 15-2) can be set to this register.

Set the lower 16 bits of the RAM address.

This register is automatically incremented when DMA transfer has been started. It is incremented by +1 in the 8-bit transfer mode and by +2 in the 16-bit transfer mode. DMA transfer is started from the address set to this DRAn register. When the data of the last address has been transferred, the DRAn register stops with the value of the last address +1 in the 8-bit transfer mode, and the last address +2 in the 16-bit transfer mode.

In the 16-bit transfer mode, the least significant bit is ignored and is treated as an even address.

The DRAn register can be read or written in 8-bit or 16-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 0000H.

Figure 15-2. Format of DMA RAM Address Register n (DRAn)

Address: FFFB2H, FFFB3H (DRA0), FFFB4H, FFFB5H (DRA1) After reset: 0000H R/W

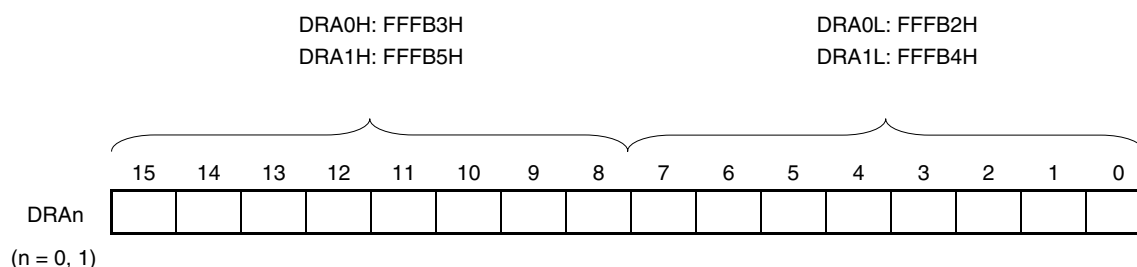


Table 15-2 Internal RAM Area other than the General-purpose Registers

Part Number	Internal RAM Area other than the General-purpose Registers
R5F10ExA (x = 8, B, G), R5F10ExC (x = 8, B, G, L)	FF700H to FFEDFH
R5F10ExD (x = 8, B, G, L)	FF300H to FFEDFH
R5F10ExE (x = 8, B, G, L)	FEF00H to FFEDFH

Remark n: DMA channel number (n = 0, 1)

15.2.3 DMA byte count register n (DBCn)

This is a 10-bit register that is used to set the number of times DMA channel n executes transfer. Be sure to set the number of times of transfer to this DBCn register before executing DMA transfer (up to 1024 times).

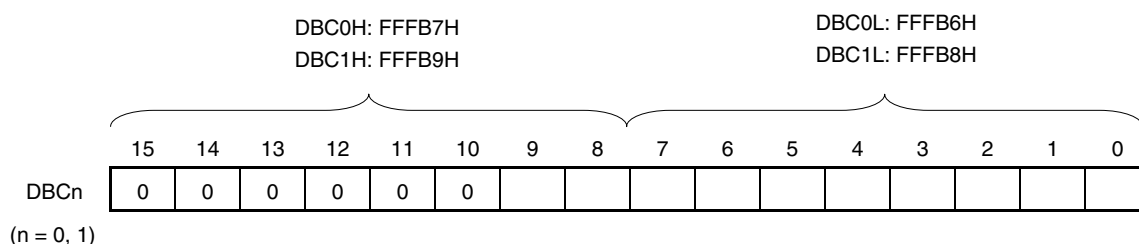
Each time DMA transfer has been executed, this register is automatically decremented. By reading this DBCn register during DMA transfer, the remaining number of times of transfer can be learned.

The DBCn register can be read or written in 8-bit or 16-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 0000H.

Figure 15-3. Format of DMA Byte Count Register n (DBCn)

Address: FFFB6H, FFFB7H (DBC0), FFFB8H, FFFB9H (DBC1) After reset: 0000H R/W



DBCn[9:0]	Number of Times of Transfer (When DBCn is Written)	Remaining Number of Times of Transfer (When DBCn is Read)
000H	1024	Completion of transfer or waiting for 1024 times of DMA transfer
001H	1	Waiting for remaining one time of DMA transfer
002H	2	Waiting for remaining two times of DMA transfer
003H	3	Waiting for remaining three times of DMA transfer
• • •	• • •	• • •
3FEH	1022	Waiting for remaining 1022 times of DMA transfer
3FFH	1023	Waiting for remaining 1023 times of DMA transfer

- Cautions**
1. Be sure to clear bits 15 to 10 to “0”.
 2. If the general-purpose register is specified or the internal RAM space is exceeded as a result of continuous transfer, the general-purpose register or SFR space are written or read, resulting in loss of data in these spaces. Be sure to set the number of times of transfer that is within the internal RAM space.

Remark n: DMA channel number (n = 0, 1)

15.3 Registers Controlling DMA Controller

DMA controller is controlled by the following registers.

- DMA mode control register n (DMCn)
- DMA operation control register n (DRCn)

Remark n: DMA channel number (n = 0, 1)

15.3.1 DMA mode control register n (DMCn)

The DMCn register is a register that is used to set a transfer mode of DMA channel n. It is used to select a transfer direction, data size, setting of pending, and start source. Bit 7 (STGn) is a software trigger that starts DMA.

Rewriting bits 6, 5, and 3 to 0 of the DMCn register is prohibited during operation (when DSTn = 1).

The DMCn register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 15-4. Format of DMA Mode Control Register n (DMCn) (1/2)

Address: FFFBAH (DMC0), FFFBBH (DMC1) After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
DMCn	STGn	DRSn	DSn	DWAITn	IFCn3	IFCn2	IFCn1	IFCn0

STGn ^{Note 1}	DMA transfer start software trigger
0	No trigger operation
1	DMA transfer is started when DMA operation is enabled (DENn = 1).

DMA transfer is performed once by writing 1 to the STGn bit when DMA operation is enabled (DENn = 1).
When this bit is read, 0 is always read.

DRSn	Selection of DMA transfer direction
0	SFR to internal RAM
1	Internal RAM to SFR

DSn	Specification of transfer data size for DMA transfer
0	8 bits
1	16 bits

DWAITn ^{Note 2}	Pending of DMA transfer
0	Executes DMA transfer upon DMA start request (not held pending).
1	Holds DMA start request pending if any.

DMA transfer that has been held pending can be started by clearing the value of the DWAITn bit to 0.
It takes 2 clocks to actually hold DMA transfer pending when the value of the DWAITn bit is set to 1.

Notes 1. The software trigger (STGn) can be used regardless of the IFCn0 to IFCn3 bits values.

2. When DMA transfer is held pending while using two or more DMA channels, be sure to hold the DMA transfer pending for all channels (by setting the DWAIT0 and DWAIT1 to 1).

Remark n: DMA channel number (n = 0, 1)

Figure 15-4. Format of DMA Mode Control Register n (DMCn) (2/2)

Address: FFFBAH (DMC0), FFFBBH (DMC1) After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
DMCn	STGn	DRSn	DSn	DWAITn	IFCn3	IFCn2	IFCn1	IFCn0

(When n = 0 or 1)

IFCn 3	IFCn 2	IFCn 1	IFCn 0	Selection of DMA start source ^{Note}	
				Trigger signal	Trigger contents
0	0	0	0	–	Disables DMA transfer by interrupt. (Only software trigger is enabled.)
0	0	0	1	INTAD	A/D conversion end interrupt
0	0	1	0	INTTM00	End of timer channel 0 count or capture end interrupt
0	0	1	1	INTTM01	End of timer channel 1 count or capture end interrupt
0	1	0	0	INTTM02	End of timer channel 2 count or capture end interrupt
0	1	0	1	INTTM03	End of timer channel 3 count or capture end interrupt
0	1	1	0	INTST0/INTCSI00	UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt
0	1	1	1	INTSR0/INTCSI01	UART0 reception transfer end interrupt/CSI01 transfer end or buffer empty interrupt
1	0	0	0	INTST1/INTCSI10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt
1	0	0	1	INTSR1/INTCSI11	UART1 reception transfer end interrupt/CSI11 transfer end or buffer empty interrupt
1	0	1	0	INTST2/INTCSI20	UART2 transmission transfer end or buffer empty interrupt/CSI20 transfer end or buffer empty interrupt
1	0	1	1	INTSR2/INTCSI21	UART2 reception transfer end interrupt/CSI21 transfer end or buffer empty interrupt
Other than above				Setting prohibited	

Note The software trigger (STGn) can be used regardless of the IFCn0 to IFCn3 bits values.

Remark n: DMA channel number (n = 0, 1)

15.3.2 DMA operation control register n (DRCn)

The DRCn register is a register that is used to enable or disable transfer of DMA channel n.

Rewriting bit 7 (DENn) of this register is prohibited during operation (when DSTn = 1).

The DRCn register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 15-5. Format of DMA Operation Control Register n (DRCn)

Address: FFFBCH (DRC0), FFFBDH (DRC1) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
DRCn	DENn	0	0	0	0	0	0	DSTn

DENn	DMA operation enable flag
0	Disables operation of DMA channel n (stops operating clock of DMA).
1	Enables operation of DMA channel n.
DMAC waits for a DMA trigger when DSTn = 1 after DMA operation is enabled (DENn = 1).	

DSTn	DMA transfer mode flag
0	DMA transfer of DMA channel n is completed.
1	DMA transfer of DMA channel n is not completed (still under execution).
DMAC waits for a DMA trigger when DSTn = 1 after DMA operation is enabled (DENn = 1). When a software trigger (STGn) or the start source trigger set by the IFCn3 to IFCn0 bits is input, DMA transfer is started. When DMA transfer is completed after that, this bit is automatically cleared to 0. Write 0 to this bit to forcibly terminate DMA transfer under execution.	

Caution The DSTn flag is automatically cleared to 0 when a DMA transfer is completed. Writing the DENn flag is enabled only when DSTn = 0. When a DMA transfer is terminated without waiting for generation of the interrupt (INTDMA_n) of DMA_n, therefore, set the DSTn bit to 0 and then the DENn bit to 0 (for details, refer to 15.5.5 Forced termination by software).

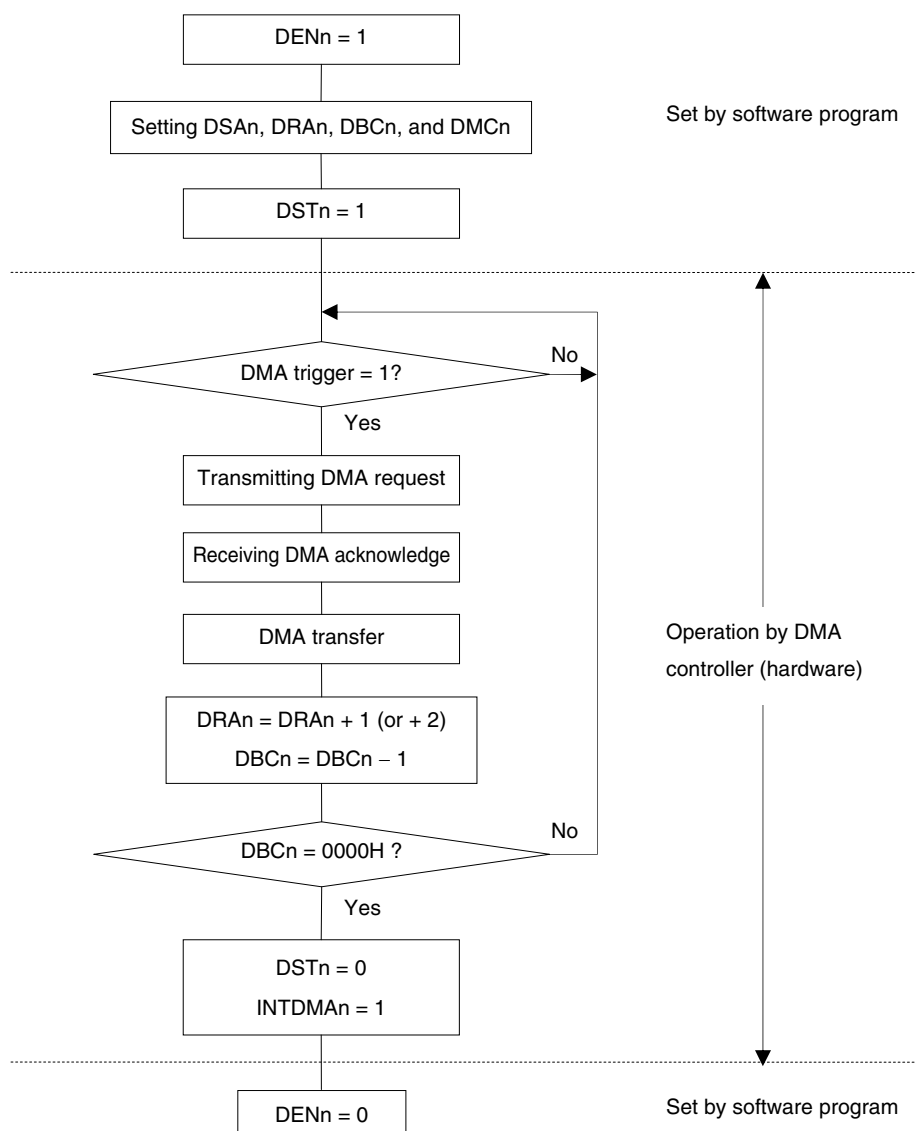
Remark n: DMA channel number (n = 0, 1)

15.4 Operation of DMA Controller

15.4.1 Operation procedure

- <1> The DMA controller is enabled to operate when DENn = 1. Before writing the other registers, be sure to set the DENn bit to 1. Use 80H to write with an 8-bit manipulation instruction.
- <2> Set an SFR address, a RAM address, the number of times of transfer, and a transfer mode of DMA transfer to DMA SFR address register n (DSAn), DMA RAM address register n (DRAn), DMA byte count register n (DBCn), and DMA mode control register n (DMCn).
- <3> The DMA controller waits for a DMA trigger when DSTn = 1. Use 81H to write with an 8-bit manipulation instruction.
- <4> When a software trigger (STGn) or a start source trigger specified by the IFCn3 to IFCn0 bits is input, a DMA transfer is started.
- <5> Transfer is completed when the number of times of transfer set by the DBCn register reaches 0, and transfer is automatically terminated by occurrence of an interrupt (INTDMA_n).
- <6> Stop the operation of the DMA controller by clearing the DENn bit to 0 when the DMA controller is not used.

Figure 15-6. Operation Procedure



Remark n: DMA channel number (n = 0, 1)

15.4.2 Transfer mode

The following four modes can be selected for DMA transfer by using bits 6 and 5 (DRSn and DS_n) of DMA mode control register n (DMCn).

DRSn	DS _n	DMA Transfer Mode
0	0	Transfer from SFR of 1-byte data (fixed address) to RAM (address is incremented by +1)
0	1	Transfer from SFR of 2-byte data (fixed address) to RAM (address is incremented by +2)
1	0	Transfer from RAM of 1-byte data (address is incremented by +1) to SFR (fixed address)
1	1	Transfer from RAM of 2-byte data (address is incremented by +2) to SFR (fixed address)

By using these transfer modes, up to 1024 bytes of data can be consecutively transferred by using the serial interface, data resulting from A/D conversion can be consecutively transferred, and port data can be scanned at fixed time intervals by using a timer.

15.4.3 Termination of DMA transfer

When DBCn = 00H and DMA transfer is completed, the DSTn bit is automatically cleared to 0. An interrupt request (INTDMA_n) is generated and transfer is terminated.

When the DSTn bit is cleared to 0 to forcibly terminate DMA transfer, DMA byte count register n (DBCn) and DMA RAM address register n (DRAn) hold the value when transfer is terminated.

The interrupt request (INTDMA_n) is not generated if transfer is forcibly terminated.

Remark n: DMA channel number (n = 0, 1)

15.5 Example of Setting of DMA Controller

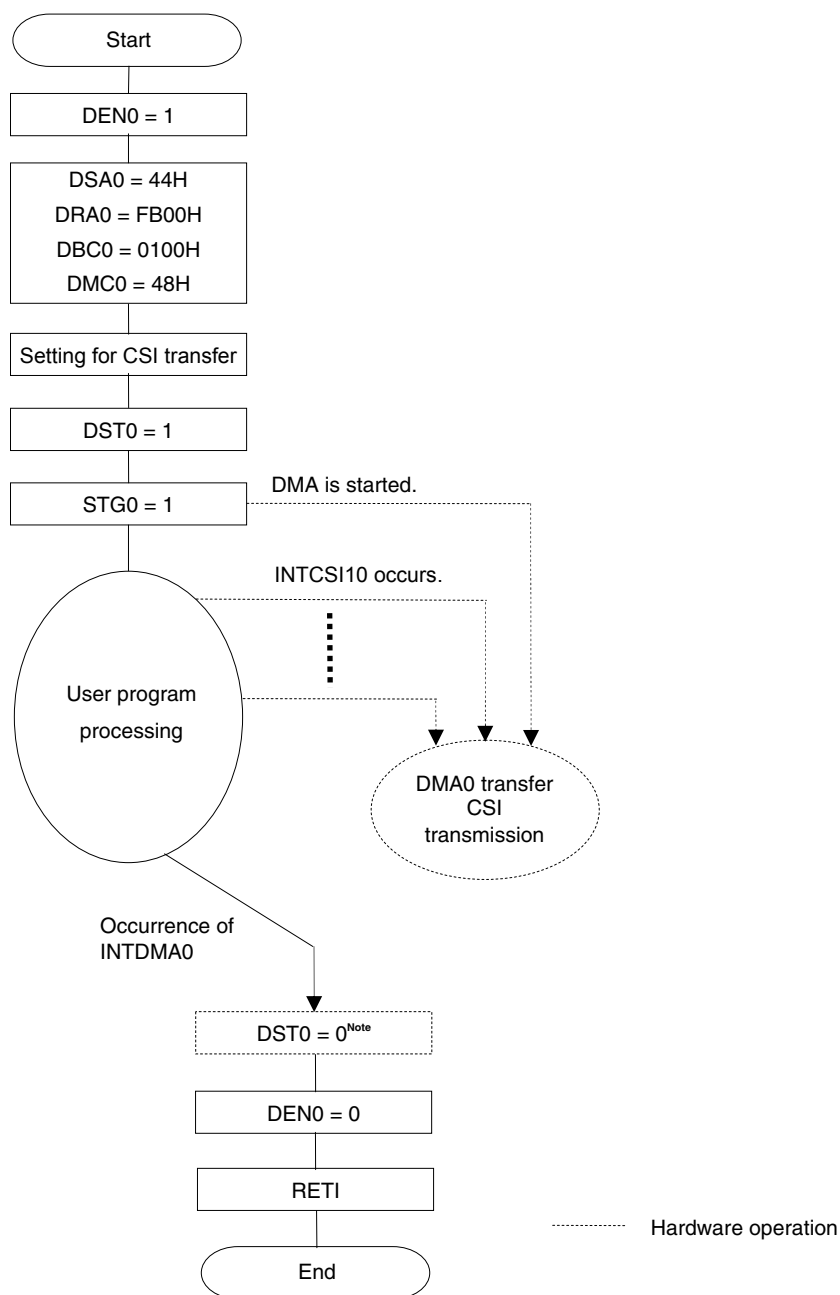
15.5.1 CSI consecutive transmission

A flowchart showing an example of setting for CSI consecutive transmission is shown below.

- Consecutive transmission of CSI10 (256 bytes)
- DMA channel 0 is used for DMA transfer.
- DMA start source: INTCSI10 (software trigger (STG0) only for the first start source)
- Interrupt of CSI10 is specified by IFC03 to IFC00 = 1000B.
- Transfers FFB00H to FFBFFH (256 bytes) of RAM to FFF44H of the data register (SIO10) of CSI.

Remark IFC03 to IFC00: Bits 3 to 0 of DMA mode control registers 0 (DMC0)

Figure 15-7. Example of Setting for CSI Consecutive Transmission



Note The DST0 flag is automatically cleared to 0 when a DMA transfer is completed.

Writing the DEN0 flag is enabled only when DST0 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA0 (INTDMA0), set the DST0 bit to 0 and then the DEN0 bit to 0 (for details, refer to **15.5.5 Forced termination by software**).

The first trigger for consecutive transmission is not started by the interrupt of CSI. In this example, it starts by a software trigger.

CSI transmission of the second time and onward is automatically executed.

A DMA interrupt (INTDMA0) occurs when the last transmit data has been written to the data register.

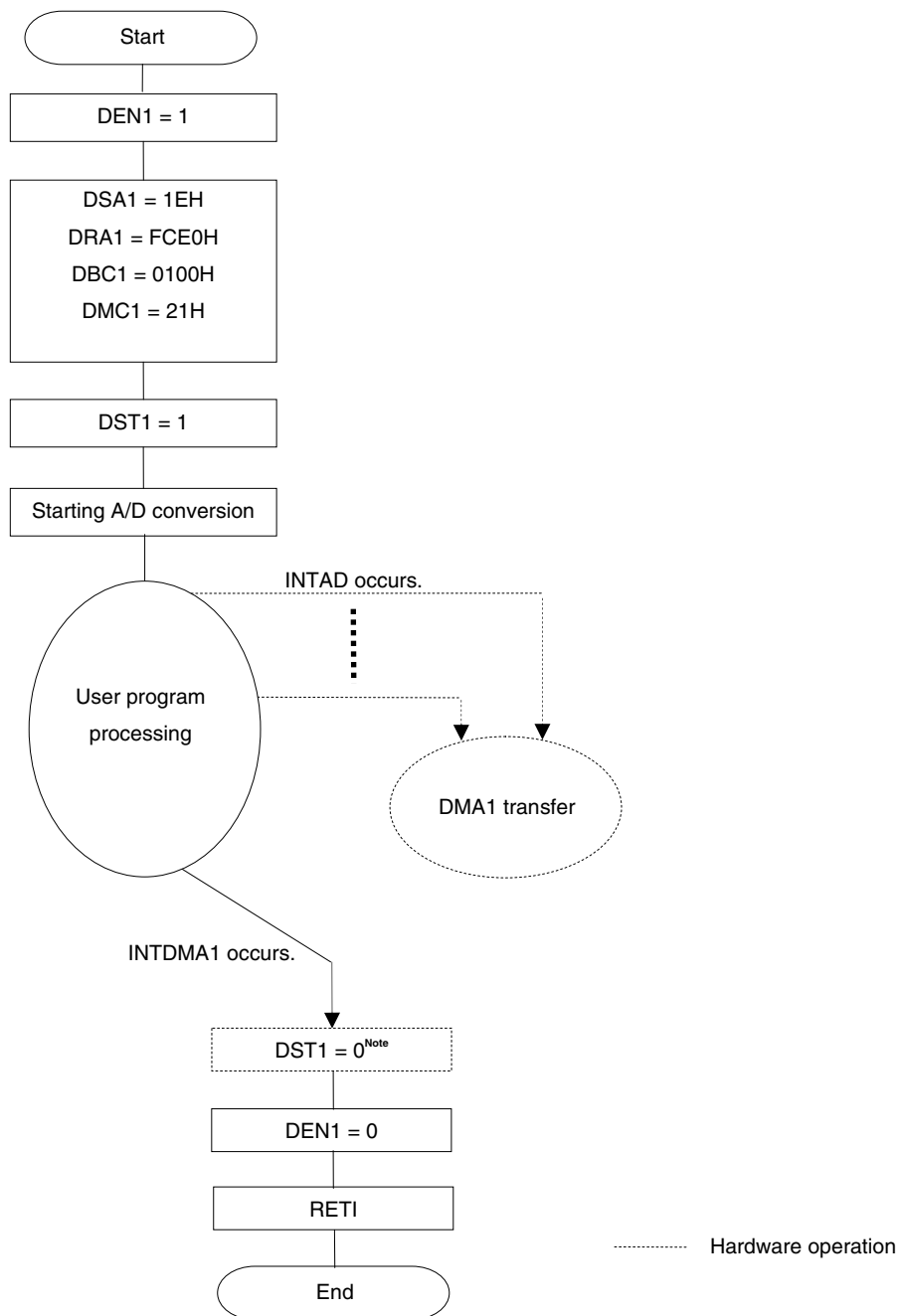
15.5.2 Consecutive capturing of A/D conversion results

A flowchart of an example of setting for consecutively capturing A/D conversion results is shown below.

- Consecutive capturing of A/D conversion results.
- DMA channel 1 is used for DMA transfer.
- DMA start source: INTAD
- Interrupt of A/D is specified by IFC13 to IFC10 = 0001B.
- Transfers FFF1EH and FFF1FH (2 bytes) of the 12-bit A/D conversion result register (ADCR) to 512 bytes of FFCE0H to FFEDFH of RAM.

Remark IFC13 to IFC10: Bits 3 to 0 of DMA mode control registers 1 (DMC1)

Figure 15-8. Example of Setting of Consecutively Capturing A/D Conversion Results



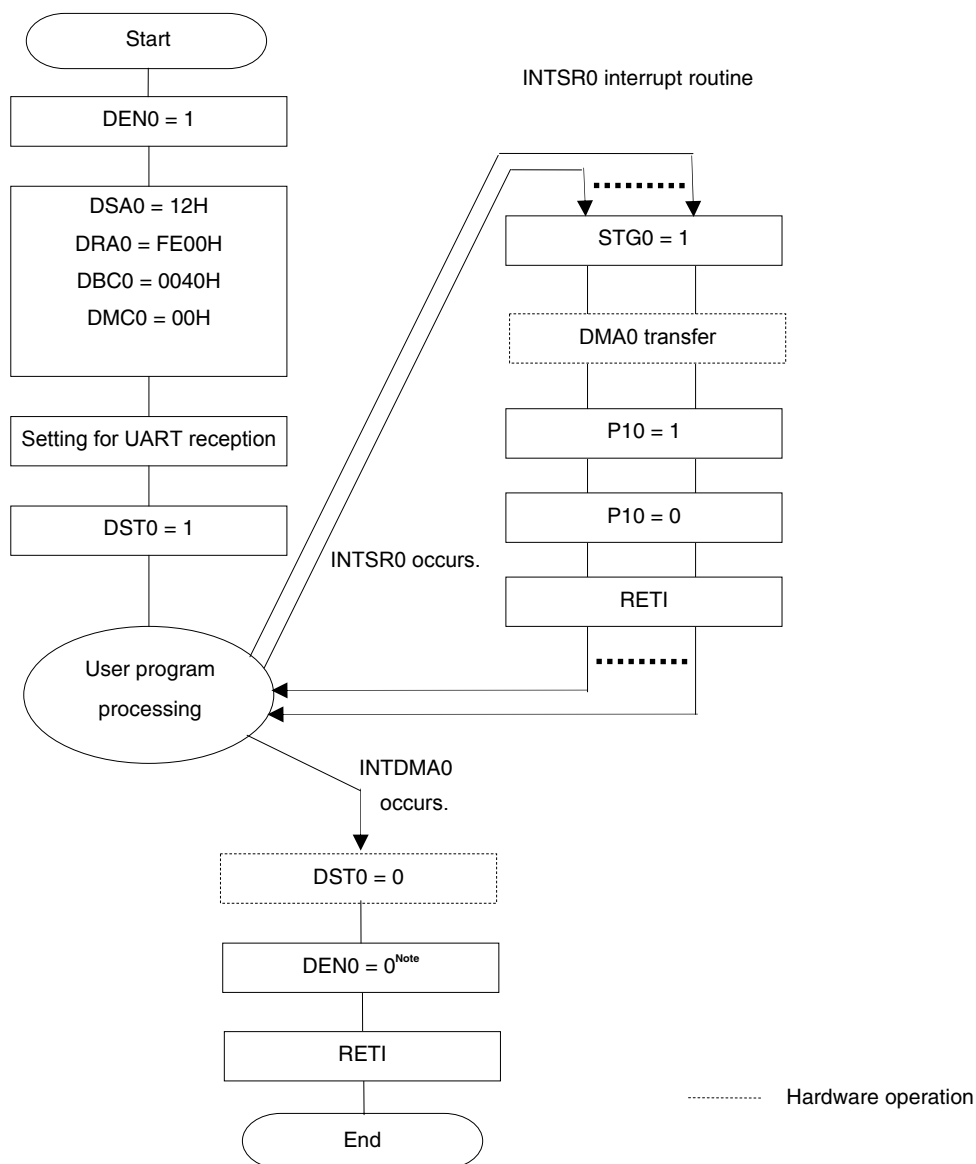
Note The DST1 flag is automatically cleared to 0 when a DMA transfer is completed.

Writing the DEN1 flag is enabled only when DST1 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA1 (INTDMA1), set the DST1 bit to 0 and then the DEN1 bit to 0 (for details, refer to **15.5.5 Forced termination by software**).

15.5.3 UART consecutive reception + ACK transmission

A flowchart illustrating an example of setting for UART consecutive reception + ACK transmission is shown below.

- Consecutively receives data from UART0 and outputs ACK to P10 on completion of reception.
- DMA channel 0 is used for DMA transfer.
- DMA start source: Software trigger (DMA transfer on occurrence of an interrupt is disabled.)
- Transfers FFF12H of UART receive data register 0 (RXD0) to 64 bytes of FFE00H to FFE3FH of RAM.

Figure 15-9. Example of Setting for UART Consecutive Reception + ACK Transmission

Note The DST0 flag is automatically cleared to 0 when a DMA transfer is completed.

Writing the DEN0 flag is enabled only when DST0 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA0 (INTDMA0), set the DST0 bit to 0 and then the DEN0 bit to 0 (for details, refer to **15.5.5 Forced termination by software**).

Remark This is an example where a software trigger is used as a DMA start source.

If ACK is not transmitted and if only data is consecutively received from UART, the UART reception end interrupt (INTSR0) can be used to start DMA for data reception.

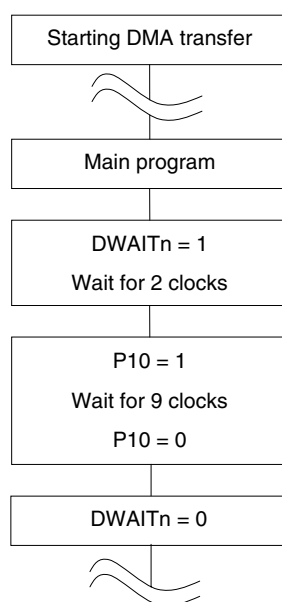
15.5.4 Holding DMA transfer pending by DWAITn bit

When DMA transfer is started, transfer is performed while an instruction is executed. At this time, the operation of the CPU is stopped and delayed for the duration of 2 clocks. If this poses a problem to the operation of the set system, a DMA transfer can be held pending by setting the DWAITn bit to 1. The DMA transfer for a transfer trigger that occurred while DMA transfer was held pending is executed after the pending status is canceled. However, because only one transfer trigger can be held pending for each channel, even if multiple transfer triggers occur for one channel during the pending status, only one DMA transfer is executed after the pending status is canceled.

To output a pulse with a width of 10 clocks of the operating frequency from the P10 pin, for example, the clock width increases to 12 if a DMA transfer is started midway. In this case, the DMA transfer can be held pending by setting the DWAITn bit to 1.

After setting the DWAITn bit to 1, it takes two clocks until a DMA transfer is held pending.

Figure 15-10. Example of Setting for Holding DMA Transfer Pending by DWAITn Bit



Caution When DMA transfer is held pending while using two or more DMA channels, be sure to held the DMA transfer pending for all channels (by setting DWAIT0 and DWAIT1 to 1). If the DMA transfer of one channel is executed while that of the other channel is held pending, DMA transfer might not be held pending for the latter channel.

Remarks

1. n: DMA channel number (n = 0, 1)
2. 1 clock: $1/f_{CLK}$ (f_{CLK} : CPU clock)

15.5.5 Forced termination by software

After the DSTn bit is set to 0 by software, it takes up to 2 clocks until a DMA transfer is actually stopped and the DSTn bit is set to 0. To forcibly terminate a DMA transfer by software without waiting for occurrence of the interrupt (INTDMA_n) of DMA_n, therefore, perform either of the following processes.

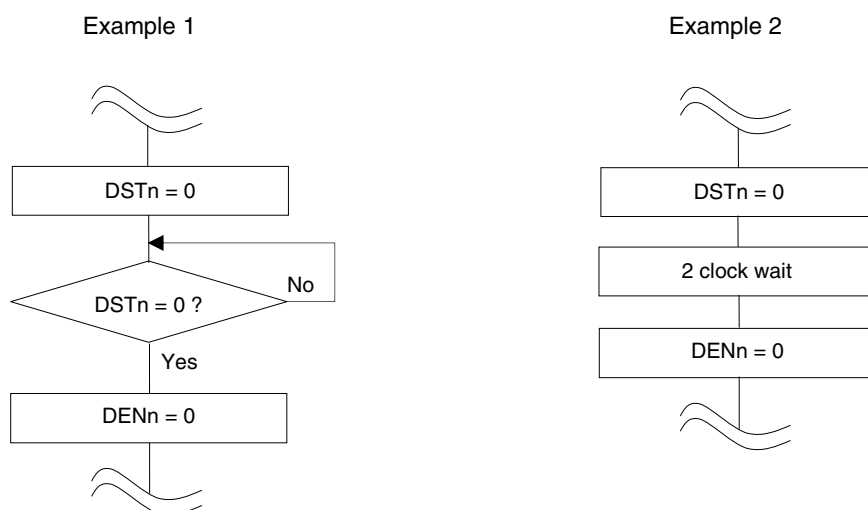
<When using one DMA channel>

- Set the DSTn bit to 0 (use DRCn = 80H to write with an 8-bit manipulation instruction) by software, confirm by polling that the DSTn bit has actually been cleared to 0, and then set the DENn bit to 0 (use DRCn = 00H to write with an 8-bit manipulation instruction).
- Set the DSTn bit to 0 (use DRCn = 80H to write with an 8-bit manipulation instruction) by software and then set the DENn bit to 0 (use DRCn = 00H to write with an 8-bit manipulation instruction) two or more clocks after.

<When using two or more DMA channels>

- To forcibly terminate DMA transfer by software when using two or more DMA channels (by setting DSTn to 0), clear the DSTn bit to 0 after the DMA transfer is held pending by setting the DWAITn bits of all using channels to 1. Next, clear the DWAITn bits of all using channels to 0 to cancel the pending status, and then clear the DENn bit to 0.

Figure 15-11. Forced Termination of DMA Transfer (1/2)

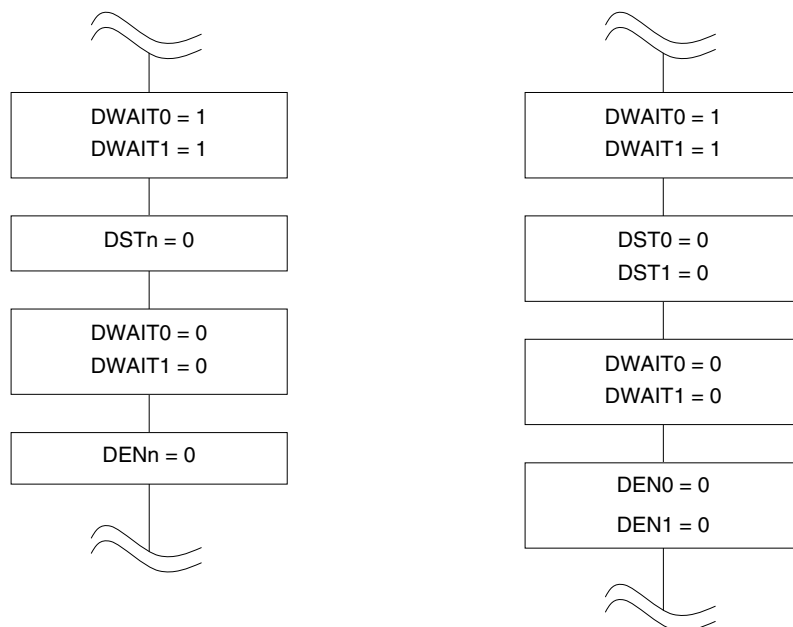


- Remarks**
1. n: DMA channel number (n = 0, 1)
 2. 1 clock: $1/f_{CLK}$ (f_{CLK} : CPU clock)

Figure 15-11. Forced Termination of DMA Transfer (2/2)**Example 3**

- Procedure for forcibly terminating the DMA transfer for one channel if both channels are used

- Procedure for forcibly terminating the DMA transfer for both channels if both channels are used



Caution In example 3, the system is not required to wait two clock cycles after the $DWAITn$ bit is set to 1. In addition, the system does not have to wait two clock cycles after clearing the $DSTn$ bit to 0, because more than two clock cycles elapse from when the $DSTn$ bit is cleared to 0 to when the $DENn$ bit is cleared to 0.

- Remarks**
1. n : DMA channel number ($n = 0, 1$)
 2. 1 clock: $1/f_{CLK}$ (f_{CLK} : CPU clock)

15.6 Cautions on Using DMA Controller

(1) Priority of DMA

During DMA transfer, a request from the other DMA channel is held pending even if generated. The pending DMA transfer is started after the ongoing DMA transfer is completed. If two or more DMA requests are generated at the same time, however, their priority are DMA channel 0 > DMA channel 1.

If a DMA request and an interrupt request are generated at the same time, the DMA transfer takes precedence, and then interrupt servicing is executed.

(2) DMA response time

The response time of DMA transfer is as follows.

Table 15-2. Response Time of DMA Transfer

	Minimum Time	Maximum Time
Response time	3 clocks	10 clocks ^{Note}

Note The maximum time necessary to execute an instruction from internal RAM is 16 clock cycles.

Cautions 1. The above response time does not include the two clock cycles required for a DMA transfer.

2. When executing a DMA pending instruction (see 15.6 (4)), the maximum response time is extended by the execution time of that instruction to be held pending.
3. Do not specify successive transfer triggers for a channel within a period equal to the maximum response time plus one clock cycle, because they might be ignored.

Remark 1 clock: $1/f_{CLK}$ (f_{CLK} : CPU clock)

(3) Operation in standby mode

The DMA controller operates as follows in the standby mode.

Table 15-3. DMA Operation in Standby Mode

Status	DMA Operation
HALT mode	Normal operation
STOP mode	Stops operation. If DMA transfer and STOP instruction execution contend, DMA transfer may be damaged. Therefore, stop DMA before executing the STOP instruction.

(4) DMA transfer pending instruction

Even if a DMA request is generated, DMA transfer is held pending immediately after the following instructions.

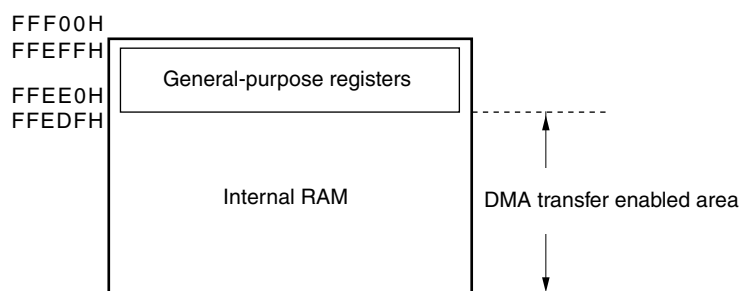
- CALL !addr16
- CALL \$!addr20
- CALL !!addr20
- CALL rp
- CALLT [addr5]
- BRK
- Bit manipulation instructions for registers IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, and PSW each.
- Instruction for accessing the data flash memory

(5) Operation if address in general-purpose register area or other than those of internal RAM area is specified

The address indicated by DMA RAM address register n (DRAn) is incremented during DMA transfer. If the address is incremented to an address in the general-purpose register area or exceeds the area of the internal RAM, the following operation is performed.

- In mode of transfer from SFR to RAM
The data of that address is lost.
- In mode of transfer from RAM to SFR
Undefined data is transferred to SFR.

In either case, malfunctioning may occur or damage may be done to the system. Therefore, make sure that the address is within the internal RAM area other than the general-purpose register area.

**(6) Operation if instructions for accessing the data flash area**

- Because DMA transfer is suspended to access to the data flash area, be sure to add the DMA pending instruction.

If the data flash area is accessed after an next instruction execution from start of DMA transfer, a 3-clock wait will be inserted to the next instruction.

Instruction 1

DMA transfer

Instruction 2 ← The wait of three clock cycles occurs.

MOV A, ! DataFlash area

CHAPTER 16 INTERRUPT FUNCTIONS

<R> The interrupt function switches the program execution to other processing. When the branch processing is finished, the program returns to the interrupted processing.

The number of interrupt sources differs, depending on the product.

		25-pin	32-pin	48-pin	64-pin
Maskable interrupts	External	5	6	10	13
	Internal	24	27	27	27

16.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into four priority groups by setting the priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H).

Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the default priority of vectored interrupt servicing. Default priority, see **Table 16-1**.

A standby release signal is generated and STOP, HALT, and SNOOZE modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

(2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

16.2 Interrupt Sources and Configuration

Interrupt sources include maskable interrupts and software interrupts. In addition, they also have up to seven reset sources (see **Table 16-1**). The vector codes that store the program start address when branching due to the generation of a reset or various interrupt requests are two bytes each, so interrupts jump to a 64 K address of 00000H to 0FFFFH.

Table 16-1. Interrupt Source List (1/3)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	64-pin	48-pin	32-pin	25-pin
		Name	Trigger							
Maskable	0	INTWDTI	Watchdog timer interval Note 3 (75% of overflow time+1/2f _{IL})	Internal	0004H	(A)	√	√	√	√
	1	INTLVI	Voltage detection Note 4		0006H		√	√	√	√
	2	INTP0	Pin input edge detection	External	0008H	(B)	√	√	√	√
	3	INTP1			000AH		√	√	√	√
	4	INTP2			000CH		√	√	√	√
	5	INTP3			000EH		√	√	√	√
	6	INTP4			0010H		√	√	√	√
	7	INTP5			0012H		√	√	—	—
	8	INTST2/ INTCSI20/ INTIIC20	UART2 transmission transfer end or buffer empty interrupt/CSI20 transfer end or buffer empty interrupt/IIC20 transfer end	Internal	0014H	(A)	√	√	√	—
	9	INTSR2/ INTCSI21/ INTIIC21	UART2 reception transfer end/CSI21 transfer end or buffer empty interrupt/IIC21 transfer end		0016H		√	√	√ Note 6	—
	10	INTSRE2	UART2 reception communication error occurrence		0018H		√	√	√	—
	11	INTDMA0	End of DMA0 transfer		001AH		√	√	√	√
	12	INTDMA1	End of DMA1 transfer		001CH		√	√	√	√
	13	INTST0/ INTCSI00/ INTIIC00	UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt/IIC00 transfer end		001EH		√	√	√	√
	14	INTSR0/ INTCSI01/ INTIIC01	UART0 reception transfer end/CSI01 transfer end or buffer empty interrupt/IIC01 transfer end		0020H		√	√	√ Note 5	√ Note 5
	15	INTSRE0	UART0 reception communication error occurrence	0022H	√	√	√	√		
		INTTM01H	End of timer channel 1 count or capture (at higher 8-bit timer operation)		√	√	√	√		

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 39 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 16-1.

3. When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.

4. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is cleared to 0.

5. INTSR0 only.

6. INTSR2 only

Table 16-1. Interrupt Source List (2/3)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	64-pin	48-pin	32-pin	25-pin
		Name	Trigger							
Maskable	16	INTST1/ INTCSI10/ INTIIC10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt/IIC10 transfer end	Internal	0024H	(A)	√	√ Note 3	√ Note 3	√ Note 3
	17	INTSR1/ INTCSI11/ INTIIC11	UART1 reception transfer end/CSI11 transfer end or buffer empty interrupt/IIC11 transfer end		0026H		√	√	√	√
	18	INTSRE1	UART1 reception communication error occurrence		0028H		√	√	√	√
		INTTM03H	End of timer channel 3 count or capture (at higher 8-bit timer operation)				√	√	√	√
	19	INTIICA0	End of IICA0 communication		002AH		√	√	√	√
	20	INTTM00	End of timer channel 0 count or capture		002CH		√	√	√	√
	21	INTTM01	End of timer channel 1 count or capture (at 16-bit/lower 8-bit timer operation)		002EH		√	√	√	√
	22	INTTM02	End of timer channel 2 count or capture		0030H		√	√	√	√
	23	INTTM03	End of timer channel 3 count or capture (at 16-bit/lower 8-bit timer operation)		0032H		√	√	√	√
	24	INTAD	End of A/D conversion		0034H		√	√	√	√
	25	INTRTC	Fixed-cycle signal of real-time clock/alarm match detection		0036H		√	√	√	√
	26	INTIT	Interval signal of 12-bit interval timer detection		0038H		√	√	√	√
	27	INTKR	Key return signal detection	External	003AH	(C)	√	√	√	(√) Note 4
	28	INTTM04	End of timer channel 4 count or capture	Internal	0042H	(A)	√	√	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 39 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 16-1.

3. INTST1 only.

4. When setting peripheral I/O redirection register (PIOR)

Table 16-1. Interrupt Source List (3/3)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	64-pin	48-pin	32-pin	25-pin
		Name	Trigger							
Maskable	29	INTTM05	End of timer channel 5 count or capture	Internal	0044H	(A)	√	√	√	√
	30	INTTM06	End of timer channel 6 count or capture		0046H		√	√	√	√
	31	INTTM07	End of timer channel 7 count or capture		0048H		√	√	√	√
	32	INTP6	Pin input edge detection	External	004AH	(B)	√	√	–	–
	33	INTP7			004CH		√	–	–	–
	34	INTP8			004EH		√	√	–	–
	35	INTP9			0050H		√	√	–	–
	36	INTP10			0052H		√	–	–	–
	37	INTP11			0054H		√	–	–	–
	38	INTMD	End of division operation/ Overflow occur	Internal	005EH	(A)	√	√	√	√
	39	INTFL	End of sequencer interrupt ^{Note 3}		0062H		√	√	√	√
Software	–	BRK	Execution of BRK instruction	–	007EH	(D)	√	√	√	√
Reset	–	RESET	RESET pin input	–	0000H	–	√	√	√	√
		POR	Power-on-reset				√	√	√	√
		LVD	Voltage detection ^{Note 3}				√	√	√	√
		WDT	Overflow of watchdog timer				√	√	√	√
		TRAP	Execution of illegal instruction ^{Note 4}				√	√	√	√
		IAW	Illegal-memory access				√	√	√	√
		RPE	RAM parity error				√	√	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 39 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 16-1.

3. Be used only at the self programming library.

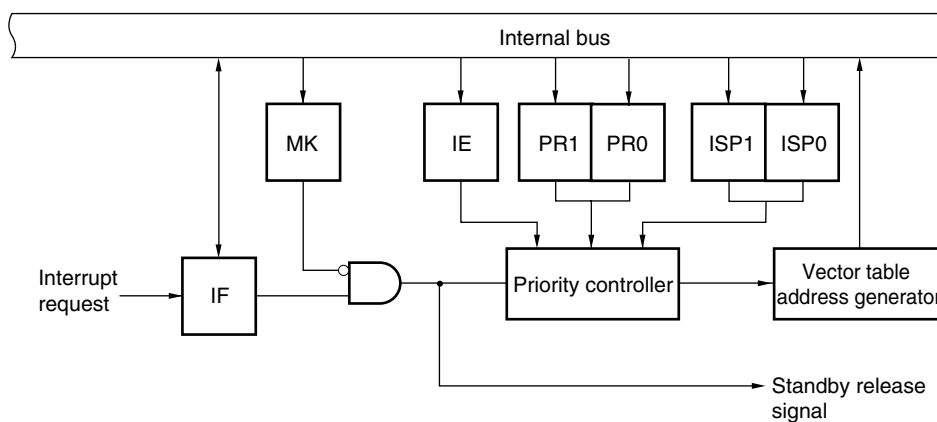
4. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is set to 1.

5. When the instruction code in FFH is executed.

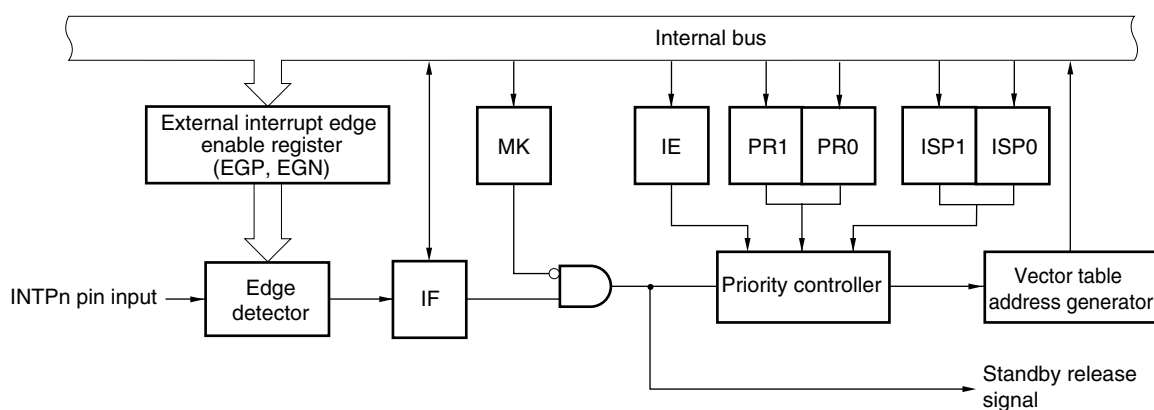
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Figure 16-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal maskable interrupt



(B) External maskable interrupt (INTPn)

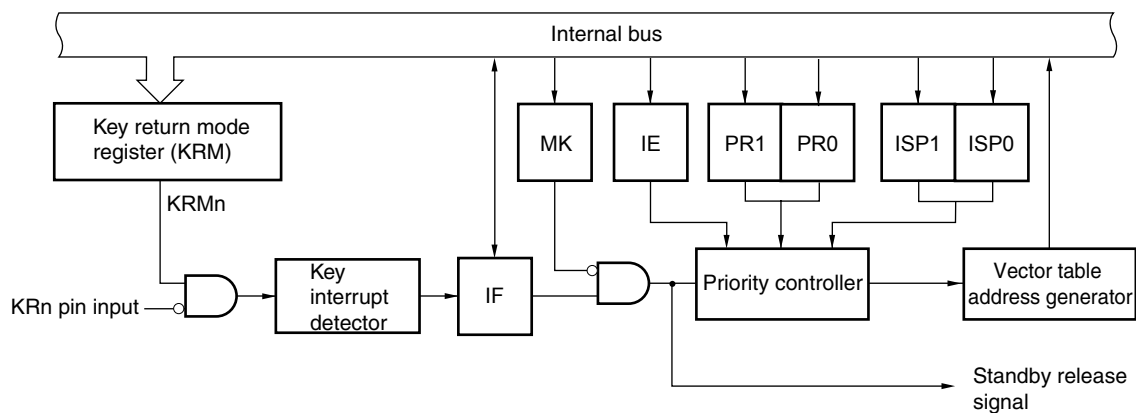


IF: Interrupt request flag
 IE: Interrupt enable flag
 ISP0: In-service priority flag 0
 ISP1: In-service priority flag 1
 MK: Interrupt mask flag
 PR0: Priority specification flag 0
 PR1: Priority specification flag 1

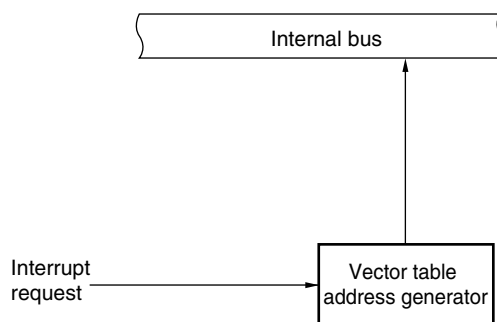
Remark 25, 32-pin: n = 0 to 4
 48-pin: n = 0 to 6, 8, 9
 64-pin: n = 0 to 11

Figure 16-1. Basic Configuration of Interrupt Function (2/2)

(C) External maskable interrupt (INTKR)



(D) Software interrupt



IF: Interrupt request flag
 IE: Interrupt enable flag
 ISP0: In-service priority flag 0
 ISP1: In-service priority flag 1
 MK: Interrupt mask flag
 PR0: Priority specification flag 0
 PR1: Priority specification flag 1

Remark 32-pin: n = 0
 48-pin: n = 0 to 5
 64-pin: n = 0 to 9

16.3 Registers Controlling Interrupt Functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)
- Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)
- Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H)
- External interrupt rising edge enable registers (EGP0, EGP1)
- External interrupt falling edge enable registers (EGN0, EGN1)
- Program status word (PSW)

Table 16-2 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 16-2. Flags Corresponding to Interrupt Request Sources (1/4)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag		64-pin	48-pin	32-pin	25-pin
		Register		Register		Register				
INTWDTI	WDTIIF	IF0L	WDTIMK	MK0L	WDTIPR0, WDTIPR1	PR00L, PR10L	√	√	√	√
INTLVI	LVIIIF		LVIMK		LVIPR0, LVIPR1		√	√	√	√
INTP0	PIF0		PMK0		PPR00, PPR10		√	√	√	√
INTP1	PIF1		PMK1		PPR01, PPR11		√	√	√	√
<R> INTP2	PIF2		PMK2		PPR02, PPR12		√	√	√	√
INTP3	PIF3		PMK3		PPR03, PPR13		√	√	√	√
INTP4	PIF4		PMK4		PPR04, PPR14		√	√	√	√
<R> INTP5	PIF5		PMK5		PPR05, PPR15		√	√	—	—

Table 16-2. Flags Corresponding to Interrupt Request Sources (2/4)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag		64-pin	48-pin	32-pin	25-pin
		Register		Register		Register				
INTST2 ^{Note 1}	STIF2 ^{Note 1}	IF0H	STMK2 ^{Note 1}	MK0H	STPR02, STPR12 ^{Note 1}	PR00H, PR10H	√	√	√	—
INTCSI20 ^{Note 1}	CSIF20 ^{Note 1}		CSIMK20 ^{Note 1}		CSIPR020, CSIPR120 ^{Note 1}		√	√	√	—
INTIIC20 ^{Note 1}	IICIF20 ^{Note 1}		IICMK20 ^{Note 1}		IICPR020, IICPR120 ^{Note 1}		√	√	√	—
INTSR2 ^{Note 2}	SRIF2 ^{Note 2}		SRMK2 ^{Note 2}		SRPR02, SRPR12 ^{Note 2}		√	√	√	—
INTCSI21 ^{Note 2}	CSIF21 ^{Note 2}		CSIMK21 ^{Note 2}		CSIPR021, CSIPR121 ^{Note 2}		√	√	—	—
INTIIC21 ^{Note 2}	IICIF21 ^{Note 2}		IICMK21 ^{Note 2}		IICPR021, IICPR121 ^{Note 2}		√	√	—	—
INTSRE2	SREIF2		SREMK2		SREPR02, SREPR12		√	√	√	—
INTDMA0	DMAIF0		DMAMK0		DMAPR00, DMAPR10		√	√	√	√
INTDMA1	DMAIF1		DMAMK1		DMAPR01, DMAPR11		√	√	√	√
INTST0 ^{Note 3}	STIF0 ^{Note 3}		STMK0 ^{Note 3}		STPR00, STPR10 ^{Note 3}		√	√	√	√
INTCSI00 ^{Note 3}	CSIF00 ^{Note 3}	IF0H	CSIMK00 ^{Note 3}	MK0H	CSIPR000, CSIPR100 ^{Note 3}	PR00H, PR10H	√	√	√	√
INTIIC00 ^{Note 3}	IICIF00 ^{Note 3}		IICMK00 ^{Note 3}		IICPR000, IICPR100 ^{Note 3}		√	√	√	√
INTSR0 ^{Note 4}	SRIF0 ^{Note 4}		SRMK0 ^{Note 4}		SRPR00, SRPR10 ^{Note 4}		√	√	√	√
INTCSI01 ^{Note 4}	CSIF01 ^{Note 4}		CSIMK01 ^{Note 4}		CSIPR001, CSIPR101 ^{Note 4}		√	√	—	—
INTIIC01 ^{Note 4}	IICIF01 ^{Note 4}		IICMK01 ^{Note 4}		IICPR001, IICPR101 ^{Note 4}		√	√	—	—
INTSRE0 ^{Note 5}	SREIF0 ^{Note 5}		SREMK0 ^{Note 5}		SREPR00, SREPR10 ^{Note 5}		√	√	√	√
INTTM01H ^{Note 5}	TMIF01H ^{Note 5}		TMMK01H ^{Note 5}		TMPR001H, TMPR101H ^{Note 5}		√	√	√	√

- Notes**
1. If one of the interrupt sources INTST2, INTCSI20, and INTIIC20 is generated, bit 0 of the IF0H register is set to 1. Bit 0 of the MK0H, PR00H, and PR10H registers can be used for all three of these interrupt sources.
 2. If one of the interrupt sources INTSR2, INTCSI21, and INTIIC21 is generated, bit 1 of the IF0H register is set to 1. Bit 1 of the MK0H, PR00H, and PR10H registers can be used for all three of these interrupt sources.
 3. If one of the interrupt sources INTST0, INTCSI00, and INTIIC00 is generated, bit 5 of the IF0H register is set to 1. Bit 5 of the MK0H, PR00H, and PR10H registers can be used for all three of these interrupt sources.
 4. If one of the interrupt sources INTSR0, INTCSI01, and INTIIC01 is generated, bit 6 of the IF0H register is set to 1. Bit 6 of the MK0H, PR00H, and PR10H registers can be used for all three of these interrupt sources.
 5. Do not use the error interrupt of UART0 reception and the interrupt of channel 1 of TAU0 (while the higher 8 bits are operating at a timer) at the same time because they share flags for the interrupt request sources. If the error interrupt of UART0 reception is not used (EOC01 = 0), UART0 and channel 1 of TAU0 (while the higher 8 bits are operating at a timer) can be used at the same time. If the interrupt source INTSRE0 or INTTM01H is generated, bit 7 of the IF0H register is set to 1. Bit 7 of the MK0H, PR00H, and PR10H registers can be used for both these interrupt sources.

Table 16-2. Flags Corresponding to Interrupt Request Sources (3/4)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag		64-pin	48-pin	32-pin	25-pin
		Register		Register		Register				
INTST1 ^{Note 1}	STIF1 ^{Note 1}	IF1L	STMK1 ^{Note 1}	MK1L	STPR01, STPR11 ^{Note 1}	PR01L, PR11L	√	√	√	√
INTCSI10 ^{Note 1}	CSIIF10 ^{Note 1}		CSIMK10 ^{Note 1}		CSIPR010, CSIPR110 ^{Note 1}		√	—	—	—
INTIIC10 ^{Note 1}	IICIF10 ^{Note 1}		IICMK10 ^{Note 1}		IICPR010, IICPR110 ^{Note 1}		√	—	—	—
INTSR1 ^{Note 2}	SRIF1 ^{Note 2}		SRMK1 ^{Note 2}		SRPR01, SRPR11 ^{Note 2}		√	√	√	√
INTCSI11 ^{Note 2}	CSIIF11 ^{Note 2}		CSIMK11 ^{Note 2}		CSIPR011, CSIPR111 ^{Note 2}		√	√	√	√
INTIIC11 ^{Note 2}	IICIF11 ^{Note 2}		IICMK11 ^{Note 2}		IICPR011, IICPR111 ^{Note 2}		√	√	√	√
INTSRE1 ^{Note 3}	SREIF1 ^{Note 3}		SREMK1 ^{Note 3}		SREPR01, SREPR11 ^{Note 3}		√	√	√	√
INTTM03H ^{Note 3}	TMIF03H ^{Note 3}		TMMK03H ^{Note 3}		TMPR003H, TMPR103H ^{Note 3}		√	√	√	√
INTIICA0	IICAIF0		IICAMK0		IICAPR00, IICAPR10		√	√	√	√
INTTM00	TMIF00		TMMK00		TMPR000, TMPR100		√	√	√	√
INTTM01	TMIF01		TMMK01		TMPR001, TMPR101		√	√	√	√
INTTM02	TMIF02		TMMK02		TMPR002, TMPR102		√	√	√	√
INTTM03	TMIF03		TMMK03		TMPR003, TMPR103		√	√	√	√
INTAD	ADIF	IF1H	ADMK	MK1H	ADPR0, ADPR1	PR01H, PR11H	√	√	√	√
INTRTC	RTCIF		RTCMK		RTCPR0, RTCPR1		√	√	√	√
INTIT	ITIF		ITMK		ITPR0, ITPR1		√	√	√	√
INTKR	KRIF		KRMK		KRPR0, KRPR1		√	√	√	(√)
INTTM04	TMIF04		TMMK04		TMPR004, TMPR104		√	√	√	√

- Notes**
1. If one of the interrupt sources INTST1, INTCSI10, and INTIIC10 is generated, bit 0 of the IF1L register is set to 1. Bit 0 of the MK1L, PR01L, and PR11L registers can be used for all three of these interrupt sources.
 2. If one of the interrupt sources INTSR1, INTCSI11, and INTIIC11 is generated, bit 1 of the IF1L register is set to 1. Bit 1 of the MK1L, PR01L, and PR11L registers can be used for all three of these interrupt sources.
 3. Do not use the error interrupt of UART1 reception and the interrupt of channel 3 of TAU0 (while the higher 8 bits are operating at a timer) at the same time because they share flags for the interrupt request sources. If the error interrupt of UART1 reception is not used (EOC02 = 0), UART1 and channel 3 of TAU0 (while the higher 8 bits are operating at a timer) can be used at the same time. If the interrupt source INTSRE1 or INTTM03H is generated, bit 2 of the IF1L register is set to 1. Bit 2 of the MK1L, PR01L, and PR11L registers can be used for both these interrupt sources.

Table 16-2. Flags Corresponding to Interrupt Request Sources (4/4)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag		64-pin	48-pin	32-pin	25-pin
		Register		Register		Register				
INTTM05	TMIF05	IF2L	TMMK05	MK2L	TMPR005, TMPR105	PR02L, PR12L	√	√	√	√
INTTM06	TMIF06		TMMK06		TMPR006, TMPR106		√	√	√	√
INTTM07	TMIF07		TMMK07		TMPR007, TMPR107		√	√	√	√
INTP6	PIF6		PMK6		PPR06, PPR16		√	√	–	–
INTP7	PIF7		PMK7		PPR07, PPR17		√	–	–	–
INTP8	PIF8		PMK8		PPR08, PPR18		√	√	–	–
INTP9	PIF9		PMK9		PPR09, PPR19		√	√	–	–
INTP10	PIF10		PMK10		PPR010, PPR110		√	–	–	–
INTP11	PIF11	IF2H	PMK11	MK2H	PPR011, PPR111	PR02H, PR12H	√	–	–	–
INTMD	MDIF		MDMK		MDPR0, MDPR1		√	√	√	√
INTFL	FLIF		FLMK		FLPR0, FLPR1		√	√	√	√

16.3.1 Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)

The interrupt request flags are set to 1 when the corresponding interrupt request is generated or an instruction is executed. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is entered.

The IF0L, IF0H, IF1L, IF1H, IF2L, and IF2H registers can be set by a 1-bit or 8-bit memory manipulation instruction. When the IF0L and IF0H registers, the IF1L and IF1H registers, and the IF2L and IF2H registers are combined to form 16-bit registers IF0, IF1, and IF2, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 16-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H) (64-pin) (1/2)

Address: FFFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIF	WDTIF

Address: FFFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	SREIF0 TMIF01H	SRIF0 CSIF01 IICIF01	STIF0 CSIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIF21 IICIF21	STIF2 CSIF20 IICIF20

Address: FFFE2H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF1L	TMIF03	TMIF02	TMIF01	TMIF00	IICAF0	SREIF1 TMIF03H	SRIF1 CSIF11 IICIF11	STIF1 CSIF10 IICIF10

Address: FFFE3H After reset: 00H R/W

Symbol	<7>	6	5	4	<3>	<2>	<1>	<0>
IF1H	TMIF04	0	0	0	KRIF	ITIF	RTCIF	ADIF

Address: FFFD0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF2L	PIF10	PIF9	PIF8	PIF7	PIF6	TMIF07	TMIF06	TMIF05

Figure 16-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H) (64-pin) (2/2)

Address: FFFD1H After reset: 00H R/W

Symbol	<7>	6	<5>	4	3	2	1	<0>
IF2H	FLIF	0	MDIF	0	0	0	0	PIF11

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Cautions 1. The above is the bit layout for the 64-pin. The available bits differ depending on the product. For details about the bits available for each product, see Table 16-2. Be sure to clear bits that are not available to 0.

2. When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as “IF0L.0 = 0;” or “_asm(“clr1 IF0L, 0”);” because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).

If a program is described in C language using an 8-bit memory manipulation instruction such as “IF0L &= 0xfe;” and compiled, it becomes the assembler of three instructions.

```
mov a, IF0L
and a, #0FEH
mov IF0L, a
```

In this case, even if the request flag of the another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between “mov a, IF0L” and “mov IF0L, a”, the flag is cleared to 0 at “mov IF0L, a”. Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.

16.3.2 Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)

The interrupt mask flags are used to enable/disable the corresponding maskable interrupt servicing.

The MK0L, MK0H, MK1L, MK1H, MK2L, and MK2H registers can be set by a 1-bit or 8-bit memory manipulation instruction. When the MK0L and MK0H registers, the MK1L and MK1H registers, and the MK2L and MK2H registers are combined to form 16-bit registers MK0, MK1, and MK2, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 16-3. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H) (64-pin)

Address: FFFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	<1>	<0>
MK1H	TMMK04	1	1	1	KRMK	ITMK	RTCMK	ADMK

Address: FFFD4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK2L	PMK10	PMK9	PMK8	PMK7	PMK6	TMMK07	TMMK06	TMMK05

Address: FFFD5H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	<0>
MK2H	FLMK	1	MDMK	1	1	1	1	PMK11

XXMKX	Interrupt servicing control						
0	Interrupt servicing enabled						
1	Interrupt servicing disabled						

Caution The above is the bit layout for the 64-pin. The available bits differ depending on the product. For details about the bits available for each product, see Table 16-2. Be sure to set bits that are not available to 1.

16.3.3 Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H)

The priority specification flag registers are used to set the corresponding maskable interrupt priority level.

A priority level is set by using the PR0xy and PR1xy registers in combination (xy = 0L, 0H, 1L, 1H, 2L, or 2H).

The PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, and the PR12H registers can be set by a 1-bit or 8-bit memory manipulation instruction. If the PR00L and PR00H registers, the PR01L and PR01H registers, the PR02L and PR02H registers, the PR10L and PR10H registers, the PR11L and PR11H registers, and the PR12L and PR12H registers are combined to form 16-bit registers PR00, PR01, PR02, PR10, PR11, and PR12, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 16-4. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H) (64-pin) (1/2)

Address: FFFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00L	PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10L	PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	SREPR00 TMPR001H	SRPR00 CSIPR001 IICPR001	STPR00 CSIPR000 IICPR000	DMAPR01	DMAPR00	SREPR02 TMPR011H	SRPR02 CSIPR021 IICPR021	STPR02 CSIPR020 IICPR020

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	SREPR10 TMPR101H	SRPR10 CSIPR101 IICPR101	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12 TMPR111H	SRPR12 CSIPR121 IICPR121	STPR12 CSIPR120 IICPR120

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	IICAPR00	SREPR01 TMPR003H	SRPR01 CSIPR011 IICPR011	STPR01 CSIPR010 IICPR010

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	IICAPR10	SREPR11 TMPR103H	SRPR11 CSIPR111 IICPR111	STPR11 CSIPR110 IICPR110

Figure 16-4. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H) (64-pin) (2/2)

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	<1>	<0>
PR01H	TMPR004	1	1	1	KRPR0	ITPR0	RTCPR0	ADPR0

Address: FFFE7FH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	<1>	<0>
PR11H	TMPR104	1	1	1	KRPR1	ITPR1	RTCPR1	ADPR1

Address: FFFD8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR02L	PPR010	PPR09	PPR08	PPR07	PPR06	TMPR007	TMPR006	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR12L	PPR110	PPR19	PPR18	PPR17	PPR16	TMPR107	TMPR106	TMPR105

Address: FFFD9H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	<0>
PR02H	FLPR0	1	MDPR0	1	1	1	1	PPR011

Address: FFFDDH After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	<0>
PR12H	FLPR1	1	MDPR1	1	1	1	1	PPR111

XXPR1X	XXPR0X	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Caution The above is the bit layout for the 64-pin. The available bits differ depending on the product. For details about the bits available for each product, see Table 16-2. Be sure to set bits that are not available to 1.

16.3.4 External interrupt rising edge enable registers (EGP0, EGP1), external interrupt falling edge enable registers (EGN0, EGN1)

These registers specify the valid edge for INTP0 to INTP11.

The EGP0, EGP1, EGN0, and EGN1 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 16-5. Format of External Interrupt Rising Edge Enable Registers (EGP0, EGP1) and External Interrupt Falling Edge Enable Registers (EGN0, EGN1) (64-pin)

Address: FFF38H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP0	EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FFF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN0	EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

Address: FFF3AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP1	0	0	0	0	EGP11	EGP10	EGP9	EGP8

Address: FFF3BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN1	0	0	0	0	EGN11	EGN10	EGN9	EGN8

EGPn	EGNn	INTPn pin valid edge selection (n = 0 to 11)
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Table 16-3 shows the ports corresponding to the EGPn and EGNn bits.

Table 16-3. Interrupt Request Signal Corresponding to EGPn and EGNn bits

Detection Enable Bit		Edge Detection Port	Interrupt Request Signal	64-pin	48-pin	32-pin	25-pin
EGP0	EGN0	P137	INTP0	√	√	√	√
EGP1	EGN1	P50	INTP1	√	√	√	√
EGP2	EGN2	P51	INTP2	√	√	√	√
EGP3	EGN3	P30	INTP3	√	√	√	√
EGP4	EGN4	P31	INTP4	√	√	√	√
EGP5	EGN5	P16	INTP5	√	√	–	–
EGP6	EGN6	P140	INTP6	√	√	–	–
EGP7	EGN7	P141	INTP7	√	–	–	–
EGP8	EGN8	P74	INTP8	√	√	–	–
EGP9	EGN9	P75	INTP9	√	√	–	–
EGP10	EGN10	P76	INTP10	√	–	–	–
EGP11	EGN11	P77	INTP11	√	–	–	–

Caution Select the port mode by clearing the EGPn and EGNn bits to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0 to 11

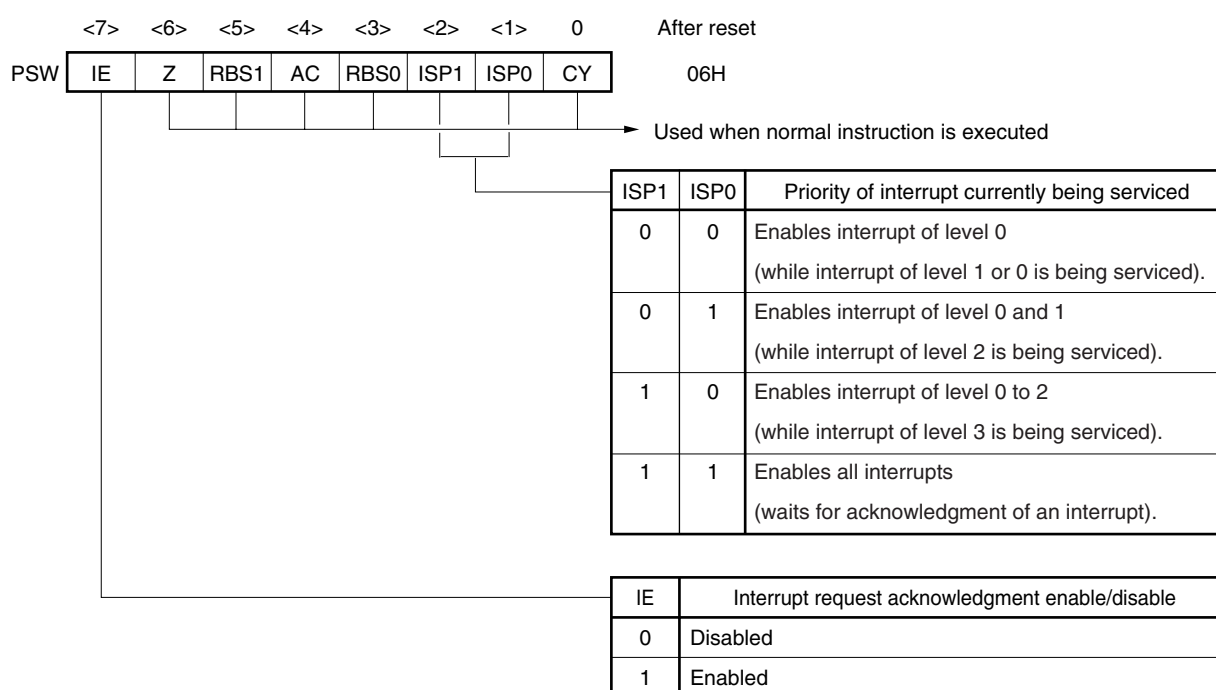
16.3.5 Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for an interrupt request. The IE flag that sets maskable interrupt enable/disable and the ISP0 and ISP1 flags that controls multiple interrupt servicing are mapped to the PSW.

Besides 8-bit read/write, this register can carry out operations using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged, if the BRK instruction is executed, the contents of the PSW are automatically saved into a stack and the IE flag is reset to 0. If a maskable interrupt request is acknowledged, the contents of the priority specification flag of the acknowledged interrupt are transferred to the ISP0 and ISP1 flags. The PSW contents are also saved into the stack with the PUSH PSW instruction. They are restored from the stack with the RETI, RETB, and POP PSW instructions.

Reset signal generation sets PSW to 06H.

Figure 16-6. Configuration of Program Status Word



16.4 Interrupt Servicing Operations

16.4.1 Maskable interrupt request acknowledgment

A maskable interrupt request becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request.

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 16-4 below.

For the interrupt request acknowledgment timing, see **Figures 16-8 and 16-9**.

Table 16-4. Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time ^{Note}
Servicing time	9 clocks	16 clocks

<R>

<R>

Note Maximum time does not apply when an instruction from the internal RAM area is executed.

Remark 1 clock: $1/f_{CLK}$ (f_{CLK} : CPU clock)

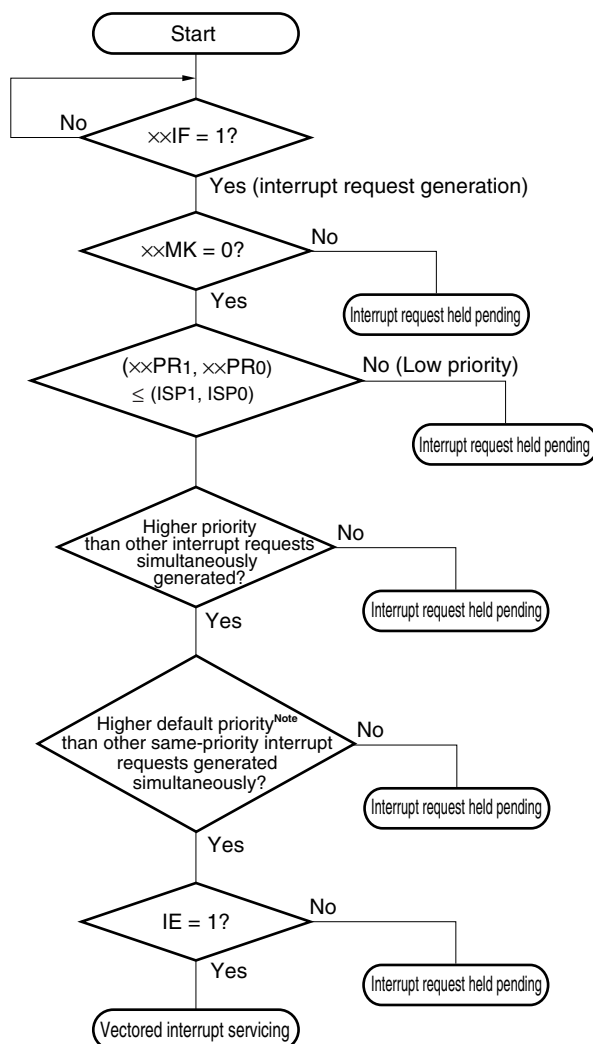
If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

Figure 16-7 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP1 and ISP0 flags. The vector table data determined for each interrupt request is loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

Figure 16-7. Interrupt Request Acknowledgment Processing Algorithm

xxIF: Interrupt request flag

xxMK: Interrupt mask flag

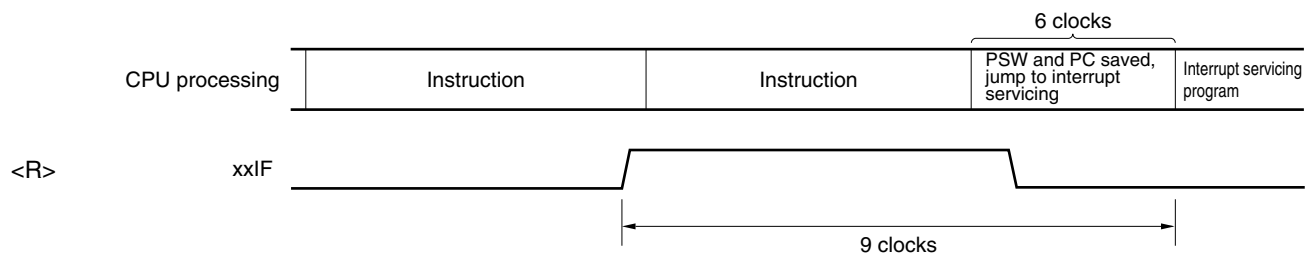
xxPR0: Priority specification flag 0

xxPR1: Priority specification flag 1

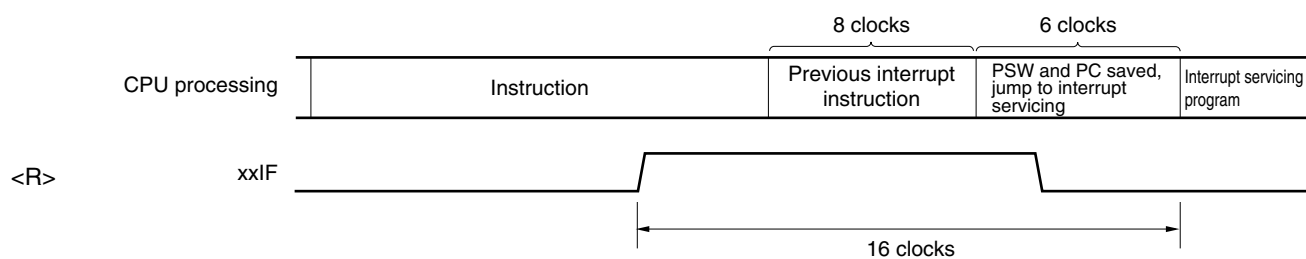
IE: Flag that controls acknowledgment of maskable interrupt request (1 = Enable, 0 = Disable)

ISP0, ISP1: Flag that indicates the priority level of the interrupt currently being serviced (see **Figure 16-6**)

Note For the default priority, refer to **Table 16-1 Interrupt Source List**.

Figure 16-8. Interrupt Request Acknowledgment Timing (Minimum Time)

Remark 1 clock: $1/f_{CLK}$ (f_{CLK} : CPU clock)

Figure 16-9. Interrupt Request Acknowledgment Timing (Maximum Time)

Remark 1 clock: $1/f_{CLK}$ (f_{CLK} : CPU clock)

16.4.2 Software interrupt request acknowledgment

A software interrupt request is acknowledged by BRK instruction execution. Software interrupts cannot be disabled.

If a software interrupt request is acknowledged, the contents are saved into the stacks in the order of the program status word (PSW), then program counter (PC), the IE flag is reset (0), and the contents of the vector table (0007EH, 0007FH) are loaded into the PC and branched.

Restoring from a software interrupt is possible by using the RETB instruction.

Caution Can not use the RETI instruction for restoring from the software interrupt.

16.4.3 Multiple interrupt servicing

Multiple interrupt servicing occurs when another interrupt request is acknowledged during execution of an interrupt.

Multiple interrupt servicing does not occur unless the interrupt request acknowledgment enabled state is selected (IE = 1). When an interrupt request is acknowledged, interrupt request acknowledgment becomes disabled (IE = 0). Therefore, to enable multiple interrupt servicing, it is necessary to set (1) the IE flag with the EI instruction during interrupt servicing to enable interrupt acknowledgment.

Moreover, even if interrupts are enabled, multiple interrupt servicing may not be enabled, this being subject to interrupt priority control. Two types of priority control are available: default priority control and programmable priority control. Programmable priority control is used for multiple interrupt servicing.

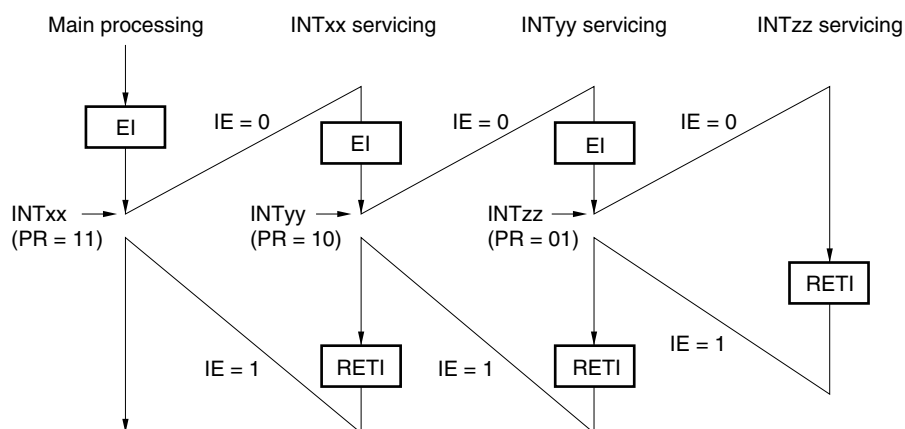
In the interrupt enabled state, if an interrupt request with a priority equal to or higher than that of the interrupt currently being serviced is generated, it is acknowledged for multiple interrupt servicing. If an interrupt with a priority lower than that of the interrupt currently being serviced is generated during interrupt servicing, it is not acknowledged for multiple interrupt servicing. Interrupt requests that are not enabled because interrupts are in the interrupt disabled state or because they have a lower priority are held pending. When servicing of the current interrupt ends, the pending interrupt request is acknowledged following execution of at least one main processing instruction execution.

Table 16-5 shows relationship between interrupt requests enabled for multiple interrupt servicing and Figure 16-10 shows multiple interrupt servicing examples.

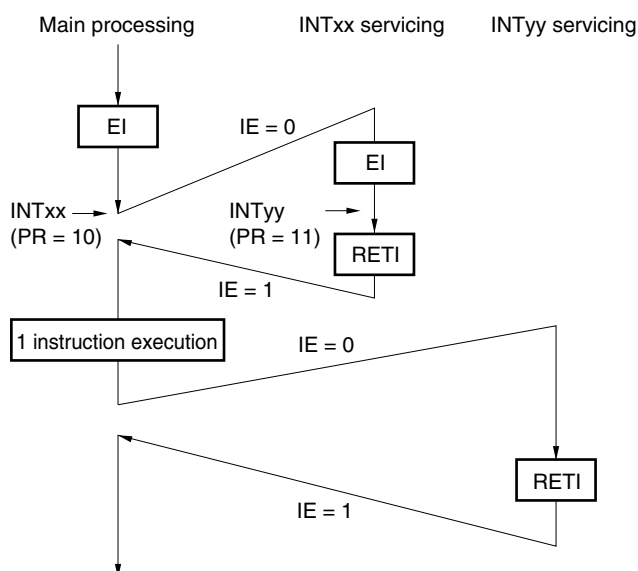
<R> **Table 16-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing**

Multiple Interrupt Request Interrupt Being Serviced		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0 ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0 ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1 ISP0 = 0	○	×	○	×	○	×	×	×	○
Software interrupt		○	×	○	×	○	×	○	×	○

- Remarks**
- : Multiple interrupt servicing enabled
 - ×: Multiple interrupt servicing disabled
 - ISP0, ISP1, and IE are flags contained in the PSW.
 ISP1 = 0, ISP0 = 0: An interrupt of level 1 or level 0 is being serviced.
 ISP1 = 0, ISP0 = 1: An interrupt of level 2 is being serviced.
 ISP1 = 1, ISP0 = 0: An interrupt of level 3 is being serviced.
 ISP1 = 1, ISP0 = 1: Wait for An interrupt acknowledgment.
 IE = 0: Interrupt request acknowledgment is disabled.
 IE = 1: Interrupt request acknowledgment is enabled.
 - PR is a flag contained in the PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, and PR12H registers.
 PR = 00: Specify level 0 with $\times\times\text{PR}1\times = 0$, $\times\times\text{PR}0\times = 0$ (higher priority level)
 PR = 01: Specify level 1 with $\times\times\text{PR}1\times = 0$, $\times\times\text{PR}0\times = 1$
 PR = 10: Specify level 2 with $\times\times\text{PR}1\times = 1$, $\times\times\text{PR}0\times = 0$
 PR = 11: Specify level 3 with $\times\times\text{PR}1\times = 1$, $\times\times\text{PR}0\times = 1$ (lower priority level)

Figure 16-10. Examples of Multiple Interrupt Servicing (1/2)**Example 1. Multiple interrupt servicing occurs twice**

During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

Example 2. Multiple interrupt servicing does not occur due to priority control

Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with $\times\times PR1\times = 0$, $\times\times PR0\times = 0$ (higher priority level)

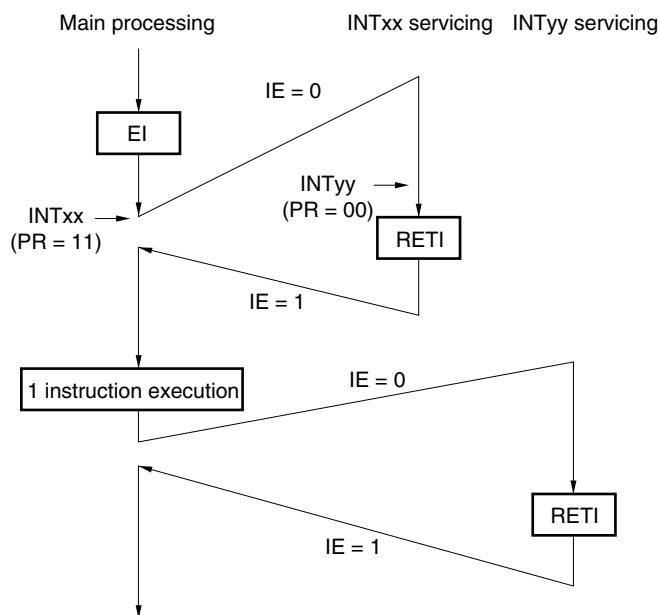
PR = 01: Specify level 1 with $\times\times PR1\times = 0$, $\times\times PR0\times = 1$

PR = 10: Specify level 2 with $\times\times PR1\times = 1$, $\times\times PR0\times = 0$

PR = 11: Specify level 3 with $\times\times PR1\times = 1$, $\times\times PR0\times = 1$ (lower priority level)

IE = 0: Interrupt request acknowledgment is disabled

IE = 1: Interrupt request acknowledgment is enabled.

Figure 16-10. Examples of Multiple Interrupt Servicing (2/2)**Example 3. Multiple interrupt servicing does not occur because interrupts are not enabled**

Interrupts are not enabled during servicing of interrupt INTxx (EI instruction is not issued), therefore, interrupt request INTyy is not acknowledged and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with $\times\times PR1\times = 0$, $\times\times PR0\times = 0$ (higher priority level)

PR = 01: Specify level 1 with $\times\times PR1\times = 0$, $\times\times PR0\times = 1$

PR = 10: Specify level 2 with $\times\times PR1\times = 1$, $\times\times PR0\times = 0$

PR = 11: Specify level 3 with $\times\times PR1\times = 1$, $\times\times PR0\times = 1$ (lower priority level)

IE = 0: Interrupt request acknowledgment is disabled

IE = 1: Interrupt request acknowledgment is enabled.

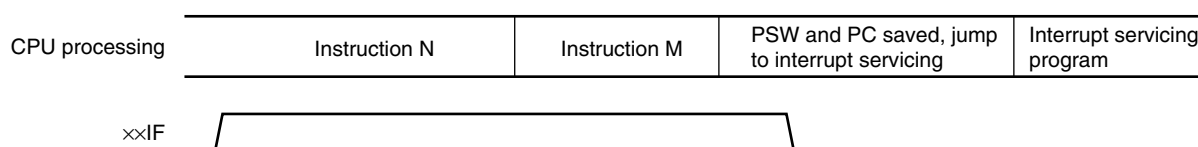
<R> 16.4.4 Interrupt request hold

There are instructions where, even if an interrupt request is issued while the instructions are being executed, interrupt request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV PSW, A
- MOV1 PSW. bit, CY
- SET1 PSW. bit
- CLR1 PSW. bit
- RETB
- RETI
- POP PSW
- BTCLR PSW. bit, \$addr20
- EI
- DI
- SKC
- SKNC
- SKZ
- SKNZ
- SKH
- SKNH
- Manipulation instructions for the IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, and PR12H registers

Figure 16-11 shows the timing at which interrupt requests are held pending.

Figure 16-11. Interrupt Request Hold



- Remarks**
1. Instruction N: Interrupt request hold instruction
 2. Instruction M: Instruction other than interrupt request hold instruction

<R>

CHAPTER 17 KEY INTERRUPT FUNCTION

The number of key interrupt input channels differs, depending on the product.

	25-pin	32-pin	48-pin	64-pin
Key interrupt input channels	0 (4) ch	1 (6) ch	6 ch	10 ch

Remarks 1. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2. Most of the following descriptions in this chapter use the 64-pin products

17.1 Functions of Key Interrupt

A key interrupt (INTKR) can be generated by inputting a rising/falling edge to the key interrupt input pins (KR0 to KR9). There are two ways to identify the channel(s) to which a valid edge has been input:

- Identify the channel(s) (KR0 to KR9) by using the port input level.
- Identify the channel(s) (KR0 to KR9) by using the key interrupt flag.

Table 17-1. Assignment of Key Interrupt Detection Pins

Key Interrupt Pins	Key return mode registers (KRM0, KRM1)	Key return flag register (KRF)
KR0	KRM00	KRF0
KR1	KRM01	KRF1
KR2	KRM02	KRF2
KR3	KRM03	KRF3
KR4	KRM04	KRF4
KR5	KRM05	KRF5
KR6	KRM06	—
KR7	KRM07	—
KR8	KRM08	—
KR9	KRM09	—

Remark (KR0 to KR3): 25-pin products
 KR0 (KR0 to KR5): 32-pin products
 KR0 to KR5: 48-pin products
 KR0 to KR9: 64-pin products

Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

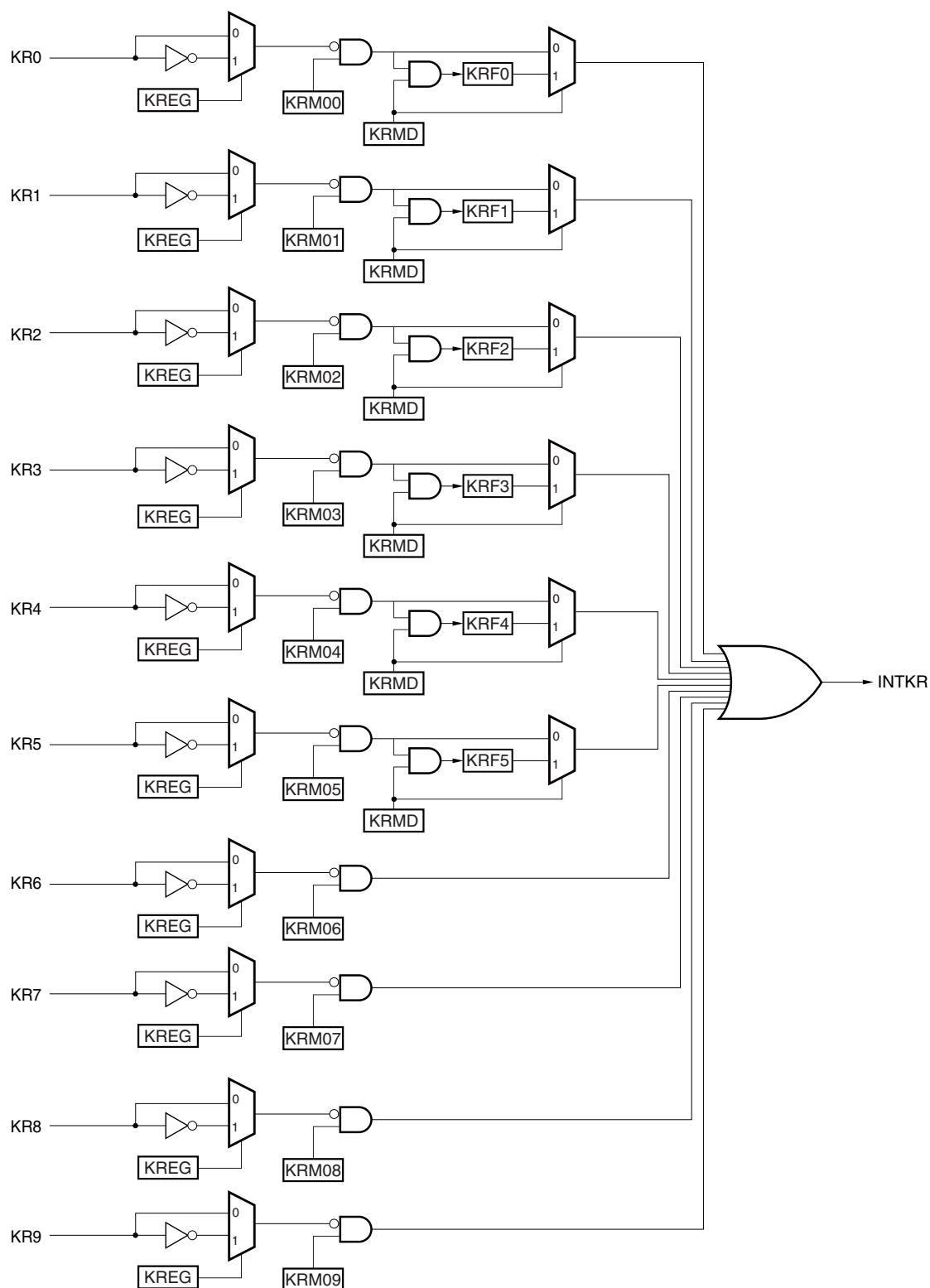
17.2 Configuration of Key Interrupt

The key interrupt includes the following hardware.

Table 17-2. Configuration of Key Interrupt

Item	Configuration
Control register	Key return control register (KRCTL) Key return mode registers 0, 1 (KRM0, KRM1) Key return flag register (KRF) Port mode registers 0 to 2, 7, 12, 15 (PM0 to PM2, PM7, PM12, PM15) Peripheral I/O redirection register (PIOR)

Figure 17-1. Block Diagram of Key Interrupt



Remark (KR0 to KR3): 25-pin products
 KR0 (KR0 to KR5): 32-pin products
 KR0 to KR5: 48-pin products
 KR0 to KR9: 64-pin products

Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

17.3 Register Controlling Key Interrupt

The key interrupt function is controlled by the following five registers:

- Key return control register (KRCTL)
- Key return mode registers (KRM0, KRM1)
- Key return flag register (KRF)
- Port mode registers 0 to 2, 7, 12, and (PM0 to PM2, PM7, PM12, PM15)
- Peripheral I/O redirection register (PIOR)

17.3.1 Key return control register (KRCTL)

This register controls the usage of the key interrupt flags (KRF0 to KRF5) and sets the detection edge.

The KRCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17-2. Format of Key Return Control Register (KRCTL)

Address: FFF34H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRCTL	KRMD	0	0	0	0	0	0	KREG

KRMD	Usage of t key interrupt flags (KRF0 to KRF5)
0	Does not use key interrupt flags
1	Uses key interrupt flags

KRMD	Selection of Detection Edge (KR0 to KR9)
0	Falling edge
1	Rising edge

17.3.2 Key return mode registers (KRM0, KRM1)

These registers set the key interrupt mode.

The KRM0 and KRM1 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 17-3. Format of Key Return Mode Registers (KRM0, KRM1)

Address: FFF37H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM0	KRM07	KRM06	KRM05	KRM04	KRM03	KRM02	KRM01	KRM00

Address: FFF36H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM1	0	0	0	0	0	0	KRM09	KRM08

KRM0n	Key interrupt mode control
0	Does not detect key interrupt signal
1	Detects key interrupt signal

- Cautions**
1. The internal pull-up resistor can be used by setting the corresponding bits to 1 in the pull-up resistor registers 0, 1, 7, and 12 (PU0, PU1, PU7, PU12) of key interrupt input pins.
 2. An interrupt will be generated if the target bit of the KRM0, KRM1 registers are set while a low level (when KREG = 0)/high level (when KREG = 1) is being input to the key interrupt input pin. To ignore this interrupt, set the KRM0, KRM1 registers after disabling interrupt servicing by using the interrupt mask flag. Afterward, clear the interrupt request flag and enable interrupt servicing after waiting for the key interrupt input high-level width/low-level width (see 29.4.1 Basic operation, 30.4.1 Basic operation).
 3. The pins not used in the key interrupt mode can be used as normal ports.

- Remarks**
1. n = 0 to 9
 2. (KR0 to KR3): 25-pin products
 KR0 (KR0 to KR5): 32-pin products
 KR0 to KR5: 48-pin products
 KR0 to KR9: 64-pin products
 Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

17.3.3 Key return flag register (KRF)

This register controls the key interrupt flags (KRF0 to KRF5).

The KRF register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17-4. Format of Key return Flag Register (KRF)

Address: FFF35H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRF	0	0	KRF5	KRF4	KRF3	KRF2	KRF1	KRF0

KRFn	Key interrupt flag
0	No key interrupt signal has been detected.
1	A key interrupt signal has been detected.

Note Writing to 1 is invalid. To clear KRFn, write “0” to the target bits and write “1” to other bits, with the 8-bit memory manipulation instruction.

Cautions 1. When KRMD = 0, prohibition of set to KRFn = 1.

2. For KR6 to KR9, identify channels by sequentially verifying the input levels.

Remark n = 0 to 5

17.3.4 Port mode registers 0 to 2, 7, 12, 15 (PM0 to PM2, PM7, PM12, PM15)

These registers set the input and output of Port0 to 2, 7, 12, 15 in 1-bit units.

Set 1 to the bit corresponding to each P70/KR0 to P77/KR7, P05/KR8, P06/KR9, P00/(KR0) to P04/(KR4), P22/(KR5) to P26/(KR9), port of P10/(KR0) to P15/(KR5), P120/(KR0), P151/(KR6) to P154/(KR9) as a key input.

In addition, set 1 to the bits corresponding with port registers 0 to 2, 7, 15 (P0 to P2, P7, P15).

The PM0 to PM2, PM7, PM12, PM15 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to FFH.

Remark Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR)

Figure 17-5. Format of Port Mode Register (PM0 to PM2, PM7, PM12, PM15)

Address: FFF20H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

Address: FFF21H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF22H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

Address: FFF27H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70

Address: FFF2CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PM12	1	1	1	1	1	1	1	PM120

Address: FFF2FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150

PM0n	I/O mode selection for Pmn/KRm pin (n = 0 to 9, m = 0 to 2, 7, 12, 15)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

17.3.5 Peripheral I/O redirection register (PIOR)

This register is used to specify whether to enable or disable the peripheral I/O redirect function.

This function is used to switch ports to which alternate functions are assigned.

Use the PIOR register to assign a port to the function to redirect and enable the function.

In addition, can be changed the settings for redirection until its function enable operation. The PIOR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 17-6. Format of Peripheral I/O Redirection Register (PIOR)

Address: F0077H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR	0	0	0	0	0	0	PIOR1	PIOR0

Function	64-pin				48-pin				32-pin				25-pin			
	Setting value of PIOR1, PIOR0				Setting value of PIOR1, PIOR0				Setting value of PIOR1, PIOR0				Setting value of PIOR1, PIOR0			
	0, 0	0, 1	1, 0	1, 1	0, 0	0, 1	1, 0	1, 1	0, 0	0, 1	1, 0	1, 1	0, 0	0, 1	1, 0	1, 1
KR0	P70	Setting prohibited	P00	P10	P70	Setting prohibited	P02	P10	P70	Setting prohibited	P120	P10	—	Setting prohibited	P02	Setting prohibited
KR1	P71		P01	P11	P71		P03	P11	—		P02	P11	—		P03	
KR2	P72		P02	P12	P72		P22	P12	—		P03	P12	—		P22	
KR3	P73		P03	P13	P73		P23	P13	—		P22	P13	—		P23	
KR4	P74		P04	P14	P74		P24	P14	—		P23	P14	—		—	
KR5	P75		P22	P15	P75		P25	P15	—		P24	P15	—		—	
KR6	P76		P23	P151	—		—	—	—		—	—	—		—	
KR7	P77		P24	P152	—		—	—	—		—	—	—		—	
KR8	P05		P25	P153	—		—	—	—		—	—	—		—	
KR9	P06		P26	P154	—		—	—	—		—	—	—		—	

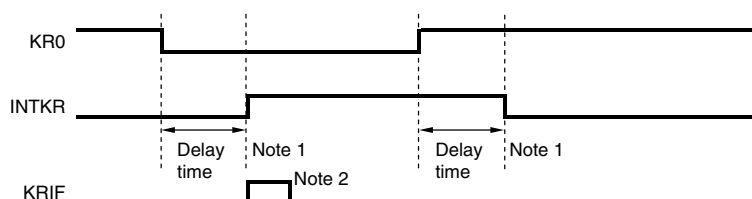
17.4 Key Interrupt Operation

17.4.1 When not using the key interrupt flag (KRMD = 0)

A key interrupt (INTKR) is generated when the valid edge specified by the setting of the KREG bit is input to a key interrupt pin (KR0 to KR9). The channel to which the valid edge was input can be identified by reading the port register and checking the port level after the key interrupt (INTKR) is generated.

The INTKR signal changes according to the input level of the key interrupt input pin (KR0 to KR9).

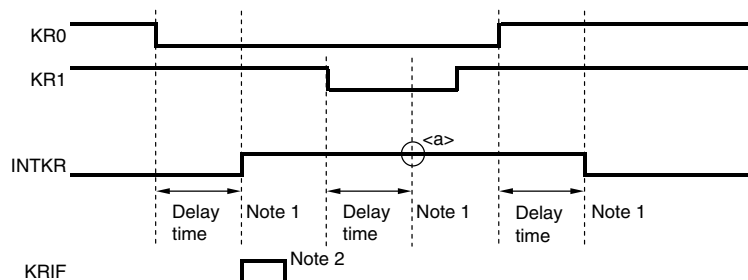
Figure 17-7. Operation of INTKR Signal When a Key Interrupt is Input to a Single Channel
(When KRMD = 0 and KREG = 0)



- Notes 1.** The maximum delay time is the maximum value of the high-level width and low-level width of the key interrupt input (see **29.4.1 Basic operation** and **30.4.1 Basic operation for details**).
- 2.** Acknowledgment of vectored interrupt request or bit cleared by software

The operation when a valid edge is input to multiple key interrupt input pins is shown in Figure 17-8 below. The INTKR signal is set while a low level is being input to one pin (when KREG is set to 0). Therefore, even if a falling edge is input to another pin in this period, a key interrupt (INTKR) will not be generated again (<1> in the figure).

Figure 17-8. Operation of INTKR Signal When Key Interrupts Are Input to Multiple Channels
(When KRMD = 0 and KREG = 0)



- Notes 1.** The maximum delay time is the maximum value of the high-level width and low-level width of the key interrupt input (see **29.4.1 Basic operation** and **30.4.1 Basic operation for details**).
- 2.** Acknowledgment of vectored interrupt request or bit cleared by software

17.4.2 When using the key interrupt flag (KRMD = 1)

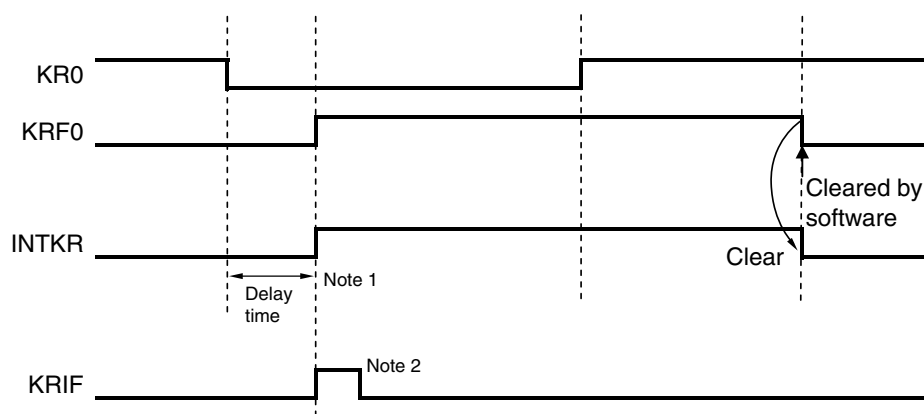
A key interrupt (INTKR) is generated when the valid edge specified by the setting of the KREG bit is input to a key interrupt pin (KR0 to KR5). The channels to which the valid edge was input can be identified by reading the key return flag register (KRF) after the key interrupt (INTKR) is generated.

If the KRMD bit is set to 1, the INTKR signal is cleared by clearing the corresponding bit in the KRF register.

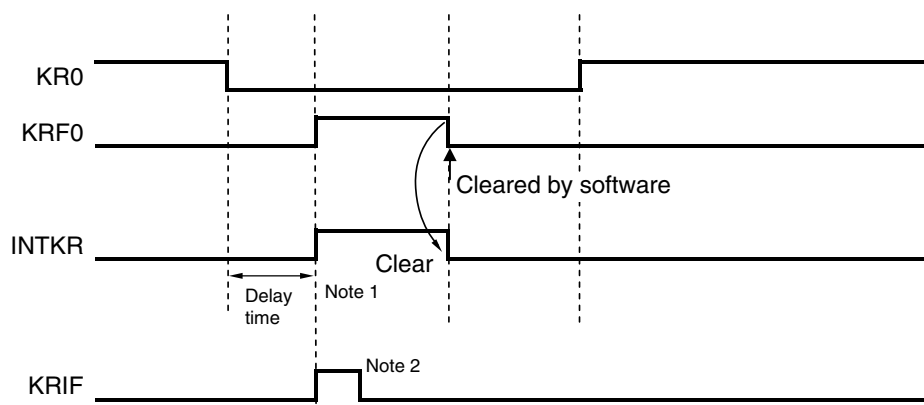
As shown in Figure 17-9, only one interrupt is generated each time a falling edge is input to one channel (when KREG = 0), regardless of whether the KRFn bit is cleared before or after a rising edge is input.

**Figure 17-9. Basic Operation of the INTKR Signal When the Key Interrupt Flag Is Used
(When KRMD = 1 and KREG = 0)**

(a) When KRF0 is cleared after a rising edge is input to the KR0 pin



(b) When KRF0 is cleared before a rising edge is input to the KR0 pin

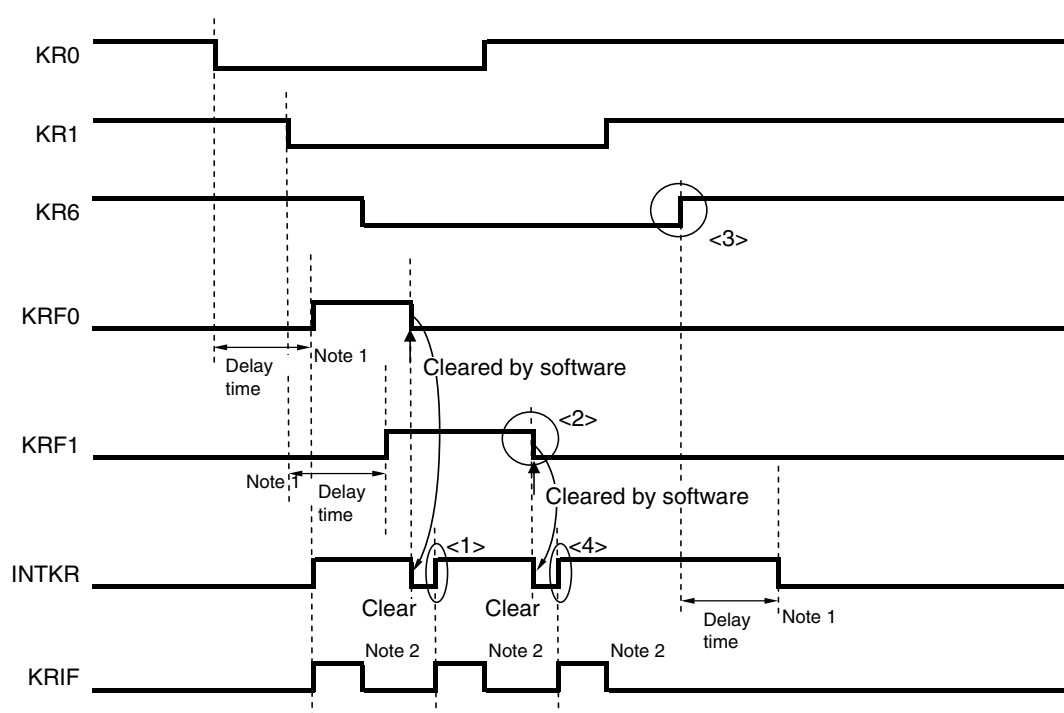


Notes 1. The maximum delay time is the maximum value of the high-level width and low-level width of the key interrupt input (see **29.4.1 Basic operation** and **30.4.1 Basic operation for details**).

2. Acknowledgment of vectored interrupt request or bit cleared by software

The operation when a valid edge is input to multiple key interrupt input pins is shown in Figure 17-10 below. A falling edge is also input to the KR1 and KR6 pins after a falling edge was input to the KR0 pin (when KREG = 0). The KRF1 bit is set when the KRF0 bit is cleared. A key interrupt (INTKR) is therefore generated one clock (fCLK) after the KRF0 bit is cleared (<1> in the figure). Also, after a falling edge has been input to the KR6 pin, a low level continues to be input to this pin (<3> in the figure) until the KRF1 bit is cleared (<2> in the figure). A key interrupt (INTKR) is therefore generated one clock (fCLK) after the KRF1 bit is cleared (<4> in the figure). It is thus possible to generate a key interrupt (INTKR) when a valid edge is input to multiple channels.

Figure 17-10. Operation of INTKR Signal When Key Interrupts Are Input to Multiple Channels
(When KRMD = 1 and KREG = 0)

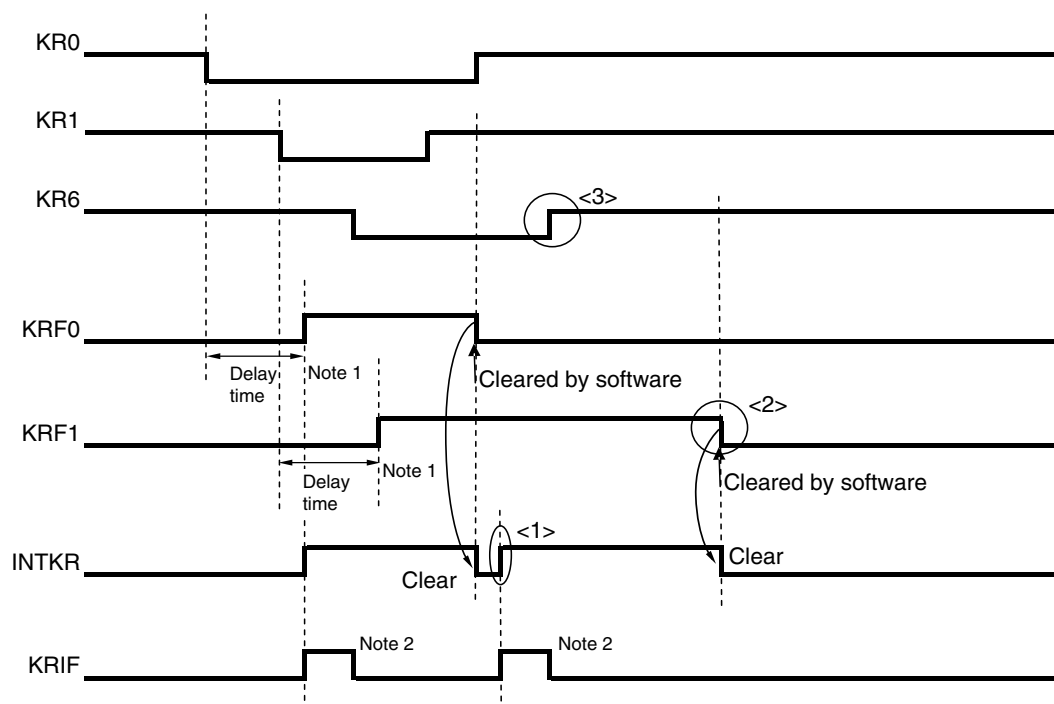


- Notes 1.** The maximum delay time is the maximum value of the high-level width and low-level width of the key interrupt input (see **29.4.1 Basic operation** and **30.4.1 Basic operation for details**).
- 2.** Acknowledgment of vectored interrupt request or bit cleared by software

Remark fCLK: CPU/peripheral hardware clock frequency

The operation when a valid edge is input to the KR6 to KR9 pins without generating a key interrupt (INTKR) is shown in Figure 17-11 below. A falling edge is also input to the KR1 and KR6 pins after a falling edge was input to the KR0 pin (when KREG = 0). The KR1 pin becomes high level when the KRF0 bit is cleared, but because the KRF1 bit is set, a key interrupt (INTKR) is generated one clock (fCLK) after the KRF0 bit is cleared (<1> in the figure). Also, because the KR6 pin was high level (<3> in the figure) before the KRF1 bit was cleared (<2> in the figure) a key interrupt (INTKR) is not generated for the KR6 pin.

**Figure 17-11. Operation When an INTKR Signal Is Not Generated upon Input of a Valid Edge to KR6 to KR9
(When KRMD = 1 and KREG = 0)**



- Notes 1.** The maximum delay time is the maximum value of the high-level width and low-level width of the key interrupt input (see **29.4.1 Basic operation** and **30.4.1 Basic operation for details**).
- 2.** Acknowledgment of vectored interrupt request or bit cleared by software

Remark fCLK: CPU/peripheral hardware clock frequency

CHAPTER 18 STANDBY FUNCTION

18.1 Standby function

The standby function reduces the operating current of the system, and the following three modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, high-speed on-chip oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and high-speed on-chip oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

(3) SNOOZE mode

In the case of CSIp or UARTq data reception and an A/D conversion request by the timer trigger signal (the interrupt request signal (INTRTC/INTIT)), the STOP mode is exited, the CSIp or UARTq data is received without operating the CPU, and A/D conversion is performed. This can only be specified when the high-speed on-chip oscillator is selected for the CPU/peripheral hardware clock (f_{CLK}).

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

- Cautions**
1. The STOP mode can be used only when the CPU is operating on the main system clock. The STOP mode cannot be set while the CPU operates with the subsystem clock. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.
 2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction (except SNOOZE mode setting unit).
 3. When using CSIp, UARTq, or the A/D converter in the SNOOZE mode, set up serial standby control register m (SSCm) and A/D converter mode register 2 (ADM2) before switching to the STOP mode. For details, see 12.3 Registers Controlling Serial Array Unit and 11.3 Registers Used in A/D Converter.
 4. The following sequence is recommended for power consumption reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of A/D converter mode register 0 (ADM0) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.
 5. It can be selected by the option byte whether the low-speed on-chip oscillator continues oscillating or stops in the HALT or STOP mode. For details, see CHAPTER 24 OPTION BYTE.

Remark p = 00; q = 0; m = 0

18.2 Registers controlling standby function

The standby function is controlled by the following two registers.

- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

Remark For the registers that start, stop, or select the clock, see **CHAPTER 5 CLOCK GENERATOR**.

18.2.1 Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter.

The X1 clock oscillation stabilization time can be checked in the following case.

- If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating.

The OSTC register can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POR, LVD, WDT, and executing an illegal instruction), the STOP instruction and MSTOP bit (bit 7 of clock operation status control register (CSC)) = 1 clear this register to 00H.

Figure 18-1. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFFA2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18

MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18	Oscillation stabilization time status		
									$f_x = 10 \text{ MHz}$	$f_x = 20 \text{ MHz}$
0	0	0	0	0	0	0	0	$2^8/f_x \text{ max.}$	25.6 μs max.	12.8 μs max.
1	0	0	0	0	0	0	0	$2^8/f_x \text{ min.}$	25.6 μs min.	12.8 μs min.
1	1	0	0	0	0	0	0	$2^9/f_x \text{ min.}$	51.2 μs min.	25.6 μs min.
1	1	1	0	0	0	0	0	$2^{10}/f_x \text{ min.}$	102.4 μs min.	51.2 μs min.
1	1	1	1	0	0	0	0	$2^{11}/f_x \text{ min.}$	204.8 μs min.	102.4 μs min.
1	1	1	1	1	0	0	0	$2^{13}/f_x \text{ min.}$	819.2 μs min.	409.6 μs min.
1	1	1	1	1	1	0	0	$2^{15}/f_x \text{ min.}$	3.27 ms min.	1.64 ms min.
1	1	1	1	1	1	1	0	$2^{17}/f_x \text{ min.}$	13.11 ms min.	6.55 ms min.
1	1	1	1	1	1	1	1	$2^{18}/f_x \text{ min.}$	26.21 ms min.	13.11 ms min.

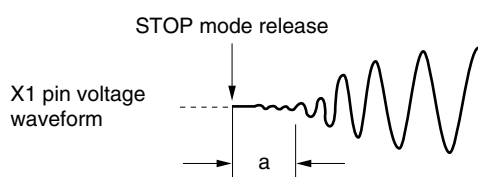
Cautions 1. After the above time has elapsed, the bits are set to 1 in order from the MOST8 bit and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the oscillation stabilization time select register (OSTS). If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- Desired OSTC register oscillation stabilization time $\leq$ Oscillation stabilization time set by OSTS register

Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after STOP mode is released.

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_x : X1 clock oscillation frequency

18.2.2 Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using the OSTS register after the STOP mode is released.

When the high-speed on-chip oscillator clock is selected as the CPU clock, confirm with the oscillation stabilization time counter status register (OSTC) that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using the OSTC register.

The OSTS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 07H.

Figure 18-2. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFFA3H After reset: 07H R/W

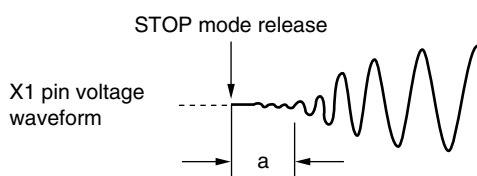
Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0		Oscillation stabilization time selection	
				$f_x = 10 \text{ MHz}$	$f_x = 20 \text{ MHz}$
0	0	0	$2^8/f_x$	25.6 μs	12.8 μs
0	0	1	$2^9/f_x$	51.2 μs	25.6 μs
0	1	0	$2^{10}/f_x$	102.4 μs	51.2 μs
0	1	1	$2^{11}/f_x$	204.8 μs	102.4 μs
1	0	0	$2^{13}/f_x$	819.2 μs	409.6 μs
1	0	1	$2^{15}/f_x$	3.27 ms	1.64 ms
1	1	0	$2^{17}/f_x$	13.11 ms	6.55 ms
1	1	1	$2^{18}/f_x$	26.21 ms	13.11 ms

- Cautions**
1. To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.
 2. Before changing the setting of the OSTS register, confirm that the count operation of the OSTC register is completed.
 3. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.
 4. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the OSTS register. If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock, set the oscillation stabilization time as follows.
 - Desired OSTC register oscillation stabilization time $\leq$ Oscillation stabilization time set by OSTS register

Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after STOP mode is released.

5. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_x : X1 clock oscillation frequency

18.3 Standby Function Operation

18.3.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock, high-speed on-chip oscillator clock, or subsystem clock.

The operating statuses in the HALT mode are shown below.

Table 18-1. Operating Statuses in HALT Mode (1/2)

HALT Mode Setting		When HALT Instruction Is Executed While CPU Is Operating on Main System Clock				
		When CPU Is Operating on High-speed On-chip Oscillator Clock (f _{IH})	When CPU Is Operating on X1 Clock (f _x)	When CPU Is Operating on External Main System Clock (f _{EX})		
Item						
System clock		Clock supply to the CPU is stopped				
Main system clock	f _{IH}	Operation continues (cannot be stopped)	Operation disabled			
	f _x	Operation disabled	Operation continues (cannot be stopped)	Cannot operate		
	f _{EX}		Cannot operate	Operation continues (cannot be stopped)		
Subsystem clock	f _{XT}	Status before HALT mode was set is retained				
	f _{EXS}					
f _{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops				
CPU		Operation stopped				
Code flash memory						
Data flash memory						
RAM						
Port (latch)		Status before HALT mode was set is retained				
Timer array unit		Operable				
Real-time clock (RTC)						
12-bit interval timer						
Watchdog timer		See CHAPTER 10 WATCHDOG TIMER				
Clock output/buzzer output		Operable				
A/D converter						
Serial array unit (SAU)						
Serial interface (IICA)						
Multiplier and divider/multiply-accumulator						
DMA controller						
Power-on-reset function						
Voltage detection function						
External interrupt						
Key interrupt function						
CRC operation function	High-speed CRC					
	General-purpose CRC				Operation stopped	
RAM parity error detection function					Operation stopped	
RAM guard function						
SFR guard function						
Illegal-memory access detection function						

Remark Operation stopped: Operation is automatically stopped before switching to the HALT mode.

Operation disabled: Operation is stopped before switching to the HALT mode.

f_{IH} : High-speed on-chip oscillator clock f_{EX} : External main system clock

f_{IL} : Low-speed on-chip oscillator clock f_{XT} : XT1 clock

f_x : X1 clock f_{EXS} : External subsystem clock

Table 18-1. Operating Statuses in HALT Mode (2/2)

HALT Mode Setting Item		When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock		
		When CPU Is Operating on XT1 Clock (f _{XT})	When CPU Is Operating on External Subsystem Clock (f _{EXS})	
System clock		Clock supply to the CPU is stopped		
Main system clock	f _{IH}	Operation disabled		
	f _X			
	f _{EX}			
	Subsystem clock	f _{XT}	Operation continues (cannot be stopped)	Cannot operate
		f _{EXS}	Cannot operate	Operation continues (cannot be stopped)
f _{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops		
CPU		Operation stopped		
Code flash memory				
Data flash memory				
RAM				
Port (latch)		Status before HALT mode was set is retained		
Timer array unit		Operable (Operation is disabled when the RTCLPC bit of the operation speed mode control (OSMC) register is 1)		
Real-time clock (RTC)		Operable		
12-bit interval timer				
Watchdog timer		See CHAPTER 10 WATCHDOG TIMER		
Clock output/buzzer output		Operable (Operation is disabled when the RTCLPC bit of the operation speed mode control (OSMC) register is 1)		
A/D converter		Operation disabled		
Serial array unit (SAU)		Operable (Operation is disabled when the RTCLPC bit of the operation speed mode control (OSMC) register is 1)		
Serial interface (IICA)		Operation disabled		
Multiplier and divider/multiply-accumulator		Operable (Operation is disabled when the RTCLPC bit of the operation speed mode control (OSMC) register is 1)		
DMA controller				
Power-on-reset function		Operable		
Voltage detection function				
External interrupt				
Key interrupt function				
CRC operation function	High-speed CRC	Operation disabled		
	General-purpose CRC	Operation stopped		
RAM parity error detection function		Operation stopped		
RAM guard function				
SFR guard function				
Illegal-memory access detection function				

Remark Operation stopped: Operation is automatically stopped before switching to the HALT mode.

Operation disabled: Operation is stopped before switching to the HALT mode.

f_{IH} : High-speed on-chip oscillator clock f_{EX} : External main system clock

f_{IL} : Low-speed on-chip oscillator clock f_{XT} : XT1 clock

f_X : X1 clock f_{EXS} : External subsystem clock

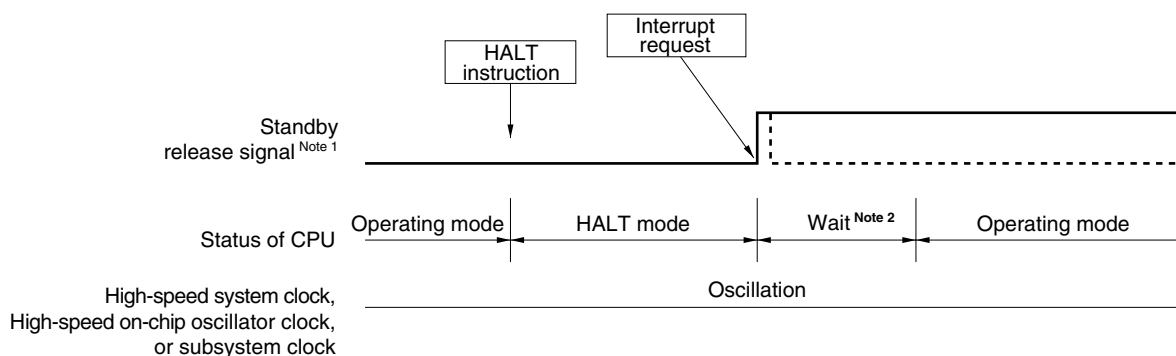
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 18-3. HALT Mode Release by Interrupt Request Generation



<R> **Notes 1.** For details of the standby release signal, see **Figure 16-1**

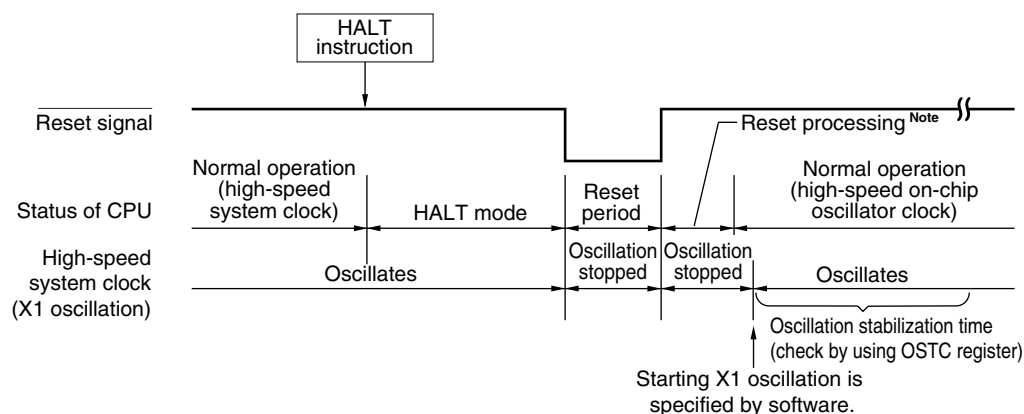
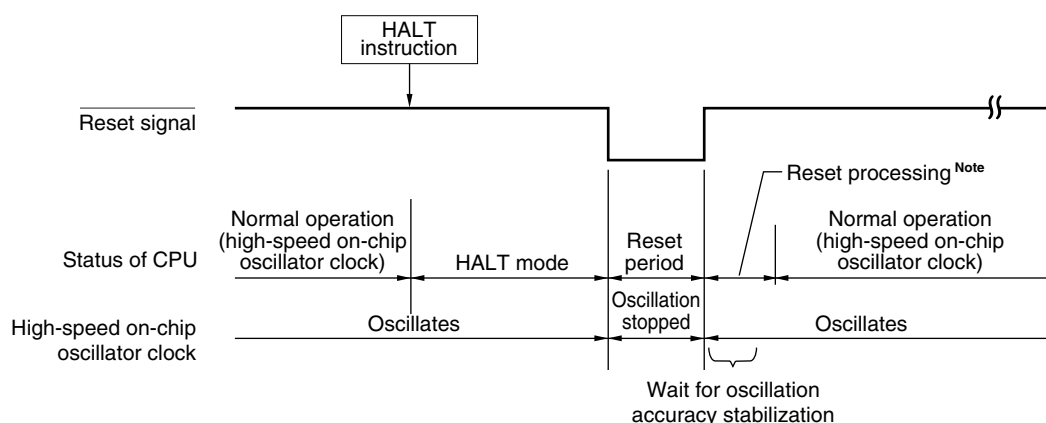
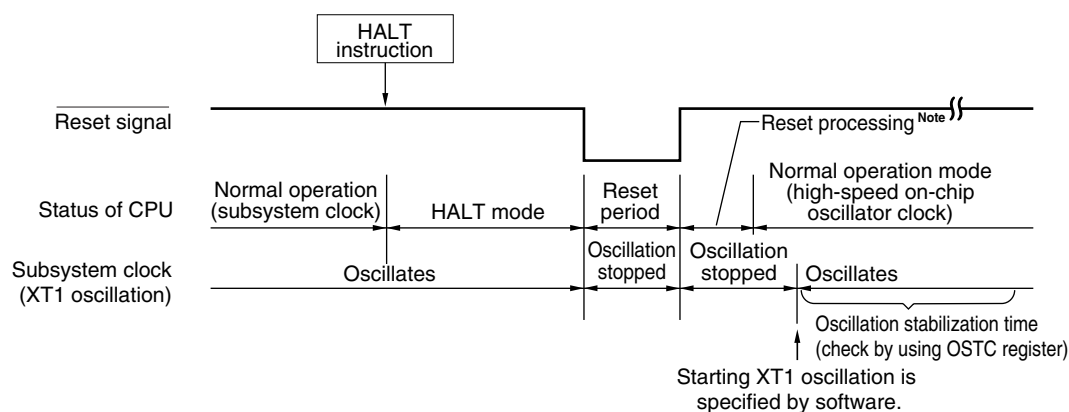
<R> **2.** Wait time for HALT mode release

- When vectored interrupt servicing is carried out
 - Main system clock: 15 to 16 clock
 - Subsystem clock (RTCLPC = 0): 10 to 11 clock
 - Subsystem clock (RTCLPC = 1): 11 to 12 clock
- When vectored interrupt servicing is not carried out
 - Main system clock: 9 to 10 clock
 - Subsystem clock (RTCLPC = 0): 4 to 5 clock
 - Subsystem clock (RTCLPC = 1): 5 to 6 clock

Remark The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

(b) Release by reset signal generation

When the reset signal is generated, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 18-4. HALT Mode Release by Reset**(1) When high-speed system clock is used as CPU clock****(2) When high-speed on-chip oscillator clock is used as CPU clock****(3) When subsystem clock is used as CPU clock**

<R>

<R>

Note For reset processing time, refer to **CHAPTER 19 RESET FUNCTION** and **CHAPTER 20 POWER-ON-RESET CIRCUIT**.

18.3.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the high-speed on-chip oscillator clock, X1 clock, or external main system clock.

- Cautions**
1. Because the interrupt request signal is used to clear the STOP mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the STOP mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.
 2. When using CSIp, UARTq, or the A/D converter in the SNOOZE mode, set up serial standby control register m (SSCm) and A/D converter mode register 2 (ADM2) before switching to the STOP mode. For details, see 12.3 Registers Controlling Serial Array Unit and 11.3 Registers Used in A/D Converter.

Remark p = 00; q = 0; m = 0

The operating statuses in the STOP mode are shown below.

Table 18-2. Operating Statuses in STOP Mode

STOP Mode Setting Item		When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
		When CPU Is Operating on High-speed on-chip oscillator clock (f _{IH})	When CPU Is Operating on X1 Clock (f _x)	When CPU Is Operating on External Main System Clock (f _{EX})
System clock		Clock supply to the CPU is stopped		
Main system clock	f _{IH}	Stopped		
	f _x			
	f _{EX}			
Subsystem clock	f _{XT}	Status before STOP mode was set is retained		
	f _{EXS}			
f _{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops		
CPU		Operation stopped		
Code flash memory				
Data flash memory		Operation stopped		
RAM		Operation stopped		
Port (latch)		Status before STOP mode was set is retained		
Timer array unit		Operation disabled		
Real-time clock (RTC)		Operable		
12-bit interval timer				
Watchdog timer		See CHAPTER 10 WATCHDOG TIMER		
Clock output/buzzer output		Operable if the subsystem clock is selected as the count clock and RTLCLPC = 0. (Operation prohibited in all other cases.)		
A/D converter		Wakeup operation is enabled (switching to the SNOOZE mode)		
Serial array unit (SAU)		Wakeup operation is enabled only for CSIp and UARTq (switching to the SNOOZE mode) Operation is disabled for anything other than CSIp and UARTq		
Serial interface (IICA)		Wakeup by address match operable		
Multiplier and divider/multiply-accumulator		Operation disabled		
DMA controller				
Power-on-reset function		Operable		
Voltage detection function				
External interrupt				
Key interrupt function				
CRC operation function	High-speed CRC	Operation stopped		
	General-purpose CRC			
RAM parity error detection function				
RAM guard function				
SFR guard function				
Illegal-memory access detection function				

Remarks 1. Operation stopped: Operation is automatically stopped before switching to the STOP mode.

Operation disabled: Operation is stopped before switching to the STOP mode.

f_{IH} : High-speed on-chip oscillator clock f_{IL} : Low-speed on-chip oscillator clock

f_x : X1 clock f_{EX} : External main system clock

f_{XT} : XT1 clock f_{EXS} : External subsystem clock

2. $p = 00$; $q = 0$

- Cautions**
1. To use the peripheral hardware that stops operation in the STOP mode, and the peripheral hardware for which the clock that stops oscillating in the STOP mode after the STOP mode is released, restart the peripheral hardware.
 2. To stop the low-speed on-chip oscillator clock in the STOP mode, must previously be set an option byte to stop the watchdog timer operation in the HALT/STOP mode (bit 0 (WDSTBYON) of 000C0H = 0).
 3. To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), temporarily switch the CPU clock to the high-speed on-chip oscillator clock before the execution of the STOP instruction. Before changing the CPU clock from the high-speed on-chip oscillator clock to the high-speed system clock (X1 oscillation) after the STOP mode is released, check the oscillation stabilization time with the oscillation stabilization time counter status register (OSTC).

(2) STOP mode release

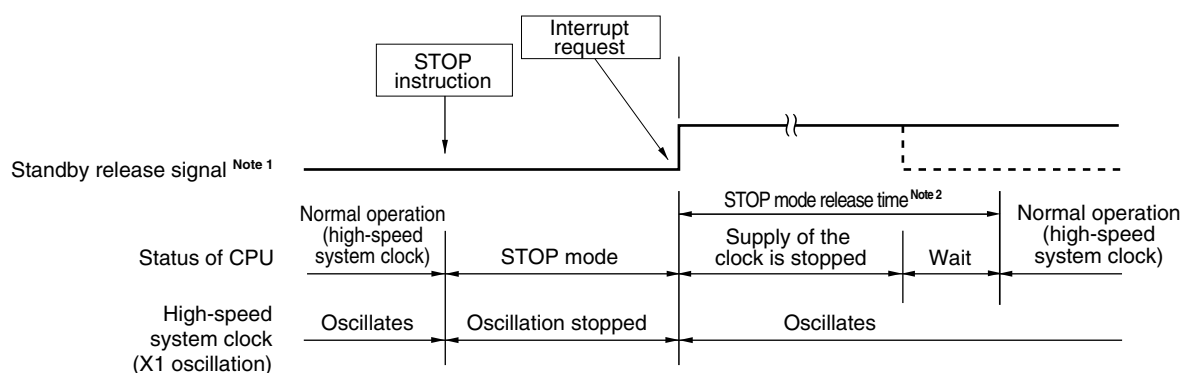
The STOP mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the STOP mode is released. After the oscillation stabilization time has elapsed, if interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 18-5. STOP Mode Release by Interrupt Request Generation (1/2)

(1) When high-speed system clock (X1 oscillation) is used as CPU clock



<R> **Notes 1.** For details of the standby release signal, see **Figure 16-1**

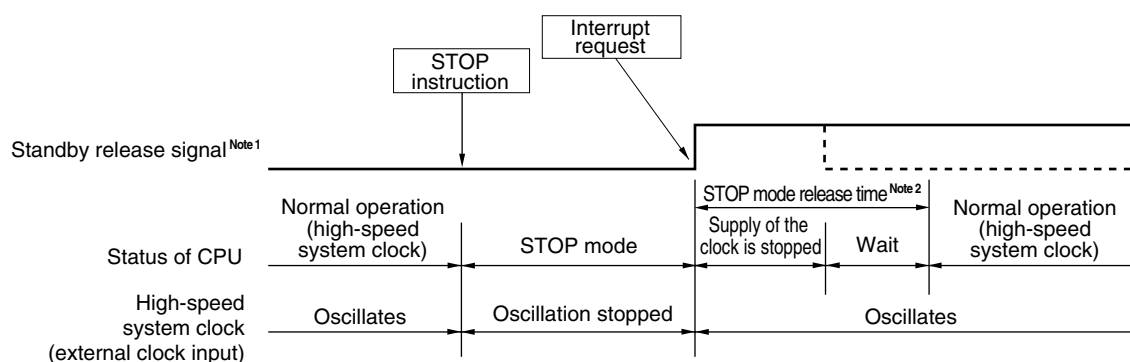
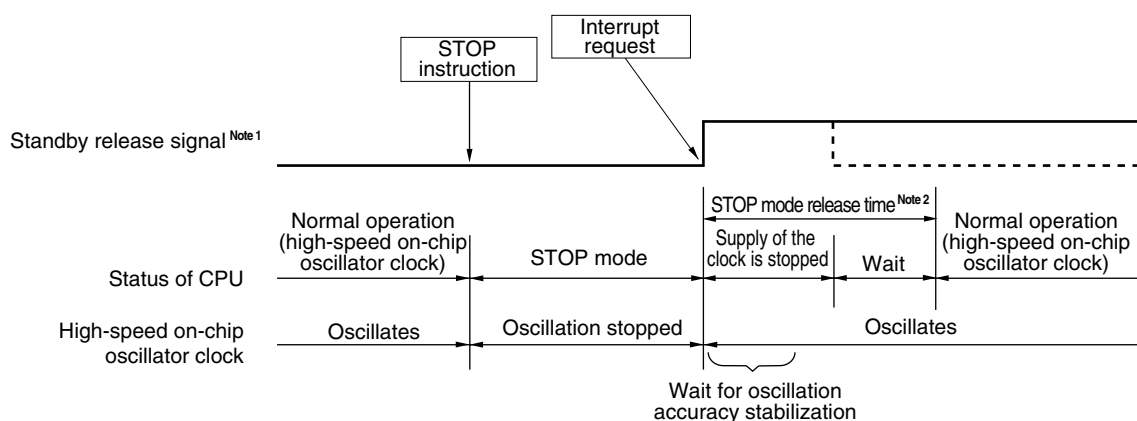
<R> **2.** STOP mode release time

Supply of the clock is stopped: 18.96 μ s to “whichever is longer 28.95 μ s and the oscillation stabilization time (set by OSTS)”

Wait

- When vectored interrupt servicing is carried out: 10 to 11 clocks
- When vectored interrupt servicing is not carried out: 4 to 5 clocks

Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Figure 18-5. STOP Mode Release by Interrupt Request Generation (2/2)**(2) When high-speed system clock (external clock input) is used as CPU clock****(3) When high-speed on-chip oscillator clock is used as CPU clock**

<R>

Notes 1. For details of the standby release signal, see **Figure 16-1**

<R>

2. STOP mode release timeSupply of the clock is stopped: 19.08 to 32.99 μ s

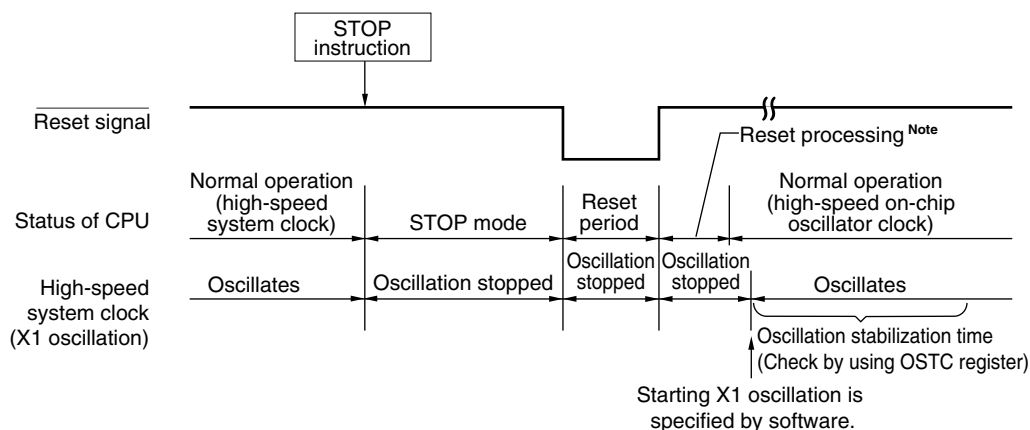
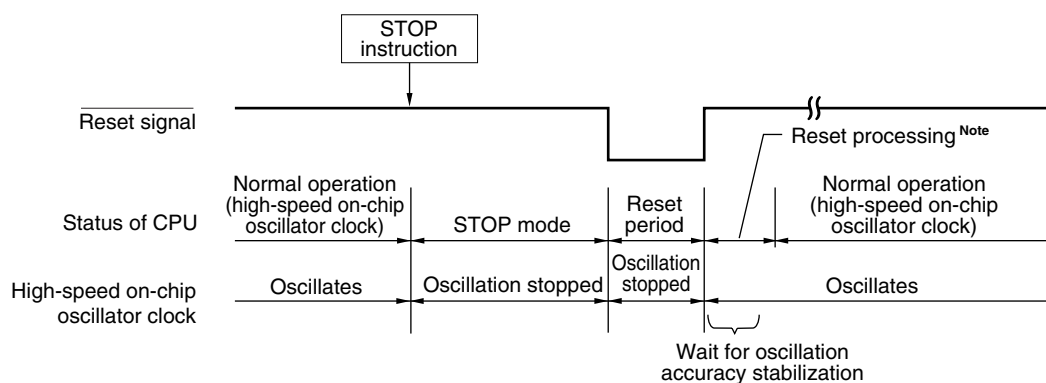
Wait

- When vectored interrupt servicing is carried out: 7 clocks
- When vectored interrupt servicing is not carried out: 1 clock

Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

(b) Release by reset signal generation

When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 18-6. STOP Mode Release by Reset**(1) When high-speed system clock is used as CPU clock****(2) When high-speed on-chip oscillator clock is used as CPU clock**

<R>

Note For reset processing time, refer to **CHAPTER 19 RESET FUNCTION** and **CHAPTER 20 POWER-ON-RESET CIRCUIT**.

18.3.3 SNOOZE mode

(1) SNOOZE mode setting and operating statuses

The SNOOZE mode can only be specified for CSIp, UARTq, or the A/D converter. Note that this mode can only be specified if the CPU clock is the high-speed on-chip oscillator clock.

When using CSIp or UARTq in the SNOOZE mode, set up serial standby control register m (SSCm) before switching to the STOP mode. For details, see **12.3 Registers Controlling Serial Array Unit**.

When using the A/D converter in the SNOOZE mode, set up A/D converter mode register 2 (ADM2) before switching to the STOP mode. For details, see **11.3 Registers Used in A/D Converter**.

Remark p = 00; q = 0; m = 0

<R> In SNOOZE mode transition, wait status to be only following time.

From STOP to SNOOZE

HS (High-speed main) mode : 18.96 to 28.95 μ s

LS (Low-speed main) mode : 20.24 to 28.95 μ s

LV (Low-voltage main) mode : 20.98 to 28.95 μ s

From SNOOZE to normal operation

- When vectored interrupt servicing is carried out:
 - HS (High-speed main) mode : 6.79 to 12.4 μ s + 7 clocks
 - LS (Low-speed main) mode : 2.58 to 7.8 μ s + 7 clocks
 - LV (Low-voltage main) mode : 12.45 to 17.3 μ s + 7 clocks
- When vectored interrupt servicing is not carried out:
 - HS (High-speed main) mode : 6.79 to 12.4 μ s + 1 clock
 - LS (Low-speed main) mode : 2.58 to 7.8 μ s + 1 clock
 - LV (Low-voltage main) mode : 12.45 to 17.3 μ s + 1 clock

The operating statuses in the SNOOZE mode are shown below.

Table 18-3. Operating Statuses in SNOOZE Mode

STOP Mode Setting Item		When Inputting CSIp/UARTq Data Reception Signal or A/D Converter Timer Trigger Signal While in STOP Mode	
		When CPU Is Operating on High-speed on-chip oscillator clock (f _{IH})	
System clock		Clock supply to the CPU is stopped	
Main system clock	f _{IH}	Operation started	
	f _X	Stopped	
	f _{EX}		
Subsystem clock	f _{XT}	Use of the status while in the STOP mode continues	
	f _{EXS}		
f _{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops	
CPU		Operation stopped	
Code flash memory			
Data flash memory			
RAM			
Port (latch)		Use of the status while in the STOP mode continues	
Timer array unit		Operation disabled	
Real-time clock (RTC)		Operable	
12-bit interval timer			
Watchdog timer		See CHAPTER 10 WATCHDOG TIMER	
Clock output/buzzer output		Operable if the subsystem clock is selected as the count clock and RTLCLPC = 0. (Operation prohibited in all other cases.)	
A/D converter		Operable	
Serial array unit (SAU)		Operable only CSIp and UARTq only. Operation disabled other than CSIp and UARTq.	
Serial interface (IICA)		Operation disabled	
Multiplier and divider/multiply-accumulator			
DMA controller			
Power-on-reset function			
Voltage detection function		Operable	
External interrupt			
Key interrupt function			
CRC operation function			
RAM parity error detection function		Operation disabled	
RAM guard function			
SFR guard function			
Illegal-memory access detection function			

Remarks 1. Operation stopped: Operation is automatically stopped before switching to the SNOOZE mode.

Operation disabled: Operation is stopped before switching to the SNOOZE mode.

f_{IH} : High-speed on-chip oscillator clock f_{IL} : Low-speed on-chip oscillator clock

f_X : X1 clock

f_{EX} : External main system clock

f_{XT} : XT1 clock

f_{EXS} : External subsystem clock

2. $p = 00$; $q = 0$

CHAPTER 19 RESET FUNCTION

The following seven operations are available to generate a reset signal.

- (1) External reset input via $\overline{\text{RESET}}$ pin
- (2) Internal reset by watchdog timer program loop detection
- (3) Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit
- (4) Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage
- (5) Internal reset by execution of illegal instruction^{Note}
- (6) Internal reset by RAM parity error
- (7) Internal reset by illegal-memory access

External and internal resets start program execution from the address at 0000H and 0001H when the reset signal is generated.

A reset is effected when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POR and LVD circuit voltage detection, execution of illegal instruction^{Note}, RAM parity error or illegal-memory access, and each item of hardware is set to the status shown in Tables 19-1.

When a low level is input to the $\overline{\text{RESET}}$ pin, the device is reset. It is released from the reset status when a high level is input to the $\overline{\text{RESET}}$ pin and program execution is started with the high-speed on-chip oscillator clock after reset processing. A reset by the watchdog timer is automatically released, and program execution starts using the high-speed on-chip oscillator clock (see **Figures 19-2 to 19-4**) after reset processing. Reset by POR and LVD circuit supply voltage detection is automatically released when $V_{DD} \geq V_{POR}$ or $V_{DD} \geq V_{LVD}$ after the reset, and program execution starts using the high-speed on-chip oscillator clock (see **CHAPTER 20 POWER-ON-RESET CIRCUIT** and **CHAPTER 21 VOLTAGE DETECTOR**) after reset processing.

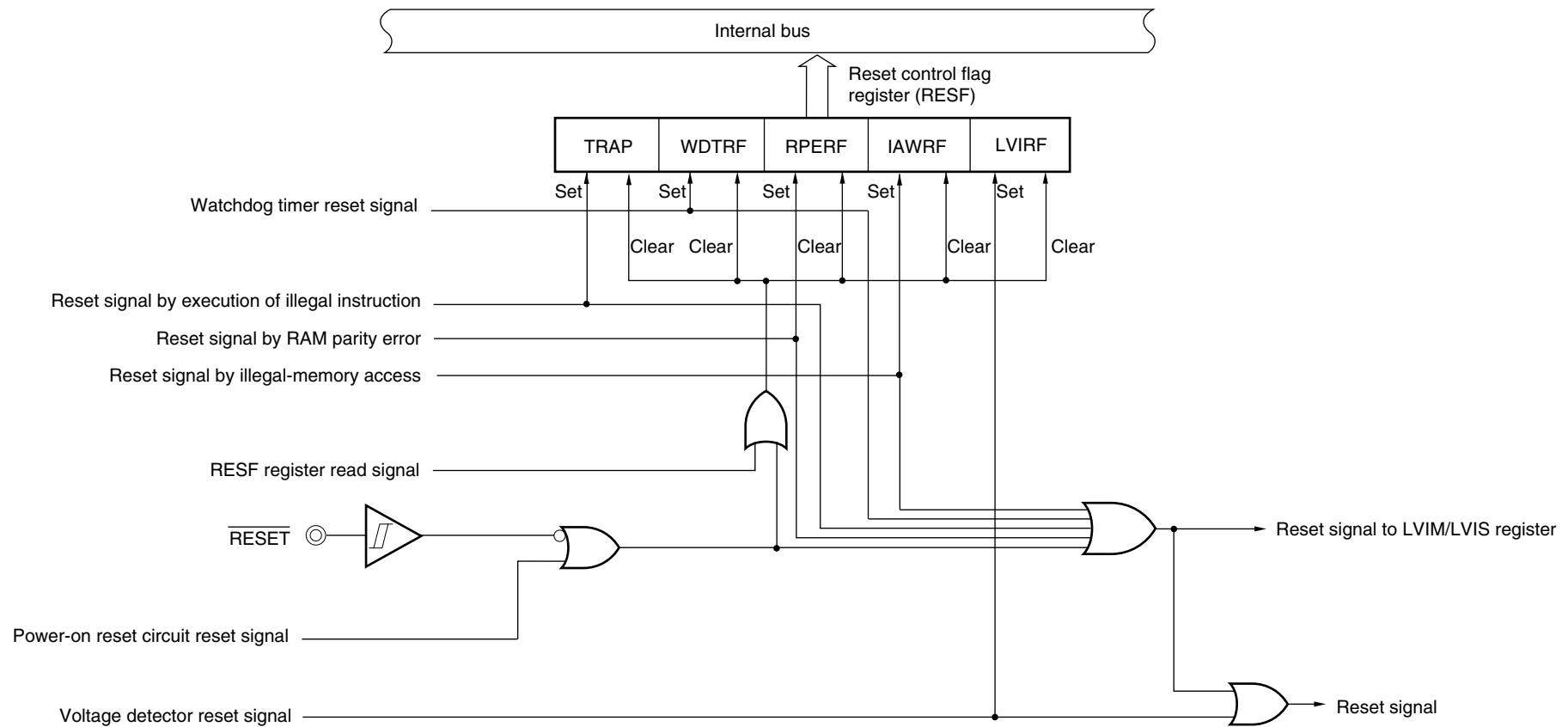
Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

- Cautions**
1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.
(To perform an external reset upon power application, a low level of at least 10 μs must be continued during the period in which the supply voltage is within the operating range ($V_{DD} \geq 1.6\text{ V}$).)
 2. During reset input, the X1 clock, XT1 clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock stop oscillating. External main system clock input and external subsystem clock input become invalid.
 3. When reset is effected, port pin P130 is set to low-level output and other port pins become high-impedance, because each SFR and 2nd SFR are initialized.

Remark V_{POR} : POR power supply rise detection voltage

Figure 19-1. Block Diagram of Reset Function



Caution An LVD circuit internal reset does not reset the LVD circuit.

Remarks

1. LVIM: Voltage detection register
2. LVIS: Voltage detection level register

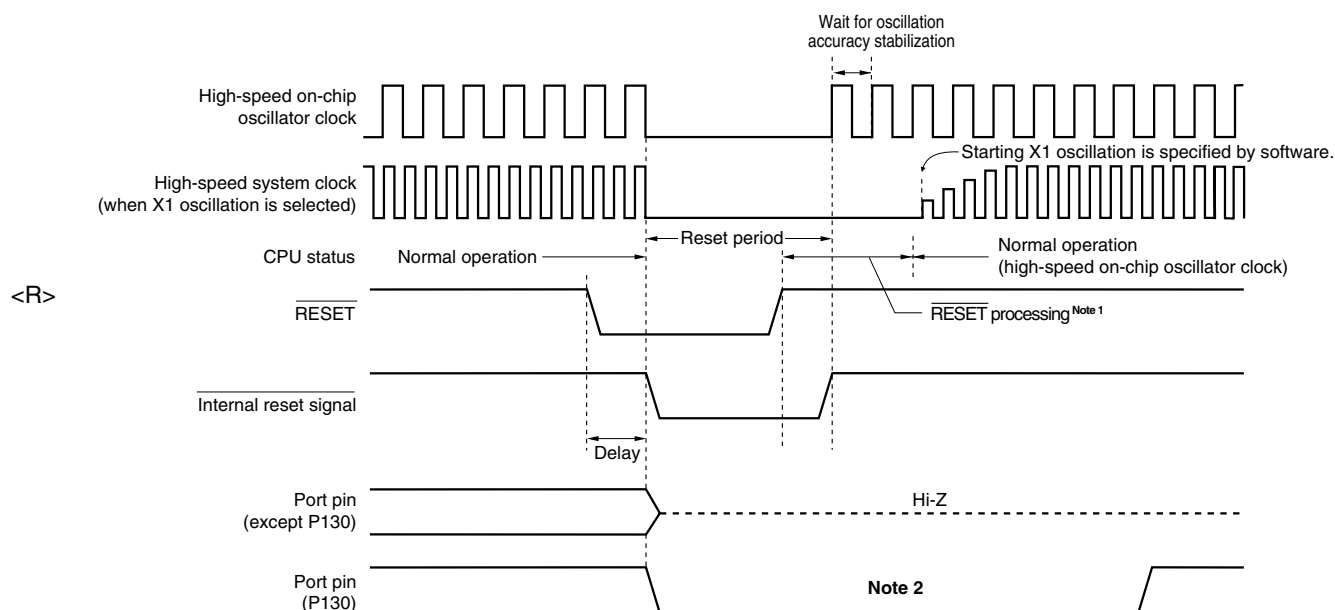
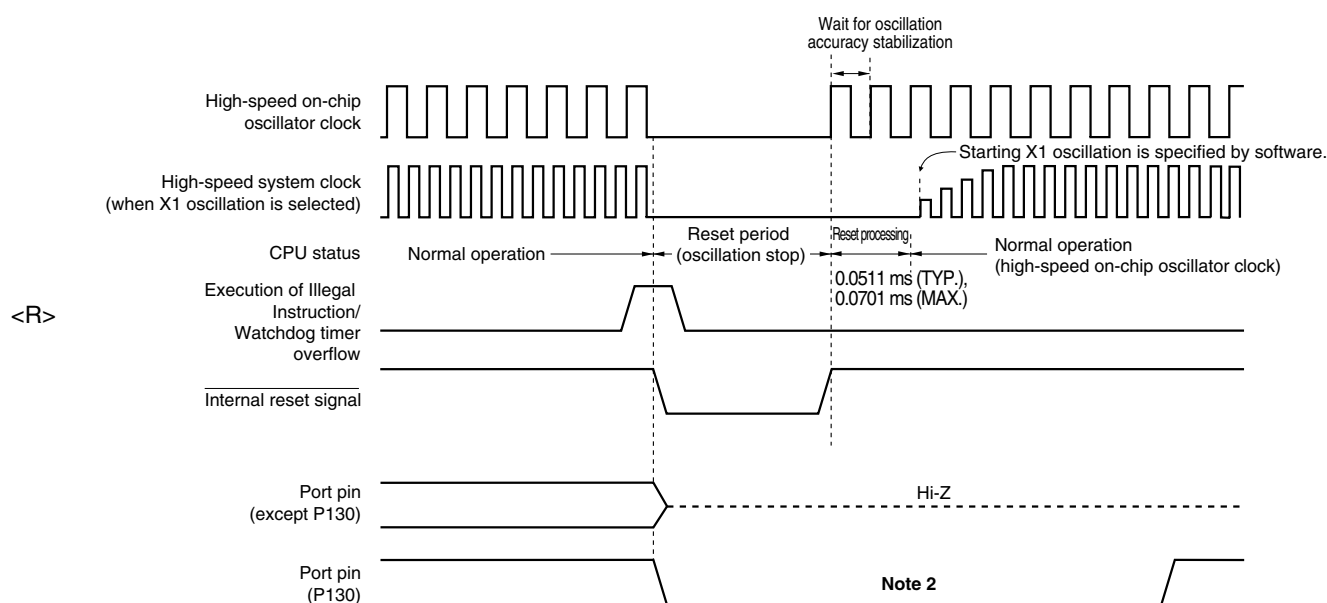
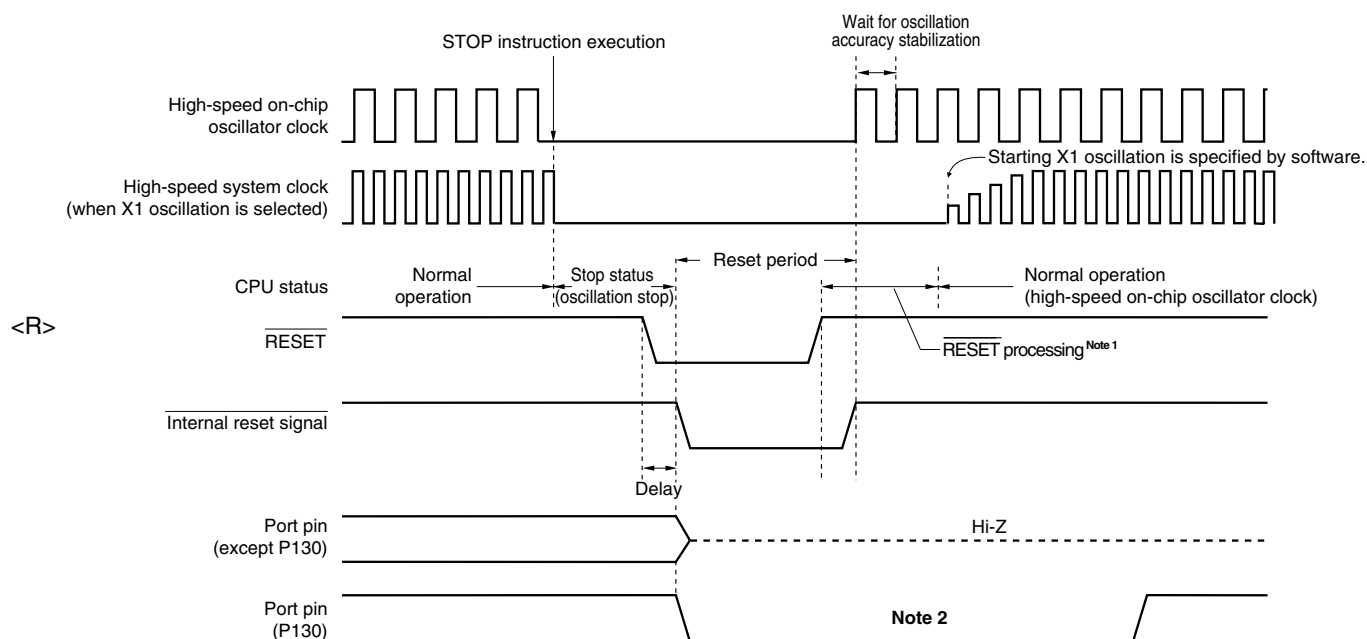
Figure 19-2. Timing of Reset by $\overline{\text{RESET}}$ Input

Figure 19-3. Timing of Reset Due to Execution of Illegal Instruction or Watchdog Timer Overflow



- <R> **Notes** 1. $\overline{\text{RESET}}$ processing time: Time required for the first $\overline{\text{RESET}}$ processing after a power-on reset ends:
 0.672 ms (TYP.), 0.832 ms (MAX.) (When LVD is used)
 0.399 ms (TYP.), 0.519 ms (MAX.) (When LVD off)
 Time required for the second and subsequent $\overline{\text{RESET}}$ processing after a power-on reset ends:
 0.531 ms (TYP.), 0.675 ms (MAX.) (LVD is used)
 0.259 ms (TYP.), 0.362 ms (MAX.) (When LVD off)
 Before $\overline{\text{RESET}}$ processing after power-on, the system must wait for the voltage to stabilize (for 0.981 ms (TYP.) to 2.30 ms (MAX.)).
2. When P130 is set to high-level output before reset is effected, the output signal of P130 can be dummy-output as a reset signal to an external device, because P130 outputs a low level when reset is effected. To release a reset signal to an external device, set P130 to high-level output by software.

Caution A watchdog timer internal reset resets the watchdog timer.

Figure 19-4. Timing of Reset in STOP Mode by RESET Input

- Notes 1.** RESET processing time: Time required for the first RESET processing after a power-on reset ends:
 0.672 ms (TYP.), 0.832 ms (MAX.) (When LVD is used)
 0.399 ms (TYP.), 0.519 ms (MAX.) (When LVD off)
 Time required for the second and subsequent RESET processing after a power-on reset ends:
 0.531 ms (TYP.), 0.675 ms (MAX.) (LVD is used)
 0.259 ms (TYP.), 0.362 ms (MAX.) (When LVD off)
- Before RESET processing after power-on, the system must wait for the voltage to stabilize (for 0.981 ms (TYP.) to 2.30 ms (MAX.)).
- 2.** When P130 is set to high-level output before reset is effected, the output signal of P130 can be dummy-output as a reset signal to an external device, because P130 outputs a low level when reset is effected. To release a reset signal to an external device, set P130 to high-level output by software.

Remark For the reset timing of the power-on-reset circuit and voltage detector, see **CHAPTER 20 POWER-ON-RESET CIRCUIT** and **CHAPTER 21 VOLTAGE DETECTOR**.

Table 19-1. Operation Statuses During Reset Period

Item			During Reset Period	
<R>	System clock		Clock supply to the CPU is stopped.	
	Main system clock	f _{IH}	Operation stopped	
		f _X	Operation stopped (the X1 and X2 pins are input port mode)	
		f _{EX}	Clock input invalid (the pin is input port mode)	
	Subsystem clock	f _{XT}	Operation stopped (the XT1 and XT2 pins are input port mode)	
		f _{EXS}	Clock input invalid (the pin is input port mode)	
	f _{IL}		Operation stopped	
	CPU			
	Code flash memory		Operation stopped	
	Data flash memory		Operation stopped	
RAM		Operation stopped		
Port (latch)		Except P40 and P130: High impedance P40: High impedance (when pin reset or POR reset) or pull-up (when except for pin reset and POR reset) P130: Low-level output.		
Timer array unit		Operation stopped		
Real-time clock (RTC)				
12-bit interval timer				
Watchdog timer				
Clock output/buzzer output				
A/D converter				
Serial array unit (SAU)				
Serial interface (IICA)				
Multiplier & divider, multiply-accumulator				
DMA controller				
Power-on-reset function		Detection operation possible		
Voltage detection function		Operation stopped		
External interrupt		Operation stopped		
Key interrupt function				
CRC operation function	High-speed CRC			
	General-purpose CRC			
RAM parity error detection function				
RAM guard function				
SFR guard function				
Illegal-memory access detection function				

Remark f_{IH}: High-speed on-chip oscillator clock
 f_X: X1 oscillation clock
 f_{EX}: External main system clock
 f_{XT}: XT1 oscillation clock
 f_{EXS}: External subsystem clock
 f_{IL}: Low-speed on-chip oscillator clock

Table 19-2. Hardware Statuses After Reset Acknowledgment (1/4)

Hardware		After Reset Acknowledgment ^{Note 1}
Program counter (PC)		The contents of the reset vector table (0000H, 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		06H
RAM	Data memory	Undefined
	General-purpose registers	Undefined
Processor mode control register (PMC)		00H
Port registers (P0 to P7, P12 to P15) (output latches)		00H
Port mode registers (PM0 to PM7, PM12 to PM15)		FFH
Port mode control registers (PMC0, PMC1, PMC3 to PMC5, PMC10, PMC7, PMC12)		FFH
Port input mode registers (PIM0, PIM1)		00H
Port output mode registers (POM0, POM1, POM5, POM7)		00H
Pull-up resistor option registers (PU0, PU1, PU3 to PU5, PU7, PU12, PU14)		00H (PU4 is 01H)
Peripheral I/O redirection register (PIOR)		00H
Clock operation mode control register (CMC)		00H
Clock operation status control register (CSC)		C0H
System clock control register (CKC)		00H
Oscillation stabilization time counter status register (OSTC)		00H
Oscillation stabilization time select register (OSTS)		07H
Noise filter enable registers 0, 1 (NFEN0, NFEN1)		00H
Peripheral enable register 0 (PER0)		00H
High-speed on-chip oscillator frequency select register (HOCODIV)		Undefined
High-speed on-chip oscillator trimming register (HIOTRM)		Note 2
Operation speed mode control register (OSMC)		00H
Timer array unit	Timer data registers 00 to 07 (TDR00 to TDR07)	0000H
	Timer mode registers 00 to 07 (TMR00 to TMR07)	0000H
	Timer status registers 00 to 07 (TSR00 to TSR07)	0000H
	Timer input select register 0 (TIS0)	00H
	Timer counter registers 00 to 07 (TCR00 to TCR07)	FFFFH
	Timer channel enable status register 0 (TE0)	0000H
	Timer channel start register 0 (TS0)	0000H
	Timer channel stop register 0 (TT0)	0000H
	Timer clock select register 0 (TPS0)	0000H
	Timer output register 0 (TO0)	0000H
	Timer output enable register 0 (TOE0)	0000H
	Timer output level register 0 (TOL0)	0000H
	Timer output mode registers 0 (TOM0)	0000H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. The reset value differs for each chip.

Remark The special function register (SFR) mounted depend on the product. See **3.1.4 Special function registers (SFRs)** and **3.1.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

Table 19-2. Hardware Statuses After Reset Acknowledgment (2/4)

Hardware		Status After Reset Acknowledgment ^{Note 1}
Real-time clock	Second count register (SEC)	00H
	Minute count register (MIN)	00H
	Hour count register (HOUR)	12H
	Week count register (WEEK)	00H
	Day count register (DAY)	01H
	Month count register (MONTH)	01H
	Year count register (YEAR)	00H
	Watch error correction register (SUBCUD)	00H
	Alarm minute register (ALARMWM)	00H
	Alarm hour register (ALARMWH)	12H
	Alarm week register (ALARMWW)	00H
	Control register 0 (RTCC0)	00H
	Control register 1 (RTCC1)	00H
12-bit interval timer	Control register (ITMC)	0FFFH
Clock output/buzzer output controller	Clock output select registers 0, 1 (CKS0, CKS1)	00H
Watchdog timer	Enable register (WDTE)	1AH/9AH ^{Note 2}
A/D converter	12-bit A/D conversion result register (ADCR)	0000H
	8-bit A/D conversion result register (ADCRH)	00H
	Mode registers 0 to 2 (ADM0 to ADM2)	00H
	Conversion result comparison upper limit setting register (ADUL)	FFH
	Conversion result comparison lower limit setting register (ADLL)	00H
	A/D test register (ADTES)	00H
	Analog input channel specification register (ADS)	00H
	A/D port configuration register (ADPC)	00H
Serial array unit (SAU)	Serial data registers 00 to 03, 10, 11 (SDR00 to SDR03, SDR10, SDR11)	0000H
	Serial status registers 00 to 03, 10, 11 (SSR00 to SSR03, SSR10, SSR11)	0000H
	Serial flag clear trigger registers 00 to 03, 10, 11 (SIR00 to SIR03, SIR10, SIR11)	0000H
	Serial mode registers 00 to 03, 10, 11 (SMR00 to SMR03, SMR10, SMR11)	0020H
	Serial communication operation setting registers 00 to 03, 10, 11 (SCR00 to SCR03, SCR10, SCR11)	0087H
	Serial channel enable status registers 0, 1 (SE0, SE1)	0000H
	Serial channel start registers 0, 1 (SS0, SS1)	0000H
	Serial channel stop registers 0, 1 (ST0, ST1)	0000H
	Serial clock select registers 0, 1 (SPS0, SPS1)	0000H
	Serial output registers 0, 1 (SO0, SO1)	0F0FH
	Serial output enable registers 0, 1 (SOE0, SOE1)	0000H
	Serial output level registers 0, 1 (SOL0, SOL1)	0000H
	Serial standby control register 0, 1 (SSC0, SSC1)	0000H
	Input switch control register (ISC)	00H

- Notes**
1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.
 2. The reset value of WDTE is determined by the option byte setting.

Remark The special function register (SFR) mounted depend on the product. See 3.1.4 **Special function registers (SFRs)** and 3.1.5 **Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

Table 19-2. Hardware Statuses After Reset Acknowledgment (3/4)

Hardware		Status After Reset Acknowledgment ^{Note 1}
Serial interface IICA	IICA shift register 0 (IICA0)	00H
	IICA status register 0 (IICS0)	00H
	IICA flag register 0 (IICF0)	00H
	IICA control register 00 (IICCTL00)	00H
	IICA control register 01 (IICCTL01)	00H
	IICA low-level width setting register 0 (IICWL0)	FFH
	IICA high-level width setting register 0 (IICWH0)	FFH
	Slave address registers 0, 1 (SVA0, SVA1)	00H
Multiplier & divider, multiply-accumulator	Multiplication/division data register A (L) (MDAL)	0000H
	Multiplication/division data register A (H) (MDAH)	0000H
	Multiplication/division data register B (L) (MDBL)	0000H
	Multiplication/division data register B (H) (MDBH)	0000H
	Multiplication/division data register C (L) (MDCL)	0000H
	Multiplication/division data register C (H) (MDCH)	0000H
	Multiplication/division control register (MDUC)	00H
Key interrupt	Key return control register (KRCTL)	00H
	Key return mode registers 0, 1 (KRM0, KRM1)	00H
	Key return flag register (KRF)	00H

Note During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

Remark The special function register (SFR) mounted depend on the product. See **3.1.4 Special function registers (SFRs)** and **3.1.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

Table 19-2. Hardware Statuses After Reset Acknowledgment (4/4)

Hardware		Status After Reset Acknowledgment ^{Note 1}
Reset function	Reset control flag register (RESF)	Undefined ^{Note 2}
Voltage detector	Voltage detection register (LVIM)	00H ^{Note 2}
	Voltage detection level register (LVIS)	00H/01H/81H ^{Notes 2, 3}
DMA controller	SFR address registers 0, 1 (DSA0, DSA1)	00H
	RAM address registers 0, 1 (DRA0, DRA1)	0000H
	Byte count registers 0, 1 (DBC0, DBC1)	0000H
	Mode control registers 0, 1 (DMC0, DMC1)	00H
	Operation control registers 0, 1 (DRC0, DRC1)	00H
Interrupt	Request flag registers 0L, 0H, 1L, 1H, 2L, 2H (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)	00H
	Mask flag registers 0L, 0H, 1L, 1H, 2L, 2H (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)	FFH
	Priority specification flag registers 00L, 00H, 01L, 01H, 02L, 02H, 10L, 10H, 11L, 11H, 12L, 12H (PR00L, PR00H, PR01L, PR01H, PR10L, PR10H, PR11L, PR11H, PR02L, PR02H, PR12L, PR12H)	FFH
	External interrupt rising edge enable registers 0, 1 (EGP0, EGP1)	00H
	External interrupt falling edge enable registers 0, 1 (EGN0, EGN1)	00H
Safety functions	Flash memory CRC control register (CRC0CTL)	00H
	Flash memory CRC operation result register (PGCRCL)	0000H
	CRC input register (CRCIN)	00H
	CRC data register (CRCD)	0000H
	Invalid memory access detection control register (IAWCTL)	00H
	RAM parity error control register (RPECTL)	00H
Flash memory	Data flash control register (DFLCTL)	00H
BCD correction circuit	BCD correction result register (BCDADJ)	Undefined

(Notes and Remark are listed on the next page.)

- Notes**
1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.
 2. These values vary depending on the reset source.

<R>

Reset Source Register		RESET Input	Reset by POR	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by RAM parity error	Reset by illegal- memory access	Reset by LVD
RESF	TRAP	Cleared (0)		Set (1)	Held			
	WDTRF			Held	Set (1)	Held		
	RPERF		Held		Set (1)	Held		
	IAWRF		Held			Set (1)		
	LVIRF		Held					Set (1)
								Set (1)
LVIM	LVISEN	Cleared (0)						Held
	LVIOMSK	Held						
	LVIF							
LVIS		Cleared (00H/01H/81H)						

3. The generation of reset signal other than an LVD reset sets as follows.

- When option byte LVIMDS1, LVIMDS0 = 1, 0: 00H
- When option byte LVIMDS1, LVIMDS0 = 1, 1: 81H
- When option byte LVIMDS1, LVIMDS0 = 0, 1: 01H

Remark The special function register (SFR) mounted depend on the product. See **3.1.4 Special function registers (SFRs)** and **3.1.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

19.1 Register for Confirming Reset Source

19.1.1 Reset Control Flag Register (RESF)

Many internal reset generation sources exist in the RL78/G1A. The reset control flag register (RESF) is used to store which source has generated the reset request.

The RESF register can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input, reset by power-on-reset (POR) circuit, and reading the RESF register clear TRAP, WDTRF, RPERF, IAWRF, and LVIRF flags.

Figure 19-5. Format of Reset Control Flag Register (RESF)

Address: FFFA8H After reset: 00H^{Note 1} R

Symbol	7	6	5	4	3	2	1	0
RESF	TRAP	0	0	WDTRF	0	RPERF	IAWRF	LVIRF

TRAP	Internal reset request by execution of illegal instruction ^{Note 2}
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

WDTRF	Internal reset request by watchdog timer (WDT)
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

RPERF	Internal reset request t by RAM parity
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

IAWRF	Internal reset request t by illegal-memory access
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

LVIRF	Internal reset request by voltage detector (LVD)
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

- Notes**
1. The value after reset varies depending on the reset source.
 2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

- Cautions**
1. Do not read data by a 1-bit memory manipulation instruction.
 2. When a reset occurs, use RAM parity error reset generation enabled (RPERDIS = 0). If RAM parity error resets to use are enabled (RPERDIS = 0), be sure to initialize the RAM area whose data is to be accessed and the RAM area from which to execute instructions + 10 bytes. Reset signal generation enable RAM parity error reset generation. For detail, refer to 22.3.3 RAM parity error detection function.

The status of the RESF register when a reset request is generated is shown in Table 19-3.

Table 19-3. RESF Register Status When Reset Request Is Generated

Reset Source Flag	RESET Input	Reset by POR	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by RAM parity error	Reset by illegal- memory access	Reset by LVD
TRAP	Cleared (0)		Set (1)	Held			
WDTRF			Held	Set (1)	Held		
RPERF			Held		Set (1)	Held	
IAWRF			Held			Set (1)	Held
LVIRF			Held				Set (1)

CHAPTER 20 POWER-ON-RESET CIRCUIT

20.1 Functions of Power-on-reset Circuit

The power-on-reset circuit (POR) has the following functions.

- Generates internal reset signal at power on.
The reset signal is released when the supply voltage (V_{DD}) exceeds 1.51 V (TYP.).
- Compares supply voltage (V_{DD}) and detection voltage ($V_{PDR} = 1.50$ V (TYP.)), generates internal reset signal when $V_{DD} < V_{PDR}$.

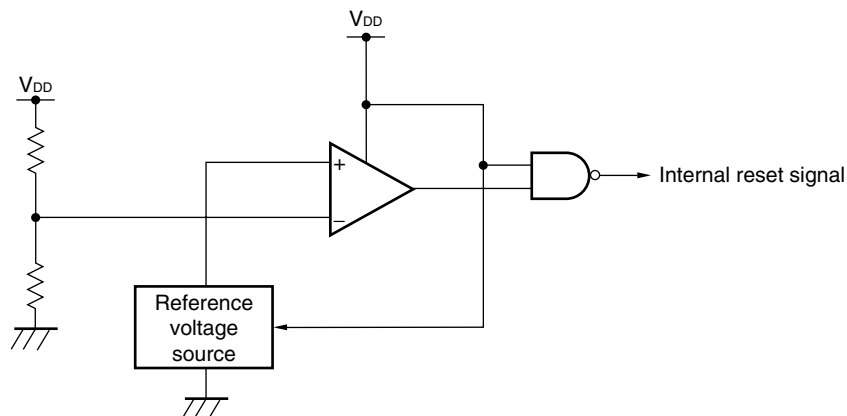
Caution If an internal reset signal is generated in the POR circuit, TRAP, WDTRF, RPERF, IAWRF, and LVIRF flags of the reset control flag register (RESF) is cleared.

Remark This product incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT), voltage-detector (LVD), illegal instruction execution, RAM parity error, or illegal-memory access. The RESF register is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by the watchdog timer (WDT), voltage-detector (LVD), illegal instruction execution, RAM parity error, or illegal-memory access.
For details of the RESF register, see **CHAPTER 19 RESET FUNCTION**.

20.2 Configuration of Power-on-reset Circuit

The block diagram of the power-on-reset circuit is shown in Figure 20-1.

Figure 20-1. Block Diagram of Power-on-reset Circuit



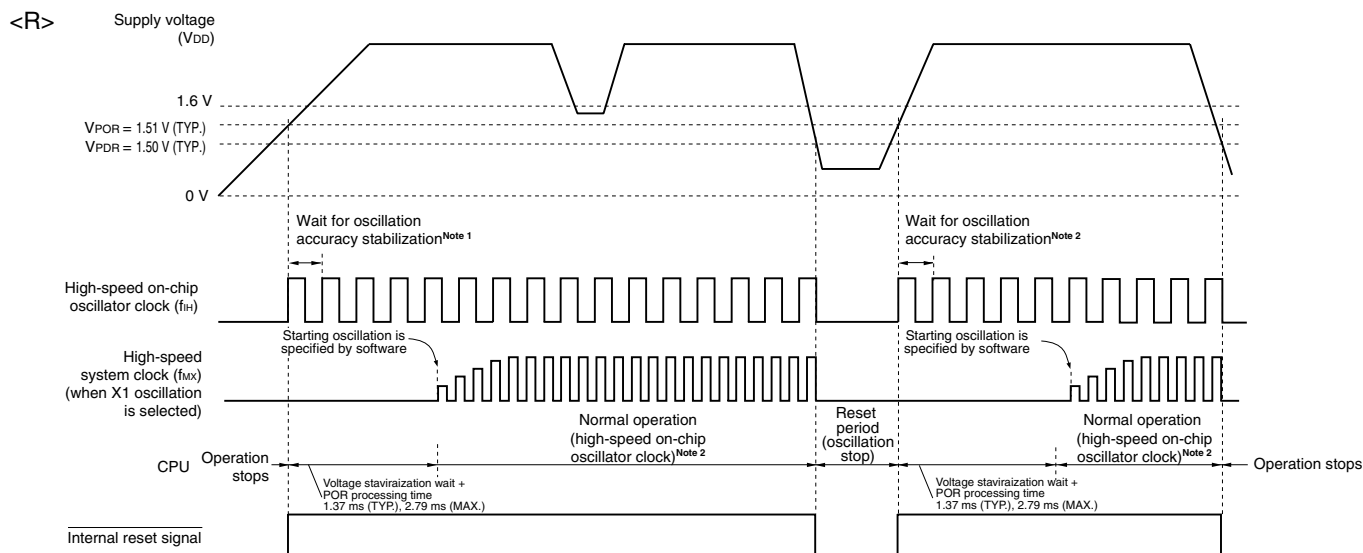
20.3 Operation of Power-on-reset Circuit

- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds the detection voltage ($V_{PDR} = 1.51 \text{ V (TYP.)}$), the reset status is released.
- The supply voltage (V_{DD}) and detection voltage ($V_{PDR} = 1.50 \text{ V (TYP.)}$) are compared. When $V_{DD} < V_{PDR}$, the internal reset signal is generated.

The timing of generation of the internal reset signal by the power-on-reset circuit and voltage detector is shown below.

Figure 20-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When LVD is OFF (option byte 000C1H: VPOC2 = 1)

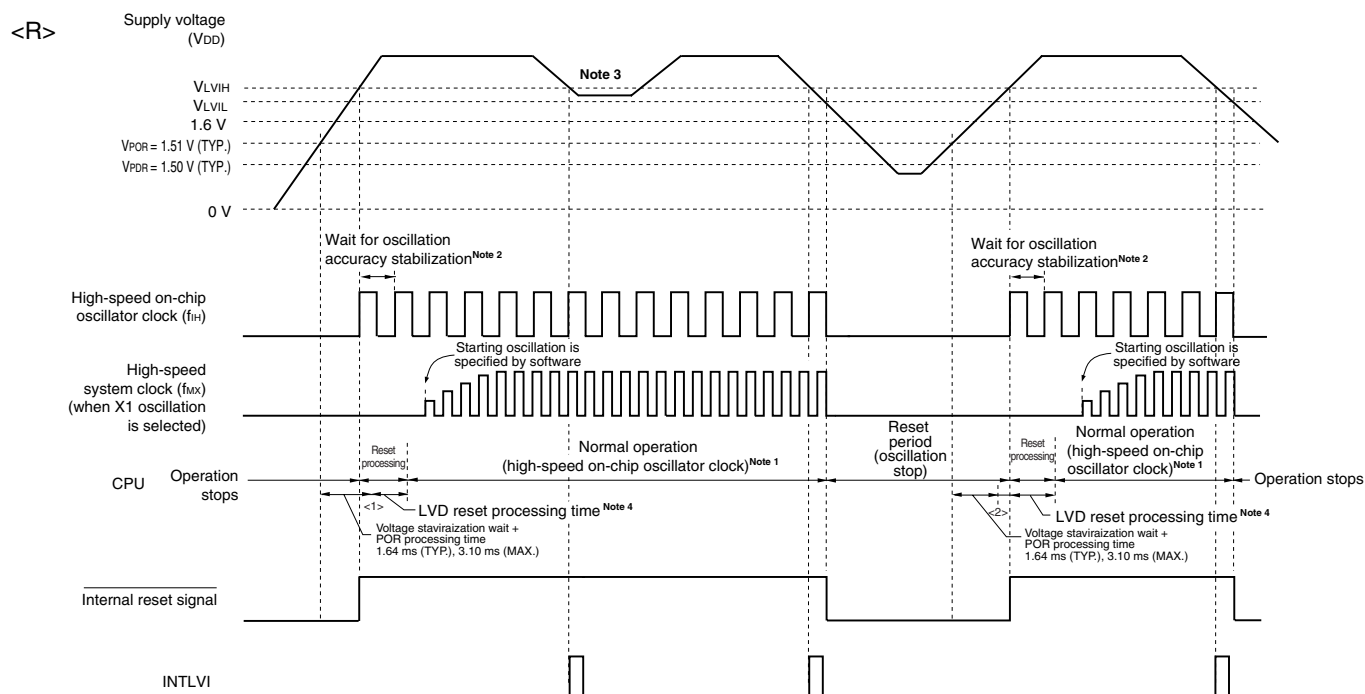


- Notes**
1. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.
 2. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

Remark V_{POR} : POR power supply rise detection voltage
 V_{PDR} : POR power supply fall detection voltage

Figure 20-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (2/3)

(2) When LVD is in interrupt & reset mode (option byte 000C1H: LVIMDS1, LVIMDS0 = 1, 0)



Notes 1. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. When using the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. When using the XT1 clock, use the timer function to confirm of the lapse of the stabilization time.

2. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

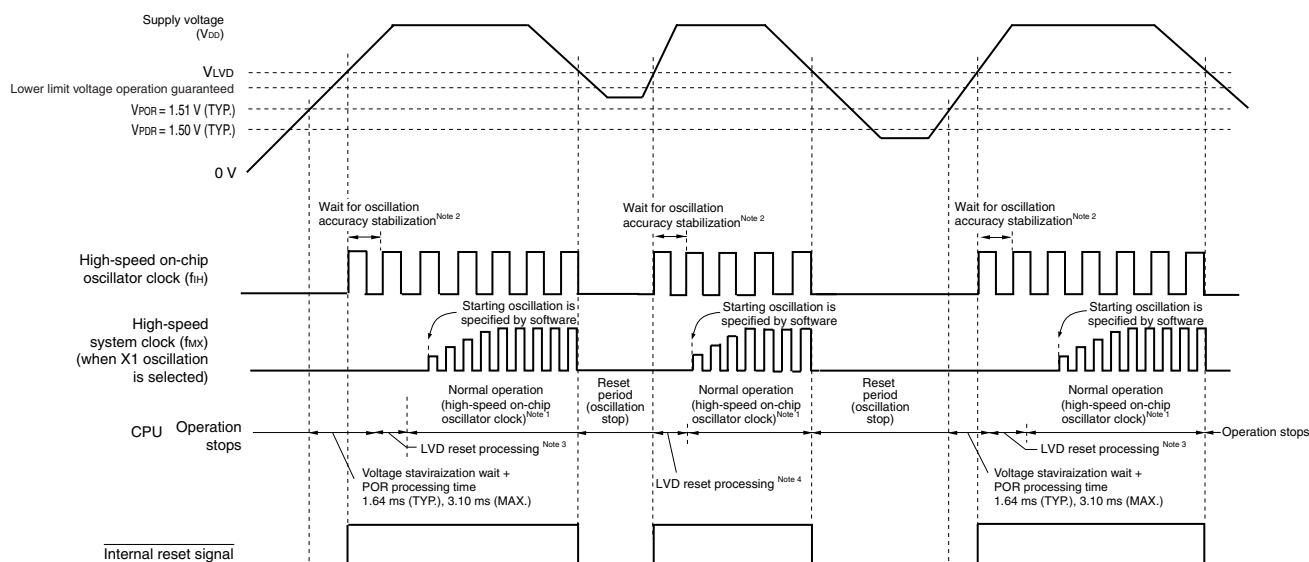
3. After the interrupt request signal (INTLVI) is generated, the LVILV and LVIMD bits of the voltage detection level register (LVIS) are automatically set to 1. To make allowances for cases when the operating voltage restores to the high voltage detection level (VLVDH) without falling below the low voltage detection level (VLVDL), perform processing according to **Figure 21-7. Processing Procedure After an Interrupt Is Generated** after INTLVI is generated.

4. The time required until normal operation starts after power-on is either of the following, depending on the time from when VPOR (1.51 V (TYP.)) is reached to when the LVD detection level (VLVD) is reached:

- If the "voltage stabilization wait time + POR processing time" has not elapsed before VLVD is reached (<1> in the figure), the following LVD reset processing time is required in addition to the "voltage stabilization wait time + POR processing time" after VPOR is reached.
LVD reset processing time: 0 to 0.0701 ms
- If the "voltage stabilization wait time + POR processing time" has elapsed before VLVD is reached (<2> in the figure), the following LVD reset processing time is required after VLVD is reached:
LVD reset processing time: 0.0511 ms (TYP.), 0.0701 ms (MAX.)

Remark VLVH, VLVIL: LVD detection voltage
VPOR: POR power supply rise detection voltage
VPDR: POR power supply fall detection voltage

<R>

Figure 20-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (3/3)**(3) When LVD is in reset mode (option byte 000C1H: LVIMDS1, LVIMDS0 = 1, 1)**

- Notes**
1. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. When using the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. When using the XT1 clock, use the timer function to confirm of the lapse of the stabilization time.
 2. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.
 3. The time required until normal operation starts after power-on is either of the following, depending on the time from when V_{POR} (1.51 V (TYP.)) is reached to when the LVD detection level (V_{LVD}) is reached:
 - If the "voltage stabilization wait time + POR processing time" has not elapsed before V_{LVD} is reached (<1> in the figure), the following LVD reset processing time is required in addition to the "voltage stabilization wait time + POR processing time" after V_{POR} is reached.
LVD reset processing time: 0 to 0.0701 ms
 - If the "voltage stabilization wait time + POR processing time" has elapsed before V_{LVD} is reached (<2> in the figure), the following LVD reset processing time is required after V_{LVD} is reached:
LVD reset processing time: 0.0511 ms (TYP.), 0.0701 ms (MAX.)
 4. When the supply voltage drops, if an internal reset generated by the voltage detector (LVD) occurs and the supply voltage stops dropping and rises to V_{LVD}, the following reset processing time is required to when the LVD detection level (V_{LVD}) is reached.
LVD reset processing time: 0 to 0.0701 ms
TYP. value: Operation in HS mode at f_{CLK} = 32 MHz

Remark V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage

20.4 Cautions for Power-on-reset Circuit

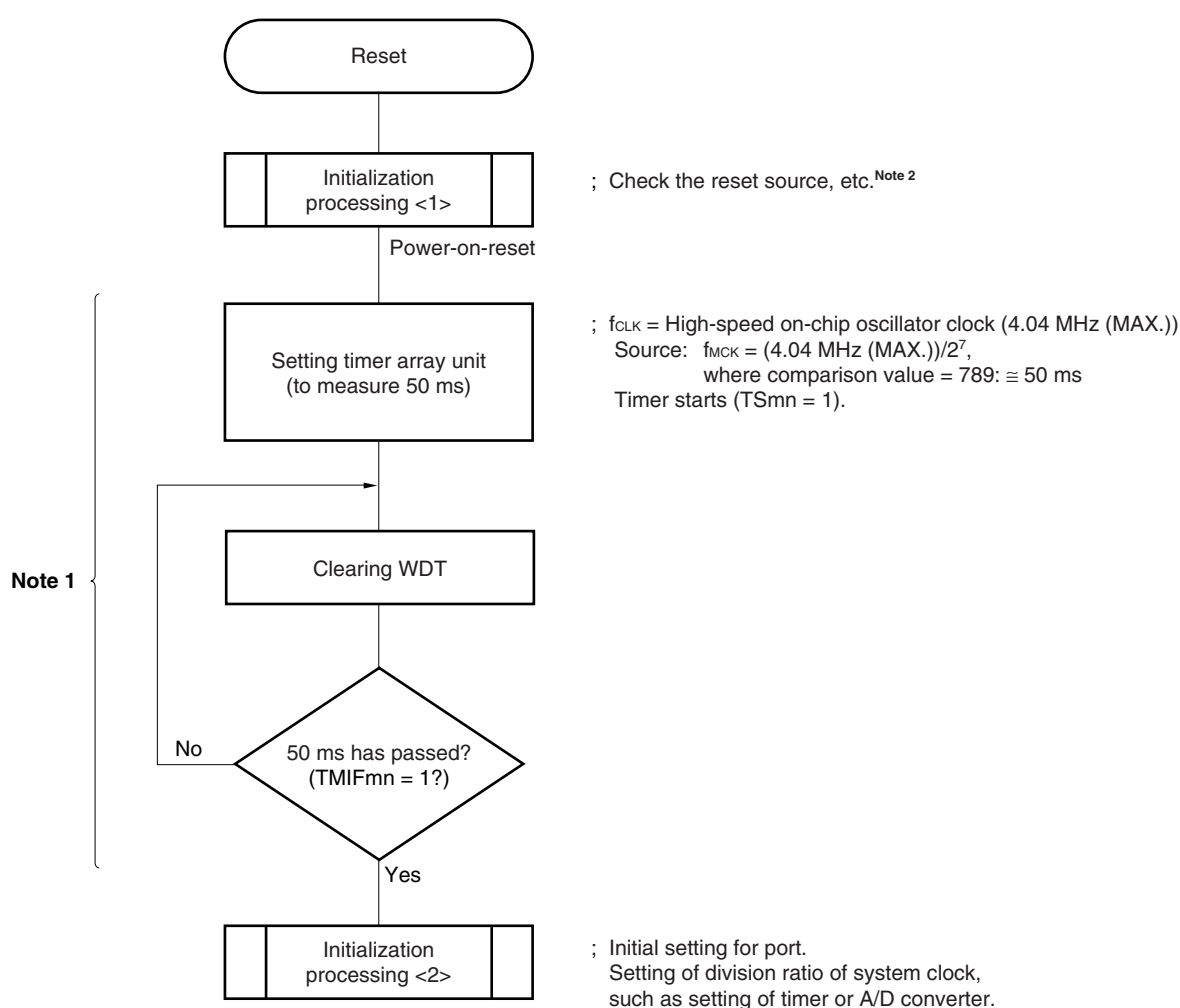
In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the POR detection voltage (V_{POR} , V_{PDR}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

Figure 20-3. Example of Software Processing After Reset Release (1/2)

- If supply voltage fluctuation is 50 ms or less in vicinity of POR detection voltage



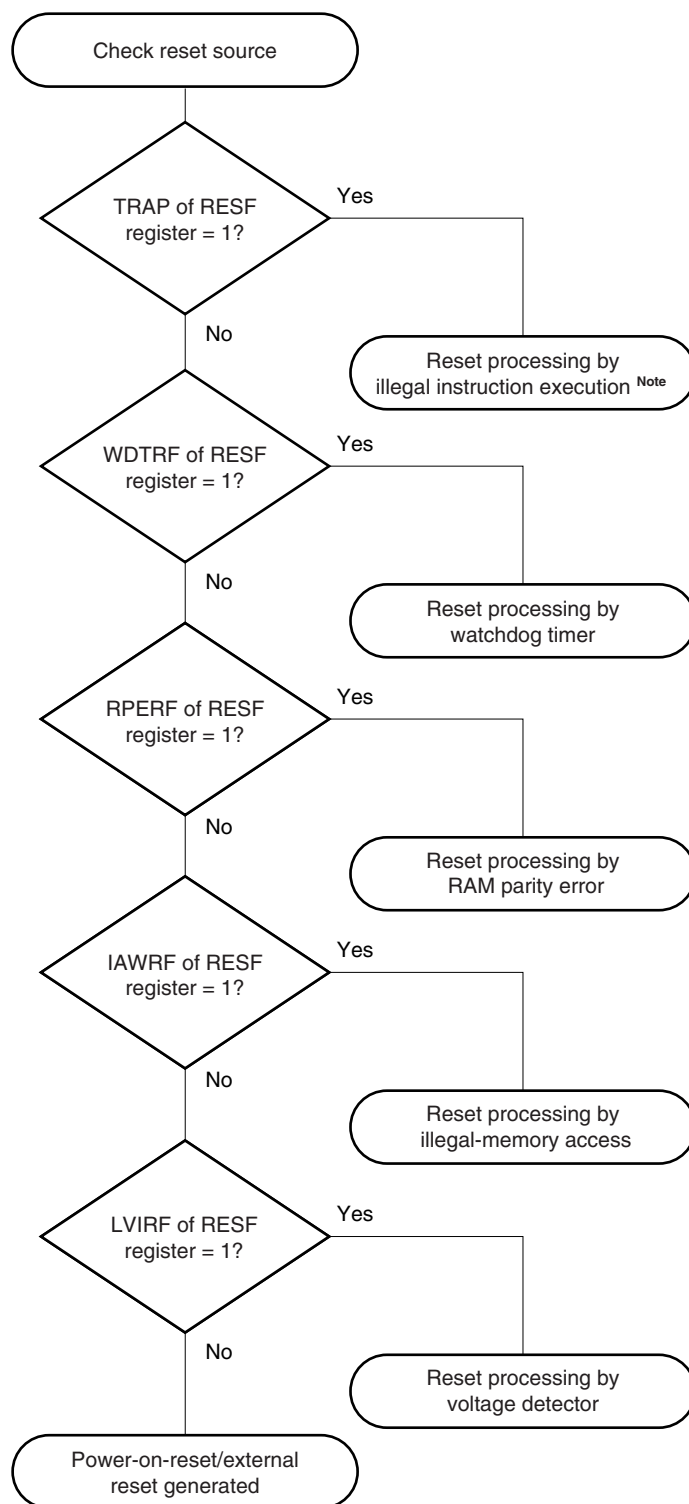
Notes 1. If reset is generated again during this period, initialization processing <2> is not started.

2. A flowchart is shown on the next page.

Remark m = 0, 1
 n = 0 to 7

Figure 20-3. Example of Software Processing After Reset Release (2/2)

- Checking reset source



Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

CHAPTER 21 VOLTAGE DETECTOR

21.1 Functions of Voltage Detector

The voltage detector (LVD) has the following functions.

- The LVD circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVDH} , V_{LVDL}), and generates an internal reset or internal interrupt signal.
- The detection level for the power supply detection voltage (V_{LVDH} , V_{LVDL}) can be selected by using the option byte as one of 12 levels (For details, see **CHAPTER 24 OPTION BYTE**).
- Operable in STOP mode.
- The following three operation modes can be selected by using the option byte.

(a) Interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0)

For the two detection voltages selected by the option byte 000C1H, the high-voltage detection level (V_{LVDH}) is used for generating interrupts and ending resets, and the low-voltage detection level (V_{LVDL}) is used for triggering resets.

(b) Reset mode (option byte LVIMDS1, LVIMDS0 = 1, 1)

The detection voltage (V_{LVD}) selected by the option byte 000C1H is used for triggering and ending resets.

(c) Interrupt mode (option byte LVIMDS1, LVIMDS0 = 0, 1)

The detection voltage (V_{LVD}) selected by the option byte 000C1H is used for generating interrupts/reset release.

Two detection voltages (V_{LVDH} , V_{LVDL}) can be specified in the interrupt & reset mode, and one (V_{LVD}) can be specified in the reset mode and interrupt mode.

The reset and interrupt signals are generated as follows according to the option byte (LVIMDS0, LVIMDS1) selection.

Interrupt & reset mode (LVIMDS1, LVIMDS0 = 1, 0)	Reset mode (LVIMDS1, LVIMDS0 = 1, 1)	Interrupt mode (LVIMDS1, LVIMDS0 = 0, 1)
Generates an internal interrupt signal when $V_{DD} < V_{LVDH}$, and an internal reset when $V_{DD} < V_{LVDL}$. Releases the reset signal when $V_{DD} \geq V_{LVDH}$.	Generates an internal reset signal when $V_{DD} < V_{LVD}$ and releases the reset signal when $V_{DD} \geq V_{LVD}$.	Generates an internal interrupt signal when V_{DD} drops lower than V_{LVD} ($V_{DD} < V_{LVD}$) or when V_{DD} becomes V_{LVD} or higher ($V_{DD} \geq V_{LVD}$). Releases the reset signal when $V_{DD} \geq V_{LVD}$ at power on.

While the voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the voltage detection flag (LVIF: bit 0 of the voltage detection register (LVIM)).

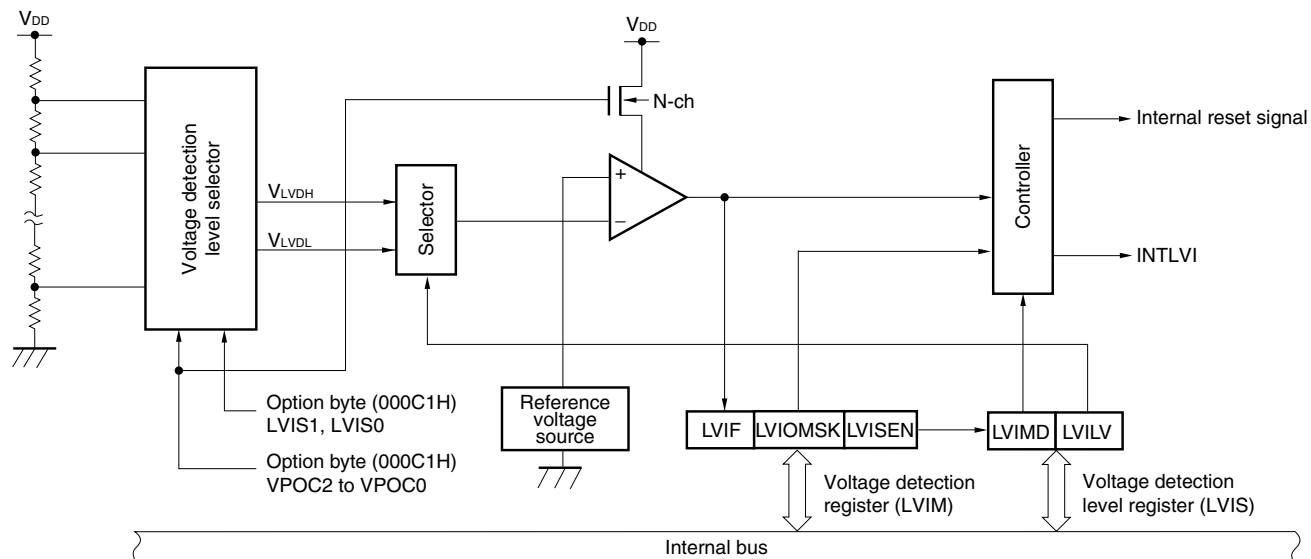
Bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of the RESF register, see **CHAPTER 19 RESET FUNCTION**.

21.2 Configuration of Voltage Detector

The block diagram of the voltage detector is shown in Figure 21-1.

<R>

Figure 21-1. Block Diagram of Voltage Detector



21.3 Registers Controlling Voltage Detector

The voltage detector is controlled by the following registers.

- Voltage detection register (LVIM)
- Voltage detection level register (LVIS)

21.3.1 Voltage detection register (LVIM)

This register is used to specify whether to enable or disable rewriting the voltage detection level register (LVIS), as well as to check the LVD output mask status.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 21-2. Format of Voltage Detection Register (LVIM)

Address: FFFA9H After reset: 00H ^{Note 1} R/W ^{Note 2}

Symbol	<7>	6	5	4	3	2	<1>	<0>
LVIM	LVISEN	0	0	0	0	0	LVIOMSK	LVIF

LVISEN	Specification of whether to enable or disable rewriting the voltage detection level register (LVIS)
0	Disabling rewriting
1	Enabling rewriting ^{Note 3}

LVIOMSK	Mask status flag of LVD output
0	Mask is invalid
1	Mask is valid ^{Note 4}

LVIF	Voltage detection flag
0	Supply voltage (V_{DD}) $\geq$ detection voltage (V_{LVD}), or when LVD operation is disabled
1	Supply voltage (V_{DD}) $<$ detection voltage (V_{LVD})

Notes 1. The reset value changes depending on the reset source.

If the LVIS register is reset by LVD, it is not reset but holds the current value. In other reset, LVISEN is cleared to 0.

2. Bits 0 and 1 are read-only.

3. This can only be use when LVIMDS1 and LVIMDS0 are set to 1 and 0 (interrupt and reset mode) by the option byte (In the other mode is invalid).

4. LVIOMSK bit is automatically set to "1" in the following periods and reset or interruption by LVD is masked.

- Period during LVISEN = 1
- Waiting period from the time when LVD interrupt is generated until LVD detection voltage becomes stable
- Waiting period from the time when the value of LVILV bit changes until LVD detection voltage becomes stable

<R>

21.3.2 Voltage detection level register (LVIS)

This register selects the voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation input sets this register to 00H/01H/81H ^{Note1}.

Figure 21-3. Format of Voltage Detection Level Select Register (LVIS)

Address:	FFFAAH	After reset:	00H/01H/81H ^{Note1}	R/W						
Symbol	<7>	6	5	4	3	2	1	<0>		
LVIS	LVIMD	0	0	0	0	0	0	LVILV		

LVIMD ^{Note2}	Operation mode of voltage detection
0	Interrupt mode
1	Reset mode

LVILV ^{Note2}	LVD detection level
0	High-voltage detection level (V _{LVDH})
1	Low-voltage detection level (V _{LVDL} or V _{LVD})

Notes 1. The reset value changes depending on the reset source and the setting of the option byte.

This register is not cleared (00H) by LVD reset.

The generation of reset signal other than an LVD reset sets as follows.

- When option byte LVIMDS1, LVIMDS0 = 1, 0: 00H
- When option byte LVIMDS1, LVIMDS0 = 1, 1: 81H
- When option byte LVIMDS1, LVIMDS0 = 0, 1: 01H

2. Writing "0" can only be allowed when LVIMDS1 and LVIMDS0 are set to 1 and 0 (interrupt and reset mode) by the option byte. In other cases, writing is not allowed and the value is switched automatically when reset or interrupt is generated.

Cautions 1. Only rewrite the value of the LVIS register after setting the LVISEN bit (bit 7 of the LVIM register) to 1.

2. Specify the LVD operation mode and detection voltage (V_{LVDH}, V_{LVDL}) by using the option byte (000C1H). Table 21-1 shows the option byte (000C1H) settings. For details about the option byte, see **CHAPTER 24 OPTION BYTE**.

Table 21-1. LVD Operation Mode and Detection Voltage Settings for User Option Byte (000C1H/010C1H) (2/2)Address: 000C1H/010C1H^{Note}

	7	6	5	4	3	2	1	0
<R>	VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

- LVD setting (interrupt mode)

Detection voltage		Option byte Setting Value						
V _{LVD}		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
1.67 V	1.63 V	0	1	0	0	0	1	1
1.77 V	1.73 V			0	0	0	1	0
1.88 V	1.84 V			0	0	1	1	1
1.98 V	1.94 V			0	0	1	1	0
2.09 V	2.04 V			0	0	1	0	1
2.50 V	2.45 V			0	1	0	1	1
2.61 V	2.55 V			0	1	0	1	0
2.71 V	2.65 V			0	1	0	0	1
2.81 V	2.75 V			0	1	1	1	1
2.92 V	2.86 V			0	1	1	1	0
3.02 V	2.96 V			0	1	1	0	1
3.13 V	3.06 V			0	0	1	0	0
Other than above		Setting prohibited						

- LVD setting (LVDOFF)

Detection voltage		Option byte Setting Value						
V _{LVD}		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
–	–	0/1	1	1	×	×	×	×
Other than above		Setting prohibited						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Remark ×: don't care

21.4 Operation of Voltage Detector

21.4.1 When used as reset mode

- When starting operation

Start in the following initial setting state.

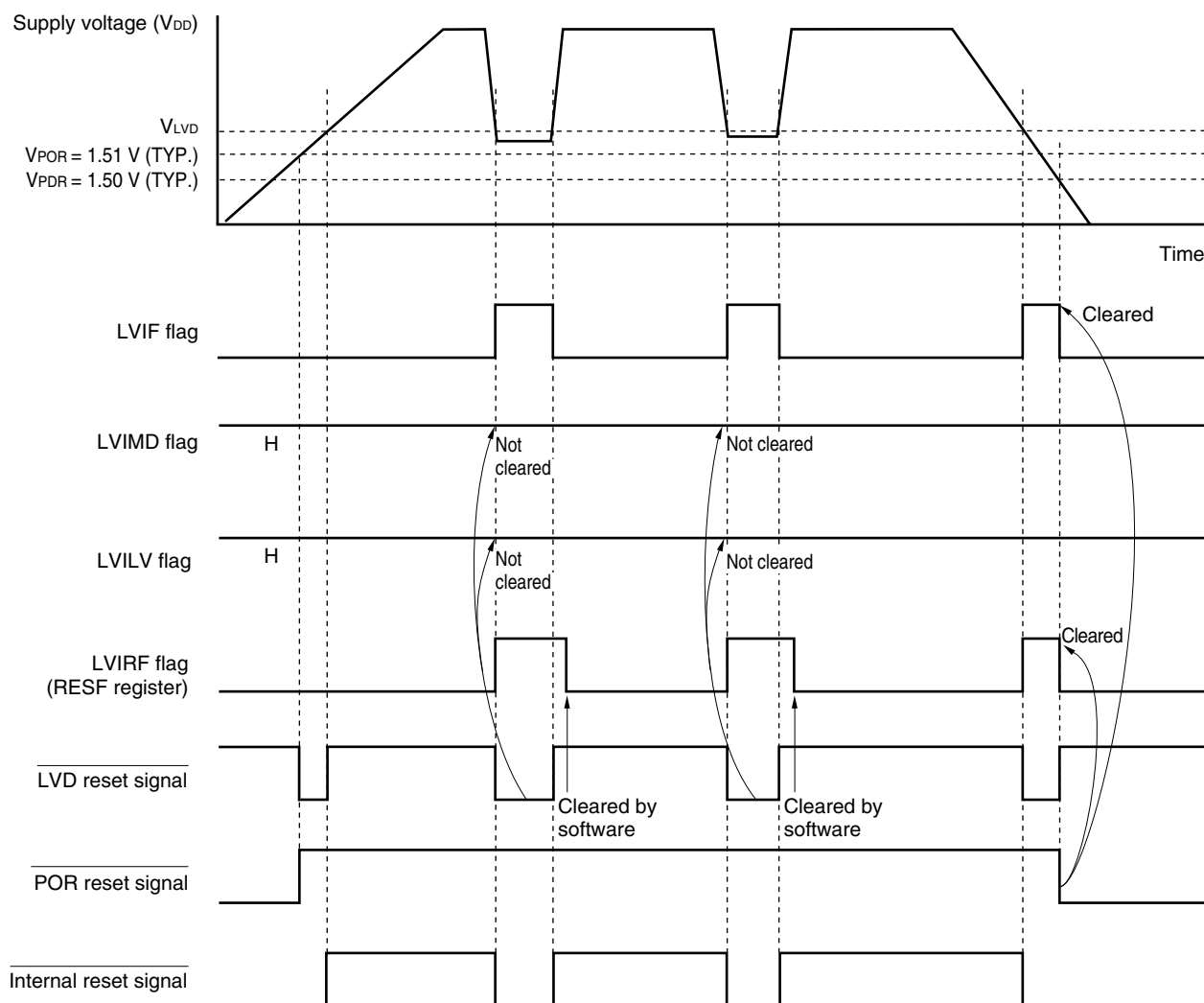
Specify the operation mode (the reset mode (LVIMDS1, LVIMDS0 = 1, 1)) and the detection voltage (V_{LVI}) by using the option byte 000C1H.

- Set bit 7 (LVISEN) of the voltage detection register (LVIM) to 0 (disable rewriting of voltage detection level register (LVIS))
- When the option byte LVIMDS1 and LVIMDS0 are set to 1, the initial value of the LVIS register is set to 81H.
 - Bit 7 (LVIMD) is 1 (reset mode).
 - Bit 0 (LVILV) is 1 (low-voltage detection level: V_{LVD}).

Figure 21-4 shows the timing of the internal reset signal generated by the voltage detector.

<R>

Figure 21-4. Timing of Voltage Detector Internal Reset Signal Generation
 (Option Byte LVIMDS1, LVIMDS0 = 1, 1)



Remark V_{POR} : POR power supply rise detection voltage
 V_{PDR} : POR power supply fall detection voltage

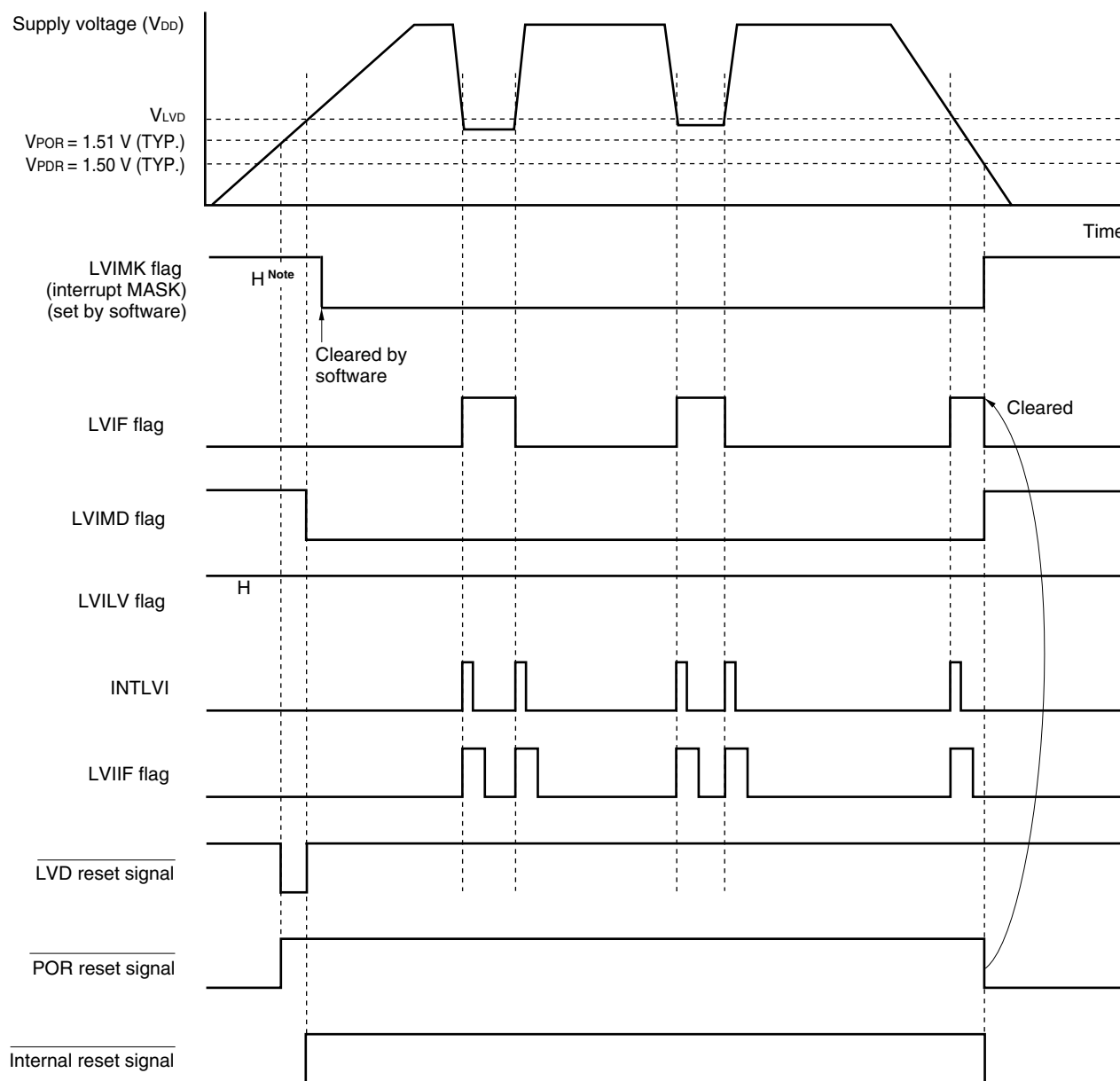
21.4.2 When used as interrupt mode

- When starting operation
Specify the operation mode (the interrupt mode (LVIMDS1, LVIMDS0 = 0, 1)) and the detection voltage (V_{LVD}) by using the option byte 000C1H.
Start in the following initial setting state.
 - Set bit 7 (LVISEN) of the voltage detection register (LVIM) to 0 (disable rewriting of voltage detection level register (LVIS))
 - When the option byte LVIMDS1 is clear to 0 and LVIMDS0 is set to 1, the initial value of the LVIS register is set to 01H.
 - Bit 7 (LVIMD) is 0 (interrupt mode).
 - Bit 0 (LVILV) is 1 (low-voltage detection level: V_{LVD}).

Figure 21-5 shows the timing of the internal interrupt signal generated by the voltage detector.

<R>

Figure 21-5. Timing of Voltage Detector Internal Interrupt Signal Generation
 (Option Byte LVIMDS1, LVIMDS0 = 0, 1)



Note The LVIMK flag is set to "1" by reset signal generation.

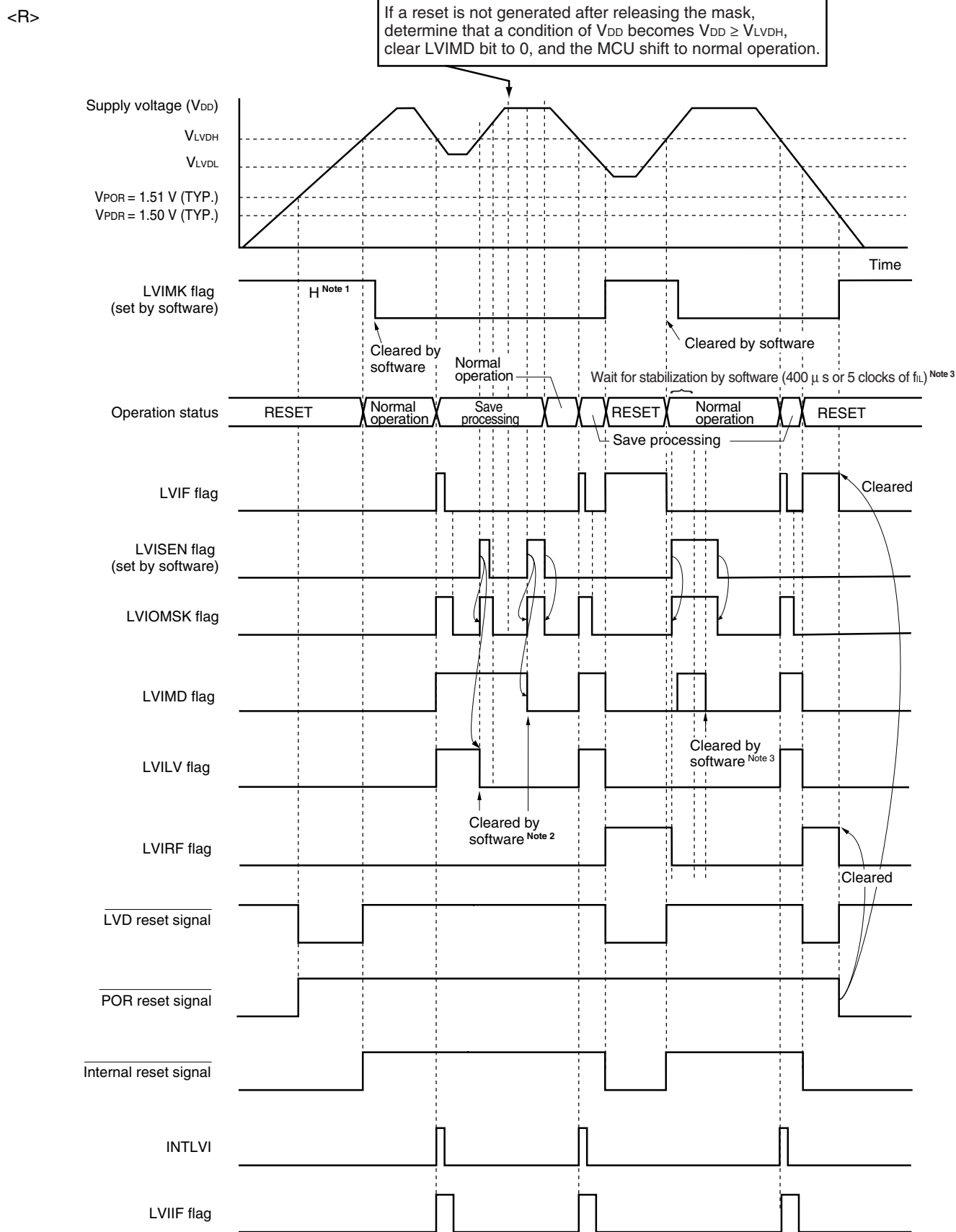
Remark V_{POR} : POR power supply rise detection voltage
 V_{PDR} : POR power supply fall detection voltage

21.4.3 When used as interrupt and reset mode

- When starting operation
Specify the operation mode (the interrupt and reset (LVIMDS1, LVIMDS0 = 1, 0)) and the detection voltage (VLVDH, VLVDL) by using the option byte 000C1H.
Start in the following initial setting state.
 - Set bit 7 (LVISEN) of the voltage detection register (LVIM) to 0 (disable rewriting of voltage detection level register (LVIS))
 - When the option byte LVIMDS1 is set to 1 and LVIMDS0 is clear to 0, the initial value of the LVIS register is set to 00H.
 - Bit 7 (LVIMD) is 0 (interrupt mode).
 - Bit 0 (LVILV) is 0 (high-voltage detection level: VLVDH).

Figure 21-6 shows the timing of the internal reset signal and interrupt signal generated by the voltage detector. Perform the processing according to **figure 21-7 Processing Procedure After an Interrupt Is Generated in interrupt and reset mode** and **figure 21-8 Initial Setting of Interrupt and Reset Mode in interrupt and reset mode**.

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation
(Option Byte LVIMDS1, LVIMDS0 = 1, 0) (1/2)

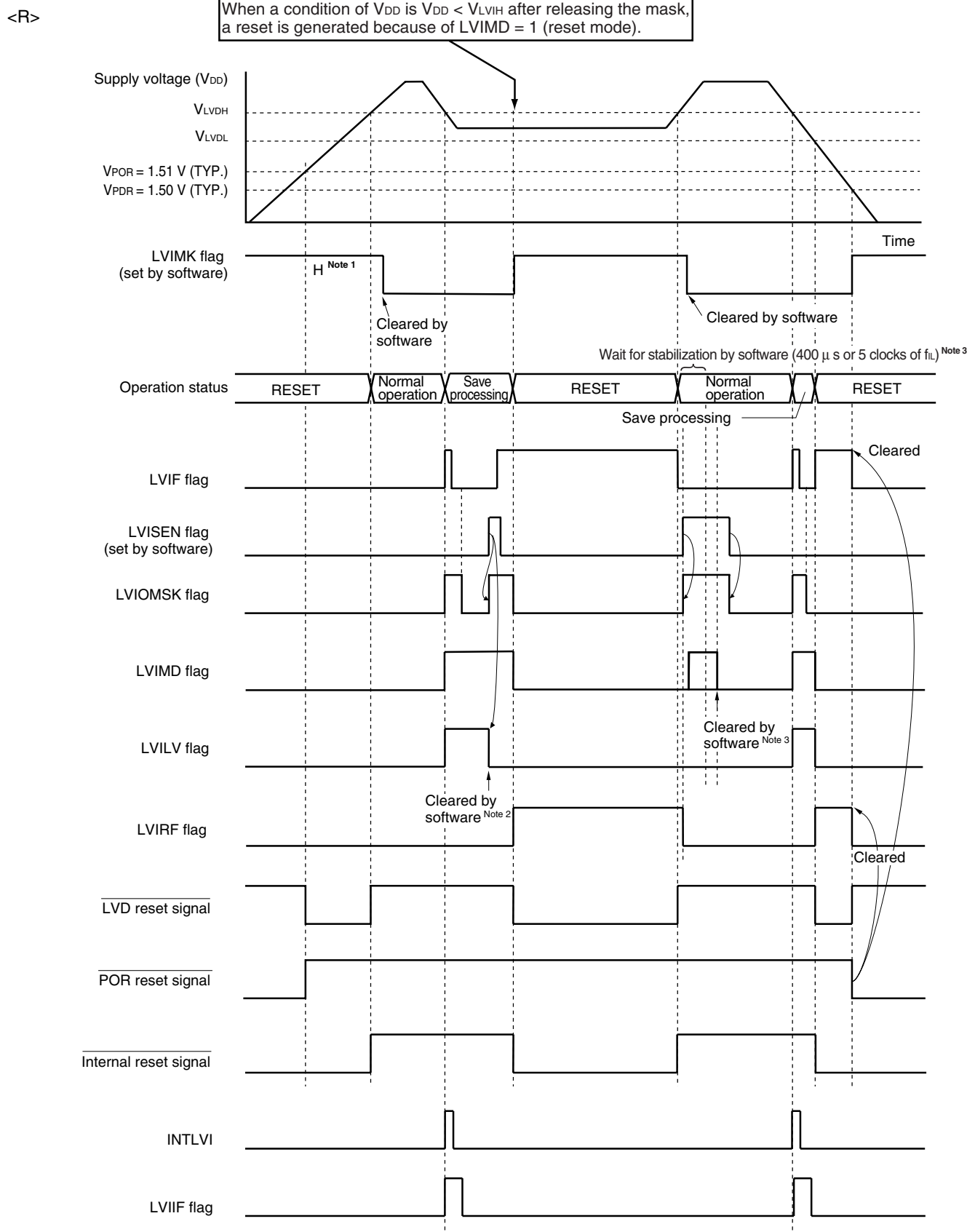


(Notes and Remark are listed on the next page.)

- Notes**
1. The LVIMK flag is set to "1" by reset signal generation.
 2. After an interrupt is generated, perform the processing according to **figure 21-7 Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.**
 3. After a reset is released, perform the processing according to **figure 21-8 Initial Setting of Interrupt and Reset Mode in interrupt and reset mode.**

Remark V_{POR} : POR power supply rise detection voltage
 V_{PDR} : POR power supply fall detection voltage

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation
(Option Byte LVIMDS1, LVIMDS0 = 1, 0) (2/2)

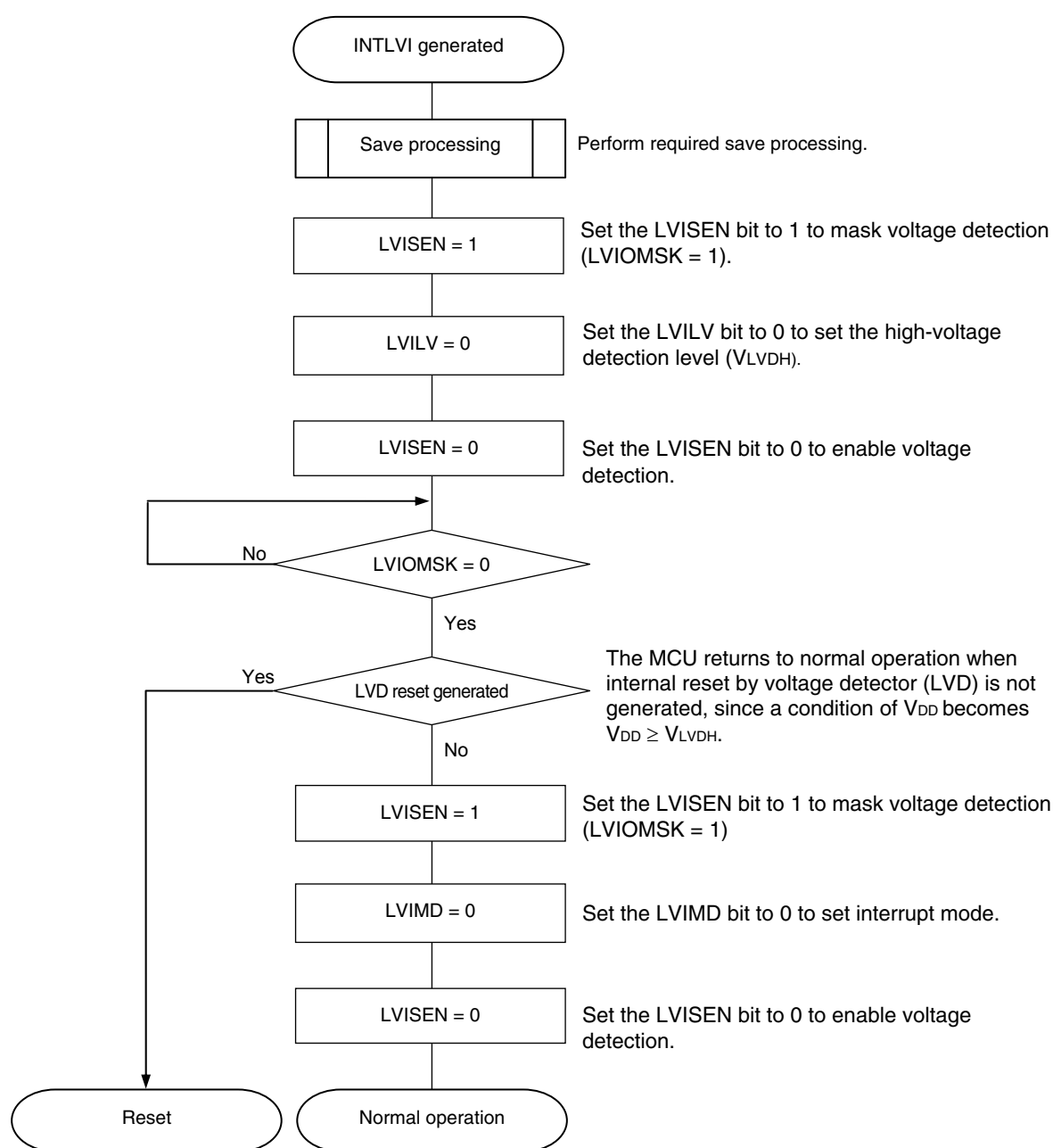


(Notes and Remark are listed on the next page.)

- Notes**
1. The LVIMK flag is set to “1” by reset signal generation.
 2. After an interrupt is generated, perform the processing according to **figure 21-7 Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.**
 3. After a reset is released, perform the processing according to **figure 21-8 Initial Setting of Interrupt and Reset Mode in interrupt and reset mode.**

Remark V_{POR} : POR power supply rise detection voltage
 V_{PDR} : POR power supply fall detection voltage

<R>

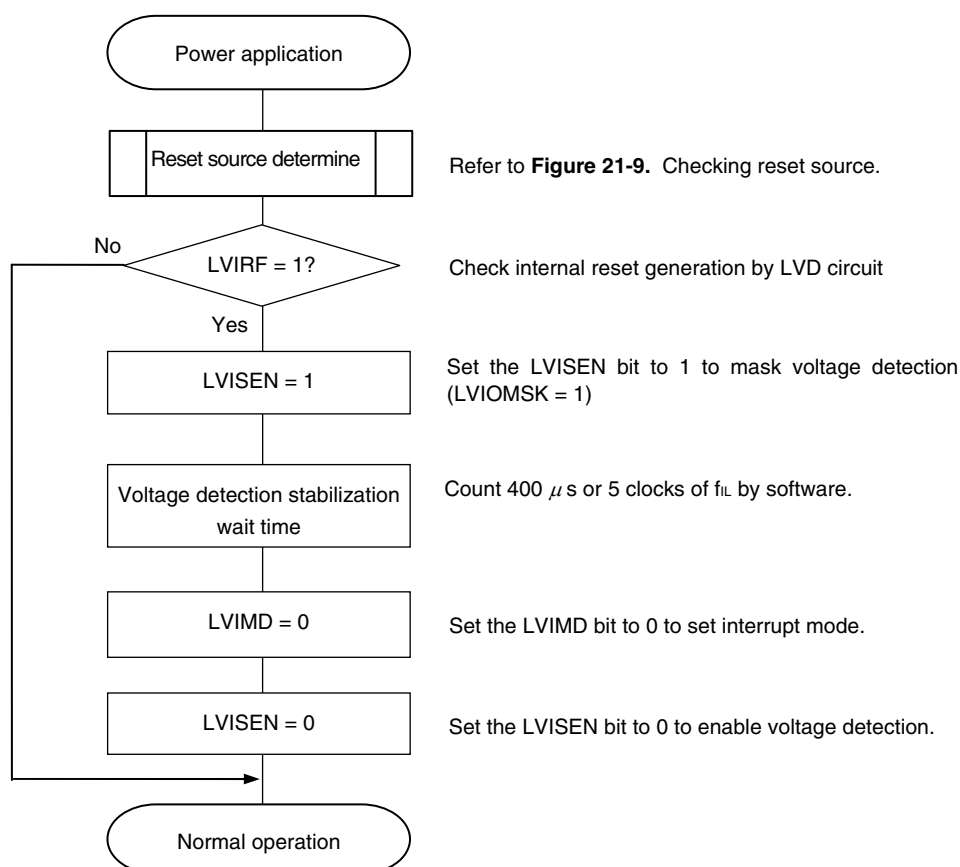
Figure 21-7. Processing Procedure After an Interrupt Is Generated

<R> When setting an interrupt and reset mode (LVIMDS1, LVIMDS0 = 1, 0), voltage detection stabilization wait time for 400 μ s or 5 clocks of f_{IL} is necessary after LVD reset is released (LVIRF = 1). After waiting until voltage detection stabilizes, (0) clear the LVIMD bit for initialization. While voltage detection stabilization wait time is being counted and when the LVIMD bit is rewritten, set LVISEN to 1 to mask a reset or interrupt generation by LVD.

Figure 21-8. shows the procedure for initial setting of interrupt and reset mode.

<R>

Figure 21-8 Initial Setting of Interrupt and Reset Mode



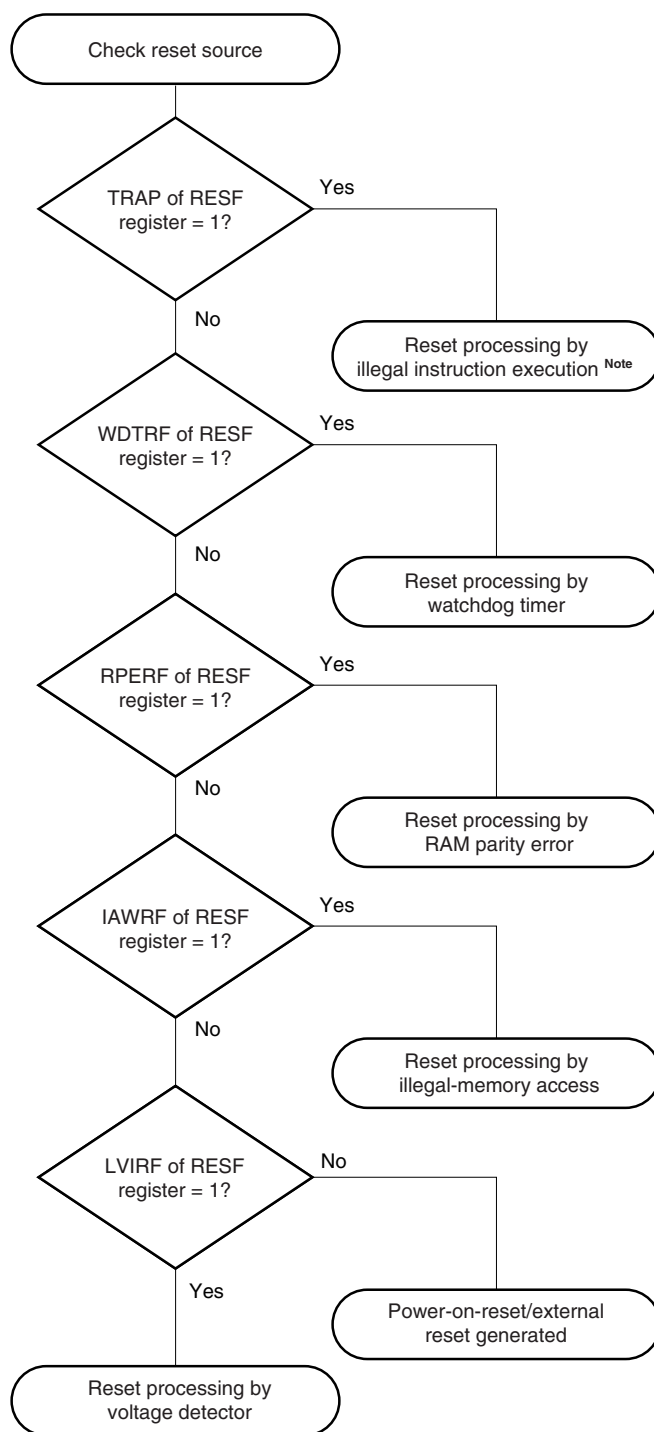
Remark f_{IL} : Low-speed on-chip oscillator clock frequency

21.5 Cautions for Voltage Detector

(1) Checking reset source

When a reset occurs, check the reset source by using the following method.

Figure 21-9. Checking reset source



Note When instruction code FFH is executed.

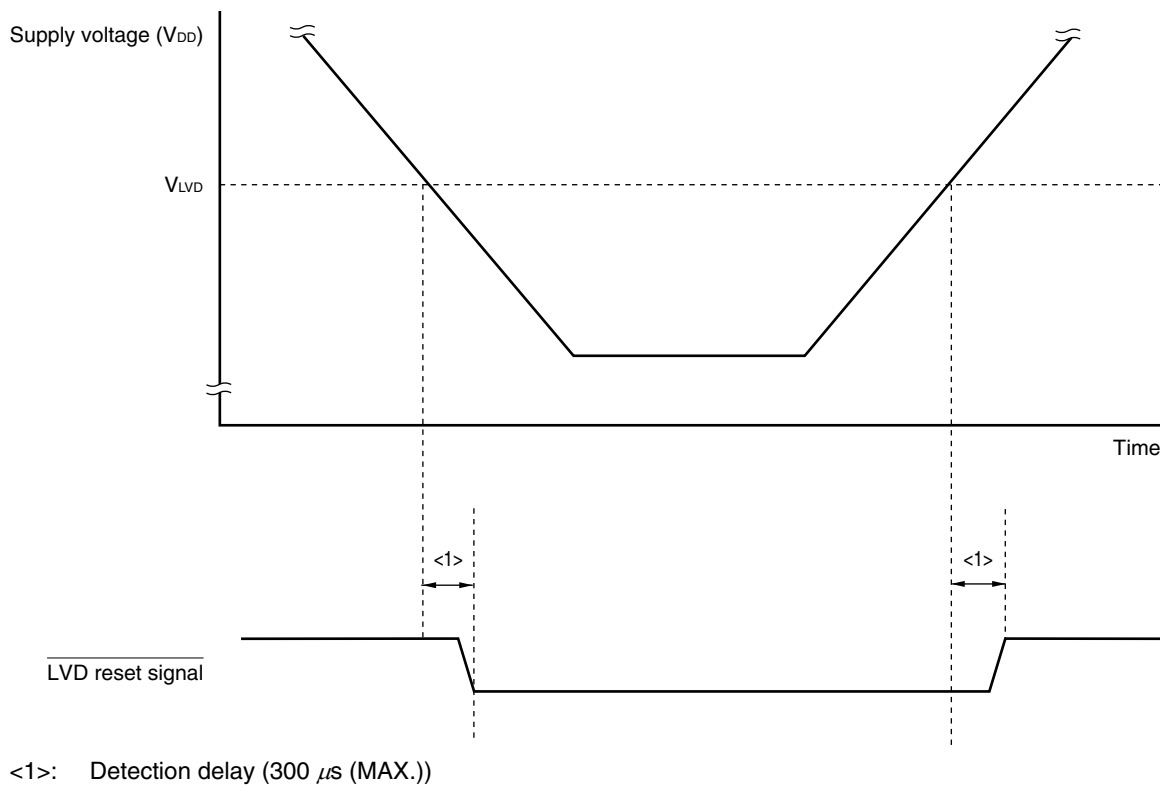
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(2) Delay from the time LVD reset source is generated until the time LVD reset has been generated or released

There is some delay from the time supply voltage (V_{DD}) < LVD detection voltage (V_{LVD}) until the time LVD reset has been generated.

In the same way, there is also some delay from the time LVD detection voltage (V_{LVD}) $\leq$ supply voltage (V_{DD}) until the time LVD reset has been released (see **Figure 21-10**).

Figure 21-10. Delay from the time LVD reset source is generated until the time LVD reset has been generated or released



CHAPTER 22 SAFETY FUNCTIONS

22.1 Overview of Safety Functions

The following safety functions are provided in the RL78/G1A to comply with the IEC60730 and IEC61508 safety standards.

These functions enable the microcontroller to self-diagnose abnormalities and stop operating if an abnormality is detected.

(1) Flash memory CRC operation function (high-speed CRC, general-purpose CRC)

This detects data errors in the flash memory by performing CRC operations.

Two CRC functions are provided in the RL78/G1A that can be used according to the application or purpose of use.

- High-speed CRC: The CPU can be stopped and a high-speed check executed on its entire code flash memory area during the initialization routine.
- General CRC: This can be used for checking various data in addition to the code flash memory area while the CPU is running.

(2) RAM parity error detection function

This detects parity errors when the RAM is read as data.

(3) RAM guard function

This prevents RAM data from being rewritten when the CPU freezes.

(4) SFR guard function

This prevents SFRs from being rewritten when the CPU freezes.

(5) Invalid memory access detection function

This detects illegal accesses to invalid memory areas (such as areas where no memory is allocated and areas to which access is restricted).

(6) Frequency detection function

This uses TAU to detect the oscillation frequency.

(7) A/D test function

This is used to perform a self-check of A/D conversion by performing A/D conversion on the internal reference voltage.

<R> **Remark** See the application note (R01AN0749) for the features required to comply with the IEC60730 standards.

22.2 Registers Used by Safety Functions

The safety functions use the following registers for each function.

Register	Each Function of Safety Function
- Flash memory CRC control register (CRC0CTL) - Flash memory CRC operation result register (PGCRCL)	Flash memory CRC operation function (high-speed CRC)
- CRC input register (CRCIN) - CRC data register (CRCD)	CRC operation function (general-purpose CRC)
RAM parity error control register (RPECTL)	RAM parity error detection function
Invalid memory access detection control register (IAWCTL)	RAM guard function
	SFR guard function
	Invalid memory access detection function
Timer input select register 0 (TIS0)	Frequency detection function
A/D test register (ADTES)	A/D test function

The content of each register is described in **22.3 Operation of Safety Functions**.

22.3 Operation of Safety Functions

22.3.1 Flash memory CRC operation function (high-speed CRC)

The IEC60730 standard mandates the checking of data in the flash memory, and recommends using CRC to do it. The high-speed CRC provided in the RL78/G1A can be used to check the entire code flash memory area during the initialization routine. The high-speed CRC can be executed only when the program is allocated on the RAM and in the HALT mode of the main system clock.

- <R> The high-speed CRC performs an operation by reading 32-bit data per clock from the flash memory while stopping the CPU. This function therefore can finish a check in a shorter time (for example, 512 μ s @ 32 MHz with 64-KB flash memory). The CRC generator polynomial used complies with “ $X^{16} + X^{12} + X^5 + 1$ ” of CRC-16-CCITT. The high-speed CRC operates in MSB first order from bit 31 to bit 0.

- <R> **Caution** The CRC operation result might differ during on-chip debugging because the monitor program is allocated.

Remark The operation result is different between the high-speed CRC and the general CRC, because the general CRC operates in LSB first order.

22.3.1.1 Flash memory CRC control register (CRC0CTL)

This register is used to control the operation of the high-speed CRC ALU, as well as to specify the operation range.

The CRC0CTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22-1. Format of Flash Memory CRC Control Register (CRC0CTL) (1/2)

Address: F02F0H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CRC0CTL	CRC0EN	0	FEA5	FEA4	FEA3	FEA2	FEA1	FEA0

CRC0EN	Control of CRC ALU operation
0	Stop the operation.
1	Start the operation according to HALT instruction execution.

FEA5	FEA4	FEA3	FEA2	FEA1	FEA0	High-speed CRC operation range
0	0	0	0	0	0	0 to 3FFBH (16 K to 4 bytes)
0	0	0	0	0	1	0 to 7FFBH (32 K to 4 bytes)
0	0	0	0	1	0	0 to BFFBH (48 K to 4 bytes)
0	0	0	0	1	1	0 to FFFBH (64 K to 4 bytes)
Other than above						Setting prohibited

Remark Input the expected CRC operation result value to be used for comparison in the lowest 4 bytes of the flash memory. Note that the operation range will thereby be reduced by 4 bytes.

22.3.1.2 Flash memory CRC operation result register (PGCRCL)

This register is used to store the high-speed CRC operation results.

The PGCRCL register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 22-2. Format of Flash Memory CRC Operation Result Register (PGCRCL)

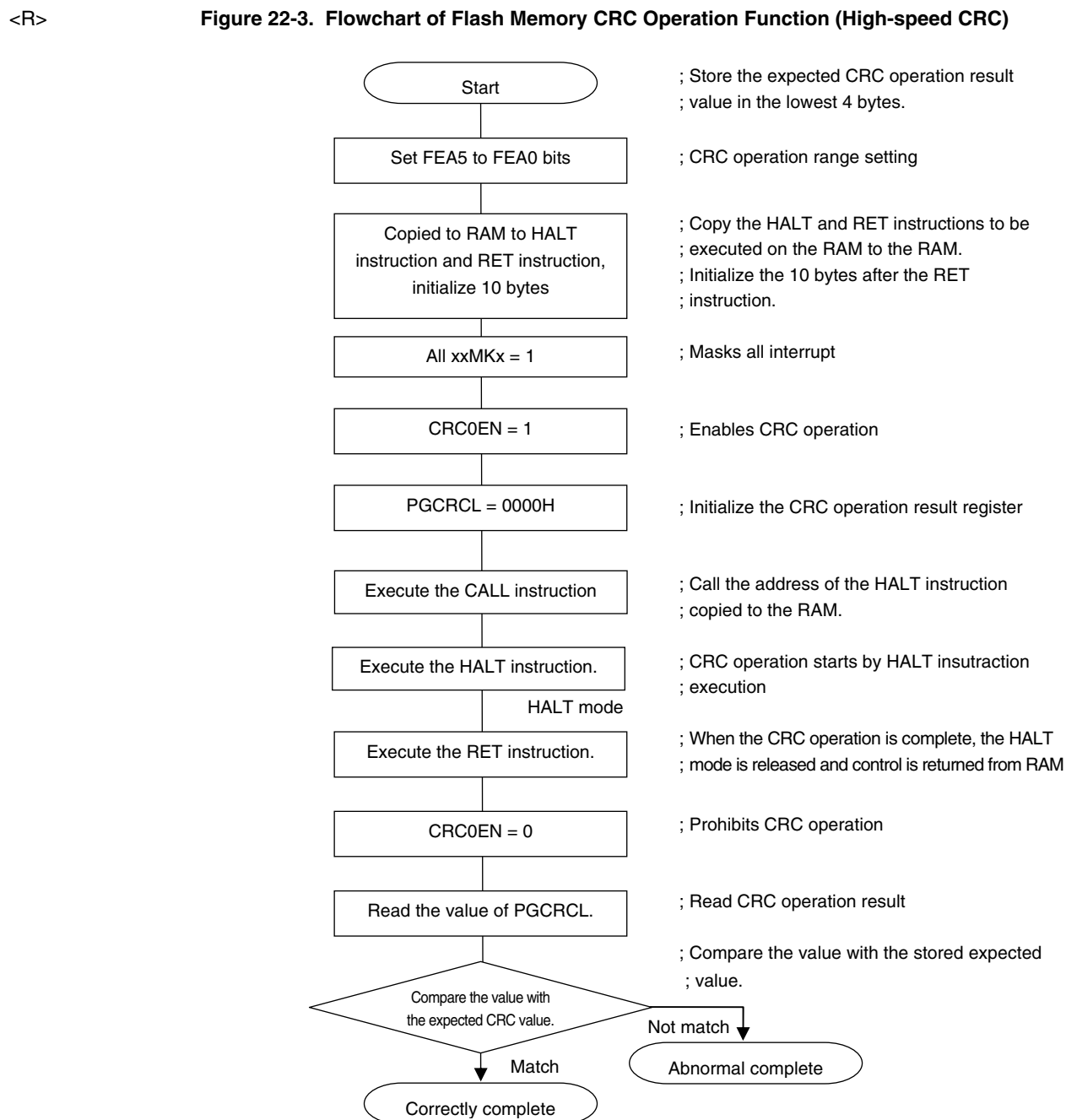
Address: F02F2H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
PGCRCL	PGCRC15	PGCRC14	PGCRC13	PGCRC12	PGCRC11	PGCRC10	PGCRC9	PGCRC8
	7	6	5	4	3	2	1	0
	PGCRC7	PGCRC6	PGCRC5	PGCRC4	PGCRC3	PGCRC2	PGCRC1	PGCRC0
PGCRC15 to 0		High-speed CRC operation results						
0000H to FFFFH		Store the high-speed CRC operation results.						

Caution The PGCRCL register can only be written if CRC0EN (bit 7 of the CRC0CTL register) = 1.

Figure 22-3 shows the flowchart of flash memory CRC operation function (high-speed CRC).

<Operation flow>



- Cautions**
1. The CRC operation is executed only on the code flash.
 2. Store the expected CRC operation value in the area below the operation range in the code flash.
 3. Boot swapping is not performed while the CRC operation is being executed.
 4. The CRC operation is enabled by executing the HALT instruction in the RAM area.
Be sure to execute the HALT instruction in RAM area.

The expected CRC value can be calculated by using tools such as the CubeSuite+ development environment. (See the CubeSuite+ user's manual for details.)

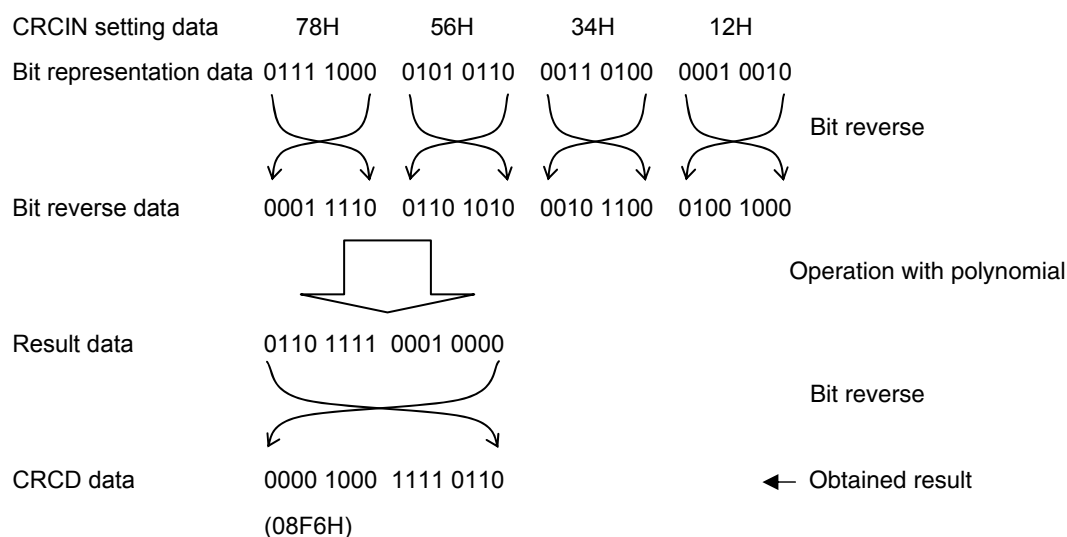
22.3.2 CRC operation function (general-purpose CRC)

In order to guarantee safety during operation, the IEC61508 standard mandates the checking of data even while the CPU is operating.

In the RL78/G1A, a general CRC operation can be executed as a peripheral function while the CPU is operating. The general CRC can be used for checking various data in addition to the code flash memory area. The data to be checked <R> can be specified by using software (a user-created program). CRC calculation function in the HALT mode can be used only during the DMA transmission.

The general CRC operation can be executed in the main system clock operation mode as well as the subsystem clock operation mode.

The CRC generator polynomial used is " $X^{16} + X^{12} + X^5 + 1$ " of CRC-16-CCITT. The data to be input is inverted in bit order and then calculated to allow for LSB-first communication. For example, if the data 12345678H is sent from the LSB, values are written to the CRCIN register in the order of 78H, 56H, 34H, and 12H, enabling a value of 08F6H to be obtained from the CRCD register. This is the result obtained by executing a CRC operation on the bit rows shown below, which consist of the data 12345678H inverted in bit order.



<R> **Caution** Because the debugger rewrites the software break setting line to a break instruction during program execution, the CRC operation result differs if a software break is set in the CRC operation target area.

22.3.2.1 CRC input register (CRCIN)

CRCIN register is an 8-bit register that is used to set the CRC operation data of general-purpose CRC.

The possible setting range is 00H to FFH.

The CRCIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22-4. Format of CRC Input Register (CRCIN)

Address: FFFACH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CRCIN								
Bits 7 to 0				Function				
00H to FFH				Data input.				

22.3.2.2 CRC data register (CRCD)

This register is used to store the CRC operation result of the general-purpose CRC.

The setting range is 0000H to FFFFH.

After 1 clock of CPU/peripheral hardware clock (f_{CLK}) has elapsed from the time CRCIN register is written, the CRC operation result is stored to the CRCD register.

The CRCD register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 22-5. Format of CRC Data Register (CRCD)

Address: F02FAH After reset: 0000H R/W

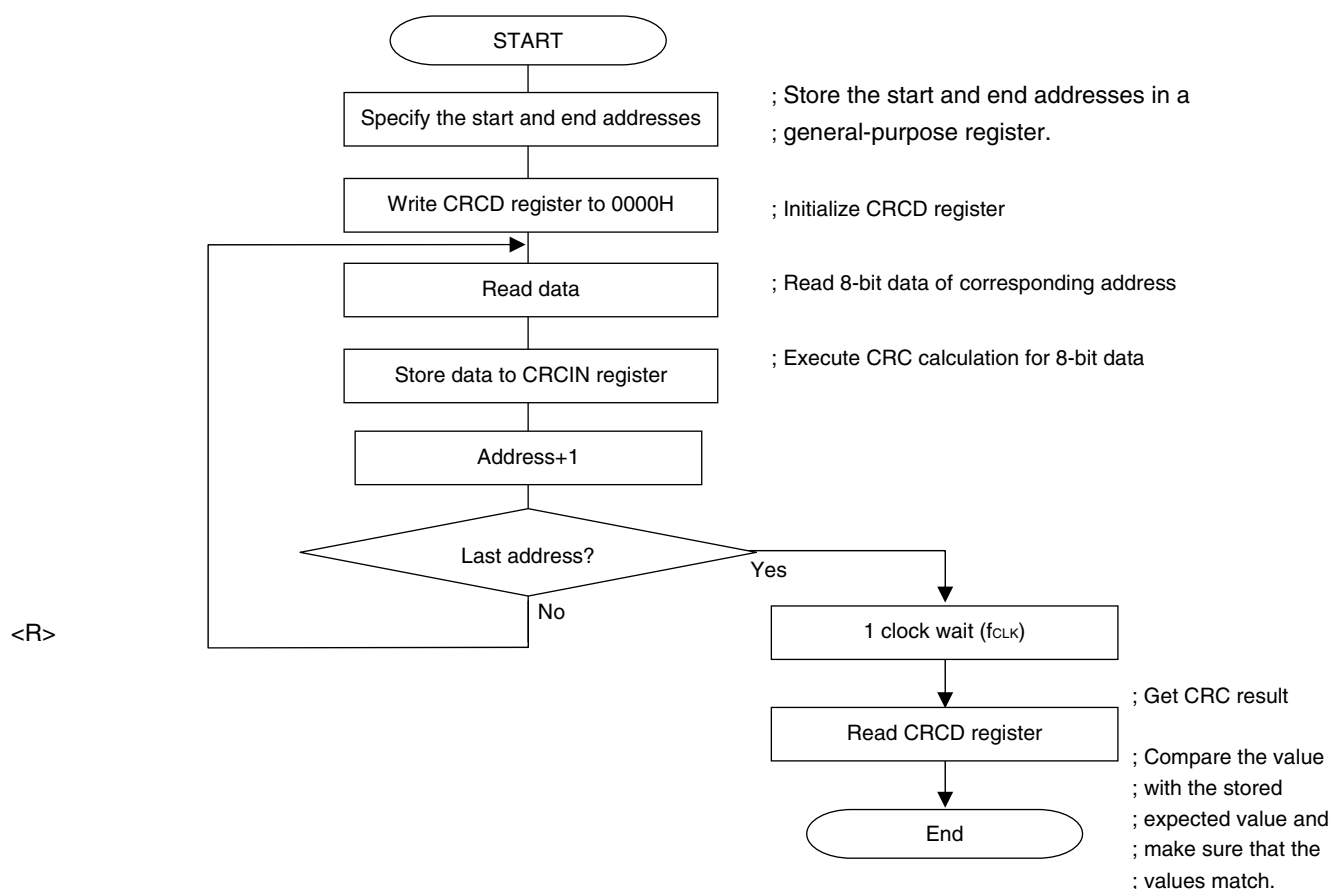
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCD																

Cautions 1. Read the value written to CRCD register before writing to CRCIN register.

2. If conflict between writing and storing operation result to CRCD register occurs, the writing is ignored.

<Operation flow>

Figure 22-6. CRC Operation Function (General-Purpose CRC)



22.3.3 RAM parity error detection function

The IEC60730 standard mandates the checking of RAM data. A single-bit parity bit is therefore added to all 8-bit data in the RL78/G1A's RAM. By using this RAM parity error detection function, the parity bit is appended when data is written, and the parity is checked when the data is read. This function can also be used to trigger a reset when a parity error occurs.

22.3.3.1 RAM parity error control register (RPECTL)

This register is used to control parity error generation check bit and reset generation due to parity errors.

The RPECTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22-7. Format of RAM Parity Error Control Register (RPECTL)

Address: F00F5H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
RPECTL	RPERDIS	0	0	0	0	0	0	RPEF

RPERDIS	Parity error reset mask flag
0	Enable parity error resets.
1	Disable parity error resets.

RPEF	Parity error status flag
0	No parity error has occurred.
1	A parity error has occurred.

<R> Caution The parity is written when the data is written, and checked when the data is read. Therefore, if RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize the RAM area whose data is to be accessed before reading the data. Also, because the CPU in the RL78 performs speculative reading in order to execute pipeline operations, a RAM area that has not been initialized might be read before the RAM area currently being used, causing a RAM parity error. It is therefore important to initialize the RAM area from which to execute instructions + 10 bytes if RAM parity error resets are enabled (RPERDIS = 0). Moreover, if RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize the RAM area to be overwritten + 10 bytes when using the self-programming feature before overwriting the RAM area.

- Remarks**
1. The RAM parity check is always on, and the result can be confirmed by checking the RPEF flag.
 2. The parity error reset is enabled by default (RPERDIS = 0).
Even if the parity error reset is disabled (RPERDIS = 1), the RPEF flag will be set (1) if a parity error occurs.
 3. The RPEF flag is set (1) by RAM parity errors and cleared (0) by writing 0 to it or by any reset source.
When RPEF = 1, the value is retained even if RAM for which no parity error has occurred is read.

22.3.4 RAM guard function

In order to guarantee safety during operation, the IEC61508 standard mandates that important data stored in the RAM be protected, even if the CPU freezes.

This RAM guard function is used to protect data in the specified memory space.

If the RAM guard function is specified, writing to the specified RAM space is disabled, but reading from the space can be carried out as usual.

22.3.4.1 Invalid memory access detection control register (IAWCTL)

This register is used to control the detection of invalid memory access and RAM/SFR guard function.

GRAM1 and GRAM0 bits are used in RAM guard function.

The IAWCTL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22-8. Format of Invalid Memory Access Detection Control Register (IAWCTL)

Address: F0078H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IAWCTL	IAWEN	0	GRAM1	GRAM0	0	GPORT	GINT	GCSC

GRAM1	GRAM0	RAM guard space ^{Note}
0	0	Disabled. RAM can be written to.
0	1	The 128 bytes starting at the lower RAM address
1	0	The 256 bytes starting at the lower RAM address
1	1	The 512 bytes starting at the lower RAM address

Note The RAM start address differs depending on the size of the RAM provided with the product.

22.3.5 SFR guard function

In order to guarantee safety during operation, the IEC61508 standard mandates that important SFRs be protected from being overwritten, even if the CPU freezes.

This SFR guard function is used to protect data in the control registers used by the port function, interrupt function, clock control function, voltage detection function, and RAM parity error detection function.

If the SFR guard function is specified, writing to the specified SFRs is disabled, but reading from the SFRs can be carried out as usual.

22.3.5.1 Invalid memory access detection control register (IAWCTL)

This register is used to control the detection of invalid memory access and RAM/SFR guard function.

GPORT, GINT and GCSC bits are used in SFR guard function.

The IAWCTL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22-9. Format of Invalid Memory Access Detection Control Register (IAWCTL)

Address: F0078H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IAWCTL	IAWEN	0	GRAM1	GRAM0	0	GPORT	GINT	GCSC

GPORT	Control registers of port function guard
0	Disabled. Control registers of port function can be read or written to.
1	Enabled. Writing to control registers of port function is disabled. Reading is enabled. [Guarded SFR] PMxx, PUxx, PIMxx, POMxx, PMCxx, ADPC, PIOR ^{Note 1}

GINT	Registers of interrupt function guard
0	Disabled. Registers of interrupt function can be read or written to.
1	Enabled. Writing to registers of interrupt function is disabled. Reading is enabled. [Guarded SFR] IFxx, MKxx, PRxx, EGPx, EGNx

GCSC ^{Notes 2}	Control registers of clock control function, voltage detector and RAM parity error detection function guard
0	Disabled. Control registers of clock control function, voltage detector and RAM parity error detection function can be read or written to.
1	Enabled. Writing to control registers of clock control function, voltage detector and RAM parity error detection function is disabled. Reading is enabled. [Guarded SFR] CMC, CSC, OSTs, CKC, PERx, OSMC, LVIM, LVIS, RPECTL

Notes 1. Pxx (Port register) is not guarded.

2. Clear GCSC bit to 0, during self programming /serial programming.

22.3.6 Invalid memory access detection function

The IEC60730 standard mandates checking that the CPU and interrupts are operating correctly.

The illegal memory access detection function triggers a reset if a memory space specified as access-prohibited is accessed.

The illegal memory access detection function applies to the areas indicated by NG in Figure 22-10.

Figure 22-10. Invalid access detection area

		Possibility access		Fetching instructions (execute)		
		Read	Write			
FFFFFH	Special function register (SFR) 256 byte	OK	OK	NG		
FFF00H FFEFFFH	General-purpose register 32 byte			OK	OK	
FFE00H FFEDFH	RAM ^{Note}					
yyyyyH	Mirror		NG	NG		
Data flash memory ^{Note 2}						
F1000H F0FFFH	Reserved				OK	OK
F0800H F07FFH	Special function register (2nd SFR) 2 Kbyte					
F0000H EFFFFH	Reserved		NG	NG		
EF000H EEFFFH						
xxxxxH	Code flash memory ^{Note}	OK	OK			
00000H						

Note Code flash memory and RAM address of each product are as follows.

Products	Code flash memory (00000H to xxxxxH)	RAM (yyyyyH to FFEFFH)
R5F10ExA (x = 8, B, G)	16384 × 8 bit (00000H to 03FFFH)	2048 × 8 bit (FF700H to FFEFFH)
R5F10ExC (x = 8, B, G, L)	32768 × 8 bit (00000H to 07FFFH)	2048 × 8 bit (FF700H to FFEFFH)
R5F10ExD (x = 8, B, G, L)	49152 × 8 bit (00000H to 0BFFFH)	3072 × 8 bit (FF300H to FFEFFH)
R5F10ExE (x = 8, B, G, L)	65536 × 8 bit (00000H to 0FFFFH)	4096 × 8 bit (FEF00H to FFEFFH)

22.3.6.1 Invalid memory access detection control register (IAWCTL)

This register is used to control the detection of invalid memory access and RAM/SFR guard function.

IAWEN bit is used in invalid memory access detection function.

The IAWCTL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22-11. Format of Invalid Memory Access Detection Control Register (IAWCTL)

Address: F0078H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IAWCTL	IAWEN	0	GRAM1	GRAM0	0	GPORT	GINT	GCSC

IAWEN ^{Note}	Control of invalid memory access detection
0	Disable the detection of invalid memory access.
1	Enable the detection of invalid memory access.

Note Only writing 1 to the IAWEN bit is enabled, not writing 0 to it after setting it to 1.

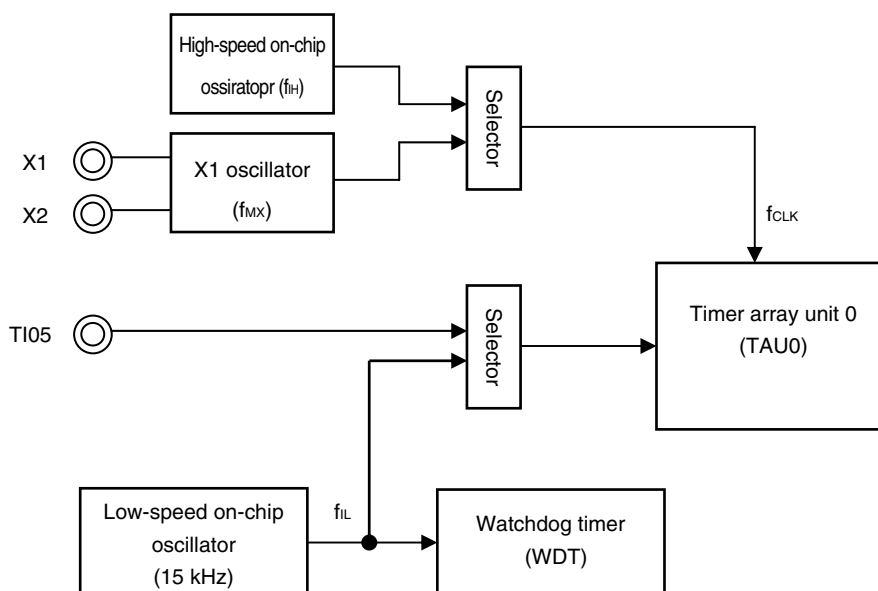
<R> **Remark** By specifying WDTON = 1 for the option byte (watchdog timer operation enable), the invalid memory access function is enabled even IAWEN = 0.

22.3.7 Frequency detection function

The IEC60730 standard mandates checking that the oscillation frequency is correct.

The frequency detection function can detect whether the clock is operating on an abnormal frequency by comparing the internal high-speed oscillation clock or external X1 oscillation clock with the internal low-speed oscillation clock (15 kHz).

Figure 22-12. Configuration of Frequency Detection Function



<Operational overview>

Whether the clock frequency is correct or not can be judged by measuring the pulse interval under the following conditions:

- The internal high-speed oscillation clock (f_H) or the external X1 oscillation clock (f_{MX}) is selected as the CPU/peripheral hardware clock (f_{CLK}).
- The internal low-speed oscillation clock (f_{IL} : 15 kHz) is selected as the timer input for channel 5 of timer array unit 0 (TAU0).

If pulse interval measurement results in an abnormal value, it can be concluded that the clock frequency is abnormal. For how to execute pulse interval measurement, see **6.7.4 Operation as input pulse interval measurement**.

22.3.7.1 Timer input select register 0 (TIS0)

This register is used to select the timer input of channel 5.

By selecting the internal low-speed oscillation clock for the timer input, its pulse interval can be measured to determine whether the proportional relationship between the internal low-speed oscillation clock and the timer operation clock is correct.

The TIS0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22-13. Format of Timer Input Select Register 0 (TIS0)

Address: F0074H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	0	0	0	0	0	TIS02	TIS01	TIS00

TIS02	TIS01	TIS00	Selection of timer input used with channel 5
0	0	0	Input signal of timer input pin (TI05)
0	0	1	
0	1	0	
0	1	1	
1	0	0	Low-speed on-chip oscillator clock (f_{IL})
1	0	1	Subsystem clock (f_{SUB})
Other than the above			Setting prohibited

22.3.8 A/D test function

The IEC60730 standard mandates testing the A/D converter. The A/D test function is used to check whether the A/D converter is operating normally by executing A/D conversions of an internal voltage of 0 V, the AV_{REF} voltage, and the internal reference voltage (1.45 V).

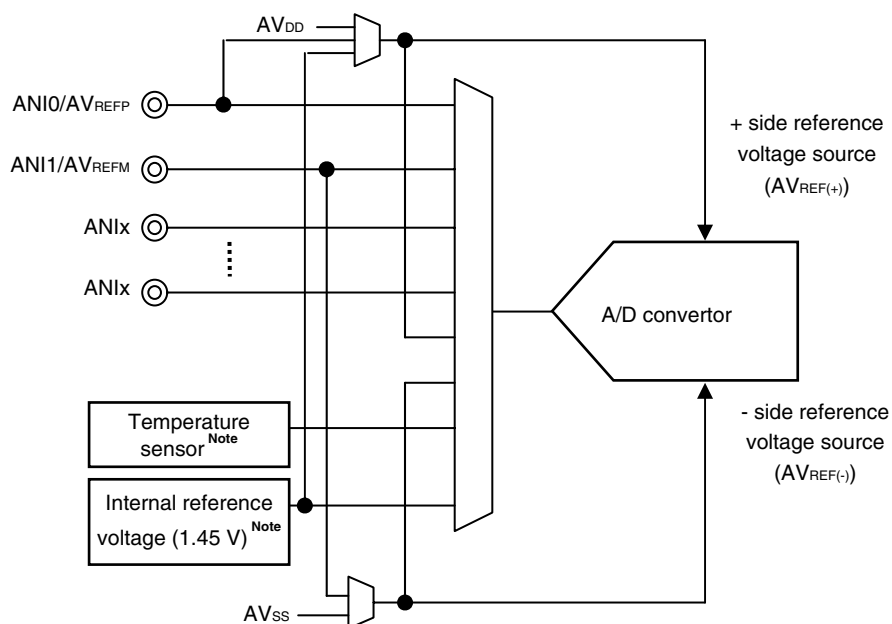
<R> The analog multiplexer can be checked using the following procedure.

- (1) Perform A/D conversion for the ANIx pin (conversion result 1).
- (2) Select – side reference voltage using the ADTES register, perform A/D conversion, and then set the voltage potential difference between the terminals of the sampling capacitor of the A/D converter to 0 V.
- (3) Perform A/D conversion for the ANIx pin (conversion result 2).
- (4) Select + side reference voltage using the ADTES register, perform A/D conversion, and then set the voltage potential difference between the terminals of the sampling capacitor of the A/D converter to AV_{REF} .
- (5) Perform A/D conversion for the ANIx pin (conversion result 3).
- (6) Make sure that conversion results 1, 2, and 3 are equal.

Using the procedure above can confirm that the analog multiplexer is selected and all wiring is connected.

- Remarks 1.** If the analog input voltage is variable during A/D conversion in steps <1> to <5> above, use another method to check the analog multiplexer.
- 2.** The conversion results might contain an error. Consider an appropriate level of error when comparing the conversion results.

Figure 22-14. Configuration of A/D Test Function



Note This setting can be used only in HS (high-speed main) mode. For detail, refer to **Figure 24-3. Format of User Option Byte (000C2H/010C2H).**

22.3.8.1 A/D test register (ADTES)

This register is used to select the + side reference voltage of A/D converter, the – side reference voltage of A/D converter, or the analog input channel (ANLxx) as the target of A/D conversion, as A/D test function.

When using the A/D test function, specify the following settings:

- Select – side reference voltage as the target of A/D conversion when converting the internal 0 V.
- Select + side reference voltage as the target of A/D conversion when converting the AV_{REF} .

The ADTES register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22-15. Format of A/D Test Register (ADTES)

Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

<R>

ADTES1	ADTES0	A/D conversion target
0	0	ANLxx/temperature sensor output ^{Note} /internal reference voltage output (1.45 V) ^{Note} (This is specified using the analog input channel specification register (ADS).)
1	0	– side reference voltage (Setting at ADREFM bit of ADM2 register)
1	1	+ side reference voltage (Setting at ADREFP1, ADREFP0 bits of ADM2 register)
Other than the above		Setting prohibited

<R>

Note Temperature sensor output/internal reference voltage (1.45 V) can be used only in HS (high-speed main) mode. For detail, refer to **Figure 24-3. Format of User Option Byte (000C2H/010C2H)**.

22.3.8.2 Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

<R> Set A/D test register (ADTES) to 00H when measuring the ANIxx/temperature sensor output /internal reference voltage (1.45 V).

The ADS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22-16. Format of Analog Input Channel Specification Register (ADS)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

○ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV _{REFF} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV _{REFM} pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	0	1	0	1	ANI5	P25/ANI5 pin
0	0	0	1	1	0	ANI6	P26/ANI6 pin
0	0	0	1	1	1	ANI7	P27/ANI7 pin
0	0	1	0	0	0	ANI8	P150/ANI8 pin
0	0	1	0	0	1	ANI9	P151/ANI9 pin
0	0	1	0	1	0	ANI10	P152/ANI10 pin
0	0	1	0	1	1	ANI11	P153/ANI11 pin
0	0	1	1	0	0	ANI12	P154/ANI12 pin
0	0	1	1	0	1	Setting prohibited	
0	0	1	1	1	0	Setting prohibited	
0	0	1	1	1	1	Setting prohibited	
0	1	0	0	0	0	ANI16	P03/ANI16 pin
0	1	0	0	0	1	ANI17	P02/ANI17 pin
0	1	0	0	1	0	ANI18	P10/ANI18 pin
0	1	0	0	1	1	ANI19	P120/ANI19 pin
0	1	0	1	0	0	ANI20	P11/ANI20 pin
0	1	0	1	0	1	ANI21	P12/ANI21 pin
0	1	0	1	1	0	ANI22	P13/ANI22 pin
0	1	0	1	1	1	ANI23	P14/ANI23 pin
0	1	1	0	0	0	ANI24	P15/ANI24 pin
0	1	1	0	0	1	ANI25	P51/ANI25 pin
0	1	1	0	1	0	ANI26	P50/ANI26 pin
0	1	1	0	1	1	ANI27	P30/ANI27 pin
0	1	1	1	0	0	ANI28	P70/ANI28 pin
0	1	1	1	0	1	ANI29	P31/ANI29 pin
0	1	1	1	1	0	ANI30	P41/ANI30 pin
0	1	1	1	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output Note
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V) Note
Other than the above						Setting prohibited	

(Note and Cautions are listed on the next page.)

<R> **Note** This setting can be used only in HS (high-speed main) mode. For detail, refer to **Figure 24-3. Format of User Option Byte (000C2H/010C2H)**.

Cautions 1. Be sure to clear bits 5 and 6 to 0.

2. Set a channel to be set the analog input by ADPC and PMC registers in the input mode by using port mode registers 0 to 5, 7, 12, or 15 (PM0 to PM5, PM7, PM12, PM15).
3. Do not set the pin that is set by the A/D port configuration register (ADPC) as digital I/O by the ADS register.
4. Do not set the pin that is set by port mode control register 0, 1, 3 to 5, 7, or 12 (PMC0, PMC1, PMC3 to PMC5, PMC7, PMC12) as digital I/O by the ADS register.
5. Only rewrite the value of the ADISS bit while conversion operation is stopped (which is indicated by the ADCE bit of A/D voltage cooperator mode register 0 (ADM0) being 0).
6. If using AV_{REFP} as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.
7. If using AV_{REFM} as the – side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.
8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source. Also, after setting the ADISS to 1, the result of the first conversion cannot be used. For details about the setting flow, refer to 11.7.4 Setup when using temperature sensor/internal reference voltage (ADISS = 1).
9. Do not set the ADISS bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. Also, if the ADISS bit is set to 1, the temperature sensor operating current (I_{TMPS}) and A/D converter reference voltage current (I_{ADREF}) indicated in 29.3.2 and 30.3.2 Supply current characteristics will be added to the current consumption when shifting to HALT mode while the CPU is operating on the main system clock.

<R>

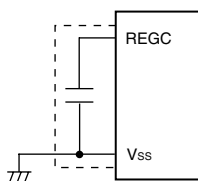
CHAPTER 23 REGULATOR

23.1 Regulator Overview

The RL78/G1A contains a circuit for operating the device with a constant voltage. At this time, in order to stabilize the regulator output voltage, connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

The regulator output voltage, see table 23-1.

<R>



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

Table 23-1. Regulator Output Voltage Conditions

Mode	Output Voltage	Condition
LV (Low voltage main) mode	1.8 V	-
LS (Low-speed main) mode		-
HS (High-speed main) mode	1.8 V	In STOP mode
		When both the high-speed system clock (f _{MX}) and the high-speed on-chip oscillator clock (f _{IH}) are stopped during CPU operation with the subsystem clock (f _{XT})
	2.1 V	When both the high-speed system clock (f _{MX}) and the high-speed on-chip oscillator clock (f _{IH}) are stopped during the HALT mode when the CPU operation with the subsystem clock (f _{XT}) has been set
		Other than above (include during OCD mode) ^{Note}

Note When it shifts to the subsystem clock operation or STOP mode during the on-chip debugging, the regulator output voltage is kept at 2.1 V (not decline to 1.8 V).

CHAPTER 24 OPTION BYTE

24.1 Functions of Option Bytes

Addresses 000C0H to 000C3H of the flash memory of the RL78/G1A form an option byte area.

Option bytes consist of user option byte (000C0H to 000C2H) and on-chip debug option byte (000C3H).

Upon power application or resetting and starting, an option byte is automatically referenced and a specified function is set. When using the product, be sure to set the following functions by using the option bytes.

To use the boot swap operation during self programming, 000C0H to 000C3H are replaced by 010C0H to 010C3H. Therefore, set the same values as 000C0H to 000C3H to 010C0H to 010C3H.

24.1.1 User option byte (000C0H to 000C2H/010C0H to 010C2H)

(1) 000C0H/010C0H

- Operation of watchdog timer
 - Operation is stopped or enabled in the HALT or STOP mode.
- Setting of interval time of watchdog timer
- Operation of watchdog timer
 - Operation is stopped or enabled.
- Setting of window open period of watchdog timer
- Setting of interval interrupt of watchdog timer
 - Used or not used

Caution Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.

(2) 000C1H/010C1H

- Setting of LVD operation mode
 - Interrupt & reset mode.
 - Reset mode.
 - Interrupt mode.
- Setting of LVD detection level (V_{LVDH} , V_{LVDL} , V_{LVD})

Caution Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

(3) 000C2H/010C2H

- Setting of flash operation mode
 - LV (low voltage main) mode
 - LS (low speed main) mode
 - HS (high speed main) mode
- Setting of the frequency of the high-speed on-chip oscillator
 - Select from 1 MHz, 4 MHz, 8 MHz, 12 MHz, 16 MHz, 24 MHz, and 32 MHz.

Caution Set the same value as 000C2H to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

24.1.2 On-chip debug option byte (000C3H/ 010C3H)

- Control of on-chip debug operation
 - On-chip debug operation is disabled or enabled.
- Handling of data of flash memory in case of failure in on-chip debug security ID authentication
 - Data of flash memory is erased or not erased in case of failure in on-chip debug security ID authentication.

Caution Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

24.2 Format of User Option Byte

The format of user option byte is shown below.

Figure 24-1. Format of User Option Byte (000C0H/010C0H)

Address: 000C0H/010C0H^{Note 1}

<R>

7	6	5	4	3	2	1	0
WDTINIT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON
WDTINIT	Use of interval interrupt of watchdog timer						
0	Interval interrupt is not used.						
1	Interval interrupt is generated when 75% + 1/2 f _{IL} of the overflow time is reached.						
WINDOW1	WINDOW0	Watchdog timer window open period ^{Note 2}					
0	0	Setting prohibited					
0	1	50%					
1	0	75%					
1	1	100%					
WDTON	Operation control of watchdog timer counter						
0	Counter operation disabled (counting stopped after reset)						
1	Counter operation enabled (counting started after reset)						
WDCS2	WDCS1	WDCS0	Watchdog timer overflow time (f _{IL} = 17.25 kHz (MAX.))				
0	0	0	2 ⁶ /f _{IL} (3.71 ms)				
0	0	1	2 ⁷ /f _{IL} (7.42 ms)				
0	1	0	2 ⁸ /f _{IL} (14.84 ms)				
0	1	1	2 ⁹ /f _{IL} (29.68 ms)				
1	0	0	2 ¹¹ /f _{IL} (118.72 ms)				
1	0	1	2 ¹³ /f _{IL} (474.90 ms)				
1	1	0	2 ¹⁴ /f _{IL} (949.80 ms)				
1	1	1	2 ¹⁶ /f _{IL} (3799.19 ms)				
WDSTBYON	Operation control of watchdog timer counter (HALT/STOP mode)						
0	Counter operation stopped in HALT/STOP mode ^{Note 2}						
1	Counter operation enabled in HALT/STOP mode						

- Notes**
1. Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.
 2. The window open period is 100% when WDSTBYON = 0, regardless the value of the WINDOW1 and WINDOW0 bits.

Caution The watchdog timer continues its operation during EEPROM emulation. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

Remark f_{IL} : Low-speed on-chip oscillator clock frequency

Figure 24-2. Format of User Option Byte (000C1H/010C1H) (1/2)

Address: 000C1H/010C1H^{Note}

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

• LVD setting (interrupt & reset mode)

Detection voltage			Option byte Setting Value						
VLVDH		VLVDL	Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	Falling edge	LVIMDS1	LVIMDS0					
1.77 V	1.73 V	1.63 V	1	0	0	0	0	1	0
1.88 V	1.84 V							0	1
2.92 V	2.86 V							0	0
1.98 V	1.94 V	1.84 V			0	0	1	1	0
2.09 V	2.04 V							0	1
3.13 V	3.06 V							0	0
2.61 V	2.55 V	2.45 V			0	1	0	1	0
2.71 V	2.65 V							0	1
2.92 V	2.86 V	2.75 V						0	1
3.02 V	2.96 V				0	1			
Other than above			Setting prohibited						

• LVD setting (reset mode)

Detection voltage		Option byte Setting Value						
V _{LVD}		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
1.67 V	1.63 V	1	1	0	0	0	1	1
1.77 V	1.73 V			0	0	0	1	0
1.88 V	1.84 V			0	0	1	1	1
1.98 V	1.94 V			0	0	1	1	0
2.09 V	2.04 V			0	0	1	0	1
2.50 V	2.45 V			0	1	0	1	1
2.61 V	2.55 V			0	1	0	1	0
2.71 V	2.65 V			0	1	0	0	1
2.81 V	2.75 V			0	1	1	1	1
2.92 V	2.86 V			0	1	1	1	0
3.02 V	2.96 V			0	1	1	0	1
3.13 V	3.06 V			0	0	1	0	0
Other than above		Setting prohibited						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Caution Be sure to set bit 4 to “1”.

<R> **Remark** Refer to LVD setting, see 21.1 Functions of Voltage Detector.

Figure 24-2. Format of User Option Byte (000C1H/010C1H) (2/2)Address: 000C1H/010C1H^{Note}

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

- LVD setting (interrupt mode)

Detection voltage		Option byte Setting Value						
V _{LVD}		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
1.67 V	1.63 V	0	1	0	0	0	1	1
1.77 V	1.73 V			0	0	0	1	0
1.88 V	1.84 V			0	0	1	1	1
1.98 V	1.94 V			0	0	1	1	0
2.09 V	2.04 V			0	0	1	0	1
2.50 V	2.45 V			0	1	0	1	1
2.61 V	2.55 V			0	1	0	1	0
2.71 V	2.65 V			0	1	0	0	1
2.81 V	2.75 V			0	1	1	1	1
2.92 V	2.86 V			0	1	1	1	0
3.02 V	2.96 V			0	1	1	0	1
3.13 V	3.06 V			0	0	1	0	0
Other than above		Setting prohibited						

- LVD setting (LVDOFF)

Detection voltage		Option byte Setting Value						
V _{LVD}		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
–	–	0/1	1	1	×	×	×	×
Other than above		Setting prohibited						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Caution Be sure to set bit 4 to “1”.

Remarks 1. ×: don't care

<R>

2. Refer to LVD setting, see **21.1 Functions of Voltage Detector**.

Figure 24-3. Format of User Option Byte (000C2H/010C2H)Address: 000C2H/010C2H^{Note}

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low voltage main) mode	1 to 4 MHz	1.6 to 3.6 V
1	0	LS (low speed main) mode	1 to 8 MHz	1.8 to 3.6 V
1	1	HS (high speed main) mode	1 to 16 MHz	2.4 to 3.6 V
			1 to 32 MHz	2.7 to 3.6 V
Other than above		Setting prohibited		

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
1	0	0	0	32 MHz
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
1	0	1	1	4 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

Note Set the same value as 000C2H to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

24.3 Format of On-chip Debug Option Byte

The format of on-chip debug option byte is shown below.

Figure 24-4. Format of On-chip Debug Option Byte (000C3H/010C3H)

Address: 000C3H/010C3H^{Note}

7	6	5	4	3	2	1	0
OCDENSET	0	0	0	0	1	0	OCDERSD

OCDENSET	OCDERSD	Control of on-chip debug operation
0	0	Disables on-chip debug operation.
0	1	Setting prohibited
1	0	Enables on-chip debugging. Erases data of flash memory in case of failures in authenticating on-chip debug security ID.
1	1	Enables on-chip debugging. Does not erases data of flash memory in case of failures in authenticating on-chip debug security ID.

Note Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

Caution Bits 7 and 0 (OCDENSET and OCDERSD) can only be specified a value.

Be sure to set 000010B to bits 6 to 1.

Remark The value on bits 3 to 1 will be written over when the on-chip debug function is in use and thus it will become unstable after the setting.

However, be sure to set the default values (0, 1, and 0) to bits 3 to 1 at setting.

24.4 Setting of Option Byte

The user option byte and on-chip debug option byte can be set using the assembler linker option, in addition to describing to the source. When doing so, the contents set by using the linker option take precedence, even if descriptions exist in the source, as mentioned below.

A software description example of the option byte setting is shown below.

OPT	CSEG	OPT_BYTE	
	DB	36H	; Does not use interval interrupt of watchdog timer, ; Enables watchdog timer operation, ; Window open period of watchdog timer is 50%, ; Overflow time of watchdog timer is $2^9/f_{IL}$, ; Stops watchdog timer operation during HALT/STOP mode
	DB	1AH	; Select 1.63 V for V_{LVDL} ; Select rising edge 1.77 V, falling edge 1.73 V for V_{LVDH} ; Select the interrupt & reset mode as the LVD operation mode
	DB	2DH	; Select the LV (low voltage main) mode as the flash operation mode and 1 MHz as the frequency of the high-speed on-chip oscillator
	DB	85H	; Enables on-chip debug operation, does not erase flash memory data when security ID authorization fails

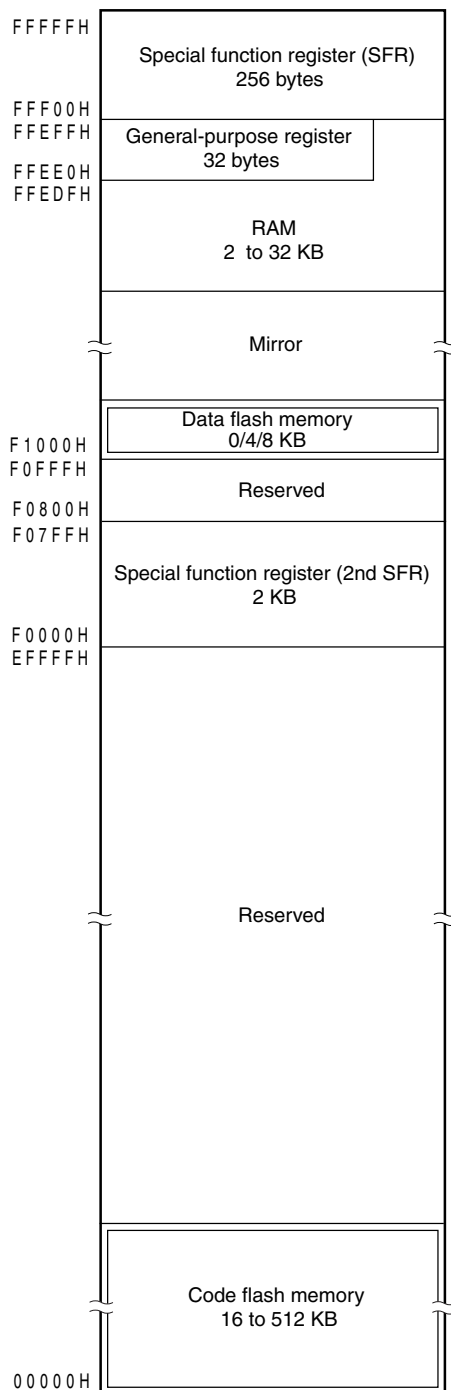
When the boot swap function is used during self programming, 000C0H to 000C3H is switched to 010C0H to 010C3H. Describe to 010C0H to 010C3H, therefore, the same values as 000C0H to 000C3H as follows.

OPT2	CSEG	AT	010C0H	
	DB		36H	; Does not use interval interrupt of watchdog timer, ; Enables watchdog timer operation, ; Window open period of watchdog timer is 50%, ; Overflow time of watchdog timer is $2^9/f_{IL}$, ; Stops watchdog timer operation during HALT/STOP mode
	DB		1AH	; Select 1.63 V for V_{LVDL} ; Select rising edge 1.77 V, falling edge 1.73 V for V_{LVDH} ; Select the interrupt & reset mode as the LVD operation mode
	DB		2DH	; Select the LV (low main voltage) mode as the flash operation mode and 1 MHz as the frequency of the high-speed on-chip oscillator
	DB		85H	; Enables on-chip debug operation, does not erase flash memory data when security ID authorization fails

Caution To specify the option byte by using assembly language, use **OPT_BYTE** as the relocation attribute name of the CSEG pseudo instruction. To specify the option byte to 010C0H to 010C3H in order to use the boot swap function, use the relocation attribute **AT** to specify an absolute address.

CHAPTER 25 FLASH MEMORY

The RL78/G1A incorporates the flash memory to which a program can be written, erased, and overwritten while mounted on the board. The flash memory includes the “code flash memory”, in which programs can be executed, and the “data flash memory”, an area for storing data.



The following three methods for programming the flash memory are available:

- Writing to flash memory by using flash memory programmer (see 25.1)
- Writing to flash memory by using external device (that Incorporates UART) (see 25.2)
- Self-programming (see 25.8)

25.1 Writing to Flash Memory by Using Flash Memory Programmer

The following dedicated flash memory programmer can be used to write data to the internal flash memory of the RL78/G1A.

- PG-FP5, FL-PR5
- E1 on-chip debugging emulator

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the RL78/G1A has been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the RL78/G1A is mounted on the target system.

Remark FL-PR5 and FA series are products of Naito Densetsu Machida Mfg. Co., Ltd.

Table 25-1. Wiring Between RL78/G1A and Dedicated Flash Memory Programmer

Pin Configuration of Dedicated Flash Memory Programmer				Pin Name	Pin No.				
					25-pin	32-pin	48-pin	64-pin	
Signal Name		I/O	Pin Function		FLGA (3x3)	WQFN (5x5)	LQFP (7x7), WQFN (7x7)	LQFP (10x10)	FBGA (4x4)
PG-FP5, FL-PR5	E1 on-chip debugging emulator								
–	TOOL0	I/O	Transmit/receive signal	TOOL0/ P40	A5	1	39	5	D6
SI/RxD	–	I/O	Transmit/receive signal						
SCK	–	Output	–	–	–	–	–	–	–
CLK	–	Output	–	–	–	–	–	–	–
–	RESET	Output	Reset signal	RESET	B5	2	40	6	E7
/RESET	–	Output							
FLMD0	–	Output	Mode signal	–	–	–	–	–	–
V _{DD}		I/O	V _{DD} voltage generation/ power monitoring	V _{DD}	B3	8	48	15	B7
GND		–	Ground	V _{SS}	B2	7	47	13	C7
				EV _{SS0}	–	–	–	14	B8
				REGC ^{Note}	A2	6	46	12	D7
EMV _{DD}		–	Driving power for TOOL pin	V _{DD}	B3	8	48	–	–
				EV _{DD0}	–	–	–	16	A8

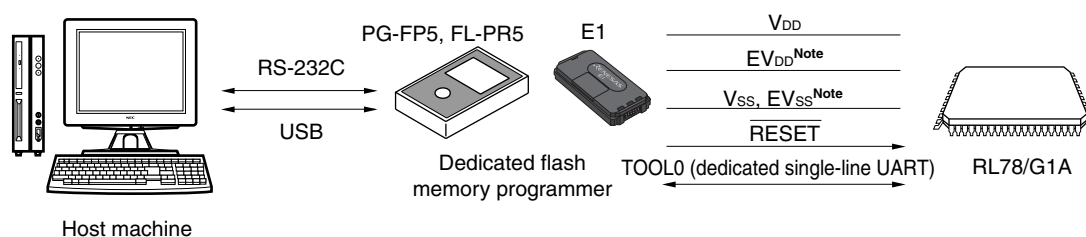
Note Connect REGC pin to ground via a capacitor (default: 0.47 μ F).

Remark Pins that are not indicated in the above table can be left open when using the flash memory programmer for flash programming.

25.1.1 Programming Environment

The environment required for writing a program to the flash memory of the RL78/G1A is illustrated below.

Figure 25-1. Environment for Writing Program to Flash Memory



Note 64-pin products only.

A host machine that controls the dedicated flash memory programmer is necessary.

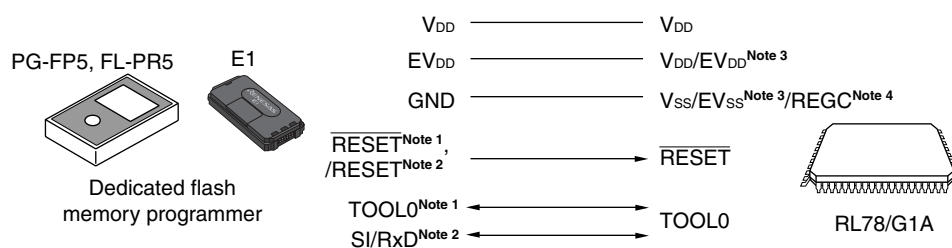
To interface between the dedicated flash memory programmer and the RL78/G1A, the TOOL0 pin is used for <R> manipulation such as writing and erasing via a dedicated single-line UART.

25.1.2 Communication Mode

Communication between the dedicated flash memory programmer and the RL78/G1A is established by serial communication using the TOOL0 pin via a dedicated single-line UART of the RL78/G1A.

Transfer rate: 1 M, 500 k, 250 k, 115.2 kbps

Figure 25-2. Communication with Dedicated Flash Memory Programmer



- Notes**
1. When using E1 on-chip debugging emulator.
 2. When using PG-FP5 or FL-PR5.
 3. 64-pin products only.
 4. Connect REGC pin to ground via a capacitor ((0.47 to 1 μ F).

<R>

The dedicated flash memory programmer generates the following signals for the RL78/G1A. See the manual of PG-FP5, FL-PR5, or E1 on-chip debugging emulator for details.

Table 25-2. Pin Connection

Dedicated Flash Memory Programmer				RL78/G1A	Connection
Signal Name		I/O	Pin Function	Pin Name	
PG-FP5, FL-PR5	E1 on-chip debugging emulator				
FLMD0	—	Output	Mode signal	—	×
V _{DD}		I/O	V _{DD} voltage generation/power monitoring	V _{DD}	⊙
GND		—	Ground	V _{SS} , EV _{SS0} , REGC ^{Note 1}	⊙
EMV _{DD}		—	Driving power for TOOL pin	V _{DD} or EV _{DD0} ^{Note 2}	⊙
CLK	—	Output	Clock output	—	×
/RESET	—	Output	Reset signal	$\overline{\text{RESET}}$	⊙
—	$\overline{\text{RESET}}$	Output			
—	TOOL0	I/O	Transmit/receive signal	TOOL0	⊙
SI/RxD	—	I/O	Transmit/receive signal		
SCK	—	Output	Transfer clock	—	×

- <R> **Notes** 1. Connect REGC pin to ground via a capacitor (0.47 to 1 μ F).
 2. Connection pin is depend on the product.. For detail, see **Table 24-1**.

Remark ○: Be sure to connect the pin.
 ×: The pin does not have to be connected.

25.2 Writing to Flash Memory by Using External Device (that Incorporates UART)

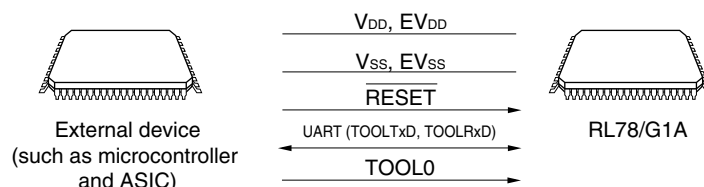
On-board data writing to the internal flash memory is possible by using the RL78/G1A and an external device (a microcontroller or ASIC) connected to a UART.

- <R> On the development of flash memory programmer by user, refer to the **RL78 Microcontrollers (RL78 Protocol A) Programmer Edition Application Note (R01AN0815)**.

25.2.1 Programming Environment

The environment required for writing a program to the flash memory of the RL78/G1A is illustrated below.

Figure 25-3. Environment for Writing Program to Flash Memory



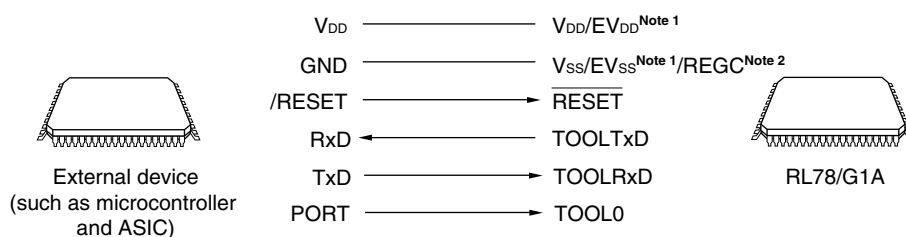
Processing to write data to or delete data from the RL78/G1A by using an external device is performed on-board. Off-board writing is not possible.

25.2.2 Communication Mode

Communication between the external device and the RL78/G1A is established by serial communication using the TOOLTxD and TOOLRxD pins via the dedicated UART of the RL78/G1A.

Transfer rate: 1 M, 500 k, 250 k, 115.2kbps

Figure 25-4. Communication with External Device



Notes 1. 64-pin products only

<R> 2. Connect REGC pin to ground **via** a capacitor (0.47 to 1 μ F).

Caution Make EV_{DD} the same potential as V_{DD}.

The external device generates the following signals for the RL78/G1A.

Table 25-3. Pin Connection

External Device			RL78/G1A	Connection
Signal Name	I/O	Pin Function	Pin Name	
V _{DD}	I/O	V _{DD} voltage generation/power monitoring	V _{DD} , EV _{DD}	⊙
GND	—	Ground	V _{SS} , EV _{SS0} , REGC ^{Note}	⊙
CLK	Output	Clock output	—	×
RESETOUT	Output	Reset signal output	RESET	⊙
RxD	Input	Receive signal	TOOLTxD	⊙
TxD	Output	Transmit signal	TOOLRxD	⊙
PORT	Output	Mode signal	TOOL0	⊙
SCK	Output	Transfer clock	—	×

<R> **Note** Connect REGC pin to ground via a capacitor (0.47 to 1 μ F).

Caution Make EV_{DD} the same potential as V_{DD}.

Remark ⊙: Be sure to connect the pin.

×: The pin does not have to be connected.

25.3 Connection of Pins on Board

To write the flash memory on-board by using the flash memory programmer, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be handled as described below.

<R> **Remark** Refer to flash programming mode, see **25.5.2 Flash memory programming mode**.

25.3.1 P40/TOOL0 pin

In the flash memory programming mode, connect this pin to the dedicated flash memory programmer via an external 1 k Ω pull-up resistor.

When this pin is used as the port pin, use that by the following method.

When used as an input pin: Input of low-level is prohibited for 1 ms period after pin reset release. Furthermore, when this pin is used via pull-down resistors, use the 500 k Ω or more resistors.

When used as an output pin: When this pin is used via pull-down resistors, use the 500 k Ω or more resistors.

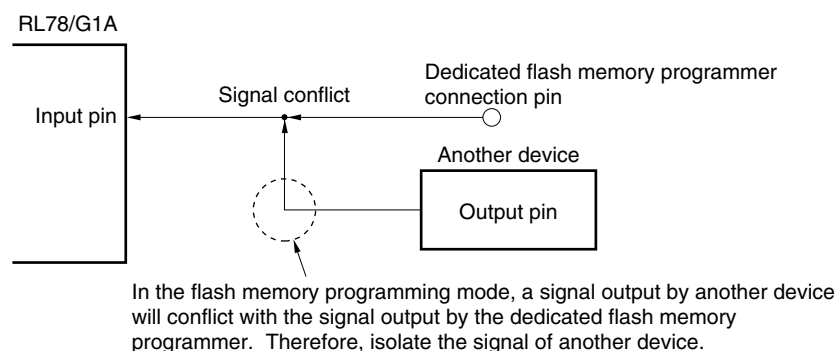
Remark The SAU and IICA pins are not used for communication between the RL78/G1A and dedicated flash memory programmer, because single-line UART (TOOL0 pin) is used.

25.3.2 $\overline{\text{RESET}}$ pin

Signal conflict will occur if the reset signal of the dedicated flash memory programmer and external device are connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board. To prevent this conflict, isolate the connection with the reset signal generator.

The flash memory will not be correctly programmed if the reset signal is input from the user system while the flash memory programming mode is set. Do not input any signal other than the reset signal of the dedicated flash memory programmer and external device.

Figure 25-5. Signal Conflict ($\overline{\text{RESET}}$ Pin)



25.3.3 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to either to V_{DD} or EV_{DD0} or V_{SS} or EV_{SS0} via a resistor.

25.3.4 REGC pin

Connect the REGC pin to GND via a capacitor (0.47 to 1 μ F) in the same manner as during normal operation. Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

25.3.5 X1 and X2 pins

Connect X1 and X2 in the same status as in the normal operation mode.

Remark In the flash memory programming mode, the high-speed on-chip oscillator clock (f_{IH}) is used.

25.3.6 Power supply

To use the supply voltage output of the flash memory programmer, connect the V_{DD} pin to V_{DD} of the flash memory programmer, and the V_{SS} pin to GND of the flash memory programmer.

To use the on-board supply voltage, connect in compliance with the normal operation mode.

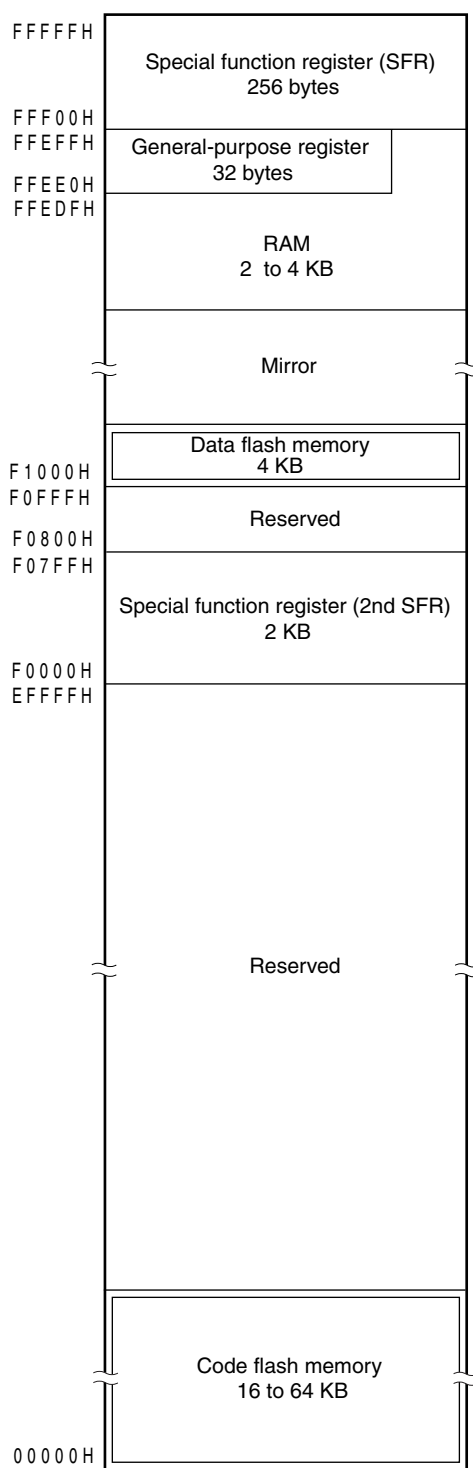
However, when writing to the flash memory by using the flash memory programmer and using the on-board supply voltage, be sure to connect the V_{DD} and V_{SS} pins to V_{DD} and GND of the flash memory programmer to use the power monitor function with the flash memory programmer.

Supply the same other power supplies (EV_{DD0} , EV_{SS0}) as those V_{DD} and V_{SS} .

25.4 Data Flash

25.4.1 Data flash overview

In addition to 16 to 64 KB of code flash memory, the RL78/G1A with data flash includes 4 KB of data flash memory for storing data.



An overview of the data flash memory is provided below. For detail of rewritten of data flash, refer to RL78family data flash library user's manual.

- The data flash memory can be written to by using the flash memory programmer or an external device
 - Programming is performed in 8-bit units
 - Blocks can be deleted in 1 KB units
 - The only access by CPU instructions is byte reading (reading: 1 clock cycle + wait 3 clock cycles)
 - Because the data flash memory is an area exclusively used for data, it cannot be used to execute instructions (code fetching)
 - Instructions can be executed from the code flash memory while rewriting the data flash memory (That is, back ground operation (BGO) is supported)
 - Accessing the data flash memory is not possible while rewriting the code flash memory (during self programming)
 - Because the data flash memory is stopped after a reset ends, the data flash control register (DFLCTL) must be set up in order to use the data flash memory
 - Manipulating the DFLCTL register is not possible while rewriting the data flash memory
- <R> Transition the HALT/STOP status is not possible while rewriting the data flash memory
- <R> **Caution** The data flash memory must be rewritten while the high-speed on-chip oscillator clock is oscillated. If the high-speed on-chip oscillator clock oscillation has stopped, start oscillating the high-speed on-chip oscillator clock (by setting HIOSTOP to 0), let the system wait for 30 us, and then execute the data flash programming library.
- <R> **Remark** Refer to rewriting code flash memory at user program, see **25.8 Flash Memory Programming by Self-Programming**.

25.4.2 Register controlling data flash memory

25.4.2.1 Data flash control register (DFLCTL)

This register is used to enable or disable accessing to the data flash.

The DFLCTL register is set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets this register to 00H.

Figure 25-6. Format of Data Flash Control Register (DFLCTL)

Address: F0090H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
DFLCTL	0	0	0	0	0	0	0	DFLEN

DFLEN	Data flash access control
0	Disables data flash access
1	Enables data flash access

Caution Manipulating the DFLCTL register is not possible while rewriting the data flash memory.

25.4.3 Procedure for accessing data flash memory

The data flash memory is initially stopped after a reset ends and cannot be accessed (read or programmed). To access the memory, perform the following procedure:

<1> Write 1 to bit 0 (DFLEN) of the data flash control register (DFLCTL).

<2> Wait for the setup to finish for software timer.etc.

The time setup takes differs for each main clock mode.

<Setup time for each main clock mode>

- HS (High-speed main): 5 μ s
- LS (Low-speed main): 720 ns
- LV (Low-voltage main): 10 μ s

<3> After the wait, the data flash memory can be accessed.

Cautions 1. Accessing the data flash memory is not possible during the setup time.

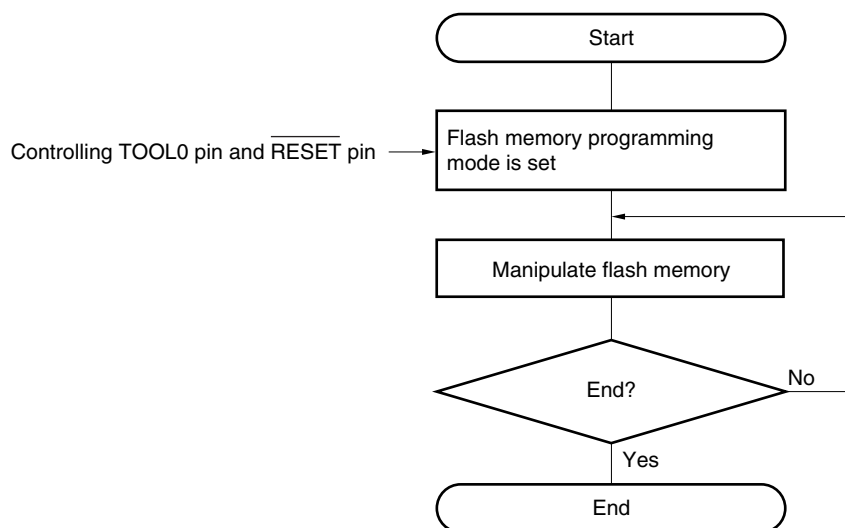
2. Before executing a STOP instruction during the setup time, temporarily clear DFLEN to 0.

25.5 Programming Method

25.5.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

Figure 25-7. Flash Memory Manipulation Procedure



25.5.2 Flash memory programming mode

To rewrite the contents of the flash memory, set the RL78/G1A in the flash memory programming mode. To enter the mode, set as follows.

<When programming by using the dedicated flash memory programmer>

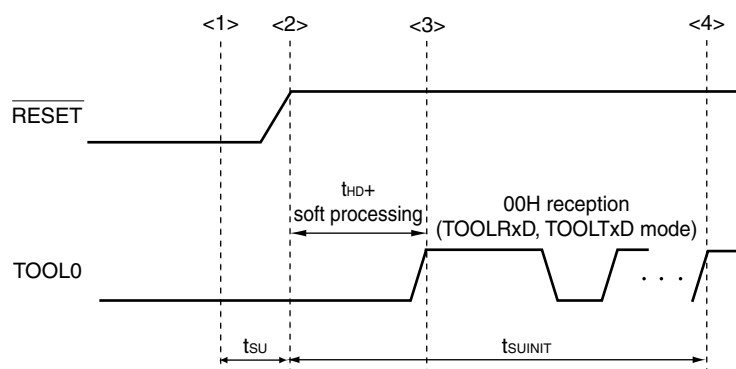
Communication from the dedicated flash memory programmer is performed to automatically switch to the flash memory programming mode.

<When programming by using an external device>

Set the TOOL0 pin to the low level, and then cancel the reset. Keep the TOOL0 pin at the low level from the reset ends to 1 ms + software processing end, and then use UART communication to send the data "00H" from the external device. Finish UART communication within 100 ms after the reset ends.

<R>

Figure 25-8. Setting of Flash Memory Programming Mode



<1> The low level is input to the TOOL0 pin.

<2> The pins reset ends (POR and LVD reset must end before the pin reset ends.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT} : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU} : How long from when the TOOL0 pin is placed at the low level until a pin reset ends

t_{HD} : How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

Table 25-4. Relationship Between TOOL0 Pin and Operation Mode After Reset Release

TOOL0	Operation Mode
EV _{DD0}	Normal operation mode
0	Flash memory programming mode

There are two flash memory programming modes for which the voltage range in which to write, erase, or verify data differs.

Table 25-5. Programming Modes and Voltages at Which Data Can Be Written, Erased, or Verified

Mode	Voltages at which data can be written, erased, or verified	Writing Clock Frequency
Wide voltage mode	1.8 V to 3.6 V	8 MHz (MAX.)
	2.4 V to 3.6 V	16 MHz (MAX.)
	2.7 V to 3.6 V	32 MHz (MAX.)
Full speed mode ^{Note}	2.4 V to 3.6 V	16 MHz (MAX.)
	2.7 V to 3.6 V	32 MHz (MAX.)

Note This can only be specified if the CMODE1 and CMODE0 bits of the option byte 000C2H are 1.

Specify the mode that corresponds to the voltage range in which to write data. When programming by using the dedicated flash memory programmer, the mode is automatically selected by the voltage setting on GUI.

- Remarks 1.** Using both the wide voltage mode and full speed mode imposes no restrictions on writing, deletion, or verification.
- 2.** For details about communication commands, see **25.5.4 Communication commands**.

25.5.3 Selecting communication mode

Communication mode of the RL78/G1A as follows.

Table 25-6. Communication Modes

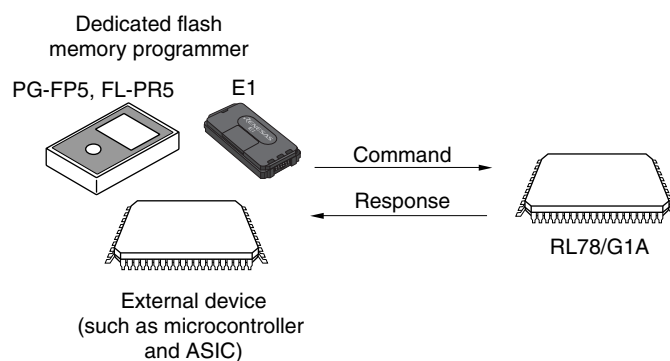
Communication Mode	Standard Setting ^{Note 1}				Pins Used
	Port	Speed ^{Note 2}	Frequency	Multiply Rate	
1-line mode (when flash memory programmer is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	—	—	TOOL0
Dedicated UART (when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	—	—	TOOLTxD, TOOLRx

- Notes 1.** Selection items for Standard settings on GUI of the flash memory programmer.
- 2.** Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

25.5.4 Communication commands

The RL78/G1A communicates with the dedicated flash memory programmer or external device by using commands. The signals sent from the flash memory programmer or external device to the RL78/G1A are called commands, and the signals sent from the RL78/G1A to the dedicated flash memory programmer or external device are called response.

Figure 25-9. Communication Commands



The flash memory control commands of the RL78/G1A are listed in the table below. All these commands are issued from the programmer or external device, and the RL78/G1A perform processing corresponding to the respective commands.

Table 25-7. Flash Memory Control Commands

Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased.
Write	Programming	Writes data to a specified area in the flash memory.
Getting information	Silicon Signature	Gets the RL78/G1A information (such as the part number, flash memory configuration, and programming firmware version).
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
	Security Get	Gets security information.
	Security Release	Release setting of prohibition of writing.
Others	Reset	Used to detect synchronization status of communication.
	Baud Rate Set	Sets baud rate when UART communication mode is selected.

The RL78/G1A returns a response for the command issued by the dedicated flash memory programmer or external device. The response names sent from the RL78/G1A are listed below.

Table 25-8. Response Names

Response Name	Function
ACK	Acknowledges command/data.
NAK	Acknowledges illegal command/data.

25.5.5 Description of signature data

When the “silicon signature” command is performed, the RL78/G1A information (such as the part number, flash memory configuration, and programming firmware version) can be obtained.

Table 25-9 and 25-10 show signature data list and example of signature data list.

Table 25-9. Signature Data List

Field name	Description	Number of transmit data
Device code	The serial number assigned to the device	3 bytes
Device name	Device name (ASCII code)	10 bytes
Code flash memory area last address	Last address of code flash memory area (Sent from lower address. Example. 00000H to 0FFFFH (64 KB) → FFH, 1FH, 00H)	3 bytes
Data flash memory area last address	Last address of data flash memory area (Sent from lower address. Example. F1000H to F1FFFH (4 KB) → FFH, 1FH, 0FH)	3 bytes
Firmware version	Version information of firmware for programming (Sent from upper address. Example. From Ver. 1.23 → 01H, 02H, 03H)	3 bytes

Table 25-10. Example of Signature Data

Field name	Description	Number of transmit data	Data (hexadecimal)
<R> Device code	RL78 protocol A	3 bytes	10 00 06
Device name	RSF10ELE	10 bytes	52 = “R” 35 = “5” 46 = “F” 31 = “1” 30 = “0” 45 = “E” 4C = “L” 45 = “E” 20 = “ ” 20 = “ ”
Code flash memory area last address	Code flash memory area 00000H to 0FFFFH (64 KB)	3 bytes	FF FF 00
Data flash memory area last address	Data flash memory area F1000H to F1FFFH (4 KB)	3 bytes	FF 1F 0F
Firmware version	Ver.1.23	3 bytes	01 02 03

25.6 Security Settings

The RL78/G1A supports a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.

The operations shown below can be performed using the Security Set command.

- Disabling block erase

Execution of the block erase command for a specific block in the flash memory is prohibited during on-board/off-board programming. However, blocks can be erased by means of self programming.

- Disabling write

Execution of the write command for entire blocks in the flash memory is prohibited during on-board/off-board programming. However, blocks can be written by means of self programming.

- Disabling rewriting boot cluster 0

Execution of the block erase command and write command on boot cluster 0 (00000H to 00FFFH) in the flash memory is prohibited by this setting.

<R> After the security settings are specified, releasing the security settings by the Security Release command is enabled by a reset.

The block erase, write commands and rewriting boot cluster 0 are enabled by the default setting when the flash memory is shipped. Security can be set by on-board/off-board programming and self programming. Each security setting can be used in combination.

Table 25-11 shows the relationship between the erase and write commands when the RL78/G1A security function is enabled.

<R> **Caution** The security function of the flash programmer does not support self-programming.

Remark To prohibit writing and erasing during self-programming, use the flash shield window function (see 25.8.2 for detail).

Table 25-11. Relationship Between Enabling Security Function and Command

(1) During on-board/off-board programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of block erase	Blocks cannot be erased.	Can be performed. ^{Note}
Prohibition of writing	Blocks can be erased.	Cannot be performed.
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Note Confirm that no data has been written to the write area. Because data cannot be erased after block erase is prohibited, do not write data if the data has not been erased.

(2) During self programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of block erase	Blocks can be erased.	Can be performed.
Prohibition of writing		
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Remark To prohibit writing and erasing during self-programming, use the flash shield window function (see 25.8.2 for detail).

Table 25-12. Setting Security in Each Programming Mode

(1) On-board/off-board programming

Security	Security Setting	How to Disable Security Setting
Prohibition of block erase	Set via GUI of dedicated flash memory programmer, etc.	Cannot be disabled after set.
Prohibition of writing		Execute security release command
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

Caution The security release command can be applied only when the security is not set as the block erase prohibition and the boot cluster 0 rewrite prohibition with code flash memory area and data flash memory area being blanks.

(2) Self programming

Security	Security Setting	How to Disable Security Setting
Prohibition of block erase	Set by using flash self programming library.	Cannot be disabled after set.
Prohibition of writing		Execute security release command during on-board/off-board programming (cannot be disabled during self programming)
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

<R> **25.7 Processing Time of Each Command When Using PG-FP5 (Reference Values)**

The processing time of each command (reference values) when using PG-FP5 as the dedicated flash memory programmer is shown below.

Table 25-13. Processing Time of Each Command When Using PG-FP5 (Reference Values)

Command of PG-FP5	Port: TOOL0 (UART)			
	Speed: 1M bps			
	16 KB	32 KB	48 KB	64 KB
	R5F10E8A R5F10EBA R5F10EGA	R5F10E8C R5F10EBC R5F10EGC R5F10ELC	R5F10E8D R5F10EBD R5F10EGD R5F10ELD	R5F10E8E R5F10EBE R5F10EGE R5F10ELE
Erase	1 s (TYP.)	1 s (TYP.)	1 s (TYP.)	1.5 s (TYP.)
Program	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)
Verify	1.5 s (TYP.)	1.5 s (TYP.)	2 s (TYP.)	2 s (TYP.)
E.P.	1.5 s (TYP.)	2 s (TYP.)	2.5 s (TYP.)	3 s (TYP.)

25.8 Flash Memory Programming by Self-Programming

The RL78/G1A supports a self-programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the RL78/G1A self-programming library, it can be used to upgrade the program in the field.

- Cautions**
1. The self-programming function cannot be used when the CPU operates with the subsystem clock.
 2. To prohibit an interrupt during self-programming, in the same way as in the normal operation mode, execute the self-programming library in the state where the IE flag is cleared (0) by the DI instruction. To enable an interrupt, clear (0) the interrupt mask flag to accept in the state where the IE flag is set (1) by the EI instruction, and then execute the self-programming library.
 3. While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes. Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 22.3.3 RAM parity error detection function.
 4. The self-programming while the high-speed on-chip oscillator clock is oscillated. If the high-speed on-chip oscillator clock oscillation has stopped, start oscillating the high-speed on-chip oscillator clock (by setting HIOSTOP to 0), let the system wait for 30 us, and then execute the data flash programming library.

- Remarks**
1. For details of the self-programming function and the RL78/G1A self-programming library, refer to **RL78 Microcontroller Self Programming Library Type01 User's Manual (R01AN0350E)**.
 2. For details of the time required to execute self programming, see the notes on use that accompany the flash self programming library tool.

Similar to when writing data by using the flash memory programmer, there are two flash memory programming modes for which the voltage range in which to write, erase, or verify data differs.

Table 25-14. Programming Modes and Voltages at Which Data Can Be Written, Erased, or Verified

Mode	Voltages at which data can be written, erased, or verified	Writing Clock Frequency
Wide voltage mode	1.8 V to 3.6 V	8 MHz (MAX.)
	2.4 V to 3.6 V	16 MHz (MAX.)
	2.7 V to 3.6 V	32 MHz (MAX.)
Full speed mode ^{Note}	2.4 V to 3.6 V	16 MHz (MAX.)
	2.7 V to 3.6 V	32 MHz (MAX.)

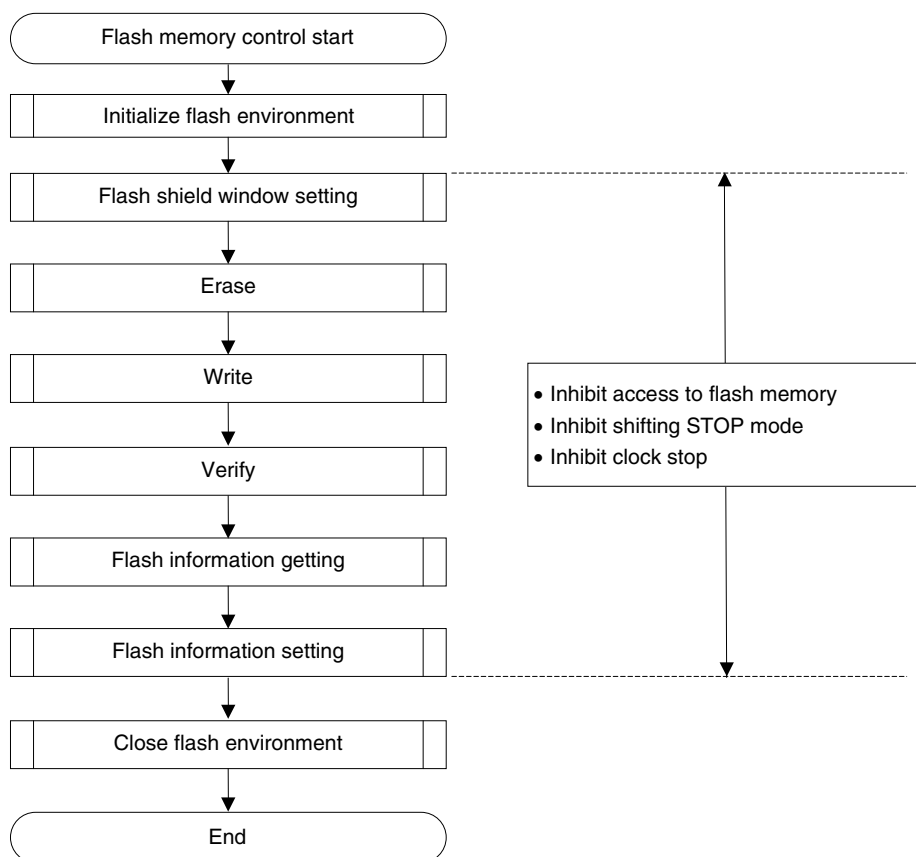
Note This can only be specified if the CMODE1 and CMODE0 bits of the option byte 000C2H are 1.

Specify the mode that corresponds to the voltage range in which to write data. If the argument `fsl_flash_voltage_u08` is other than 00H when the `FSL_Init` function of the self programming library provided by Renesas Electronics is executed, wide-voltage mode is specified. If the argument is 00H, full-speed mode is specified.

- Remarks 1.** Using both the wide voltage mode and full speed mode imposes no restrictions on writing, deletion, or verification.
- 2.** For details of the self-programming function and the RL78/G1A self-programming library, refer to **RL78 Microcontroller Self Programming Library Type01 User's Manual (R01AN0350E)**.

The following figure illustrates a flow of rewriting the flash memory by using a self programming library.

Figure 25-10. Flow of Self Programming (Rewriting Flash Memory)



25.8.1 Boot swap function

If rewriting the boot area failed by temporary power failure or other reasons, restarting a program by resetting or overwriting is disabled due to data destruction in the boot area.

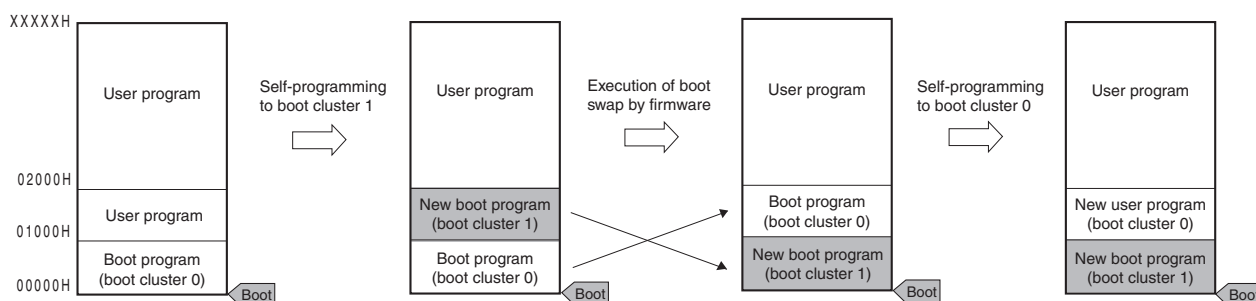
The boot swap function is used to avoid this problem.

Before erasing boot cluster 0^{Note}, which is a boot program area, by self-programming, write a new boot program to boot cluster 1 in advance. When the program has been correctly written to boot cluster 1, swap this boot cluster 1 and boot cluster 0 by using the set information function of the firmware of the RL78/G1A, so that boot cluster 1 is used as a boot area. After that, erase or write the original boot program area, boot cluster 0.

As a result, even if a power failure occurs while the boot programming area is being rewritten, the program is executed correctly because it is booted from boot cluster 1 to be swapped when the program is reset and started next.

Note A boot cluster is a 4 KB area and boot clusters 0 and 1 are swapped by the boot swap function.

Figure 25-11. Boot Swap Function



In an example of above figure, it is as follows.

Boot cluster 0: Boot program area before boot swap

Boot cluster 1: Boot program area after boot swap

Figure 25-12. Example of Executing Boot Swapping



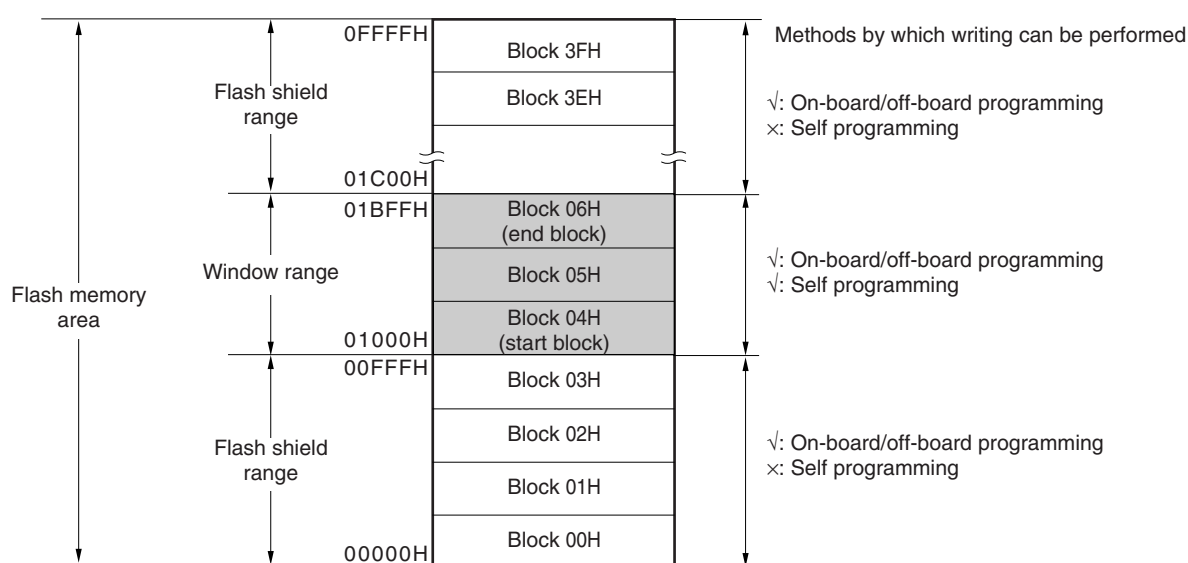
25.8.2 Flash shield window function

The flash shield window function is provided as one of the security functions for self programming. It disables writing to and erasing areas outside the range specified as a window only during self programming.

The window range can be set by specifying the start and end blocks. The window range can be set or changed during both on-board/off-board programming and self programming.

Writing to and erasing areas outside the window range are disabled during self programming. During on-board/off-board programming, however, areas outside the range specified as a window can be written and erased.

Figure 25-13. Flash Shield Window Setting Example
(Target Devices: R5F10ELE, Start Block: 04H, End Block: 06H)



- Cautions**
1. If the rewrite-prohibited area of the boot cluster 0 overlaps with the flash shield window range, prohibition to rewrite the boot cluster 0 takes priority.
 2. The flash shield window can only be used for the code flash memory (and is not supported for the data flash memory).

Table 25-15. Relationship between Flash Shield Window Function Setting/Change Methods and Commands

Programming conditions	Window Range Setting/Change Methods	Execution Commands	
		Block erase	Write
Self-programming	Specify the starting and ending blocks by the flash self programming library.	Block erasing is enabled only within the window range.	Writing is enabled only within the range of window range.
On-board/Off-board programming	Specify the starting and ending blocks on GUI of dedicated flash memory programmer, etc.	Block erasing is enabled also outside the window range.	Writing is enabled also outside the window range.

Remark See 25.6 Security Settings to prohibit writing/erasing during on-board/off-board programming.

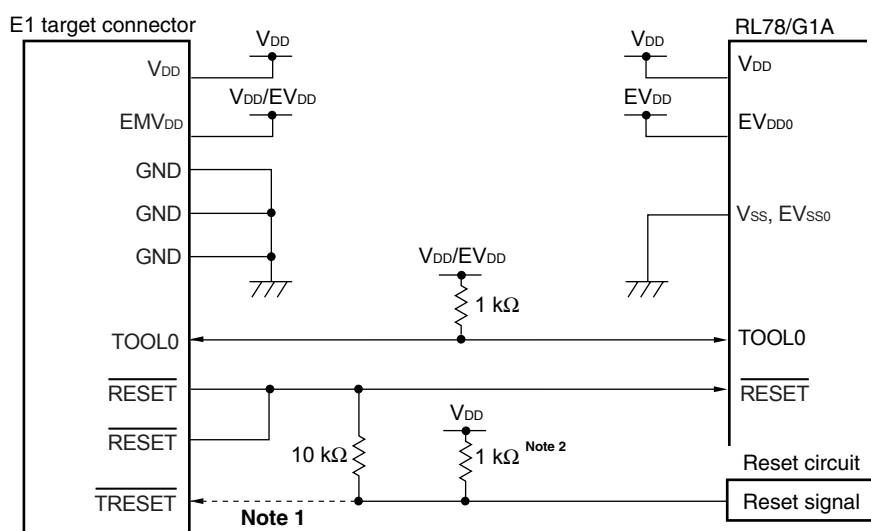
CHAPTER 26 ON-CHIP DEBUG FUNCTION

26.1 Connecting E1 On-chip Debugging Emulator to RL78/G1A

The RL78/G1A uses the V_{DD} , $\overline{\text{RESET}}$, TOOL0, and V_{SS} pins to communicate with the host machine via an E1 on-chip debugging emulator. Serial communication is performed by using a single-line UART that uses the TOOL0 pin.

Caution The RL78/G1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Figure 26-1. Connection Example of E1 On-chip Debugging Emulator and RL78/G1A



Notes 1. Connecting the dotted line is not necessary during flash programming.

2. If the reset circuit on the target system does not have a buffer and generates a reset signal only with resistors and capacitors, this pull-up resistor is not necessary.

Caution This circuit diagram is assumed that the reset signal outputs from an N-ch O.D. buffer (output resistor: 100 Ω or less)

26.2 On-Chip Debug Security ID

The RL78/G1A has an on-chip debug operation control bit in the flash memory at 000C3H (see **CHAPTER 24 OPTION BYTE**) and an on-chip debug security ID setting area at 000C4H to 000CDH, to prevent third parties from reading memory content.

When the boot swap function is used, also set a value that is the same as that of 010C3H and 010C4H to 010CDH in advance, because 000C3H, 000C4H to 000CDH and 010C3H, and 010C4H to 010CDH are switched.

Table 26-1. On-Chip Debug Security ID

Address	On-Chip Debug Security ID
000C4H to 000CDH	Any ID code of 10 bytes
010C4H to 010CDH	

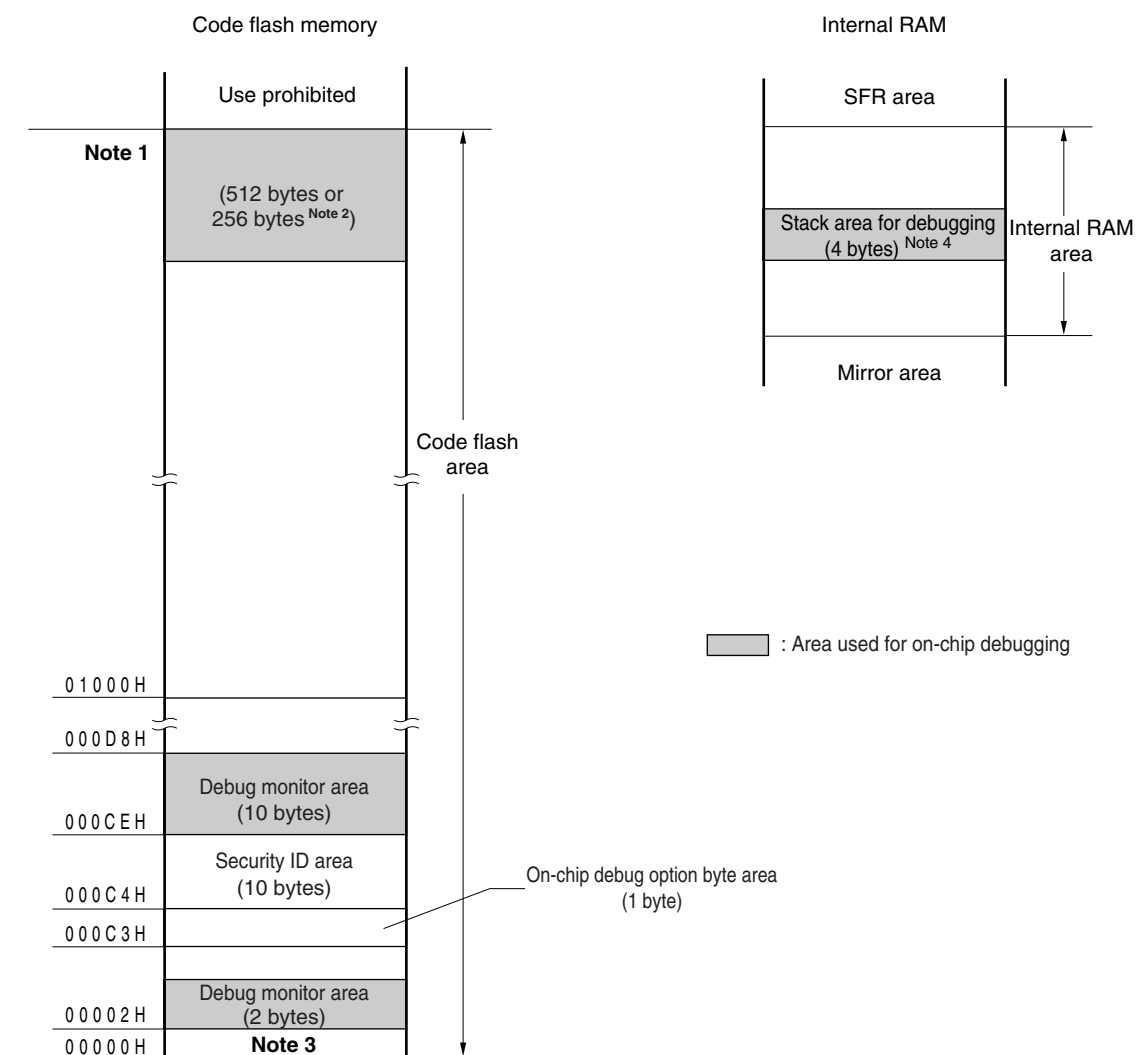
26.3 Securing of User Resources

To perform communication between the RL78/G1A and E1 on-chip debugging emulator, as well as each debug function, the securing of memory space must be done beforehand.

If Renesas Electronics assembler or compiler is used, the items can be set by using linker options.

(1) Securement of memory space

The shaded portions in Figure 26-2 are the areas reserved for placing the debug monitor program, so user programs or data cannot be allocated in these spaces. When using the on-chip debug function, these spaces must be secured so as not to be used by the user program. Moreover, this area must not be rewritten by the user program.

Figure 26-2. Memory Spaces Where Debug Monitor Programs Are Allocated

Notes 1. Address differs depending on products as follows.

Products (code flash memory capacity)	Address of Note 1
R5F10ExA (x = 8, B, G)	03FFFH
R5F10ExC (x = 8, B, G, L)	07FFFH
R5F10ExD (x = 8, B, G, L)	0BFFFH
R5F10ExE (x = 8, B, G, L)	0FFFFH

- When real-time RAM monitor (RRM) function and dynamic memory modification (DMM) function are not used, it is 256 bytes.
- In debugging, reset vector is rewritten to address allocated to a monitor program.
- Since this area is allocated immediately before the stack area, the address of this area varies depending on the stack increase and decrease. That is, 4 extra bytes are consumed for the stack area used. When using self-programming, 12 extra bytes are consumed for the stack area used.

CHAPTER 27 BCD CORRECTION CIRCUIT

27.1 BCD Correction Circuit Function

The result of addition/subtraction of the BCD (binary-coded decimal) code and BCD code can be obtained as BCD code with this circuit.

The decimal correction operation result is obtained by performing addition/subtraction having the A register as the operand and then adding/ subtracting the BCD correction result register (BCDADJ).

27.2 Registers Used by BCD Correction Circuit

The BCD correction circuit uses the following registers.

- BCD correction result register (BCDADJ)

27.2.1 BCD correction result register (BCDADJ)

The BCDADJ register stores correction values for obtaining the add/subtract result as BCD code through add/subtract instructions using the A register as the operand.

The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags.

The BCDADJ register is read by an 8-bit memory manipulation instruction.

Reset input sets this register to undefined.

Figure 27-1. Format of BCD Correction Result Register (BCDADJ)

Address: F00FEH After reset: undefined R

Symbol	7	6	5	4	3	2	1	0
BCDADJ								

27.3 BCD Correction Circuit Operation

The basic operation of the BCD correction circuit is as follows.

(1) Addition: Calculating the result of adding a BCD code value and another BCD code value by using a BCD code value

- <1> The BCD code value to which addition is performed is stored in the A register.
- <2> By adding the value of the A register and the second operand (value of one more BCD code to be added) as are in binary, the binary operation result is stored in the A register and the correction value is stored in the BCD correction result register (BCDADJ).
- <3> Decimal correction is performed by adding in binary the value of the A register (addition result in binary) and the BCDADJ register (correction value), and the correction result is stored in the A register and CY flag.

Caution The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags. Therefore, execute the instruction <3> after the instruction <2> instead of executing any other instructions. To perform BCD correction in the interrupt enabled state, saving and restoring the A register is required within the interrupt function. PSW (CY flag and AC flag) is restored by the RETI instruction.

An example is shown below.

Examples 1: $99 + 89 = 188$

Instruction	A Register	CY Flag	AC Flag	BCDADJ Register
MOV A, #99H ; <1>	99H	–	–	–
ADD A, #89H ; <2>	22H	1	1	66H
ADD A, !BCDADJ ; <3>	88H	1	0	–

Examples 2: $85 + 15 = 100$

Instruction	A Register	CY Flag	AC Flag	BCDADJ Register
MOV A, #85H ; <1>	85H	–	–	–
ADD A, #15H ; <2>	9AH	0	0	66H
ADD A, !BCDADJ ; <3>	00H	1	1	–

Examples 3: $80 + 80 = 160$

Instruction	A Register	CY Flag	AC Flag	BCDADJ Register
MOV A, #80H ; <1>	80H	–	–	–
ADD A, #80H ; <2>	00H	1	0	60H
ADD A, !BCDADJ ; <3>	60H	1	0	–

(2) Subtraction: Calculating the result of subtracting a BCD code value from another BCD code value by using a BCD code value

- <1> The BCD code value from which subtraction is performed is stored in the A register.
- <2> By subtracting the value of the second operand (value of BCD code to be subtracted) from the A register as is in binary, the calculation result in binary is stored in the A register, and the correction value is stored in the BCD correction result register (BCDADJ).
- <3> Decimal correction is performed by subtracting the value of the BCDADJ register (correction value) from the A register (subtraction result in binary) in binary, and the correction result is stored in the A register and CY flag.

Caution The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags. Therefore, execute the instruction <3> after the instruction <2> instead of executing any other instructions. To perform BCD correction in the interrupt enabled state, saving and restoring the A register is required within the interrupt function. PSW (CY flag and AC flag) is restored by the RETI instruction.

An example is shown below.

Example: $91 - 52 = 39$

Instruction	A Register	CY Flag	AC Flag	BCDADJ Register
MOV A, #91H ; <1>	91H	–	–	–
SUB A, #52H ; <2>	3FH	0	1	06H
SUB A, !BCDADJ ; <3>	39H	0	0	–

CHAPTER 28 INSTRUCTION SET

This chapter lists the instructions in the RL78 microcontroller instruction set. For details of each operation and operation code, refer to the separate document **RL78 Microcontrollers User's Manual: software**.

28.1 Conventions Used in Operation List

28.1.1 Operand identifiers and specification methods

Operands are described in the “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, !!, \$, \$!, [], and ES: are keywords and are described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: 16-bit absolute address specification
- !!: 20-bit absolute address specification
- \$: 8-bit relative address specification
- \$!: 16-bit relative address specification
- []: Indirect address specification
- ES:: Extension address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, !!, \$, \$!, [], and ES: symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 28-1. Operand Identifiers and Specification Methods

Identifier	Description Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special-function register symbol (SFR symbol) FFF00H to FFFFFH
sfrp	Special-function register symbols (16-bit manipulatable SFR symbol. Even addresses only ^{Note}) FFF00H to FFFFFH
saddr	FFE20H to FFF1FH Immediate data or labels
saddrp	FFE20H to FF1FH Immediate data or labels (even addresses only ^{Note})
addr20	00000H to FFFFFH Immediate data or labels
addr16	0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions ^{Note})
addr5	0080H to 00BFH Immediate data or labels (even addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
RBn	RB0 to RB3

Note Bit 0 = 0 when an odd address is specified.

Remark The special function registers can be described to operand sfr as symbols. See **Table 3-5 SFR List** for the symbols of the special function registers. The extended special function registers can be described to operand !addr16 as symbols. See **Table 3-6 Extended SFR (2nd SFR) List** for the symbols of the extended special function registers.

28.1.2 Description of operation column

The operation when the instruction is executed is shown in the “Operation” column using the following symbols.

Table 28-2. Symbols in “Operation” Column

Symbol	Function
A	A register; 8-bit accumulator
X	X register
B	B register
C	C register
D	D register
E	E register
H	H register
L	L register
ES	ES register
CS	CS register
AX	AX register pair; 16-bit accumulator
BC	BC register pair
DE	DE register pair
HL	HL register pair
PC	Program counter
SP	Stack pointer
PSW	Program status word
CY	Carry flag
AC	Auxiliary carry flag
Z	Zero flag
RBS	Register bank select flag
IE	Interrupt request enable flag
()	Memory contents indicated by address or register contents in parentheses
X _H , X _L	16-bit registers: X _H = higher 8 bits, X _L = lower 8 bits
X _S , X _H , X _L	20-bit registers: X _S = (bits 19 to 16), X _H = (bits 15 to 8), X _L = (bits 7 to 0)
∧	Logical product (AND)
∨	Logical sum (OR)
⊕	Exclusive logical sum (exclusive OR)
—	Inverted data
addr5	16-bit immediate data (even addresses only in 0080H to 00BFH)
addr16	16-bit immediate data
addr20	20-bit immediate data
jdisp8	Signed 8-bit data (displacement value)
jdisp16	Signed 16-bit data (displacement value)

28.1.3 Description of flag operation column

The change of the flag value when the instruction is executed is shown in the “Flag” column using the following symbols.

Table 28-3. Symbols in “Flag” Column

Symbol	Change of Flag Value
(Blank)	Unchanged
0	Cleared to 0
1	Set to 1
×	Set/cleared according to the result
R	Previously saved value is restored

28.1.4 PREFIX instruction

Instructions with “ES:” have a PREFIX operation code as a prefix to extend the accessible data area to the 1 MB space (00000H to FFFFFH), by adding the ES register value to the 64 KB space from F0000H to FFFFFH. When a PREFIX operation code is attached as a prefix to the target instruction, only one instruction immediately after the PREFIX operation code is executed as the addresses with the ES register value added.

A interrupt and DMA transfer are not acknowledged between a PREFIX instruction code and the instruction immediately after.

Table 28-4. Use Example of PREFIX Operation Code

Instruction	Opcode				
	1	2	3	4	5
MOV !addr16, #byte	CFH	!addr16		#byte	–
MOV ES:!addr16, #byte	11H	CFH	!addr16		#byte
MOV A, [HL]	8BH	–	–	–	–
MOV A, ES:[HL]	11H	8BH	–	–	–

Caution Set the ES register value with MOV ES, A, etc., before executing the PREFIX instruction.

28.2 Operation List

Table 28-5. Operation List (1/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	MOV	r, #byte	2	1	–	$r \leftarrow \text{byte}$			
		PSW, #byte	3	3	–	$\text{PSW} \leftarrow \text{byte}$	×	×	×
		CS, #byte	3	1	–	$\text{CS} \leftarrow \text{byte}$			
		ES, #byte	2	1	–	$\text{ES} \leftarrow \text{byte}$			
		!addr16, #byte	4	1	–	$(\text{addr16}) \leftarrow \text{byte}$			
		ES:!addr16, #byte	5	2	–	$(\text{ES}, \text{addr16}) \leftarrow \text{byte}$			
		saddr, #byte	3	1	–	$(\text{saddr}) \leftarrow \text{byte}$			
		sfr, #byte	3	1	–	$\text{sfr} \leftarrow \text{byte}$			
		[DE+byte], #byte	3	1	–	$(\text{DE}+\text{byte}) \leftarrow \text{byte}$			
		ES:[DE+byte], #byte	4	2	–	$((\text{ES}, \text{DE})+\text{byte}) \leftarrow \text{byte}$			
		[HL+byte], #byte	3	1	–	$(\text{HL}+\text{byte}) \leftarrow \text{byte}$			
		ES:[HL+byte], #byte	4	2	–	$((\text{ES}, \text{HL})+\text{byte}) \leftarrow \text{byte}$			
		[SP+byte], #byte	3	1	–	$(\text{SP}+\text{byte}) \leftarrow \text{byte}$			
		word[B], #byte	4	1	–	$(\text{B}+\text{word}) \leftarrow \text{byte}$			
		ES:word[B], #byte	5	2	–	$((\text{ES}, \text{B})+\text{word}) \leftarrow \text{byte}$			
		word[C], #byte	4	1	–	$(\text{C}+\text{word}) \leftarrow \text{byte}$			
		ES:word[C], #byte	5	2	–	$((\text{ES}, \text{C})+\text{word}) \leftarrow \text{byte}$			
		word[BC], #byte	4	1	–	$(\text{BC}+\text{word}) \leftarrow \text{byte}$			
		ES:word[BC], #byte	5	2	–	$((\text{ES}, \text{BC})+\text{word}) \leftarrow \text{byte}$			
		A, r Note 3	1	1	–	$\text{A} \leftarrow r$			
		r, A Note 3	1	1	–	$r \leftarrow \text{A}$			
		A, PSW	2	1	–	$\text{A} \leftarrow \text{PSW}$			
		PSW, A	2	3	–	$\text{PSW} \leftarrow \text{A}$	×	×	×
		A, CS	2	1	–	$\text{A} \leftarrow \text{CS}$			
		CS, A	2	1	–	$\text{CS} \leftarrow \text{A}$			
		A, ES	2	1	–	$\text{A} \leftarrow \text{ES}$			
		ES, A	2	1	–	$\text{ES} \leftarrow \text{A}$			
		A, !addr16	3	1	4	$\text{A} \leftarrow (\text{addr16})$			
		A, ES:!addr16	4	2	5	$\text{A} \leftarrow (\text{ES}, \text{addr16})$			
		!addr16, A	3	1	–	$(\text{addr16}) \leftarrow \text{A}$			
		ES:!addr16, A	4	2	–	$(\text{ES}, \text{addr16}) \leftarrow \text{A}$			
		A, saddr	2	1	–	$\text{A} \leftarrow (\text{saddr})$			
		saddr, A	2	1	–	$(\text{saddr}) \leftarrow \text{A}$			

- Notes**
1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
 2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.
 3. Except $r = \text{A}$

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (2/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	MOV	A, sfr	2	1	–	$A \leftarrow \text{sfr}$			
		sfr, A	2	1	–	$\text{sfr} \leftarrow A$			
		A, [DE]	1	1	4	$A \leftarrow (\text{DE})$			
		[DE], A	1	1	–	$(\text{DE}) \leftarrow A$			
		A, ES:[DE]	2	2	5	$A \leftarrow (\text{ES}, \text{DE})$			
		ES:[DE], A	2	2	–	$(\text{ES}, \text{DE}) \leftarrow A$			
		A, [HL]	1	1	4	$A \leftarrow (\text{HL})$			
		[HL], A	1	1	–	$(\text{HL}) \leftarrow A$			
		A, ES:[HL]	2	2	5	$A \leftarrow (\text{ES}, \text{HL})$			
		ES:[HL], A	2	2	–	$(\text{ES}, \text{HL}) \leftarrow A$			
		A, [DE+byte]	2	1	4	$A \leftarrow (\text{DE} + \text{byte})$			
		[DE+byte], A	2	1	–	$(\text{DE} + \text{byte}) \leftarrow A$			
		A, ES:[DE+byte]	3	2	5	$A \leftarrow ((\text{ES}, \text{DE}) + \text{byte})$			
		ES:[DE+byte], A	3	2	–	$((\text{ES}, \text{DE}) + \text{byte}) \leftarrow A$			
		A, [HL+byte]	2	1	4	$A \leftarrow (\text{HL} + \text{byte})$			
		[HL+byte], A	2	1	–	$(\text{HL} + \text{byte}) \leftarrow A$			
		A, ES:[HL+byte]	3	2	5	$A \leftarrow ((\text{ES}, \text{HL}) + \text{byte})$			
		ES:[HL+byte], A	3	2	–	$((\text{ES}, \text{HL}) + \text{byte}) \leftarrow A$			
		A, [SP+byte]	2	1	–	$A \leftarrow (\text{SP} + \text{byte})$			
		[SP+byte], A	2	1	–	$(\text{SP} + \text{byte}) \leftarrow A$			
		A, word[B]	3	1	4	$A \leftarrow (\text{B} + \text{word})$			
		word[B], A	3	1	–	$(\text{B} + \text{word}) \leftarrow A$			
		A, ES:word[B]	4	2	5	$A \leftarrow ((\text{ES}, \text{B}) + \text{word})$			
		ES:word[B], A	4	2	–	$((\text{ES}, \text{B}) + \text{word}) \leftarrow A$			
		A, word[C]	3	1	4	$A \leftarrow (\text{C} + \text{word})$			
		word[C], A	3	1	–	$(\text{C} + \text{word}) \leftarrow A$			
		A, ES:word[C]	4	2	5	$A \leftarrow ((\text{ES}, \text{C}) + \text{word})$			
		ES:word[C], A	4	2	–	$((\text{ES}, \text{C}) + \text{word}) \leftarrow A$			
		A, word[BC]	3	1	4	$A \leftarrow (\text{BC} + \text{word})$			
		word[BC], A	3	1	–	$(\text{BC} + \text{word}) \leftarrow A$			
		A, ES:word[BC]	4	2	5	$A \leftarrow ((\text{ES}, \text{BC}) + \text{word})$			
		ES:word[BC], A	4	2	–	$((\text{ES}, \text{BC}) + \text{word}) \leftarrow A$			

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (3/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Flag
				Note 1	Note 2	
8-bit data transfer	MOV	A, [HL+B]	2	1	4	$A \leftarrow (HL + B)$
		[HL+B], A	2	1	–	$(HL + B) \leftarrow A$
		A, ES:[HL+B]	3	2	5	$A \leftarrow ((ES, HL) + B)$
		ES:[HL+B], A	3	2	–	$((ES, HL) + B) \leftarrow A$
		A, [HL+C]	2	1	4	$A \leftarrow (HL + C)$
		[HL+C], A	2	1	–	$(HL + C) \leftarrow A$
		A, ES:[HL+C]	3	2	5	$A \leftarrow ((ES, HL) + C)$
		ES:[HL+C], A	3	2	–	$((ES, HL) + C) \leftarrow A$
		X, laddr16	3	1	4	$X \leftarrow (addr16)$
		X, ES:laddr16	4	2	5	$X \leftarrow (ES, addr16)$
		X, saddr	2	1	–	$X \leftarrow (saddr)$
		B, laddr16	3	1	4	$B \leftarrow (addr16)$
		B, ES:laddr16	4	2	5	$B \leftarrow (ES, addr16)$
		B, saddr	2	1	–	$B \leftarrow (saddr)$
		C, laddr16	3	1	4	$C \leftarrow (addr16)$
		C, ES:laddr16	4	2	5	$C \leftarrow (ES, addr16)$
		C, saddr	2	1	–	$C \leftarrow (saddr)$
		ES, saddr	3	1	–	$ES \leftarrow (saddr)$
	XCH	A, r ^{Note 3}	1 (r = X) 2 (other than r = X)	1	–	$A \longleftrightarrow r$
		A, laddr16	4	2	–	$A \longleftrightarrow (addr16)$
		A, ES:laddr16	5	3	–	$A \longleftrightarrow (ES, addr16)$
		A, saddr	3	2	–	$A \longleftrightarrow (saddr)$
		A, sfr	3	2	–	$A \longleftrightarrow sfr$
		A, [DE]	2	2	–	$A \longleftrightarrow (DE)$
		A, ES:[DE]	3	3	–	$A \longleftrightarrow (ES, DE)$
		A, [HL]	2	2	–	$A \longleftrightarrow (HL)$
		A, ES:[HL]	3	3	–	$A \longleftrightarrow (ES, HL)$
		A, [DE+byte]	3	2	–	$A \longleftrightarrow (DE + \text{byte})$
		A, ES:[DE+byte]	4	3	–	$A \longleftrightarrow ((ES, DE) + \text{byte})$
		A, [HL+byte]	3	2	–	$A \longleftrightarrow (HL + \text{byte})$
		A, ES:[HL+byte]	4	3	–	$A \longleftrightarrow ((ES, HL) + \text{byte})$

- Notes**
1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
 2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.
 3. Except $r = A$

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (4/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	XCH	A, [HL+B]	2	2	–	$A \leftrightarrow (HL+B)$			
		A, ES:[HL+B]	3	3	–	$A \leftrightarrow ((ES, HL)+B)$			
		A, [HL+C]	2	2	–	$A \leftrightarrow (HL+C)$			
		A, ES:[HL+C]	3	3	–	$A \leftrightarrow ((ES, HL)+C)$			
	ONEB	A	1	1	–	$A \leftarrow 01H$			
		X	1	1	–	$X \leftarrow 01H$			
		B	1	1	–	$B \leftarrow 01H$			
		C	1	1	–	$C \leftarrow 01H$			
		!addr16	3	1	–	$(addr16) \leftarrow 01H$			
		ES:!addr16	4	2	–	$(ES, addr16) \leftarrow 01H$			
		saddr	2	1	–	$(saddr) \leftarrow 01H$			
	CLRB	A	1	1	–	$A \leftarrow 00H$			
		X	1	1	–	$X \leftarrow 00H$			
		B	1	1	–	$B \leftarrow 00H$			
		C	1	1	–	$C \leftarrow 00H$			
		!addr16	3	1	–	$(addr16) \leftarrow 00H$			
		ES:!addr16	4	2	–	$(ES, addr16) \leftarrow 00H$			
		saddr	2	1	–	$(saddr) \leftarrow 00H$			
	MOVS	[HL+byte], X	3	1	–	$(HL+byte) \leftarrow X$	×		×
		ES:[HL+byte], X	4	2	–	$(ES, HL+byte) \leftarrow X$	×		×
16-bit data transfer	MOVW	rp, #word	3	1	–	$rp \leftarrow word$			
		saddrp, #word	4	1	–	$(saddrp) \leftarrow word$			
		sfrp, #word	4	1	–	$sfrp \leftarrow word$			
		AX, rp ^{Note 3}	1	1	–	$AX \leftarrow rp$			
		rp, AX ^{Note 3}	1	1	–	$rp \leftarrow AX$			
		AX, !addr16	3	1	4	$AX \leftarrow (addr16)$			
		!addr16, AX	3	1	–	$(addr16) \leftarrow AX$			
		AX, ES:!addr16	4	2	5	$AX \leftarrow (ES, addr16)$			
		ES:!addr16, AX	4	2	–	$(ES, addr16) \leftarrow AX$			
		AX, saddrp	2	1	–	$AX \leftarrow (saddrp)$			
		saddrp, AX	2	1	–	$(saddrp) \leftarrow AX$			
		AX, sfrp	2	1	–	$AX \leftarrow sfrp$			
		sfrp, AX	2	1	–	$sfrp \leftarrow AX$			

- Notes**
1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
 2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.
 3. Except $rp = AX$

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (5/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit data transfer	MOVW	AX, [DE]	1	1	4	AX ← (DE)			
		[DE], AX	1	1	–	(DE) ← AX			
		AX, ES:[DE]	2	2	5	AX ← (ES, DE)			
		ES:[DE], AX	2	2	–	(ES, DE) ← AX			
		AX, [HL]	1	1	4	AX ← (HL)			
		[HL], AX	1	1	–	(HL) ← AX			
		AX, ES:[HL]	2	2	5	AX ← (ES, HL)			
		ES:[HL], AX	2	2	–	(ES, HL) ← AX			
		AX, [DE+byte]	2	1	4	AX ← (DE+byte)			
		[DE+byte], AX	2	1	–	(DE+byte) ← AX			
		AX, ES:[DE+byte]	3	2	5	AX ← ((ES, DE) + byte)			
		ES:[DE+byte], AX	3	2	–	((ES, DE) + byte) ← AX			
		AX, [HL+byte]	2	1	4	AX ← (HL + byte)			
		[HL+byte], AX	2	1	–	(HL + byte) ← AX			
		AX, ES:[HL+byte]	3	2	5	AX ← ((ES, HL) + byte)			
		ES:[HL+byte], AX	3	2	–	((ES, HL) + byte) ← AX			
		AX, [SP+byte]	2	1	–	AX ← (SP + byte)			
		[SP+byte], AX	2	1	–	(SP + byte) ← AX			
		AX, word[B]	3	1	4	AX ← (B + word)			
		word[B], AX	3	1	–	(B + word) ← AX			
		AX, ES:word[B]	4	2	5	AX ← ((ES, B) + word)			
		ES:word[B], AX	4	2	–	((ES, B) + word) ← AX			
		AX, word[C]	3	1	4	AX ← (C + word)			
		word[C], AX	3	1	–	(C + word) ← AX			
		AX, ES:word[C]	4	2	5	AX ← ((ES, C) + word)			
		ES:word[C], AX	4	2	–	((ES, C) + word) ← AX			
		AX, word[BC]	3	1	4	AX ← (BC + word)			
		word[BC], AX	3	1	–	(BC + word) ← AX			
		AX, ES:word[BC]	4	2	5	AX ← ((ES, BC) + word)			
		ES:word[BC], AX	4	2	–	((ES, BC) + word) ← AX			

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (6/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit data transfer	MOVW	BC, laddr16	3	1	4	BC ← (addr16)			
		BC, ES:laddr16	4	2	5	BC ← (ES, addr16)			
		DE, laddr16	3	1	4	DE ← (addr16)			
		DE, ES:laddr16	4	2	5	DE ← (ES, addr16)			
		HL, laddr16	3	1	4	HL ← (addr16)			
		HL, ES:laddr16	4	2	5	HL ← (ES, addr16)			
		BC, saddrp	2	1	–	BC ← (saddrp)			
		DE, saddrp	2	1	–	DE ← (saddrp)			
		HL, saddrp	2	1	–	HL ← (saddrp)			
	XCHW	AX, rp ^{Note 3}	1	1	–	AX ↔ rp			
	ONEW	AX	1	1	–	AX ← 0001H			
		BC	1	1	–	BC ← 0001H			
	CLRW	AX	1	1	–	AX ← 0000H			
		BC	1	1	–	BC ← 0000H			
8-bit operation	ADD	A, #byte	2	1	–	A, CY ← A + byte	x	x	x
		saddr, #byte	3	2	–	(saddr), CY ← (saddr)+byte	x	x	x
		A, r ^{Note 4}	2	1	–	A, CY ← A + r	x	x	x
		r, A	2	1	–	r, CY ← r + A	x	x	x
		A, laddr16	3	1	4	A, CY ← A + (addr16)	x	x	x
		A, ES:laddr16	4	2	5	A, CY ← A + (ES, addr16)	x	x	x
		A, saddr	2	1	–	A, CY ← A + (saddr)	x	x	x
		A, [HL]	1	1	4	A, CY ← A + (HL)	x	x	x
		A, ES:[HL]	2	2	5	A, CY ← A + (ES, HL)	x	x	x
		A, [HL+byte]	2	1	4	A, CY ← A + (HL+byte)	x	x	x
		A, ES:[HL+byte]	3	2	5	A, CY ← A + ((ES, HL)+byte)	x	x	x
		A, [HL+B]	2	1	4	A, CY ← A + (HL+B)	x	x	x
		A, ES:[HL+B]	3	2	5	A, CY ← A + ((ES, HL)+B)	x	x	x
		A, [HL+C]	2	1	4	A, CY ← A + (HL+C)	x	x	x
		A, ES:[HL+C]	3	2	5	A, CY ← A + ((ES, HL) + C)	x	x	x

- Notes**
1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
 2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.
 3. Except rp = AX
 4. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (7/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	ADDC	A, #byte	2	1	–	$A, CY \leftarrow A + \text{byte} + CY$	x	x	x
		saddr, #byte	3	2	–	$(\text{saddr}), CY \leftarrow (\text{saddr}) + \text{byte} + CY$	x	x	x
		A, r ^{Note 3}	2	1	–	$A, CY \leftarrow A + r + CY$	x	x	x
		r, A	2	1	–	$r, CY \leftarrow r + A + CY$	x	x	x
		A, laddr16	3	1	4	$A, CY \leftarrow A + (\text{laddr16}) + CY$	x	x	x
		A, ES:laddr16	4	2	5	$A, CY \leftarrow A + (\text{ES}, \text{laddr16}) + CY$	x	x	x
		A, saddr	2	1	–	$A, CY \leftarrow A + (\text{saddr}) + CY$	x	x	x
		A, [HL]	1	1	4	$A, CY \leftarrow A + (\text{HL}) + CY$	x	x	x
		A, ES:[HL]	2	2	5	$A, CY \leftarrow A + (\text{ES}, \text{HL}) + CY$	x	x	x
		A, [HL+byte]	2	1	4	$A, CY \leftarrow A + (\text{HL} + \text{byte}) + CY$	x	x	x
		A, ES:[HL+byte]	3	2	5	$A, CY \leftarrow A + ((\text{ES}, \text{HL}) + \text{byte}) + CY$	x	x	x
		A, [HL+B]	2	1	4	$A, CY \leftarrow A + (\text{HL} + B) + CY$	x	x	x
		A, ES:[HL+B]	3	2	5	$A, CY \leftarrow A + ((\text{ES}, \text{HL}) + B) + CY$	x	x	x
		A, [HL+C]	2	1	4	$A, CY \leftarrow A + (\text{HL} + C) + CY$	x	x	x
		A, ES:[HL+C]	3	2	5	$A, CY \leftarrow A + ((\text{ES}, \text{HL}) + C) + CY$	x	x	x
	SUB	A, #byte	2	1	–	$A, CY \leftarrow A - \text{byte}$	x	x	x
		saddr, #byte	3	2	–	$(\text{saddr}), CY \leftarrow (\text{saddr}) - \text{byte}$	x	x	x
		A, r ^{Note 3}	2	1	–	$A, CY \leftarrow A - r$	x	x	x
		r, A	2	1	–	$r, CY \leftarrow r - A$	x	x	x
		A, laddr16	3	1	4	$A, CY \leftarrow A - (\text{laddr16})$	x	x	x
		A, ES:laddr16	4	2	5	$A, CY \leftarrow A - (\text{ES}, \text{laddr16})$	x	x	x
		A, saddr	2	1	–	$A, CY \leftarrow A - (\text{saddr})$	x	x	x
		A, [HL]	1	1	4	$A, CY \leftarrow A - (\text{HL})$	x	x	x
		A, ES:[HL]	2	2	5	$A, CY \leftarrow A - (\text{ES}, \text{HL})$	x	x	x
		A, [HL+byte]	2	1	4	$A, CY \leftarrow A - (\text{HL} + \text{byte})$	x	x	x
		A, ES:[HL+byte]	3	2	5	$A, CY \leftarrow A - ((\text{ES}, \text{HL}) + \text{byte})$	x	x	x
		A, [HL+B]	2	1	4	$A, CY \leftarrow A - (\text{HL} + B)$	x	x	x
		A, ES:[HL+B]	3	2	5	$A, CY \leftarrow A - ((\text{ES}, \text{HL}) + B)$	x	x	x
		A, [HL+C]	2	1	4	$A, CY \leftarrow A - (\text{HL} + C)$	x	x	x
		A, ES:[HL+C]	3	2	5	$A, CY \leftarrow A - ((\text{ES}, \text{HL}) + C)$	x	x	x

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

3. Except $r = A$

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (8/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	SUBC	A, #byte	2	1	–	$A, CY \leftarrow A - \text{byte} - CY$	x	x	x
		saddr, #byte	3	2	–	$(saddr), CY \leftarrow (saddr) - \text{byte} - CY$	x	x	x
		A, r Note 3	2	1	–	$A, CY \leftarrow A - r - CY$	x	x	x
		r, A	2	1	–	$r, CY \leftarrow r - A - CY$	x	x	x
		A, laddr16	3	1	4	$A, CY \leftarrow A - (\text{addr16}) - CY$	x	x	x
		A, ES:laddr16	4	2	5	$A, CY \leftarrow A - (ES, \text{addr16}) - CY$	x	x	x
		A, saddr	2	1	–	$A, CY \leftarrow A - (saddr) - CY$	x	x	x
		A, [HL]	1	1	4	$A, CY \leftarrow A - (HL) - CY$	x	x	x
		A, ES:[HL]	2	2	5	$A, CY \leftarrow A - (ES, HL) - CY$	x	x	x
		A, [HL+byte]	2	1	4	$A, CY \leftarrow A - (HL+\text{byte}) - CY$	x	x	x
		A, ES:[HL+byte]	3	2	5	$A, CY \leftarrow A - ((ES, HL)+\text{byte}) - CY$	x	x	x
		A, [HL+B]	2	1	4	$A, CY \leftarrow A - (HL+B) - CY$	x	x	x
		A, ES:[HL+B]	3	2	5	$A, CY \leftarrow A - ((ES, HL)+B) - CY$	x	x	x
		A, [HL+C]	2	1	4	$A, CY \leftarrow A - (HL+C) - CY$	x	x	x
		A, ES:[HL+C]	3	2	5	$A, CY \leftarrow A - ((ES:HL)+C) - CY$	x	x	x
	AND	A, #byte	2	1	–	$A \leftarrow A \wedge \text{byte}$	x		
		saddr, #byte	3	2	–	$(saddr) \leftarrow (saddr) \wedge \text{byte}$	x		
		A, r Note 3	2	1	–	$A \leftarrow A \wedge r$	x		
		r, A	2	1	–	$R \leftarrow r \wedge A$	x		
		A, laddr16	3	1	4	$A \leftarrow A \wedge (\text{addr16})$	x		
		A, ES:laddr16	4	2	5	$A \leftarrow A \wedge (ES:\text{addr16})$	x		
		A, saddr	2	1	–	$A \leftarrow A \wedge (saddr)$	x		
		A, [HL]	1	1	4	$A \leftarrow A \wedge (HL)$	x		
		A, ES:[HL]	2	2	5	$A \leftarrow A \wedge (ES:HL)$	x		
		A, [HL+byte]	2	1	4	$A \leftarrow A \wedge (HL+\text{byte})$	x		
		A, ES:[HL+byte]	3	2	5	$A \leftarrow A \wedge ((ES:HL)+\text{byte})$	x		
		A, [HL+B]	2	1	4	$A \leftarrow A \wedge (HL+B)$	x		
		A, ES:[HL+B]	3	2	5	$A \leftarrow A \wedge ((ES:HL)+B)$	x		
		A, [HL+C]	2	1	4	$A \leftarrow A \wedge (HL+C)$	x		
		A, ES:[HL+C]	3	2	5	$A \leftarrow A \wedge ((ES:HL)+C)$	x		

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

3. Except $r = A$

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (9/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	OR	A, #byte	2	1	–	$A \leftarrow A \vee \text{byte}$	x		
		saddr, #byte	3	2	–	$(\text{saddr}) \leftarrow (\text{saddr}) \vee \text{byte}$	x		
		A, r Note 3	2	1	–	$A \leftarrow A \vee r$	x		
		r, A	2	1	–	$r \leftarrow r \vee A$	x		
		A, laddr16	3	1	4	$A \leftarrow A \vee (\text{addr16})$	x		
		A, ES:laddr16	4	2	5	$A \leftarrow A \vee (\text{ES:addr16})$	x		
		A, saddr	2	1	–	$A \leftarrow A \vee (\text{saddr})$	x		
		A, [HL]	1	1	4	$A \leftarrow A \vee (\text{H})$	x		
		A, ES:[HL]	2	2	5	$A \leftarrow A \vee (\text{ES:HL})$	x		
		A, [HL+byte]	2	1	4	$A \leftarrow A \vee (\text{HL} + \text{byte})$	x		
		A, ES:[HL+byte]	3	2	5	$A \leftarrow A \vee ((\text{ES:HL}) + \text{byte})$	x		
		A, [HL+B]	2	1	4	$A \leftarrow A \vee (\text{HL} + \text{B})$	x		
		A, ES:[HL+B]	3	2	5	$A \leftarrow A \vee ((\text{ES:HL}) + \text{B})$	x		
		A, [HL+C]	2	1	4	$A \leftarrow A \vee (\text{HL} + \text{C})$	x		
		A, ES:[HL+C]	3	2	5	$A \leftarrow A \vee ((\text{ES:HL}) + \text{C})$	x		
	XOR	A, #byte	2	1	–	$A \leftarrow A \oplus \text{byte}$	x		
		saddr, #byte	3	2	–	$(\text{saddr}) \leftarrow (\text{saddr}) \oplus \text{byte}$	x		
		A, r Note 3	2	1	–	$A \leftarrow A \oplus r$	x		
		r, A	2	1	–	$r \leftarrow r \oplus A$	x		
		A, laddr16	3	1	4	$A \leftarrow A \oplus (\text{addr16})$	x		
		A, ES:laddr16	4	2	5	$A \leftarrow A \oplus (\text{ES:addr16})$	x		
		A, saddr	2	1	–	$A \leftarrow A \oplus (\text{saddr})$	x		
		A, [HL]	1	1	4	$A \leftarrow A \oplus (\text{HL})$	x		
		A, ES:[HL]	2	2	5	$A \leftarrow A \oplus (\text{ES:HL})$	x		
		A, [HL+byte]	2	1	4	$A \leftarrow A \oplus (\text{HL} + \text{byte})$	x		
		A, ES:[HL+byte]	3	2	5	$A \leftarrow A \oplus ((\text{ES:HL}) + \text{byte})$	x		
		A, [HL+B]	2	1	4	$A \leftarrow A \oplus (\text{HL} + \text{B})$	x		
		A, ES:[HL+B]	3	2	5	$A \leftarrow A \oplus ((\text{ES:HL}) + \text{B})$	x		
		A, [HL+C]	2	1	4	$A \leftarrow A \oplus (\text{HL} + \text{C})$	x		
		A, ES:[HL+C]	3	2	5	$A \leftarrow A \oplus ((\text{ES:HL}) + \text{C})$	x		

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

3. Except $r = A$

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (10/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
<R> 8-bit operation	CMP	A, #byte	2	1	–	A – byte	x	x	x
		!addr16, #byte	4	1	4	(addr16) – byte	x	x	x
		ES:!addr16, #byte	5	2	5	(ES:addr16) – byte	x	x	x
		saddr, #byte	3	1	–	(saddr) – byte	x	x	x
		A, r ^{Note3}	2	1	–	A – r	x	x	x
		r, A	2	1	–	r – A	x	x	x
		A, !addr16	3	1	4	A – (addr16)	x	x	x
		A, ES:!addr16	4	2	5	A – (ES:addr16)	x	x	x
		A, saddr	2	1	–	A – (saddr)	x	x	x
		A, [HL]	1	1	4	A – (HL)	x	x	x
		A, ES:[HL]	2	2	5	A – (ES:HL)	x	x	x
		A, [HL+byte]	2	1	4	A – (HL+byte)	x	x	x
		A, ES:[HL+byte]	3	2	5	A – ((ES:HL)+byte)	x	x	x
		A, [HL+B]	2	1	4	A – (HL+B)	x	x	x
		A, ES:[HL+B]	3	2	5	A – ((ES:HL)+B)	x	x	x
		A, [HL+C]	2	1	4	A – (HL+C)	x	x	x
		A, ES:[HL+C]	3	2	5	A – ((ES:HL)+C)	x	x	x
	CMP0	A	1	1	–	A – 00H	x	0	0
		X	1	1	–	X – 00H	x	0	0
		B	1	1	–	B – 00H	x	0	0
		C	1	1	–	C – 00H	x	0	0
		!addr16	3	1	4	(addr16) – 00H	x	0	0
		ES:!addr16	4	2	5	(ES:addr16) – 00H	x	0	0
		saddr	2	1	–	(saddr) – 00H	x	0	0
	CMPS	X, [HL+byte]	3	1	4	X – (HL+byte)	x	x	x
		X, ES:[HL+byte]	4	2	5	X – ((ES:HL)+byte)	x	x	x

- Notes**
1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
 2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.
 3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (11/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit operation	ADDW	AX, #word	3	1	–	AX, CY ← AX+word	x	x	x
		AX, AX	1	1	–	AX, CY ← AX+AX	x	x	x
		AX, BC	1	1	–	AX, CY ← AX+BC	x	x	x
		AX, DE	1	1	–	AX, CY ← AX+DE	x	x	x
		AX, HL	1	1	–	AX, CY ← AX+HL	x	x	x
		AX, !addr16	3	1	4	AX, CY ← AX+(addr16)	x	x	x
		AX, ES:!addr16	4	2	5	AX, CY ← AX+(ES:addr16)	x	x	x
		AX, saddrp	2	1	–	AX, CY ← AX+(saddrp)	x	x	x
		AX, [HL+byte]	3	1	4	AX, CY ← AX+(HL+byte)	x	x	x
		AX, ES: [HL+byte]	4	2	5	AX, CY ← AX+((ES:HL)+byte)	x	x	x
	SUBW	AX, #word	3	1	–	AX, CY ← AX – word	x	x	x
		AX, BC	1	1	–	AX, CY ← AX – BC	x	x	x
		AX, DE	1	1	–	AX, CY ← AX – DE	x	x	x
		AX, HL	1	1	–	AX, CY ← AX – HL	x	x	x
		AX, !addr16	3	1	4	AX, CY ← AX – (addr16)	x	x	x
		AX, ES:!addr16	4	2	5	AX, CY ← AX – (ES:addr16)	x	x	x
		AX, saddrp	2	1	–	AX, CY ← AX – (saddrp)	x	x	x
		AX, [HL+byte]	3	1	4	AX, CY ← AX – (HL+byte)	x	x	x
		AX, ES: [HL+byte]	4	2	5	AX, CY ← AX – ((ES:HL)+byte)	x	x	x
	CMPW	AX, #word	3	1	–	AX – word	x	x	x
		AX, BC	1	1	–	AX – BC	x	x	x
		AX, DE	1	1	–	AX – DE	x	x	x
		AX, HL	1	1	–	AX – HL	x	x	x
		AX, !addr16	3	1	4	AX – (addr16)	x	x	x
		AX, ES:!addr16	4	2	5	AX – (ES:addr16)	x	x	x
		AX, saddrp	2	1	–	AX – (saddrp)	x	x	x
		AX, [HL+byte]	3	1	4	AX – (HL+byte)	x	x	x
		AX, ES: [HL+byte]	4	2	5	AX – ((ES:HL)+byte)	x	x	x
Multiply	MULU	X	1	1	–	AX ← A×X			

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (12/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Increment/decrement	INC	r	1	1	—	$r \leftarrow r+1$	x	x	
		!addr16	3	2	—	$(addr16) \leftarrow (addr16)+1$	x	x	
		ES:!addr16	4	3	—	$(ES, addr16) \leftarrow (ES, addr16)+1$	x	x	
		saddr	2	2	—	$(saddr) \leftarrow (saddr)+1$	x	x	
		[HL+byte]	3	2	—	$(HL+byte) \leftarrow (HL+byte)+1$	x	x	
		ES: [HL+byte]	4	3	—	$((ES:HL)+byte) \leftarrow ((ES:HL)+byte)+1$	x	x	
	DEC	r	1	1	—	$r \leftarrow r-1$	x	x	
		!addr16	3	2	—	$(addr16) \leftarrow (addr16)-1$	x	x	
		ES:!addr16	4	3	—	$(ES, addr16) \leftarrow (ES, addr16)-1$	x	x	
		saddr	2	2	—	$(saddr) \leftarrow (saddr)-1$	x	x	
		[HL+byte]	3	2	—	$(HL+byte) \leftarrow (HL+byte)-1$	x	x	
		ES: [HL+byte]	4	3	—	$((ES:HL)+byte) \leftarrow ((ES:HL)+byte)-1$	x	x	
	INCW	rp	1	1	—	$rp \leftarrow rp+1$			
		!addr16	3	2	—	$(addr16) \leftarrow (addr16)+1$			
		ES:!addr16	4	3	—	$(ES, addr16) \leftarrow (ES, addr16)+1$			
		saddrp	2	2	—	$(saddrp) \leftarrow (saddrp)+1$			
		[HL+byte]	3	2	—	$(HL+byte) \leftarrow (HL+byte)+1$			
		ES: [HL+byte]	4	3	—	$((ES:HL)+byte) \leftarrow ((ES:HL)+byte)+1$			
	DECW	rp	1	1	—	$rp \leftarrow rp-1$			
		!addr16	3	2	—	$(addr16) \leftarrow (addr16)-1$			
		ES:!addr16	4	3	—	$(ES, addr16) \leftarrow (ES, addr16)-1$			
		saddrp	2	2	—	$(saddrp) \leftarrow (saddrp)-1$			
		[HL+byte]	3	2	—	$(HL+byte) \leftarrow (HL+byte)-1$			
		ES: [HL+byte]	4	3	—	$((ES:HL)+byte) \leftarrow ((ES:HL)+byte)-1$			
Shift	SHR	A, cnt	2	1	—	$(CY \leftarrow A_0, A_{m-1} \leftarrow A_m, A_7 \leftarrow 0) \times cnt$			x
	SHRW	AX, cnt	2	1	—	$(CY \leftarrow AX_0, AX_{m-1} \leftarrow AX_m, AX_{15} \leftarrow 0) \times cnt$			x
	SHL	A, cnt	2	1	—	$(CY \leftarrow A_7, A_m \leftarrow A_{m-1}, A_0 \leftarrow 0) \times cnt$			x
		B, cnt	2	1	—	$(CY \leftarrow B_7, B_m \leftarrow B_{m-1}, B_0 \leftarrow 0) \times cnt$			x
		C, cnt	2	1	—	$(CY \leftarrow C_7, C_m \leftarrow C_{m-1}, C_0 \leftarrow 0) \times cnt$			x
	SHLW	AX, cnt	2	1	—	$(CY \leftarrow AX_{15}, AX_m \leftarrow AX_{m-1}, AX_0 \leftarrow 0) \times cnt$			x
		BC, cnt	2	1	—	$(CY \leftarrow BC_{15}, BC_m \leftarrow BC_{m-1}, BC_0 \leftarrow 0) \times cnt$			x
	SAR	A, cnt	2	1	—	$(CY \leftarrow A_0, A_{m-1} \leftarrow A_m, A_7 \leftarrow A_7) \times cnt$			x
	SARW	AX, cnt	2	1	—	$(CY \leftarrow AX_0, AX_{m-1} \leftarrow AX_m, AX_{15} \leftarrow AX_{15}) \times cnt$			x

- Notes**
1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
 2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

- Remarks**
1. Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.
 2. cnt indicates the bit shift count.

Table 28-5. Operation List (13/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Rotate	ROR	A, 1	2	1	–	$(CY, A_7 \leftarrow A_0, A_{m-1} \leftarrow A_m) \times 1$			×
	ROL	A, 1	2	1	–	$(CY, A_0 \leftarrow A_7, A_{m+1} \leftarrow A_m) \times 1$			×
	RORC	A, 1	2	1	–	$(CY \leftarrow A_0, A_7 \leftarrow CY, A_{m-1} \leftarrow A_m) \times 1$			×
	ROLC	A, 1	2	1	–	$(CY \leftarrow A_7, A_0 \leftarrow CY, A_{m+1} \leftarrow A_m) \times 1$			×
	ROLWC	AX, 1	2	1	–	$(CY \leftarrow AX_{15}, AX_0 \leftarrow CY, AX_{m+1} \leftarrow AX_m) \times 1$			×
		BC, 1	2	1	–	$(CY \leftarrow BC_{15}, BC_0 \leftarrow CY, BC_{m+1} \leftarrow BC_m) \times 1$			×
Bit manipulate	MOV1	CY, A.bit	2	1	–	$CY \leftarrow A.bit$			×
		A.bit, CY	2	1	–	$A.bit \leftarrow CY$			
		CY, PSW.bit	3	1	–	$CY \leftarrow PSW.bit$			×
		PSW.bit, CY	3	4	–	$PSW.bit \leftarrow CY$	×	×	
		CY, saddr.bit	3	1	–	$CY \leftarrow (saddr).bit$			×
		saddr.bit, CY	3	2	–	$(saddr).bit \leftarrow CY$			
		CY, sfr.bit	3	1	–	$CY \leftarrow sfr.bit$			×
		sfr.bit, CY	3	2	–	$sfr.bit \leftarrow CY$			
		CY, [HL].bit	2	1	4	$CY \leftarrow (HL).bit$			×
		[HL].bit, CY	2	2	–	$(HL).bit \leftarrow CY$			
		CY, ES:[HL].bit	3	2	5	$CY \leftarrow (ES, HL).bit$			×
		ES:[HL].bit, CY	3	3	–	$(ES, HL).bit \leftarrow CY$			
	AND1	CY, A.bit	2	1	–	$CY \leftarrow CY \wedge A.bit$			×
		CY, PSW.bit	3	1	–	$CY \leftarrow CY \wedge PSW.bit$			×
		CY, saddr.bit	3	1	–	$CY \leftarrow CY \wedge (saddr).bit$			×
		CY, sfr.bit	3	1	–	$CY \leftarrow CY \wedge sfr.bit$			×
		CY, [HL].bit	2	1	4	$CY \leftarrow CY \wedge (HL).bit$			×
		CY, ES:[HL].bit	3	2	5	$CY \leftarrow CY \wedge (ES, HL).bit$			×
	OR1	CY, A.bit	2	1	–	$CY \leftarrow CY \vee A.bit$			×
		CY, PSW.bit	3	1	–	$CY \leftarrow CY \vee PSW.bit$			×
		CY, saddr.bit	3	1	–	$CY \leftarrow CY \vee (saddr).bit$			×
		CY, sfr.bit	3	1	–	$CY \leftarrow CY \vee sfr.bit$			×
		CY, [HL].bit	2	1	4	$CY \leftarrow CY \vee (HL).bit$			×
		CY, ES:[HL].bit	3	2	5	$CY \leftarrow CY \vee (ES, HL).bit$			×

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (14/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Bit manipulate	XOR1	CY, A.bit	2	1	–	$CY \leftarrow CY \oplus A.bit$			×
		CY, PSW.bit	3	1	–	$CY \leftarrow CY \oplus PSW.bit$			×
		CY, saddr.bit	3	1	–	$CY \leftarrow CY \oplus (saddr).bit$			×
		CY, sfr.bit	3	1	–	$CY \leftarrow CY \oplus sfr.bit$			×
		CY, [HL].bit	2	1	4	$CY \leftarrow CY \oplus (HL).bit$			×
		CY, ES:[HL].bit	3	2	5	$CY \leftarrow CY \oplus (ES, HL).bit$			×
	SET1	A.bit	2	1	–	$A.bit \leftarrow 1$			
		PSW.bit	3	4	–	$PSW.bit \leftarrow 1$	×	×	×
		!addr16.bit	4	2	–	$(addr16).bit \leftarrow 1$			
		ES:!addr16.bit	5	3	–	$(ES, addr16).bit \leftarrow 1$			
		saddr.bit	3	2	–	$(saddr).bit \leftarrow 1$			
		sfr.bit	3	2	–	$sfr.bit \leftarrow 1$			
		[HL].bit	2	2	–	$(HL).bit \leftarrow 1$			
		ES:[HL].bit	3	3	–	$(ES, HL).bit \leftarrow 1$			
	CLR1	A.bit	2	1	–	$A.bit \leftarrow 0$			
		PSW.bit	3	4	–	$PSW.bit \leftarrow 0$	×	×	×
		!addr16.bit	4	2	–	$(addr16).bit \leftarrow 0$			
		ES:!addr16.bit	5	3	–	$(ES, addr16).bit \leftarrow 0$			
		saddr.bit	3	2	–	$(saddr).bit \leftarrow 0$			
		sfr.bit	3	2	–	$sfr.bit \leftarrow 0$			
		[HL].bit	2	2	–	$(HL).bit \leftarrow 0$			
		ES:[HL].bit	3	3	–	$(ES, HL).bit \leftarrow 0$			
	SET1	CY	2	1	–	$CY \leftarrow 1$			1
	CLR1	CY	2	1	–	$CY \leftarrow 0$			0
	NOT1	CY	2	1	–	$CY \leftarrow CY$			×

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (15/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Call/ return	CALL	rp	2	3	–	(SP – 2) ← (PC+2) _S , (SP – 3) ← (PC+2) _H , (SP – 4) ← (PC+2) _L , PC ← CS, rp, SP ← SP – 4			
		\$!addr20	3	3	–	(SP – 2) ← (PC+3) _S , (SP – 3) ← (PC+3) _H , (SP – 4) ← (PC+3) _L , PC ← PC+3+jdisp16, SP ← SP – 4			
		!addr16	3	3	–	(SP – 2) ← (PC+3) _S , (SP – 3) ← (PC+3) _H , (SP – 4) ← (PC+3) _L , PC ← 0000, addr16, SP ← SP – 4			
		!!addr20	4	3	–	(SP – 2) ← (PC+4) _S , (SP – 3) ← (PC+4) _H , (SP – 4) ← (PC+4) _L , PC ← addr20, SP ← SP – 4			
	CALLT	[addr5]	2	5	–	(SP – 2) ← (PC+2) _S , (SP – 3) ← (PC+2) _H , (SP – 4) ← (PC+2) _L , PC _S ← 0000, PC _H ← (0000, addr5+1), PC _L ← (0000, addr5), SP ← SP – 4			
	BRK	-	2	5	–	(SP – 1) ← PSW, (SP – 2) ← (PC+2) _S , (SP – 3) ← (PC+2) _H , (SP – 4) ← (PC+2) _L , PC _S ← 0000, PC _H ← (0007FH), PC _L ← (0007EH), SP ← SP – 4, IE ← 0			
	RET	-	1	6	–	PC _L ← (SP), PC _H ← (SP+1), PC _S ← (SP+2), SP ← SP+4			
	RETI	-	2	6	–	PC _L ← (SP), PC _H ← (SP+1), PC _S ← (SP+2), PSW ← (SP+3), SP ← SP+4	R	R	R
	RETB	-	2	6	–	PC _L ← (SP), PC _H ← (SP+1), PC _S ← (SP+2), PSW ← (SP+3), SP ← SP+4	R	R	R

- Notes**
1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
 2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (16/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Stack manipulate	PUSH	PSW	2	1	–	$(SP - 1) \leftarrow PSW, (SP - 2) \leftarrow 00H,$ $SP \leftarrow SP - 2$			
		rp	1	1	–	$(SP - 1) \leftarrow rp_H, (SP - 2) \leftarrow rp_L,$ $SP \leftarrow SP - 2$			
	POP	PSW	2	3	–	$PSW \leftarrow (SP + 1), SP \leftarrow SP + 2$	R	R	R
		rp	1	1	–	$rp_L \leftarrow (SP), rp_H \leftarrow (SP + 1), SP \leftarrow SP + 2$			
	MOVW	SP, #word	4	1	–	$SP \leftarrow word$			
		SP, AX	2	1	–	$SP \leftarrow AX$			
		AX, SP	2	1	–	$AX \leftarrow SP$			
		HL, SP	3	1	–	$HL \leftarrow SP$			
		BC, SP	3	1	–	$BC \leftarrow SP$			
		DE, SP	3	1	–	$DE \leftarrow SP$			
	ADDW	SP, #byte	2	1	–	$SP \leftarrow SP + byte$			
	SUBW	SP, #byte	2	1	–	$SP \leftarrow SP - byte$			
Unconditional branch	BR	AX	2	3	–	$PC \leftarrow CS, AX$			
		\$addr20	2	3	–	$PC \leftarrow PC + 2 + jdisp8$			
		!addr20	3	3	–	$PC \leftarrow PC + 3 + jdisp16$			
		laddr16	3	3	–	$PC \leftarrow 0000, addr16$			
		!!addr20	4	3	–	$PC \leftarrow addr20$			
Conditional branch	BC	\$addr20	2	2/4 ^{Note3}	–	$PC \leftarrow PC + 2 + jdisp8$ if CY = 1			
	BNC	\$addr20	2	2/4 ^{Note3}	–	$PC \leftarrow PC + 2 + jdisp8$ if CY = 0			
	BZ	\$addr20	2	2/4 ^{Note3}	–	$PC \leftarrow PC + 2 + jdisp8$ if Z = 1			
	BNZ	\$addr20	2	2/4 ^{Note3}	–	$PC \leftarrow PC + 2 + jdisp8$ if Z = 0			
	BH	\$addr20	3	2/4 ^{Note3}	–	$PC \leftarrow PC + 3 + jdisp8$ if $(Z \vee CY) = 0$			
	BNH	\$addr20	3	2/4 ^{Note3}	–	$PC \leftarrow PC + 3 + jdisp8$ if $(Z \vee CY) = 1$			
	BT	saddr.bit, \$addr20	4	3/5 ^{Note3}	–	$PC \leftarrow PC + 4 + jdisp8$ if (saddr).bit = 1			
		sfr.bit, \$addr20	4	3/5 ^{Note3}	–	$PC \leftarrow PC + 4 + jdisp8$ if sfr.bit = 1			
		A.bit, \$addr20	3	3/5 ^{Note3}	–	$PC \leftarrow PC + 3 + jdisp8$ if A.bit = 1			
		PSW.bit, \$addr20	4	3/5 ^{Note3}	–	$PC \leftarrow PC + 4 + jdisp8$ if PSW.bit = 1			
		[HL].bit, \$addr20	3	3/5 ^{Note3}	6/7	$PC \leftarrow PC + 3 + jdisp8$ if (HL).bit = 1			
		ES:[HL].bit, \$addr20	4	4/6 ^{Note3}	7/8	$PC \leftarrow PC + 4 + jdisp8$ if (ES, HL).bit = 1			

- Notes**
1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
 2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.
 3. This indicates the number of clocks “when condition is not met/when condition is met”.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 28-5. Operation List (17/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Conditional branch	BF	saddr.bit, \$addr20	4	3/5 ^{Note3}	–	PC ← PC + 4 + jdisp8 if (saddr).bit = 0			
		sfr.bit, \$addr20	4	3/5 ^{Note3}	–	PC ← PC + 4 + jdisp8 if sfr.bit = 0			
		A.bit, \$addr20	3	3/5 ^{Note3}	–	PC ← PC + 3 + jdisp8 if A.bit = 0			
		PSW.bit, \$addr20	4	3/5 ^{Note3}	–	PC ← PC + 4 + jdisp8 if PSW.bit = 0			
		[HL].bit, \$addr20	3	3/5 ^{Note3}	6/7	PC ← PC + 3 + jdisp8 if (HL).bit = 0			
		ES:[HL].bit, \$addr20	4	4/6 ^{Note3}	7/8	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 0			
	BTCLR	saddr.bit, \$addr20	4	3/5 ^{Note3}	–	PC ← PC + 4 + jdisp8 if (saddr).bit = 1 then reset (saddr).bit			
		sfr.bit, \$addr20	4	3/5 ^{Note3}	–	PC ← PC + 4 + jdisp8 if sfr.bit = 1 then reset sfr.bit			
		A.bit, \$addr20	3	3/5 ^{Note3}	–	PC ← PC + 3 + jdisp8 if A.bit = 1 then reset A.bit			
		PSW.bit, \$addr20	4	3/5 ^{Note3}	–	PC ← PC + 4 + jdisp8 if PSW.bit = 1 then reset PSW.bit	×	×	×
		[HL].bit, \$addr20	3	3/5 ^{Note3}	–	PC ← PC + 3 + jdisp8 if (HL).bit = 1 then reset (HL).bit			
		ES:[HL].bit, \$addr20	4	4/6 ^{Note3}	–	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 1 then reset (ES, HL).bit			
Conditional skip	SKC	–	2	1	–	Next instruction skip if CY = 1			
	SKNC	–	2	1	–	Next instruction skip if CY = 0			
	SKZ	–	2	1	–	Next instruction skip if Z = 1			
	SKNZ	–	2	1	–	Next instruction skip if Z = 0			
	SKH	–	2	1	–	Next instruction skip if (Z∨CY)=0			
	SKNH	–	2	1	–	Next instruction skip if (Z∨CY)=1			
CPU control	SEL ^{Note4}	RBn	2	1	–	RBS[1:0] ← n			
	NOP	–	1	1	–	No Operation			
	EI	–	3	4	–	IE ← 1 (Enable Interrupt)			
	DI	–	3	4	–	IE ← 0 (Disable Interrupt)			
	HALT	–	2	3	–	Set HALT Mode			
	STOP	–	2	3	–	Set STOP Mode			

- Notes**
1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
 2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.
 3. This indicates the number of clocks “when condition is not met/when condition is met”.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

CHAPTER 29 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$) (TARGET)

<R> Target products A : Consumer applications $T_A = -40$ to $+85^\circ\text{C}$

R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA

R5F10EBAANA, R5F10EBCANA, R5F10EBDANA, R5F10EBEANA

R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB

R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA

R5F10ELCAFB, R5F10ELDADF, R5F10ELEAFB

R5F10ELCABG, R5F10ELDABG, R5F10ELEABG

G : Industrial applications When $T_A = -40$ to $+105^\circ\text{C}$ products is used in the range of $T_A = -40$ to $+85^\circ\text{C}$

R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGFB, R5F10EGEGFB

R5F10ELCGFB, R5F10ELDGFB, R5F10ELEGFB

Cautions 1. The RL78/G1A have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

<R> **2. With products not provided with an EV_{DD0} , EV_{DD1} , EV_{SS0} , or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD} , or replace EV_{SS0} and EV_{SS1} with V_{SS} .**

<R> **3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions Mounted According to Product.**

29.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

	Parameter	Symbols	Conditions	Ratings	Unit
<R>	Supply voltage	V _{DD}		−0.5 to +6.5	V
		EV _{DD0}		−0.5 to +6.5	V
		AV _{DD}		−0.5 to +4.6	V
		AV _{REFP}		−0.3 to AV _{DD} +0.3 ^{Note 3}	V
		V _{SS}		−0.5 to +0.3	V
		EV _{SS0}		−0.5 to +0.3	V
		AV _{SS}		−0.5 to +0.3	V
		AV _{REFM}		−0.3 to AV _{DD} +0.3 ^{Note 3} and AV _{REFM} ≤ AV _{REFP}	V
	REGC pin input voltage	V _I REGC	REGC	−0.3 to +2.8 and −0.3 to V _{DD} +0.3 ^{Note 1}	V
<R>	Input voltage	V _{I1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	−0.3 to EV _{DD0} +0.3 and −0.3 to V _{DD} +0.3 ^{Note 2}	V
		V _{I2}	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
		V _{I3}	P121 to P124, P137, EXCLK, EXCLKS, RESET	−0.3 to V _{DD} +0.3 ^{Note 2}	V
		V _{I4}	P20 to P27, P150 to P154	−0.3 to AV _{DD} +0.3 ^{Note 2}	V
<R>	Output voltage	V _{O1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	−0.3 to EV _{DD0} +0.3 ^{Note 2}	V
		V _{O2}	P20 to P27, P150 to P154	−0.3 to AV _{DD} +0.3 ^{Note 2}	V
<R>	Analog input voltage	V _{AI1}	ANI16 to ANI30	−0.3 to EV _{DD0} +0.3 and −0.3 to AV _{REF(+) +0.3} ^{Notes 2,4}	V
		V _{AI2}	ANI0 to ANI12	−0.3 to AV _{DD} +0.3 and −0.3 to AV _{REF(+) +0.3} ^{Notes 2,4}	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Must be 4.6 V or lower.

<R> 4. Do not exceed AV_{REF(+) + 0.3 V} in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

<R> 2. AV_{REF(+) + 0.3 V} : + side reference voltage of the A/D converter.

Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	−40	mA
		Total of all pins −170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	−70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,	−100	mA
	I _{OH2}	Per pin	P20 to P27, P150 to P154	−0.1	mA
		Total of all pins		−1.3	mA
	Output current, low	I _{OL1}	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	40
Total of all pins 170 mA			P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77	100	mA
I _{OL2}		Per pin	P20 to P27, P150 to P154	0.4	mA
		Total of all pins		6.4	mA
Operating ambient temperature		T _A	In normal operation mode		−40 to +85
	In flash memory programming mode				
Storage temperature	T _{stg}			−65 to +150	°C

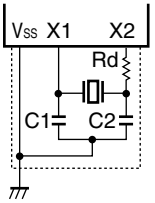
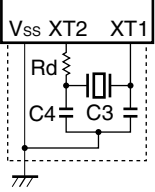
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

29.2 Oscillator Characteristics

29.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq E_{VDD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = E_{VSS0} = 0\text{ V}$)

Parameter	Resonator	Recommended Circuit	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_{X1}) ^{Note}	Ceramic resonator/ crystal resonator		$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	1.0		20.0	MHz
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		8.0	MHz
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$	1.0		4.0	MHz
XT1 clock oscillation frequency (f_{XT1}) ^{Note}	Crystal resonator			32	32.768	35	kHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.
 3. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

<R> 29.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq E_{VDD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = E_{VSS0} = 0\text{ V}$)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Note 1}	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy ^{Note 2}		-20 to $+85^\circ\text{C}$	$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-1		+1	%
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$	-5		+5	%
		-40 to -20°C	$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-1.5		+1.5	%
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. Frequency can be selected in a high-speed on-chip oscillator. Selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

29.3 DC Characteristics

29.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	1.6 V ≤ EV _{DD0} ≤ 3.6 V		–10.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70% ^{Note 3})	2.7 V ≤ EV _{DD0} ≤ 3.6 V		–10.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		–5.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		–2.5	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77, (When duty = 70% ^{Note 3})	2.7 V ≤ EV _{DD0} ≤ 3.6 V		–19.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		–10.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		–5.0	mA
		Total of all pins (When duty = 70% ^{Note 3})	1.6 V ≤ EV _{DD0} ≤ 3.6 V		–29.0	mA
	I _{OH2}	Per pin for P20 to P27, P150 to P154	1.6 V ≤ AV _{DD} ≤ 3.6 V		–0.1 ^{Note 2}	mA
		Total of all pins (When duty = 70% ^{Note 3})	1.6 V ≤ AV _{DD} ≤ 3.6 V		–1.3	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OH} = –10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7) / (50 \times 0.01) = -14.0 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $1.6\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141			20.0 ^{Note 2}	mA
		Per pin for P60 to P63			15.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70% ^{Note 3})	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$		15.0	mA
			$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		9.0	mA
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$		4.5	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77 (When duty = 70% ^{Note 3})	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$		35.0	mA
			$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		20.0	mA
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$		10.0	mA
		Total of all pins (When duty = 70% ^{Note 3})			50.0	mA
	I _{OL2}	Per pin for P20 to P27, P150 to P154			0.4 ^{Note 2}	mA
		Total of all pins (When duty = 70% ^{Note 3})	$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$		5.2	mA

- Notes**
1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0} and V_{SS} pin.
 2. However, do not exceed the total current value.
 3. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where n = 50% and I_{OL} = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(50 \times 0.01) = 14.0\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $1.6\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	Normal input buffer	$0.8EV_{DD0}$		EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer $3.3\text{ V} \leq EV_{DD0} < 3.6\text{ V}$	2.0		EV_{DD0}	V
			TTL input buffer $1.6\text{ V} \leq EV_{DD0} < 3.3\text{ V}$	1.5		EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P154		$0.7AV_{DD}$		AV_{DD}	V
	V_{IH4}	P60 to P63		$0.7EV_{DD0}$		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	Normal input buffer	0		$0.2EV_{DD0}$	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer $3.3\text{ V} \leq EV_{DD0} < 3.6\text{ V}$	0		0.5	V
			TTL input buffer $1.6\text{ V} \leq EV_{DD0} < 3.3\text{ V}$	0		0.32	V
	V_{IL3}	P20 to P27, P150 to P154		0		$0.3AV_{DD}$	V
	V_{IL4}	P60 to P63		0		$0.3EV_{DD0}$	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		$0.2V_{DD}$	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 is EV_{DD0} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $1.6\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $I_{OH1} = -2.0\text{ mA}$	$EV_{DD0} - 0.6$		V
			$1.8\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $I_{OH1} = -1.5\text{ mA}$	$EV_{DD0} - 0.5$		V
			$1.6\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $I_{OH1} = -1.0\text{ mA}$	$EV_{DD0} - 0.5$		V
	V_{OH2}	P20 to P27, P150 to P154	$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$	$AV_{DD} - 0.5$		V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $I_{OL1} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $I_{OL1} = 1.5\text{ mA}$		0.4	V
			$1.8\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $I_{OL1} = 0.6\text{ mA}$		0.4	V
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$, $I_{OL1} = 0.3\text{ mA}$		0.4	V
	V_{OL2}	P20 to P27, P150 to P154	$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$		0.4	V
	V_{OL3}	P60 to P63	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $I_{OL3} = 3.0\text{ mA}$		0.4	V
			$1.8\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $I_{OL3} = 2.0\text{ mA}$		0.4	V
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$, $I_{OL3} = 1.0\text{ mA}$		0.4	V

Caution P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $1.6\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I _{LH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P140, P141	V _I = EV _{DD0}		1	μA		
	I _{LH2}	P137, RESET	V _I = V _{DD}		1	μA		
	I _{LH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input	1	μA		
				In resonator connection	10	μA		
	I _{LH4}	P20 to P27, P150 to P154	V _I = AV _{DD}		1	μA		
Input leakage current, low	I _{LIL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P67, P70 to P77, P120, P140, P141	V _I = EV _{SS0}		−1	μA		
	I _{LIL2}	P137, RESET	V _I = V _{SS}		−1	μA		
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input	−1	μA		
				In resonator connection	−10	μA		
	I _{LIL4}	P20 to P27, P150 to P154	V _I = AV _{SS}		−1	μA		
On-chip pll-up resistance	R _U	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	V _I = EV _{SS0} , In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

29.3.2 Supply current characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

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Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} ^{Note 1}	Operating mode	HS (high-speed main) mode ^{Note 5}	$f_{\text{IH}} = 32\text{ MHz}$ ^{Note 3}	Basic operation	$\text{V}_{\text{DD}} = 3.0\text{ V}$		2.1		mA
					Normal operation	$\text{V}_{\text{DD}} = 3.0\text{ V}$		4.6	7.0	mA
				$f_{\text{IH}} = 24\text{ MHz}$ ^{Note 3}	Normal operation	$\text{V}_{\text{DD}} = 3.0\text{ V}$		3.7	5.5	mA
					Normal operation	$\text{V}_{\text{DD}} = 3.0\text{ V}$		2.7	4.0	mA
			LS (low-speed main) mode ^{Note 5}	$f_{\text{IH}} = 8\text{ MHz}$ ^{Note 3}	Normal operation	$\text{V}_{\text{DD}} = 3.0\text{ V}$		1.2	1.8	mA
						$\text{V}_{\text{DD}} = 2.0\text{ V}$		1.2	1.8	mA
			LV (Low-voltage main) mode ^{Note 5}	$f_{\text{IH}} = 4\text{ MHz}$ ^{Note 3}	Normal operation	$\text{V}_{\text{DD}} = 3.0\text{ V}$		1.2	1.7	mA
						$\text{V}_{\text{DD}} = 2.0\text{ V}$		1.2	1.7	mA
			HS (high-speed main) mode ^{Note 5}	$f_{\text{MX}} = 20\text{ MHz}$ ^{Note 2} , $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				$f_{\text{MX}} = 10\text{ MHz}$ ^{Note 2} , $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
			LS (low-speed main) mode ^{Note 5}	$f_{\text{MX}} = 8\text{ MHz}$ ^{Note 2} , $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
				$f_{\text{MX}} = 8\text{ MHz}$ ^{Note 2} , $\text{V}_{\text{DD}} = 2.0\text{ V}$	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
			Subsystem clock mode	$f_{\text{SUB}} = 32.768\text{ kHz}$ ^{Note 4} $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				$f_{\text{SUB}} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.2	4.9	μA
						Resonator connection		4.3	5.0	μA
				$f_{\text{SUB}} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		4.3	5.5	μA
						Resonator connection		4.4	5.6	μA
				$f_{\text{SUB}} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		4.5	6.3	μA
						Resonator connection		4.6	6.4	μA
				$f_{\text{SUB}} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		4.8	7.7	μA
						Resonator connection		4.9	7.8	μA

(Notes and Remarks are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time counter interval timer and watchdog timer is stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

<R>	HS (high-speed main) mode:		$V_{DD} = 2.7\text{ V to }3.6\text{ V@1 MHz to }32\text{ MHz}$
			$V_{DD} = 2.4\text{ V to }3.6\text{ V@1 MHz to }16\text{ MHz}$
	LS (low-speed main) mode:		$V_{DD} = 1.8\text{ V to }3.6\text{ V@1 MHz to }8\text{ MHz}$
	LV (Low-voltage main) mode:		$V_{DD} = 1.6\text{ V to }3.6\text{ V@1 MHz to }4\text{ MHz}$

Remarks 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH} : High-speed on-chip oscillator clock frequency

3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)**(2/3)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} ^{Note 2}	HALT mode	HS (high-speed main) mode ^{Note 7}	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 3.0 V		0.54	1.63	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 3.0 V		0.44	1.28	mA	
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 3.0 V		0.40	1.00	mA	
			LS (low-speed main) mode ^{Note 7}	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		270	530	μA	
					V _{DD} = 2.0 V		270	530	μA	
			LV (Low-voltage main) mode ^{Note 7}	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V		435	640	μA	
					V _{DD} = 2.0 V		435	640	μA	
			HS (high-speed main) mode ^{Note 7}	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
			LS (low-speed main) mode ^{Note 7}	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380	μA	
				f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380	μA	
			Subsystem clock mode	f _{SUB} = 32.768 kHz ^{Note 5} T _A = −40°C	Square wave input		0.25	0.57	μA	
					Resonator connection		0.44	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input		0.30	0.57	μA	
					Resonator connection		0.49	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input		0.38	1.17	μA	
					Resonator connection		0.57	1.36	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.52	1.97	μA	
					Resonator connection		0.71	2.16	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input		0.97	3.37	μA	
					Resonator connection		1.16	3.56	μA	
	I _{DD3} ^{Note 6}	STOP mode ^{Note 8}	T _A = −40°C					0.16	0.50	μA
			T _A = +25°C					0.23	0.50	μA
			T _A = +50°C					0.34	1.10	μA
			T _A = +70°C					0.46	1.90	μA
			T _A = +85°C					0.75	3.30	μA

(Notes and Remarks are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, the A/D converter, and LVD circuit are stopped.

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator and subsystem clock are stopped.
4. When high-speed system clock and subsystem clock are stopped.

<R> 5. When operating real-time clock (RTC), $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). When high-speed on-chip oscillator and high-speed system clock are stopped. When interval timer and watchdog timer are stopped. The values below the MAX. column include the leakage current.

6. When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.

<R> 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 32 MHz

$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 16 MHz

LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} < 3.6\text{ V}$ @ 1 MHz to 8 MHz

LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ @ 1 MHz to 4 MHz

<R> 8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.

Remarks 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH} : High-speed on-chip oscillator clock frequency

3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

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	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	RTC operating current	I _{RTC} ^{Notes 1, 2}			0.02 ^{Note 3}		μA
	Interval timer operating current	I _{IT} ^{Notes 2, 4}			0.02 ^{Note 3}		μA
<R>	Watchdog timer operating current	I _{WDT} ^{Notes 2, 5}	f _{IL} = 15 kHz, f _{MAIN} is stopped		0.22		μA
<R>	A/D converter operating current	I _{ADC} ^{Notes 6, 7}	AV _{DD} = 3.0 V, When conversion at maximum speed		420	720	μA
<R>	AV _{REF} (+) current	I _{AVREF} ^{Note 8}	AV _{DD} = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 ^{Note 7}		14.0	25.0	μA
			AV _{REFP} = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 ^{Note 10}		14.0	25.0	μA
			ADREFP1 = 1, ADREFP0 = 0 ^{Note 11}		14.0	25.0	μA
<R>	A/D converter reference voltage current	I _{ADREF} ^{Note 9}	V _{DD} = 3.0 V ^{Note 11}		75.0		μA
<R>	Temperature sensor operating current	I _{TMPS}	V _{DD} = 3.0 V ^{Note 11}		75.0		μA
	LVD operating current	I _{LVI} ^{Note 12}			0.08		μA
	BGO operating current	I _{BGO} ^{Note 13}			2.5	12.2	mA
<R>	SNOOZE operating current	I _{SNOZ}	A/D converter operation (AV _{DD} = 3.0 V)	The mode is performed ^{Notes 11, 14}	0.50	0.60	mA
				During A/D conversion ^{Note 11}	0.60	0.75	mA
				During A/D conversion ^{Note 7H}	420	720	μA
			CSI/UART operation ^{Note 11}		0.70	0.84	mA

Notes 1. Current flowing only to the real-time clock (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78/G1A microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. However, I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

<R> 3. Add 200 μA when using f_{IL}.

4. Current flowing only to the interval timer (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78/G1A microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the interval timer operates in operation mode or HALT mode.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78/G1A is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when f_{CLK} = f_{SUB} when the watchdog timer operates.

6. Current flowing only to the A/D converter. The current value of the RL78/G1A is the sum of I_{DD1} or I_{DD2} and I_{ADC}, I_{AVREF}, I_{ADREF} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing to the AV_{DD}.

8. Current flowing from the reference voltage source of A/D converter.

9. Operation current flowing to the internal reference voltage.

10. Current flowing to the AV_{REFP}.

11. Current flowing to the V_{DD}.

12. Current flowing only to the LVD circuit. The current value of the RL78/G1A is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.

13. Current flowing only to the BGO. The current value of the RL78/G1A is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in an operation mode.

<R> 14. Refer to 18.3.3 SNOOZE mode for shift time to the SNOOZE mode.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

29.4 AC Characteristics

29.4.1 Basic operation

<R> (T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{main}) mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LV (Low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 3.6 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 3.6 V	0.125		1	μs
		Subsystem clock (f _{SUB}) operation		1.8 V ≤ V _{DD} ≤ 3.6 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LV (Low-voltage main) mode	1.8 V ≤ V _{DD} ≤ 3.6 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 3.6 V	0.125		1	μs
External main system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 3.6 V		1.0		20.0	MHz	
		1.8 V ≤ V _{DD} < 2.7 V		1.0		8.0	MHz	
		1.6 V ≤ V _{DD} < 1.8 V		1.0		4.0	MHz	
	f _{EXS}			32		35	kHz	
External main system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 3.6 V		24			ns	
		1.8 V ≤ V _{DD} < 2.7 V		60			ns	
		1.6 V ≤ V _{DD} < 1.8 V		120			ns	
	t _{EXHS} , t _{EXLS}			13.7			μs	
TI00, TI01, TI03 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} +10			ns ^{Note}	
TO00, TO01, TO03 to TO07 output frequency	f _{TO}	HS (high-speed main) mode	2.7 V ≤ EV _{DD0} ≤ 3.6 V			8	MHz	
			1.8 V ≤ EV _{DD0} < 2.7 V			4	MHz	
			1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz	
		LV (Low-voltage main) mode	1.6 V ≤ EV _{DD0} ≤ 3.6 V			2	MHz	
			LS (low-speed main) mode	1.8 V ≤ EV _{DD0} ≤ 3.6 V			4	MHz
		1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz		
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	2.7 V ≤ EV _{DD0} ≤ 3.6 V			8	MHz	
			1.8 V ≤ EV _{DD0} < 2.7 V			4	MHz	
			1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz	
		LV (Low-voltage main) mode	1.8 V ≤ EV _{DD0} ≤ 3.6 V			4	MHz	
			1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz	
		LS (low-speed main) mode	1.8 V ≤ EV _{DD0} ≤ 3.6 V			4	MHz	
1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz				
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	1.6 V ≤ V _{DD} ≤ 3.6 V	1			μs	
		INTP1 to INTP11	1.6 V ≤ EV _{DD0} ≤ 3.6 V	1			μs	
Key interrupt input high-level width, low-level width	t _{KR}	KR0 to KR9	1.8 V ≤ EV _{DD0} ≤ 3.6 V, 1.8 V ≤ AV _{DD} ≤ 3.6 V	250			ns	
			1.6 V ≤ EV _{DD0} < 1.8 V, 1.6 V ≤ AV _{DD} < 1.8 V	1			μs	
RESET low-level width	t _{RSL}			10			μs	

(Note, Caution and Remark are listed on the next page.)

Note The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$

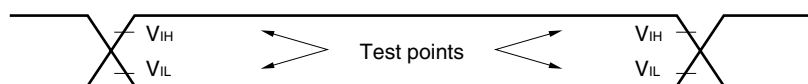
$1.8\text{ V} \leq E_{VDD0} < 2.7\text{ V}$: MIN. 125 ns

$1.6\text{ V} \leq E_{VDD0} < 1.8\text{ V}$: MIN. 250 ns

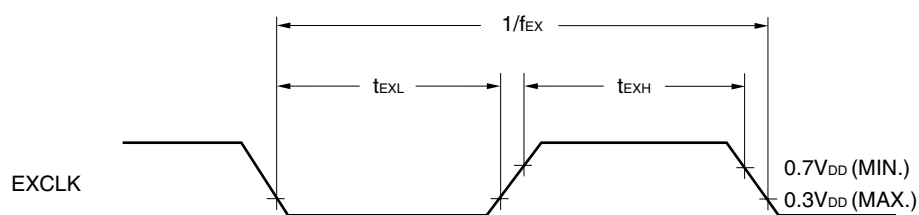
Remark f_{MCK} : Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

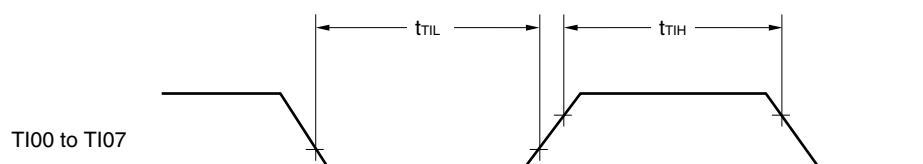
<R> AC Timing Test Points



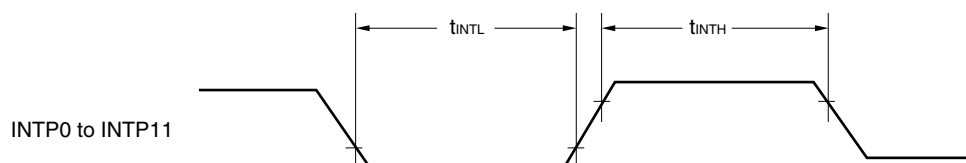
External System Clock Timing

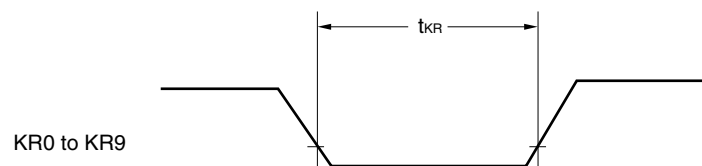
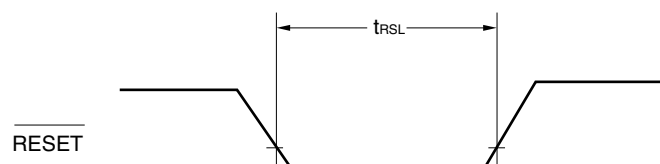


TI/TO Timing



Interrupt Request Input Timing



Key Interrupt Input Timing **$\overline{\text{RESET}}$ Input Timing**

29.5 Peripheral Functions Characteristics

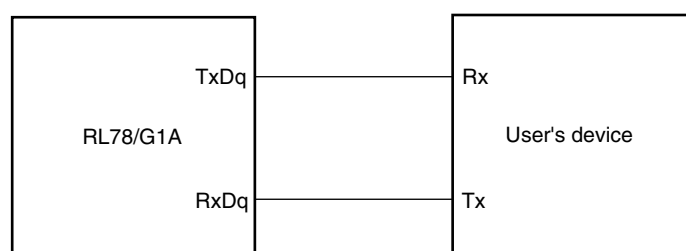
29.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

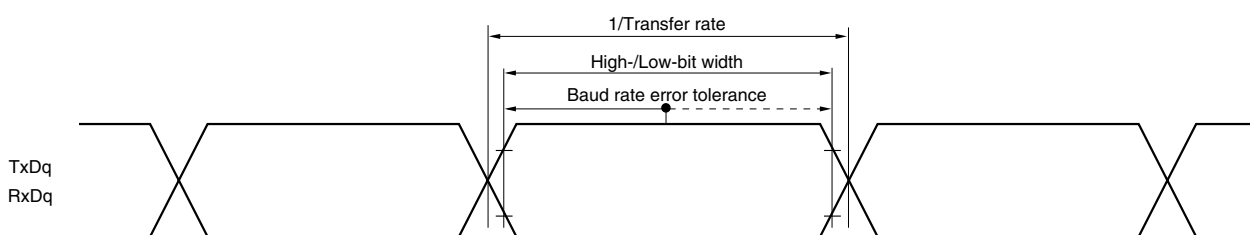
($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD0}} \leq V_{\text{DD}} \leq 3.6\text{ V}$, $V_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate ^{Note 1}					$f_{\text{MCK}}/6$ ^{Note 2}	bps
		Theoretical value of the maximum transfer rate $f_{\text{CLK}} = 32\text{ MHz}$, $f_{\text{MCK}} = f_{\text{CLK}}$			5.3	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Notes 1. Transfer rate in the SNOOZE mode is max. 9600 bps, min. 4800 bps.

2. The following conditions are required for low voltage interface when $\text{EV}_{\text{DD0}} < V_{\text{DD}}$.

$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$: MAX. 2.6 Mbps

$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 2.4\text{ V}$: MAX. 1.3 Mbps

$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$: MAX. 0.6 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

2. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

<R> (2) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output corresponding CSI00 only)

(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t _{KCY1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V t _{KCY1} ≥ 2/f _{CLK}	83.3 ^{Notes 1, 2}			ns
$\overline{\text{SCKp}}$ high-/low-level width	t _{KH1} , t _{KL1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	t _{KCY1} /2 – 10			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) ^{Note 3}	t _{SIK1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	33			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) ^{Note 4}	t _{SIH1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	10			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output ^{Note 5}	t _{KSO1}	C = 20 pF ^{Note 6}			10	ns

Notes 1. The value must also be 2/f_{CLK} or more.

2. Using the f_{MCK} within 24 MHz.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to $\overline{\text{SCKp}}\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from $\overline{\text{SCKp}}\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from $\overline{\text{SCKp}}\uparrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. C is the load capacitance of the $\overline{\text{SCKp}}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

<R> (3) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output)
 ($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ $t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	125 ^{Note 1}			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ $t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	250 ^{Note 1}			ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ $t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	500 ^{Note 1}			ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ $t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	1000 ^{Note 1}			ns
$\overline{\text{SCKp}}$ high-/low-level width	$t_{\text{KH1}},$ t_{KL1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$t_{\text{KCY1}}/2 - 18$			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$t_{\text{KCY1}}/2 - 38$			ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$t_{\text{KCY1}}/2 - 50$			ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$t_{\text{KCY1}}/2 - 100$			ns
<R> SIp setup time (to $\overline{\text{SCKp}}\uparrow$) ^{Note 2}	t_{SIK1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	44			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	75			ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	110			ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	220			ns
<R> SIp hold time (from $\overline{\text{SCKp}}\uparrow$) ^{Note 3}	t_{SI1}		19			ns
<R> Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output ^{Note 4}	t_{KSO1}	$C = 30\text{ pF}$ ^{Note 5}			25	ns

Notes 1. The value must also be $4/f_{\text{CLK}}$ or more.

2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The SIp setup time becomes “to $\overline{\text{SCKp}}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The SIp hold time becomes “from $\overline{\text{SCKp}}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
4. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from $\overline{\text{SCKp}}\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
5. C is the load capacitance of the $\overline{\text{SCKp}}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
 g: PIM and POM numbers (g = 0, 1)

(4) During communication at same potential (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time ^{Note 5}	t _{KCY2}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	16 MHz < f _{MCK}	8/f _{MCK}		ns
			f _{MCK} ≤ 16 MHz	6/f _{MCK}		ns
		1.8 V ≤ EV _{DD0} < 2.7 V	16 MHz < f _{MCK}	8/f _{MCK}		ns
			f _{MCK} ≤ 16 MHz	6/f _{MCK}		ns
		1.6 V ≤ EV _{DD0} < 1.8 V		6/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	1.6 V ≤ EV _{DD0} ≤ 3.6 V	t _{KCY2} /2			ns
<R> SIp setup time (to $\overline{\text{SCKp}}\uparrow$) ^{Note 1}	t _{SIK2}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	1/f _{MCK} + 20			ns
		1.8 V ≤ EV _{DD0} < 2.7 V	1/f _{MCK} + 30			ns
		1.6 V ≤ EV _{DD0} < 1.8 V	1/f _{MCK} + 40			ns
<R> SIp hold time (from $\overline{\text{SCKp}}\uparrow$) ^{Note 2}	t _{KSI2}	2.7 V ≤ EV _{DD0} ≤ 3.6 V	1/f _{MCK} +31			ns
		1.8 V ≤ EV _{DD0} < 2.7 V	1/f _{MCK} +31			ns
		1.6 V ≤ EV _{DD0} < 1.8 V	1/f _{MCK} + 250			ns
<R> Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	2.7 V ≤ EV _{DD0} ≤ 3.6 V		2/f _{MCK} +44	ns
			2.4 V ≤ EV _{DD0} < 2.7 V		2/f _{MCK} +75	ns
			1.8 V ≤ EV _{DD0} < 2.4 V		2/f _{MCK} +110	ns
			1.6 V ≤ EV _{DD0} < 1.8 V		2/f _{MCK} +220	ns

Notes 1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The SIp setup time becomes “to $\overline{\text{SCKp}}\downarrow$ ” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The SIp hold time becomes “from $\overline{\text{SCKp}}\uparrow$ ” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from $\overline{\text{SCKp}}\uparrow$ ” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

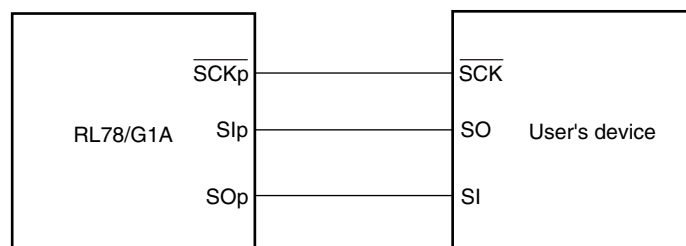
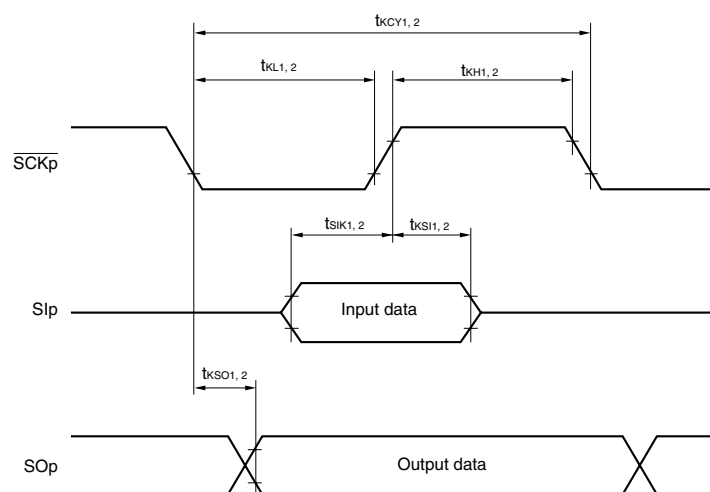
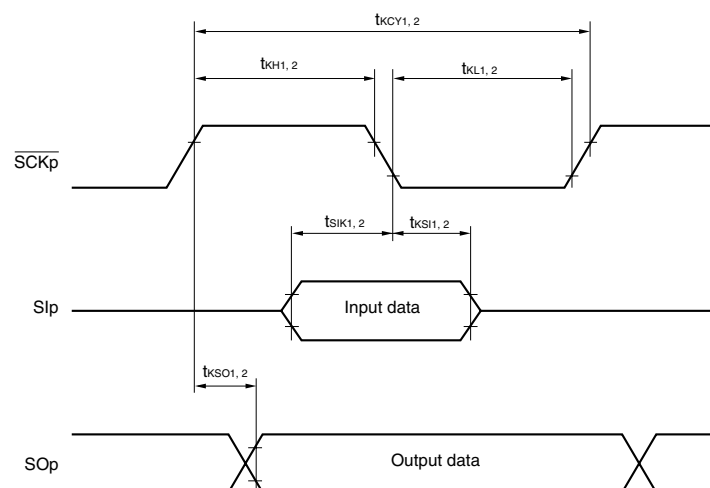
4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

<R> **Caution** Select the normal input buffer for the SIp pin and $\overline{\text{SCKp}}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

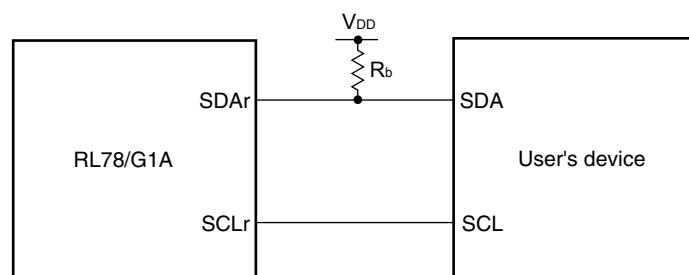
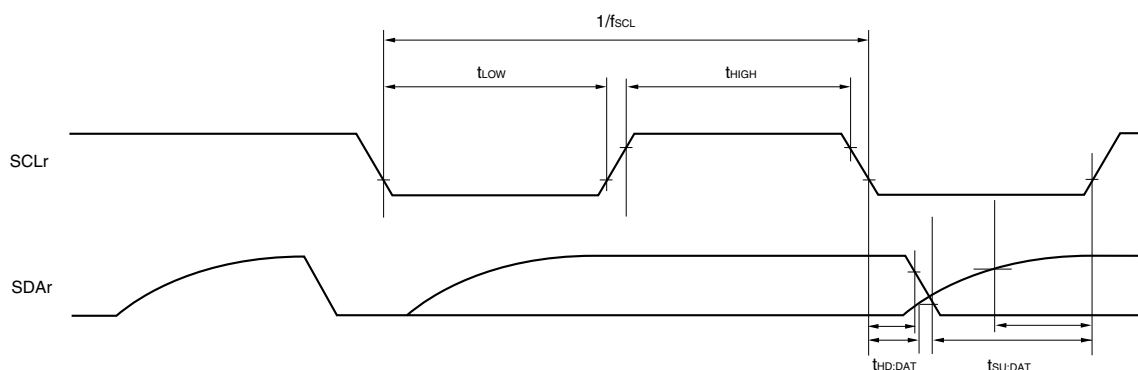
CSI mode connection diagram (during communication at same potential)
CSI mode serial transfer timing (during communication at same potential)
 (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (during communication at same potential)
 (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)


- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21)
 2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(5) During communication at same potential (simplified I²C mode)**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = V_{SS0} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq V_{DD0} \leq 3.6\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		1000 ^{Note 1}	kHz
		$1.8\text{ V} \leq V_{DD0} \leq 3.6\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$		400 ^{Note 1}	kHz
		$1.8\text{ V} \leq V_{DD0} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$		300 ^{Note 1}	kHz
		$1.6\text{ V} \leq V_{DD0} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$		250 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq V_{DD0} \leq 3.6\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	475		ns
		$1.8\text{ V} \leq V_{DD0} \leq 3.6\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	1150		ns
		$1.8\text{ V} \leq V_{DD0} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	1550		ns
		$1.6\text{ V} \leq V_{DD0} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	1850		ns
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq V_{DD0} \leq 3.6\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	475		ns
		$1.8\text{ V} \leq V_{DD0} \leq 3.6\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	1150		ns
		$1.8\text{ V} \leq V_{DD0} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	1550		ns
		$1.6\text{ V} \leq V_{DD0} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	1850		ns
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq V_{DD0} \leq 3.6\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 85$ ^{Note 2}		ns
		$1.8\text{ V} \leq V_{DD0} \leq 3.6\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 145$ ^{Note 2}		ns
		$1.8\text{ V} \leq V_{DD0} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	$1/f_{\text{MCK}} + 230$ ^{Note 2}		ns
		$1.6\text{ V} \leq V_{DD0} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	$1/f_{\text{MCK}} + 290$ ^{Note 2}		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq V_{DD0} \leq 3.6\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	305	ns
		$1.8\text{ V} \leq V_{DD0} \leq 3.6\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	355	ns
		$1.8\text{ V} \leq V_{DD0} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	0	405	ns
		$1.6\text{ V} \leq V_{DD0} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	0	405	ns

<R> **Notes 1.** The value must also be $f_{\text{CLK}}/4$ or lower.**2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".**(Caution and Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

<R> Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number, mn = 00 to 03, 10, 11)

(6) Communication at different potential (2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		reception	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$			$f_{MCK}/6$ ^{Note 1}	bps
				Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$		5.3	Mbps
			$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$			$f_{MCK}/6$ Notes 1 to 3	bps
				Theoretical value of the maximum transfer rate $f_{CLK} = 8\text{ MHz}$, $f_{MCK} = f_{CLK}$		1.3	Mbps

Notes 1. Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps**2.** Use it with $EV_{DD0} \geq V_b$.**3.** The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$. $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MAX. 2.6 Mbps $1.8\text{ V} \leq EV_{DD0} < 2.4\text{ V}$: MAX. 1.3 Mbps $1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$: MAX. 0.6 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. $V_b[V]$: Communication line voltage**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)**3.** f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(6) Communication at different potential (2.5 V) (UART mode) (dedicated baud rate generator output) (2/2)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		transmission	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V			Notes 1, 2	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V			1.2 ^{Note 5}	Mbps
			1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			Notes 1, 4, 5	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V			0.43 ^{Note 6}	Mbps

Notes 1. Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps

2. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} ≤ 3.6 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \quad [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

3. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 2 above to calculate the maximum transfer rate under conditions of the customer.

4. Use it with EV_{DD0} ≥ V_b.

5. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \quad [\%]$$

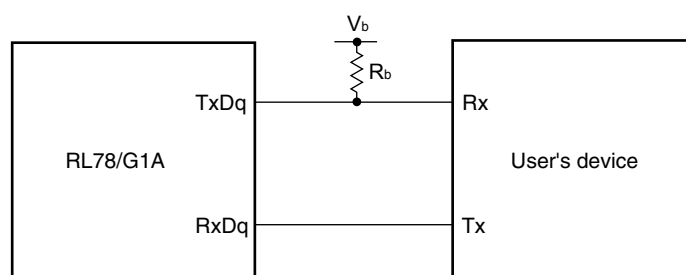
* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 7 above to calculate the maximum transfer rate under conditions of the customer.

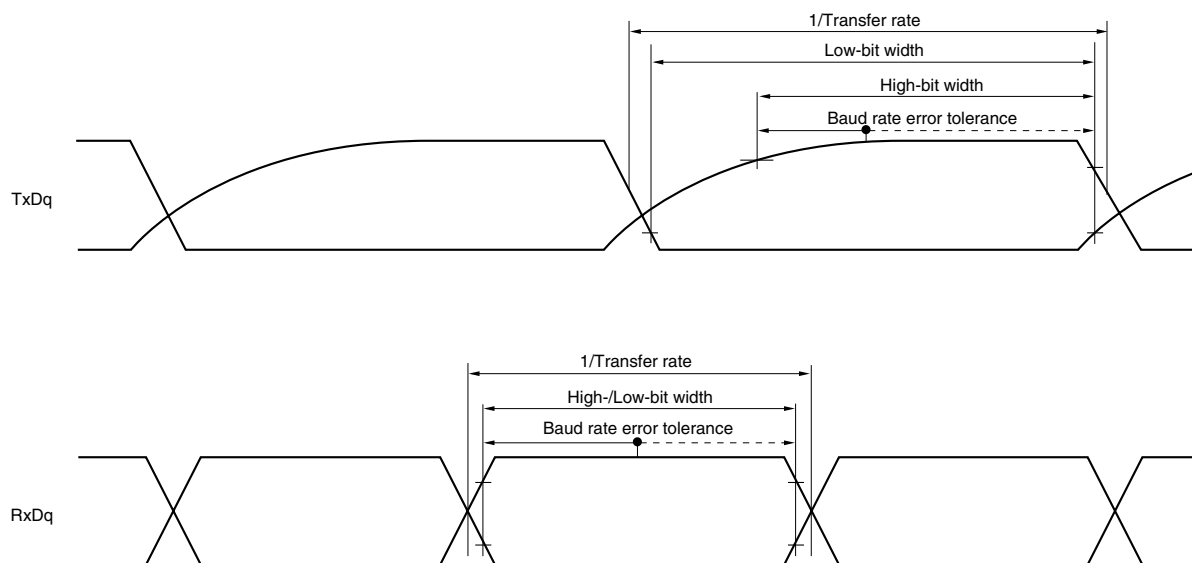
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

(7) Communication at different potential (2.5 V) (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output, corresponding CSI00 only)(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

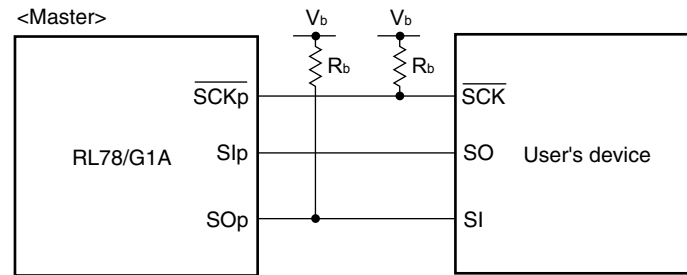
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t _{KCY1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	300 ^{Note 1}			ns
$\overline{\text{SCKp}}$ high-level width	t _{KH1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	t _{KCY1} /2 – 120			ns
$\overline{\text{SCKp}}$ low-level width	t _{KL1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	t _{KCY1} /2 – 10			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) ^{Note 2}	t _{SIK1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	121			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) ^{Note 2}	t _{KSI1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	10			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output ^{Note 2}	t _{KSO1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			130	ns
Slp setup time (to $\overline{\text{SCKp}}\downarrow$) ^{Note 3}	t _{SIK1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	33			ns
Slp hold time (from $\overline{\text{SCKp}}\downarrow$) ^{Note 3}	t _{KSI1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	10			ns
Delay time from $\overline{\text{SCKp}}\uparrow$ to SOp output ^{Note 3}	t _{KSO1}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			10	ns

Notes 1. The value must also be 2/f_{CLK} or more.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

3. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(Caution and Remark are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks 1.** $R_b[\Omega]$: Communication line ($\overline{\text{SCKp}}$, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line ($\overline{\text{SCKp}}$, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
- 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 1)

(8) Communication at different potential (2.5 V) (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output) (1/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	500 ^{Note}		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	1150 ^{Note}		ns
$\overline{\text{SCKp}}$ high-level width	t_{KH1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 170$			ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 458$			ns
$\overline{\text{SCKp}}$ low-level width	t_{KL1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 18$			ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 50$			ns

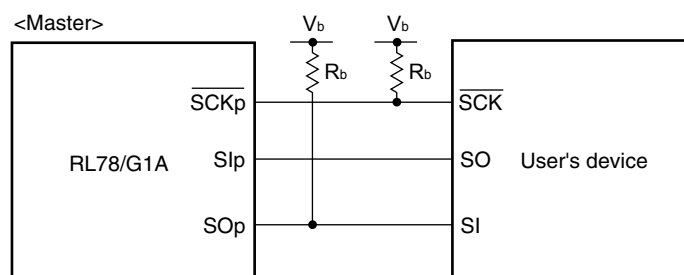
Note The value must also be $4/f_{\text{CLK}}$ or more.

- Cautions**
1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).
 2. Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.

- Remarks**
1. $\text{R}_b[\Omega]$: Communication line ($\overline{\text{SCKp}}$, SOp) pull-up resistance, $\text{C}_b[\text{F}]$: Communication line ($\overline{\text{SCKp}}$, SOp) load capacitance, $\text{V}_b[\text{V}]$: Communication line voltage
 2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)
 3. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(8) Communication at different potential (2.5 V) (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output) (2/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) ^{Note 1}	t_{SIK1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	177			ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	479			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) ^{Note 1}	t_{KSI1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	19			ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	19			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SO output ^{Note 1}	t_{KSO1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$			195	ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$			483	ns
Slp setup time (to $\overline{\text{SCKp}}\downarrow$) ^{Note 2}	t_{SIK1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	44			ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	110			ns
Slp hold time (from $\overline{\text{SCKp}}\downarrow$) ^{Note 2}	t_{KSI1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	19			ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	19			ns
Delay time from $\overline{\text{SCKp}}\uparrow$ to SO output ^{Note 2}	t_{KSO1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$			25	ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$			25	ns

Notes 1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.**CSI mode connection diagram (during communication at different potential)**

Cautions 1. Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

2. Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.

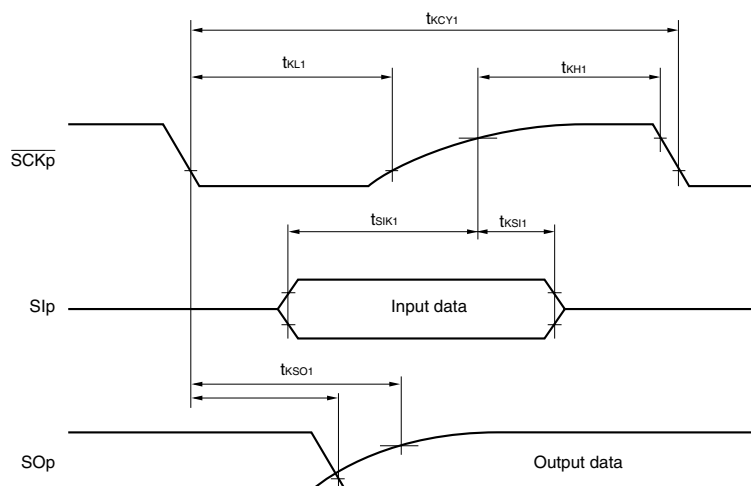
Remarks 1. $\text{R}_b[\Omega]$: Communication line ($\overline{\text{SCKp}}$, SOp) pull-up resistance, $\text{C}_b[\text{F}]$: Communication line ($\overline{\text{SCKp}}$, SOp) load capacitance, $\text{V}_b[\text{V}]$: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10),

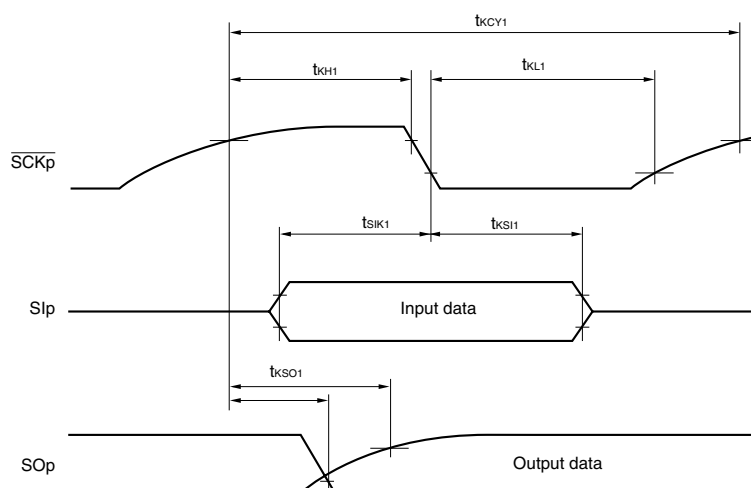
g: PIM and POM number (g = 0, 1)

3. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

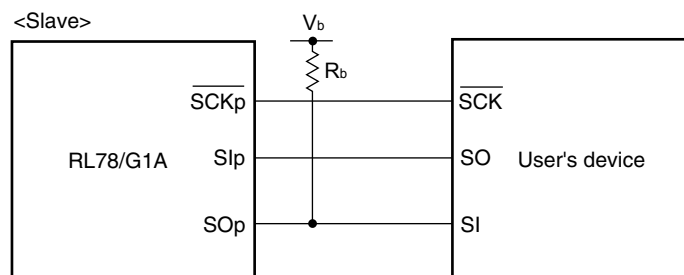
- Remarks**
1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (m = 00, 02, 10), g: PIM and POM number (g = 0, 1)
 2. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (2.5 V) (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input) $(T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time ^{Note 1}	t_{KCY2}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$20/f_{\text{MCK}}$			ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$16/f_{\text{MCK}}$			ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$14/f_{\text{MCK}}$			ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$12/f_{\text{MCK}}$			ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$8/f_{\text{MCK}}$			ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$6/f_{\text{MCK}}$			ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2}	$24\text{ MHz} < f_{\text{MCK}}$	$48/f_{\text{MCK}}$			ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$36/f_{\text{MCK}}$			ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$32/f_{\text{MCK}}$			ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$26/f_{\text{MCK}}$			ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$			ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$10/f_{\text{MCK}}$			ns
$\overline{\text{SCKp}}$ high-/low-level width	t_{KH2} , t_{KL2}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$t_{\text{KCY2}}/2 - 18$			ns	
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2}	$t_{\text{KCY2}}/2 - 50$			ns	
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) ^{Note 3}	t_{SIK2}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$1/f_{\text{MCK}} + 20$			ns	
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2}	$1/f_{\text{MCK}} + 30$			ns	
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) ^{Note 4}	t_{KSI2}		$1/f_{\text{MCK}} + 31$			ns	
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output ^{Note 5}	t_{KSO2}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$			$2/f_{\text{MCK}} + 214$	ns	
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$			$2/f_{\text{MCK}} + 573$	ns	

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps2. Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to $\overline{\text{SCKp}}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.4. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from $\overline{\text{SCKp}}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.5. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from $\overline{\text{SCKp}}\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

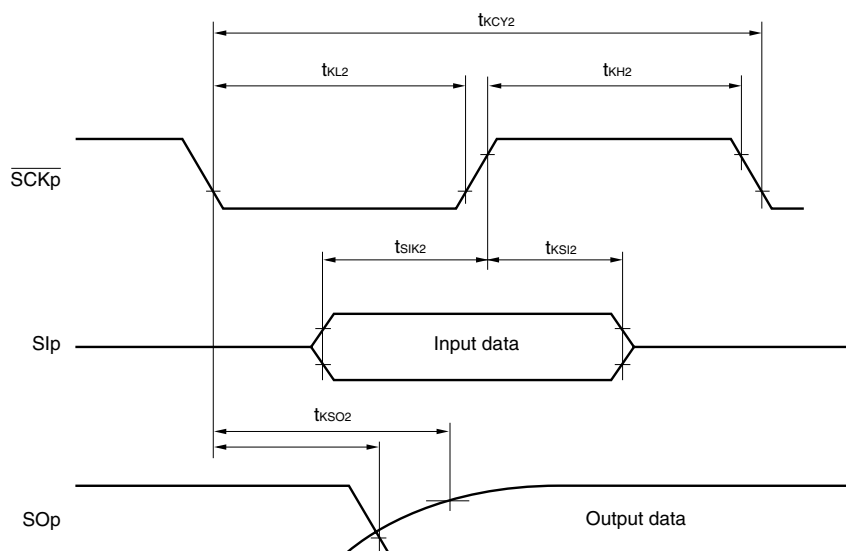
(Caution and Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

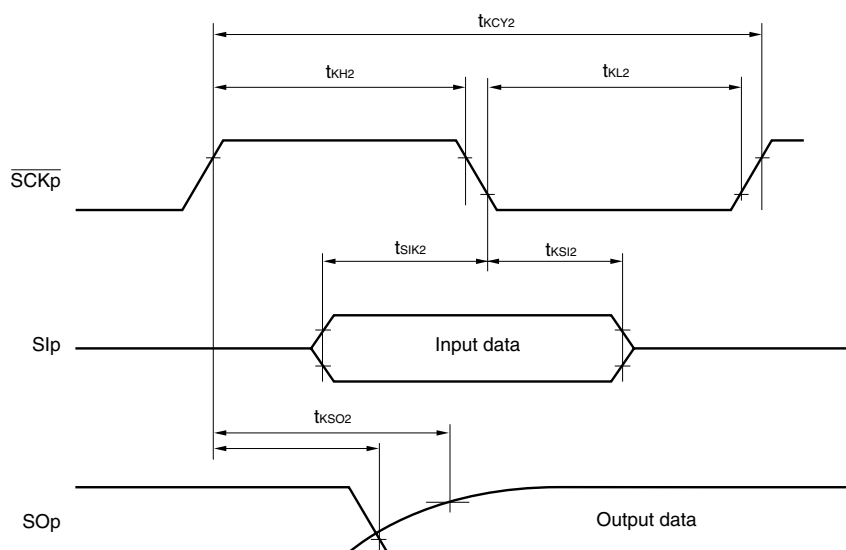
Caution Select the TTL input buffer for the Slp pin and $\overline{\text{SCKp}}$ pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number ($p = 00, 10, 20$), m: Unit number ($m = 0, 1$), n: Channel number ($n = 00, 02, 10$), g: PIM and POM number ($g = 0, 1$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00, 02, 10$))
 4. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the Slp pin and $\overline{\text{SCKp}}$ pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)
 2. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(10) Communication at different potential (2.5 V) (simplified I²C mode) (1/2)(T_A = -40 to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		1000 ^{Note 1}	kHz
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		400 ^{Note 1}	kHz
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$		300 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	475		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	1150		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	1550		ns
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	200		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	600		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	610		ns

(Notes, Caution and Remarks are listed on the next page.)

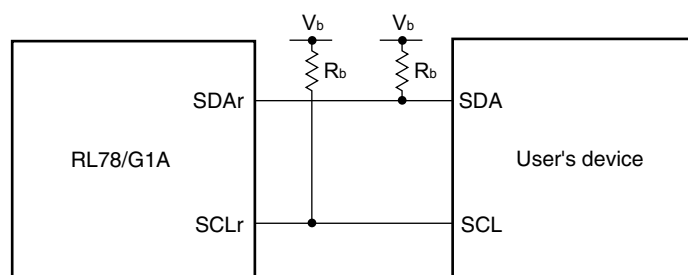
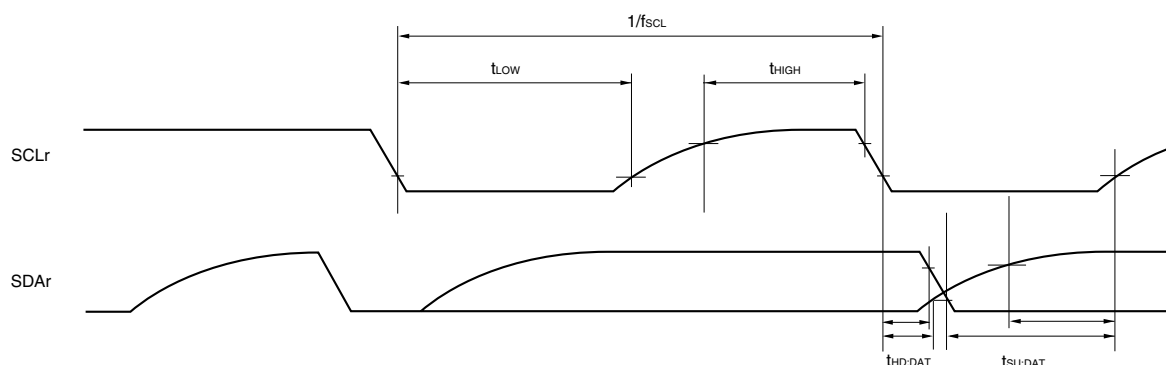
(10) Communication at different potential (2.5 V) (simplified I²C mode) (2/2)(T_A = -40 to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 135$ Note 3		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 190$ Note 3		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ Note 2, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$1/f_{\text{MCK}} + 190$ Note 3		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	0	305	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	0	355	ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ Note 2, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	0	405	ns

<R> **Notes 1.** The value must also be $f_{\text{CLK}}/4$ or lower.**2.** Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.**3.** Set the f_{MCK} value to keep the hold time of $\text{SCLr} = \text{"L"}$ and $\text{SCLr} = \text{"H"}$.

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(Remarks is listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))
 4. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

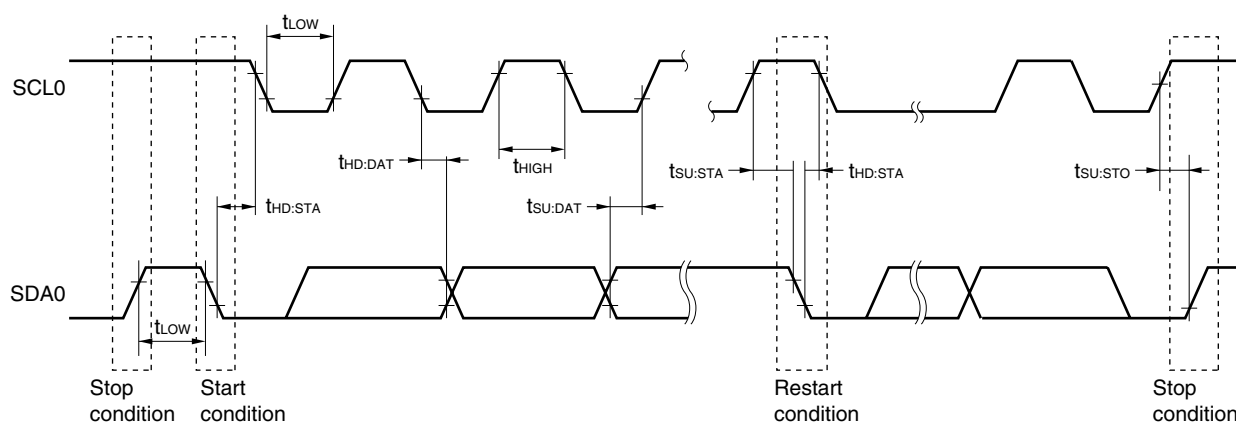
29.5.2 Serial interface IICA

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: $f_{\text{CLK}} \geq 10\text{ MHz}$					0	1000	kHz
		Fast mode: $f_{\text{CLK}} \geq 3.5\text{ MHz}$			0	400			kHz
		Normal mode: $f_{\text{CLK}} \geq 1\text{ MHz}$	0	100					kHz
Setup time of restart condition	$t_{\text{SU:STA}}$		4.7		0.6		0.26		μs
Hold time ^{Note 1}	$t_{\text{HD:STA}}$		4.0		0.6		0.26		μs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		0.5		μs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		0.26		μs
Data setup time (reception)	$t_{\text{SU:DAT}}$		250		100		50		ns
<R> Data hold time (transmission) ^{Note 2}	$t_{\text{HD:DAT}}$		0	3.45	0	0.9	0	0.45	μs
Setup time of stop condition	$t_{\text{SU:STO}}$		4.0		0.6		0.26		μs
Bus-free time	t_{BUF}		4.7		1.3		0.5		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of $t_{\text{HD:DAT}}$ is during normal transfer and a wait state is inserted in the $\overline{\text{ACK}}$ (acknowledge) timing.**Remark** The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.Standard mode: $C_b = 400\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ Fast mode: $C_b = 320\text{ pF}$, $R_b = 1.1\text{ k}\Omega$ Fast mode plus: $C_b = 120\text{ pF}$, $R_b = 1.1\text{ k}\Omega$

IICA serial transfer timing



29.5.3 On-chip debug (UART)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = V_{SS0} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			115.2 k		1 M	bps

29.6 Analog Characteristics

<R> 29.6.1 A/D converter characteristics

Division of A / D Converter Characteristics

Reference voltage Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = AV_{DD} Reference voltage (-) = AV_{SS}	Reference voltage (+) = Internal reference voltage Reference voltage (-) = AV_{SS}
High-accuracy channel ; ANI0 to ANI12 (input buffer power supply : AV_{DD})	See 29.6.1 (1)	See 29.6.1 (2)	See 29.6.1 (5)
Normal channel ; ANI16 to ANI30 (input buffer power supply : V_{DD} or EV_{DD0})	See 29.6.1 (3)	See 29.6.1 (4)	

(1) When $AV_{REF(+)} = AV_{REFP}/ANI0$ (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)} = AV_{REFM}/ANI1$ (ADREFM = 1), target ANI pin : ANI0 to ANI12

<R> (T_A = -40 to +85°C, $1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

<R>

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R _{ES}		2.4 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V	8		10 ^{Note 1}	
			1.6 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V	8 ^{Note 2}			
Overall error ^{Note 3}	AINL	12-bit resolution	2.4 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±2.5	
Conversion time	t _{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution ^{Note 1}	1.8 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution ^{Note 2}	1.6 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V	2.5625			
			1.8 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V	5.125			
			1.6 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V	10.25			
Zero-scale error ^{Note 3}	E _{ZS}	12-bit resolution	2.4 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±4.5	LSB
		10-bit resolution	1.8 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±4.5	
		8-bit resolution	1.6 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±2.0	
Full-scale error ^{Note 3}	E _{FS}	12-bit resolution	2.4 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±4.5	LSB
		10-bit resolution	1.8 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±4.5	
		8-bit resolution	1.6 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±2.0	
Integral linearity error ^{Note 3}	ILE	12-bit resolution	2.4 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±1.5	
		8-bit resolution	1.6 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±1.0	
Differential linearity error ^{Note 3}	DLE	12-bit resolution	2.4 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±1.5	LSB
		10-bit resolution	1.8 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±1.5	
		8-bit resolution	1.6 V ≤ AV _{REFP} ≤ AV _{DD} ≤ 3.6 V			±1.0	
Analog input voltage	V _{AIN}			0		AV _{REFP}	V
	V _{BGR}	Select interanal reference voltage output 2.4 V ≤ V _{DD} ≤ 3.6 V, HS (high-speed main) mode		1.38	1.45	1.5	V

- Notes**
1. Cannot be used for lower 2 bit of ADCR register
 2. Cannot be used for lower 4 bit of ADCR register
 3. Excludes quantization error (±1/2 LSB).

(2) When $AV_{REF(+)} = AV_{DD}$ ($ADREFP1 = 0$, $ADREFP0 = 0$), $AV_{REF(-)} = AV_{SS}$ ($ADREFM = 0$), target ANI pin : ANI0 to ANI12

<R> ($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{DD} , Reference voltage (-) = $AV_{SS} = 0\text{ V}$)

<R>	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
	Resolution	RES		2.4 V ≤ AVDD ≤ 3.6 V	8		12	bit
				1.8 V ≤ AVDD ≤ 3.6 V	8		10 ^{Note 1}	
				1.6 V ≤ AVDD ≤ 3.6 V	8 ^{Note 2}			
Overall error ^{Note 3}	AINL	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±7.5	LSB	
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±5.5		
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±3.0		
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V	3.375			μs	
		ADTYP = 0, 10-bit resolution ^{Note 1}	1.8 V ≤ AVDD ≤ 3.6 V	6.75				
		ADTYP = 0, 8-bit resolution ^{Note 2}	1.6 V ≤ AVDD ≤ 3.6 V	13.5				
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V	2.5625				
			1.8 V ≤ AVDD ≤ 3.6 V	5.125				
			1.6 V ≤ AVDD ≤ 3.6 V	10.25				
Zero-scale error ^{Note 3}	EZS	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±6.0	LSB	
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±5.0		
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±2.5		
Full-scale error ^{Note 3}	EFS	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±6.0	LSB	
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±5.0		
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±2.5		
Integral linearity error ^{Note 3}	ILE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±3.0	LSB	
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±2.0		
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±1.5		
Differential linearity error ^{Note 3}	DLE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±2.0	LSB	
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±2.0		
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±1.5		
Analog input voltage	VAIN				0		AVDD	V
	VBGR	Select interanal reference voltage output 2.4 V ≤ VDD ≤ 3.6 V, HS (high-speed main) mode			1.38	1.45	1.5	V

Notes 1. Cannot be used for lower 2 bit of ADCR register

2. Cannot be used for lower 4 bit of ADCR register

3. Excludes quantization error ($\pm 1/2$ LSB).

(3) When $AV_{REF(+)} = AV_{REFP}/ANI0$ (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)} = AV_{REFM}/ANI1$ (ADREFM = 1), target ANI pin : ANI16 to ANI30

<R> (T_A = -40 to +85°C, $1.6\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

<R>

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		$2.4\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$	8		12	bit
			$1.8\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$	8		10 ^{Note 1}	
			$1.6\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$	8 ^{Note 2}			
Overall error ^{Note 3}	AINL	12-bit resolution	$2.4\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±7.0	LSB
		10-bit resolution	$1.8\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±5.5	
		8-bit resolution	$1.6\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±3.0	
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	$2.4\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$	4.125			μs
		ADTYP = 0, 10-bit resolution ^{Note 1}	$1.8\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$	9.5			
		ADTYP = 0, 8-bit resolution ^{Note 2}	$1.6\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$	57.5			
		ADTYP = 1, 8-bit resolution	$2.4\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$	3.3125			
			$1.8\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$	7.875			
			$1.6\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$	54.25			
Zero-scale error ^{Notes 3}	EVS	12-bit resolution	$2.4\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±5.0	LSB
		10-bit resolution	$1.8\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±5.0	
		8-bit resolution	$1.6\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±2.5	
Full-scale error ^{Notes 3}	EFS	12-bit resolution	$2.4\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±5.0	LSB
		10-bit resolution	$1.8\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±5.0	
		8-bit resolution	$1.6\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±2.5	
Integral linearity error ^{Note 3}	ILE	12-bit resolution	$2.4\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±3.0	LSB
		10-bit resolution	$1.8\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±2.0	
		8-bit resolution	$1.6\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±1.5	
Differential linearity error ^{Note 3}	DLE	12-bit resolution	$2.4\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±2.0	LSB
		10-bit resolution	$1.8\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±2.0	
		8-bit resolution	$1.6\text{ V} \leq \text{AVREFP} \leq \text{AVDD} \leq 3.6\text{ V}$			±1.5	
Analog input voltage	VAIN			0		AVREFP and EVDD0	V
	VBGR	Select interanal reference voltage output 2.4 V ≤ VDD ≤ 3.6 V, HS (high-speed main) mode		1.38	1.45	1.5	V

- Notes**
1. Cannot be used for lower 2 bit of ADCR register
 2. Cannot be used for lower 4 bit of ADCR register
 3. Excludes quantization error (±1/2 LSB).

(4) When $AV_{REF(+)} = AV_{DD}$ ($ADREFP1 = 0$, $ADREFP0 = 0$), $AV_{REF(-)} = AV_{SS}$ ($ADREFM = 0$), target ANI pin : ANI16 to ANI30

<R> ($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} \leq V_{DD0} \leq 3.6\text{ V}$, $1.6\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{DD} , Reference voltage (-) = $AV_{SS} = 0\text{ V}$)

<R>

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AVDD ≤ 3.6 V	8		12	bit
			1.8 V ≤ AVDD ≤ 3.6 V	8		10 ^{Note 1}	
			1.6 V ≤ AVDD ≤ 3.6 V	8 ^{Note 2}			
Overall error ^{Note 3}	AINL	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.5	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±6.0	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±3.5	
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution ^{Note 1}	1.8 V ≤ AVDD ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution ^{Note 2}	1.6 V ≤ AVDD ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V	3.3125			μs
	1.8 V ≤ AVDD ≤ 3.6 V		7.875				
	1.6 V ≤ AVDD ≤ 3.6 V		54.25				
Zero-scale error ^{Note 3}	EVS	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±3.0	
Full-scale error ^{Note 3}	EFS	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±3.0	
Integral linearity error ^{Note 3}	ILE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±3.5	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±1.5	
Differential linearity error ^{Note 3}	DLE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±2.5	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±2.0	
Analog input voltage	VAIN			0		AVDD and EVDD0	V
	VBGR	Select interanal reference voltage output 2.4 V ≤ VDD ≤ 3.6 V, HS (high-speed main) mode		1.38	1.45	1.5	V

- Notes**
1. Cannot be used for lower 2 bit of ADCR register
 2. Cannot be used for lower 4 bit of ADCR register
 3. Excludes quantization error ($\pm 1/2$ LSB).

(5) When $AV_{REF(+)} =$ Internal reference voltage (1.45 V) ($ADREFP1 = 1$, $ADREFP0 = 0$), $AV_{REF(-)} = AV_{SS}$ ($ADREFM = 0$), target ANI pin : ANI0 to ANI12, ANI16 to ANI30

<R> ($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $1.6\text{ V} \leq EV_{DD} \leq V_{DD}$, $1.6\text{ V} \leq AV_{DD} \leq V_{DD}$, $V_{SS} = EV_{SS0} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = Internal reference voltage, Reference voltage (-) = $AV_{SS} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		8			bit
Conversion time	t_{CONV}	8-bit resolution	16			μs
Zero-scale error ^{Note}	E_{ZS}	8-bit resolution			± 4.0	LSB
Integral linearity error ^{Note}	I_{LE}	8-bit resolution			± 2.0	LSB
Differential linearity error ^{Note}	D_{LE}	8-bit resolution			± 2.5	LSB
Reference voltage (+)	$AV_{REF(+)}$	= Internal reference voltage (V_{BGR})	1.38	1.45	1.5	V
Analog input voltage	V_{AIN}		0		V_{BGR}	V

Note Excludes quantization error ($\pm 1/2$ LSB).

29.6.2 Temperature sensor, internal reference voltage output characteristics

<R> ($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Reference output voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/C
Operation stabilization wait time	t_{AMP}		10			μs

29.6.3 POR circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width	T_{PW}		300			μs
Detection delay time					350	μs

29.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, V_{PDR} ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
<R>	Detection voltage	V _{LVD2}	Power supply rise time	3.07	3.13	3.19	V		
			Power supply fall time	3.00	3.06	3.12	V		
		V _{LVD3}	Power supply rise time	2.96	3.02	3.08	V		
			Power supply fall time	2.90	2.96	3.02	V		
		V _{LVD4}	Power supply rise time	2.86	2.92	2.97	V		
			Power supply fall time	2.80	2.86	2.91	V		
		V _{LVD5}	Power supply rise time	2.76	2.81	2.87	V		
			Power supply fall time	2.70	2.75	2.81	V		
		V _{LVD6}	Power supply rise time	2.66	2.71	2.76	V		
			Power supply fall time	2.60	2.65	2.70	V		
		V _{LVD7}	Power supply rise time	2.56	2.61	2.66	V		
			Power supply fall time	2.50	2.55	2.60	V		
		V _{LVD8}	Power supply rise time	2.45	2.50	2.55	V		
			Power supply fall time	2.40	2.45	2.50	V		
		V _{LVD9}	Power supply rise time	2.05	2.09	2.13	V		
			Power supply fall time	2.00	2.04	2.08	V		
		V _{LVD10}	Power supply rise time	1.94	1.98	2.02	V		
			Power supply fall time	1.90	1.94	1.98	V		
		V _{LVD11}	Power supply rise time	1.84	1.88	1.91	V		
			Power supply fall time	1.80	1.84	1.87	V		
		V _{LVD12}	Power supply rise time	1.74	1.77	1.81	V		
			Power supply fall time	1.70	1.73	1.77	V		
		V _{LVD13}	Power supply rise time	1.64	1.67	1.70	V		
			Power supply fall time	1.60	1.63	1.66	V		
		Minimum pulse width		t _{LW}		300			μs
		Detection delay time						300	μs

<R> **Caution** Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: V_{DD} = 2.7 to 3.6 V@1 MHz to 32 MHz

V_{DD} = 2.4 to 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: V_{DD} = 1.8 to 3.6 V@1 MHz to 8 MHz

LV (low voltage main) mode: V_{DD} = 1.6 to 3.6 V@1 MHz to 4 MHz

Remark V_{LVD(n-1)} > V_{LVDn}; n = 3 to 13

LVD Detection Voltage of Interrupt & Reset Mode(T_A = -40 to +85°C, V_{PDR} ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVD13}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 0, falling reset voltage: 1.6 V		1.60	1.63	1.66	V
	V _{LVD12}	LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V _{LVD11}	LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V _{LVD4}	LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVD11}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 1, falling reset voltage: 1.8 V		1.80	1.84	1.87	V
	V _{LVD10}	LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V _{LVD9}	LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V _{LVD2}	LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V _{LVD8}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 0, falling reset voltage: 2.4 V		2.40	2.45	2.50	V
	V _{LVD7}	LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V _{LVD6}	LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V _{LVD5}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage: 2.7 V		2.70	2.75	2.81	V
	V _{LVD4}	LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V

<R> **Caution** Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: V_{DD} = 2.7 to 3.6 V@1 MHz to 32 MHz

V_{DD} = 2.4 to 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: V_{DD} = 1.8 to 3.6 V@1 MHz to 8 MHz

LV (low voltage main) mode: V_{DD} = 1.6 to 3.6 V@1 MHz to 4 MHz

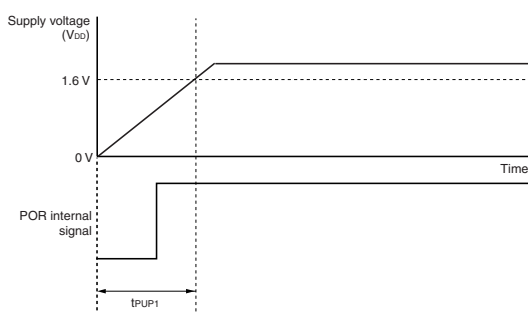
Supply Voltage Rise Time ($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.6 V (V_{DD} (MIN.)) ^{Note} (V_{DD} : 0 V $\rightarrow$ 1.6 V)	t_{PUP1}	When RESET input is not used			3.2	ms

Note Make sure to raise the power supply in a shorter time than this.

Supply Voltage Rise Time Timing

- When RESET pin input is not used

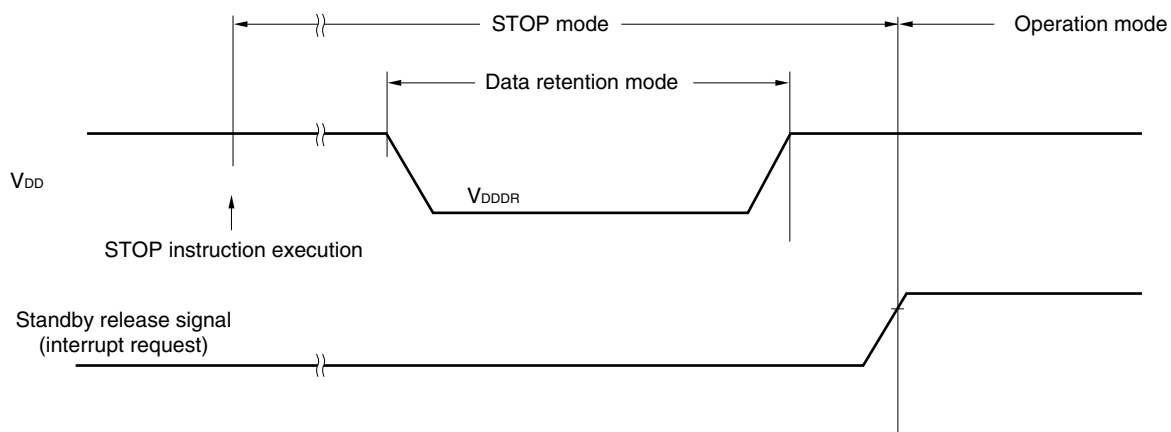


29.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47 ^{Note}		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



29.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)

<R>	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
	CPU/peripheral hardware clock frequency	f _{CLK}	1.8 V ≤ V _{DD} ≤ 3.6 V		1		32	MHz
	Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years	T _A = 85°C ^{Note 3}	1,000			Times
	Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years	T _A = 25°C ^{Note 3}		1,000,000		
			Retained for 5 years	T _A = 85°C ^{Note 3}	100,000			
Retained for 20 years			T _A = 85°C ^{Note 3}	10,000				

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This is a characteristic of the flash memory obtained as a result of our reliability test.

Remark When updating data multiple times, use the flash memory as one for updating data.

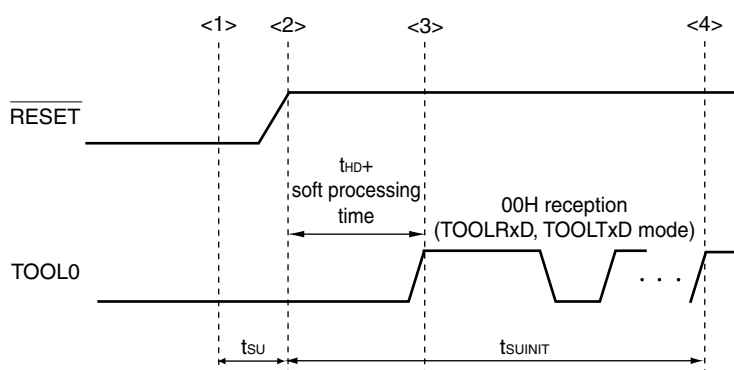
29.9 Timing Specs for Switching Flash Memory Programming Modes

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a pin reset ends until the initial communication settings are specified	t_{SUNIT}	POR and LVD reset must end before the pin reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a pin reset ends	t_{SU}	POR and LVD reset must end before the pin reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time)	t_{HD}	POR and LVD reset must end before the pin reset ends.	1			ms

<R>

<R>



<1> The low level is input to the TOOL0 pin.

<2> The pins reset ends (POR and LVD reset must end before the pin reset ends.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUNIT} : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU} : How long from when the TOOL0 pin is placed at the low level until a pin reset ends (MIN. 10 μs)

t_{HD} : How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

<R>

CHAPTER 30 ELECTRICAL SPECIFICATIONS
(G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$) (TARGET)Target products G : Industrial applications $T_A = -40$ to $+105^\circ\text{C}$

R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGFB, R5F10EGEGFB

R5F10ELCGFB, R5F10ELDGFB, R5F10ELEGB

- Cautions**
1. The RL78/G1A have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. With products not provided with an EV_{DD0} , EV_{DD1} , EV_{SS0} , or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD} , or replace EV_{SS0} and EV_{SS1} with V_{SS} .
 3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions Mounted According to Product.

Remark When RL78/G1A is used in the range of $T_A = -40$ to $+85^\circ\text{C}$, refer to **CHAPTER 29 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$) (TARGET)**.

30.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to $+6.5$	V
	EV_{DD0}		-0.5 to $+6.5$	V
	AV_{DD}		-0.5 to $+4.6$	V
	AV_{REFP}		-0.3 to $AV_{DD} + 0.3$	V
	V_{SS}		-0.5 to $+0.3$	V
	EV_{SS0}		-0.5 to $+0.3$	V
	AV_{SS}		-0.5 to $+0.3$	V
	AV_{REFM}		-0.3 to $AV_{DD} + 0.3$ and $AV_{REFM} \leq AV_{REFP}$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to $+2.8$ and -0.3 to $V_{DD} + 0.3$ ^{Note 1}	V
Input voltage	V_{I1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to $+6.5$	V
	V_{I3}	P121 to P124, P137, EXCLK, EXCLKS, RESET	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I4}	P20 to P27, P150 to P154	-0.3 to $AV_{DD} + 0.3$ ^{Note 2}	V
Output voltage	V_{O1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	-0.3 to $EV_{DD0} + 0.3$ ^{Note 2}	V
	V_{O2}	P20 to P27, P150 to P154	-0.3 to $AV_{DD} + 0.3$ ^{Note 2}	V
Analog input voltage	V_{AI1}	ANI16 to ANI30	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $AV_{REF(+) } + 0.3$ ^{Notes 2, 4}	V
	V_{AI2}	ANI0 to ANI12	-0.3 to $AV_{DD} + 0.3$ and -0.3 to $AV_{REF(+) } + 0.3$ ^{Notes 2, 4}	V

- Notes**
1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
 2. Must be 6.5 V or lower.
 3. Must be 4.6 V or lower.
 4. Do not exceed $AV_{REF(+)} + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks**
1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
 2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$) (2/2)

Absolute Maximum Ratings (TA = 25 °C) (2/2)					
Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	−40	mA
		Total of all pins −170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	−70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,	−100	mA
	IOH2	Per pin	P20 to P27, P150 to P154	−0.1	mA
		Total of all pins		−1.3	mA
	Output current, low	IOL1	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	40
Total of all pins 170 mA			P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77	100	mA
IOL2		Per pin	P20 to P27, P150 to P154	0.4	mA
		Total of all pins		6.4	mA
Operating ambient temperature		TA	In normal operation mode		−40 to +105 ^{Note}
	In flash memory programming mode				
Storage temperature	Tstg			−65 to +150	°C

Note Operating time at $T_A = +85^{\circ}\text{C}$ to $+105^{\circ}\text{C}$: 10,000 times

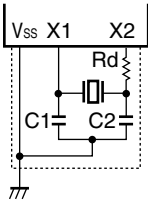
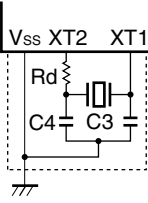
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

30.2 Oscillator Characteristics

30.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)

Parameter	Resonator	Recommended Circuit	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_{X1}) ^{Note}	Ceramic resonator/ crystal resonator		$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	1.0		20.0	MHz
			$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		8.0	MHz
XT1 clock oscillation frequency (f_{XT1}) ^{Note}	Crystal resonator			32	32.768	35	kHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.
 3. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

30.2.2 On-chip oscillator characteristics**($T_A = -40$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = V_{SS0} = 0\text{ V}$)**

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Note 1}	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy ^{Note 2}		+85 to $+105^{\circ}\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-2		+2	%
		-20 to $+85^{\circ}\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-1		+1	%
		-40 to -20°C	$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. Frequency can be selected in a high-speed on-chip oscillator. Selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

30.3 DC Characteristics

30.3.1 Pin characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	$2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$		-3.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70% ^{Note 3})	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$		-10.0	mA
			$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		-5.0	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77, (When duty = 70% ^{Note 3})	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$		-19.0	mA
			$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		-10.0	mA
	I _{OH2}	Total of all pins (When duty = 70% ^{Note 3})	$2.4\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$		-29.0	mA
		Per pin for P20 to P27, P150 to P154	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$		-0.1 ^{Note 2}	mA
		Total of all pins (When duty = 70% ^{Note 3})	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$		-1.3	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0} , V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 50\%$ and $I_{OH} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(50 \times 0.01) = -14.0\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ AVDD ≤ VDD ≤ 3.6 V, 2.4 V ≤ EVDD0 ≤ VDD ≤ 3.6 V, VSS = EVSS0 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	IOL1	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141			8.5 ^{Note 2}	mA
		Per pin for P60 to P63			15.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70% ^{Note 3})	2.7 V ≤ EVDD0 ≤ 3.6 V		15.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		9.0	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77 (When duty = 70% ^{Note 3})	2.7 V ≤ EVDD0 ≤ 3.6 V		35.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		20.0	mA
		Total of all pins (When duty = 70% ^{Note 3})			50.0	mA
	IOL2	Per pin for P20 to P27, P150 to P154			0.4 ^{Note 2}	mA
		Total of all pins (When duty = 70% ^{Note 3})	2.4 V ≤ AVDD ≤ 3.6 V		5.2	mA

- Notes**
1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0 and VSS pin.
 2. However, do not exceed the total current value.
 3. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OL} \times 0.7) / (n \times 0.01)$

<Example> Where $n = 50\%$ and $I_{OL} = 10.0$ mA

$$\text{Total output current of pins} = (10.0 \times 0.7) / (50 \times 0.01) = 14.0 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ AVDD ≤ VDD ≤ 3.6 V, 2.4 V ≤ EVDD0 ≤ VDD ≤ 3.6 V, VSS = EVSS0 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	0.8EV _{DD0}		EV _{DD0}	V
	V _{IH2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer 3.3 V ≤ EV _{DD0} < 3.6 V	2.0	EV _{DD0}	V
			TTL input buffer 2.4 V ≤ EV _{DD0} < 3.3 V	1.5	EV _{DD0}	V
	V _{IH3}	P20 to P27, P150 to P154	0.7AV _{DD}		AV _{DD}	V
	V _{IH4}	P60 to P63	0.7EV _{DD0}		6.0	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	0		0.2EV _{DD0}	V
	V _{IL2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer 3.3 V ≤ EV _{DD0} < 3.6 V	0	0.5	V
			TTL input buffer 2.4 V ≤ EV _{DD0} < 3.3 V	0	0.32	V
	V _{IL3}	P20 to P27, P150 to P154	0		0.3AV _{DD}	V
	V _{IL4}	P60 to P63	0		0.3EV _{DD0}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		0.2V _{DD}	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 is EV_{DD0}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ AVDD ≤ VDD ≤ 3.6 V, 2.4 V ≤ EVDD0 ≤ VDD ≤ 3.6 V, VSS = EVSS0 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.7 V ≤ EVDD0 ≤ 3.6 V, IOH1 = -2.0 mA	EVDD0 - 0.6		V
			2.4 V ≤ EVDD0 ≤ 3.6 V, IOH1 = -1.5 mA	EVDD0 - 0.5		V
	VOH2	P20 to P27, P150 to P154	2.4 V ≤ AVDD ≤ 3.6 V, IOH2 = -100 μA	AVDD - 0.5		V
Output voltage, low	VOL1	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.7 V ≤ EVDD0 ≤ 3.6 V, IOL1 = 3.0 mA		0.6	V
			2.7 V ≤ EVDD0 ≤ 3.6 V, IOL1 = 1.5 mA		0.4	V
			2.4 V ≤ EVDD0 ≤ 3.6 V, IOL1 = 0.6 mA		0.4	V
	VOL2	P20 to P27, P150 to P154	2.4 V ≤ AVDD ≤ 3.6 V, IOL2 = 400 μA		0.4	V
	VOL3	P60 to P63	2.7 V ≤ EVDD0 ≤ 3.6 V, IOL3 = 3.0 mA		0.4	V
			2.4 V ≤ EVDD0 ≤ 3.6 V, IOL3 = 2.0 mA		0.4	V

Caution P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ AVDD ≤ VDD ≤ 3.6 V, 2.4 V ≤ EVDD0 ≤ VDD ≤ 3.6 V, VSS = EVSS0 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I _{LIH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P140, P141	V _I = EV _{DD0}		1	μA		
	I _{LIH2}	P137, $\overline{\text{RESET}}$	V _I = V _{DD}		1	μA		
	I _{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input	1	μA		
				In resonator connection	10	μA		
	I _{LIH4}	P20 to P27, P150 to P154	V _I = AV _{DD}		1	μA		
Input leakage current, low	I _{LIL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P67, P70 to P77, P120, P140, P141	V _I = EV _{SS0}		−1	μA		
	I _{LIL2}	P137, $\overline{\text{RESET}}$	V _I = V _{SS}		−1	μA		
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input	−1	μA		
				In resonator connection	−10	μA		
	I _{LIL4}	P20 to P27, P150 to P154	V _I = AV _{SS}		−1	μA		
On-chip pll-up resistance	R _U	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	V _I = EV _{SS0} , In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

30.3.2 Supply current characteristics

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = V_{SS0} = 0\text{ V}$)

(1/3)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} ^{Note 1}	Operating mode	HS (high-speed main) mode ^{Note 5}	$f_{IH} = 32\text{ MHz}$ ^{Note 3}	Basic operation	$V_{DD} = 3.0\text{ V}$		2.1		mA
					Normal operation	$V_{DD} = 3.0\text{ V}$		4.6	7.5	mA
				$f_{IH} = 24\text{ MHz}$ ^{Note 3}	Normal operation	$V_{DD} = 3.0\text{ V}$		3.7	5.8	mA
					Normal operation	$V_{DD} = 3.0\text{ V}$		2.7	4.2	mA
			HS (high-speed main) mode ^{Note 5}	$f_{MX} = 20\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				$f_{MX} = 10\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
		Subsystem clock mode		$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.2	4.9	μA
						Resonator connection		4.3	5.0	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		4.3	5.5	μA
						Resonator connection		4.4	5.6	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		4.5	6.3	μA
						Resonator connection		4.6	6.4	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		4.8	7.7	μA
						Resonator connection		4.9	7.8	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		6.9	19.7	μA
						Resonator connection		7.0	19.8	μA

Notes 1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

- When high-speed on-chip oscillator and subsystem clock are stopped.
- When high-speed system clock and subsystem clock are stopped.
- When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time counter, interval timer and watchdog timer is stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
- Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $V_{DD} = 2.7\text{ V to }3.6\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $V_{DD} = 2.4\text{ V to }3.6\text{ V}@1\text{ MHz to }16\text{ MHz}$

Remarks 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

- f_{IH} : High-speed on-chip oscillator clock frequency
- f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
- Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 ≤ VDD ≤ 3.6 V, VSS = EVSS0 = 0 V)

(2/3)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 3.0 V		0.54	2.90	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 3.0 V		0.44	2.30	mA	
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 3.0 V		0.40	1.70	mA	
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.28	1.90	mA	
					Resonator connection		0.45	2.00	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.19	1.02	mA	
					Resonator connection		0.26	1.10	mA	
			Subsystem clock mode	f _{SUB} = 32.768 kHz ^{Note 5} T _A = −40°C	Square wave input		0.25	0.57	μA	
					Resonator connection		0.44	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input		0.30	0.57	μA	
					Resonator connection		0.49	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input		0.38	1.17	μA	
		Resonator connection				0.57	1.36	μA		
		f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C		Square wave input		0.52	1.97	μA		
				Resonator connection		0.71	2.16	μA		
		f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C		Square wave input		0.97	3.37	μA		
				Resonator connection		1.16	3.56	μA		
		f _{SUB} = 32.768 kHz ^{Note 5} T _A = +105°C	Square wave input		3.01	15.37	μA			
			Resonator connection		3.20	15.56	μA			
	I _{DD3} Note 6	STOP mode Note 8	T _A = −40°C					0.16	0.50	μA
			T _A = +25°C					0.23	0.50	μA
			T _A = +50°C					0.34	1.10	μA
			T _A = +70°C					0.46	1.90	μA
			T _A = +85°C					0.75	3.30	μA
			T _A = +105°C					2.94	15.30	μA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When operating real-time clock (RTC), RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator and high-speed system clock are stopped. When interval timer and watchdog timer are stopped. The values below the MAX. column include the leakage current.

6. When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V @ 1 MHz to 32 MHz

2.4 V ≤ V_{DD} ≤ 3.6 V @ 1 MHz to 16 MHz

8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.

- Remarks 1.** f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH} : High-speed on-chip oscillator clock frequency
3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 ≤ VDD ≤ 3.6 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} ^{Notes 1, 2}			0.02 ^{Note 3}		μA
Interval timer operating current	I_{IT} ^{Notes 2, 4}			0.02 ^{Note 3}		μA
Watchdog timer operating current	I_{WDT} ^{Notes 2, 5}	$f_{\text{IL}} = 15 \text{ kHz}$, f_{MAIN} is stopped.		0.22		μA
A/D converter operating current	I_{ADC} ^{Notes 6, 7}	$\text{AV}_{\text{DD}} = 3.0 \text{ V}$, When conversion at maximum speed		420	720	μA
AVREF (+) current	I_{AVREF} ^{Note 8}	$\text{AV}_{\text{DD}} = 3.0 \text{ V}$, $\text{ADREFP1} = 0$, $\text{ADREFP0} = 0$ ^{Note 7}		14.0	25.0	μA
		$\text{AV}_{\text{REFP}} = 3.0 \text{ V}$, $\text{ADREFP1} = 0$, $\text{ADREFP0} = 1$ ^{Note 10}		14.0	25.0	μA
		$\text{ADREFP1} = 1$, $\text{ADREFP0} = 0$ ^{Note 11}		14.0	25.0	μA
A/D converter reference voltage current	I_{ADREF} ^{Note 9}	$\text{V}_{\text{DD}} = 3.0 \text{ V}$ ^{Note 11}		75.0		μA
Temperature sensor operating current	I_{TMPS}	$\text{V}_{\text{DD}} = 3.0 \text{ V}$ ^{Note 11}		75.0		μA
LVD operating current	I_{LVI} ^{Note 12}			0.08		μA
BGO operating current	I_{BGO} ^{Note 13}			2.50	12.2	mA
SNOOZE operating current	I_{SNOZ}	A/D converter operation ($\text{AV}_{\text{DD}} = 3.0 \text{ V}$)	The mode is performed ^{Notes 11, 14}	T.B.D.		mA
			During A/D conversion ^{Note 11}	T.B.D.		mA
			During A/D conversion ^{Note 7}	T.B.D.		μA
		CSI/UART operation ^{Note 11}		T.B.D.		mA

- Notes**
1. Current flowing only to the real-time clock (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78/G1A microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. However, I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
 2. When high speed on-chip oscillator and high-speed system clock are stopped.
 3. Add 200 μA when using f_{IL} .
 4. Current flowing only to the interval timer (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78/G1A microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{IT} , when the interval timer operates in operation mode or HALT mode.
 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78/G1A is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{WDT} when $f_{\text{CLK}} = f_{\text{SUB}}$ when the watchdog timer operates.
 6. Current flowing only to the A/D converter. The current value of the RL78/G1A is the sum of I_{DD1} or I_{DD2} and I_{ADC} , I_{AVREF} , I_{ADREF} when the A/D converter operates in an operation mode or the HALT mode.
 7. Current flowing to the AV_{DD} .
 8. Current flowing from the reference voltage source of A/D converter.
 9. Operation current flowing to the internal reference voltage.
 10. Current flowing to the AV_{REFP} .
 11. Current flowing to the V_{DD} .
 12. Current flowing only to the LVD circuit. The current value of the RL78/G1A is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.
 13. Current flowing only to the BGO. The current value of the RL78/G1A is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in an operation mode.
 14. Refer to **18.3.3 SNOOZE mode** for shift time to the SNOOZE mode.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

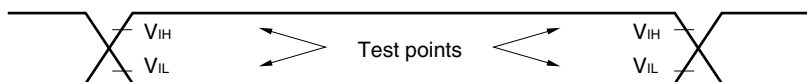
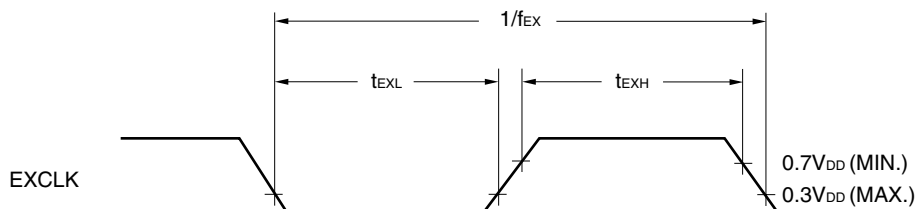
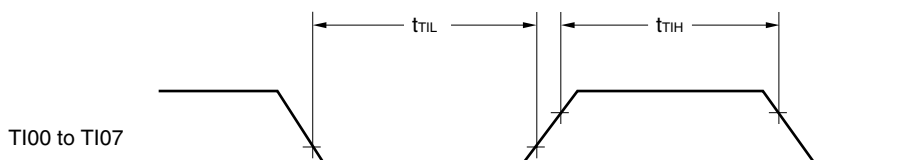
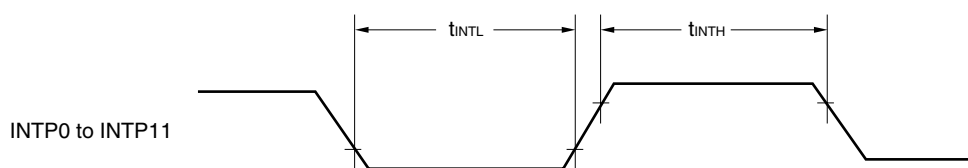
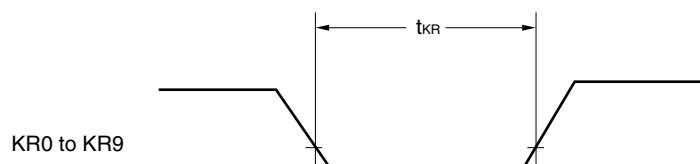
30.4 AC Characteristics

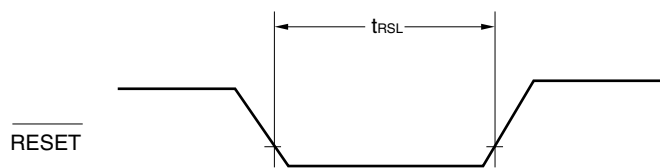
(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$, $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{main}) mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f _{sub}) Operation		2.4 V ≤ V _{DD} ≤ 3.6 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
External main system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 3.6 V		1.0		20.0	MHz	
		2.4 V ≤ V _{DD} < 2.7 V		1.0		8.0	MHz	
	f _{EXS}			32		35	kHz	
External main system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 3.6 V		24			ns	
		2.4 V ≤ V _{DD} < 2.7 V		60			ns	
	t _{EXHS} , t _{EXLS}			13.7			μs	
TI00, TI01, TI03 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} +10			ns ^{Note}	
TO00, TO01, TO03 to TO07 output frequency	f _{TO}	HS (high-speed main) mode	2.7 V ≤ EV _{DD0} ≤ 3.6 V			8	MHz	
			2.4 V ≤ EV _{DD0} < 2.7 V			4	MHz	
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	2.7 V ≤ EV _{DD0} ≤ 3.6 V			8	MHz	
			2.4 V ≤ EV _{DD0} < 2.7 V			4	MHz	
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	2.4 V ≤ V _{DD} ≤ 3.6 V	1			μs	
		INTP1 to INTP11	2.4 V ≤ EV _{DD0} ≤ 3.6 V	1			μs	
Key interrupt input high-level width, low-level width	t _{KR}	KR0 to KR9	2.4 V ≤ EV _{DD0} ≤ 3.6 V, 2.4 V ≤ AV _{DD} ≤ 3.6 V	250			ns	
RESET low-level width	t _{RSL}			10			μs	

Note The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$ $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MIN. 125 ns**Remark** f_{MCK}: Timer array unit operation clock frequency

(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

AC Timing Test Points**External System Clock Timing****TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing**

RESET Input Timing

30.5 Peripheral Functions Characteristics

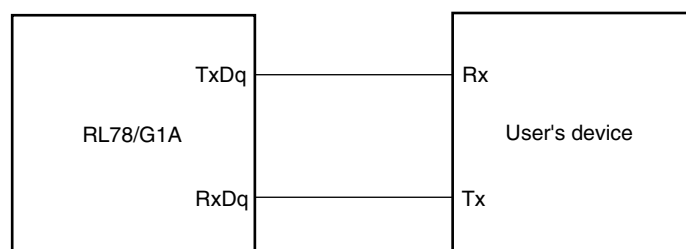
30.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

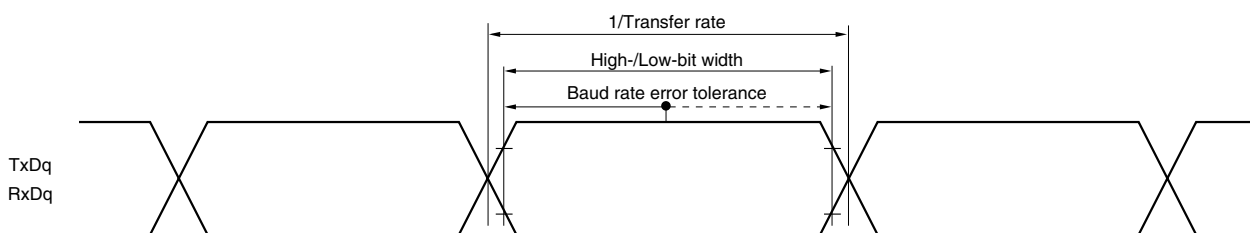
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq E_{VDD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = E_{VSS0} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate ^{Note 1}					$f_{MCK}/12$ ^{Note 2}	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$			2.6	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Notes 1. Transfer rate in the SNOOZE mode is max. 9600 bps, min. 4800 bps.

2. The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$.

$2.4\text{ V} \leq E_{VDD0} < 2.7\text{ V}$: MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

2. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSMn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ $t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	250 ^{Note 1}			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$ $t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	500 ^{Note 1}			ns
$\overline{\text{SCKp}}$ high-/low-level width	$t_{\text{KH1}},$	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$t_{\text{KCY1}}/2 - 36$			ns
	t_{KL1}	$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$t_{\text{KCY1}}/2 - 76$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) ^{Note 2}	t_{SIK1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	66			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	113			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) ^{Note 3}	t_{SI1}		38			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output ^{Note 4}	t_{KS01}	$C = 30\text{ pF}$ ^{Note 5}			50	ns

Notes 1. The value must also be $4/f_{\text{CLK}}$ or more.**2.** When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to $\overline{\text{SCKp}}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.**3.** When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from $\overline{\text{SCKp}}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.**4.** When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from $\overline{\text{SCKp}}\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.**5.** C is the load capacitance of the $\overline{\text{SCKp}}$ and SOp output lines.**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).**Remark** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM numbers (g = 0, 1)

(3) During communication at same potential (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time ^{Note 5}	t_{CY2}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$16\text{ MHz} < f_{\text{MCK}}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 16\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$	$16\text{ MHz} < f_{\text{MCK}}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 16\text{ MHz}$	$12/f_{\text{MCK}}$		ns
$\overline{\text{SCKp}}$ high-/low-level width	$t_{\text{KH2}},$ t_{KL2}	$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$t_{\text{CY2}}/2$			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) ^{Note 1}	t_{SIK2}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$1/f_{\text{MCK}} + 40$			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$	$1/f_{\text{MCK}} + 60$			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) ^{Note 2}	t_{SI2}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$	$1/f_{\text{MCK}} + 62$			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$	$1/f_{\text{MCK}} + 62$			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output ^{Note 3}	t_{SO2}	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$		$2/f_{\text{MCK}} + 66$	ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$		$2/f_{\text{MCK}} + 113$	ns

Notes 1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to $\overline{\text{SCKp}}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from $\overline{\text{SCKp}}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from $\overline{\text{SCKp}}\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

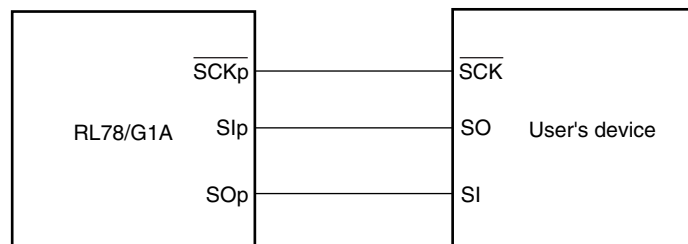
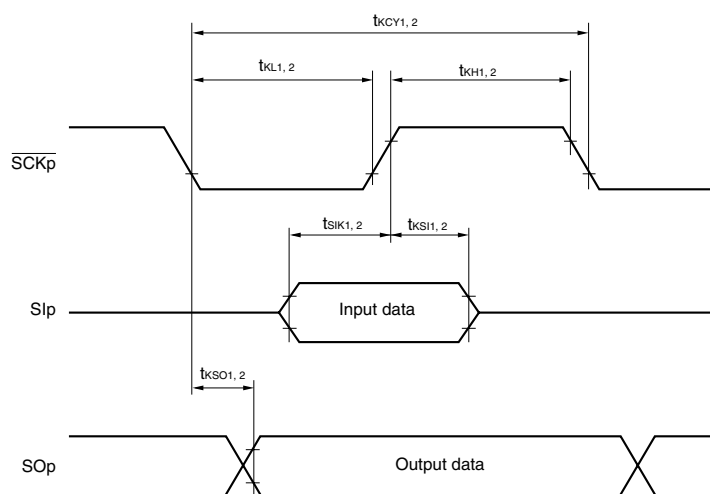
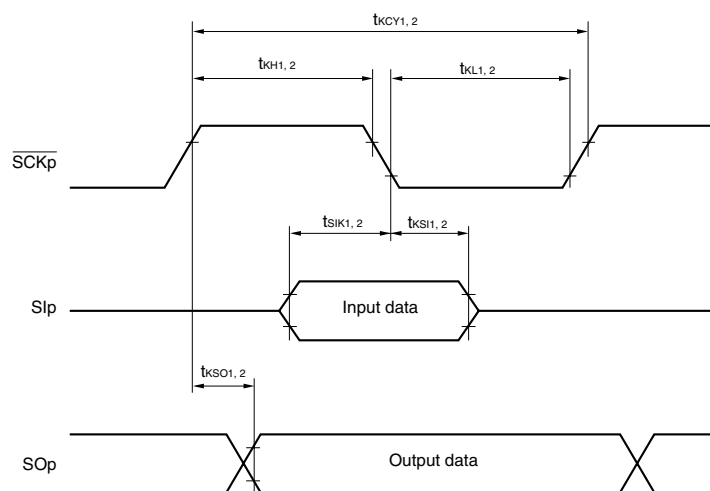
4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and $\overline{\text{SCKp}}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1)

2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

CSI mode connection diagram (during communication at same potential)**CSI mode serial transfer timing (during communication at same potential)**
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**CSI mode serial transfer timing (during communication at same potential)**
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

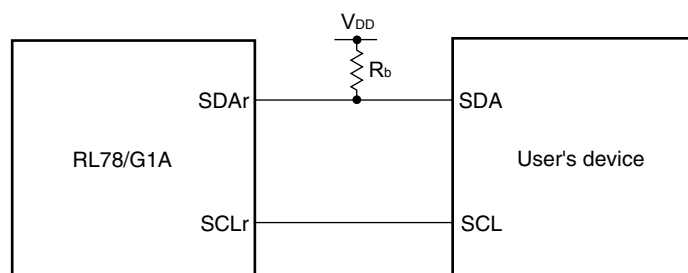
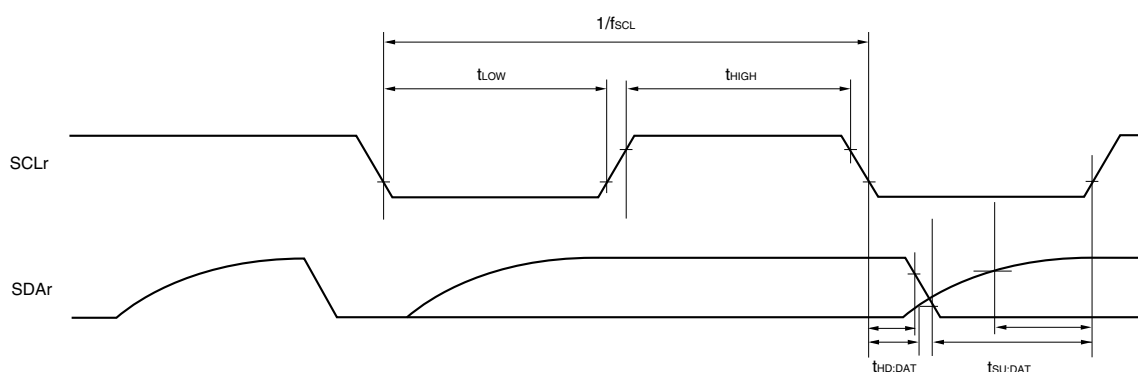
- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21)
 2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(4) During communication at same potential (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note 1}	kHz
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 220$ ^{Note 2}		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ ^{Note 2}		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	1420	ns

<R> **Notes 1.** The value must also be $f_{\text{CLK}}/4$ or lower.**2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

(Caution and Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number, mn = 00 to 03, 10, 11)

(5) Communication at different potential (2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq E_{VDD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = E_{VSS0} = 0\text{ V}$)**

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		reception	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$				$f_{\text{MCK}}/12$ Note 1	bps
			Theoretical value of the maximum transfer rate $f_{\text{CLK}} = 32\text{ MHz}$, $f_{\text{MCK}} = f_{\text{CLK}}$			2.6	Mbps	
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$				$f_{\text{MCK}}/12$ Notes 1 to 3	bps
			Theoretical value of the maximum transfer rate $f_{\text{CLK}} = 8\text{ MHz}$, $f_{\text{MCK}} = f_{\text{CLK}}$			0.6	Mbps	

- Notes**
1. Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps
 2. Use it with $E_{VDD0} \geq V_b$.
 3. The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$.
 $2.4\text{ V} \leq E_{VDD0} < 2.7\text{ V}$: MAX. 2.6 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ E_{VDD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(5) Communication at different potential (2.5 V) (UART mode) (dedicated baud rate generator output) (2/2)**(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		transmission	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V			Notes 1, 2	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V			1.2 ^{Note 5}	Mbps
			2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			Notes 1, 4, 5	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V			0.43 ^{Note 6}	Mbps

Notes 1. Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps

2. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} ≤ 3.6 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{\frac{1}{(\text{Transfer rate})} \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

3. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 2 above to calculate the maximum transfer rate under conditions of the customer.

4. Use it with EV_{DD0} ≥ V_b.

5. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{\frac{1}{(\text{Transfer rate})} \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

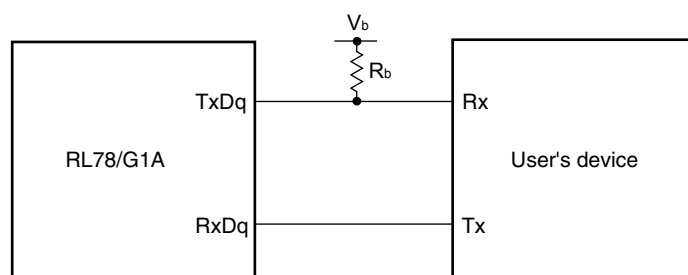
* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 7 above to calculate the maximum transfer rate under conditions of the customer.

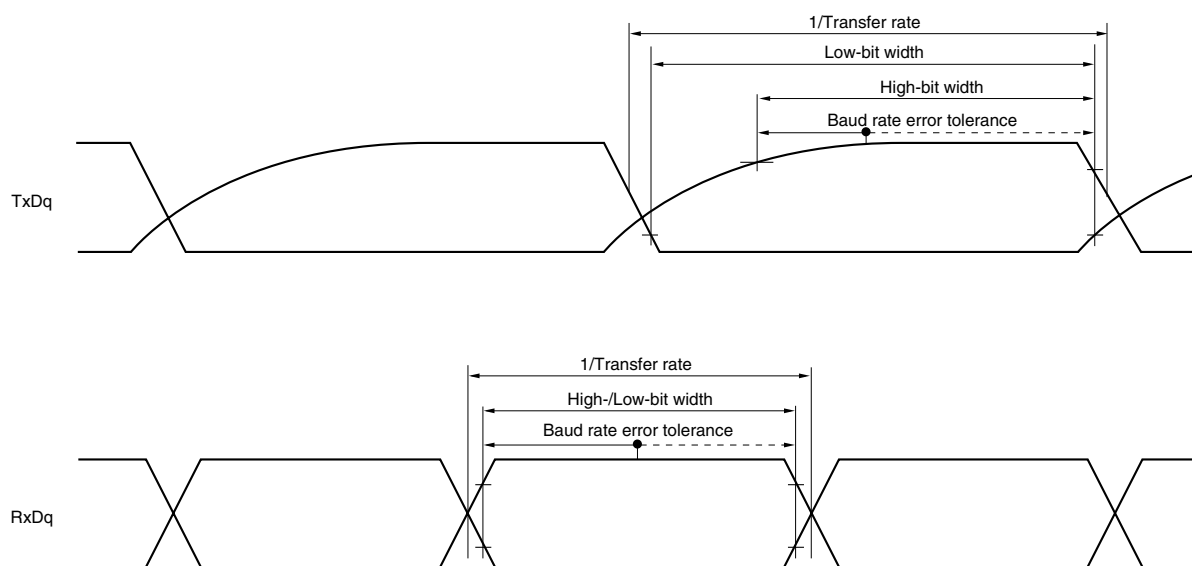
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[\text{F}]$: Communication line (TxDq) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))
 4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $V_b[\text{V}]$: Communication line voltage
 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

(6) Communication at different potential (2.5 V) (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output) (1/2)
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	1000 ^{Note}		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	2300 ^{Note}		ns
$\overline{\text{SCKp}}$ high-level width	t_{KH1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 340$			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 916$			ns
$\overline{\text{SCKp}}$ low-level width	t_{KL1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 36$			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 100$			ns

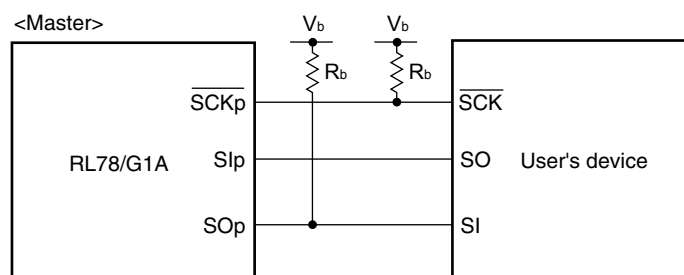
Note The value must also be $4/f_{\text{CLK}}$ or more.

- Cautions**
1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).
 2. Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.

- Remarks**
1. $\text{R}_b[\Omega]$: Communication line ($\overline{\text{SCKp}}$, SOp) pull-up resistance, $\text{C}_b[\text{F}]$: Communication line ($\overline{\text{SCKp}}$, SOp) load capacitance, $\text{V}_b[\text{V}]$: Communication line voltage
 2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)
 3. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(6) Communication at different potential (2.5 V) (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output) (2/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) ^{Note 1}	t_{SIK1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	354			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	958			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) ^{Note 1}	t_{KSI1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	38			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	38			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SO output ^{Note 1}	t_{KSO1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$			390	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$			966	ns
Slp setup time (to $\overline{\text{SCKp}}\downarrow$) ^{Note 2}	t_{SIK1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	88			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	220			ns
Slp hold time (from $\overline{\text{SCKp}}\downarrow$) ^{Note 2}	t_{KSI1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	38			ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	38			ns
Delay time from $\overline{\text{SCKp}}\uparrow$ to SO output ^{Note 2}	t_{KSO1}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$			50	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$			50	ns

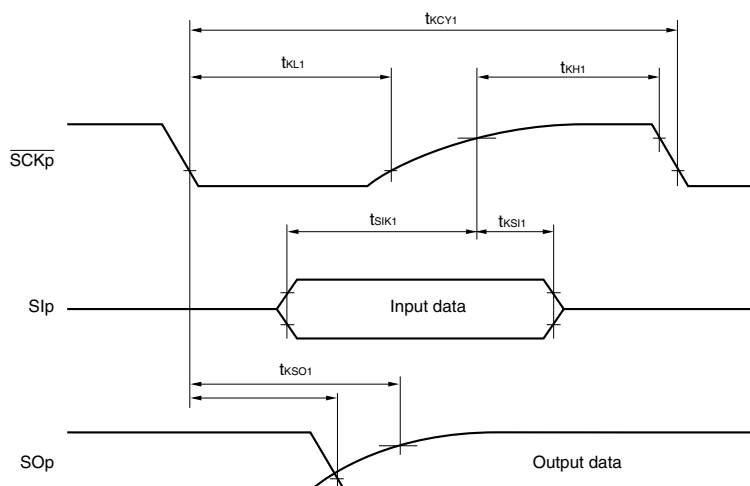
Notes 1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.**CSI mode connection diagram (during communication at different potential)****Cautions** 1. Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).2. Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.**Remarks** 1. $\text{R}_b[\Omega]$: Communication line ($\overline{\text{SCKp}}$, SOp) pull-up resistance, $\text{C}_b[\text{F}]$: Communication line ($\overline{\text{SCKp}}$, SOp) load capacitance, $\text{V}_b[\text{V}]$: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10),

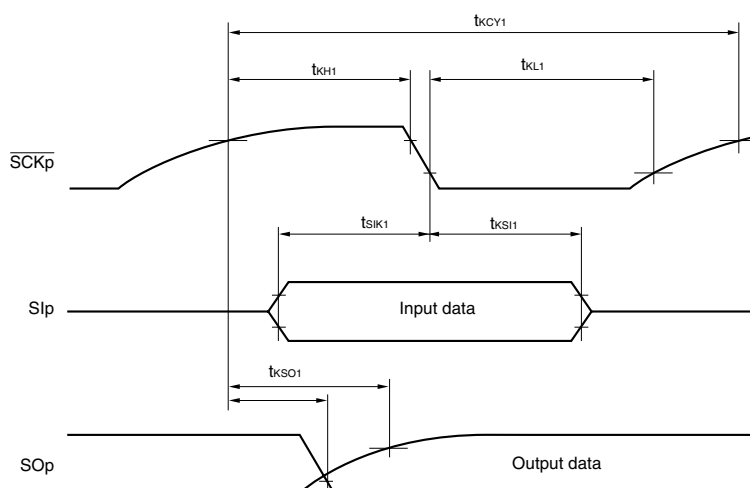
g: PIM and POM number (g = 0, 1)

3. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

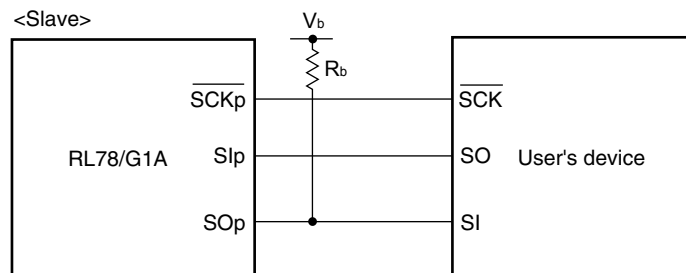
- Remarks**
1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (m = 00, 02, 10), g: PIM and POM number (g = 0, 1)
 2. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(7) Communication at different potential (2.5 V) (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time ^{Note 1}	t _{KCY2}	2.7 V ≤ EV _{DD0} ≤ 3.6 V,	24 MHz < f _{MCK}	40/f _{MCK}			ns
		2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK} ≤ 24 MHz	32/f _{MCK}			ns
			16 MHz < f _{MCK} ≤ 20 MHz	28/f _{MCK}			ns
			8 MHz < f _{MCK} ≤ 16 MHz	24/f _{MCK}			ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}			ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}			ns
		2.4 V ≤ EV _{DD0} < 3.3 V,	24 MHz < f _{MCK}	96/f _{MCK}			ns
		1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	20 MHz < f _{MCK} ≤ 24 MHz	72/f _{MCK}			ns
			16 MHz < f _{MCK} ≤ 20 MHz	64/f _{MCK}			ns
			8 MHz < f _{MCK} ≤ 16 MHz	52/f _{MCK}			ns
			4 MHz < f _{MCK} ≤ 8 MHz	32/f _{MCK}			ns
			f _{MCK} ≤ 4 MHz	20/f _{MCK}			ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V	t _{KCY2} /2 – 36			ns	
		2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	t _{KCY2} /2 – 100			ns	
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V	1/f _{MCK} + 40			ns	
		2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1/f _{MCK} + 60			ns	
Slp hold time (from SCKp↑) ^{Note 4}	t _{KSI2}		1/f _{MCK} + 62			ns	
Delay time from SCKp↓ to SOp output ^{Note 5}	t _{KSO2}	2.7 V ≤ EV _{DD0} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 428	ns	
		2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 1146	ns	

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps2. Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to $\overline{\text{SCKp}}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.4. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from $\overline{\text{SCKp}}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.5. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from $\overline{\text{SCKp}}\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

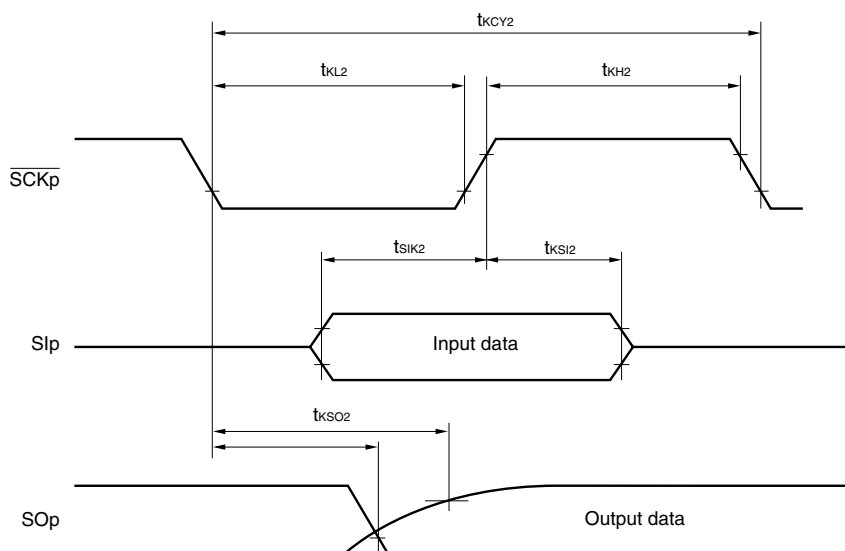
(Caution and Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

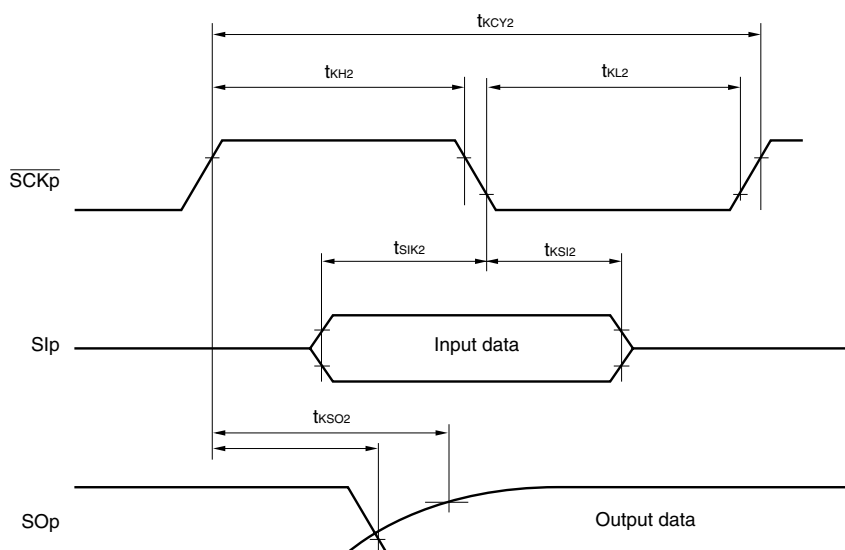
Caution Select the TTL input buffer for the SIp pin and $\overline{\text{SCKp}}$ pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number ($p = 00, 10, 20$), m: Unit number ($m = 0, 1$), n: Channel number ($n = 00, 02, 10$), g: PIM and POM number ($g = 0, 1$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00, 02, 10$))
 4. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the Slp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)
 2. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(8) Communication at different potential (2.5 V) (simplified I²C mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note 1}	kHz
		$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		100 ^{Note 1}	kHz
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	4600		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	500		ns
		$2.7\text{ V} \leq EV_{DD0} \leq 3.6\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	2400		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	1830		ns

(Notes, Caution and Remarks are listed on the next page.)

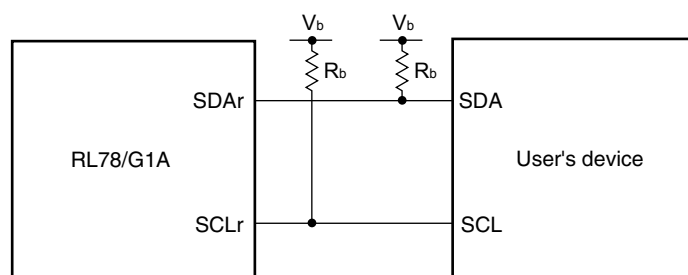
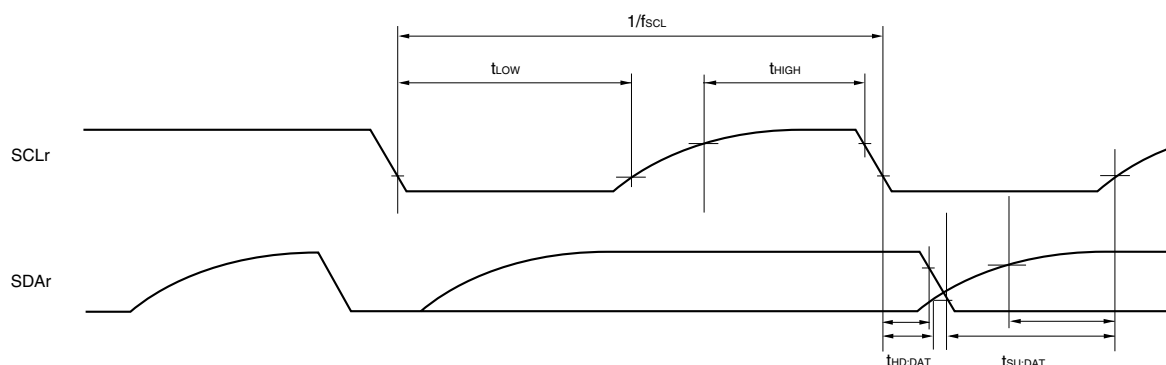
(8) Communication at different potential (2.5 V) (simplified I²C mode) (2/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 340$ Note 3		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 760$ Note 3		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ Note 2, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$1/f_{\text{MCK}} + 570$ Note 3		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	0	1420	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ Note 2, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	0	1215	ns

<R> **Notes 1.** The value must also be $f_{\text{CLK}}/4$ or lower.**2.** Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.**3.** Set the f_{MCK} value to keep the hold time of $\text{SCLr} = \text{"L"}$ and $\text{SCLr} = \text{"H"}$.

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(Remarks is listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (When 25- to 48-pin products)/ EV_{DD} tolerance (When 64-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))
 4. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

30.5.2 Serial interface IICA

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
		Fast mode: $f_{\text{CLK}} \geq 3.5\text{ MHz}$ Normal mode: $f_{\text{CLK}} \geq 1\text{ MHz}$	$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 3.6\text{ V}$		
Setup time of restart condition	$t_{\text{SU:STA}}$		4.7		0.6		μs
Hold time ^{Note 1}	$t_{\text{HD:STA}}$		4.0		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{\text{SU:DAT}}$		250		100		ns
Data hold time (transmission) ^{Note 2}	$t_{\text{HD:DAT}}$		0	3.45	0	0.9	μs
Setup time of stop condition	$t_{\text{SU:STO}}$		4.0		0.6		μs
Bus-free time	t_{BUF}		4.7		1.3		μs

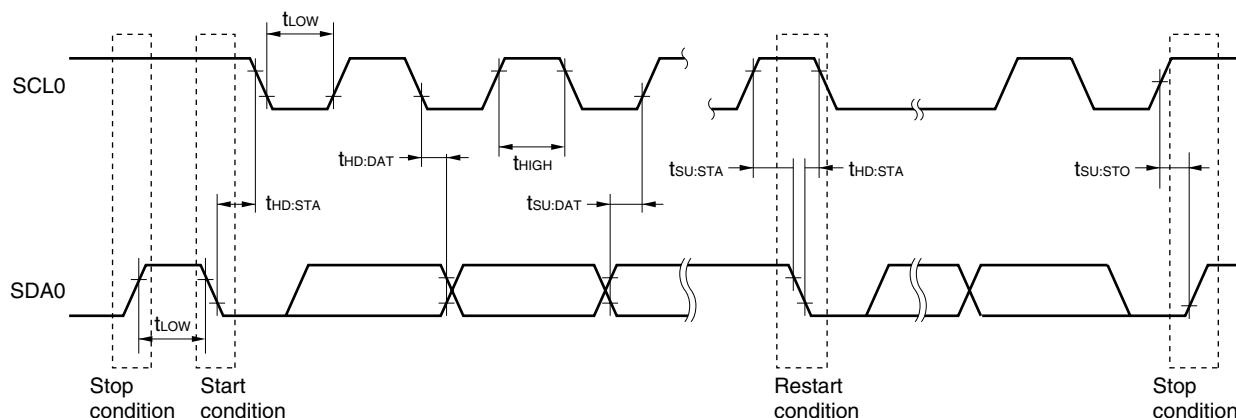
- Notes**
- The first clock pulse is generated after this period when the start/restart condition is detected.
 - The maximum value (MAX.) of $t_{\text{HD:DAT}}$ is during normal transfer and a wait state is inserted in the $\overline{\text{ACK}}$ (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 k Ω

Fast mode: C_b = 320 pF, R_b = 1.1 k Ω

IICA serial transfer timing



30.5.3 On-chip debug (UART)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			115.2 k		1 M	bps

30.6 Analog Characteristics

30.6.1 A/D converter characteristics

Division of A / D Converter Characteristics

Reference voltage Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = AV_{DD} Reference voltage (-) = AV_{SS}	Reference voltage (+) = Internal reference voltage Reference voltage (-) = AV_{SS}
High-accuracy channel ; ANI0 to ANI12 (input buffer power supply : AV_{DD})	See 30.6.1 (1)	See 30.6.1 (2)	See 30.6.1 (5)
Normal channel ; ANI16 to ANI30 (input buffer power supply : V_{DD} or EV_{DD0})	See 30.6.1 (3)	See 30.6.1 (4)	

(1) When $AV_{REF(+)} = AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), $AV_{REF(-)} = AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin : ANI0 to ANI12

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.		T.B.D.	bit
Overall error ^{Note 3}	$AINL$	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.			μs
		ADTYP = 1, 8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.			
Zero-scale error ^{Note 3}	EZS	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Full-scale error ^{Note 3}	EFS	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Integral linearity error ^{Note 3}	ILE	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Differential linearity error ^{Note 3}	DLE	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Analog input voltage	V_{AIN}			T.B.D.		T.B.D.	V
	V_{BGR}	Select internal reference voltage output $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, HS (high-speed main) mode		T.B.D.	T.B.D.	T.B.D.	V

- Notes**
1. Cannot be used for lower 2 bit of ADCR register
 2. Cannot be used for lower 4 bit of ADCR register
 3. Excludes quantization error ($\pm 1/2$ LSB).

(2) When $AV_{REF(+)} = AV_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF(-)} = AV_{SS}$ (ADREFM = 0), target ANI pin : ANI0 to ANI12

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{DD} , Reference voltage (-) = $AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.		T.B.D.	bit
Overall error ^{Note 3}	AINL	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.			μs
		ADTYP = 1, 8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.			
Zero-scale error ^{Note 3}	EZS	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Full-scale error ^{Note 3}	EFS	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Integral linearity error ^{Note 3}	ILE	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Differential linearity error ^{Note 3}	DLE	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Analog input voltage	V_{AIN}			T.B.D.		T.B.D.	V
	V_{BGR}	Select internal reference voltage output $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, HS (high-speed main) mode		T.B.D.	T.B.D.	T.B.D.	V

- Notes**
1. Cannot be used for lower 2 bit of ADCR register
 2. Cannot be used for lower 4 bit of ADCR register
 3. Excludes quantization error ($\pm 1/2$ LSB).

(3) When $AV_{REF(+)} = AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), $AV_{REF(-)} = AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin : ANI16 to ANI30

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.		T.B.D.	bit
Overall error ^{Note 3}	$AINL$	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		T.B.D.	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.		μs
		ADTYP = 1, 8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.		
Zero-scale error ^{Note 3}	EZS	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		T.B.D.	
Full-scale error ^{Note 3}	EFS	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		T.B.D.	
Integral linearity error ^{Note 3}	ILE	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		T.B.D.	
Differential linearity error ^{Note 3}	DLE	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		T.B.D.	
Analog input voltage	V_{AIN}		T.B.D.		T.B.D.	V
	V_{BGR}	Select internal reference voltage output $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, HS (high-speed main) mode	T.B.D.	T.B.D.	T.B.D.	V

- Notes**
1. Cannot be used for lower 2 bit of ADCR register
 2. Cannot be used for lower 4 bit of ADCR register
 3. Excludes quantization error ($\pm 1/2$ LSB).

(4) When $AV_{REF(+)} = AV_{DD}$ ($ADREFP1 = 0$, $ADREFP0 = 0$), $AV_{REF(-)} = AV_{SS}$ ($ADREFM = 0$), target ANI pin : ANI16 to ANI30 (supply ANI pin to EV_{DD0})

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} \leq V_{DD0} \leq 3.6\text{ V}$, $2.4\text{ V} \leq AV_{DD} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{DD} , Reference voltage (-) = $AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.		T.B.D.	bit
Overall error ^{Note 3}	AINL	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.			μs
		ADTYP = 1, 8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	T.B.D.			μs
Zero-scale error ^{Note 3}	EVS	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Full-scale error ^{Note 3}	EFS	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Integral linearity error ^{Note 3}	ILE	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Differential linearity error ^{Note 3}	DLE	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	LSB
		8-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			T.B.D.	
Analog input voltage	V_{AIN}			T.B.D.		T.B.D.	V
	V_{BGR}	Select internal reference voltage output $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, HS (high-speed main) mode		T.B.D.	T.B.D.	T.B.D.	V

- Notes**
1. Cannot be used for lower 2 bit of ADCR register
 2. Cannot be used for lower 4 bit of ADCR register
 3. Excludes quantization error ($\pm 1/2$ LSB).

(5) When $AV_{REF(+)} =$ Internal reference voltage (1.45 V) ($ADREFP1 = 1$, $ADREFP0 = 0$), $AV_{REF(-)} = AV_{SS}$ ($ADREFM = 0$), target ANI pin : ANI0 to ANI12, ANI16 to ANI30

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $2.4\text{ V} \leq EV_{DD} \leq V_{DD}$, $2.4\text{ V} \leq AV_{DD} \leq V_{DD}$, $V_{SS} = EV_{SS0} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = Internal reference voltage, Reference voltage (-) = $AV_{SS} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		T.B.D.			bit
Conversion time	t_{CONV}	8-bit resolution	T.B.D.			μs
Zero-scale error ^{Note}	E_{ZS}	8-bit resolution			T.B.D.	LSB
Integral linearity error ^{Note}	I_{LE}	8-bit resolution			T.B.D.	LSB
Differential linearity error ^{Note}	D_{LE}	8-bit resolution			T.B.D.	LSB
Reference voltage (+)	$AV_{REF(+)}$	= Internal reference voltage (V_{BGR})	T.B.D.	T.B.D.	T.B.D.	V
Analog input voltage	V_{AIN}		T.B.D.		T.B.D.	V

Note Excludes quantization error ($\pm 1/2$ LSB).

30.6.2 Temperature sensor, internal reference voltage output characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Reference output voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/C
Operation stabilization wait time	t_{AMP}		10			μs

30.6.3 POR circuit characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	T_{PW}		300			μs
Detection delay time					350	μs

30.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq EV_{DD0} \leq V_{DD} \leq 3.6$ V, $V_{SS} = EV_{SS0} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVD2	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		VLVD3	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		VLVD4	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		VLVD5	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		VLVD6	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		VLVD7	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

Remark $V_{LVD(n-1)} > V_{LVDn}$: $n = 3$ to 7

LVD Detection Voltage of Interrupt & Reset Mode

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq EV_{DD0} \leq V_{DD} \leq 3.6$ V, $V_{SS} = EV_{SS0} = 0$ V)

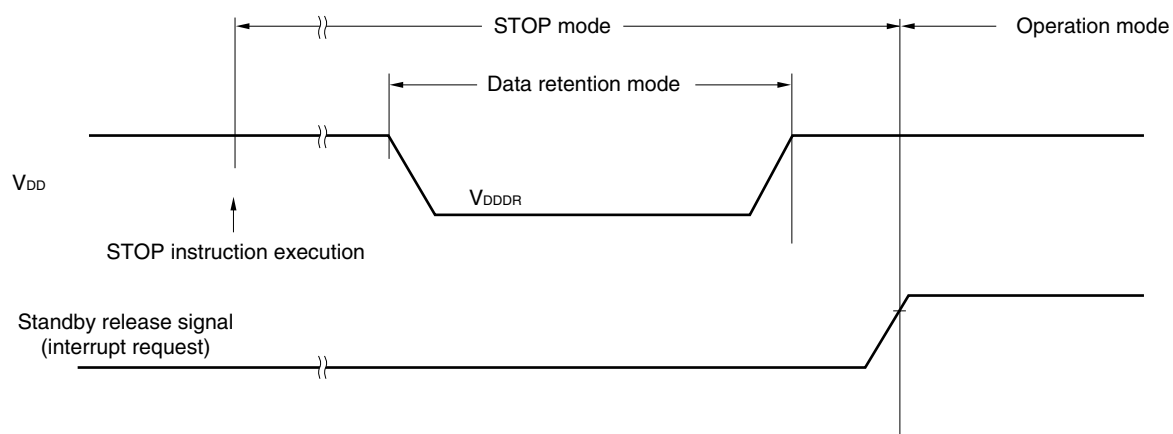
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVD5}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage: 2.7 V		2.64	2.75	2.86	V
	V _{LVD4}	LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V

Caution Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.HS (high-speed main) mode: $V_{DD} = 2.7$ to 3.6 V@1 MHz to 32 MHz $V_{DD} = 2.4$ to 3.6 V@1 MHz to 16 MHz

30.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics $(T_A = -40$ to $+105^\circ\text{C})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 ^{Note}		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.

**30.8 Flash Memory Programming Characteristics** $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = V_{SS0} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f _{CLK}	1.8 V ≤ V _{DD} ≤ 3.6 V		1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years	T _A = 85°C ^{Note 3}	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years	T _A = 25°C ^{Note 3}		1,000,000		
		Retained for 5 years	T _A = 85°C ^{Note 3}	100,000			
		Retained for 20 years	T _A = 85°C ^{Note 3}	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

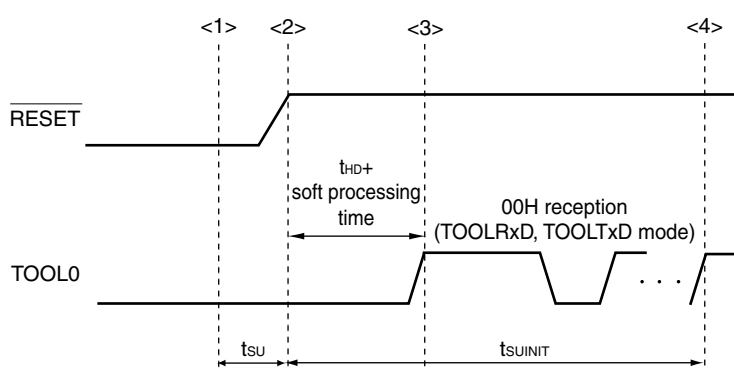
2. When using flash memory programmer and Renesas Electronics self programming library

3. This is a characteristic of the flash memory obtained as a result of our reliability test.

Remark When updating data multiple times, use the flash memory as one for updating data.

30.9 Timing Specs for Switching Flash Memory Programming Modes**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{V}_{\text{DD}} \leq 3.6\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a pin reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the pin reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a pin reset ends	t_{SU}	POR and LVD reset must end before the pin reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time)	t_{HD}	POR and LVD reset must end before the pin reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The pins reset ends (POR and LVD reset must end before the pin reset ends.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

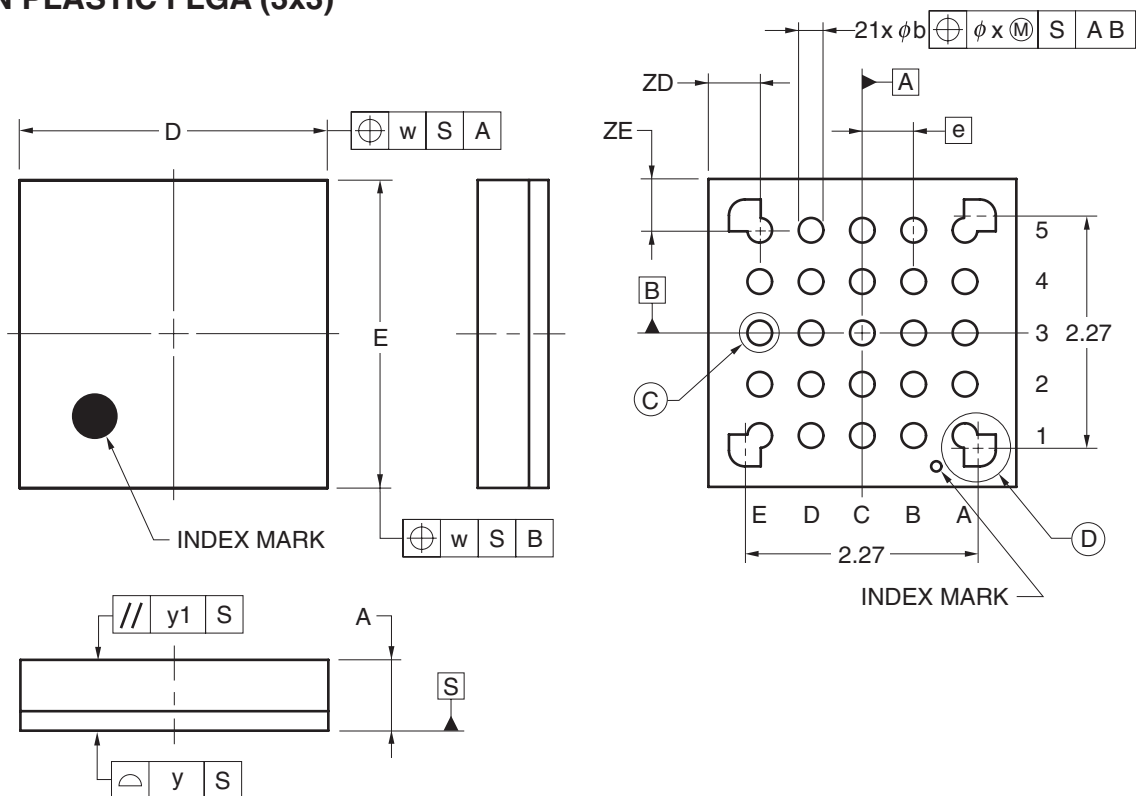
Remark t_{SUINIT} : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end. t_{SU} : How long from when the TOOL0 pin is placed at the low level until a pin reset ends (MIN. 10 μs) t_{HD} : How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

CHAPTER 31 PACKAGE DRAWINGS

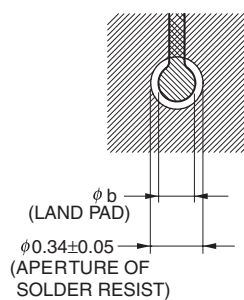
31.1 25-pin products

R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA

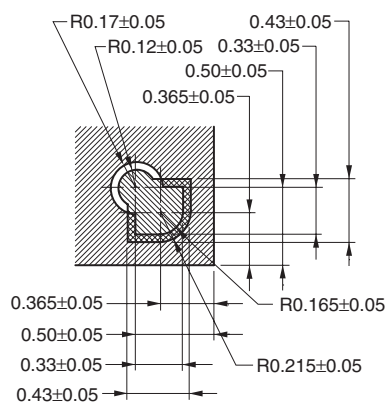
25-PIN PLASTIC FLGA (3x3)



DETAIL OF (C) PART



DETAIL OF (D) PART



(UNIT:mm)

ITEM	DIMENSIONS
D	3.00 ± 0.10
E	3.00 ± 0.10
w	0.20
e	0.50
A	0.69 ± 0.07
b	0.24 ± 0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

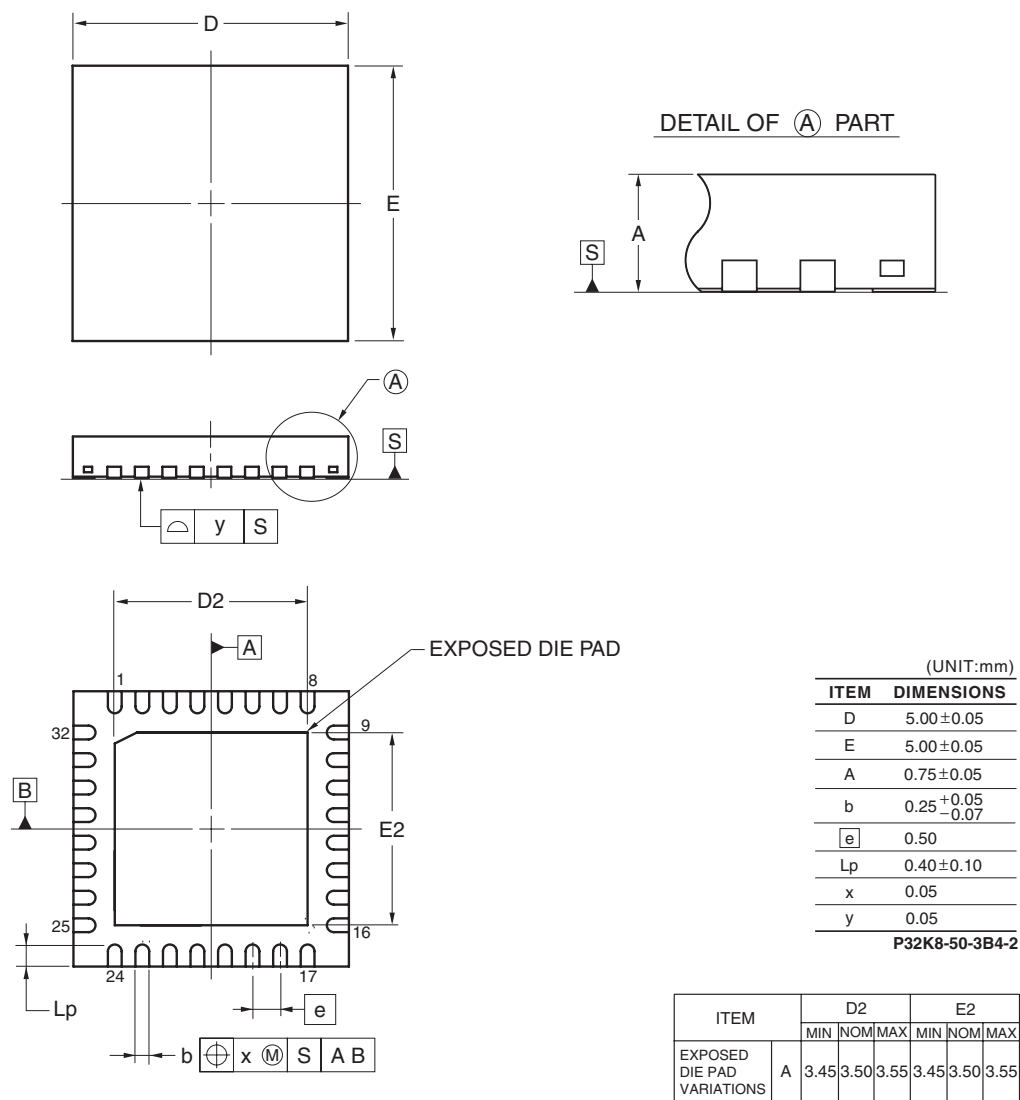
P25FC-50-2N2-1

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31.2 32-pin products

R5F10EBAANA, R5F10EBCANA, R5F10EBDANA, R5F10EBEANA

32-PIN PLASTIC WQFN(5x5)

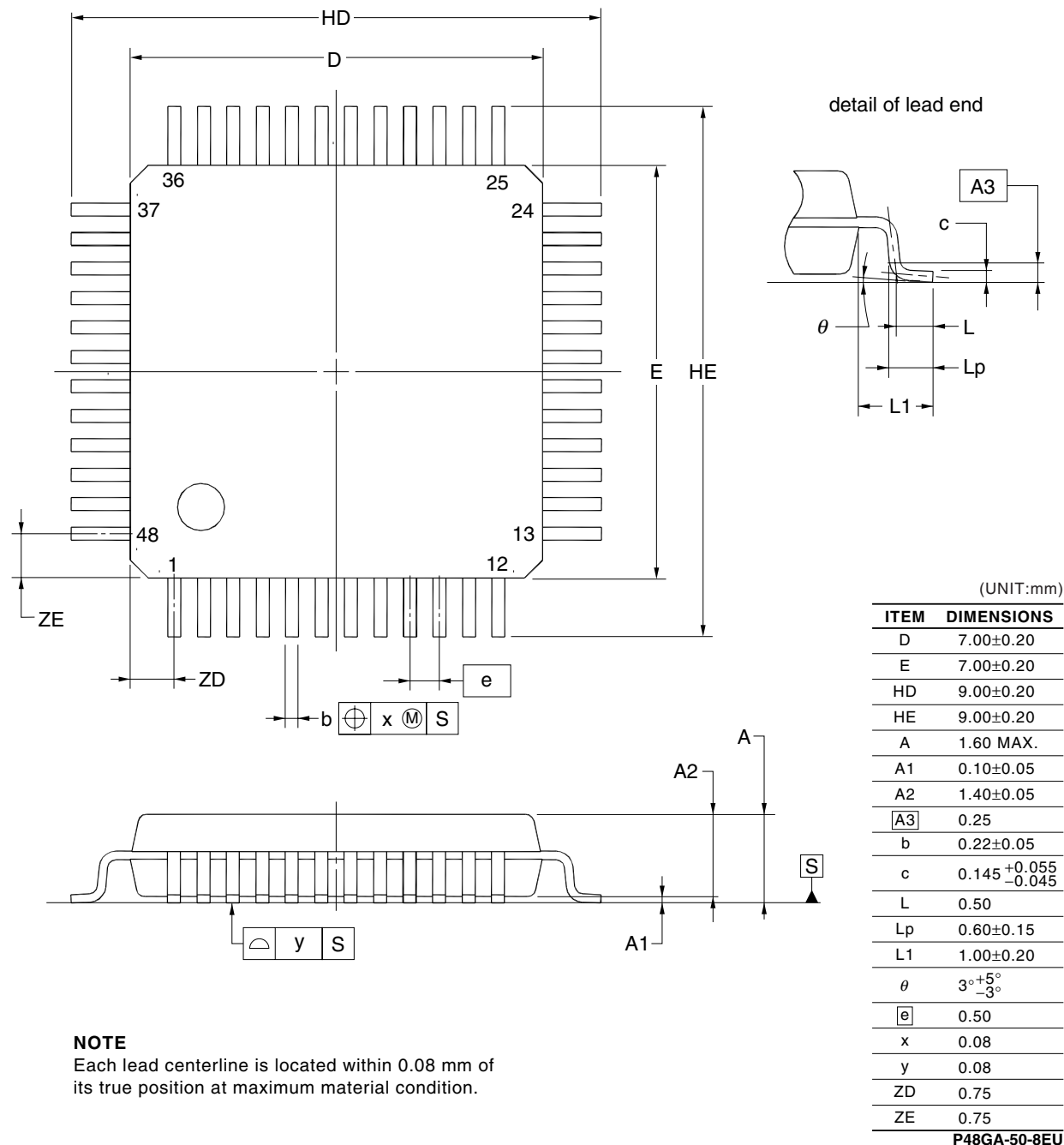


31.3 48-pin products

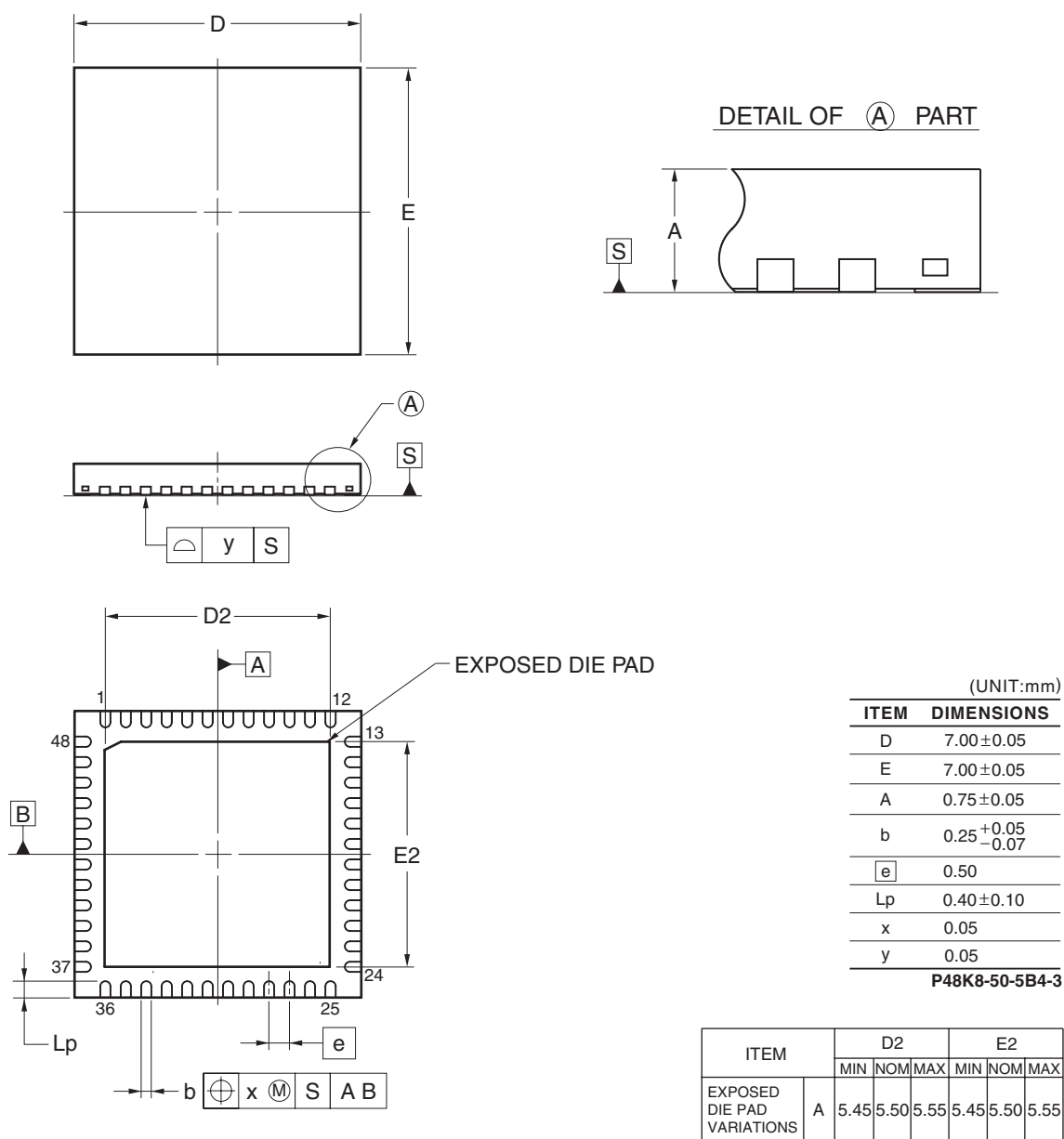
R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB

<R> R5F10EGAGFB, R5F10EGCGFB, R5F10EGDGFB, R5F10EGEGFB

48-PIN PLASTIC LQFP (FINE PITCH)(7x7)



R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA

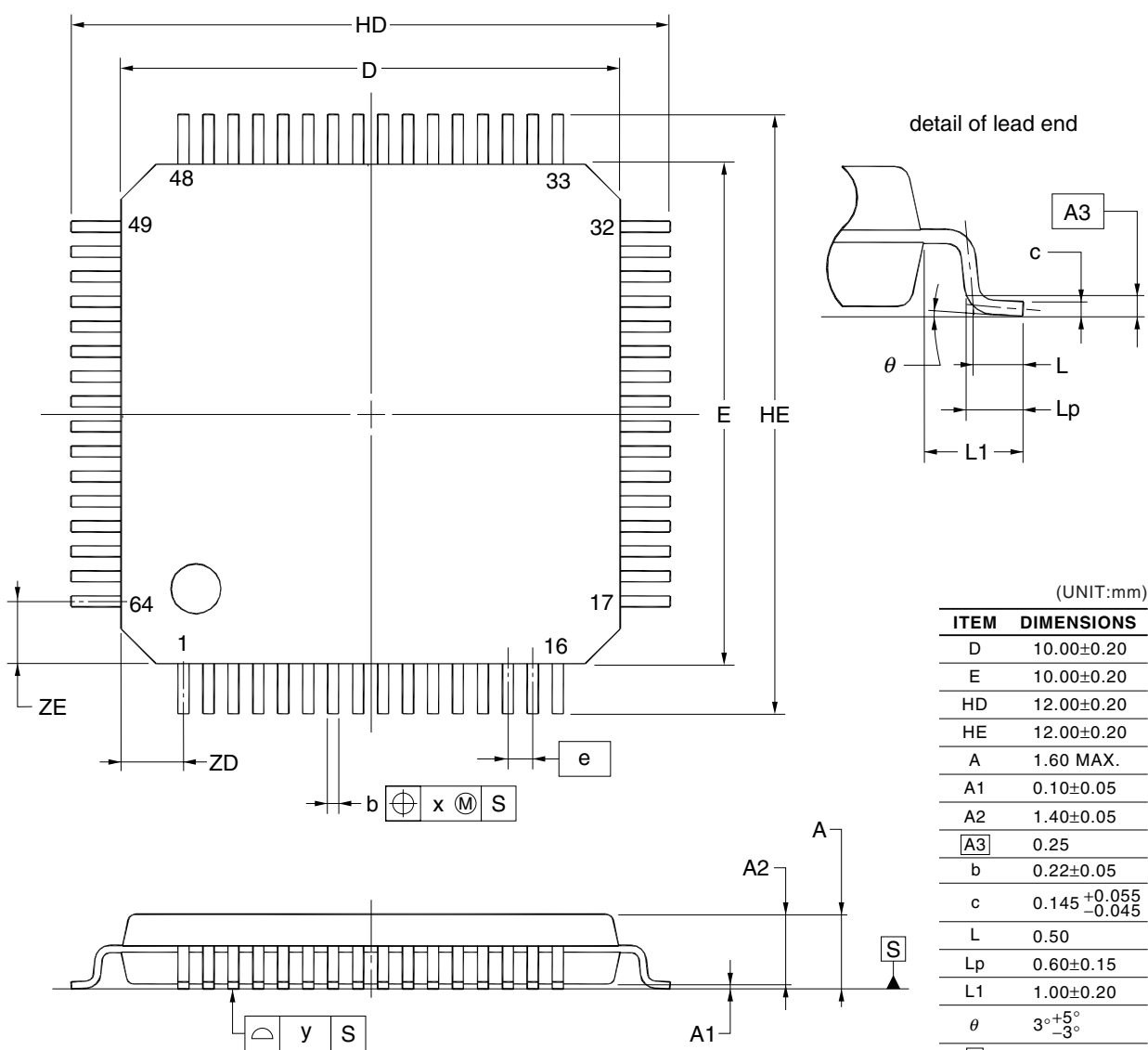
48-PIN PLASTIC WQFN(7x7)

31.4 64-pin products

R5F10ELCAFB, R5F10ELDAFB, R5F10ELEAFB

<R> R5F10ELCGFB, R5F10ELDGFB, R5F10ELEGFB

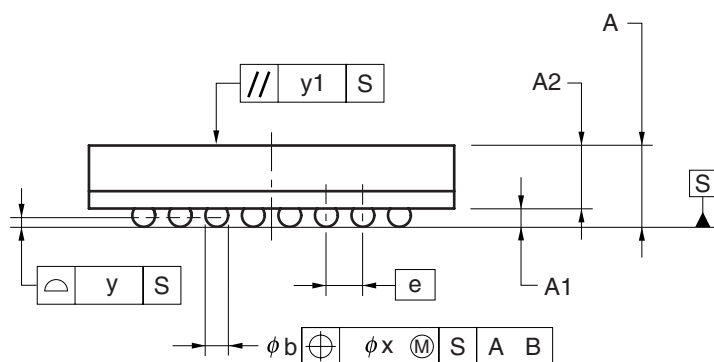
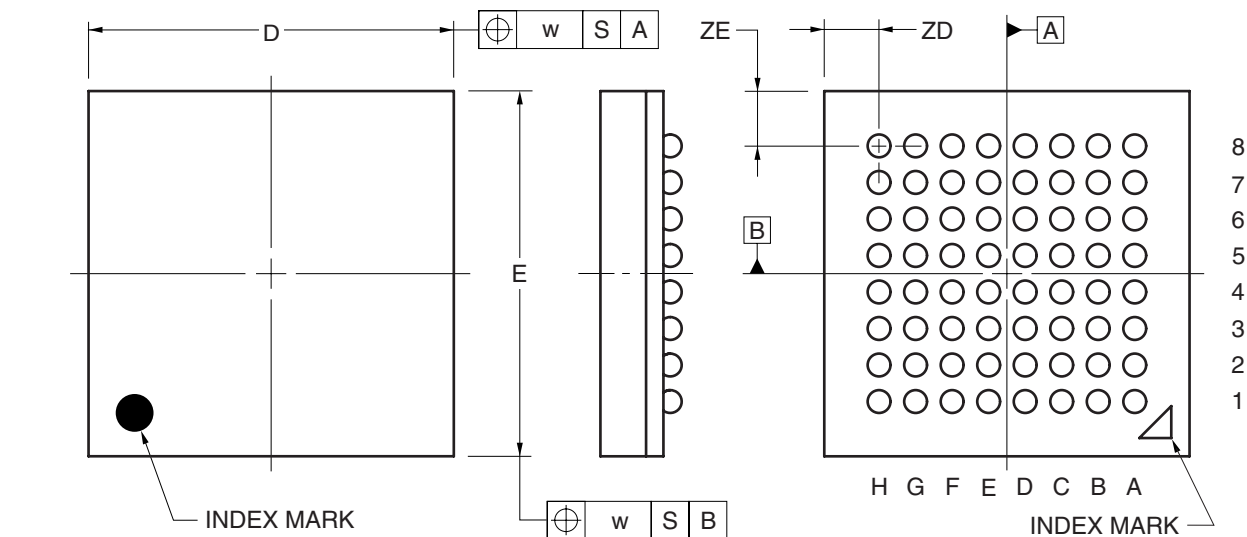
64-PIN PLASTIC LQFP(FINE PITCH)(10x10)



NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F10ELCABG, R5F10ELDABG, R5F10ELEABG

64-PIN PLASTIC FBGA (4x4)

(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.15
A	0.89±0.10
A1	0.20±0.05
A2	0.69
e	0.40
b	0.25±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60

P64F1-40-AA2-1

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APPENDIX A REVISION HISTORY

A.1 Major Revisions in This Edition

(1/9)

Page	Description	Classification
Though out	Renamed interval timer (unit) to 12-bit interval timer	(b)
	Renamed V_{LVI} , V_{LVIH} , V_{LVIL} to V_{LVD} , V_{LVDH} , V_{LVDL} (LVD detection voltage)	(b)
	Renamed interrupt source of RAM parity error (RAMTOP) to RPE	(b)
CHAPTER 1 OUTLINE		
p.3	Modification of 1.2 Ordering Information	(c)
p.4	Addition of Figure 1-1. Part Number, Memory Size, and Package of RL78/G1A	(c)
p.12 to 15	Modification of 1.5.1 25-pin products to 1.5.4 64-pin products	(d)
CHAPTER 2 PIN FUNCTIONS		
p.18	Modification of Table 2-1. Pin I/O Buffer Power Supplies	(b)
p.19 to 25	Modification of 2.1 Port Function	(c)
p.26 to 31	Modification of description in 2.2 Functions other than port pins (Deletion of Description of Port Function)	(c)
p.32	Addition of remark to 2.3 Pin I/O Circuits and Recommended Connection of Unused Pins	(c)
p.33	Change of Table 2-3. Connection of Unused Pins (64-pin products) (2/2)	(c)
CHAPTER 3 CPU ARCHITECTURE		
p.37, 38	Addition of note 1 to Figures 3-1, 3-2	(c)
p.37 to 40	Addition of caution to Figures 3-1 to 3-4	(c)
p.39, 40	Modification of note in Figures 3-3, 3-4	(c)
p.63	Addition of remark to Table 3-1. Correspondence Between Address Values and Block Numbers in Flash Memory	(c)
p.69	Modification of caution 2 in 3.1.3 Internal data memory space	(c)
p.50, 51	Addition of note 1 to Figures 3-6, 3-7	(c)
p.50 to 53	Addition of caution to Figures 3-6 to 3-9	(c)
p.52, 53	Addition of note 1 to Figures 3-8, 3-9	(c)
p.55	Modification of caution 3 in 3.2.1 (3) Stack pointer (SP)	(c)
p.53	Deletion of caution 2 in 3.2.2 General-purpose registers	(c)

Remark "Classification" in the above table classifies revisions as follows.

- (a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

(2/9)

Page	Description	Classification
CHAPTER 4 PORT FUNCTIONS		
p.85	Modification of 4.1 Port Functions	(c)
p.91 to 93, 97, 98 to 102, 115, 122, 124	Modification of block diagrams	(a, c)
p.104	Addition of description to 4.2.3 Port 2	(c)
p.135	Addition of description to 4.2.12 Port 15	(c)
p.137	Addition of caution to 4.3 Registers Controlling Port Function	(c)
p.141	Modification of Figure 4-39. Format of Port Register (64-pin products)	(c)
p.142	Modification of description and addition of caution to 4.3.3 Pull-up resistor option registers (PUxx)	(c)
p.144	Addition of 4.3.5 Port output mode registers (POMxx)	(b)
p.145	Addition of cautions 1 and 2 to Figure 4-43. Format of Port Mode Control Register	(b)
p.146	Addition of caution 1 to Figure 4-44. Format of A/D Port Configuration Register (ADPC)	(b)
p.147	Modification of description in 4.3.8 Peripheral I/O redirection register (PIOR)	(c)
p.148	Addition of remark to 4.3.9 Global digital input disable register (GDIDIS) Modification of description to 4.3.10 Global analog input disable register (GAIDIS)	(c)
p.149	Modification of description in 4.4.1 (2) Input mode and 4.4.3 (2) Input mode	(b)
p.151	Addition of description to 4.4.4 (2) Setting procedure when using I/O pins of IIC00, IIC10, and IIC20 functions	(c)
P.152	Addition of caution to 4.5 Settings of Port Mode Register, and Output Latch When Using Alternate Function	(c)
p.158	Addition of 4.6.2 Notes on specifying the pin settings	(c)
CHAPTER 5 CLOCK GENERATOR		
p.159	Addition of 5.1 (1) <2> High-speed on-chip oscillator	(b)
p.162	Modification of Figure 5-1. Block Diagram of Clock Generator	(b)
p.164	Modification of caution 1 and addition of cautions 4 to 6 to Figure 5-2. Format of Clock Operation Mode Control Register (CMC)	(c)
p.176	Modification of cautions 1 to 3 in Figure 5-9. Format of High-speed On-chip Oscillator Frequency Select Register (HOCODIV)	(a)
p.184	Modification of note 3 in Figure 5-14. Clock Generator Operation When Power Supply Voltage Is Turned On	(c)

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- (a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

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Page	Description	Classification
p.186	Addition of description to 5.6.2 Example of setting X1 oscillation clock	(c)
p.188	Addition of description to Figure 5-15. CPU Clock Status Transition Diagram	(c)
p.189	Modification of Table 5-3. CPU Clock Transition and SFR Register Setting Examples	(c)
p.194	Modification and deletion of description in Table 5-4. Changing CPU Clock	(c)
p.196	Modification of remark 2 to 5.6.6 Time required for switchover of CPU clock and system clock	(b)
p.198 to 201	Addition of 5.7 Recommended Oscillator Constants	(c)
CHAPTER 6 TIMER ARRAY UNIT		
p.205	Modification of description in 6.1.1 (7) Delay counter	(a)
p.206	Modification of caution in 6.1.2 (3) Multiple PWM (Pulse Width Modulation) output	(c)
p.211	Modification of Figure 6-2. Internal Block Diagram of Channels of Timer Array Unit 0, 2, 4, 6	(a)
p.211 to 213	Addition of Figures 6-3 to 6-6	(c)
p.214	Modification of Table 6-3. Timer Count Register mn (TCRmn) Read Value in Various Operation Modes	(c)
p.219	Modification of note and remark 2 and addition of caution to Figure 6-11. Format of Timer Clock Select register m (TPSm)	(c)
p.222 to 225	Modification of Figure 6-12. Format of Timer Mode Register mn (TMRmn)	(a)
p.231	Modification of description in Figure 6-18. Format of Timer Output Enable register m (TOEm)	(c)
p.243	Modification of description in 6.5.1 (1) When operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits is selected (CCSmn = 0)	(c)
p.245	Modification of description in Table 6-6. Operations from Count Operation Enabled State to Timer count Register mn (TCRmn) Count Start	(c)
p.246	Addition of title and remark to 6.5.3 Operation of counter	(c)
p.248	Modification of description, remark and addition note to Figure 6-29. Start Timing (In Capture Mode : Input Pulse Interval Measurement)	(a)
p.250	Modification of remark 1 in Figure 6-31. Operation Timing (In Capture & One-count Mode : High-level Width Measurement)	(c)
p.252	Modification of description in 6.6.2 TOmn Pin Output Setting	(c)
p.254 to 256	Modification of Figures 6-34 to 6-36	(c)
p.262, 268, 277, 281, 285, 292, 307	Modification of description in Figures 6-43, 6-47, 6-55, 6-59, 6-63, 6-68, 6-78 Example of Set Contents of Registers	(a)
p.266, 271, 275, 280, 283, 289	Modification of Figures 6-45, 6-49, 6-57, 6-61, 6-65 Block Diagram	(b)
p.270, 274, 278, 282, 287, 294, 308	Modification of Figures 6-48, 6-52, 6-56, 6-60, 6-64, 6-69, 6-79 Operation Procedure	(c)
p.302, 303, 305, 307	Modification of remark in 6.8.3 Operation as multiple PWM output function	(a)

Remark "Classification" in the above table classifies revisions as follows.

- (a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

(4/9)

Page	Description	Classification
CHAPTER 7 REAL-TIME CLOCK		
p.329	Modification of 7.4.2 Shifting to HALT/STOP mode after starting operation	(c)
p.336	Modification of Figure 7-23. Operation when (DEV, F6, F5, F4, F3, F2, F1, F0) = (1, 1, 1, 0, 1, 1, 1, 0)	
p.341	Modification of Figure 8-5. 12-bit Interval Timer Operation Timing (ITCMP11 to ITCMP0 = 0FFH, count clock: $f_{SUB} = 32.768$ kHz)	
CHAPTER 9 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER		
p.343	Addition of caution in 9.1 Functions of Clock Output/Buzzer Output Controller	(c)
p.345	Modification of Figure 9-2. Format of Clock Output Select Register n (CKSn)	(c)
p.347	Addition of 9.5 Cautions of clock output/buzzer output controller	(c)
CHAPTER 10 WATCHDOG TIMER		
p.348, 354	Modification of description in 10.1 Functions of Watchdog Timer, 10.4.4 Setting watchdog timer interval interrupt	(b)
p.349	Modification of Figure 10-1 . Block Diagram of Watchdog Timer	
CHAPTER 11 A/D CONVERTER		
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A.2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

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Ver.0.02	Change of Table 2-3. Connection of Unused Pins (64-pin products)	CHAPTER 2 PIN FUNCTIONS
	Change of Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used	CHAPTER 11 A/D CONVERTER
	Change of Table 11-3. A/D Conversion Time Selection	
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	Change of Conditions in 29.7.1 A/D converter characteristics	CHAPTER 29 ELECTRICAL SPECIFICATIONS (TARGET)

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