12-INPUT NAND GATE — 54/74134

SPEED/PACKAGE AVAILABILITY

54S F,W 74S B,F

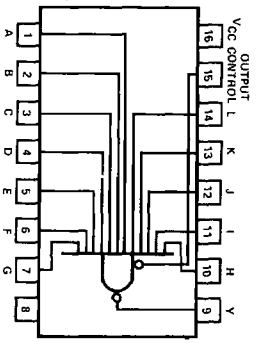
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS		54/74S C_L=15pF R_L=280Ω			
PARAMETER		MIN	TYP	MAX	UNIT
Propagation delay time					
t_{PLH}	Low-to-high	2	4	6	ns
t_{PHL}	High-to-low	2	5	7.5	
		C_L=50pF			
t_{PLH}	Low-to-high		5.5		
t_{PHL}	High-to-low		7		
Output enable time		C_L=50pF			
t_{ZH}	To High level		13	19.5	ns
t_{ZL}	To low level		14	21	
Output disable time		C_L=5pF			
t_{HZ}	From high level		5.5	8.5	ns
t_{LZ}	From low level		9	14	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

INPUTS												OUTPUT	OUTPUT
A	B	C	D	E	F	G	H	I	J	K	L	CONTROL	Y
H	H	H	H	H	H	H	H	H	H	H	H	L	H
ANY NUMBER OF INPUTS LOW												L	H
X	X	X	X	X	X	X	X	X	X	X	X	H	Z

H = high logic level, L = low logic level, X = irrelevant
Z = high-impedance (output off)

LOGIC

QUAD EXCLUSIVE-OR/NOR GATE — 54/74135

SPEED/PACKAGE AVAILABILITY

54S W,F 74S B,F

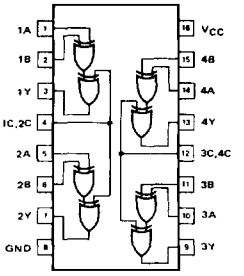
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time							
t_{PLH}	Low-to-high	A,B	B,A = L, C = L		8.5	13	ns
t_{PHL}	High-to-low				11	15	
t_{PLH}	Low-to-high	A,B	B,A = H, C = L		8	12	
t_{PHL}	High-to-low				9	13.5	
t_{PLH}	Low-to-high	A,B	B,A = L, C = H		10	15	
t_{PHL}	High-to-low				6.5	10	
t_{PLH}	Low-to-high	A,B	B,A = H, C = H		8.5	12	
t_{PHL}	High-to-low				7	11	
t_{PLH}	Low-to-high	C	A = B		8	12	
t_{PHL}	High-to-low				9.5	14.5	
t_{PLH}	Low-to-high	C	A ≠ B		7.5	11.5	
T_{PHL}	High-to-low				8	12	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = high level, L = low level