ID342K01

Flash Miniature Card

16M

(Model No.: ID342K01)

Spec No.: U904005
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  - Instrumentation and measuring equipment
  - Machine tools
  - Audiovisual equipment
  - Home appliances
  - Communication equipment other than for trunk lines

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  - Mainframe computers
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  - Gas leak detectors and automatic cutoff devices
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1. General Descriptions

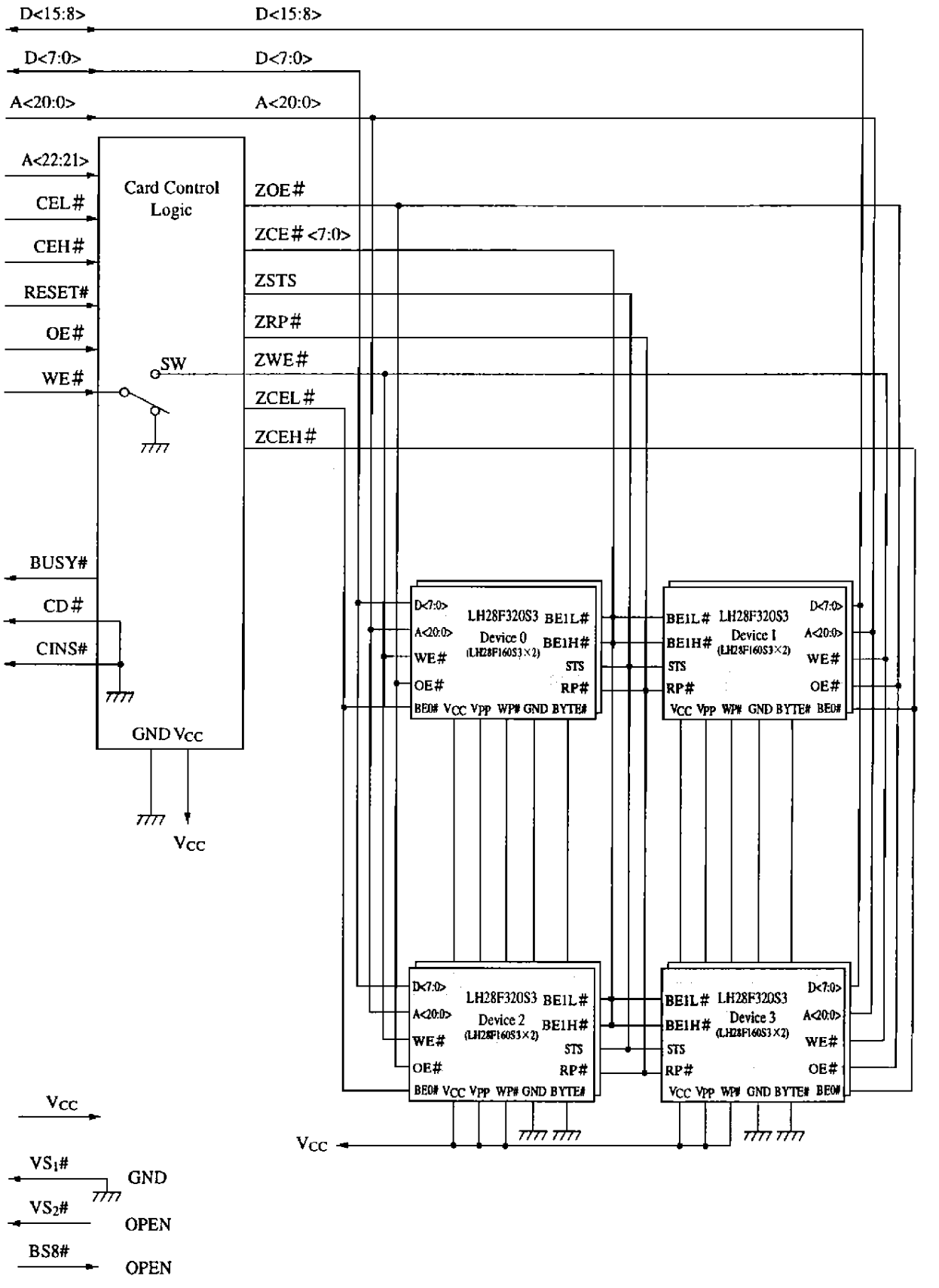
The SHARP ID342K01, which panel design is SHARP standard, is a 16MB Flash Memory Miniature Card conforms to Miniature Card Specification Release 1.1 and is offered to customers giving aim to confirm an external shape or electrical performances of the card. Before mass production, we will create a new product name dedicated for a customer and also present a specification which implies customer's request including panel design.

2. Features

2.1	Type	16MB Flash Memory Miniature Card (Conforms to Miniature Card Specification Release 1.1)
2.2	Memory Capacity Main Memory	8M words × 16 bits (16M words × 8 bits)
2.3	Supply Voltage	3.3V ± 0.3V
2.4	Erase Unit	64K word Blocks
2.5	Program/Erase Cycles	100,000 cycles per Block
2.6	Interface	Parallel I/O Interface
2.7	Function Table	See Function Table in page. 10
2.8	External Dimensions	33.0 × 38.0 × 3.5 mm
2.9	Pin Connections	See Pin Connections in page. 5
2.10	Type of Connector	Conforms to Miniature Card Specification Release 1.1 Card Use Connector
2.11	Average Weight	9g
2.12	Operating Temp. Range	0 to 60°C
2.13	Storage Temp. Range	–30 to 70°C
2.14	External Appearance	External appearance shall be free of any dirt, cratches and abnormalities that could adversely affect sales.
2.15	Manufacturer's Code	The manufacturer's code shall be printed on the Miniature card directly or on the seal which is then attached to the Miniature card.
2.16	Brand Name	The user's brand name will used.

2.17 Not designed for rated radiation hardened.

3. Block Diagram



4. Pin Connections

PAD#	SIGNAL	I/O	FUNCTION	ACTIVE
1	A_{18}	I	Address Bit 18	
2	A_{16}	I	Address Bit 16	
3	A_{14}	I	Address Bit 14	
4	Vccr	I	Voltage Refresh	N.C.
5	CEH#	I	Card Enable High Byte	Low
6	A_{11}	I	Address Bit 11	
7	A_9	I	Address Bit 9	
8	A_8	I	Address Bit 8	
9	A_6	I	Address Bit 6	
10	A_5	I	Address Bit 5	
11	A_3	I	Address Bit 3	
12	A_2	I	Address Bit 2	
13	A_0	I	Address Bit 0	
14	RAS#	I	Row Address Strobe	N.C.
15	A_{24}	I	Address Bit 24	N.C.
16	A_{23}	I	Address Bit 23	N.C.
17	A_{22}	I	Address Bit 22	
18	OE#	I	Output Enable	Low
19	D_{15}	I/O	Data Bit 15	
20	D_{13}	I/O	Data Bit 13	
21	D_{12}	I/O	Data Bit 12	
22	D_{10}	I/O	Data Bit 10	
23	D_9	I/O	Data Bit 9	
24	D_0	I/O	Data Bit 0	
25	D_2	I/O	Data Bit 2	
26	D_4	I/O	Data Bit 4	
27	RFU		Reserved	
28	D_7	I/O	Data Bit 7	
29	SDA	I/O	Serial Data and Address	N.C.
30	SCL	I	Serial Clock	N.C.

PAD#	SIGNAL	I/O	FUNCTION	ACTIVE
31	A_{19}	I	Address Bit 19	
32	A_{17}	I	Address Bit 17	
33	A_{15}	I	Address Bit 15	
34	A_{13}	I	Address Bit 13	
35	A_{12}	I	Address Bit 12	
36	RESET#	I	Reset	Low
37	A_{10}	I	Address Bit 10	
38	VS_1#	O	Voltage Sence 1	Low
39	A_7	I	Address Bit 7	
40	BS8#	I	Bus Size 8	N.C.
41	A_4	I	Address Bit 4	
42	CEL#	I	Card Enable Low Byte	Low
43	A_1	I	Address Bit 1	
44	CASL#	I	Column Address Strobe Low Byte	N.C.
45	CASH#	I	Column Address Strobe High Byte	N.C.
46	CD#	O	Card Detect	Low
47	A_{21}	I	Address Bit 21	
48	BUSY#	O	Ready/Busy	Low
49	WE#	I	Write Enable	Low
50	D_{14}	I/O	Data Bit 14	
51	RFU		Reserved	
52	D_{11}	I/O	Data Bit 11	
53	VS_2#	O	Voltage Sence 2	N.C.
54	D_8	I/O	Data Bit 8	
55	D_1	I/O	Data Bit 1	
56	D_3	I/O	Data Bit 3	
57	D_5	I/O	Data Bit 5	
58	D_6	I/O	Data Bit 6	
59	RFU		Reserved	
60	A_{20}	I	Address Bit 20	

Power/Insertion Signals

SIGNAL NO.	SIGNAL
61	GND
62	CINS#
63	V_{CC}

Interface Signals

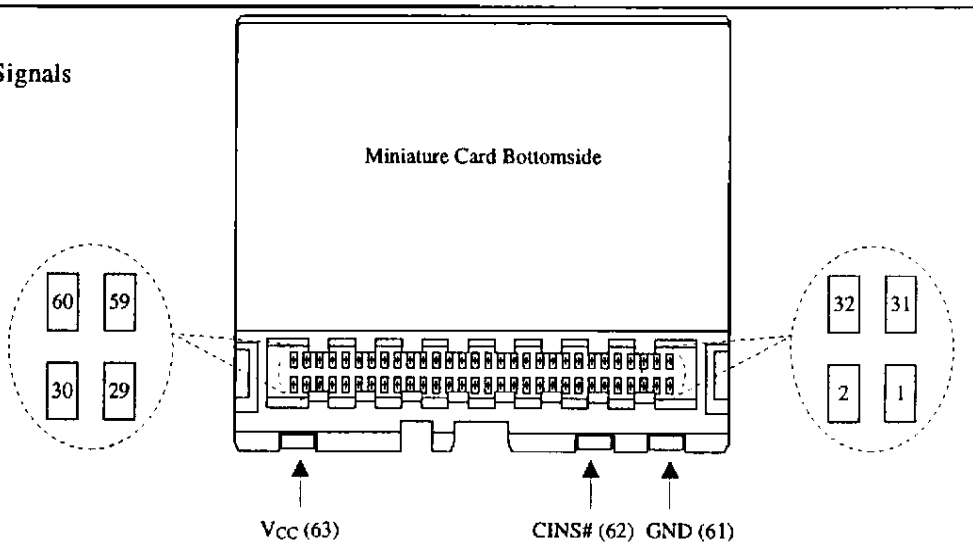


Figure 1. Card Interface Signal Assignment

5. Signal Description

Interface Signal Description

Symbol	Type	Name and Function
A_0-A_{24}	INPUT	**ADDRESS INPUTS:** Addresses A_0 through A_{24} enable direct addressing of up to 64 MB of memory on the card. The memory will wrap at the card density boundary. The system should NOT try to access memory beyond the card's density, since the upper addresses are not decoded.
D_0-D_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** D_0 through D_{15} constitute the bi-directional data bus. D_{15} is the most significant bit.
CEL# CEH#	INPUT	**CARD ENABLE LOW & HIGH:** CEL# enables accesses on the low byte of the data bus D_{0-7}. CEH# enables accesses on the high byte of the data bus D_{8-15}. Both CEL# and CEH# are active low signals. A 16-bit host must always assert both CEL# and CEH#.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal, enables read data from the Miniature card.
WE#	INPUT	**WRITE ENABLE:** Active low signal, enables write data to the Miniature card.
BUSY#	OUTPUT	**BUSY:** Active low signal, indicates the status of internally timed erase or write activities. A high output indicates the Miniature card is ready to accept another command
CD#	OUTPUT	**CARD DETECT:** Active low signal, provides for card insertion detection. CD# connects to ground internally on the Miniature card, and will be forced low when the CD# interface signal connects to the host.
RESET#	INPUT	**RESET:** Active low input signal, resets the device's command user interface and places the card into a deep power-down mode. The host must drive this signal.
VS_1# VS_2#	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's V_{CC} requirements. VS_1# is grounded and VS_2# is left open to indicate a 3.3V capable card has been inserted.
RFU	—	**RESERVED FOR FUTURE USE**

Power/Insertion Signal Description

Symbol	Type	Name and Function
CINS#	OUTPUT	**CARD INSERTION DETECT:** This signal provides for early card insertion detection. CINS# connects to ground internally on the Miniature card, and will be forced low when the power/insertion signals connect to the host.
V_{CC}	—	**CARD POWER SUPPLY:** 5.0V
GND	—	**GROUND**

6. LH28F320S3 Control Logic

6. 1 Bus Operations

The host executes read, write and erase operations by issuing the appropriate command to the flash device's Command User Interface (CUI). The CUI serves as the interface between the host processor and internal operation of the flash device. These commands can be issued to the CUI using standard microprocessor bus cycles.

6. 1. 1 Read Array

The host enables reads from the card by writing the appropriate read command to the CUI. The LH28F320S3 automatically resets to read array mode upon initial device power-up, or after reset. CEL#, CEH#, and OE# must be logically active to obtain 16 data bits at the outputs. The Card Enables (CEL# and CEH#) are used to select the addressed devices. Output Enable (OE#) is the data input/output (D_0–D_{15}) direction control, and when active, drives data from the selected memory onto the data bus. WE# and RESET# must be driven to V_{IH} during a read access.

6. 1. 2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Outputs (D_0–D_{15}) are placed in a high-impedance state.

6. 1. 3 Standby

CEL# and CEH# at a logic-high level (V_{IH}) places the card in standby mode. Standby operation disables much of the card's circuitry and substantially reduces device power consumption. The outputs (D_0–D_{15}) are placed in a high-impedance state independent of the status of OE#. If the host deselects the card during a write or erase, the card continues to function and consume normal active power until the operation completes.

6. 1. 4 Deep Power-Down

RESET# at V_{IL} initiates the deep power-down mode.

During reads, an active RESET# deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. RESET# must be held low for a minimum of 100 ns. After returning from deep power-down, the host must wait before initial memory access outputs are valid, as determined by t_{PHQV}. After this wake-up interval, the host can resume normal operations to the card. Card reset forces the CUI to reset to read array mode and sets the status register to 80H.

During block erase, full chip erase or (multi)word/byte write, an active RESET# will abort the operation. BUSY# remains low until the reset operation completes. Memory contents being altered are no longer valid; the data may be partially erased or written. The host must wait after RESET# goes to logic-High (V_{IH}) before it can write another command, as determined by t_{PHWL}.

It is important to assert RESET# to the card during a system reset. Automated flash memories provide status information when accessed during block erase, full chip erase and (multi) word/byte write. If a CPU reset occurs without a card reset, the host will not be able to read from the card if that card is in a different mode when the system reset occurs. For example, if an end-user initiates a host reset when the card is in read status register mode, the host will attempt to read code from the card, but will actually read status register data.

Sharp's ID342K01 Series Flash Memory Miniature Card allows proper card reset following a system reset through the use of the RESET# input. System RESET# circuitry can reset the host CPU in addition to the card.

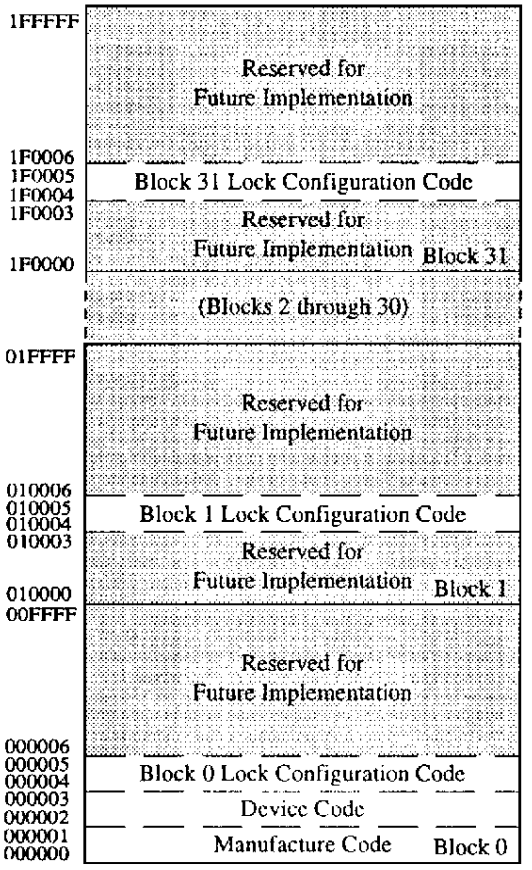


Figure 2. Device Identifier Code Memory Map

6. 1. 5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code (Block 0), device code (Block 0), and block lock configuration codes (for each block), see Figure 2. Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock codes identify locked and unlocked blocks. This card is can not lock bit configuration.

6. 1. 6 Query Operation

The query operation outputs the query structure. Query database is stored in the 48byte ROM. Query structure allows system software to gain critical infomation for controlling the flash component.

6. 1. 7 CUI Writes

Writes to the CUI enable reading of device data and intelligent identifiers. They also control inspection and clearing of the Status Register.

The CUI itself does not occupy an addressable memory location. The interface register is a latch used to store the command, address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Write Setup command requires both appropriate command data and the address of the location to be written, while the Write command consists of the data to be written and the address of the location to be written.

The CUI is written by bringing WE# to a logic-low level (V_{IL}) while CEL#,CEH# is low. Addresses and data are latched on the rising edge of WE#. Standard microprocessor write timings are used.

When a write or erase command has been issued to the CUI, the internal Write State Machine (WSM) becomes busy and will not be ready until it has completed the operation.

7. Card Control Logic

7. 1 Word Addressing

Sharp's ID342K01 Series Flash Memory Miniature Card uses two × 8 devices in parallel to form the Miniature card × 16 data bus. If the host writes a command to the card, it must make sure that it writes the command to both devices in the card. For example, a component write command is 40H, so a card write command must be 4040H. This same procedure must be followed when reading from the status register. A component status register is only 8 bits and may return 80H when read. However, the card status register is 16 bits and may return 8080H.

7. 2 Decode Logic

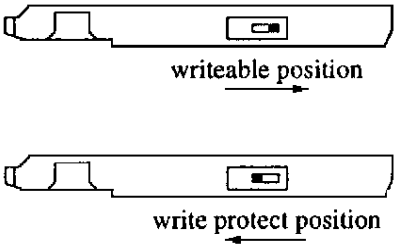
The decode logic enables the appropriate component device pair during a read or write access. Unused upper addresses for the ID342K01 Series Flash Memory Miniature Card will not be decoded. The address decoding will wrap around at the card's density.

7. 3 Write Protect Switch

The ID343K01 Series Flash Memory Miniature Card has a write protect switch on the side of the card. When the switch is in the write protect position, the card blocks all writes to the card (see Figure 3).

NOTE

When the write protect switch is in the write protect position, all writes are disabled to the flash array including all commands to the CUI.



NOTE:
The write protect switch is represented by the solid black rectangle.

Figure 3. Write Protect Switch

7. 4 Data Control

As shown in Table 1. data paths and directions are selected by the Data Control logic using WE#, OE#, CEL#, and CEH#, as logic inputs.

NOTE:

This card has a ×16 interface. The High byte CANNOT be accessed on the lower data path (D_{0-7}).

Mode	RESET#	CEH#	CEL#	OE#	WE#	A_0	D_{8-15}	D_{0-7}	Notes
Low Byte-Read	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	×	High-Z	Low (6)	1.2.3
High Byte-Read	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	×	High (6)	High-Z	1.2.3
Word-Read	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	×	High (6)	Low (6)	1.2.3
Low Byte-Write	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	×	×××	Low (6)	3.4
High Byte-Write	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	×	High (6)	×××	3.4
Word-Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	×	High (6)	Low (6)	3.4
Manufacturer ID	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	B0H	B0H	—
Device ID	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	D0H	D0H	5
Query	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	See Table 5~9	Note 7	Note 7	—
Standby	V_{IH}	V_{IH}	V_{IH}	×	×	×	High-Z	High-Z	—
Output Disable	V_{IH}	×	×	V_{IH}	V_{IH}	×	High-Z	High-Z	—
Power-Down	V_{IL}	×	×	×	×	×	High-Z	High-Z	—

Table 1. Function Table

NOTES:

1. Refer to DC Characteristics.
2. × can be V_{IL} or V_{IH} for control pins and address.
3. BUSY# is V_{OL} when the WSM is executing internal byte write or block erase algorithms. It is V_{OH} when the WSM is not busy, in erase suspend mode, or deep power-down mode.
4. Refer to Table 2 for valid D_{IN} during a write operation.
5. Although the device code is D0H, other Sharp's Flash Memory Miniature Card could also have device codes AAH, A6H or A7H. Software should check for all four cases for compatibility with future cards.
6. High indicates high byte data, Low indicates low byte data.
7. See section 8.5 for query data.

8. Command Definitions

Device operations are selected by writing specific commands into the Command User Interface. Table 2 defines the LH28F320S3 commands.

NOTE:

When the write protect switch is in the write protect position, all writes are disabled to the flash array including commands to the CUI.

Table 2. Command Definitions (7)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array/Reset	1	—	Write	×	FFFFH	—	—	—
Read Identifier Codes	≥2	4	Write	×	9090H	Read	IA	ID
Query	≥2	—	Write	×	9898H	Read	QA	QD
Read Status Register	2	—	Write	×	7070H	Read	×	SRD
Clear Status Register	1	—	Write	×	5050H	—	—	—
Block Erase Setup / Confirm	2		Write	BA	2020H	Write	BA	D0D0H
Full Chip Erase Setup / Confirm	2		Write	×	3030H	Write	×	D0D0H
Word / Byte Write Setup / Write	2	5	Write	WA	4040H or 1010H	Write	WA	WD
Multi Word / Byte Write Setup / Confirm	≥4	6	Write	WA	E8E8H	Write	WA	N-1
Block Erase and (Multi) Word/byte Write Suspend	1		Write	×	B0B0H	—		—
Confirm and Block Erase and (Multi)Word/byte Write Resume	1		Write	×	D0D0H	—		—

NOTES:

1. BUS operations are defined in Table 1.
2. × = Any valid address within the device.
   IA = Identifier Code Address: see Figure 2.
   QA = Query Offset Address.
   BA = Address within the block being erased or locked.
   WA = Address of memory location to be written.
3. SRD = Data read from status register. See Table 10 for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (Whichever goes high first).
   ID = Data read from identifier codes.
   QD = Data read from query database.
4. Following the Read Identifier Codes command, read operations access manufacturer, device and block status codes. See Section 8.2 for read identifier code data.
5. Either 40H or 10H are recognized by the WSM as the byte write setup.
6. Following the Third Bus Cycle, inputs the write address and write data of 'N' times. Finally, input the confirm command 'D0D0H'.
7. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

8. 1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the card defaults to read array mode. The host can also read by writing the Read Array command. The device remains enabled for reads until the host writes another valid command. Once the internal WSM has started a block erase, full chip erase or (multi) word/byte write, the device will not recognize the Read Array command until the WSM completes its operation. However, the host can suspend the WSM using an Erase Suspend or Word Write Suspend command. RESET# must be V_{IH}.

8. 2 Read Identifier Codes Command

The host initiates the identifier code operation by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 2 retrieve the manufacturer, device and block lock configuration codes (see Table 3 for identifier code data). To terminate the operation, write another valid command. Although Table 3 lists the device code as D0D0, other Sharp's Flash Memory Miniature Card could also have device codes AAAA, A6A6 or A7A7. Host software should check for all four cases for compatibility with future cards.

Table 3. Identifier Codes

Code	Address	Data
Manufacture Code	00000 00001	B0B0
Device Code	00002 00003	D0D0
Block Status Code	×0004(1) ×0005(1)	
• Block is Unlocked		$D_{0,8} = 0$
• Block is Locked (3)		$D_{0,8} = 1$
• Last erase operation completed successfully		$D_{1,9} = 0$
• Last erase operation did not completed successfully		$D_{1,9} = 1$
• Reserved for Future Use		$D_{2\text{-}7}, D_{10\text{-}15}$

NOTES:
1. × selects the specific block status code to be read. See Figure 2 for the device identifier code memory map.
2. The addresses listed are word addresses and store 16 bits of data.
3. This card is can not lock bit configuration.

8. 3 Read Status Register Command

The LH28F320S5B components on the ID342K01 Series Flash Memory Miniature Card each contain a Status Register which may be read to determine when a (multi) word/byte write, block erase or full chip erase is complete, and whether that operation completed successfully (see Table 10). The host may read the Status Register at any time by writing the Read Status Register command to the CUI. After writing this command, all subsequent read operations output data from the Status Register, until the host writes another valid command to the CUI. The flash components latch the contents of the Status Register on the falling edge of OE# or CE#, whichever occurs first. OE# or CE# must be toggled to V_{IH} before further reads to update the Status Register latch. RESET# must be V_{IH}.

NOTE:
The ID342K01 Series Flash Memory Miniature Card arranges two LH28F320S3 devices in parallel to from a ×16 bus. Both status registers need to be checked when determining the status of a ×16 erase/write operation.

8. 4 Clear Status Register Command

The WSM sets the Erase Status and Write Status bits to "1"s and they can only be reset by the Clear Status Register command. These bits indicate various failure conditions(see Table 10). By allowing system software to reset these bits, seversl operations (such as cumulatively erasing or locking multiple blocks or writting several bytes in sequence) may be performed. The status register may be polled to determine if an error occurs during the sequence.

The WSM sets these bits to "1" when a write or erase operation has failed. The host can issue additional write and erase commands to the CUI without clearing the status register. This allows a system to write a sequence of bytes before checking the write status bit. However, if an error has occurred the system will not know which write in the sequence has failed. To clear the Status Register, the Clear Status Register command (5050H) is written to the CUI.

RESET# must be V_{IH}. This command is not functional during block erase, full chip erase, (multi) word/byte write, block erase suspend or (multi) word/byte write suspend modes.

8. 5 Query Command

Query database can be read by writing Query command (98H). Following the command write, read cycle from address shown in Table 5~ 8 retrieve the critical information to write, erase and otherwise control the flash component. A_0 of query offset address is ignored. RESET# must be V_{IH}.

Table 4. Example of Query Output

Mode	Offset Address	Output	
		DQ_{15-8}	DQ_{7-0}
×16Mode	A_5,A_4,A_3,A_2,A_1,A_0		
	1, 0, 0, 0, 0, 0 (20H)	"Q"	"Q"
	1, 0, 0, 0, 0, 1 (21H)	"Q"	"Q"
	1, 0, 0, 0, 1, 0 (22H)	"R"	"R"
	1, 0, 0, 0, 1, 1 (23H)	"R"	"R"

8. 5. 1 Block Stasus Register

This field provides lock configuration and erase status for the specified block. These infomations are only available when device is ready (SR.7=1). If block erase or full chip erase operation is finished irregulary, block erase status bit will be set to "1". If bit 1 is "1", this block is invalid. This card is not support Block lock configuration.

Table 5. Query Block Status Register

Offset (Word Address)	Length	Description
(BA+2)H	01H	Block Status Register bit0 Block Lock Configuration 0 = Block is unlocked 1 = Block is Locked bit1 Block Erase Status 0 = Last erase operation completed successfully 1 = Last erase operation not completed successfully bit2-7 reserved for future use

Note:

1. BA = The beginning of a Block Address.

8. 5. 2 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. Additionally, it indicates which version of the spec and which Vendor-specified command set(s) is (are) supported.

Table 6. CFI Query Identification String

Offset (Word Address)	Length	Description
10H, 11H, 12H	03H	Query Unique ASCII string "QRY" 51H, 52H, 59H
13H, 14H	02H	Primary Vendor Command Set and Control Interface ID Code 01H, 00H (SCS ID Code)
15H, 16H	02H	Address for Primary Algorithm Extended Query Table 31H, 00H (SCS Extended Query Table Offset)
17H, 18H	02H	Alternate Vendor Command Set and Control Interface ID Code 0000H (0000H means that no alternate exists)
19H, 1AH	02H	Address for Alternate Algorithm Extended Query Table 0000H (0000H means that no alternate exists)

8. 5. 3 System Interface Information

The following device information can be useful in optimizng system interface software.

Table 7. System Information String

Offset (Word Address)	Length	Description
1BH	01H	V_{CC} Logic Supply Minimum Write/Erase voltage 27H (2.7V)
1CH	01H	V_{CC} Logic Supply Maximum Write/Erase voltage 55H (5.5V)
1DH	01H	V_{PP} Programming Supply Minimum Write/Erase voltage 27H (2.7V)
1EH	01H	V_{PP} Programming Supply Maximum Write/Erase voltage 55H (5.5V)
1FH	01H	Typical Timeout per Single Byte/Word Write 03H ($2^3 = 8$ µs), 2^N µs
20H	01H	Typical Timeout for Maximum Size Buffer Write (32 Bytes) 06H ($2^6 = 64$ µs)
21H	01H	Typical Timeout per Individual Block Erase 0AH (0AH = 10, $2^{10} = 1024$ms)
22H	01H	Typical Timeout for Bank Erase 0FH (0FH = 15, $2^{15} = 32768$ms)
23H	01H	Maximum Timeout per Single Byte/Word Write, 2^N times of typical. 04H ($2^4 = 16$, 8 µs × 16 = 128 µs)
24H	01H	Maximum Timeout Maximum Size Buffer Write, 2^N times of typical. 04H ($2^4 = 16$, 64 µs × 16 = 1024 µs)
25H	01H	Maximum Timeout per Individual Block Erase, 2^N times of typical. 04H ($2^4 = 16$, 1024ms × 16 = 16384ms)
26H	01H	Maximum Timeout For Bank Erase, 2^N times of typical. 04H ($2^4 = 16$, 32768ms × 16 = 524288ms)

8. 5. 4 Device Geometry Definition

This field provides critical details of the flash device geometry.

Table 8. Device Geometry Definition

Offset (Word Address)	Length	Description
27H	01H	Device Size 15H (15H = 21, $2^{21} = 2097152 = 2$M Bytes)
28H, 29H	02H	Flash Device Interface description 02H, 00H (×8/×16 supports ×8 and ×16 via BYTE#)
2AH, 2BH	02H	Maximum Number of Bytes in Multi-byte 05H, 00H ($2^5 = 32$ Bytes)
2CH	02H	Number of Erase Block Regions within device 01H (symmetrically blocked)
2DH, 2EH	02H	The Number of Erase Blocks 1FH, 00H (1FH = 31 ==> 31 + 1 = 32 Blocks)
2FH, 30H	02H	The Number of "256 Bytes" cluster in a Erase block 00H, 01H (0100H = 256 ==> 256 Bytes × 256 = 64K Bytes in a Erase Block)

8. 5. 5 SCS OEM Specific Extended Query Table

Certain flash features and commands may be optional in a vendor-specific algorithm specification. The optional vendor-specific Query table(s) may be used to specify this and other types of information. These structures are defind solely by the flash vendor(s).

Table 9. SCS OEM Specific Extended Query Table

Offset (Word Address)	Length	Description
31H, 32H, 33H	03H	PRI 50H, 52H, 49H
34H	01H	31H (1) Major Version Number, ASCII
35H	01H	30H (0) Minor Version Number, ASCII
36H, 37H, 38H, 39H	04H	0FH, 00H, 00H, 00H Optional Command Support bit0 = 1 : Chip Erase Supported bit1 = 1 : Suspend Erase Supported bit2 = 1 : Suspend Write Supported bit3 = 1 : Lock/Unlock Supported* bit4 = 0 : Queued Erase Not Supported bit5-31 = 0 : reserved for future use *This card is not support block lock configuration.
3AH	01H	01H Supported Functions after Suspend bit0 = 1 : Write Supported after Erase Suspend bit1-7 = 0 : reserved for future use
3BH, 3CH	02H	03H, 00H Block Status Register Mask bit0 = 1 : Block Status Register Lock Bit [BSR.0] active bit1 = 0 : Block Status Register Valid Bit [BSR.1] active bit2-15 = 0 : reserved for future use
3DH	01H	V_{CC} Logic Supply Optimum Write/Erase voltage (highest performance) 50H (5.0V)
3EH	01H	V_{PP} Programming Supply Optimum Write/Erase voltage (highest performance) 50H (5.0V)
3FH	reserved	Reserved for future versions of the SCS Specification

8. 6 Block Erase Command

The host executes an erase command one block at a time using a two-cycle command. The host writes a block erase setup command first, followed by a block erase confirm command. These two commands require appropriate sequencing and an address within the block to complete (erase changes all block data to FFH). The WSM handles block preconditioning, erase, and verify internally (invisible to the system). After the host writes the two-cycle block erase sequence, the device automatically outputs status register data when read. The CPU can detect block erase completion by analyzing the output data of the BUSY# signal or status register bit SR.7.

When the block erase completes, status register bit SR.5 should be checked. If a block erase error is detected, the host should clear the status register before system software attempts corrective actions. The CUI remains in read status register mode until the host issues a new command.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in the WSM setting status register bits SR.4 and SR.5 to "1".

8. 7 Full Chip Erase Command

This command followed by a confirm command(D0D0H) erases all of the unlocked blocks. A full chip erase setup is first written, followed by a full chip erase confirm. After a confirm command is written, device erases the all unlocked blocks from Block 0 to Block 31 block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM(invisible to the system). After the two-cycle full chip erase sequence is written, the device automatically outputs status register data when read. The CPU can detect full chip erase completion by analyzing the output data of the BUSY# pin or status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issured. If error is detected on a block during full chip erase operation, WSM stops erasing. Reading the block valid status by issuing Read ID Codes command or Query command informs which blocks failed to its erase.

8. 8 Word/Byte Write Command

The host executes a word/byte write by a two-cycle command sequence. The host writes word/byte write setup (standard 4040H or alternate 1010H) first, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the host writes the word/byte write sequence, the device automatically output status register data when read. The CPU can detect the completion of the word/byte write event by analyzing the BUSY# pin or status register bit SR.7.

When the WSM completes the word/byte writes, the host should check status register bit SR.4. If the host detects a write error, it should clear the status register. The internal WSM verify only detects errors for "1"s that do not successfully writes to "0"s. The CUI remains in read status register mode until it receives another command.

8. 9 Multi Word/Byte Write Command

Multi word/byte write is executed by at least four-cycle or up to 35-cycle command sequence. Up to 32 bytes can be loaded into the buffer and written to Flash Array. First, multi word/byte write setup (E8H) is written with the write address. At this point, the device automatically outputs extended status register data (XSR) when read. If extended status register bit XSR.7 is 0, no Multi Word/Byte Write command is available and multi word/byte write setup which just has been written is ignored. To retry, continue monitoring XSR.7 by writing multi word/byte write setup with write address until XSR.7 transitions to 1. When XSR.7 transitions to 1, the device is ready for loading the data to the buffer. A word/byte count (N)-1 is written with write address. After writing a word/byte count (N)-1 must be less than or equal to 1FH. On the next write, device start address is written with buffer data. Subsequent writes provide additional device address and data, depending on the count. All subsequent address must lie within the start address plus the count. After the final buffer data is written, write confirm (D0H) must be written. This initiates WSM to begin copying the buffer data to the Flash Array. An invalid Multi Word/Byte Write command sequence will result in both status register bits SR.4 and SR.5 being set to "1". For additional multi word/byte write, write another multi word/byte write setup and check XSR.7. The Multi Word/Byte Write command can be queued while WSM is busy as long as XSR.7 indicates "1", because LH320S5B has two buffers. If an error occurs while writing, the device will stop writing and flash next mult word/byte write command. Status register bit SR.4 will be set to "1". No multi word/byte write command. Status register bit SR.4 will be set to "1". No multi word/byte write command is available if either SR.4 or SR.5 are set to "1". SR.4 and SR.5 should be cleared before issuing multi word/byte write command. If a muti word/byte write command is attempted past an erase block boundary, the device will write the data to Flash Array up to an erase block boundary and then stop writing. Status register bits SR.4 and SR.5 will be set to "1".

8. 10 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. After the host writes the Block Erase Suspend command, the host should then write the Read Status Register command. Polling status register bits SR.7 and SR.6 can determine when the WSM suspends the block erase operation (both will be set to "1"). BUSY# will also transition to V_{OH} Specification t_{WHRH2} defines the block erase suspend latency. It is also possible that the block erase completes before the device has an opportunity to suspend. The host should also check for this condition.

After the block erase has been suspended, the host can issue a read array command or a word write command to any block except the one that has been suspended. Using the Word Write Suspend command (see Section 8.11), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to "0" and the BUSY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status. The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After the host writes a Block Erase Resume command to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and BUSY# will return to V_{OL}. After the host writes the Erase Resume command, the device automatically outputs status register data when read. Block erase cannot resume until word write operation initiated during block erase suspend have completed.

8. 11 (Multi)Word/Byte Write Suspend Command

The (Multi)Word/Byte Write Suspend command allows (multi)word/byte write interruption to read data in other flash memory locations. Once the (multi)word/byte write process starts, writing the (Multi)Word/Byte Write Suspend command requests that the WSM suspend the (multi)word/byte write sequence at a predetermined point in the algorithm. After the host writes the (Multi)Word/Byte Write Suspend command, it should write the Read Status Register command. Polling status register bits SR.7 and SR.2 can determine when the WSM suspends the (multi)word/byte write operation (both will be set to "1"). BUSY# will also transition to V_{OH}. Specification t_{WHRH1} defines the (multi)word/byte write suspend latency. It is also possible that the (multi)word/byte write completes before the device has an opportunity to suspend. The host should also check for this condition.

After the (multi)word/byte write has been suspended, the host can write the Read Array command to read data from any location except the suspended location. The only other valid commands while (multi)word/byte write is suspended are Read Status Register and (Multi)Word/Byte Write Resume. After the host writes a (Multi)Word/Byte Write Resume to the CUI, the WSM will continue the (multi)word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and BUSY# will return to V_{OL}. After the host writes the (Multi)Word/Byte Write Resume command, the device automatically outputs status register data when read.

8.12 Status Register

The memory devices in this card have Status Register which shows state of the device.

Byte Access × 8 Bits

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SR. 7	SR. 6	SR. 5	SR. 4	SR. 3	SR. 2	SR. 1	SR. 0
WSMS	BESS	ECBLBS	WSBLBS	VPPS	WSS	DPS	R

Table 10. Status Register Definition

SR. 7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR. 6 = BLOCK ERASE SUSPEND STATUS
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR. 5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS
1 = Error in Erase or Clear Block Lock-Bits
0 = Successful Erase or Clear Block Lock-Bits

SR. 4 = WRITE AND SET BLOCK-BIT STATUS
1 = Error in Write or Set Block Lock-Bit
0 = Successful Write or Set Block Lock-Bit

SR. 3 = V_{PP} STATUS
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

SR. 2 = WRITE SUSPEND STATUS
1 = Write Suspended
0 = Write in Progress/Completed

SR. 1 = DEVICE PROTECT STATUS
1 = Block Lock-Bit and/or WP# Lock Detected,Operation Abort
0 = Unlock

SR. 0 = RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

Check SR.7 to determine block erase, full chip erase, (multi) word/byte write or block lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (multi) word/byte write, block lock-bit configuration or STS configuration attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when V_{PP} 3.3V± 0.3V

SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates the block lock-bit, and WP# only after Block Erase, full chip erase, (multi) Word/Byte Write, or Block Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set and/or WP# is not V_{IH}. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock-bit status.

This card is not support block lock configuration.

SR.0 is reserved for future use and should be masked out when polling the status register.

Table 11. Extended Status Register Definition

XSR.7	XSR.6	XSR.5	XSR.4	XSR.3	XSR.2	XSR.1	XSR.0
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.7 = STATE MACHINE STATUS 1 = Multi Word/Byte Write available 2 = Multi Word/Byte Write not available XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS	NOTES: After issue a Multi Word/Byte Write command: XSR.7 indicates that a next Multi Word/Byte Write command is available. XSR.6-0 is reserved for future use and should be masked out when polling the extended status register.

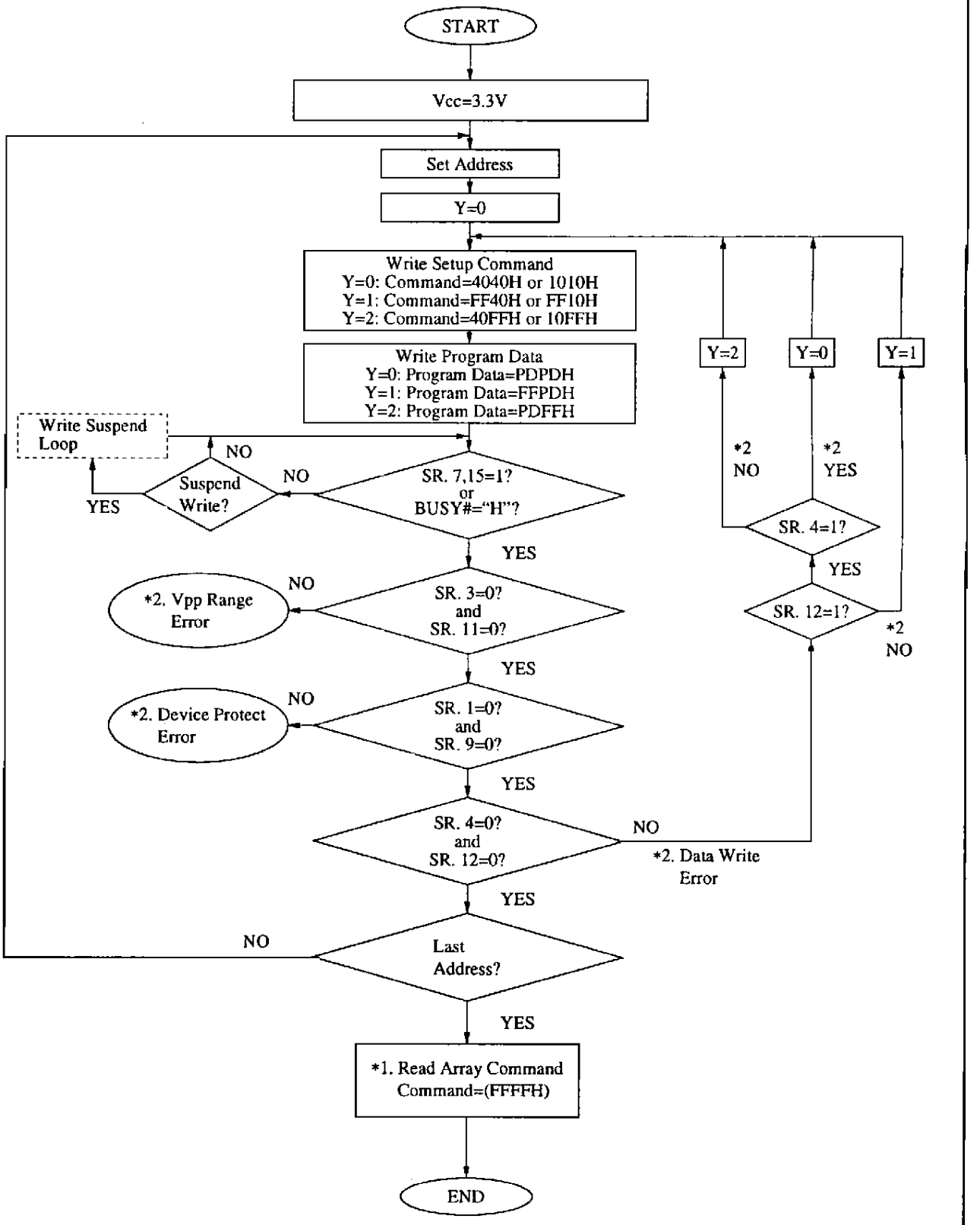
Word Access × 16 Bits

bit15 bit8 bit7 bit0

SR.15	SR.14	SR.13	SR.12	SR.11	SR.10	SR.9	SR.8	SR.7	SR.6	SR.5	SR.4	SR.3	SR.2	SR.1	SR.0
XSR.15	XSR.14	XSR.13	XSR.12	XSR.11	XSR.10	XSR.9	XSR.8	XSR.7	XSR.6	XSR.5	XSR.4	XSR.3	XSR.2	XSR.1	XSR.0

High Byte device Low Byte device

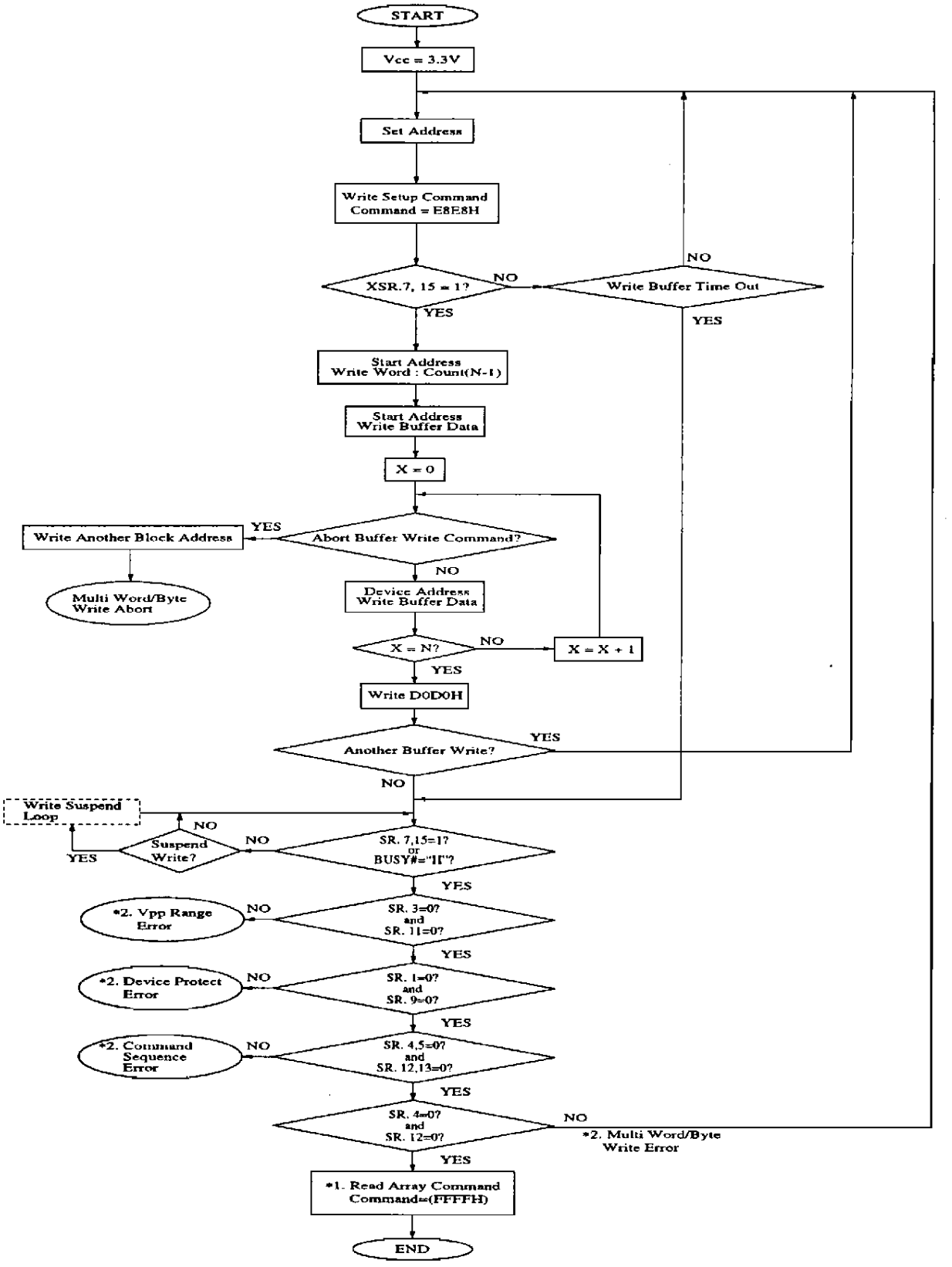
8.13 Automated Word/Byte Write Flowchart



Note) *1. Write FFFFH after the last word write operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

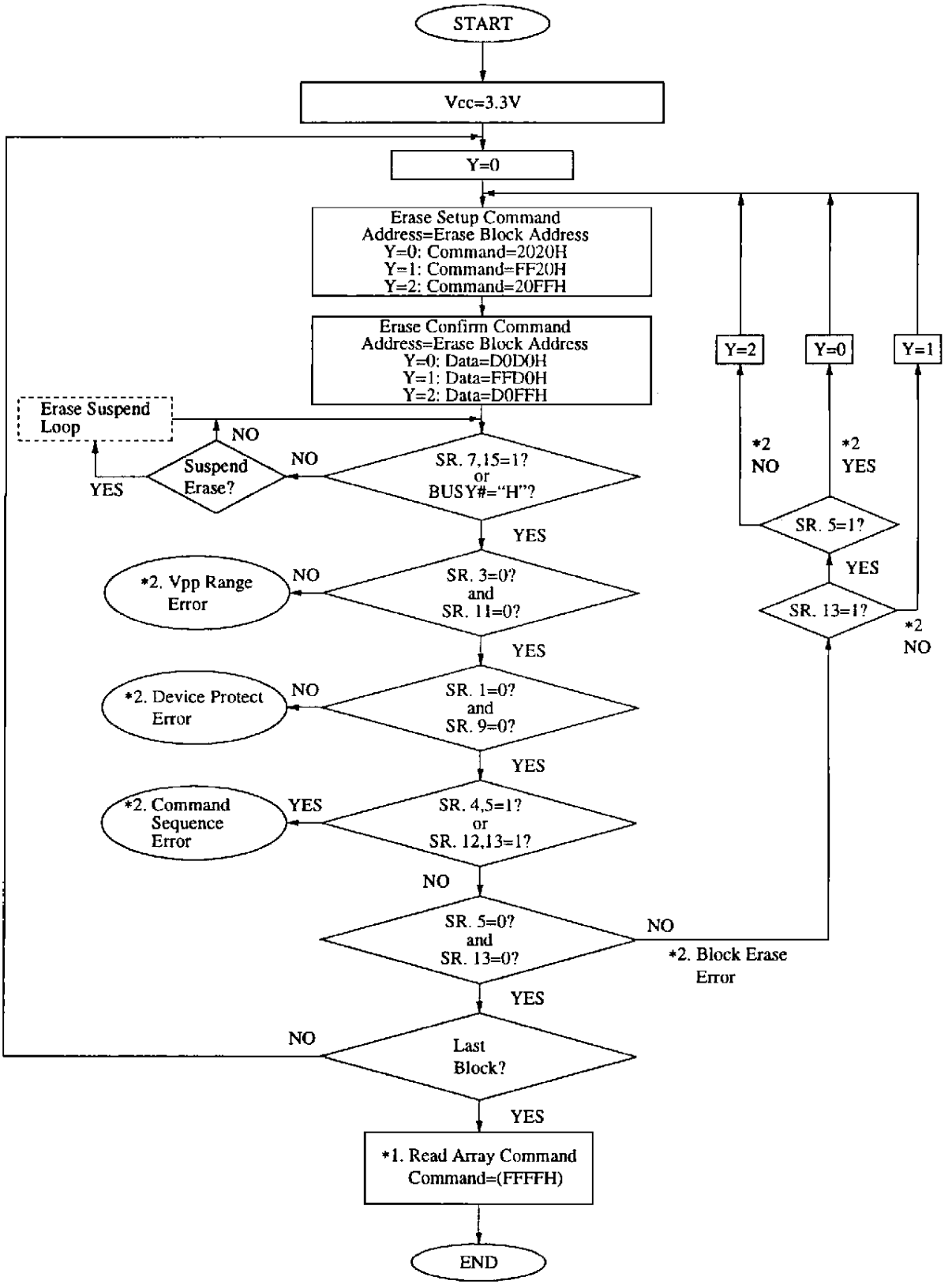
8.14 Multi Word/Byte Write Flowchart



Note) *1. Write FFH after the last word write operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

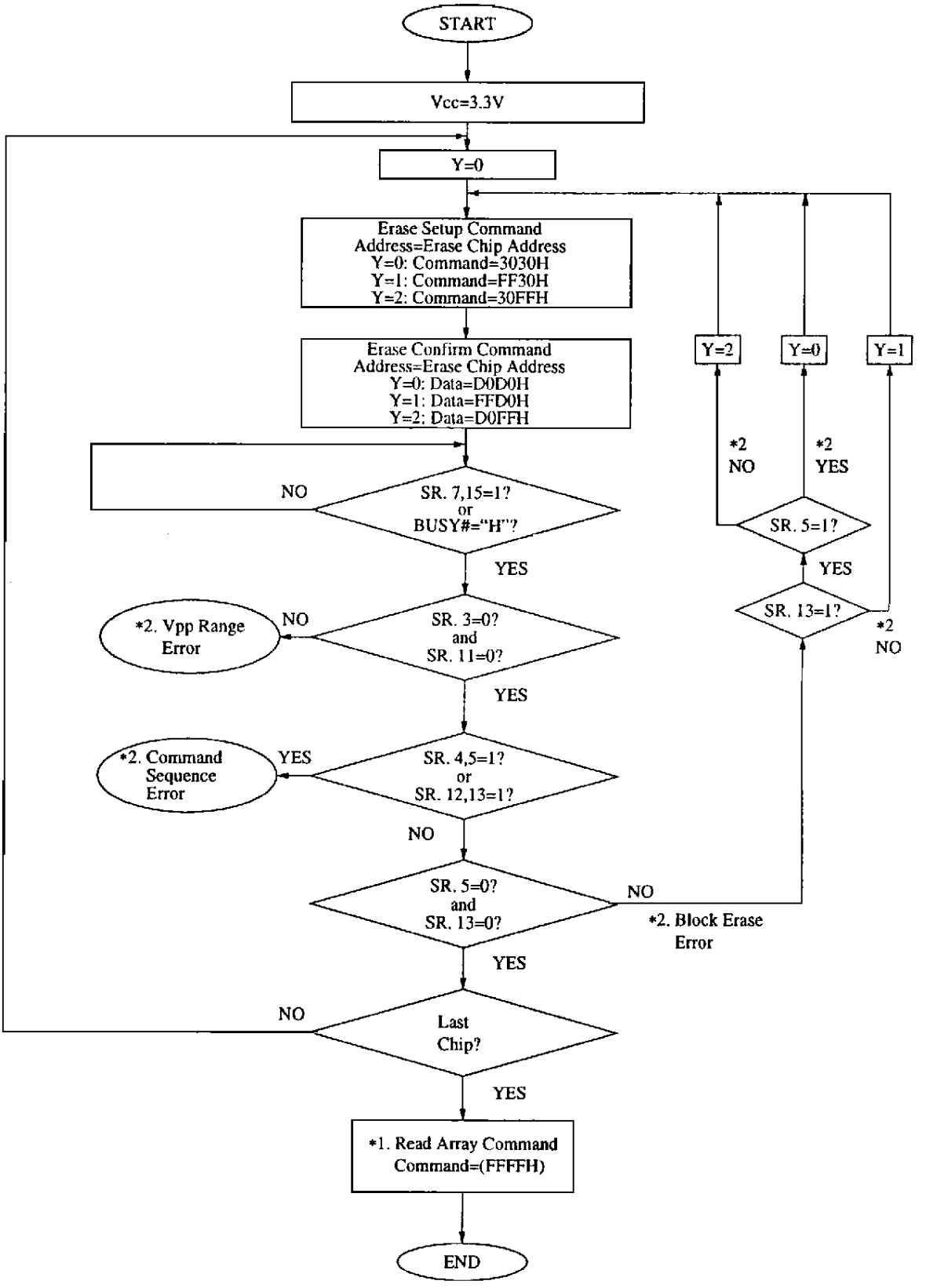
8.15 Automated Block Erase Flowchart



\Note) *1. Write FFFFH after the last block erase operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

8.16 Automated Full Chip Erase Flowchart



Note) *1. Write FFH after the last block erase operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

9. Electrical Specifications

9. 1 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage (2)	V_{CC}	-0.2 to 7.0	V
Input Voltage (2)	V_{IN}	-0.5 to V_{CC} + 0.5 (Max: 7.0)	V
Output Short Circuit Current (3)	I_{OUT}	100	mA
Operating Temperature (1)	T_{OPR}	0 to 60	°C
Storage Temperature	T_{STG}	-30 to 70	°C

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND.
3. Output shorted for no more than one second. No more than one output shorted at a time.

9. 2 Recommended Operating Conditions

PARAMETER	SYMBOL	MINIMUM	MAXMUM	UNIT
Operating Temperature	T_{OPR}	0	60	°C
Supply Voltage	V_{CC}	3.0	3.6	V

9. 3 Capacitance

Ta = 25°C, f = 1MHz

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Capacitance	C_{IN}	—	56	80	pF	V_{IN} = 0.0V
Input/Output Capacitance	C_{IO}	—	36	48	pF	V_{OUT} = 0.0V

9. 4 AC Input/Output Test Conditions

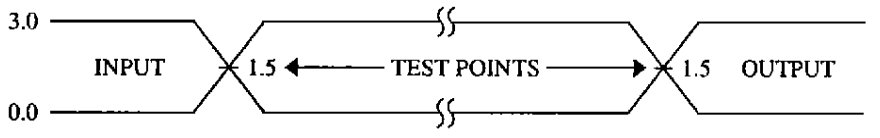


Figure 4.Transient Input/Output Reference Waveform for V_{CC} = 3.3V ± 0.3V
(Standard Testing Configuration)

AC test inputs are driven at 3.0V for a Logic " 1 " and 0.0V for a Logic " 0 ". Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10ns.

10. DC Characteristics

(Ta = 0~60°C)

PARAMETER	SYMBOL	NOTES	V_{CC} = 3.3V		UNIT	TEST CONDITIONS
			MIN	MAX		
Input Leakage Current (A0–A20)	I_{LI1}	1	—	±5	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
Input Leakage Current (A21,22)	I_{LI2}	1	–2	41	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
Input Leakage Current (CEL#,CEH#)	I_{LI3}	1	–40	2	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
Input Leakage Current (OE#,WE#)	I_{LI4}	1	–42	4	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
Input Leakage Current (RESET#)	I_{LI4}	1	-40	1	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
Output Leakage Current (D0–D15)	I_{LO}	1	—	±2	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
V_{CC} Standby Current	I_{CCS}	1, 3	—	990	μA	V_{CC} = V_{CC} Max, CEL# ,CEH# = V_{CC} ± 0.2V, RESET# = V_{CC} ± 0.2V
V_{CC} Deep Power-Down Current	I_{CCD}	1, 3	—	230	μA	RESET# = GND ± 0.2V, I_{OUT} (BUSY#)=0 mA
V_{CC} Read Current	I_{CCR}	1, 3, 4, 5	—	60	mA	V_{CC} = V_{CC} Max, CEL#,CEH#= GND±0.2V, t_{cycle} =100ns, I_{OUT} =0 mA
V_{CC} Word Write Current	I_{CCW}	1, 5	—	202	mA	
V_{CC} Block Erase Current	I_{CCE}	1, 5	—	122	mA	
V_{CC} Word Write or Block Erase Suspend Current	I_{CCWS} I_{CCES}	1, 2, 5	—	9	mA	CEL# = CEH# = V_{IH}

PARAMETER	SYMBOL	NOTES	V_{CC} = 3.3V		UNIT	TEST CONDITIONS
			MIN	MAX		
Input Low Voltage	V_{IL}	—	–0.5	0.8	V	
Input High Voltage	V_{IH}	—	0.7 V_{CC}	V_{CC}+0.5	V	
Output Low Voltage	V_{OL}	—	—	0.1V_{CC}	V	V_{CC}= V_{CC} Min, I_{OL}= 2mA
Output High Voltage	V_{OH}	—	0.9V_{CC}	—	V	V_{CC} = V_{CC} Min I_{OH} = –100μA
V_{CC} Lockout Voltage	V_{LKO}	—	2.0	—	V	

NOTES:

1. All currents are in RMS unless otherwise noted.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V.
4. Automatic Power Savings (APS) reduces typical I_{CCR} to 3mA at 3.3V V_{CC} in static operation (addresses not switching).
5. All values are based on word accesses. Values for byte accesses are 50% of the specification listed.

11. AC Characteristics (Ta = 0~60°C)

Testing Conditions :

1) Input Pulse Level : 0.0V~3.0V
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 1.5V
4) Output Load : 30pF (including scope and jig capacitance)

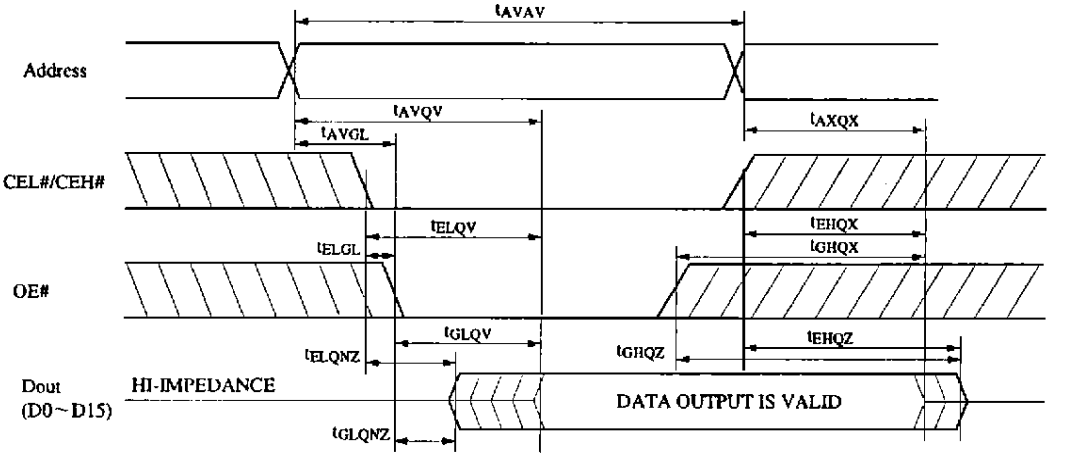
11. 1 Read Operations

(Ta = 0 ~ 60℃)

PARAMETER	SYMBOL	V_{CC} = 3.3V		UNIT
	IEEE	MIN	MAX	
Read Cycle Time	t_{AVAV}	150	—	ns
Address Access Time	t_{AVQV}	—	150	
Card Enable Access Time	t_{ELQV}	—	150	
Output Enable Access Time	t_{GLQV}	—	50	
Output Disable Time from CEL#/CEH#*	t_{EHQZ}	—	20	
Output Disable Time from OE#*	t_{GHQZ}	—	20	
Output Enable Time from CEL#/CEH#	t_{ELQNZ}	5	—	
Output Enable Time from OE#	t_{GLQNZ}	5	—	
Data Hold from Address	t_{AXQX}	0	—	
Data Hold from CEL#/CEH#	t_{EHQX}	0	—	
Data Hold from OE#	t_{GHQX}	0	—	
CE# Setup Time to OE# Active	t_{ELGL}	0	—	
Address Setup Time to OE# Active	t_{AVGL}	0	—	
Power-Down Recovery to Output Delay	t_{PHQV}	—	600	

* Time until output becomes floating. (The output voltage is not defined.)

11. 2 AC Waveforms for Read Operations



Note) 1. WE# = "HIGH", during a read cycle.

2. Either "HIGH" or "LOW" in diagonal areas.

3. The output data becomes valid when last interval, t_{AXQV}, t_{ELQV} or t_{GLQV} have concluded.

11.3 Write Operations

11.3.1 WE# Controlled Write Operations

(Ta = 0~60°C)

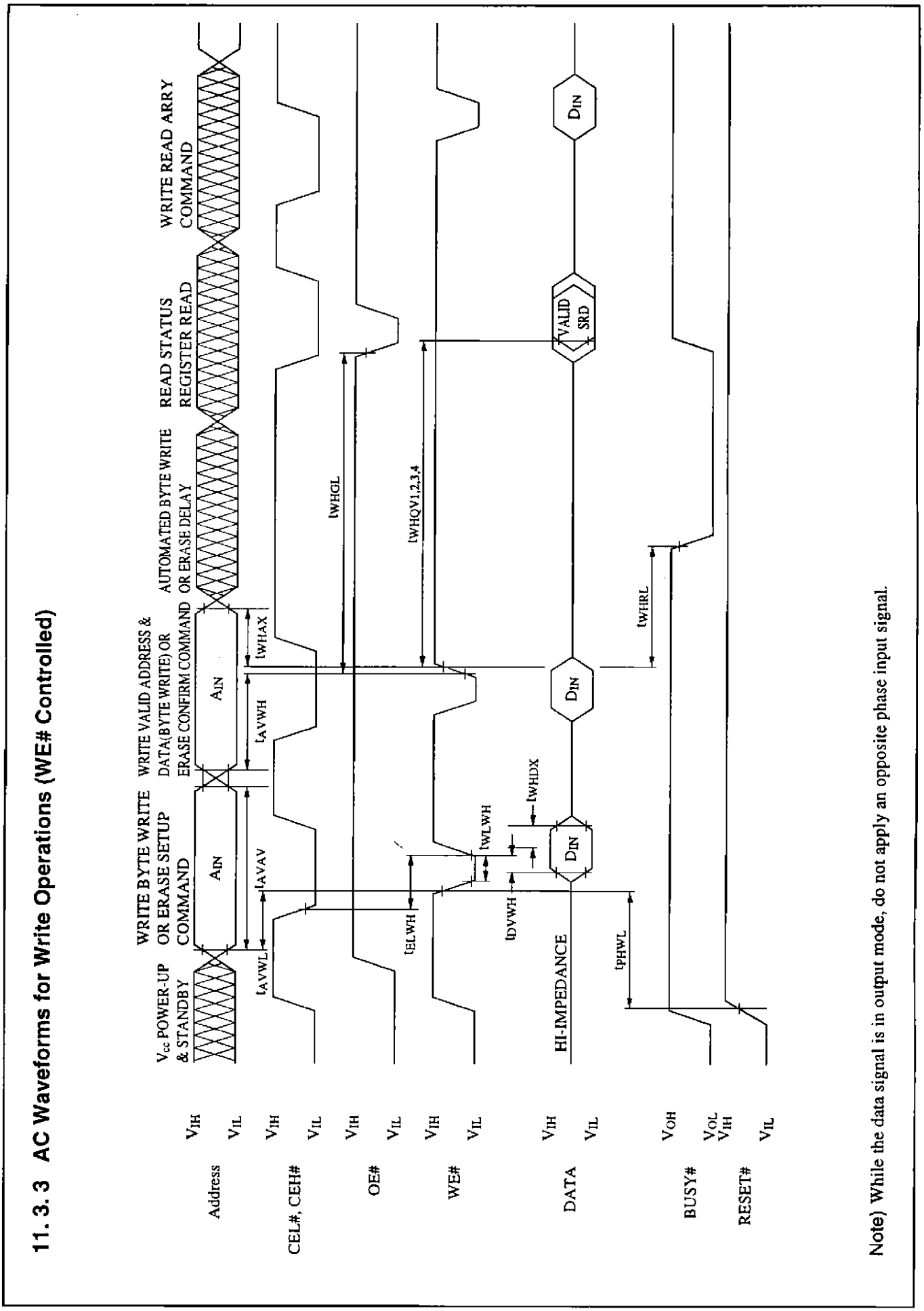
PARAMETER	SYMBOL	V_{CC} = 3.3V		UNIT
	IEEE	MIN	MAX	
Write Cycle Time	t_{AVAV}	150	—	ns
Address Setup Time	t_{AVWL}	20		
Write Recovery Time	t_{WHAX}	5	—	
Data Setup Time for WE#	t_{DVWH}	50	—	
Data Hold Time	t_{WHDX}	20	—	
Output Enable Hold from WE#	t_{WHGL}	10	—	
Card Enable Setup time for WE#	t_{ELWH}	100		
Address Setup for WE#	t_{AVWH}	100	—	
Write Pulse Width	t_{WLWH}	80	—	
WE# High to RDY/BSY# Going Low	t_{WHRL}	—	300	
Power-Down Recovery to WE# Going Low	t_{PHWL}	1	—	μs

11.3.2 CE# Controlled Write Operations

(Ta = 0~60°C)

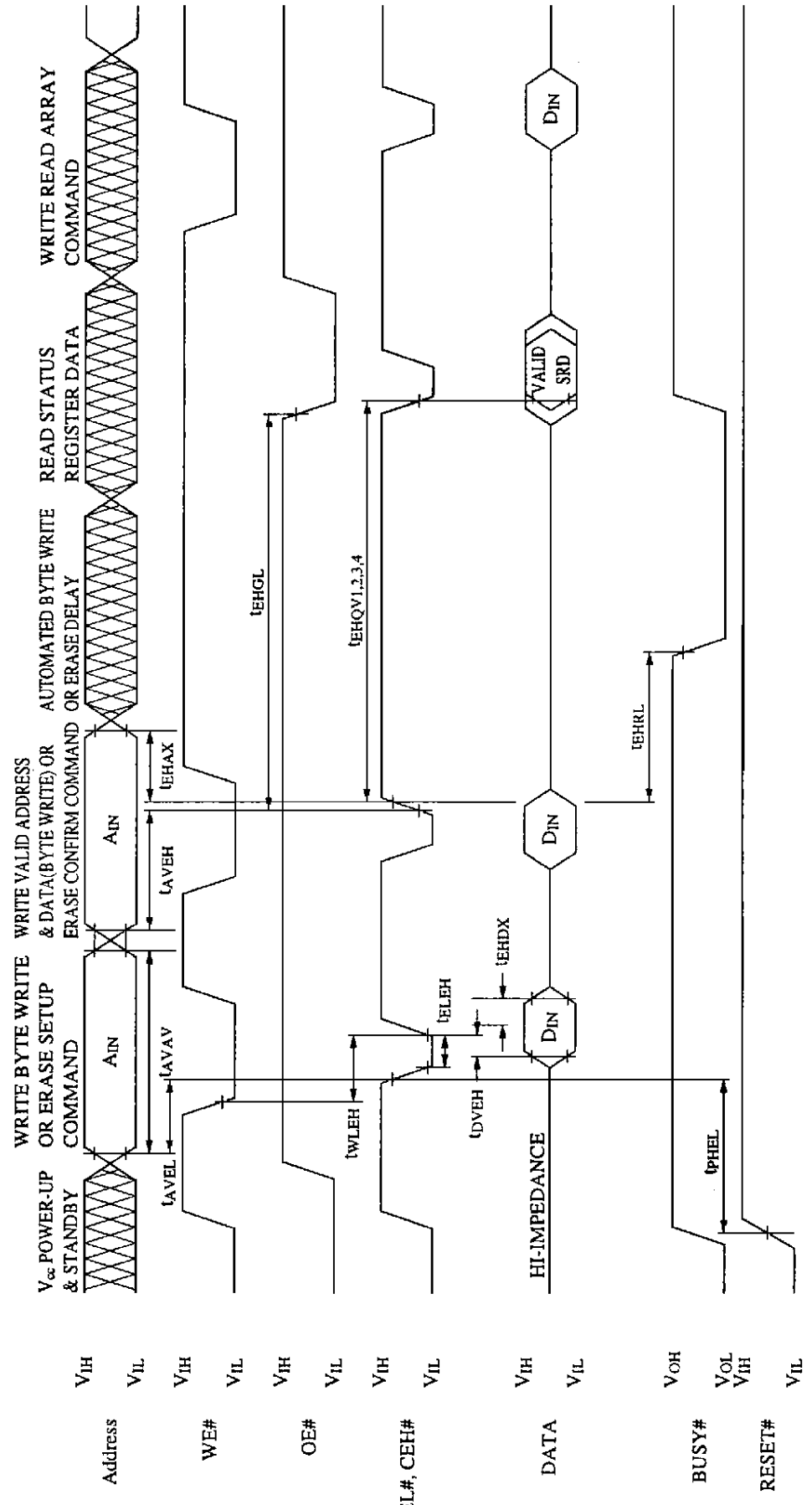
PARAMETER	SYMBOL	V_{CC} = 3.3V		UNIT
	IEEE	MIN	MAX	
Write Cycle Time	t_{AVAV}	150	—	ns
Address Setup Time	t_{AVEL}	20		
Write Recovery Time	t_{EHAX}	5	—	
Data Setup Time for CE#	t_{DVEH}	50	—	
Data Hold Time	t_{EHDX}	20	—	
Output Enable Hold from CE#	t_{EHGL}	10	—	
Write Enable Setup time for CE#	t_{WLEH}	100		
Address Setup for CE#	t_{AVEH}	100	—	
Card Enable Pulse Width	t_{ELEH}	80	—	
CE# High to RDY/BSY# Going Low	t_{EHRL}	—	300	
Power-Down Recovery to CE# Going Low	t_{PHEL}	1	—	μs

11. 3. 3 AC Waveforms for Write Operations (WE# Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase input signal.

11. 3. 4 AC Waveforms for Write Operations (CE# Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase input signal.

11. 4 Erase and Data Write Performance(3)

(Ta = 0~60°C)

PARAMETER	SYMBOL	NOTES	V_{CC} = 3.3V			UNIT
			MIN	TYP(1)	MAX	
Byte Write Time	t_{WHQV1} t_{EHQV1}	2	—	19.51	—	µs
Block Write Time		2	—	1.28	16.5	s
Multi Word/Byte Write Time			—	5.66	—	µs
Block Erase Time	t_{WHQV2} t_{EHQV2}	2	—	0.55	10	s
Full Chip Erase Time			—	17.6	—	s
Byte Write Suspend Latency Time to Read	t_{WHRH1} t_{EHRH1}	—	—	7.1	10	µs
Erase Suspend Latency Time to Read	t_{WHRH2} t_{EHRH2}	—	—	15.2	21.1	µs

NOTES:

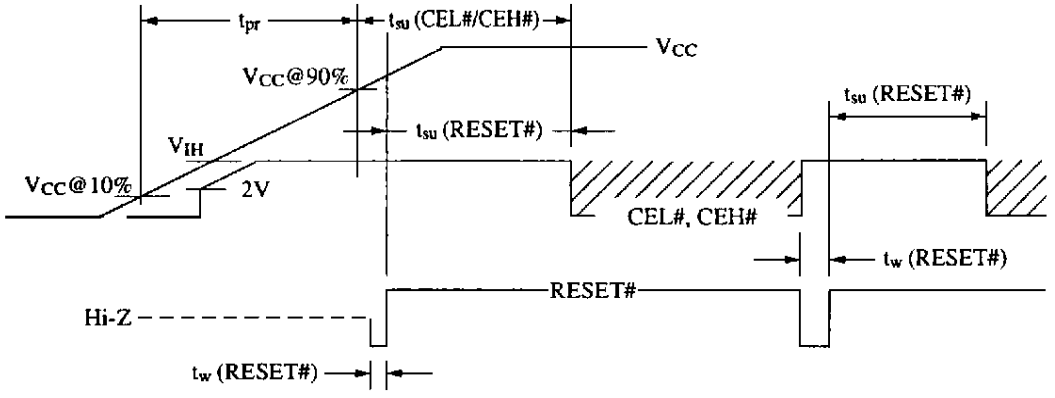
1. Typical values measured at Ta = 25°C and norminal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.

11.5 Power-Up

PARAMETER	SYMBOL	NOTES	MIN	MAX	UNITS
CE# Setup Time	t_{su} (CEL# /CEH#)	—	1	—	ms
RESET# Setup Time	t_{su} (RESET#)	—	1	—	ms
V_{CC} Rising Time	t_{pr}	1	0.1	100	ms
RESET# Width	t_w (RESET#)	—	1	—	μs

NOTES:

1. The t_{pr} is defined as "linear waveform" in the period of 10% to 90%. Even if the waveform is not a "liner waveform," its rising time must meet this specification.



Power-Up Timing for Systems Supporting RESET#

12. Specification Changes

Specifications may be changed upon discussion and agreement between both parties.

13. Other Precautions

- Permanent damage occures if the Miniature card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommeded Operating Conditions may affect device reliability.
- Writing to the Miniature card can be prevented by switching on the write protect switch on the side of the Miniature card.
- Avoid allowing the Miniature card Pads to come in contact with metals and avoid touching the Pads, as the internal circuits can be damaged by static electricity.
- Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
- Avoid subjecting the Miniature card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
- When the Miniature card is not being used, return it to its protective case.
- Do not allow the Miniature card to come in contact with fire.

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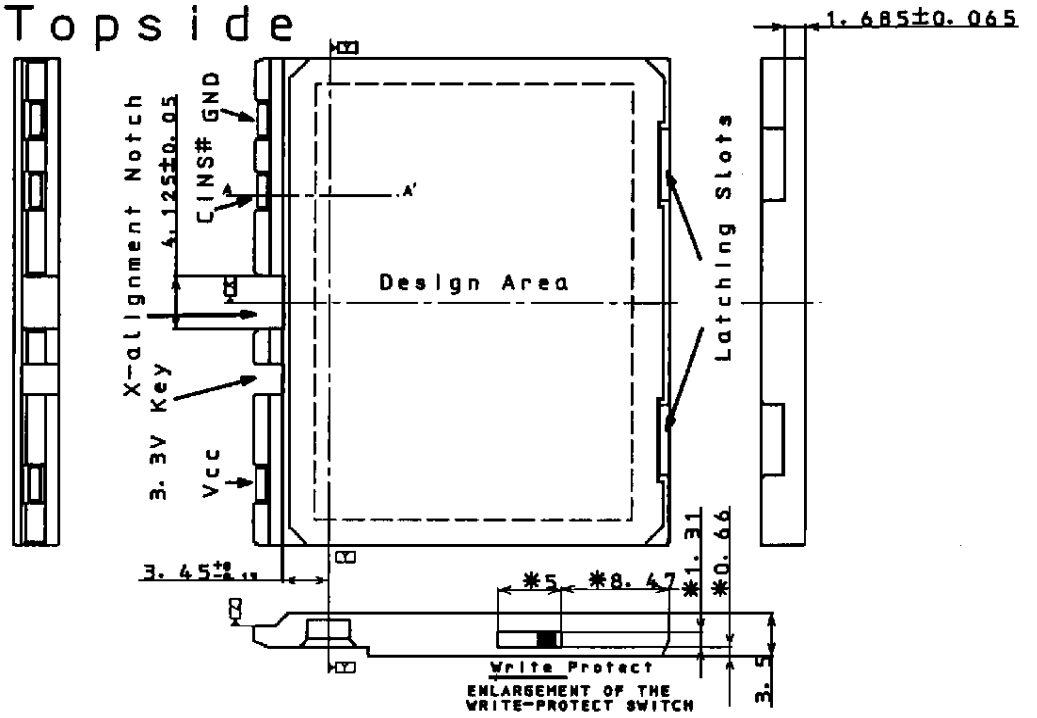
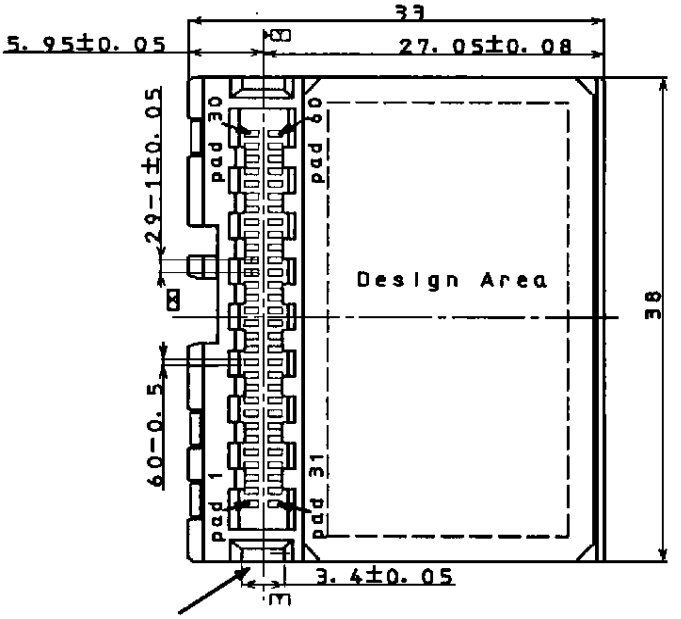
14. External Dimensions

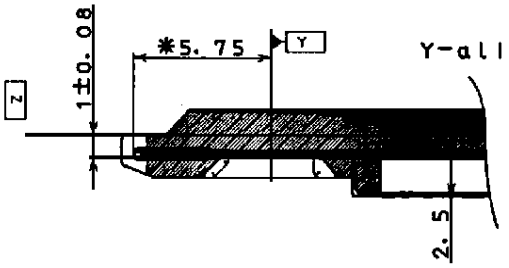
Topside



Bottomside



SECTION A-A'

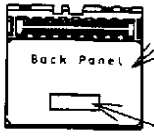


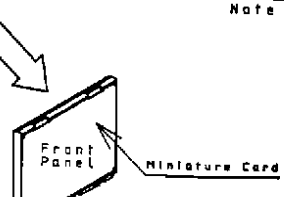
APPPLICABLE		SCALE	UNIT				
			mm	CH. DATE	REVISE	CHARGE	
THICKNESS	TOLERANCES	MATERIAL	FINISH	NAME	Miniature Card External Dimensions 3.3Voltage-key		
	DECIMALS .XX =±0.13 *X.XX=±0.25				Miniature Card Release 1.1		
DATE	1998.10.28						
DESIGN/DRAW	CHECK	APPROVE	IMAGE DEVICE ENGINEERING DEPT. 2	DRAWING NO.	IMC248-A300		
H. Tanaka		H. Tanaka	INTEGRATED CIRCUITS GROUP				
			SHARP CORPORATION				

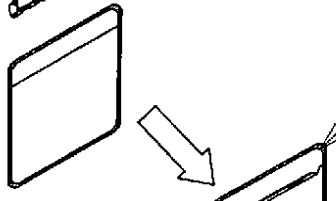
SHARP

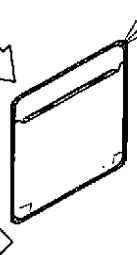
15. Packing Specification

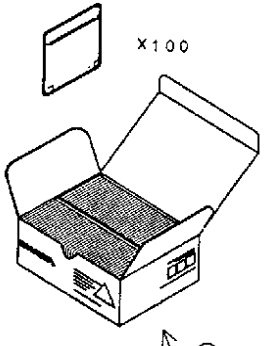
Bottom side

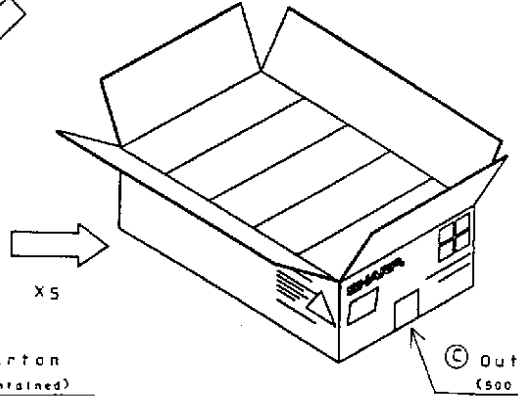


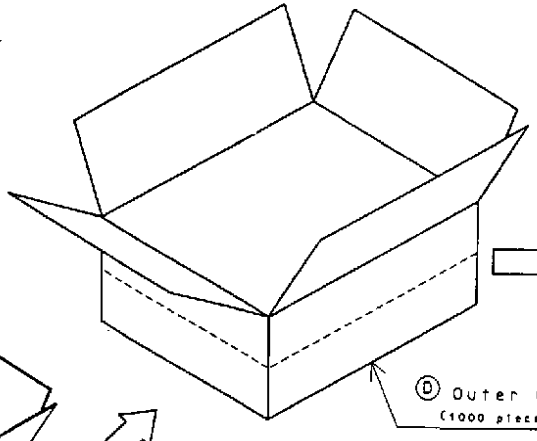


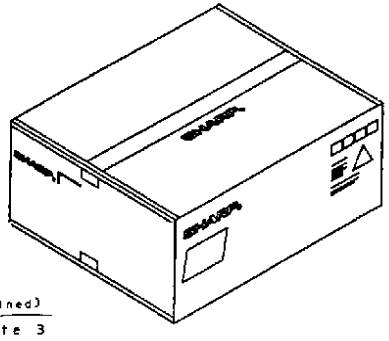












Parts List

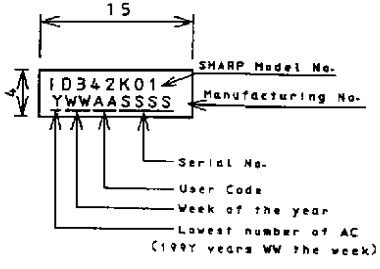
	Parts Name
A	Flexible Plastic Bag
B	Inner Carton (100 pieces contained)
C	Outer Carton (500 pieces contained)
D	Outer Case (1000 pieces contained)

Packing Specification

1. Label on which the Model No. and Manufacturing No. are printed is attached on the back panel of the card.
2. Each Miniature Card is contained in the Flexible plastic bag. (The terminals of the card come to opposite side of the place where the card is released from the bag, so that the terminals are not touched by finger, as shown in the figure.)
3. The inner carton contains 100 pieces of the card. (Note 1.)
4. The product name, Lot no. (product no.), quantity and the date are either written directly on the inner carton, or printed on the label which is attached on inner carton.
5. The outer carton contains 5 inner cartons. (Note 2.)
6. The product name, Lot no. (product no.), quantity and the date are either written directly on the outer carton, or printed on the label which is attached on the outer carton.
7. The outer carton is put into the outer case, which contains 2 outer cartons. (Note 3.)
8. The product name, Lot no. (product no.), quantity and the date are either written directly on the case or printed on the label which is attached on the case.

Note 1. The least packing unit is 100 pieces, which is the number contained in the inner carton.

2. The inner space of the outer carton is filled with card boards.
3. Other size of outer case may be used if there is not enough quantity to fill the normal outer case which can contain 2 outer cartons.
4. The size and descriptions of the label on the back panel of the card are follows. [unit:mm]



APPLICABLE MODEL	ID342K01	SCALE	UNIT mm
THICKNESS	DEFFERENCE	MATERIAL	FINISH
DATE	1999. 4. 12	Image Device Engineering Dept. I, INTEGRATED CIRCUITS GROUP, SHARP CORPORATION	

CH. DATE	REVISE	CHARGE
NAME	ID342K01 Packing Specification	
DRAWING NO.	IMC248-J300	

Miniature Flash Card, PCMCIA, 16 MByte, ID342K01