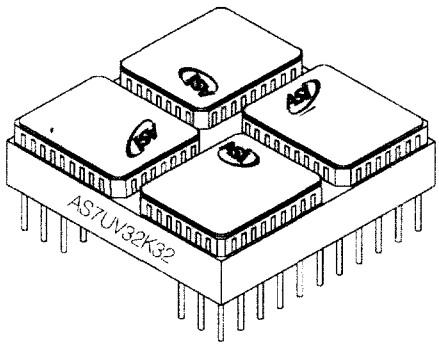
UVEPROM MODULE

PRELIMINARY

FEATURES

- Access times of 55, 70, 85 ns
- Built in decoupling capacitors for low noise operation
- Organized as 32K x 32
- Low power CMOS
- TTL Compatible Inputs and Outputs
- Packaging
  66 pin PGA type 1.09 inch square maximum
- Ultra-violet Erasable
- Programming Voltage Vpp=12.75 ± 0.25V
- Common Data Imputs and Outputs

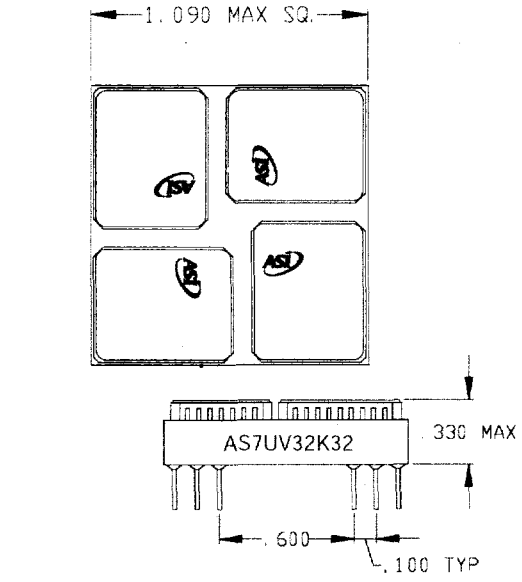


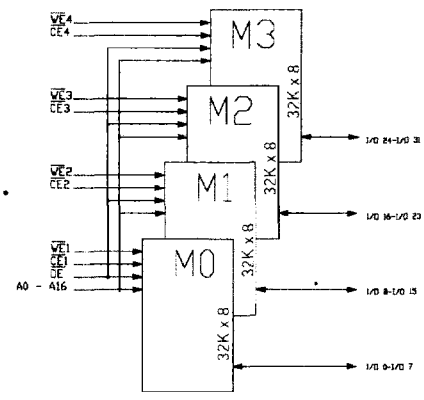
GENERAL DESCRIPTION

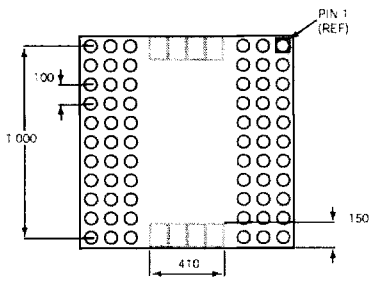
The AS7UV32K32 is a 768 Kilobit CMOS UVEPROM Module Organized as 32Kx32 user configurable to 64K x 16 and 128K x 8. The AS7UV32K32 achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

These advanced features make ASI modules ideally suited for military applications.

The AS7UV32K32 module is constructed using a 1.09 inch square ceramic pin grid array substrate. This compact layout reduces space requirements for board assembly to a minimum.







PIN CONFIGURATION (TOP VIEW)

I/O8	1	A14	12	I/O15	23		I/O24	34	VCC	45	I/O31	56
I/O9	2	$\overline{CE2}$/PGM	13	I/O14	24		I/O25	35	$\overline{CE4}$/PGM	46	I/O30	57
I/O10	3	GND	14	I/O13	25		I/O26	36	A14	47	I/O29	58
A13	4	I/O11	15	I/O12	26		A6	37	I/O27	48	I/O28	59
A14	5	A10	16	$\overline{OE}$	27		A7	38	A3	49	AO	60
NC	6	A11	17	NC	28		NC	39	A4	50	A1	61
NC	7	A12	18	A14	29		A8	40	A5	51	A2	62
NC	8	VCC	19	I/O7	30		A9	41	A14	52	I/O23	63
I/O0	9	$\overline{CE1}$/PGM	20	I/O6	31		I/O16	42	$\overline{CE3}$/PGM	53	I/O22	64
I/O1	10	NC	21	I/O5	32		I/O17	43	GND	54	I/O21	65
I/O2	11	I/O3	22	I/O4	33		I/O18	44	I/O19	55	I/O20	66

ABSOLUTE MAXIMUM RATINGS*

Voltage of Vcc Supply Relative to Vss.....-0.6V to +7V
Storage Temperature.....-65°C to +150°C
Voltage on Any Pin Relative to Vss.....-0.6V to +7V
Vpp with respect to Vss.....-0.6V to +13V
Junction Temperature**.....+150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow.

Operating Range

Range	Temperature	Vcc
Industrial	-40°C to +85°C	+5V ± 10%
Military	-55°C to + 125°C	+5V ± 10%

DC Read Characteristics Over Operating Range with $V_{PP}=V_{CC}$

Parameter		Symbol	Min	Max	Units	Notes
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High		V_{IH}	2.0	V_{CC}+0.3V	V	4
Input Low		V_{IL}	-0.1	0.8	V	4
High Level Output	I_{OH}=-4ma	V_{OH}	2.4		V	
Low Level Output	I_{OL}=16ma	V_{OL}		0.4	V	
Input Leakage		I_{IL}	-20	+20	µA	
Output Leakage	$V_{OUT}=V_{CC}$ or GND	I_{LO}	-20	+20	µA	
Power Supply Current (CMOS)	Outputs not loaded	I_{CC1}		120	mA	1,3
Power Supply Current (TTL)	Outputs not loaded	I_{CC2}		240	mA	2,3
Standby Current (CMOS)	$\overline{CE}=V_{CC}\pm0.3C$	I_{SB1}		2	mA	1
Standby Current (TTL)	$\overline{CE}=V_{IH}$	I_{SB2}		20	mA	2
V_{PP} Supply Current Programming	$V_{PP}=V_{CC}$	I_{PP}		400mA	µA	
V_{PP} Supply Current Read		V_{PPR}	V_{CC}-.4	V_{CC}	V	

AC Read Characteristics Over Operating Range, with $V_{PP} = V_{CC}$

Parameter	Symbol	55ns		70ns		85ns		Units	Notes
		Min	Max	Min	Max	Min	Max		
Address to output delay	t_{ACC}		55		70		85	ns	
$\overline{CE}$ to output delay	t_{CE}		55		70		85	ns	
$\overline{CE}$ to output delay	t_{OE}		25		30		35	ns	
Output disable to output float	t_{ODF}		25		30		35	ns	
Address to output hold	t_{AOH}	0		0		0		ns	

Capacitance[5]

(T_A=25°C;V_{CC} = 5V ± 10%f = 1MHz unless otherwise noted)

Parameter	Symbol	Max	Units	Notes
Input Capacitance	C_{I1}	24	pF	4
Output Capacitance	C_O	16	pF	4
V_{PP} Capacitance	C_{VPP}	100	pF	4

DC Characteristics (Programming) [6,7,8]

(T_A=25° ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

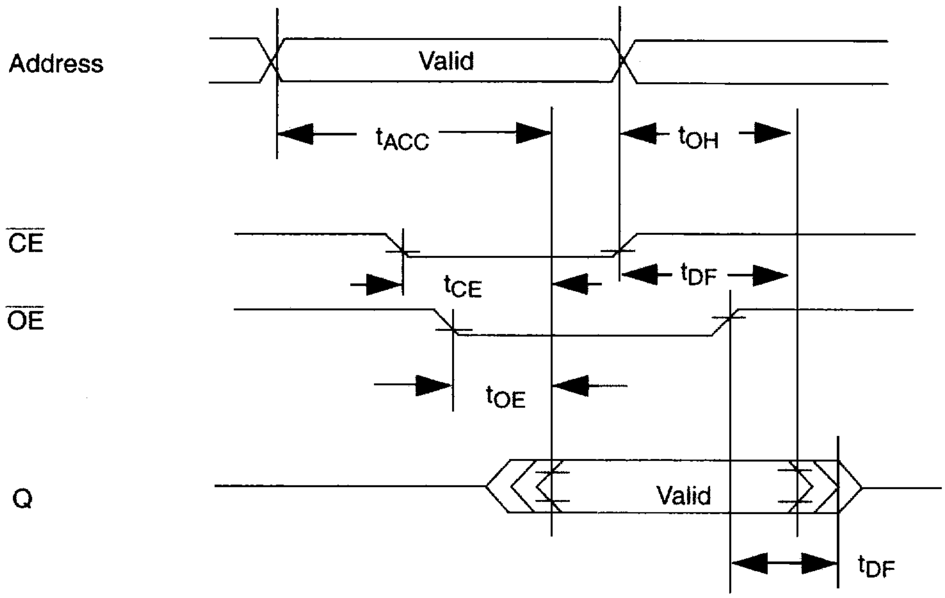
Parameter		Symbol	Min	Max	Units	Notes
V_{PP} Supply Current	$\overline{CE}$/PGM=V_{IL}	I_{PP}		240	mA	
Vcc Supply Current		Icc		140	mA	4
Output Low Voltage	IOL=16mA During verify	V_{OLV}		0.4	V	
Output High Voltage	IOM=-4mA During verify	V_{OHV}	2.4		V	

AC Characteristics (Programming) (6,7,8)

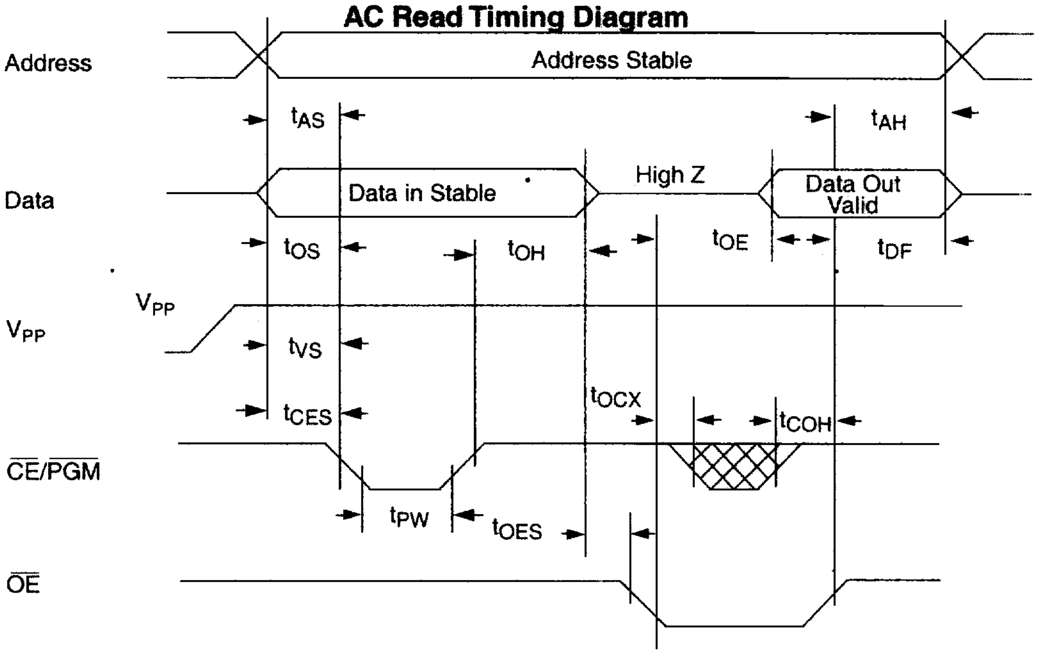
(T_A=25° ± 5°C, V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 ± 0.25 V)

Parameter	Symbol	Min	Type	Max	Units	Notes
Address setup time	t_{AS}	2		240	µs	
$\overline{CE}$ high to $\overline{OE}$ high	t_{COH}	2		140	µs	
Output enable setup time	t_{OES}	2		0.4	µs	
Data setup time	t_{OS}	2			µs	
Address hold time	t_{OS}	0			µs	
Data hold time	t_{OS}	2			µs	
Chip disable to output float delay	t_{DF}	0		130	ns	
Data valid from output enable	t_{DOE}			130	ns	
Vpp setup time/$\overline{CE}$ setup time	t_{VS}/t_{CES}	2			µs	
PGm pulse width	t_{PW}	100		200	µs	
$\overline{OE}$ low to $\overline{CE}$ "don't care"	t_{OCX}	2			µs	

Note:
1. CMOS inputs GND ± 0.3V or V_{CC} ± 0.3V
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} > 2.0V$
3. Add 3mA/MHz for AC power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and or tester noise.
   Do not attempt to test these values without suitable equipment.
5. This parameter is only sampled and is not 100% tested.
6. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7. V_{PP} must not be greater than 13 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
8. During power up the PGM pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.
9. User must tie externally Do-D7, D8-D15, D16-D24 to use 8 bit operation.



AC Read Timing Diagram



Programming Waveform