

1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The WD33C93B, a MOS/LSI device implemented in Western Digital's CMOS process, operates from a single 5-volt supply and is available in either a 44-pin chip carrier or a 40-pin dual-in-line package. All inputs and outputs are TTL-compatible.

The WD33C93B is intended for use in systems which interface to the Small Computer System Interface (SCSI) Bus. The WD33C93B can operate in both the initiator (typically, a Host computer system) and the target (typically, a peripheral device) SCSI bus roles.

When used in the Host system, the WD33C93B interfaces to both the Host bus and the SCSI bus. To perform a SCSI operation, the Host processor issues a command to the WD33C93B to select the desired target. The WD33C93B then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a device with higher priority, it continues trying and notifies the Host when it has succeeded by generating an interrupt. At this point, the WD33C93B is operating in the initiator role. When the peripheral requests a SCSI command from the Host, the WD33C93B receives the request and generates another interrupt to the Host. The Host responds to this interrupt by issuing a "Transfer Info" command and supplying SCSI command bytes to the WD33C93B. The WD33C93B transfers the SCSI command to the peripheral and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The WD33C93B also offers high-level, Select-and-Transfer commands which eliminate the interrupt handling otherwise required between each SCSI bus phase.

When the WD33C93B is used in a peripheral system, the WD33C93B operates primarily in a target role. It interfaces with a local processor and the SCSI bus in this environment just as it does when used in a Host adapter. The target-role command set enables the WD33C93B to request each SCSI bus phase individually or to sequence

the SCSI bus phases automatically through the use of combination commands.

The WD33C93B has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-off mode for standard SCSI applications.

1.2 FEATURES

- Implements full SCSI bus features: arbitration, disconnect, reconnect, parity generation and checking on both data ports, soft reset, and synchronous data transfers.
- Includes 48 mA drivers for direct connection to the SCSI bus.
 - Data Bus pins ($\overline{\text{SDB}}\ 0-7$ and $\overline{\text{SDP}}$) utilizes active negation drivers for better noise immunity.
 - $\overline{\text{REQ}}$ and $\overline{\text{ACK}}$ pins have 57mA active negation drivers to accommodate higher current terminators.
- Includes a high-performance SCSI bus receiver to afford 800 mV (typical) of hysteresis to reject most reflection induced noise.
- Operates in both initiator and target roles.
- Synchronous offset selectable from 1 to 12 bytes.
- Programmable time-out for selection and reselection.
- Support for SCSI-2 features:
 - Synchronous transfer rates up to 10 MB/s for Fast SCSI transfers; up to 5 MB/s for standard SCSI transfers.
 - Select-And-Transfer, Reselect-And-Transfer, and Wait-For-Select-And-Receive commands provide support for queue tag messages and target routine identify messages.
- Special Translate Address command performs the Logical-to-Physical address mapping.
- Combination commands greatly reduce interrupt-handling responsibilities.
- Compatible with most microprocessors

through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature.

- Burst data transfers up to 4096 bytes.
- Data transfer options include programmed I/O, single-byte DMA, burst (multibyte) DMA, or direct bus access (WD bus) transfers.
- Improved host interface timings to support faster CPUs.
- Single +5 V supply.
- Available in 44-pin chip carrier or 40-pin DIP.
- Low-power CMOS design.

1.3 DIFFERENCES BETWEEN THE WD33C93A AND WD33C93B

The WD33C93B delivers the same functionality as the WD33C93A as well as additional features to support SCSI-2 and improve system performance. Unless the device is configured with the RAF bit in the Own ID register set, the WD33C93B is completely backward-compatible to the WD33C93A. Consequently, in most applications, it may replace the WD33C93A with no modification to the hardware or the firmware.

The WD33C93B has grouped several recently added features of the WD33C93A with two WD33C93B-only enhancements into a mode enabled by configuring the device with the RAF bit set. The first two features---the loading of the microcode revision on a soft reset condition and the aborting of a target Receive command upon the detection of the SCSI Attention condition or of a parity error---existed in the WD33C93A design. The WD33C93B design has added to this mode the ability to detect possible data corruption and unexpected disconnects from the SCSI bus when operating as a target.

To support SCSI-2, the combination commands Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive optionally send or receive Queue-tag messages at appropriate points in the SCSI bus sequence. The Host via two bits in the Destination ID register and the newly added Queue Tag register provides information which the first two commands use to generate and check these messages. Wait-for-

Select-and-Receive, through the same locations, relays information to the Host regarding the type of Queue-tag message received, including whether the initiator sent a message or not, and the actual queue tag.

These commands also support the LUNTAR bit in the Identify message. By setting the corresponding bit in the Target LUN register, the Host enables the Select-And-Transfer and Reselect-And-Transfer commands to send an Identify message for a target routine. In the case of Select-And-Transfer, setting this bit also enables the WD33C93B to accept automatically an Identify message with the LUNTAR bit set. The Host also has the option to let the Wait-for-Select-and-Receive command receive a target routine Identify message and proceed to the next phase or to interrupt the Host so that it may reject the message when the application does not support target routines.

The last new feature pertaining to SCSI-2 relates to Fast SCSI. When the WD33C93B has an input clock between 16 MHz and 20 MHz, by controlling the Fast SCSI Select (FSS) bit in the Synchronous Transfer register, the Host can select between normal synchronous transfers which reach a maximum transfer rate of 5 MB/s and Fast synchronous transfers with a peak rate of 10 MB/s on both the SCSI and Host DMA interfaces.

Another addition to the WD33C93B is the FIFO Full/Empty (FFE) bit in the Auxiliary Status register to be used primarily during polled I/O transfers. As its name suggests, this bit reflects the full or empty state of the FIFO depending on the direction of the transfer. If the Host is writing data to the FIFO, the WD33C93B sets this bit when the FIFO is empty, indicating that the Host may write up to 12 bytes to the FIFO without having to poll the DBR bit before writing each byte. Similarly, when the Host is reading data from the FIFO, the WD33C93B sets this bit when the FIFO is full, indicating that the Host may read the DATA register twelve times without polling DBR before each read. Some restrictions do apply when using this bit.

The final addition to the WD33C93B is the usage of Active Negation Drivers. In order to support fast SCSI (10 MB/s) transfer without increasing the

signal reflection problem, the data pins (\overline{SD} 0-7, \overline{SDP}) and \overline{REQ} , \overline{ACK} pins utilizes Active Negation Drivers, instead of Wired-OR type drivers that came with the WD33C93A. Other SCSI bus pins still have wired-OR type drivers.

Active Negation driver can actively pull up the high (negation) level as well as driving it low (assertion) level, it can more readily control rise/fall time and negation level. Wired-OR type drivers does not control the negation level and rise time. Active negation drivers can source more current to the bus to help bus terminators to reduce the reflection problem.

Combined with high-performance, Schmit trigger receivers on all SCSI bus pins, the WD33C93B ensures a more reliable, high-performance operation.