PICTURE-IN-PICTURE CONTROLLER (PIPCO)

GENERAL DESCRIPTION

The SAA9068 is a controller for picture-in-picture applications. The PIPCO receives time multiplexed YUV data from an external analogue-to-digital converter (ADC) or from the Digital Vertical Filter (SAA9069). The device provides YUV data, via an internal digital-to-analogue converter (DAC), to the external filters. The device automatically detects the 50/60 Hz acquisition. Picture data is stored in an external 10 k by 8-bit SRAM. The device also produces the control signal for the SAA9069 (DVF). All features of the PIPCO are software controlled via an I^2C bus.

Features

- Automatic detection of acquisition signals
- Automatic detection of display signals
- The following features are software controlled via an I^2C bus:
  PIP ON/OFF
  border colour, one out of eight
  freeze PIP
  PIP top or bottom of screen
  PIP left or right of screen
  blank PIP
- Y-delay to compensate for delay differences in the pre-filters

QUICK REFERENCE DATA

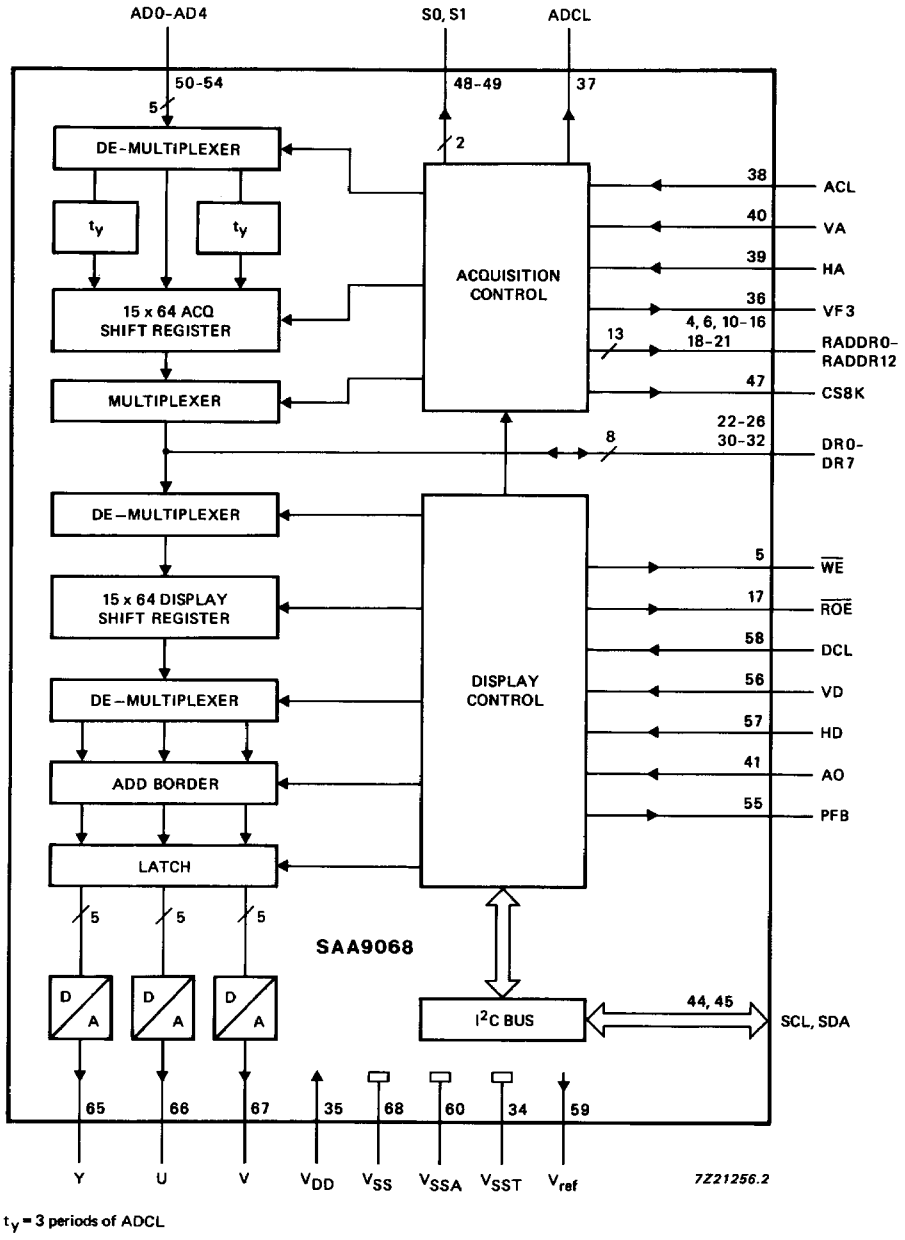
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	−0,5	–	7,0	V
Input voltage range	note 1	V_I	−0,5	–	V_{DD}+0,5	V
Maximum input current		I_{IM}	–	–	±10	mA
Maximum output current		I_{OM}	–	–	±10	mA
Inputs						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	V_{DD}	V
Input leakage current	T_{amb} = 25 °C	$\pm I_I$	–	–	1	μA
Outputs	except analogue outputs					
Output voltage LOW	I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,8 mA	V_{OH}	V_{DD}−0,4	–	V_{DD}	V

Note to the Quick Reference Data

1. V_{DD} + 0,5 V must not exceed 7,0 V

PACKAGE OUTLINE

68-lead plastic leaded chip-carrier (SOT188).



t_y = 3 periods of ADCL

Fig. 1 Block diagram.

DEVELOPMENT DATA

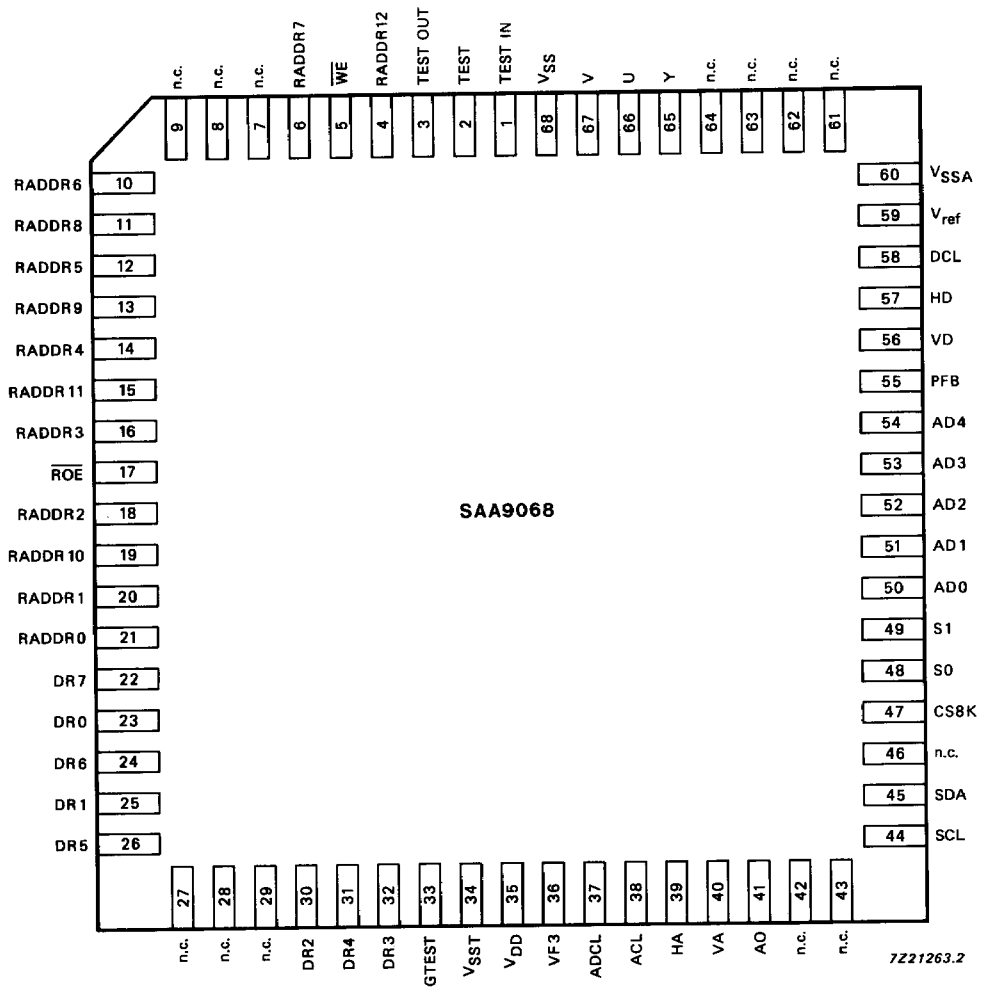


Fig. 2 Pinning diagram.

PINNING

pin	mnemonic	description
Power supplies		
34	V_{SST}	ground for dynamic shift registers
35	V_{DD}	positive supply voltage
60	V_{SSA}	ground for digital-to-analogue converters
68	V_{SS}	ground (0 V)
Inputs		
1	TEST IN	data input for testing the DAC
2	TEST	when HIGH, test mode for DAC enabled
33	GTEST	when LOW GTEST returns all memory elements to a known state, except for line memories
38	ACL	acquisition clock, typ. 10,9 MHz
39	HA	start of line in acquisition mode
40	VA	start of field in acquisition mode
41	A0	programming of I^2C bus slave address
50 to 54	AD0 to AD4	YUV data stream from ADC or SAA9069
56	VD	start of field in display mode
57	HD	start of line in display mode
58	DCL	display clock, typ. 15,8 MHz
Outputs		
3	TEST OUT	test data to DAC
4	RADDR12	SRAM address output
5	$\overline{WE}$	write enable (active LOW)
6	RADDR7	SRAM address output
10	RADDR6	SRAM address output
11	RADDR8	SRAM address output
12	RADDR5	SRAM address output
13	RADDR9	SRAM address output
14	RADDR4	SRAM address output
15	RADDR11	SRAM address output
16	RADDR3	SRAM address output
17	$\overline{ROE}$	RAM output enable (active LOW)
18	RADDR2	SRAM address output
19	RADDR10	SRAM address output
20	RADDR1	SRAM address output
21	RADDR0	SRAM address output
36	VF3	line selection to SAA9069
37	ADCL	acquisition clock signal (ACL/2) to ADC or SAA9069
47	CS8k	chip select for 8 k SRAM
48 to 49	S0 and S1	Y, U and V selection signal to analogue switch or SAA9069
55	PFB	picture-in-picture fast blanking
Inputs/outputs		
22 to 26, 30 to 32	DR0 to DR7	data to and from SRAM
44	SCL	I^2C bus clock
45	SDA	I^2C bus data signals

Analogue outputs

59	V_{ref}	voltage reference level for DAC
65	Y	analogue video signal from 5-bit DAC
66	U	analogue video signal from 5-bit DAC
67	V	analogue video signal from 5-bit DAC

Others

7 to 9, 27 to 29, 42, 43, 62 to 64	n.c.	not internally connected

FUNCTIONAL DESCRIPTION (see Fig. 1)

The YUV data stream is converted from analogue-to-digital data by the 5-bit ADC, this data is then stored in an acquisition line memory every third line. When enabled by the display section of the PIPCO, the data is transferred to the external SRAM. Data from the SRAM is transferred to the display line memory after which it is converted from digital to analogue by the DAC.

I²C bus (SDA; SCL)

The I²C bus provides bidirectional 2-line communication between different ICs or modules. The SDA is the serial data line; SCL is the serial clock line. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C bus format (slave address and receiver formats)

All 8 bits of the subaddress have to be decoded by the device. After power-on reset all control bits are set to zero. This device does not respond to the general call address.

0	0	1	0	0	1	A0	0

Fig. 3 Slave address.

DETAILED INFORMATION ON I²C BUS SPECIFICATION IS AVAILABLE ON REQUEST.

Table 1 Data byte format

	function							
	D7	D6	D5	D4	D3	D2	D1	D0
control	PIPON	STILL	BLPIP	TOP	LEFT	BOC2	BOC1	BOC0

Table 2 Definition of bits D7 to D3

bit	definition
PIPON	PIPON = 1, picture-in-picture is ON PIPON = 0, picture-in-picture is OFF
STILL	STILL = 1, still picture-in-picture STILL = 0, moving picture-in-picture
BLPIP	BLPIP = 1, blanking of picture-in-picture BLPIP = 0, display picture-in-picture
TOP	TOP = 1, picture-in-picture in upper part of screen TOP = 0, picture-in-picture in lower part of screen
LEFT	LEFT = 1, picture-in-picture in left part of screen LEFT = 0, picture-in-picture in right part of screen

Table 3 Colour reproduction

colour	BOC2	BOC1	BOC0	−U	−V
dark pink	0	0	0	0,00	−0,50
reddish brown	0	0	1	0,25	−0,50
light brown	0	1	0	0,50	−0,50
light purple	0	1	1	−0,25	−0,50
dark grey	1	0	0	0,00	0,00
dark green	1	0	1	0,25	0,00
green	1	1	0	0,50	0,00
medium blue	1	1	1	−0,20	0,00

If a function is not implemented, the bit related to this function is transmitted as a logic 0 and the general call address is not accepted. If no supply voltage is present, inputs SCL and SDA are in a high ohmic state.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	7,0	V
Input voltage range	note 1	V_I	−0,5	V_{DD}+0,5	V
Input current		I_I	−	±10	mA
Output current		I_O	−	±10	mA
Supply current in V_{SS}		I_{SS}	−	60	mA
Supply current in V_{DD}		I_{DD}	−	60	mA
Power dissipation per output		P	−	40	mW
Total power dissipation		P_{tot}	−	300	mW
Storage temperature range		T_{stg}	−55	+ 150	°C
Operating ambient temperature range		T_{amb}	−25	+ 70	°C

Note

1. V_{DD}+0,5 must not exceed 7,0 V.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 5 V ± 5%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply current						
Quiescent current	T_{amb} = 25 °C; all inputs to V_{DD} or V_{SS}	I_{DD}	–	–	175	μA
Inputs						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	V_{DD}	V
Input leakage current	T_{amb} = 25 °C; except GTEST	$\pm I_I$	–	–	1	μA
Input leakage current	GTEST	$\pm I_I$	–	–	30	μA
Outputs	except analogue outputs					
Output voltage LOW	I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,8 mA	V_{OH}	V_{DD}–0,4	–	V_{DD}	V
Analogue outputs	Y, U, V at output load = 22 kΩ					
Output voltage LOW		V_{OL}	0,80	–	1,45	V
Output voltage HIGH		V_{OH}	3,75	–	4,75	V
Output level n+1 (step)	note 1	V_n	level n	level n + V_s	level n + $2V_s$	V
Output voltage HIGH to output voltage LOW with 1 kΩ load		V_{OH}-V_{OL}	1,75	1,95	2,15	V
Voltage reference						
Output voltage	V_{DD} = 5 V	V_O	0,7	–	1,3	V

Note to the DC characteristics

1. $V_s = \frac{V_{OH}-V_{OL}}{31}$

AC CHARACTERISTICS

V_{DD} = 5 V ± 5%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance		C_i	–	–	3	pF
AD0 - AD4 to ACL	Fig. 8					
data set-up time		$t_{SU;DAT}$	30	–	–	ns
data hold time		$t_{HD;DAT}$	10	–	–	ns
DR0 - DR7 to DCL	Fig. 7					
data set-up time		$t_{SU;DAT}$	30	–	–	ns
data hold time		$t_{HD;DAT}$	10	–	–	ns
HA, HD, VA, VD	notes 1 to 4					
ACL	note 5					
pulse width LOW		t_{WL}	25	–	–	ns
pulse width HIGH		t_{WH}	25	–	–	ns
rise time		t_r	–	–	7	ns
fall time		t_f	–	–	7	ns
frequency		f_{ACL}	–	10,9	–	MHz
DCL	note 6					
pulse width LOW		t_{WL}	18	–	–	ns
pulse width HIGH		t_{WH}	18	–	–	ns
rise time		t_r	–	–	4	ns
fall time		t_f	–	–	4	ns
frequency		f_{DCL}	–	15,8	–	MHz
Outputs	DCL = 15,8 MHz					
Load capacitance		C_L	–	–	20	pF
DCL to DR0 - DR7 propagation delay	Fig. 6	t_d	10	–	135	ns
DCL to RADDR0 - RADDR12 and CS8K propagation delay	Fig. 6	t_d	0	–	70	ns
DCL to $\overline{ROE}$ propagation delay	Fig. 6	t_d	0	–	150	ns
DCL to $\overline{WE}$ (falling edge) propagation delay	Fig. 6	t_d	70	–	105	ns
DCL to $\overline{WE}$ (rising edge) propagation delay	Fig. 6	t_d	195	–	235	ns
DCL to PFB propagation delay	Fig. 7	t_d	0	–	50	ns
ACL to ADCL propagation delay	Fig. 8	t_d	0	–	115	ns
ACL to S0 and S1 propagation delay	Fig. 8	t_d	0	–	115	ns

Notes to the AC characteristics

1. Pulse width HA (typ. 250 ns): the first sample of a line occurs after approximately 124 periods of ACL (counted on the negative edge of HA). The internal horizontal acquisition off-set value is chosen in such a way that ACL = 10,9 MHz, when this condition is satisfied the acquired picture is centralized within the PIP. The off-set value is dependent upon the acquisition frequency, 50 Hz or 60 Hz (124 ACL periods of 50 Hz and 108 ACL periods of 60 Hz). If the pulse width of HA increases, the acquired picture will shift to the left within the PIP picture (see Fig. 4).

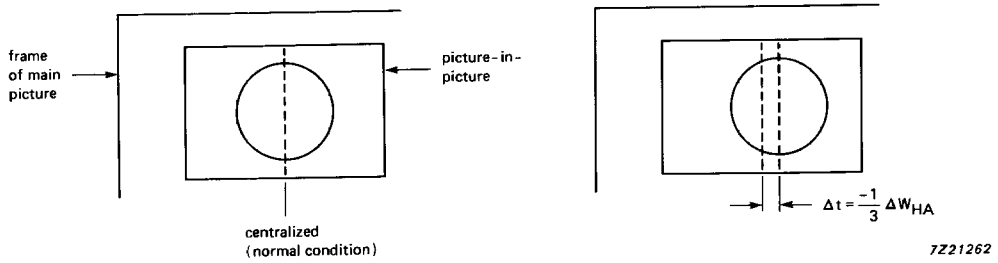


Fig. 4 PIP position; (a) ACL = 10,9 MHz, (b) $\Delta t = -1/3\ \Delta W_{HA}$.

2. Pulse width HD (typ. 250 ns): the first sample of a line is displayed after XXX periods of DCL with respect to the negative edge of HD. The internal horizontal display off-set is fixed in the hardware and depends upon the frequency (50 Hz or 60 Hz) and the right/left position of the display.
   The following values are implemented:

   - 50 Hz; position of display, right; t = 574 periods of DCL
   - 50 Hz; position of display, left; t = 134 periods of DCL
   - 60 Hz; position of display, right; t = 558 periods of DCL
   - 60 Hz; position of display, left; t = 126 periods of DCL

   If the pulse width of HD increases the distance between screen border and the left border of the PIP will enlarge and the picture will shift to the right. The width of the complete PIP, inclusive of border, is 268 clock pulses.

3. VA pulse width, minimum 8 pulses of ACL.

4. VD pulse width, minimum 5 pulses of DCL.

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5. If ACL = k x 10,9 MHz, the effects are shown in Fig. 5:
   - if $k > 1$ then the acquired picture will be expanded horizontally and its centre will shift to the right.
   - if $k < 1$ then the acquired picture will be reduced horizontally and its center will shift to the left.

Fig. 5 PIP geometry; (a) $k > 1$, (b) $k < 1$.

6. DCL: if DCL $\neq$ 15,8 MHz but DCL = k x 15,8 MHz the effects are:
   - all horizontal sizes and values are multiplied by k.

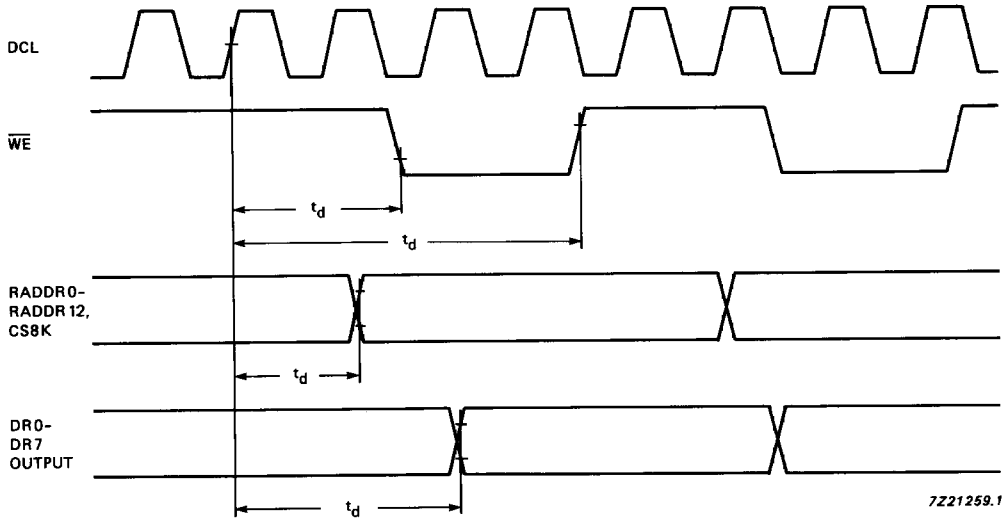

Fig. 6 Data and display clock timing waveform.

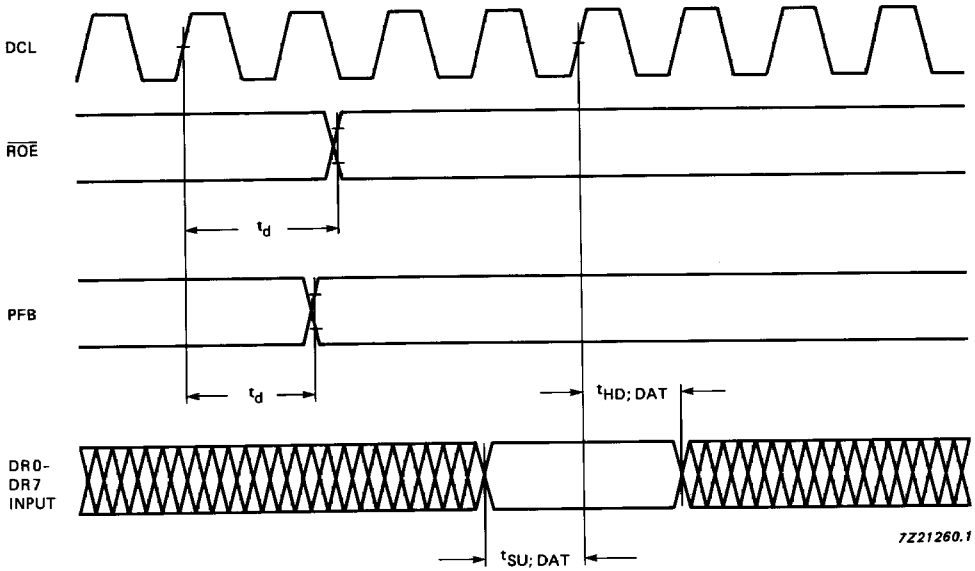

Fig. 7 Data and display clock timing waveform.

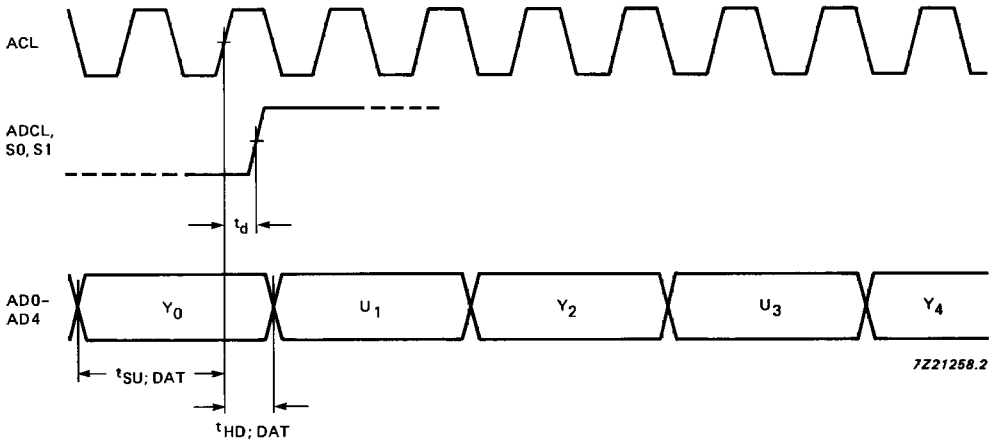

Fig. 8 Input data and acquisition clock waveform.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

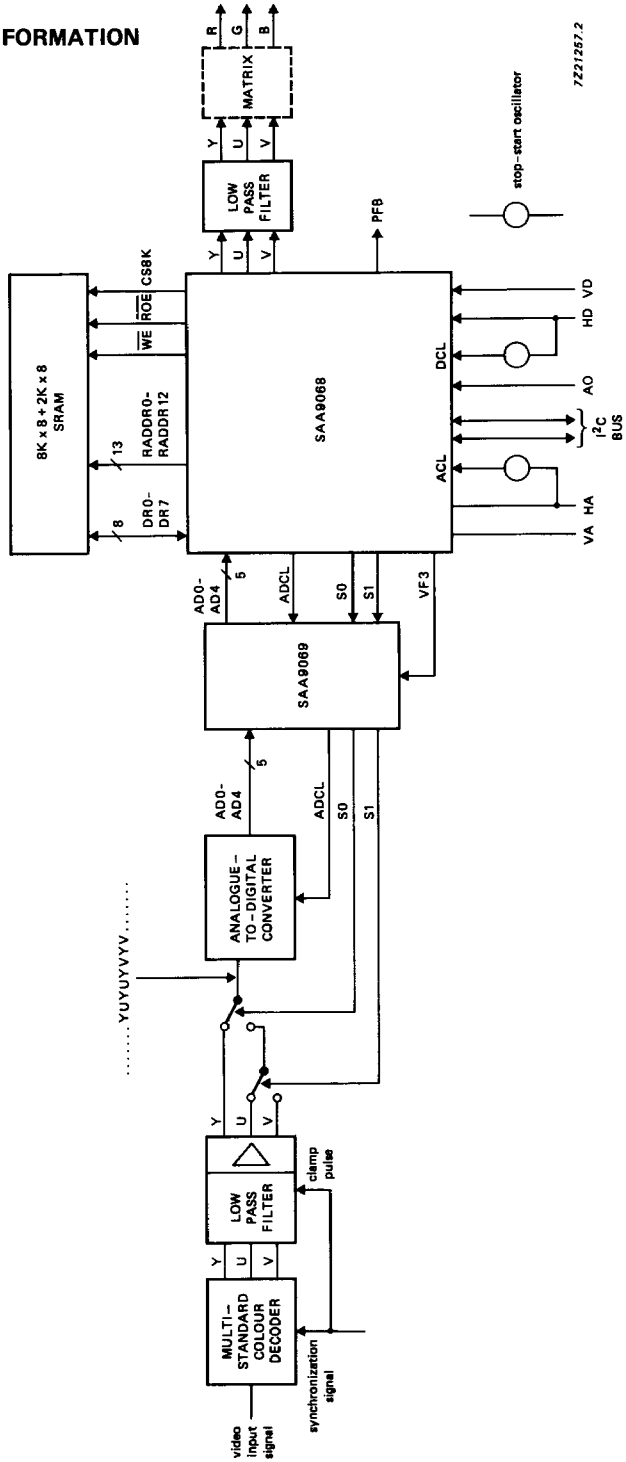

Fig. 9 Application diagram, using SAA9069.

DEVELOPMENT DATA