SED1352F0A

GRAPHICS LCD CONTROLLER

■ DESCRIPTION

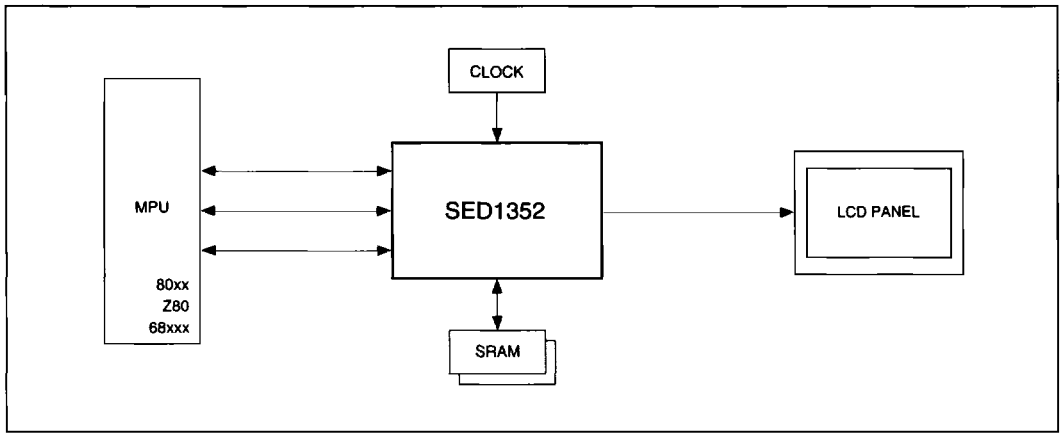
The SED1352 is a high duty cycle, graphic display LCD controller capable of displaying a maximum of 16 levels of gray shade on single and dual scan Liquid Crystal Displays. A 16x4 lookup table is provided to allow remapping of the 16 possible gray shades displayed on the LCD panel. The SED1352 can interface to MC68000 microprocessor, 8/16 bit ISA Bus, and 8/16 bit MPUs with READY (WAIT#) signal with minimum external "glue" logic. This chip can directly control up to 128 Kbytes of static SRAM.

Optimized for cost and power savings, the SED1352 can operate from 2.7 Volt to 5.5 Volt and from 5 Mhz to 25Mhz.

■ FEATURES

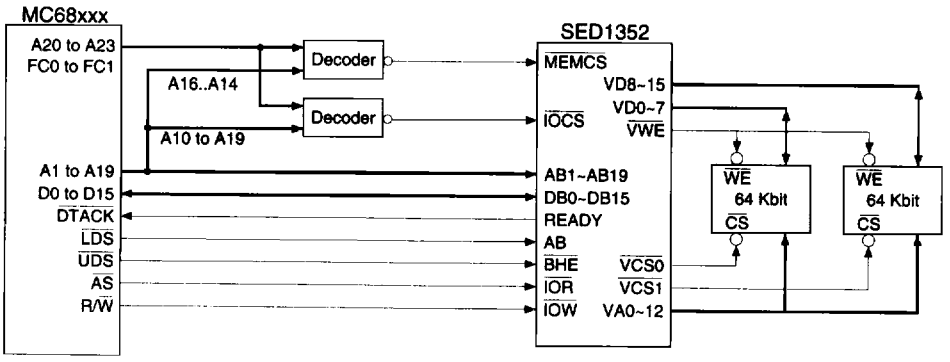
- 16-bit 16 Mhz MC68000 MPU interface
- 8/16-bit ISA data bus interface bus
- 8/16 bit MPU interface controlled by a READY (or WAIT#) signal
- Option to use built-in index register or direct-mapping to access one of fifteen internal registers
- 2-terminal crystal input for internal or external crystal oscillator
- 8/16 bit SRAM interface configurations
- Two software power-save modes
- Low power consumption
- Virtual display support
- Packed pixel mode support
- Display modes:
  - 2 bit/pixel, 4-level gray-scale display
  - 4 bit/pixel, 16-level gray-scale display
- Display memory interface:
  - One 1 Mbit SRAM(64Kx16)
  - One or two 32Kbyte SRAM(s)
  - One or two 8Kbyte SRAM(s)
  - One 8Kbyte and one 32Kbyte SRAM
- LCD panel configurations:
  - Single-panel, single-drive display
  - Dual-panel, dual-drive display
- Maximum number of vertical lines:
  - 1,024 lines (single-panel, single-drive display)
  - 2,048 lines (dual-panel, dual-drive display)
- Split screen display support at single-panel mode
- QFP5-100-S2 package

■ SYSTEM BLOCK DIAGRAM



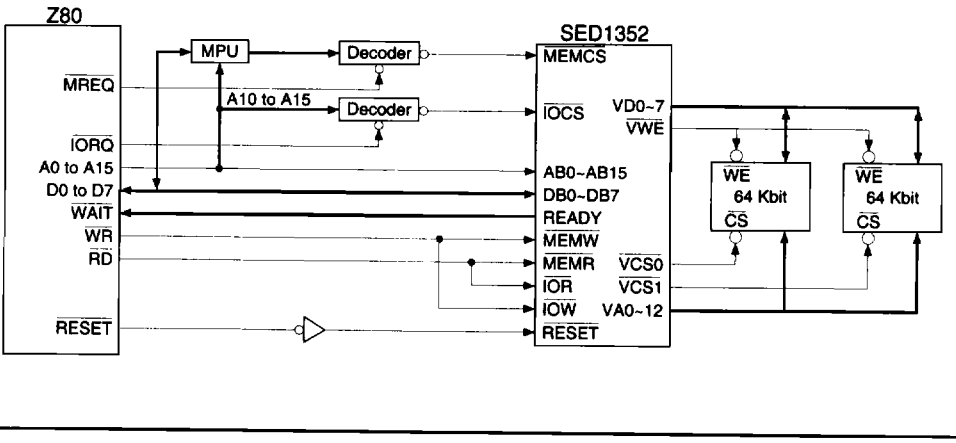
■ INTERFACE OPTIONS

Interface with 16-bit MC68xxx MPU and 16Kbytes SRAM (2 of 8K × 8)



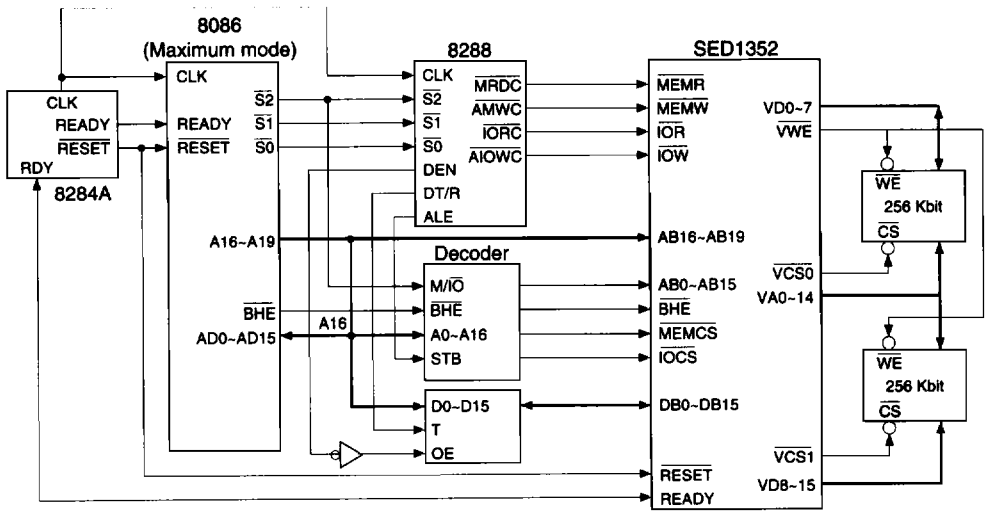
Note: Example implementation, actual may vary.

Interface with 8-bit Z80 MPU and 16Kbytes SRAM (2 of 8K × 8)



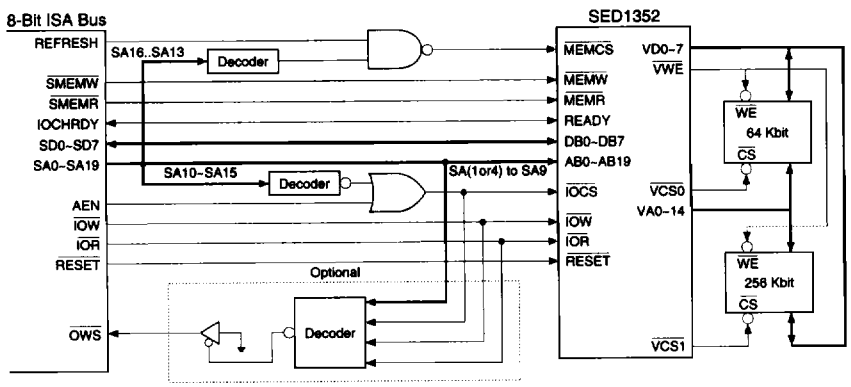
Note: Example implementation, actual may vary.

Interface with 16-bit 8086 MPU and 64Kbytes SRAM (2 of 32K × 8)



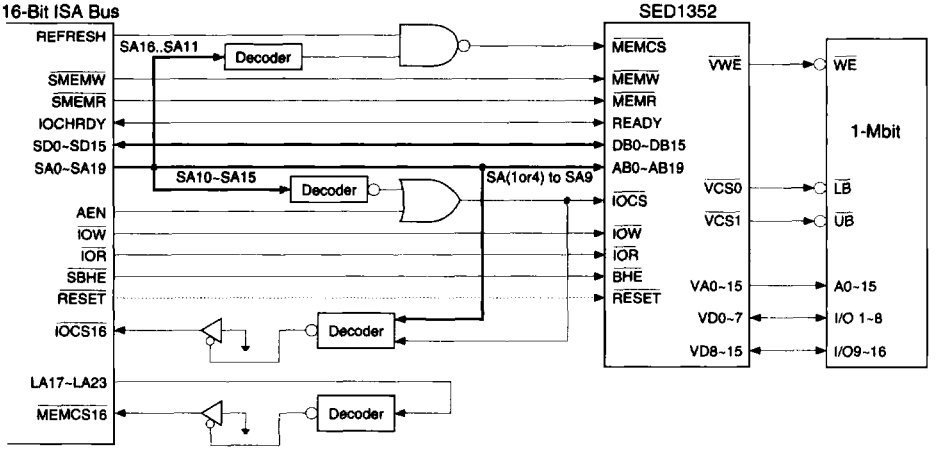
Note: Example implementation, actual may vary.

Interface with 8-bit ISA Bus and 40Kbytes SRAM (1 of 8K × 8 and 1 of 32K × 8)



Note: Example implementation, actual may vary.

Interface with 16-bit ISA Bus and 128Kbytes SRAM (1 of 128K × 8)

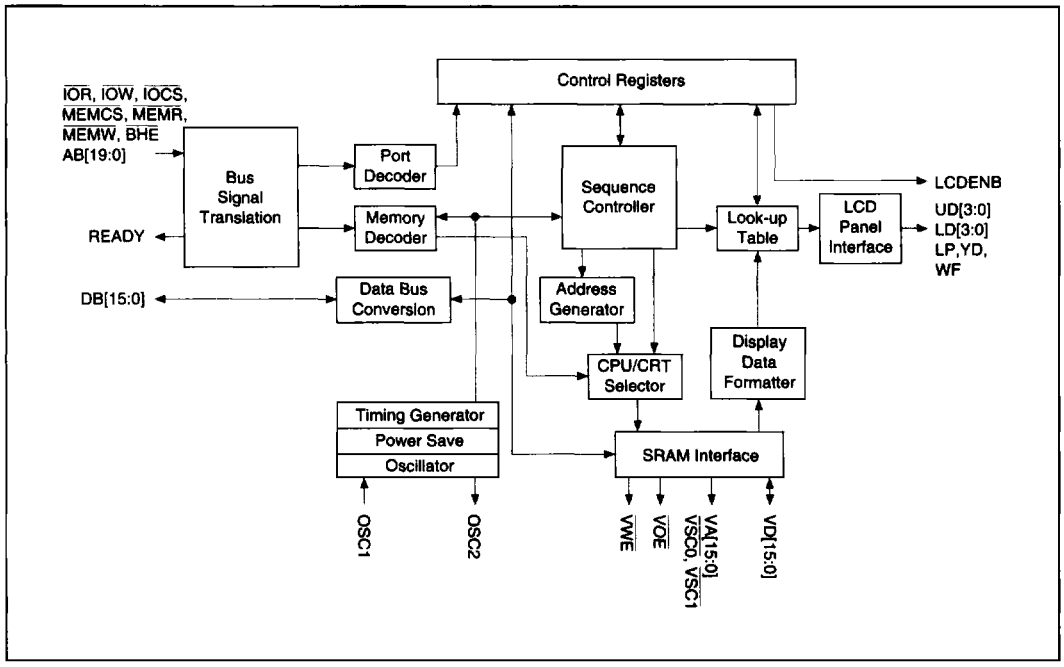


Note: Example implementation, actual may vary.

■ SUPPORTED RESOLUTIONS

Display RAM	Example Display Size		SRAM Type	CPU Interface	SRAM Interface
	4 Grays	16 Grays			
	x y	x y			
8 Kbyte	256 x 128	128 x 128	1 of 8Kx8	8-bit	8-bit
16 Kbyte	320 x 200	200 x 160	2 of 8Kx8	8-bit	8-bit/16-bit
				16-bit	16-bit
32 Kbyte	512 x 256	256 x 256	1 of 32Kx8	8-bit	8-bit
40 Kbyte	512 x 320	320 x 256	1 of 8Kx8 and 1 of 32Kx8	8-bit	8-bit
64 Kbyte	512 x 512	512 x 256	2 of 32Kx8	8-bit	8-bit/16-bit
				16-bit	16-bit
128 Kbyte	1024 x 512	512 x 512	1 of 64Kx16	16-bit	16-bit

■ BLOCK DIAGRAM



■ DC SPECIFICATIONS

● Absolute Maximum Ratings

Parameters	Symbol	Rating	Units
Supply voltage	V_{DD}	V_{SS} –0.3 to +6.5	V
Input voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	V_{SS} –0.3 to V_{DD} +0.3	V
Ambient temperature	T_A	–55 to 125	°C
Storage temperature	Tstg	–65 to 150	°C
Solder temperature/time	T_{SOL}	260 for 10 sec. max at lead	°C

● Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units
Supply voltage	$V_{DD(1)}$	V_{SS} = 0V	4.5	5.0	5.5	V
Supply voltage	$V_{DD(2)}$	V_{SS} = 0V	2.7	3.0	3.3	V
Input voltage	V_{IN}		V_{SS}	—	V_{DD}	V
Junction temperature	T_j		0	—	115	°C
Operating temperature	T_{OPR}		0	25	70	°C

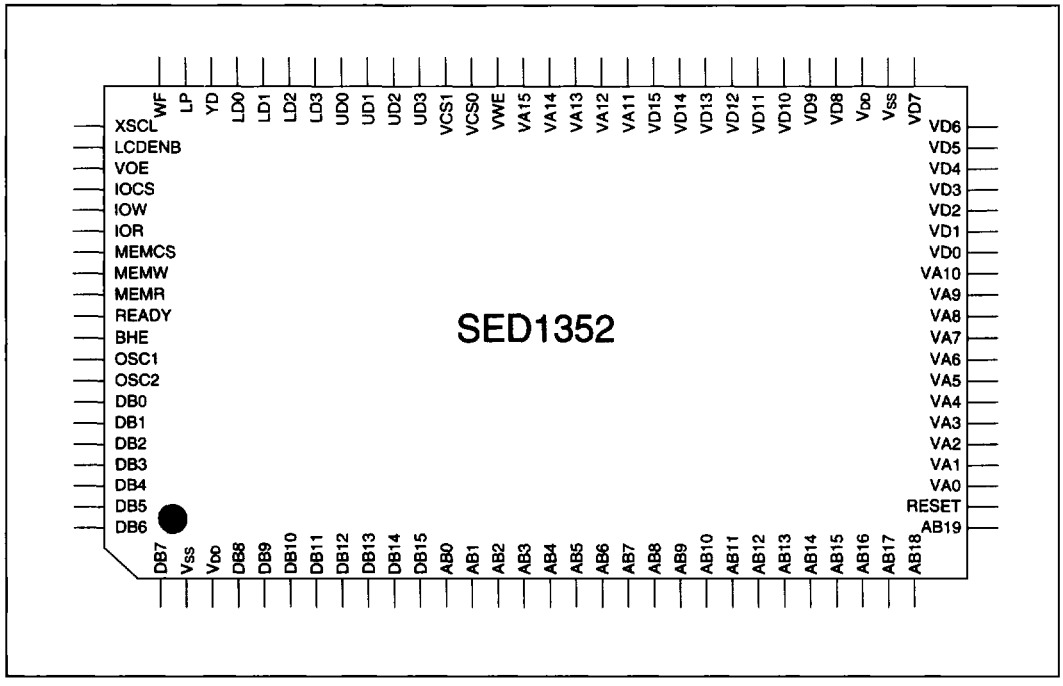
● **Input Specifications**

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units
Low level input voltage CMOS inputs TTL inputs	V_{IL}	V_{DD} = Min			1.0 0.8	V V
Low level input voltage CMOS inputs TTL inputs	V_{IH}	V_{DD} = Max	3.5 2.0			V V
Positive going threshold CMOS Schmitt inputs TTL Schmitt inputs	V_{T+}	V_{DD} = 5.0			4.0 2.4	V V
Negative going threshold CMOS Schmitt inputs TTL Schmitt inputs	V_{T-}	V_{DD} = 5.0	0.8 0.6			V V
Hysteresis voltage CMOS Schmitt inputs TTL Schmitt inputs	V_H	V_{DD} = 5.0	0.3 0.1			V V
Input leakage current	I_{IZ}	V_{DD} = MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	–1		1	µA
Input pin capacitance	C_{IN}			4		pF
Pull down resistance	HR_{PD}	V_{DD} = 5.0 V V_I = V_{DD}	50	100	180	KΩ
Pull down resistance	LR_{PD}	V_{DD} = 3.3 V V_I = V_{DD}	90	180	360	KΩ

● **Output Specifications**

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units
Low level output voltage Type 2 – TS2, CO2, TS2D1 Type 3 – TS3 Type 4 – TS4, OD4	V_{OL}	I_{OL} = 6 mA I_{OL} = 12 mA I_{OL} = 24 mA			V_{SS} + 0.4	V
High level output voltage Type 2 – TS2, CO2, TS2D1 Type 3 – TS3 Type 4 – TS4, OD4	V_{OH}	I_{OL} = –2 mA I_{OL} = –4 mA I_{OL} = –8 mA	V_{DD} – 0.4			V
Output leakage current	I_{OZ}	V_{DD} = MAX V_{OH} = V_{DD} V_{OL} = V_{SS}	–1		1	µA
Output pin capacitance	C_{OUT}			6		pF
Bidirectional pin capacitance	C_{BID}			10		pF

■ SED1352 PIN OUTS



■ PIN DESCRIPTION

Key

A = Analog
I = Input
O = Output
I/O = Bi-directional
P = Power

Bus Interface

Pin Name	Type	Pin #	Description
DB0-DB15	I/O	94 - 100, 1, 4 - 11	These pins are connected to the system data bus. In 8-bit bus mode, DB8-DB15 must be tied to VDD.
AB0	I	12	In MC68000 MPU interface, this pin is connected to the Lower Data Strobe (LDS#) pin of MC68000. In other bus interfaces, this pin is connected to the system address bus.
AB1-AB19	I	13 - 31	These pins are connected to the system address bus.
BHE#	I	91	In MC68000 MPU interface, this pin is connected to the Upper Data Strobe (UDS#) pin of MC68000. In other bus interfaces, this pin is the Bus High Enable Input for use with 16-bit system. In 8-bit bus mode, tie BHE# input to VDD.
IOCS#	I	84	Active low input to select one of fifteen internal registers.
IOW#	I	85	In MC68000 MPU interface, this pin is connected to the R/W# pin of MC68000. This input pin will define whether the data transfer is a read (active high) or write (active low) cycle. In other bus interfaces, this is the active low input to write data into an internal register.
IOR#	I	86	In MC68000 MPU interface, this pin is connected to the AS# pin of MC68000. This input pin will indicate a valid address is available on the address bus. In other bus interfaces, this is the active low input to read data from an internal register.
MEMCS#	I	87	Active low input to indicate the attempt to access the display memory.
MEMW#	I	88	Active low input to write data to the display memory.
MEMR#	I	89	Active low input to read data from the display memory.
READY	O	90	For MC68000 MPU interface, this pin is connected to the DTACK# pin of MC68000 and will be driven low whenever a data transfer is complete. In other bus interfaces, this output is driven low to force the system to insert wait states when needed. READY is released to high-Z after the transfer is completed.
RESET	I	32	Active high input to force all signals to their inactive states.

Display Memory Interface

Pin Name	Type	Pin #	Description
VD0-VD15	I/O	44-51, 54-61	These pins are connected to the display memory data bus. For 16-bit interface, VD0-VD7 are connected to the display memory data bus of even byte addresses and VD8-VD15 are connected to the display memory data bus of odd byte addresses. The output drivers of these pins are placed into a high-Z state when RESET is high. On the falling edge of RESET, the values of VD0-VD15, each with internal pull-down resistor, will be latched into the chip to configure various hardware options.
VA0-VA15	O	33-43, 62-66	These pins are connected to the display memory address bus.
VCS1#	O	69	Active low chip-select output to the second or odd byte address SRAM. See display memory interface section for details.
VCS0#	O	68	Active low chip-select output to the first or even byte address SRAM. See display memory interface section for details.
VWE#	O	67	Active low output used for writing data to the display memory. This pin is connected to the WE# input of the SRAMs.
VOE#	O	83	Active low output to enable reading of data from the display memory. This pin is connected to the OE# input of the SRAMs.

LCD Interface

Pin Name	Type	Pin#	Description
UD3-UD0	O	70 - 73	Upper panel display data for dual panel mode. For single panel mode, these bits are the most significant 4 bits of the 8 bits output data to the panel (PD[4:7]). For 4-bit signel panel mode, these bits are the 4 bits of output data to the panel.
LD3-LD0	O	74 - 77	Lower panel display data for dual panel mode. For 8-bit single panel mode, these bits are the least significant 4 bits of the 8 bits output data to the panel (PD[0:3]). For 4-bit signel panels, these bits are driven 0 (low state).
XSCL	O	81	Display data shift clock. Data is shifted into the LCD X-drivers on the falling edge of this signal.
LP	O	79	Display data latch clock. The falling edge of this signal is used to latch a row of display data in the LCD X-drivers and to turn on the row driver (Ydriver).
WF	O	80	LCD AC-drive signal output.
YD	O	78	Vertical scanning start pulse. A logic '1' on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row driver (Y driver) to indicate the start of the vertical frame.
LCDENB	O	82	LCD enable signal output. It can be used externally to turn off the panel supply voltage and backlight.

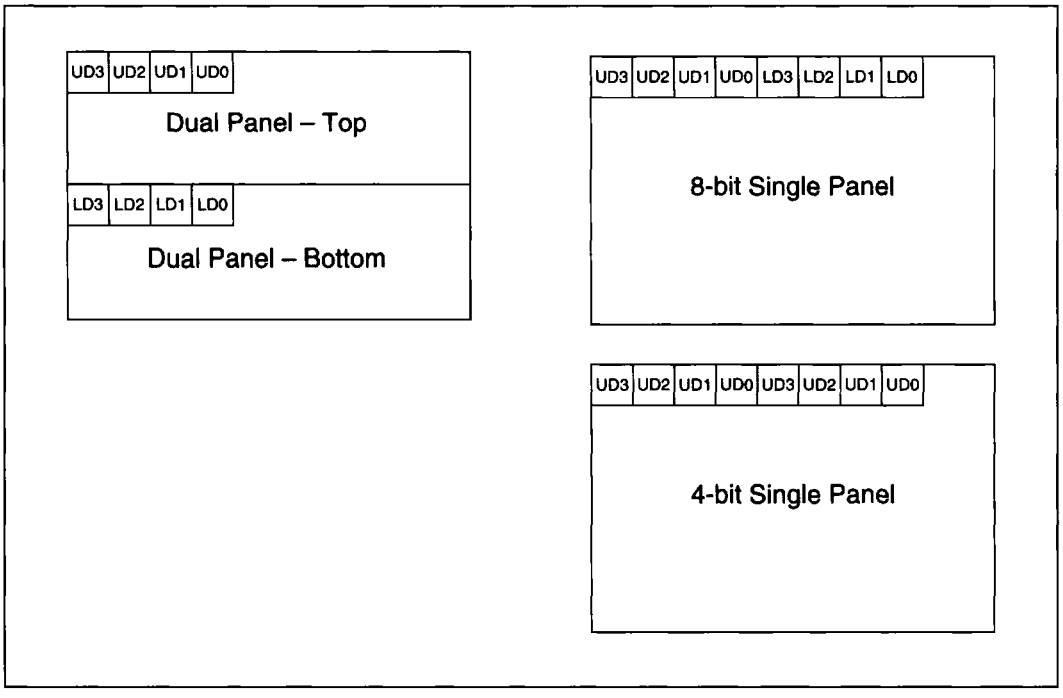
Clock Inputs

Pin Name	Type	Pin#	Description
OSC1	I	92	This pin, along with OSC2 is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
OSC2	O	93	This pin, along with OSC1 is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.

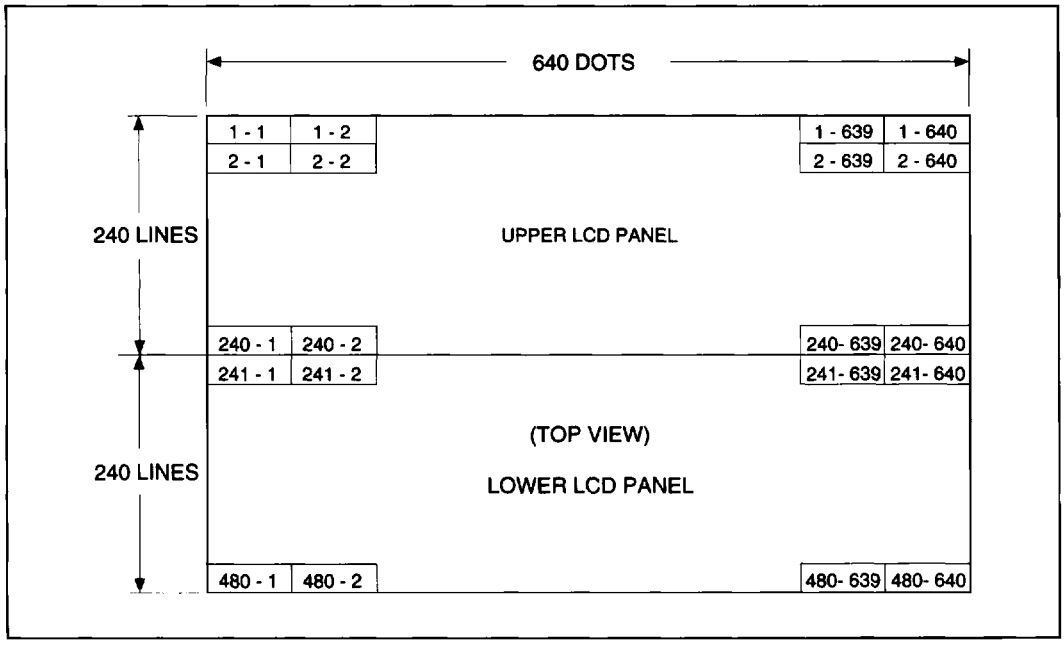
Power Supply

Pin Name	Type	Pin#	Description
V_{DD}	P	3, 53	Voltage supply.
V_{SS}	P	2, 52	Voltage ground.

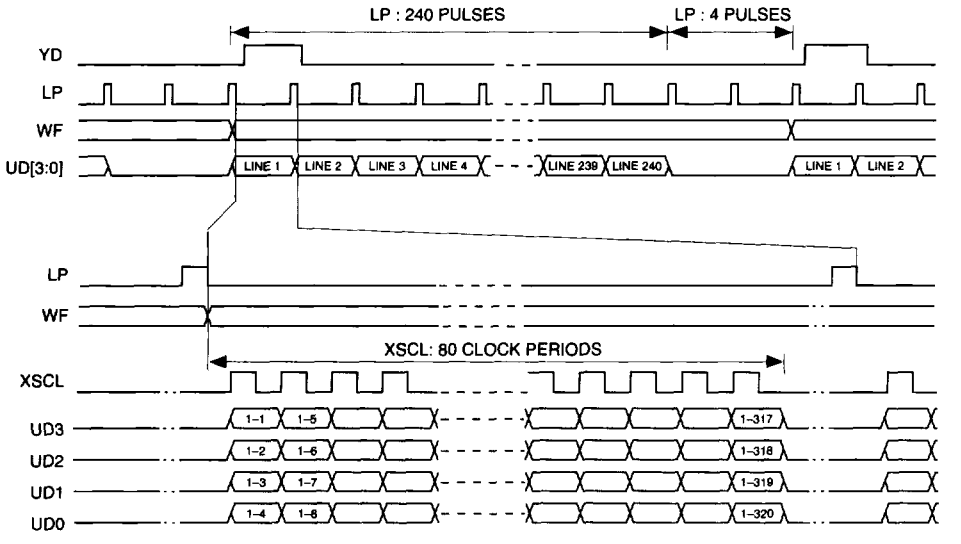
Illustrated below are the display data output which are output from the UD0 to UD3, LD0/UD4 to LD3/UD7 and the display on the panel:



■ LCD PANEL PIXELS

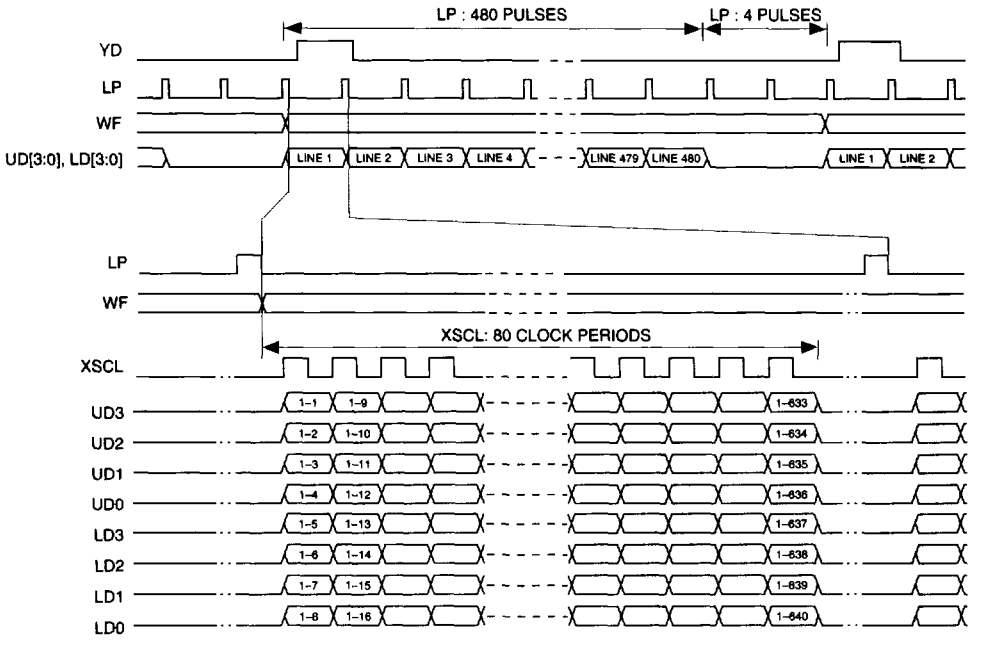


■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE



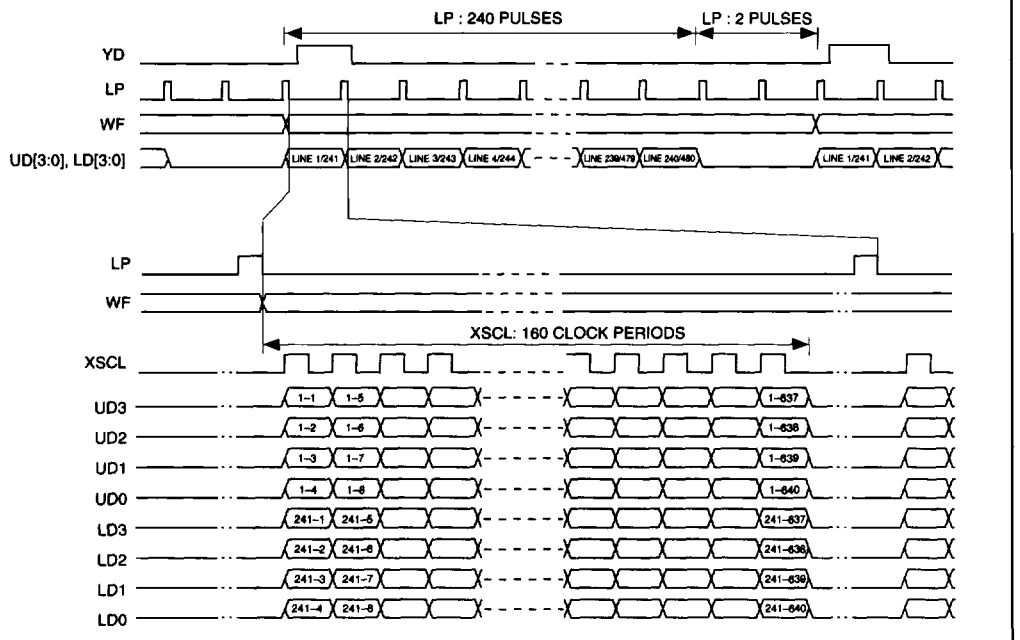
Example timing for 320 × 240 single panel

■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE



Example timing for 640 × 480 panel

■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE



Example timing for 640 × 480 panel

■ PACKAGE DIMENSIONS

QFP5-100-S2 100 pin

Unit: mm